

***RoHS Compliant***

**Compact Flash 4 Series**  
***Specification***

**November 17, 2009**

***Version 1.1***



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## Features:

- **CompactFlash Association Specification Revision 4.1 Standard Interface**
  - 512 bytes per sector
  - ATA command set compatible
  - ATA mode support for up to:
    - PIO Mode-6
    - Multiword DMA Mode-4
    - Ultra DMA Mode-6
- **Capacities**
  - 2, 4, 8, 16, 32 GB
- **Sustained read performance**
  - Up to 50 MB/sec
- **Sustained write performance**
  - Up to 12 MB/sec
- **Flash management**
  - Advanced wear-leveling algorithms to substantially increase longevity of flash media
  - Built-in ECC support for correcting up to 8/15 random single-bit errors per 512-byte sector
  - Read Recovery Technology
  - Power Failure Recovery
  - S.M.A.R.T. Technology
- **NAND Flash Type: MLC**
- **Temperature ranges**
  - Operation: 0°C to 70°C
  - Storage: -40°C to 100°C
- **Support for voltage read and write operations**
  - 3.3 V or 5 V
- **Low power consumption (typical)**
  - Active mode: 95 mA/ 90 mA (3.3 V/ 5 V)
  - Sleep mode: 0.2 mA/ 0.2 mA (3.3 V/ 5 V)
- **Connector Type**
  - 50 pins female
- **Physical Dimensions**
  - 36.4mm x 42.8mm x 3.3mm
- **RoHS compliant**

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## **1. General Description**

Apacer's Compact Flash 4 offers the most reliable and high performance storage which is compatible with CF Type I and Type II device. Unlike the others, Apacer Compact Flash 4 provides solid traceability to ensure all products HW/SW are the same as you qualified.

Apacer's Compact Flash 4 complies with the interfaces, such as the commands, timings, and protocols based on the Compact Flash Specification (CFA standard), and operates as the PC Card ATA interface providing complete PCMCIA - ATA functionality and compatibility. Apacer's Compact Flash 4 is designed for use in Point of Sale (POS) terminals, telecom, IP-STB, medical instruments, surveillance systems, industrial PCs and handheld applications.

### **1.1 Performance-Optimized Controller**

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Compact Flash 4 Controller translates standard CF signals into flash media data and control signals.

#### **1.1.1 FIFO Buffer**

Compact Flash 4 Controller performs as an FIFO buffer to optimize the host's data transfer to and from the flash media for reliable storage via performing data correction and moving data to another block in case of the correctable error.

#### **1.1.2 Error Correction Code (ECC)**

Compact Flash 4 adopts Error Detection Code (EDC) and Error Correction Code (ECC) algorithms which correct up to 8/15 random single-bit errors for each 512-byte block of data.

High performance is achieved through hardware-based error detection and correction.

## 2. Functional Block

Compact Flash 4 Card includes a controller and flash media, as well as the standard Compact Flash interface. Figure 2-1 shows the functional block diagram.

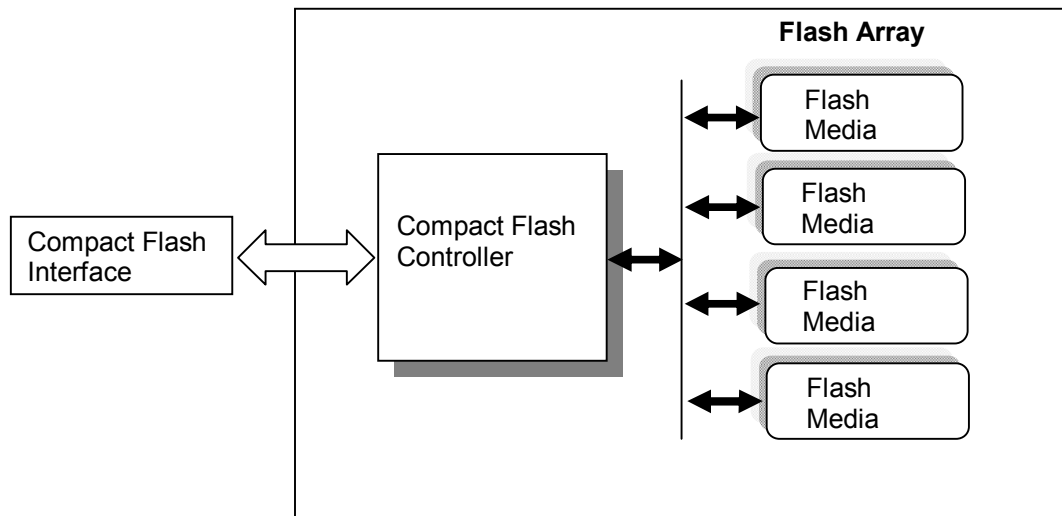


Figure 2-1: Functional block diagram

## 3. Pin Assignments

Table 3-1 lists the pin assignments with respective signal names for the 50-pin configuration. A “#” suffix indicates the active low signal. The pin type can be input, output or input/output.

**Table 3-1:** Pin assignments (1 of 2)

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
1	GND	-	GND	-	GND	-
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	#CE1	I	#CE1	I	#CS0	I
8	A10	I	A10	I	A10 <sup>1</sup>	I
9	#OE	I	#OE	I	#ATA SEL	I
10	A9	I	A9	I	A9 <sup>1</sup>	I
11	A8	I	A8	I	A8 <sup>1</sup>	I
12	A7	I	A7	I	A7 <sup>1</sup>	I
13	VCC	-	VCC	-	VCC	-
14	A6	I	A6	I	A6 <sup>1</sup>	I
15	A5	I	A5	I	A5 <sup>1</sup>	I
16	A4	I	A4	I	A4 <sup>1</sup>	I
17	A3	I	A3	I	A3 <sup>1</sup>	I
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	#IOIS16	O	#IOCS16	O
25	#CD2	O	#CD2	O	#CD2	O
26	#CD1	O	#CD1	O	#CD1	O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O
32	#CE2	I	#CE2	I	#CS1	I
33	#VS1	O	#VS1	O	#VS1	O
34	#IORD	I	#IORD	I	#IORD	I
35	#IOWR	I	#IOWR	I	#IOWR	I
36	#WE	I	#WE	I	#WE	I
37	RDY/-BSY	O	#IREQ	O	INTRQ	O
38	VCC	-	VCC	-	VCC	-
39	#CSEL	I	#CSEL	I	#CSEL	I
40	#VS2	O	#VS2	O	#VS2	O
41	RESET	I	RESET	I	#RESET	I

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**Table 3-1:** Pin assignments (2 of 2)

Pin No.	Memory card mode		I/O card mode		True IDE mode	
	Signal name	Pin I/O type	Signal name	Pin I/O type	Signal name	Pin I/O type
42	#WAIT	O	#WAIT	O	IORDY	O
43	#INPACK	O	#INPACK	O	DMARQ <sup>2</sup>	O
44	#REG	I	#REG	I	DMACK <sup>2</sup>	I
45	BVD2	O	#SPKR	O	#DASP	O
46	BVD1	O	#STSCHG	O	#PDIAG	O
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	-	GND	-	GND	-

1. The signal should be grounded by the host.

2. Connection required when UDMA is in use.

## 4. Capacity Specification

Capacity specification of Compact Flash 4 series is available as shown in Table 4-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

**Table 4-1:** Capacity specifications

Capacity	Total bytes <sup>1,2</sup>	Cylinders	Heads	Sectors	Max LBA
2GB	2,048,901,120	3,970	16	63	4,001,760
4GB	4,110,188,544	7,964	16	63	8,027,712
8GB	8,195,604,480	15,880	16	63	16,007,040
16GB	16,391,208,960	16,383 <sup>3</sup>	16	63	32,014,080
32GB	32,001,048,576	16,383 <sup>3</sup>	16	63	62,502,048

1. Total bytes includes reserved block.

2. Display of total bytes varies from operating systems.

3. Cylinders, heads or sectors are not applicable for these capacities. Only LBA addressing applies

### 4.1 Environmental Specifications

Environmental specification of Compact Flash 4 series follows the MIL-STD-810F standards as shown in Table 4-2.

**Table 4-2:** Environmental specifications

Environment		Specification
Temperature	Operation	0°C to 70°C
	Storage	-40°C to 100°C
Humidity		5% to 95% RH (Non-condensing)
Vibration (Non-Operation)		Sine wave: 10~2000Hz, 15G (X, Y, Z axes)
Shock (Non-Operation)		Half sine wave, Peak acceleration 50 G, 11 ms (X, Y, Z ; All 6 axes)



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## 5. Flash Management

### 5.1 Advanced Wear Leveling

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The goal of advanced wear leveling algorithms is to evenly spread the program and erase cycles on the area of programmed and erased multiple times and the area of programmed one and read multiple times among the available blocks in the flash array.

### 5.2 Read Recovery Technology

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Read Recovery Technology enables reliable storage. When it is detected correctable error during read command operation, all data of related block is corrected and is moved to other block. Since it continues to read data after recovery operation, read data is the same as no error data for host system. However, since data transfer is stopped temporarily, the output time of BSY signal becomes long. In order to perform Read Command Recovery, it is necessary to set up the threshold for the number of detected error bit. Read Command Recovery is performed by following commands.

- READ DMA
- READ MULTIPLE
- READ SECTOR(S)
- READ VERIFY SECTOR(S)

### 5.3 Power Failure Recovery

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The controller enables to reduce data loss in case of sudden power fail. Once power was failure before cached data writing back into flash, data in the cache will lost. The next time the power is on, the controller will check these fragmented data segment, and, if necessary, replace them with old data kept in flash until programmed successfully.

### 5.4 S.M.A.R.T. Technology

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S.M.A.R.T. is an acronym for Self-Monitoring, Analysis and Reporting Technology and enables to expect the endurance of flash memory. The S.M.A.R.T. function protects the user from unexpected fault of product. The S.M.A.R.T function enables to predict the occurrence of near-term degradation or fault conditions by monitoring and storing critical parameters of flash memory (ex. Number of bad block, maximum number of erase, etc). The host system is warned of a negative reliability condition which is the impending risk of data loss by the S.M.A.R.T. function. Then the user can take appropriate action to minimize the risk.

## 6. Software Interface

### 6.1 CF-ATA Command Set

Table 6-1 summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

**Table 6-1:** CFC-ATA command set (1/2)

<b>Command</b>	<b>Code</b>	<b>Command Protocol</b>
CFA Erase-Sector(s)	C0H	Non-data
CFA Request Extended Error Code	03H	Non-data
CFA Translate-Sector	87H	PIO data-in
CFA Write-Multiple-Without-Erase	CDH	PIO data-out
CFA Write-Sector(s)-Without-Erase	38H	PIO data-out
Check-Power-Mode	E5H or 98H	Non-data
Download Microcode	92H	PIO data-out
Execute-Drive-Diagnostic	90H	Device Diagnostic
Flush-Cache	E7H	Non-data
Format-Track	50H	PIO data-out
Identify-Drive	ECH	PIO data-in
Idle	E3H or 97H	Non-data
Idle-Immediate	E1H or 95H	Non-data
Initialize-Drive-Parameters	91H	Non-data
NOP	00H	Non-data
Read-Buffer	E4H	PIO data-in
Read DMA	C8H or C9H	DMA
Read Long	22h or 23h	PIO data-in
Read-Multiple	C4H	PIO data-in
Read-Sector(s)	20H or 21H	PIO data-in
Read-Verify-Sector(s)	40H or 41H	Non-data
Recalibrate	1XH	Non-data
Security Disable Password	F6H	PIO data-out
Security Erase Prepare	F3H	Non-data
Security Erase Unit	F4H	PIO data-out
Security Freeze Lock	F5H	Non-data
Security Set Password	F1H	PIO data-out
Security Unlock	F2H	PIO data-out

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**Table 6-1:** CFC-ATA command set (2/2)

Command	Code	Command Protocol
Seek	7XH	Non-data
Set-Features	EFH	Non-data
Set-Multiple-mode	C6H	Non-data
Sleep	E6H or 99H	Non-data
SMART Disable Operations	B0H	Non-data
SMART Enable/Disable Attribute Autosave	B0H	Non-data
SMART Enable Operations	B0H	Non-data
SMART Read Attribute Thresholds	B0H	PIO data-in
SMART Read Data	B0H	PIO data-in
SMART Read Log	B0H	PIO data-in
SMART Return Status	B0H	Non-data
Standby	E2H or 96H	Non-data
Standby-Immediate	E0H or 94H	Non-data
Write Buffer	E8H	PIO data-out
Write DMA	CAH or CBH	DMA
Write Long	32H or 33H	PIO data-out
Write Multiple	C5H	PIO data-out
Write Sector(s)	30H or 31H	PIO data
Write Verify	3CH	PIO data
Write Level	F5H	Non-data

## 7. Electrical Specification

### 7.1 Absolute Maximum Ratings

**Caution: Absolute Maximum Ratings** – Applied conditions greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 7-1: Absolute maximum ratings

(Based on GND [0V])

Item	Symbol	Rated Value	Unit	Condition
Power supply voltage	VDDIO	-0.5~+4.6	V	
Input voltage	V <sub>IN</sub> (Standard)	-0.5~+4.6	V	V <sub>IN</sub> < VDDIO+0.5V
	V <sub>IN</sub> (5V-Tolerant)	-0.5~+6.6 (The power is supplied)	V	V <sub>IN</sub> < VDDIO+3V
Output current	I <sub>OUT</sub>	±11	mA	3mA buffer
		±21	mA	6mA buffer
		±29	mA	9mA buffer
		±45	mA	12mA buffer
Storage temperature	T <sub>STG</sub>	-40~+100	°C	

### 7.2 Recommended Operating Conditions

Table 7-2: Recommended Operating Conditions

Item	Symbol	Rated Value	Unit	Condition
Input voltage	V <sub>IN</sub> (Standard)	2.7~3.6	V	
	V <sub>IN</sub> (5V-Tolerant)	4.5~5.5	V	
Operating ambient temperature	T <sub>A</sub>	0~+70	°C	

## 7.3 DC Characteristics

**Table 7-3: DC Characteristics (@ VDDIO=3.3V)**

Item	Symbol	Standard Value			Unit	Measurement Condition
		Min	Typ	Max		
Input voltage (TTL level)	V <sub>IH</sub>	2.0	—	VDDIO	V	
	V <sub>IL</sub>	0	—	0.7	V	VDDIO=2.7V
Schmidt trigger input (TTL level)	V <sub>+</sub>	1.2	—	2.4	V	
	V <sub>-</sub>	0.6	—	1.8	V	
	V <sub>h</sub>	0.3	—	1.5	V	
Output voltage	V <sub>OH</sub>	VDDIO-0.1	—	—	V	I <sub>OH</sub> =0mA
	V <sub>OL</sub>	—	—	0.1	V	I <sub>OL</sub> =0mA
Input leak current	I <sub>IH</sub>	-10	—	+10	uA	V <sub>IN</sub> =VDDIO
	I <sub>IL</sub>	-10	—	+10	uA	V <sub>IN</sub> =VSS
Output leak current	I <sub>OZ</sub>	-10	—	+10	uA	Hi-Z state
Pull-up resistance	R <sub>PU</sub>	14.2	31.9	80.7	kΩ	V <sub>IN</sub> =VSS
Pull-down resistance	R <sub>PD</sub>	20.6	44.9	116.4	kΩ	V <sub>IN</sub> =VDDIO
Current consumption (VDDIO)	I <sub>CC33udma6</sub>	—	40	—	mA	UDMA mode 6 (when 2ch interleave)
	I <sub>CC33pio6</sub>	—	20	—	mA	PIO mode 6 (when 2ch interleave)
	I <sub>CC33idl</sub>	—	2	—	mA	IDLE
	I <sub>CC33slp</sub>	—	0.1	—	mA	SLEEP

## 7.4 Capacitance

**Table 7-4: Capacitance**

Item	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance (5V-Tolerant)	C <sub>i</sub> (5V-Tolerant)	7	—	11	pF
I/O Pin Capacitance (5V-Tolerant)	C <sub>io</sub> (5V-Tolerant)	7	—	11	pF

## 7.5 Integrated Series Termination Resistor

**Table 7-5: Integrated Series Termination Resistor**

Item	Symbol	Min	Typ	Max	Unit
Terminator Resistance	R <sub>term</sub>	27	33	39	Ω

INTRQ, #INPACK, IORDY, DMACK, #CS0, #CS1, #IORD, #IOWR, A[2:0] and D[15:0] (IDE mode) signals that have integrated series termination resistors.

## 7.6 Power Supply Sequence

The controller is an IC that functions at 3.3V for the I/O power supply. These power supplies will deliver power to the chip externally, but a through current may occur inside the chip depending on the power-on and power-off sequence. For this reason, the power supply should be turned on and off simultaneously for reliability. Refer to figure 7-1.

- Turn on condition  
Time difference of  $VDDIO*0$  to both  $VDDIO*0.9$  is less than 100[ms].
- Turn off condition  
Time difference of  $VDDIO*0.9$  to both  $VDDIO*0.1$  is less than 100[ms].
- 5V tolerant buffer  
Before/after power supply is turned on/off, it must not apply 5V voltage.

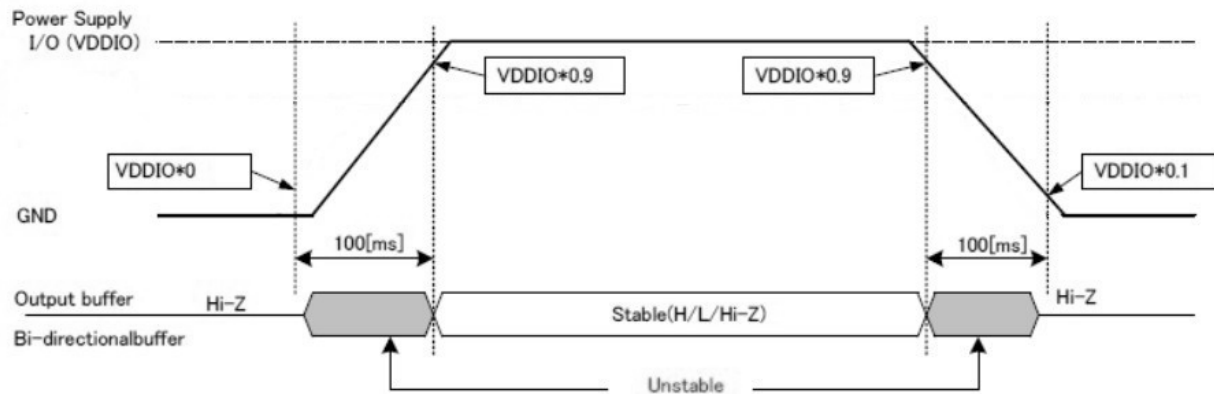


Figure 7-1 Power ON/OFF Sequence

## 7.7 Setup Time

Hardware reset time (reset release to a ready state) is less than about 100 [ms] in PC Card/HOST Memory Bus mode. For IDE mode, it is less than about 450 [ms] when master connection, and is less than about 250 [ms] when slave connection. Setup time does not depend on the total capacity of connected flash memory.

## 8. Physical Characteristics

### 8.1 Dimension

TABLE 8-1: Type I CFC physical specification

<b>Length:</b>	36.40 +/- 0.15mm (1.433+/- 0.06 in.)
<b>Width:</b>	42.80 +/- 0.10mm (1.685+/- 0.04 in.)
<b>Thickness (Including Label Area):</b>	3.3mm+/-0.10mm (0.130+/-0.04in.)

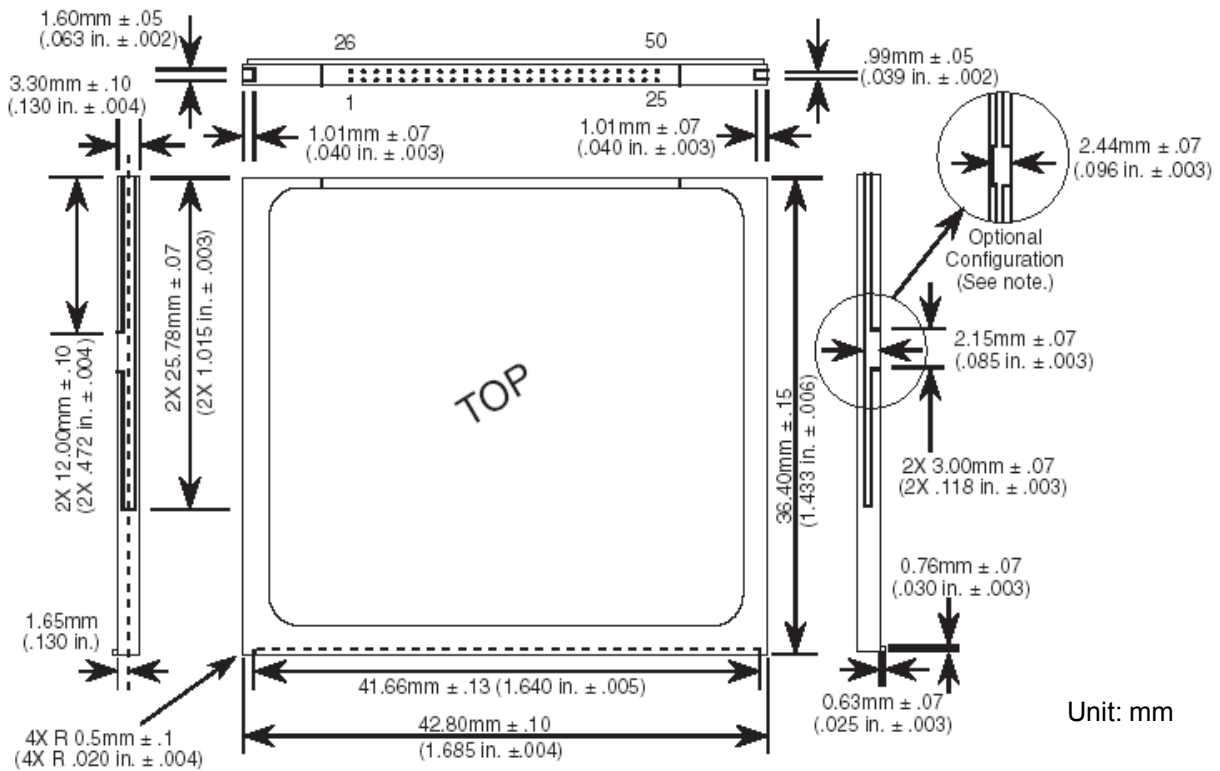
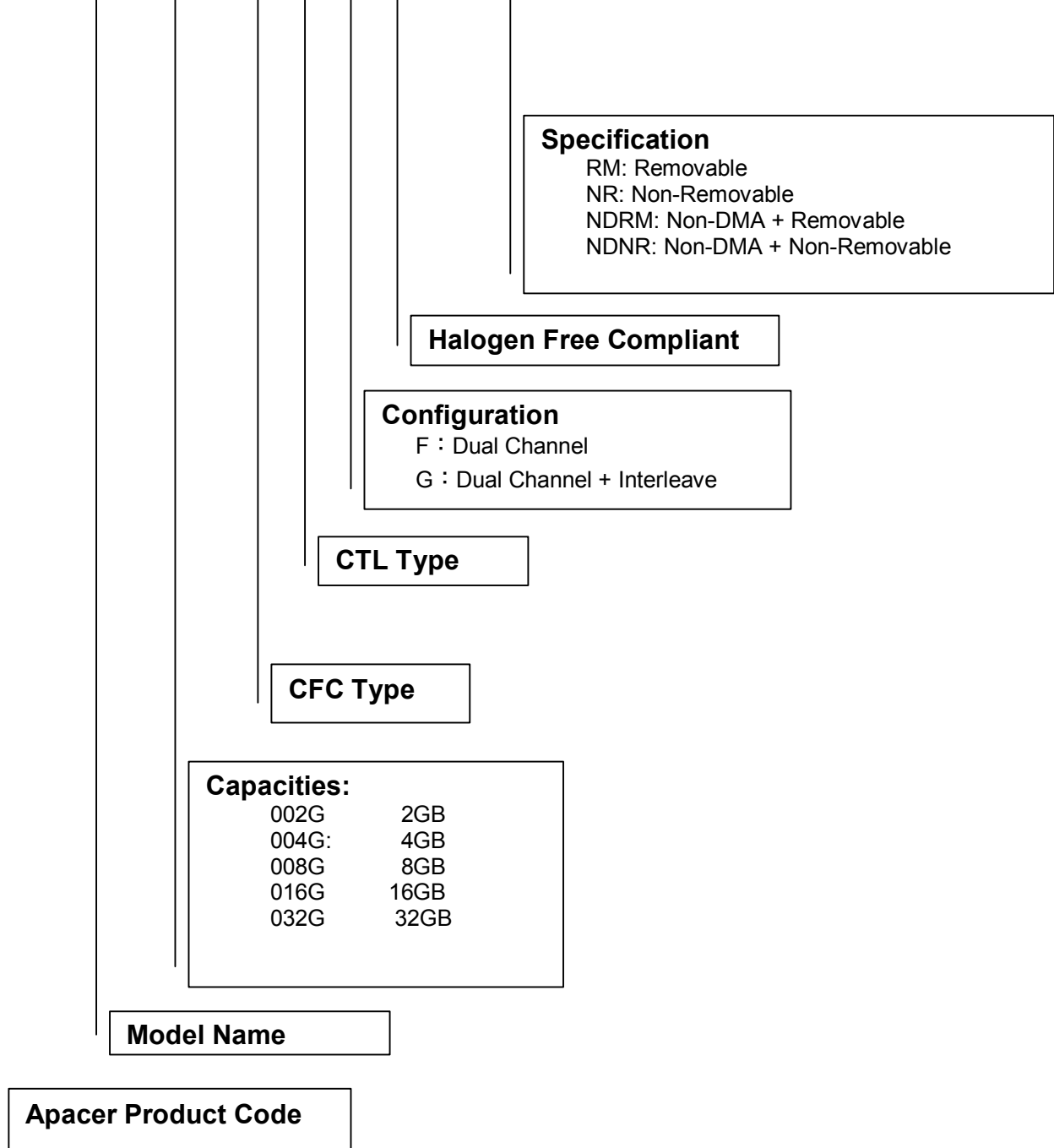


FIGURE 8-1: Physical dimension

## 9. Product Ordering Information

### 9.1 Product Code Designations

A P - C F x x x x B 5 X S - X X X X





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## 9.2 Valid Combinations

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### 9.2.1 Standard Temperature

- 9.2.1.1 Removable

<i>Capacity</i>	<i>AP/N</i>
2GB	AP-CF002GB5FS-RM
4GB	AP-CF004GB5FS-RM
8GB	AP-CF008GB5GS-RM
16GB	AP-CF016GB5GS-RM
32GB	AP-CF032GB5GS-RM

- 9.2.1.2 Non-Removable

<i>Capacity</i>	<i>AP/N</i>
2GB	AP-CF002GB5FS-NR
4GB	AP-CF004GB5FS-NR
8GB	AP-CF008GB5GS-NR
16GB	AP-CF016GB5GS-NR
32GB	AP-CF032GB5GS-NR

- 9.2.1.3 Non-DMA + Removable

<i>Capacity</i>	<i>AP/N</i>
2GB	AP-CF002GB5FS-NDRM
4GB	AP-CF004GB5FS-NDRM
8GB	AP-CF008GB5GS-NDRM
16GB	AP-CF016GB5GS-NDRM
32GB	AP-CF032GB5GS-NDRM

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- 9.2.1.4 Non-DMA + Non-Removable

<i>Capacity</i>	<i>AP/N</i>
2GB	AP-CF002GB5FS-NDNR
4GB	AP-CF004GB5FS-NDNR
8GB	AP-CF008GB5GS-NDNR
16GB	AP-CF016GB5GS-NDNR
32GB	AP-CF032GB5GS-NDNR

**Note:** Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

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## Revision History

Revision	Date	Description	Remark
0.1	09/03/2009	Preliminary	
1.0	10/07/2009	Official release	
1.1	11/17/2009	Command set revised	

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## Global Presence

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