Lattice Semiconductor Corporation

Lowest Power 10G SERDES!

XPIO 110GXS

Fully Integrated 10Gbps Serializer/Deserializer Device

Features

- ■ **Single chip SERDES solution with integrated transmitter and receiver**
- ■ **Continuous serial operation range from 9.95 Gbps to 10.31 Gbps**
- ■ **Parallel LVDS data range from 622 Mbps to 644 Mbps**
- ■ **Low power consumption (800 mW typical)**
- ■ **Performs 16:1 serialization and 1:16 deserialization**
- ■ **Embedded Limiting Amplifier enhances receiver sensitivity**
- ■ **Low-jitter PLL for clock generation**
- ■ **On-chip Clock Data Recovery circuit**
- ■ **On-chip FIFO to decouple transmit clocks**
- ■ **Bit order swap for 10GE operations**
- ■ **Programmable 4-phase LVDS clock output for easy system design**
- ■ **Repeating serial data output**
- ■ **Line loopback, diagnostic loopback, and simultaneous loopback modes**
- ■ **Frequency Lock Alarm Output**
- ■ **Programmable differential output swing on both Serial driver and Parallel LVDS driver**
- ■ **1.3V core voltage and 2.5V I/O voltage**
- ■ **Supports 10GE (10-Gigabit Ethernet), OC-192, XFP, XSBI and SFI-4.1 interfaces**
- ■ **269-pin flip-chip BGA (15 x 15 mm body size, 0.8 mm pitch)**
- ■ **-40 to 85°C operating temperature**

General Description

The XPIO™ 110GXS is a fully integrated 10 Gbps serializer/deserializer device designed for high-speed switches and routers that require very low power budget and a small footprint as well. Centering on 10 Gbps speed, the XPIO 110GXS is a versatile chip that is capable of handling applications in various standards, such as OC-192 (9.95 Gbps) and 10GE (10.31 Gbps).

An on-chip low jitter PLL generates all required clocks based on an external reference clock at 1/16 or 1/64 frequency of the serial data rate, which is 622.08 MHz or 155.52 MHz, respectively, for OC-192 applications. An Integrated Limiting Amplifier allows flexibility in placement and reduced bit-error rates (BER).

Fabricated with state-of-the-art CMOS technology, the XPIO 110GXS performs all necessary functions for serial-to-parallel and parallel-to-serial conversions, and consumes less than one third of the power consumed by the more conventional SiGe Bi-CMOS designs.

Overview

The XPIO 110GXS consists primarily of blocks of parallel-to-serial and serial-to-parallel functions plus system timing. Low Voltage Differential Signaling (LVDS) is used for parallel signal input and output while Current Mode Logic (CML) is used for serial transmission and reception. A limiting amplifier is designed into the chip to improve serial receiver sensitivity. The system timing blocks consist of the clock-multiplier-unit (CMU), LVPLL (LVDS interface timing Phase-Lock-Loop) and CDR (clock-data-recovery) units, which generate clocks for the chip. Figure 1 shows the XPIO 110GXS chip block diagram.

Table 1. XPIO 110GXS Supported Protocols

Device	Standards Supported	Data Rate
XPIO 110GXS	OC-192 10GE	9.95 Gbps 10.31 Gbps

Figure 1. XPIO 110GXS Block Diagram
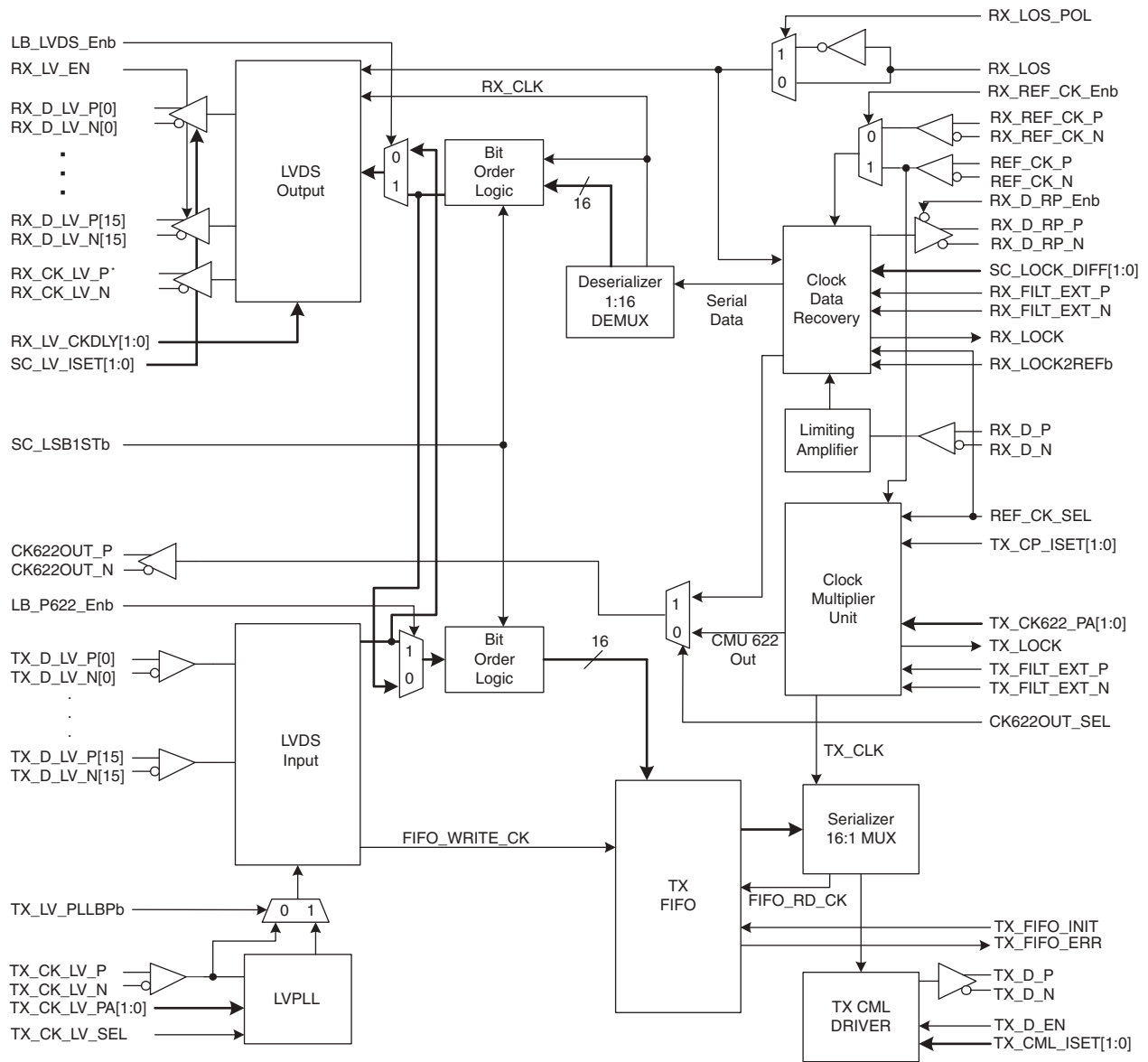
The XPIO 110GXS is divided into a transmitter section and a receiver section. The major operations performed by the chip are:

Transmitter Operation
1. Low jitter clock generation via the Clock-Multiplier-Unit (CMU)
2. 16-bit LVDS parallel data input
3. Parallel-to-serial conversion
10Gbps CML serial data output
Receiver Operation
1. CML serial input to a limiting amplifier
2. Clock and data recovery
3. Serial-to-parallel conversion
4. 16-bit LVDS parallel data output, with a synchronizing clock output
5. Built-in LVDS line loopback, and LVDS diagnostic loopback modes for testing and network diagnosis

Functional Description

The XPIO 110GXS transceiver is a low power, low jitter, and fully integrated serializer/deserializer chip. It operates in the data rate range of 9.95-10.31 Gbps, performs all necessary parallel-to-serial and serial-to-parallel conversions. The chip is suitable for applications utilizing OC-192 and 10GE. The serial interface I/O uses the CML standard while the low speed parallel I/O is based on the LVDS standard. These standards are compliant to both the Optical Interface Forum's SFI-4 standard and the 10GE's XSBI standard. The LVDS parallel I/O can be directly connected to Multi-Standard-Agreement (MSA) 300 systems.

To accommodate bit order differences between OC-192 and 10GE, the XPIO 110GXS provides the capability of bit swapping. The data presented on TX_D_LV_P/N[15] or MSB is transmitted first, followed in order by TX_D_LV_P/N[14] to TX_D_LV_P/N[0] when SC_LSB1STb is not connected or is connected to a logic high. TX_D_LV_P/N[0] or LSB is transmitted first followed in order by TX_D_LV_P/N[1] to TX_D_LV_P/N[15] when SC_LSB1STb is connected to a logic low. The parallel receive bus mirrors this behavior. The SC_LSB1STb unconnected, or at logic high, the first serial bit received is presented on RX_D_LV_P/N[15]. Conversely the first bit received is presented on RX_D_LV_P/N[0] when SC_LSB1STb is pulled low.

Transmitter

The transmitter performs the serialization process, converting the 16-bit parallel LVDS data stream to a serial data stream at approximately a 10 Gbps data rate. The transmitter consists of a LVDS data receiver, a FIFO, a 16:1 serializer, a low jitter CMU, and a 10Gbps output data driver.

LVDS Data Receiver
The Input and Analog Pin Assignments and Descriptions table in this document shows the 16 LVDS differential data input pairs (TX_D_LV_P/N [15:0]). Data applied at the transmit data pairs is aligned to the LVDS input clock (TX_CK_LV_P/N), which can be either 1/16th or 1/32nd the transmit data rate (622.08 or 311.04 nominally for OC-192). The clock rate is selected through the assertion or deassertion of the TX_CK_LV_SEL pin. Figure 13 describes the LVDS data relationship to the LVDS input clock.

The LVDS input receivers convert the LVDS signals to CMOS signals. The converted signals are latched based on an internal clock that is generated from the TX_CK_LV_P/N input clock through a phase-lock-loop (LVPLL). In order to achieve optimal latch timing, the phase relationship between the internal clock and the TX_CK_LV_P/N clock can be adjusted by programming TX_CK_LV_PA[1:0]. The LVDS PLL can also be bypassed by the assertion of the TX_LV_PLLBPb pin, which is a desirable feature in some applications. When the LVPLL is bypassed it is up to the system designer to manage the TX_CK_LV_P/N input.

Transmitter FIFO
A 16 bit wide and 8-word deep FIFO is designed into the XPIO 110GXS to decouple the LVDS clock from the serial transmission clock. In addition, the FIFO also improves the tolerance to minor phase differences between the FIFO write clock and read clock due to phase drift or phase wander.

The FIFO circuitry indicates an overflow or underflow condition by asserting TX_FIFO_ERR high. The TX_FIFO_ERR only provides status information about an overflow or underflow. It does not indicate which of the two events actually occurred. During the period of time when the TX_FIFO_ERR signal is asserted, the TX_D_P/N pins toggle at a constant rate. This prevents the AC coupling capacitors from becoming blocking capacitors.

The transmit FIFO's read and write pointers can be recentered by asserting the TX_FIFO_INIT pin high. Thus, one way to automatically recenter the FIFO read/write pointers after TX_FIFO_ERR is asserted is to connect TX_FIFO_INIT and TX_FIFO_ERR together.

The FIFO read/write pointers are re-centered after:

- Device power on reset
- Transmitter reset (asserting RESET_TXb low)
- CMU PLL is out of lock

Serialization

The output data bus from the FIFO feeds a 16:1 serializer to generate a 9.953 Gbps (OC-192 rate) data stream. The high-speed clock (TX_CLK) is a low jitter clock generated by the CMU. The serializer uses TX_CLK to clock out high-speed data.

TX CML Driver

The serial data stream in turn becomes an input to a differential high-speed CML data driver. The TX_D CML driver incorporates an internal 50-ohm termination resistor on both P and N branches for impedance matching with the PCB transmission line. The CML output may require AC coupling (as in Figure 5). The output current of the CML driver can be adjusted using two configuration pins, TX_CML_ISET[1:0]. These configuration pins are used to balance power consumption and performance.

In normal operation, the data presented at the LVDS TX inputs requires about nine clocks to transit the various logic blocks before being presented at the TX CML driver output.

Clock-Multiplier-Unit (CMU)

The CMU consists of a differential PLL that is capable of producing a very low jitter serial clock. The clock is generated through a reference clock (REF_CLK_P/N) at either $1/16^{th}$ or $1/64^{th}$ the data transmission rate (This is nominally 622.08 or 155.52 MHz for OC-192 data rates). This reference clock must be generated from a differential crystal oscillator that has a frequency accuracy of better than ±20ppm for SONET applications.

The CMU PLL can provide a phase-adjustable parallel data rate clock (CK622OUT_P/N) that is $1/16^{th}$ the transmit data rate to clock other devices or systems. The output of CK622OUT_P/N meets the LVDS signaling specifications. Using the TX_CK622_PA[1:0] configuration pins, the phase can be adjusted in T/4 increments, where T is the period of the clock for the parallel interface.

Receiver

Limiting Amplifier

The XPIO 110GXS 10 Gbps CMOS receiver integrates a highly sensitive limiting amplifier. The XPIO 110GXS also implements an amplifier offset compensation technology that works in conjunction with the limiting amplifier to achieve superior amplifier input sensitivity. Sufficient gain is designed into the limiting amplifier to detect a peak-to-peak differential input as small as 50mV. This attenuated signal can be properly detected and amplified to saturation.

Clock and Data Recovery (CDR)

One of the most critical circuits in the receiver is the clock and data recovery (CDR) block. The CDR block extracts the clock from an incoming high-speed, non-return to zero (NRZ) data, and retimes the data based on an external reference clock. Extraction of the clock embedded in the serial data-stream is performed through comparison of the phase relationship between transitions of the data and the external reference clock.

The external reference clock is essential for the CDR block. The reference clock provides two functions: One function is training the VCO in the CDR PLL to the serial data-stream frequency. The other is to generate a stable clock when the input serial data is absent. The CDR PLL creates an internal reference frequency. The reference frequency is monitored, and a loss of lock is asserted when it goes out of specification.

Lock Detect
The XPIO 110GXS implements a CDR lock detector circuit that monitors the frequency of the internal clock. RX_LOCK is asserted whenever a REF_CK or RX_REF_CK are operating within specification. RX_LOCK is deasserted under some specific circumstances:

1. When RX_RESETb is asserted (i.e. '0')

2. When the REF_CK (or RX_REF_CK) is not present.

3. When the clock recovered from the incoming datastream falls outside the range specified by the SC_LOCK_DIFF input pins. When the recovered clock is out of range, RX_LOCK will deassert briefly and then be reasserted as it relocks to the REF_CK (RX_REF_CK). This effectively leaves the RX_LOCK signal toggling as it attempts to reacquire the clock embedded in the RX_D_P/N data inputs.

Deserialization
The XPIO 110GXS uses a 1:16 demultiplexer to deserialize the high speed data from the CDR. The demultiplexer generates the 16 bit parallel data stream. The bit order presented on the RX_D_LV_P/N[0..15] LVDS outputs mirrors the order on the TX_D_LV[0..15]P/N LVDS inputs. The first data bit received by the CDR is present on RX_D_LV_P/N[15] when SC_LSB1STb is connected to a logic high, and it is present on RX_D_LV_P/N[0] when SC_LSB1STb is connected to a logic low.

LVDS Data Transmitter
The 16-bit parallel data and clock are sent out via the RX_D_LV_P/N[0..15] and RX_LV_CK_P/N LVDS pins, respectively. Data on the RX_D_LV_P/N pins is synchronous to the RX_LV_CK_P/N output pins. The data coming in on the RX_D_P/N pins requires around five clocks to arrive at the RX_D_LV_P/N outputs. The output current of the LVDS outputs is adjustable using the SC_LV_ISET[1:0] configuration pins. System designers can use these pins to optimize the LVDS receive data performance.

XFP Module Considerations
The XPIO110GXS was conceived and implemented prior to the finalization of the XFP specification. The implication of this is the CML TX voltage swing is typically higher than that specified in the XFP MSA documents.

The XFP MSA specification indicates a XFP module should accept a maximum of 800mV input swing. In practice it is the individual XFP module internal architecture that defines the maximum range. However, most XFP modules simply rate themselves to the 800mV specification regardless of the likelihood they may operate beyond the range specified in the XFP MSA.

Actual operation of the XPIO110GXS with existing XFP modules shows these still operate with the CML swing set to the default TX_CML_ISET[1:0] = "11". In order to more closely match the XFP specification a TX_CML_ISET[1:0] = "01" configuration is recommended. This places the typical output swing from the CML TX outputs at 650mV to 1100mV.

Loopback Operation

The XPIO 110GXS supports several loopback operations to provide diagnostic functions and to aid in performing SONET/SDH functional tests.

LVDS Diagnostic Loopback
In LVDS loopback mode, 16 bit-wide data is fed into the TX LVDS input. The XPIO 110GXS routes data from the LVDS transmit interface to the internal receiver interface, and then repeats the data at the LVDS RX output.

To enable this mode of operation set BIST_ENb=0, LB_LVDS_ENb=0, and BIST_LB_SC[1:0]=10.

Figure 2. LVDS Loopback Mode Block Diagram
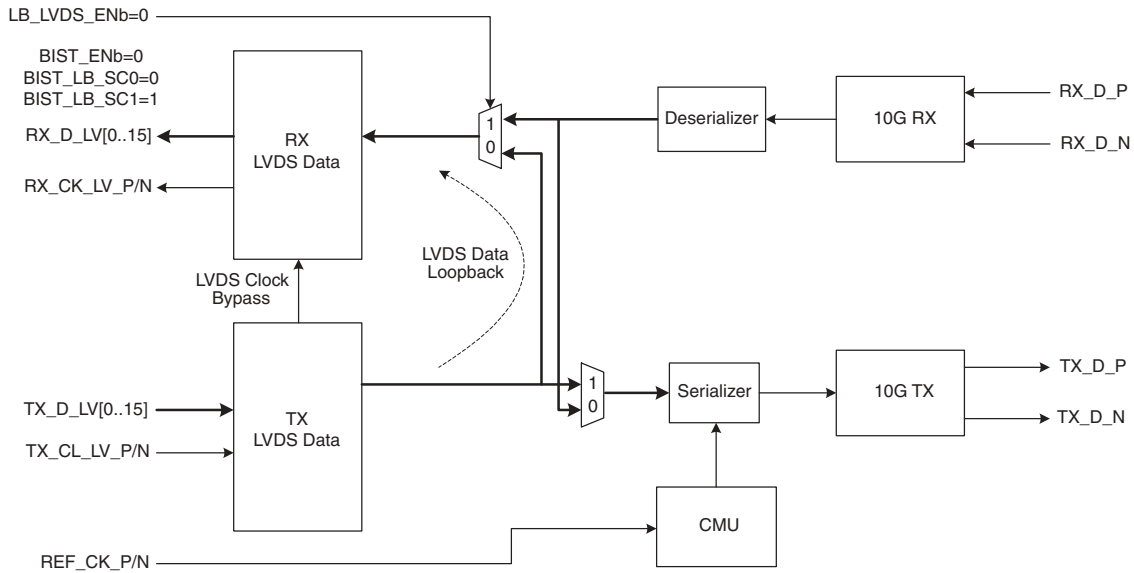
LVDS Line Loopback

Line loopback is a diagnostic mode that establishes a parallel connection between the output of the deserializer and the input to the serializer. When this mode is active, serial receive data is deserialized, and internally looped back to the serializer. The data provided at the serializer is transmitted via the CML output. Line loopback is activated by setting the LB_P622_Enb pin to a logic low.

Mode 1: Synchronous line loopback without clock clean-up. Driving LB_P622_Enb low enables line loopback mode. Connecting the LVDS output clock, RX_CK_LV_P/N, to REF_CK_P/N makes the loopback mode synchronous. In addition, a separate reference clock is input to RX_REF_CKP/N for use by the CDR logic. The data transmitted across the TX_D_P/N pins is now timed to the LVDS clock making the RX and TX data synchronous. However, the RX_CK_LV_P/N does not require SONET/SDH tolerance in order to transmit the parallel LVDS data. This means the data repeated on TX_D_P/N will have significant jitter.

Figure 3. Line Loopback Mode 1 Block Diagram

6
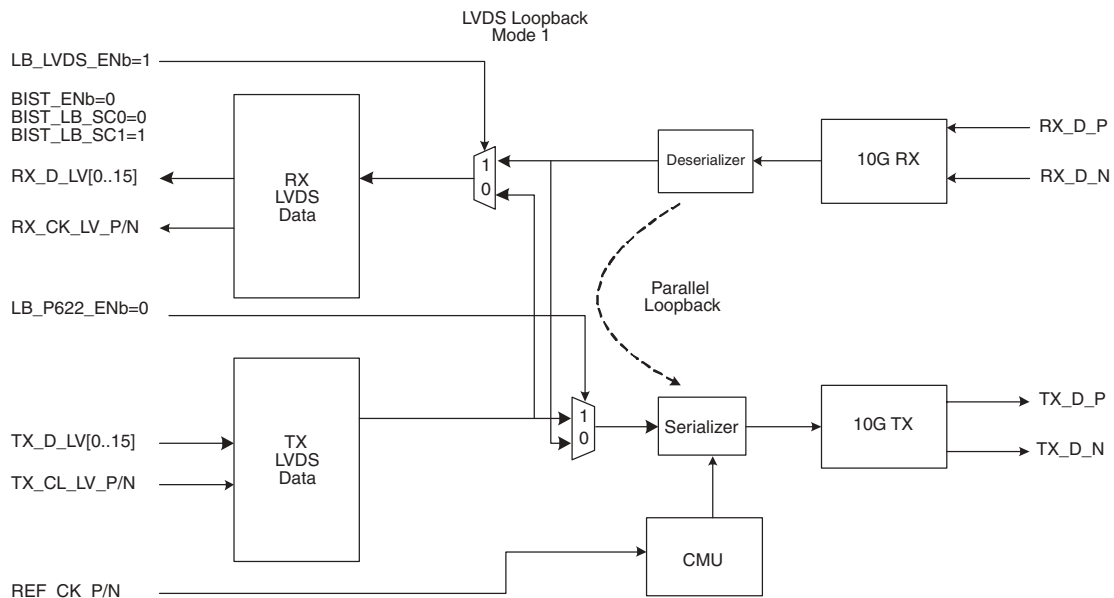
Mode 2: Synchronous line loopback with clock clean-up. Driving LB_P622_Enb low enables line loopback mode. In order to make this loopback mode SONET/SDH compliant the CK622OUT_P/N must be connected to a VCXO-powered PLL chip (e.g. MAX3670), and CK622OUT_SEL pulled/driven high. The output of the PLL provides a low jitter reference clock that is in phase with the data presented at the LVDS parallel outputs. This reference clock is connected to REF_CK_P/N. As in Mode 1 a separate reference clock is input to RX_REF_CK_P/N to drive the CDR logic. Data on the TX_D_P/N and RX_D_P/N pins are now synchronous, and the data repeated on TX_D_P/N meets SONET/SDH line loopback application requirements.

Figure 4. Line Loopback Mode 2 Block Diagram
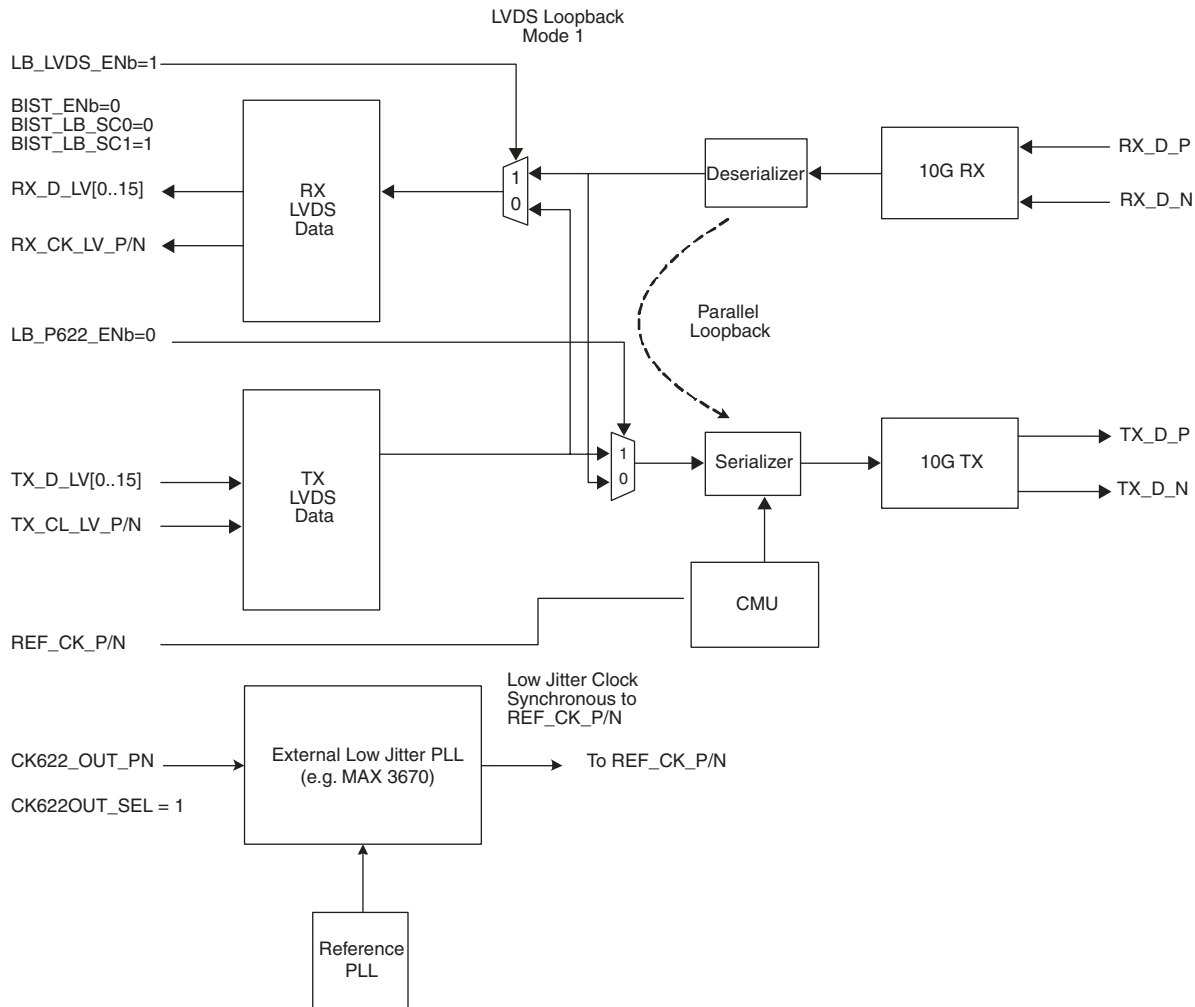
Reference Clocks

There are two AC coupled reference clock input pairs, REF_CK_P/N, and RX_REF_CK_P/N. The CDR block is driven by either REF_CK_P/N or RX_REF_CK_P/N. The CMU block is only driven by REF_CK_P/N. The reference clock input frequency for REF_CK_P/N can be either 1/16th (622MHz) or 1/64th (155MHz) the transmitter/receiver data rate. Likewise, RX_REF_CK_P/N can be 1/16th or 1/64th the 10Gbps receiver rate. RX_REF_CK_P/N and REF_CK_P/N are configured in tandem to 1/16th or 1/64th by REF_CK_SEL. They cannot be configured independently. AC coupling for all reference clocks is recommended.

Driving RX_REF_CK_P/N is only necessary when:

- The transmitter and receiver run at independent data rates
- Line Loopback Mode 1 is active
- Line Loopback Mode 2 is active

Figure 5 shows how a reference clock is input to the XPIO 110GXS using an AC coupling scheme.

Figure 5. CML Output Driver Termination (AC Coupled)
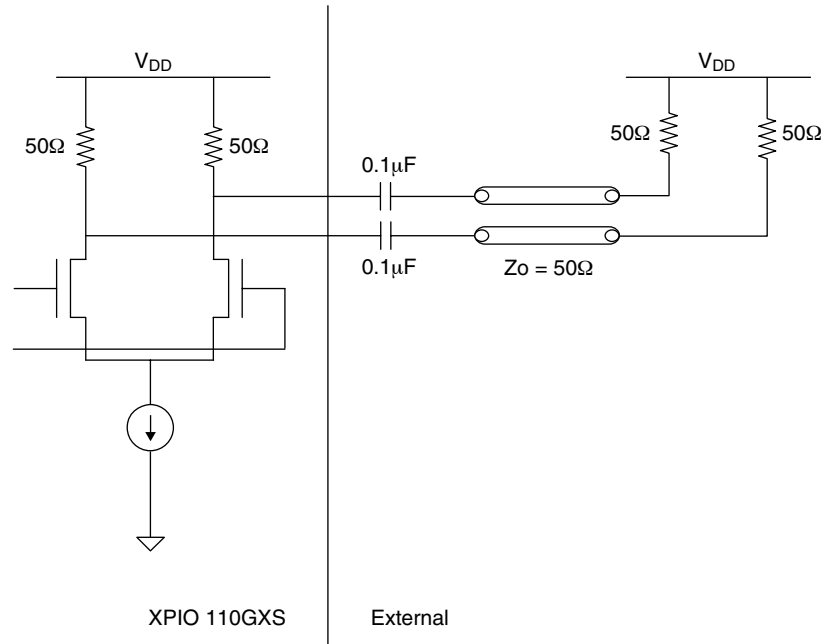
Figure 6. CML Input Receiver (AC Coupled)
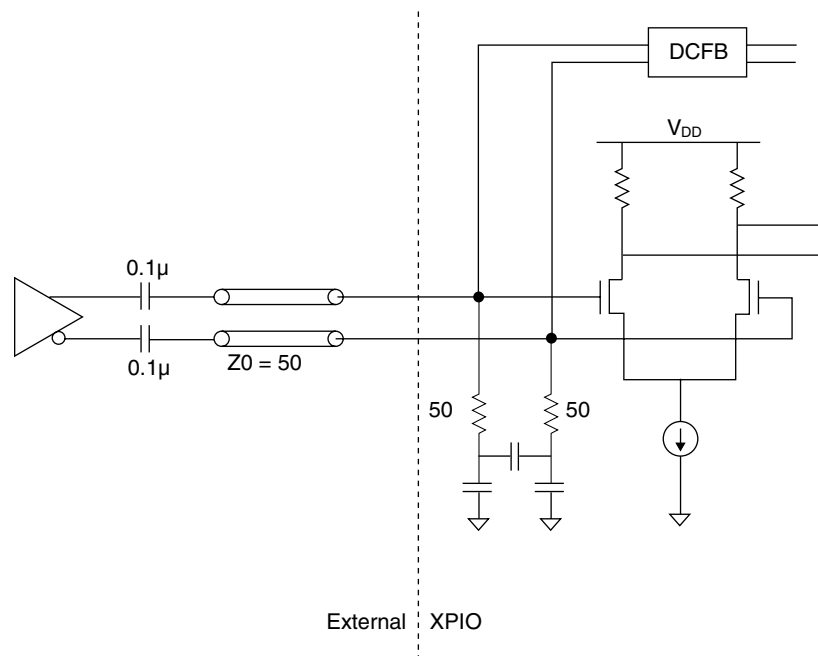
Figure 7. Differential Oscillator Driving to XPIO 110GXS Clock Input (AC Coupled)

0.1μF

0.1μF

Zo = 50Ω

100Ω

External   XPIO 110GXS
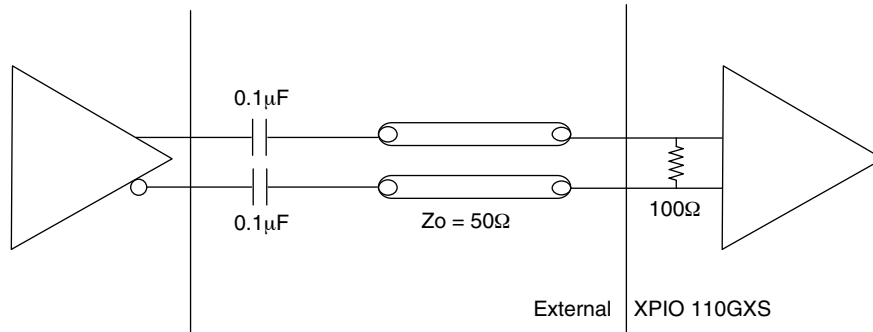
Figure 8. LVDS Output and Input Connection

Zo = 50Ω

100Ω

LVDS Output

External   LVDS Input
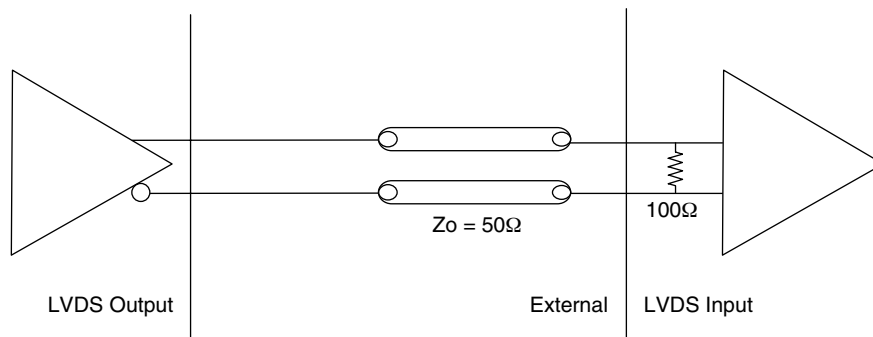
Figure 9. External Loop Filter Components

0.01 μF

396Ω   396Ω

TX_FILT_EXTP   TX_FILT_EXTN

0.39μF

RX_FILT_EXTP   RX_FILT_EXTN

PCB Layout Recommendations

The TX/RX filter components should be small form factor capacitors and resistors. They should be placed as close as possible to the XPIO 110 device.

The TX filter components should be surrounded by a copper trace to GND. As shown below, the RX filter components should be enclosed by the GND.

Figure 10. PCB Layout Examples
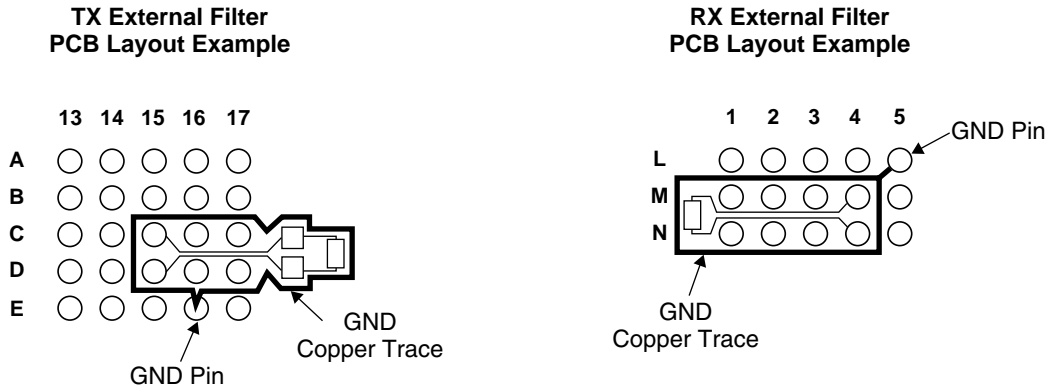
Bottom View

These diagrams for example purposes only.

Electrical Specifications

AC Signaling Definitions

Figure 11. Differential Voltage Measurements
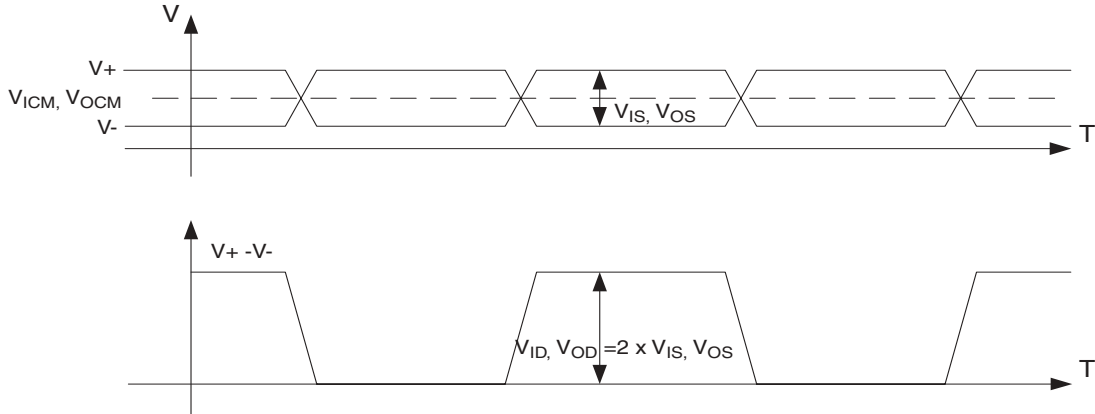
Figure 12. Rise and Fall Time Measurements
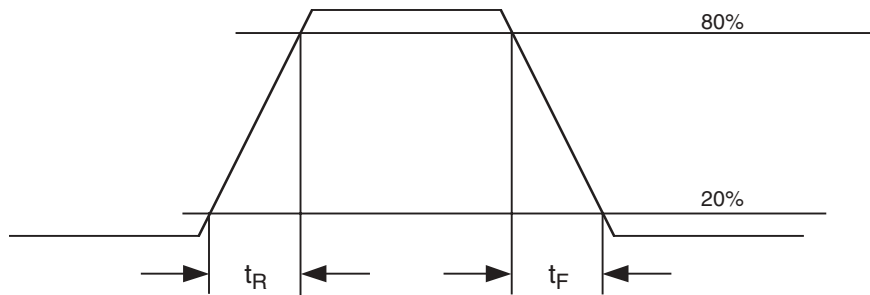
Figure 13. LVDS Data to Clock Relationship of Transmitter, 1/16th of Frequency (622.08MHz for OC-192)
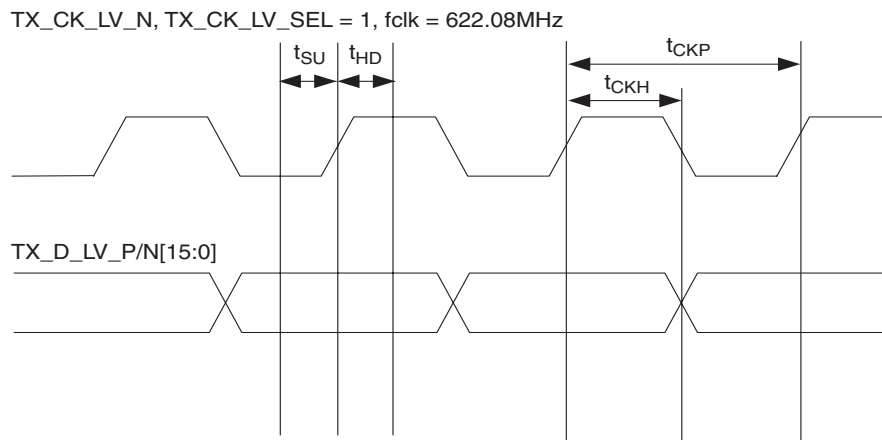
Note: TX_D_LV_P/N[15:0] is latched using the rising edge of TX_CK_LV_N.

Figure 14. LVDS Data to Clock Relationship of Transmitter, 1/32nd of Frequency (311.04MHz for OC-192)

TX_CK_LV_P, TX_CK_LV_SEL = 0, fclk = 311.04MHz

t_{SU} t_{CKP} t_{CKH}

TX_D_LV_P/N[15:0]

t_{HD}
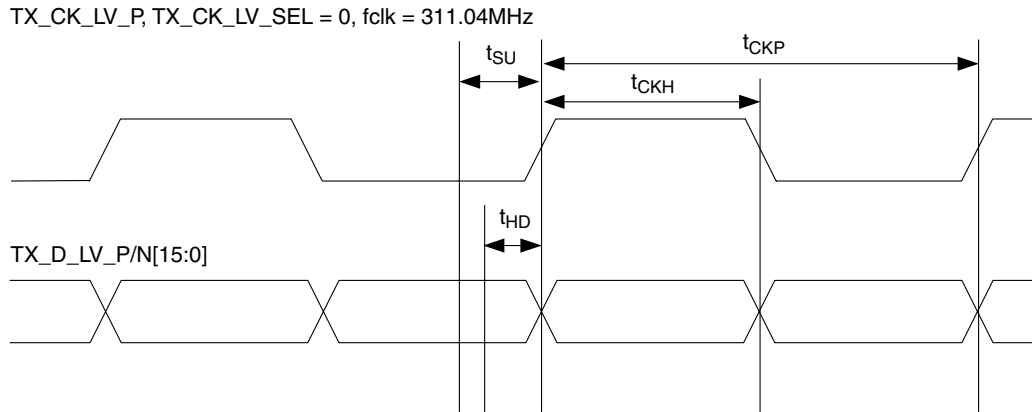
Figure 15. LVDS Data to Clock Relationship of Receiver

RX_D_LV_P/N[15:0]

t_{CQB}

t_{CQA}

RX_CK_LV_P
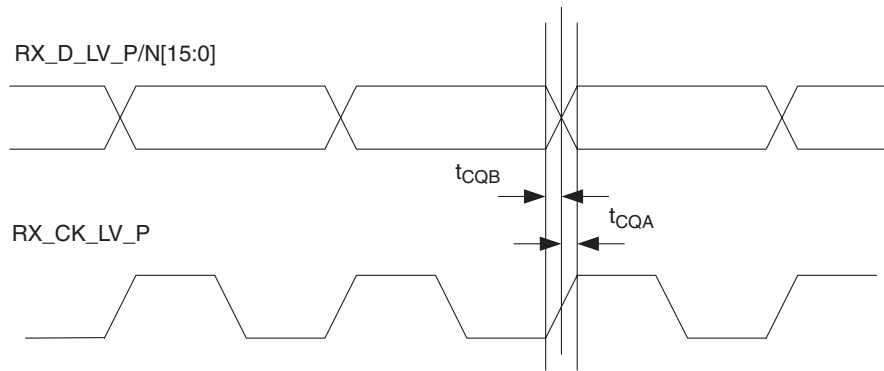
Configuration Pin Descriptions

Pin Name	State	Action
Transmitter Controls		
TX_D_EN	1	TX_D_P/N output is active
	0	TX_D_P/N output is inactive.
TX_LV_PLLBPb	1	The internal LVDS PLL is active
	0	The internal LVDS PLL is bypassed. External clock management and phase adjustment is required when this pin is 0.
TX_FIFO_INIT	1	Initialize the TXFIFO
	0	No action
TX_CML_ISET[1:0]	11	See V_{OD} in the High Speed Input/Output Specifications section of this data sheet.
	10	
	01	
	00	
TX_CK622_PA[1:0][1]	11	3T/4[2]
	10	Adjust T/2
	01	Adjust T/4
	00	No Adjust
RESET_TXb	1	Transmitter in normal operation
	0	Resets the transmitter
PWDN_TXb	1	Transmitter is operating
	0	Transmitter is powered down
TX_CK_LV_SEL	1	TX_CK_LV is 1/16 of frequency
	0	TX_CK_LV is 1/32 of frequency
TX_CK_LV_PA[1:0]	TX_CK_LV_SEL = 1/16th of Frequency	
	11	Clock delay = 0
	10	Clock delay = -T/16
	01	Clock delay = T/16
	00	Clock delay = T/8
	TX_CK_LV_SEL = 1/32nd of Frequency	
	11	Clock delay = T/4
	10	Clock delay = T/4-T/32
	01	Clock delay = T/4+T/32
	00	Clock delay = T/4+T/16
TX_CP_ISET[1:0]	11	622MHz clock (default using internal pull-ups)
	10	Invalid
	01	Invalid
	00	155MHz clock
Receiver Controls		
RX_REF_CK_ENb	1	RX_REF_CK is disabled
	0	RX_REF_CK is enabled
RX_LV_CKDLY[1:0]	11	LVDS output clock is delayed: 90ps
	10	LVDS output clock is delayed: 180ps
	01	LVDS output clock is delayed: 270ps
	00	LVDS output clock is delayed: 360ps

Configuration Pin Descriptions (Continued)

Pin Name	State	Action	
		RX_LOS_POL = 0	**RX_LOS_POL = 1**
RX_LOS	1	Asserted by the receiver to indicate it has lost the data signal.	Receiver OK
	0	Receiver OK	Asserted by the receiver to indicate it has lost the data signal.
RX_LOS_POL	1	RX_LOS is an active-low input	
	0	RX_LOS is an active-high input.	
RX_D_RP_ENb	1	RX_D_RP_P/N signals are inactive	
	0	RX_D_RP_P/N signals are active	
RX_LOCK2REFb[3]	1	RX_PLL locks to the recovered receive data clock.	
	0	RX_PLL locks to the REF_CK or RX_REF_CK input	
SC_LOCK_DIFF[1:0][3]	11	See LOCK$_{TOL}$ in the High Speed Input/Output Specifications section of this data sheet.	
	10		
	01		
	00		
SC_LV_ISET[1:0]	11	See V$_{OS}$ in the Low Speed Input/Output Specifications section of this data sheet.	
	10		
	01		
	00		
RX_LV_EN	1	RX_D_LV_P/N[15:0] are enabled	
	0	RX_D_LV_P/N[15:0] are disabled	
PWDN_RXb	1	Receiver is operating	
	0	Receiver is powered down	
RESET_RXb	1	Receiver normal operation	
	0	Resets the receiver logic.	
General Controls			
CK622OUT_SEL	1	CK622 sourced by CDR	
	0	CK622 sourced by CMU	
SC_LSB1STb	1	TX_D_LV_P/N[15] transmitted over TX_D_P/N first RX_D_LV_P/N[15] first bit received from RX_D_P/N (e.g. SONET applications)	
	0	TX_D_LV_P/N[0] transmitted over TX_D_P/N first RX_D_LV_P/N[0] first bit received from RX_D_P/N (e.g. 10GE applications)	
REF_CK_SEL[4]	1	REF_CK is 1/16 of frequency (622.08MHz for OC-192)	
	0	REF_CK is 1/64 of frequency (155.52MHz for OC-192)	
BIST_ENb	1	Normal operation, built-in self tests are disabled.	
	0	Built-in self test enabled. Enable this for LVDS loopback mode only.	
BIST_LB_SC[1:0]	11	Invalid	
	10	LVDS loopback mode enable	
	01	Invalid	
	00	Invalid	

1. Only available when CK622OUT_SEL = 0 (CMU CLK Mode).
2. T = period
3. Locks to REF_CK when RX_REF_CK_Enb = 1. Locks to RX_REF_CK when RX_REF_CK_Enb = 0.
4. Applies to RX_REF_CK also.

Absolute Maximum Ratings[1, 2, 3]

1.3V Supply Voltage. . . . . -0.5 to 1.43V

2.5V Supply Voltage. . . . . -0.5 to 2.75V

DC Input Voltage (Differential Inputs). . . . . -0.3 to V_{DD25} + 0.3V

DC Input Voltage (LVCMOS Inputs) . . . . -0.3 to V_{DD25} + 0.3V

Output Current (Differential Outputs) . . . . ±50 mA

Output Current (LVCMOS Outputs) . . . . ±15 mA

Storage Temperature . . . . -65 to 150°C

Case Temperature Under Bias. . . . . -55 to 125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied (while programming, following the programming specifications).
2. Thermal characteristics, maximum ratings, and thermal compliance requirements can be found in the Lattice *Thermal Management* document.
3. All voltages referenced to GND.

Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Ambient Temperature (Commercial)	T_A		0		70	°C
Ambient Temperature (Industrial)	T_A		-40		85	°C
1.3V Supply Voltage	VDDAR VDDAT VDDL VDDT VDDR		1.23	1.30	1.37	V
2.5V Supply Voltage	VDDAT25 VDDAR25 VDDH		2.37	2.5	2.63	V

Electrical Characteristics

High Speed Input/Output Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
AC Characteristics						
t_R	CML output rise time	See Figure 12.	—	35	45	ps
t_F	CML output fall time	See Figure 12.	—	35	45	ps
f_{REFCLK}	Input reference clock frequency (REF_CK_P/N)	REF_CK_SEL = 1	622.08	—	644.53	MHz
		REF_CK_SEL = 0	155.52	—	161.13	MHz
f_{REFCLK}	Receiver input reference clock frequency (RX_REF_CK_P/N, active only in applications where REF_CK_P/N is used as a transmitter)	REF_CK_SEL = 1	622.08	—	644.53	MHz
		REF_CK_SEL = 0	155.52	—	161.13	MHz
t_{DCREF}	Reference clock duty cycle		40	—	60	%
Δf_{REFCLK}	Reference clock frequency tolerance		-100	—	100	ppm
DC Characteristics						
V_{COM}	Serial output common mode voltage (TX_D_P/N)	V_{DDT} = 1.3V, See Figure 11.	0.65	—	1.0	V
V_{OD}	Serial output differential voltage swing (TX_D_P/N)	V_{DDT} = 1.3V, TX_CML_ISET[1:0]=11, See Figure 11.	1100	—	1750	mV (pk-pk)
		V_{DDT} = 1.3V, TX_CML_ISET[1:0]=10	1000	—	1500	
		V_{DDT} = 1.3V, TX_CML_ISET[1:0]=01	650	—	1100	
		V_{DDT} = 1.3V, TX_CML_ISET[1:0]=00	1250	—	1800	
V_{ID}	Serial input differential voltage swing (RX_D_P/N)	See Figure 11.	50	—	2000	mV (pk-pk)
V_{ICM}	Serial input common mode voltage (RX_D_P/N)	See Figure 11.	0.75	—	1.15	V
V_{ID}	Input voltage differential swing for (REF_CK_P/N, RX_REF_CK_P/N)	See Figure 11.	250	—	2400	mV (pk-pk)
Performance Characteristics						
J_{GEN}	Transmitter jitter generation (peak to peak)		—	0.085	—	UI
t_{ACQ}	Transmitter CMU PLL acquisition time		—	10	—	µS
$LOCK_{TOL}$	Frequency difference at which receiver PLL goes out of lock	SC_LOCK_DIFF[1:0] = 11	—	1200	—	ppm
		SC_LOCK_DIFF[1:0] = 10	—	600	—	ppm
		SC_LOCK_DIFF[1:0] = 01	—	1200	—	ppm
		SC_LOCK_DIFF[1:0] = 00	—	600	—	ppm
J_{TOL}	Receiver jitter tolerance		Exceeds SONET Jitter Tolerance Mask			
t_{ACQ}	Receiver PLL acquisition time		—	10	—	µS

Note: Reference clock input characteristics should meet the following requirements for SONET/SDH applications:
-125 dBc/HZ @ 1 MHz offset
-105 dBc/HZ @ 100 KHz offset

Electrical Characteristics (Continued)

Low Speed Input/Output Specifications
Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
AC Characteristics						
t_R	LVDS output rise times	See Figure 12.	—	120	250	ps
t_F	LVDS output fall times	See Figure 12.	—	120	250	ps
t_{CQB}	LVDS output data invalid prior to LVDS output clock	See Figure 15.	—	—	150	ps
t_{CQA}	LVDS output data invalid after LVDS output clock	See Figure 15.	—	—	150	ps
f_{CLKOUT}	LVDS output clock frequency, OC192 rate (CK622OUT_P/N, RX_CK_LV_P/N)		—	622.08	—	MHz
t_{DCCLK}	LVDS output clock frequency duty cycle (CK622OUT_P/N, RX_CK_LV_P/N)	t_{CKH}/t_{CKP} See Figure 13.	45	—	55	%
t_R	LVDS input rise times	See Figure 12.	—	—	300	ps
t_F	LVDS input fall times	See Figure 12.	—	—	300	ps
t_{SU}	LVDS input data setup to LVDS input clock	See Figure 13. TX_CK_LV_SEL =1, TX_CK_LV_PA[1:0]=11	260	—	—	ps
		t_{SU} See Figure 13. TX_CK_LV_SEL =0 and TX_CK_LV_PA[1:0]=11	320	—	—	ps
t_{HD}	LVDS input data hold from LVDS input clock	See Figure 13. TX_CK_LV_SEL =1 and TX_CK_LV_PA[1:0]=11	260	—	—	ps
		See Figure 13. TX_CK_LV_SEL =0 and TX_CK_LV_PA[1:0]=11	150	—	—	ps
f_{CLK}	LVDS input clock frequency at OC-192 rate (TX_CK_LV_P/N)	TX_CK_LV_SEL is no connect or high	—	622.08	—	MHz
		TX_CK_LV_SEL is connected to low	—	311.04	—	MHz
t_{DCCLK}	LVDS input clock frequency duty cycle (TX_CK_LV_P/N)	t_{CKH}/t_{CKP} See Figure 13.	45	—	55	%
DC Characteristics						
V_{OCM}	LVDS transmitter common mode range RX_D_LV_P/N[15:0], RX_CK_LV_P/N, TX_CK622_P/N)	100Ω load on line-to-line See Figure 11.	0.95	—	1.3	V
V_{OS}	LVDS single-ended output voltage swing (RX_D_LV_P/N[15:0], RX_CK_LV_P/N)	See Figure 11. 100Ω load on line-to-line, SC_LV_ISET[1:0]=11	100	—	165	mV (pk-pk)
		See Figure 11. 100Ω load on line-to-line, SC_LV_ISET[1:0]=10	50	—	100	mV (pk-pk)
		See Figure 11. 100Ω load on line-to-line, SC_LV_ISET[1:0]=01	80	—	125	mV (pk-pk)
		See Figure 11. 100Ω load on line-to-line, SC_LV_ISET[1:0]=00	130	—	210	mV (pk-pk)

Electrical Characteristics (Continued)

Low Speed Input/Output Specifications (Continued)

Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{ICM}	LVDS receiver common mode range (TX_D_LV_P/N[15:0], TX_CK_LV_P/N)	See Figure 11.	0.9	—	1.6	V
V_{IH}	LVDS input voltage HIGH (TX_D_LV_P/N[15:0], TX_CK_LV_P/N)		—	—	2.4	V
V_{IS}	LVDS single-ended input voltage swing (TX_D_LV_P/N[15:0], TX_CK_LV_P/N)	See Figure 11.	100	—	600	mV (pk-pk)

LVCMOS Input/Output Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{IH}	LVCMOS input high voltage		1.6	—	2.6	V
V_{IL}	LVCMOS input low voltage		0	—	0.8	V
I_{IH}	LVCMOS input high current		—	—	10	µA
I_{IL}	LVCMOS input low current		—	—	10	µA
V_{OH}	LVCMOS output high voltage	With 4mA load	2.0	—	2.5	V
V_{OL}	LVCMOS output low voltage	With 4mA load	0	—	0.4	V
I_{PU}	LVCMOS input pull-up current		90	—	170	µA

Power Supply Specifications

Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
P_D	Power dissipation		—	0.8	1.05	W
I_{DD13}[1]	1.3V supply current		—	390	460	mA
I_{DD25}[2]	2.5V supply current		—	130	160	mA

1. 1.3V power supplies, including VDDAR, VDDAT, VDDL, VDDT, VDDR.
2. 2.5V power supplies, including VDDAR25, VDDAT25, VDDH.

Common Pin Assignments and Descriptions[4]

Pad Name	Pin Description	Flip-chip BGA Ball Number[4]
GND[1, 3]	RX analog circuit ground	E16, K14, L14, M15
	TX analog circuit ground	F3, L5
	I/O ground	D8, D9, E8, F7, F8, G8, H7, H8, H9, H10, J8, J9, J10, K8, K9, K10, L9, L10, M10, N10, P10, R10, R11, R12
	Logic circuit ground	C1, D12, D13, J12, M12, M16, N7, N14, P14, P15, R1
	PLL ground	C12
	High-speed limit amplifier ground	F14, G13, H13, J14
	High-speed transmitter driver ground	F4, G5, H5, J4, K4, L4
VDDAR	RX analog circuit power	E11, F10, J15, J16
VDDAT	TX analog circuit power	M1, R8
VDDH	I/O power	C4, C5, C6, C7, C8, C9, C10, C11, D5, D10, D11, K11, L7, L8, L11, M6, M7, M8, M9, M11, N11, N12, P9, P11, P12
VDDL	Logic circuit power	D4, E6, L12, R15, E10
VDDR	High-speed limit amplifier power	F15, F16
VDDT	High-speed transmitter driver power	J2, J3, M3
VDDAR25	Reference circuit power	J11
VDDAT25	Reference circuit power	F1
NC[2]	No connect	C2, C14, C15, C16, C17, D1, D14, D16, E1, E2, E4, E7, E13, E14, F5, F6, F12, F13, F17, G4, G6, G10, G11, H4, H6, H12, J7, J13, J17, K5, K6, K7, K12, K13, L6, L13, M2, M13, N2, N3, N5, N8, N9, N17, P3, P4, P7, P16, P17, R2, R14

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{DD} or GND.
3. Balls for GND, VDDAR, VDDAT, VDDH, VDDL, VDDR, VDDT, VDDAR25 and VDDAT25 are connected within the substrate to their respective common signals.
4. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

Output Pin Assignments and Descriptions

Pin Name	Pin Description	Function	Flip-chip BGA Ball #
TX_D_N TX_D_P	10 Gbps CML transmit data. See Figure 5.	CML/ Out	K3 L3
TX_LOCK	TX PLL lock indicator: TX LOCK = 1, internal TX_CLK locked to REF_CLK; TX LOCK = 0, PLL is unlocked.	LVCMOS/ Out	D7
CK622OUT_N CK622OUT_P	622 MHz LVDS clock output. Phase is adjustable[1] and locks to CMU or CDR clock.[2]	LVDS/ Out	R4 R5
RX_CK_LV_P RX_CK_LV_N	LVDS clock output. Clock is source synchronous to the LVDS receive, runs at 622MHz and is phase adjustable.	LVDS/ Out	U9 T9
RX_D_LV_N[15], RX_D_LV_P[15], RX_D_LV_N[14], RX_D_LV_P[14], RX_D_LV_N[13], RX_D_LV_P[13], RX_D_LV_N[12], RX_D_LV_P[12], RX_D_LV_N[11], RX_D_LV_P[11], RX_D_LV_N[10], RX_D_LV_P[10], RX_D_LV_N[9], RX_D_LV_P[9], RX_D_LV_N[8], RX_D_LV_P[8], RX_D_LV_N[7], RX_D_LV_P[7], RX_D_LV_N[6], RX_D_LV_P[6], RX_D_LV_N[5], RX_D_LV_P[5], RX_D_LV_N[4], RX_D_LV_P[4], RX_D_LV_N[3], RX_D_LV_P[3], RX_D_LV_N[2], RX_D_LV_P[2], RX_D_LV_N[1],RX_D_LV_P[1], RX_D_LV_N[0], RX_D_LV_P[0]	LVDS data output. See Figure 8.	LVDS/ Out	T1, U1, T2, U2 T3, U3 T4, U4 T5, U5 T6, U6 T7, U7 T8, U8 T10, U10 T11, U11 T12, U12 T13, U13 T14, U14 T15, U15 T16, U16 T17, U17
RX_LOCK	Receiver PLL lock indicator. The PLL locks to REF_CK/RX_REF_CK. RX_LOCK = 1, receiver PLL frequency is within 300 ppm; RX_LOCK = 0, receiver PLL frequency is larger than 450 ppm; Frequency difference range is adjustable by SC_LOCK_DIFF[1:0].	LVCMOS/ Out	M17
RX_D_RP_P[3] RX_D_RP_N	10 Gbps CML output, repeat data. This output repeats the data at the RX_D_P/N inputs when RX_D_RP_Enb = 0. This output can be used for diagnostic purposes and to evaluate the receivers limiting amplifier. These pins can be left unconnected if unused.	CML/ Out	H14 G14
TX_FIFO_ERR	FIFO error. 1 = error, 0 = normal operation.	LVCMOS/ Out	D6

1. CMU mode only.
2. Based on RX_REF_CK_Enb
3. Operation above 10.3Gbps is not supported.
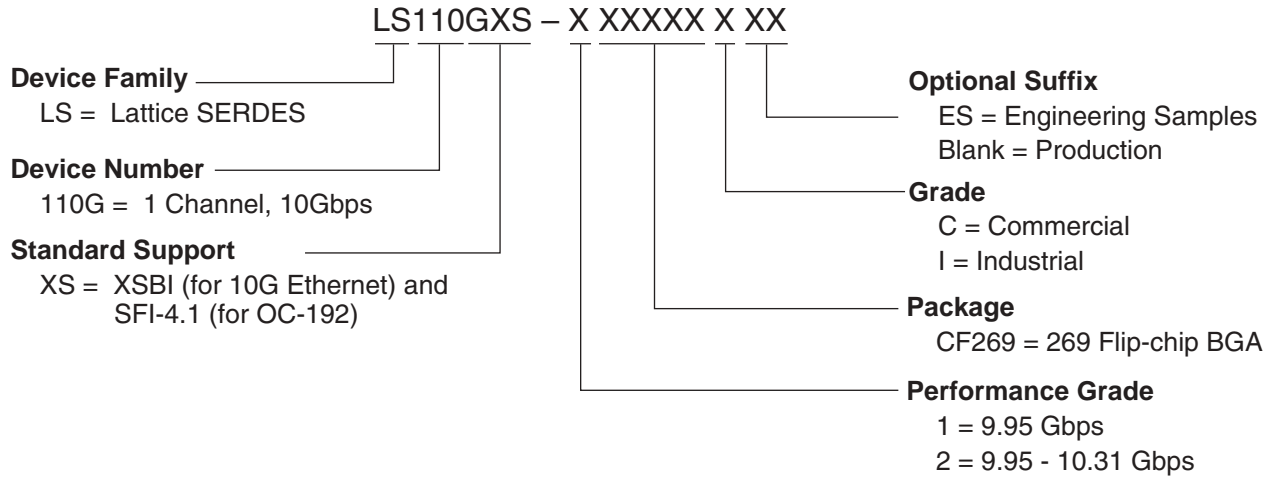
Input and Analog Pin Assignments and Descriptions[1]

Pin Name	Pin Description	Function	Flip-chip BGA Ball #
RX_D_P, RX_D_N	10 Gbps CML input.	CML/In	L15, K15
RX_REF_CK_P RX_REF_CK_N	LVPECL/CML 155/622 MHz reference clock for RX. See Figure 7.	CML/In or LVPECL/In	E17 D17
REF_CK_N[2] REF_CK_P	Transmitter reference clock input, see Figure 7. REF_CK is the CMU reference clock.	CML/In CML/In	N1 P1
TX_CK_LV_N, TX_CK_LV_P	LVDS TX clock, 622 MHz/311 MHz selectable, phase adjustable.	LVDS/In	B9, A9
TX_D_LV_N[15], TX_D_LV_P[15] TX_D_LV_N[14], TX_D_LV_P[14] TX_D_LV_N[13], TX_D_LV_P[13] TX_D_LV_N[12], TX_D_LV_P[12] TX_D_LV_N[11], TX_D_LV_P[11] TX_D_LV_N[10], TX_D_LV_P[10] TX_D_LV_N[9], TX_D_LV_P[9] TX_D_LV_N[8], TX_D_LV_P[8] TX_D_LV_N[7], TX_D_LV_P[7] TX_D_LV_N[6], TX_D_LV_P[6] TX_D_LV_N[5], TX_D_LV_P[5] TX_D_LV_N[4], TX_D_LV_P[4] TX_D_LV_N[3], TX_D_LV_P[3] TX_D_LV_N[2], TX_D_LV_P[2] TX_D_LV_N[1], TX_D_LV_P[1] TX_D_LV_N[0], TX_D_LV_P[0]	LVDS data input. See Figure 8.	LVDS/In	B17, A17 B16, A16 B15, A15 B14, A14 B13, A13 B12, A12 B11, A11 B10, A10 B8, A8 B7, A7 B6, A6 B5, A5 B4, A4 B3, A3 B2, A2 B1, A1
RX_FILT_EXTP RX_FILT_EXTN	RX External Filter. See Figure 9.	Analog	D15 E15
TX_FILT_EXTP TX_FILT_EXTN	TX External Filter. See Figure 9.	Analog	M4 N4
RX_REF_CK_Enb	RX reference clock enable.	LVCMOS/In	M14
RX_LV_CKDLY[0] RX_LV_CKDLY[1]	LVDS output clock delay programming.	LVCMOS/In	P13 R13
SC_LV_ISET[0] SC_LV_ISET[1]	LVDS output current settings.	LVCMOS/In	R16 R17
RX_LOS	RX loss of signal. When RX_LOS is asserted, LVDS clock RX_CK_LV_P/N is driven out, and the LVDS data pins are muted (i.e. at differential 0).	LVCMOS/In	G12
RX_LOS_POL	RX lose signal polarity change.	LVCMOS/In	R7
RX_D_RP_Enb	Receive data repeater enable.	LVCMOS/In	H11
RX_LOCK2REFb	RX PLL lock to reference. The RX PLL locks to the recovered data clock when this pin is unconnected/pulled high. The RX PLL locks to either RX_REF_CK or REF_CK depending on the state of RX_REF_CK_ENb.	LVCMOS/In	F11
SC_LOCK_DIFF[1] SC_LOCK_DIFF[0]	Lock indicate frequency resolution settings.	LVCMOS/In	N13 N15
RESET_TXb	Transmitter reset.	LVCMOS/In	F9
LB_P622_Enb	Loopback enabled at parallel 622 MHz port.	LVCMOS/In	E12
LB_LVDS_Enb	Loopback of TX 16b LVDS to RX 16b LVDS.	LVCMOS/In	C13
TX_FIFO_INIT	FIFO initialization.	LVCMOS/In	D3
SC_LSB1STb	SERDES LSB 1 first out selection.	LVCMOS/In	F2
TX_CML_ISET[1] TX_CML_ISET[0]	CML output current settings.	LVCMOS/In	J5 J1

Input and Analog Pin Assignments and Descriptions[1] (Continued)

Pin Name	Pin Description	Function	Flip-chip BGA Ball #
TX_CK_LV_PA[0] TX_CK_LV_PA[1]	LVDS TX clock adjustment for 622 MHz or 311 MHz mode.	LVCMOS/In	G7 C3
TX_D_EN	10 Gbps CML TX enable.	LVCMOS/In	J6
TX_CK622_PA[1] TX_CK622_PA[0]	CLK622 timing adjustment.	LVCMOS/In	P2 N6
PWDN_TXb	TX power down.	LVCMOS/In	P5
PWDN_RXb	RX power down.	LVCMOS/In	N16
RESET_RXb	RX reset.	LVCMOS/In	R6
CK622OUT_SEL	CK622 enable.	LVCMOS/In	P6
REF_CK_SEL	Ref CLK frequency selection.	LVCMOS/In	P8
RX_LV_EN	LVDS output enable.	LVCMOS/In	R9
TX_CP_ISET[1] [0]	TX charge pump current setting.	LVCMOS/In	R3, M5
TX_LV_PLLBPb	LVDS PLL bypass. Inverting phase of 622M clock TX_CK_LV_P/N is used to sample the input parallel data.	LVCMOS/In	E9
TX_CK_LV_SEL	Sets TX_CK_LV_P/N frequency.	LVCMOS/In	G9
BIST ENb	Enable built-in self test. Used for LVDS loopback.	LVCMOS/In	E5
BIST LB SC[1] [0]	Configures LVDS loopback		D2, E3

1. All LVCMOS/In pins have built-in pullup resistors.
2. REF_CK is the CDR reference clock when RX_REF_CK_Enb = 1.

Part Number Description

LS110GXS – X XXXXX X XX

Device Family
LS = Lattice SERDES

Device Number
110G = 1 Channel, 10Gbps

Standard Support
XS = XSBI (for 10G Ethernet) and
SFI-4.1 (for OC-192)

Optional Suffix
ES = Engineering Samples
Blank = Production

Grade
C = Commercial
I = Industrial

Package
CF269 = 269 Flip-chip BGA

Performance Grade
1 = 9.95 Gbps
2 = 9.95 - 10.31 Gbps

Ordering Information

Commercial

Part Number	Supported Data Rates (Gbps)	Voltage	Speed Grade	Package	Balls
LS110GXS-1CF269C	9.953	1.3V	-1	fcBGA	269
LS110GXS-2CF269C	9.953 to 10.31	1.3V	-2	fcBGA	269

Industrial

Part Number	Supported Data Rates (Gbps)	Voltage	Speed Grade	Package	Balls
LS110GXS-1CF269I	9.953	1.3V	-1	fcBGA	269