LDFM
LDFM50

500 mA very low drop voltage regulator

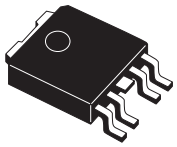
Datasheet – production data

Features

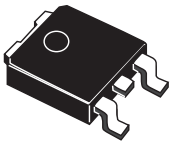
- Input voltage from 2.5 to 16 V
- Very low dropout voltage (300 mV max. at 500 mA load)
- Low quiescent current (200 µA typ. @ 500 mA load)
- Output voltage tolerance: ± 2% at 25 °C
- 500 mA guaranteed output current
- Wide range of output voltages available on request: adjustable from 0.8 V, fixed up to 12 V in 100 mV steps
- Logic-controlled electronic shutdown (PPAK)
- Power Good (on fixed versions in PPAK package)
- Fast dynamic response to line and load changes
- Internal current and thermal protection
- Temperature range: - 40 °C to 125 °C

Applications

- PCs and laptop computers
- Battery-powered equipment
- Industrial and medical equipment
- Portable equipment



PPAK



DPAK

Description

The LDFM is a fast, very low drop linear regulator which operates from an input supply voltage in the range of 2.5 V to 16 V.

It is available in fixed and adjustable output voltage versions, from 0.8 V to 12 V.

The LDFM features high output precision, very low dropout voltage, low noise, and low quiescent current, therefore suitable for low voltage microprocessors and memory applications.

Enable logic control pin and Power Good output are featured on the PPAK package.

Current and thermal protection are provided.

Table 1. Device summary

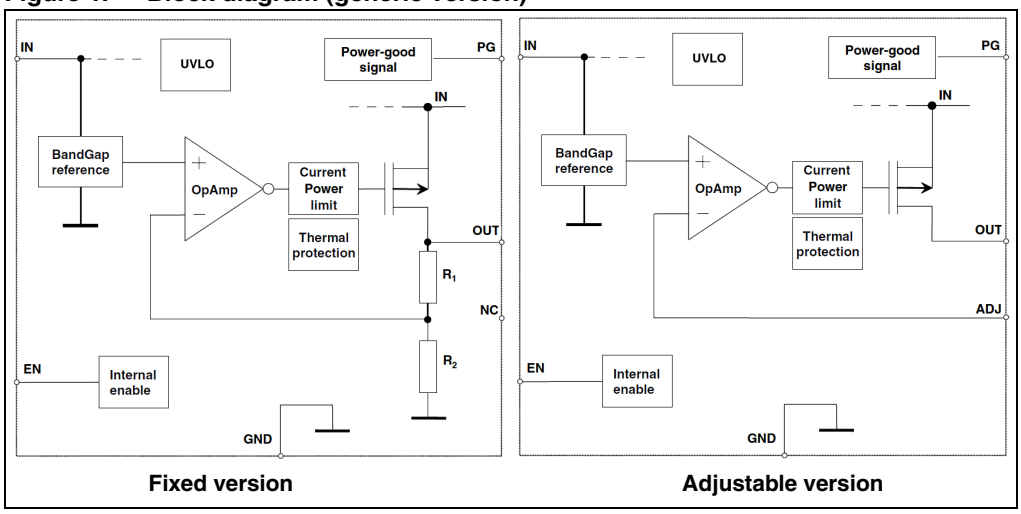
Part numbers	Order codes	Packages	Output voltages
LDFM50	LDFM50DT-TR	DPAK	5 V
LDFM50	LDFM50PT-TR	PPAK	5 V
LDFM	LDFMPT-TR	PPAK	Adjustable from 0.8 V

This is information on a product in full production. www.st.com

Contents

1 Block diagram

Figure 1. Block diagram (generic version)



2 Pin configuration

Figure 2. Pin connection (top view)

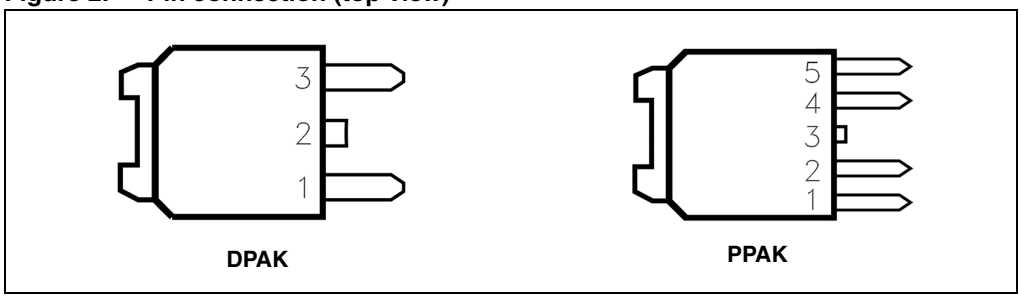
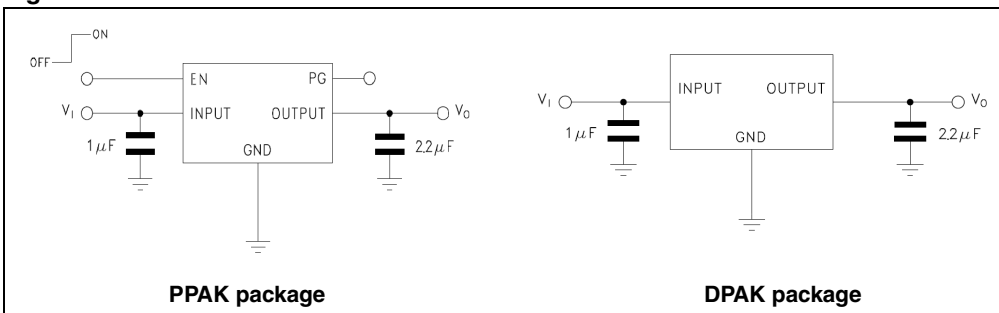


Table 2. Pin description

Pin n°		Symbol	Function
PPAK	DPAK		
5	-	ADJ/PG	For adjustable versions: Error amplifier input pin. For fixed version: Power Good output
2	1	V_{IN}	Input voltage
4	3	V_{OUT}	Output voltage
1	-	EN	Enable pin logic input: Low = shutdown, High = active
3	2	GND	Ground
TAB	TAB	GND	Ground

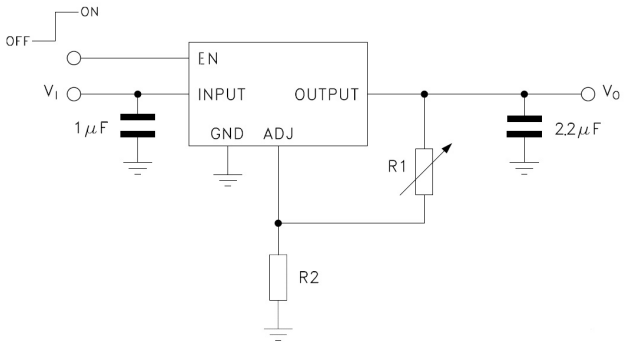
3 Typical application

Figure 3. Fixed versions



PPAK package DPAK package

Figure 4. Adjustable version (PPAK package)



$V_O = V_{REF} (1 + R_1/R_2)$

4 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	DC input voltage	- 0.3 to 20	V
V_{OUT}	DC output voltage	- 0.3 to V_{IN} + 0.3	V
V_{EN}	Enable input voltage	- 0.3 to V_{IN} + 0.3	V
V_{ADJ}	Adjust pin voltage	- 0.3 to 2	V
V_{PG}	Power Good pin voltage	- 0.3 to V_{IN} + 0.3	V
I_{LOAD}	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	- 65 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 125	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 4. Thermal data

Symbol	Parameter	Value		Unit
		PPAK	DPAK	
R_{thJA}	Thermal resistance junction-ambient	100	100	°C/W
R_{thJC}	Thermal resistance junction-case	8	8	°C/W

5 Electrical characteristics

T_J = 25 °C, V_{IN} = $V_{OUT(NOM)}$ + 1 V (1), C_{IN} = 1 µF, C_{OUT} = 2.2 µF, I_{LOAD} = 10 mA, V_{EN} = 2 V, unless otherwise specified.

Table 5. Electrical characteristics for LDFM50 (fixed versions)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		2.5		16	V
V_{OUT}	V_{OUT} accuracy	V_{OUT}+1 V(1)≤ V_{IN} ≤ 16 V I_{LOAD} = 10 mA	-2		2	%
		10 mA ≤ I_{LOAD} ≤ 500 mA T_J = -40 to 125 °C	-3		3	%
ΔV_{OUT}	Static line regulation	V_{OUT}+1 V(1)≤ V_{IN} ≤ 16 V		0.01		%/V
		V_{OUT}+1 V(1)≤ V_{IN} ≤ 16 V, T_J = -40 to 125 °C			0.04	
ΔV_{OUT}	Static load regulation	10 mA ≤ I_{LOAD} ≤ 500 mA		0.1		%/A
		10 mA ≤ I_{LOAD} ≤ 500 mA, T_J = -40 to 125 °C		0.15	0.4	
V_{DROP}	Dropout voltage (2)	I_{LOAD} = 500 mA, -40 °C<T_J<125 °C		125	300	mV
I_Q	Quiescent current	ON mode: V_{EN} = 2 V I_{LOAD} = 10 mA to 500 mA, T_J = -40 to 125 °C		200	800	µA
		OFF mode: V_{EN} = GND, PPAK version		50		µA
		OFF mode: V_{EN} = GND, PPAK version -40 °C<T_J<125 °C			300	
I_{SC}	Short-circuit current			0.8		A
V_{EN}	Enable input logic low	V_{IN} = 2.5 V to 16 V, -40 °C<T_J<125 °C			0.8	V
	Enable input logic high		2			
I_{EN}	Enable pin input current	V_{EN} = V_{IN}		5	10	µA
PG	Power Good output threshold	Rising edge		0.92* V_{OUT}		V
		Falling edge		0.8* V_{OUT}		
	Power Good output voltage low	I_{SINK} = 6 mA, open drain output		0.4		
SVR	Supply voltage rejection	V_{IN} = 6 V +/- 0.5 V_{RIPPLE} Freq. = 120 Hz, V_{OUT} = 5 V		60		dB
		V_{IN} = 6 V +/- 0.5 V_{RIPPLE} Freq. = 10 kHz, V_{OUT} = 5 V		52		

Table 5. Electrical characteristics for LDFM50 (fixed versions)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
e_N	Output noise voltage	Bw = 10 Hz to 100 kHz, I_{LOAD} = 100 mA. C_{OUT} = 2.2 µF		45		$\mu V_{RMS}/V_{OUT}$
T_{SHDN}	Thermal shutdown			170		°C
	Hysteresis			10		

1. For V_{OUT} < 1.5 V; V_{IN} = 2.5 V.
2. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply for output voltages below 1.5 V.

T_J = 25 °C, $V_{IN} = V_{OUT(NOM)}$ + 1 V (1), C_{IN} = 1 µF, C_{OUT} = 2.2 µF, I_{LOAD} = 10 mA, V_{EN} = 2 V, unless otherwise specified.

Table 6. Electrical characteristics for LDFM (adjustable version)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		2.5		16	V
V_{ADJ}	Reference voltage	$V_{IN} = V_{OUT}$+1 V(1)		0.8		V
	Reference voltage tolerance	V_{OUT}+1 V(1) ≤ V_{IN} ≤ 16 V I_{LOAD} = 10 mA	-2		2	%
		10 mA ≤ I_{LOAD} ≤ 500 mA T_J = -40 to 125 °C	-3		3	
ΔV_{OUT}	Static line regulation	V_{OUT}+1 V(1)≤ V_{IN} ≤ 16 V		0.01		%/V
		V_{OUT}+1 V(1)≤ V_{IN} ≤ 16 V, T_J = -40 to 125 °C			0.04	
ΔV_{OUT}	Static load regulation	10 mA ≤ I_{LOAD} ≤ 500 mA		0.06		%/A
		10 mA ≤ I_{LOAD} ≤ 500 mA, T_J = -40 to 125 °C		0.2	0.4	
V_{DROP}	Dropout voltage (2)	V_{OUT} fixed to 2.5 V, I_{LOAD} = 500 mA, -40 °C<T_J<125 °C		125	300	mV
I_Q	Quiescent current	ON mode: V_{EN} = 2 V I_{LOAD} = 10 mA to 500 mA, T_J = -40 to 125 °C		200	800	µA
		OFF mode: V_{EN} = GND, PPAK version		50		µA
		OFF mode: V_{EN} = GND, PPAK version -40 °C<T_J<125 °C			200	
I_{SC}	Short-circuit current			0.8		A
V_{EN}	Enable input logic low	V_{IN}= 2.5 V to 16 V, -40 °C<T_J<125 °C			0.8	V
	Enable input logic high		2			
I_{EN}	Enable pin input current	$V_{EN} = V_{IN}$		5	10	µA

Table 6. Electrical characteristics for LDFM (adjustable version)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PG	Power Good output threshold	Rising edge		0.92* V_{ADJ}		V
		Falling edge		0.8* V_{ADJ}		
	Power Good output voltage low	I_{SINK} = 6 mA, open drain output		0.4		
SVR	Supply voltage rejection	$V_{IN} = V_{OUT}$+1 V +/- 0.5 V_{RIPPLE} Freq. = 120 Hz, V_{OUT} = 0.8 V		62		dB
		$V_{IN} = V_{OUT}$+1 V +/- 0.5 V_{RIPPLE} Freq. = 10 kHz, V_{OUT} = 0.8 V		55		
e_N	Output noise voltage	Bw = 10 Hz to 100 kHz, I_{LOAD} = 100 mA. C_{OUT} = 2.2 µF		50		μV_{RMS} /V_{OUT}
T_{SHDN}	Thermal shutdown			170		°C
	Hysteresis			10		

1. For V_{OUT}<1.5 V; V_{IN} = 2.5 V.
2. Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value. This specification does not apply for output voltages below 1.5 V.

6 Application information

6.1 External capacitors

The LDFM requires external capacitors for regulator stability. These capacitors must be selected to meet the requirements of minimum capacitance and equivalent series resistance (see *Figure 26 and 27*). It is advisable to locate the input/output capacitors as close as possible to the relative pins.

6.1.1 Input capacitor

An input capacitor with a minimum value of 1 µF is required with the LDFM. This capacitor must be located a distance of not more than 0.5" from the input pin of the device and returned to a clean analog ground. Any good quality ceramic capacitors can be used for this capacitor.

6.1.2 Output capacitor

It is possible to use ceramic capacitors but the output capacitor must meet the requirements for minimum amount of capacitance and E.S.R. (equivalent series resistance) value.

A minimum capacitance of 2.2 µF is a good choice to guarantee the stability of the regulator. However, other C_{OUT} values can be used according to *Figure 26 and 27,* showing the allowable ESR range as a function of the output capacitance.

The output capacitor must maintain its ESR in the stable region over the full operating temperature range to assure stability. Also, capacitor tolerance and variation with temperature must be kept in consideration in order to assure the minimum amount of capacitance at all times.

6.2 Enable pin operation

The Enable pin can be used to turn OFF the regulator when pulled down, so drastically reducing the current consumption. When the enable feature is not used, this pin must be tied to V_{IN} to keep the regulator output ON at all times. To assure proper operation, the signal source used to drive the Enable pin must be able to swing above and below the specified thresholds listed in the electrical characteristics section (V_{EN}). The Enable pin must not be left floating because it is not internally pulled down/up.

6.3 Power Good

The LDFM features an open drain Power Good (PG) pin to sequence external supplies or loads and to provide fault detection. This pin requires an external resistor (R_{PG}) to pull PG high when the output is within the PG tolerance window. Typical values for this resistor range from 10 k to 100 k.

7 Typical performance characteristics

$C_{IN} = C_{OUT} = 1\ \mu F$, $V_{IN} = V_{OUT} + 1$ V, V_{EN} to V_{IN}, $I_{OUT} = 10$ mA, unless otherwise specified.

Figure 5. Output voltage vs. temperature

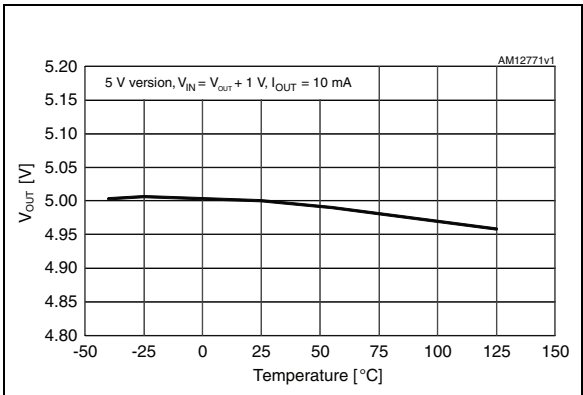


Figure 6. Output voltage vs. temperature for adjustable

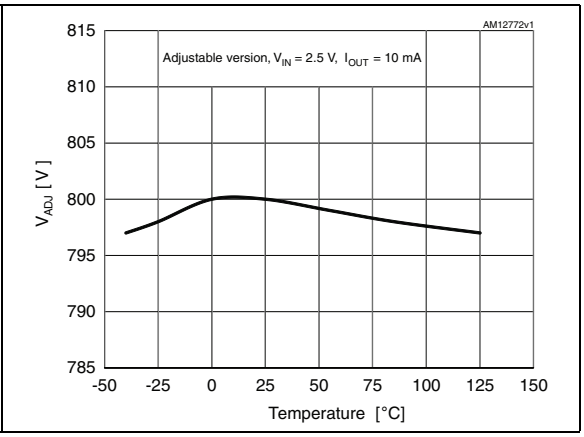


Figure 7. Line regulation vs. temperature

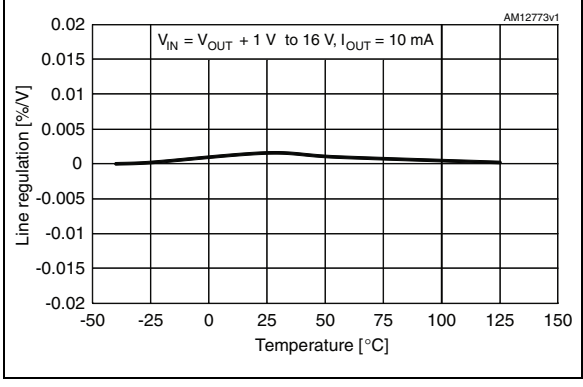


Figure 8. Load regulation vs. temperature

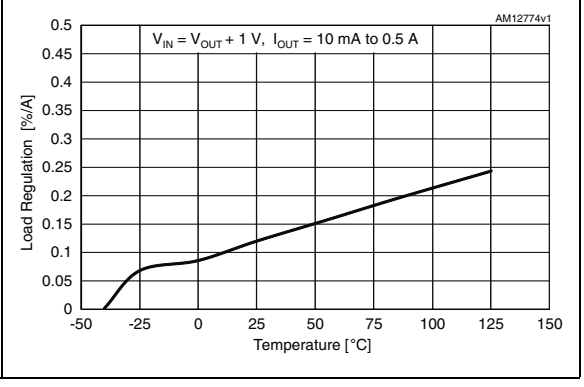


Figure 9. Short-circuit current vs. drop voltage

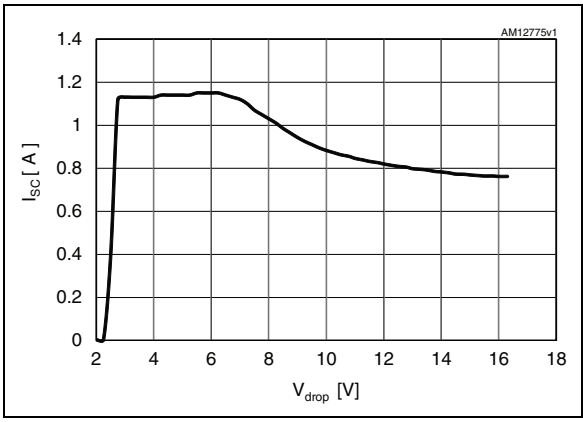


Figure 10. Dropout voltage vs. temperature

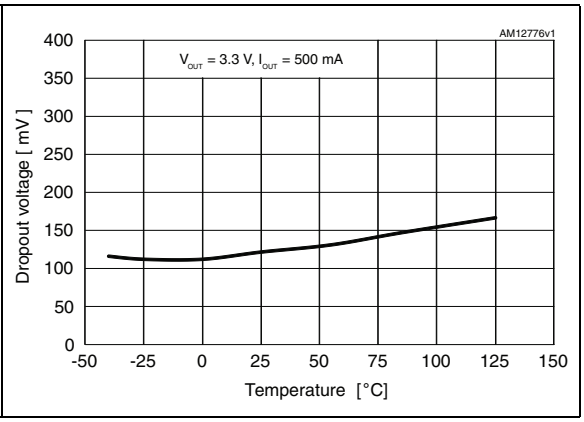


Figure 11. Quiescent current vs. temperature (I_O = 0 mA)

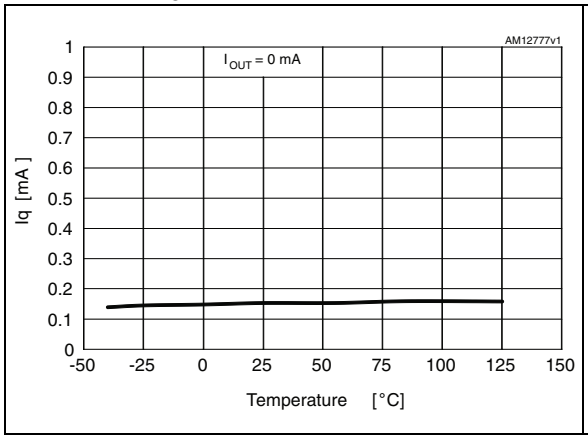


Figure 12. Quiescent current vs. temperature (I_O = 500 mA)

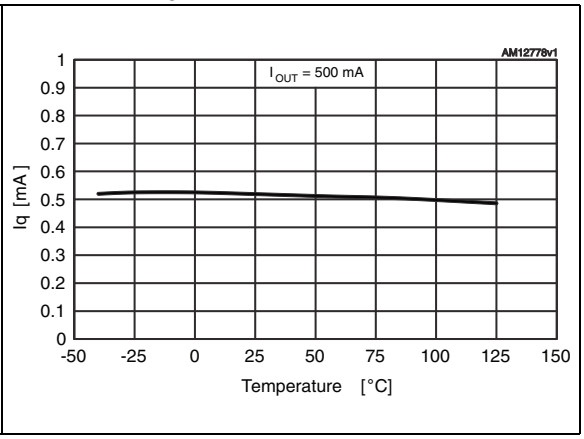


Figure 13. Shutdown current vs. temperature

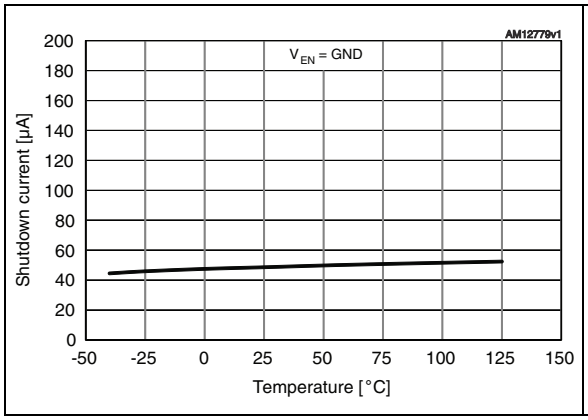


Figure 14. Enable pin current vs. temperature

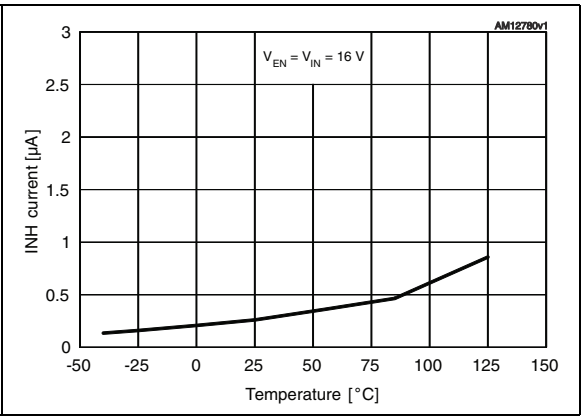


Figure 15. Enable high threshold vs. temperature

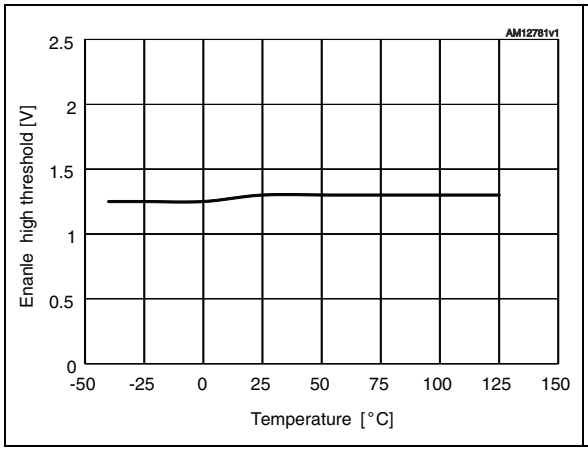


Figure 16. Enable low threshold vs. temperature

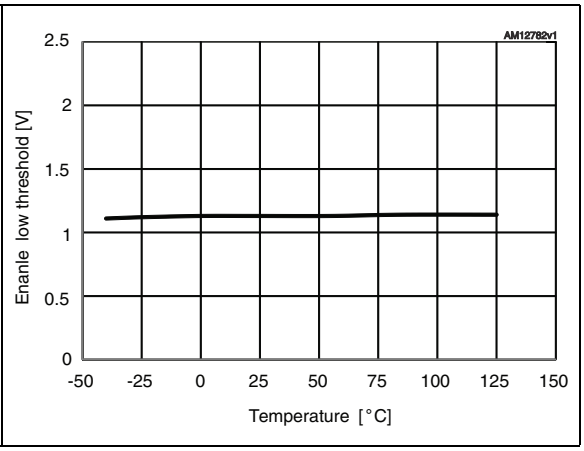


Figure 17. Output voltage vs. input voltage

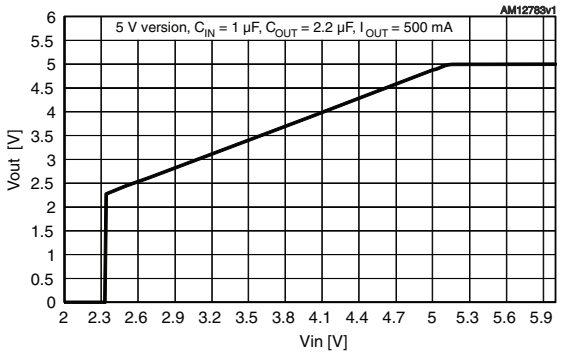
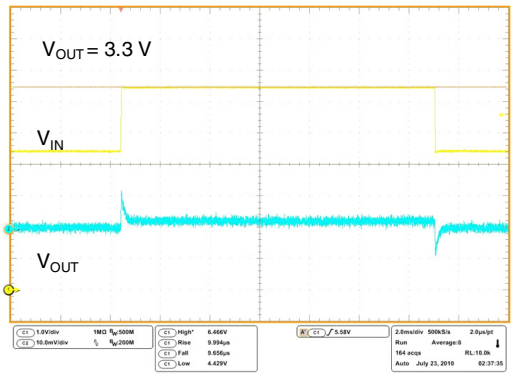
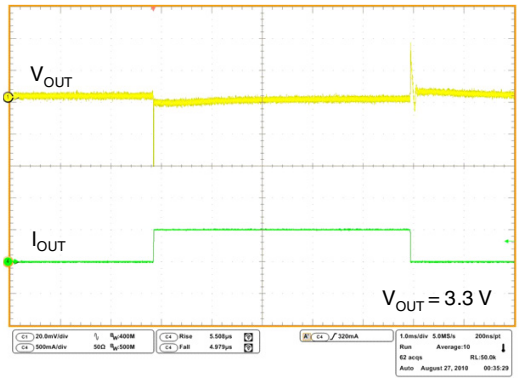


Figure 18. Line transient



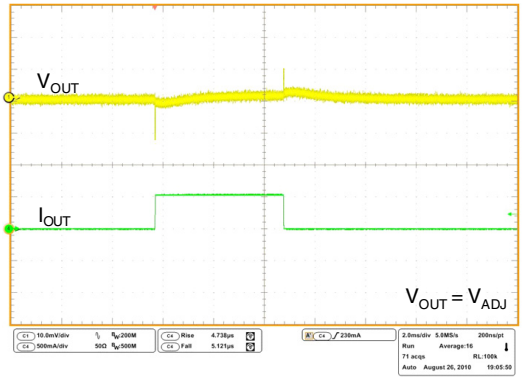
V_{IN} = from 4.5 to 6.5 V, I_{OUT} = 10 mA, t_{rise} = t_{fall} = 10 µs, C_{OUT} = 2.2 µF

Figure 19. Load transient (V_{OUT} = 3.3 V)



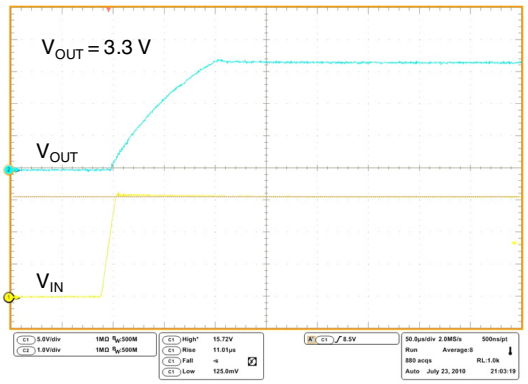
V_{EN} = V_{IN} = 4.5 V, I_{OUT} = from 1 to 500 mA, t_{rise} = t_{fall} = 5 µs, C_{OUT} = 2.2 µF

Figure 20. Load transient (V_{OUT} = V_{ADJ})



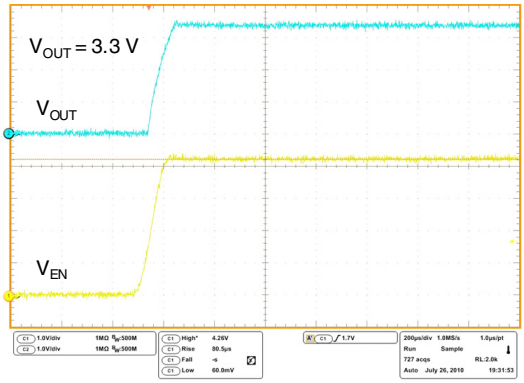
V_{EN} = V_{IN} = 4.5 V, I_{OUT} = from 1 to 500 mA, t_{rise} = t_{fall} = 5 µs, C_{OUT} = 2.2 µF

Figure 21. Startup transient



V_{EN} = V_{IN} = from 0 to 16 V, I_{OUT} = 10 mA, t_{rise} = 10 µs, C_{OUT} = 2.2 µF

Figure 22. Enable transient



V_{IN} = 4.3 V, V_{EN} = from 0 to 4.3 V, I_{OUT} = 10 mA, t_{rise} = 100 µs, C_{OUT} = 2.2 µF

Figure 23. SVR vs. frequency (V_{OUT} = 5 V)

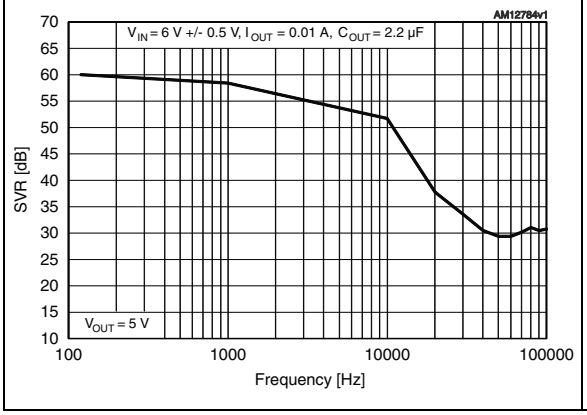


Figure 24. SVR vs. frequency (V_{OUT} = V_{ADJ})

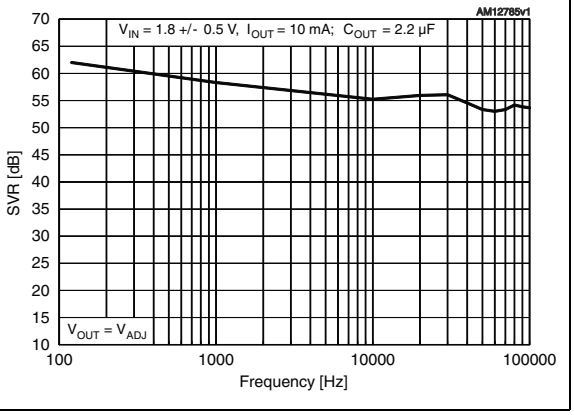


Figure 25. Stability plane adj (C_{OUT}, ESR)

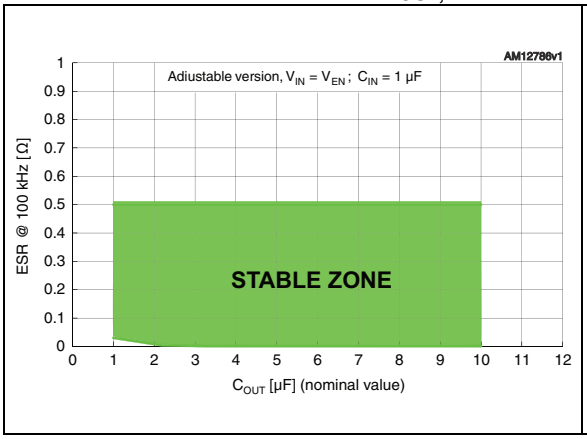
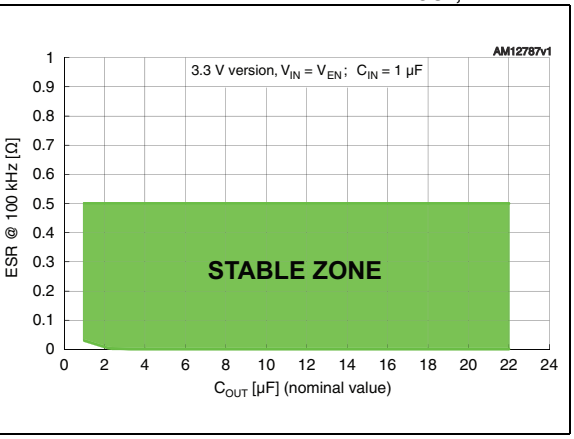


Figure 26. Stability plane 3.3 V (C_{OUT}, ESR)



8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

Table 7. DPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 27. DPAK drawing

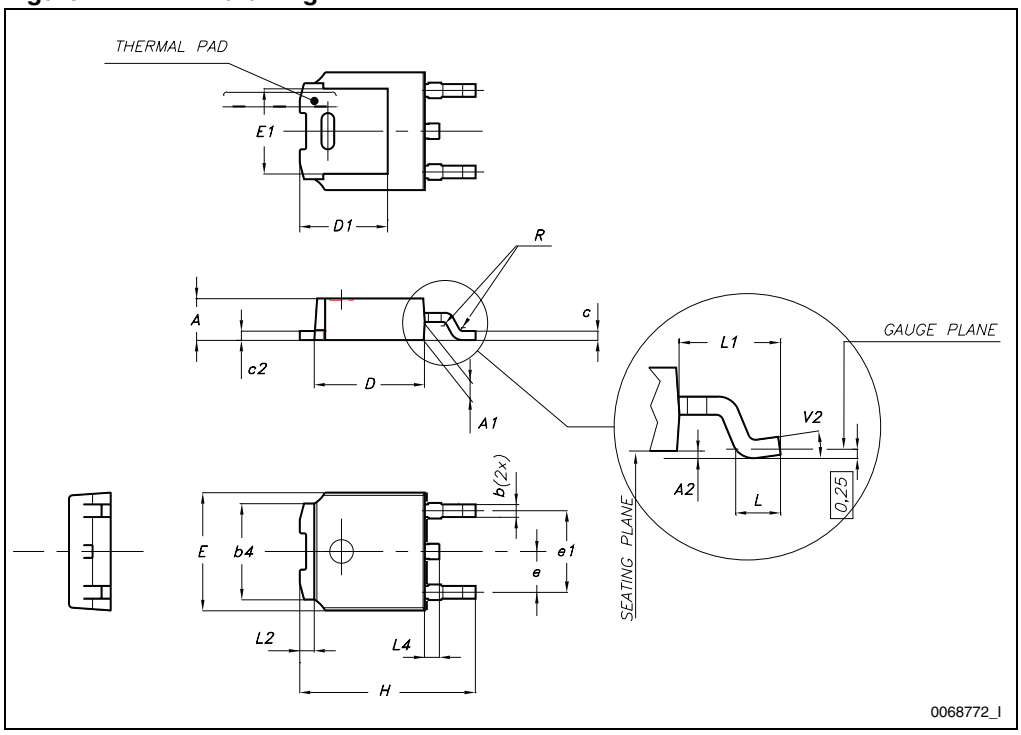
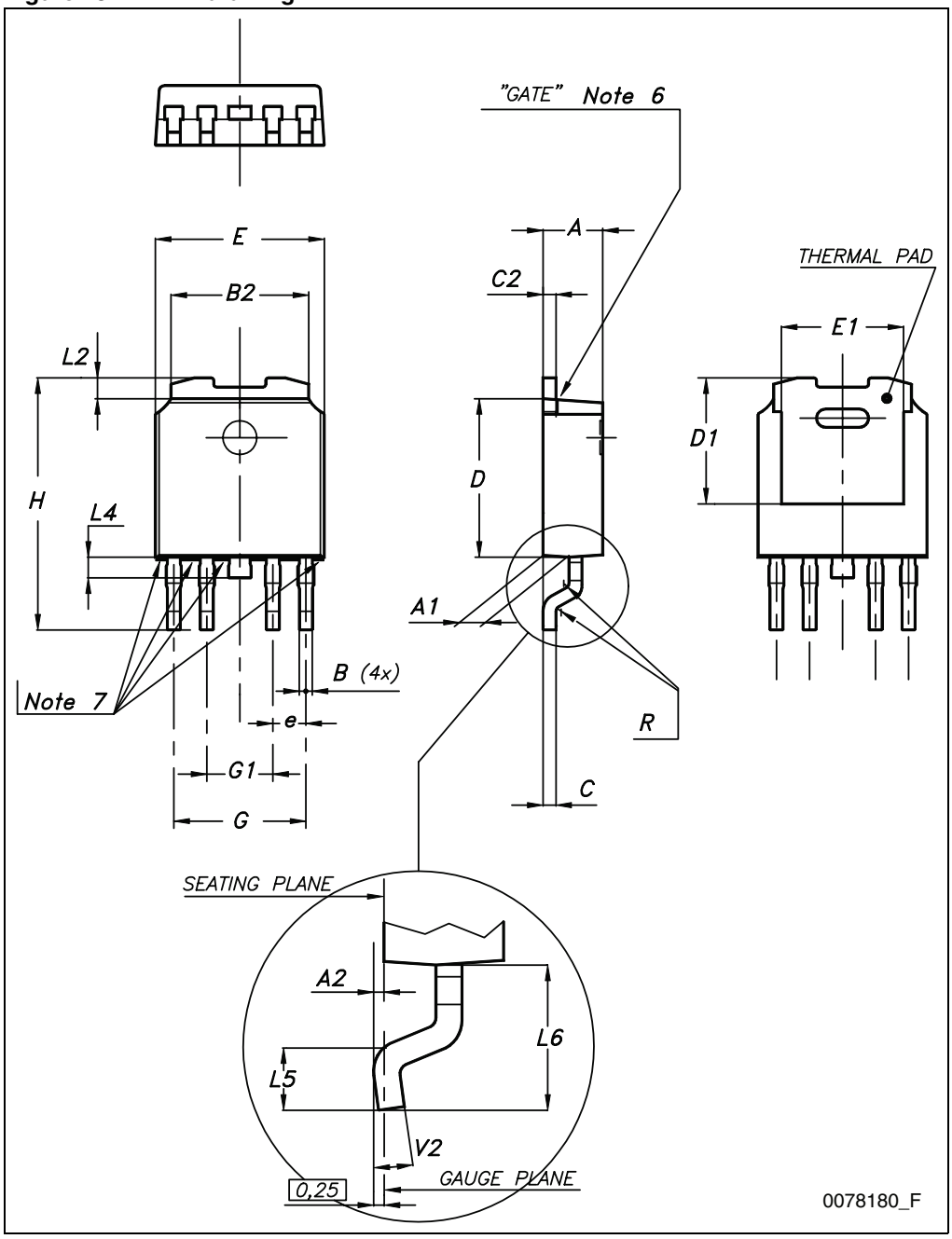


Table 8. PPAK mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.2		2.4
A1	0.9		1.1
A2	0.03		0.23
B	0.4		0.6
B2	5.2		5.4
C	0.45		0.6
C2	0.48		0.6
D	6		6.2
D1		5.1	
E	6.4		6.6
E1		4.7	
e		1.27	
G	4.9		5.25
G1	2.38		2.7
H	9.35		10.1
L2		0.8	1
L4	0.6		1
L5	1		
L6		2.8	
R		0.20	
V2	0°		8°

Figure 28. PPAK drawing



9 Revision history

Table 9. Document revision history

Date	Revision	Changes
28-Aug-2012	1	Initial release.