16-bit edge-triggered D-type flip-flop; 5 V tolerant; 3-state

Rev. 11 — 16 January 2013

**Product data sheet** 

## 1. General description

The 74LVC16374A and 74LVCH16374A are 16-bit edge-triggered flip-flops featuring separate D-type inputs with bus hold (74LVCH16374A only) for each flip-flop and 3-state outputs for bus-oriented applications. It consists of two sections of eight positive edge-triggered flip-flops. A clock input (nCP) and an output enable (nOE) are provided for each octal.

The flip-flops store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition.

When pin  $n\overline{OE}$  is LOW, the contents of the flip-flops are available at the outputs. When pin  $n\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of input  $n\overline{OE}$  does not affect the state of the flip-flops.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

Bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

### 2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Multibyte flow-through standard pinout architecture
- Low inductance multiple supply pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH16374A only)
- High-impedance outputs when V<sub>CC</sub> = 0 V
- Complies with JEDEC standard:
  - ◆ JESD8-7A (1.65 V to 1.95 V)
  - ◆ JESD8-5A (2.3 V to 2.7 V)
  - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ♦ HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-B exceeds 200 V
  - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

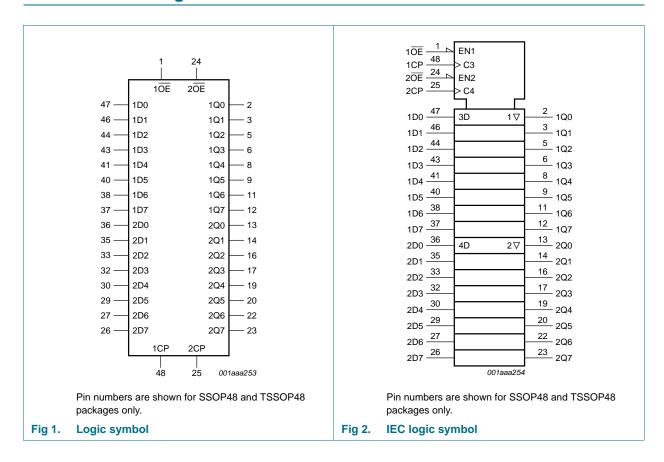


# 3. Ordering information

Table 1. Ordering information

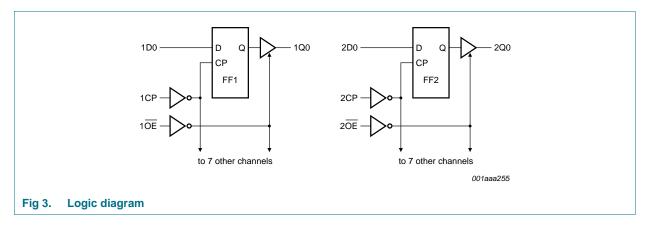
Type number	Package			
	Temperature range	Name	Description	Version
74LVC16374ADL	–40 °C to +125 °C	SSOP48	plastic shrink small outline package; 48 leads;	SOT370-1
74LVCH16374ADL			body width 7.5 mm	
74LVC16374ADGG	–40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package;	SOT362-1
74LVCH16374ADGG			48 leads; body width 6.1 mm	
74LVC16374ABX	−40 °C to +125 °C	HXQFN60U	plastic thermal enhanced extremely thin quad flat	SOT1134-1
74LVCH16374ABX			package; no leads; 60 terminals; UTLP based; body $4 \times 6 \times 0.5$ mm	

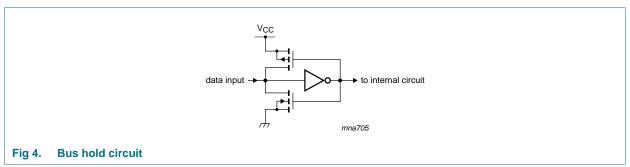
# 4. Functional diagram



74LVC\_LVCH16374A

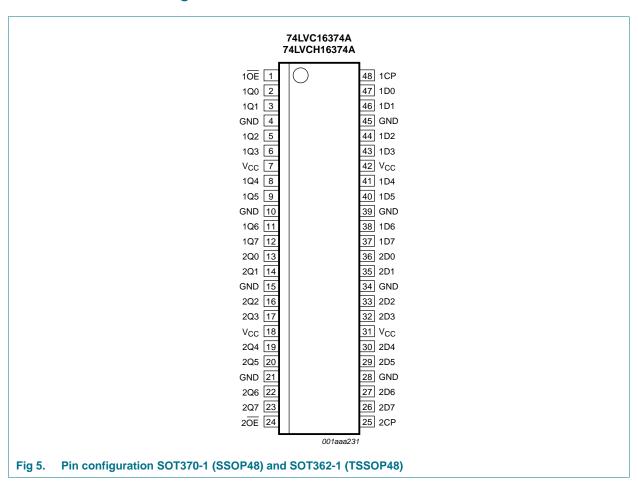
Downloaded from Elcodis.com electronic components distributor





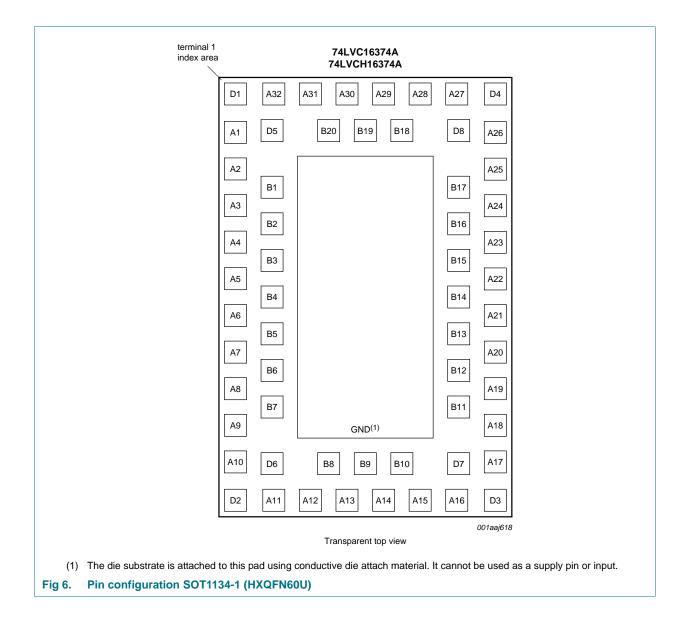
# 5. Pinning information

### 5.1 Pinning



74LVC\_LVCH16374A

Downloaded from Elcodis.com electronic components distributor



74LVC\_LVCH16374A

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Pin				
	SOT370-1 and SOT362-1	SOT1134-1				
10E, 20E	1, 24	A30, A13	output enable input (active LOW)			
GND	4, 10, 15, 21, 28, 34, 39, 45	A32, A3, A8, A11, A16, A19, A24, A27	ground (0 V)			
$V_{CC}$	7, 18, 31, 42	A1, A10, A17, A26	supply voltage			
1Q0 to 1Q7	2, 3, 5, 6, 8, 9, 11, 12	B20, A31, D5, D1, A2, B2, B3, A5	data output			
2Q0 to 2Q7	13, 14, 16, 17, 19, 20, 22, 23	A6, B5, B6, A9, D2, D6, A12, B8	data output			
1D0 to 1D7	47, 46, 44, 43, 41, 40, 38, 37	B18, A28, D8, D4, A25, B16, B15, A22	data input			
2D0 to 2D7	36, 35, 33, 32, 30, 29, 27, 26	A21, B13, B12, A18, D3, D7, A15, B10	data input			
1CP, 2CP	48, 25	A29, A14	clock input			

# 6. Functional description

Table 3. Function selection[1]

Operating mode	Input			Internal flip-flop	Output nQ0 to nQ7
	nOE	nCP	nDn		
Load and read register	L	<b>↑</b>	I	L	L
	L	<b>↑</b>	h	Н	Н
Load register and disable outputs	Н	<b>↑</b>	I	L	Z
	Н	<b>↑</b>	h	Н	Z

<sup>[1]</sup> H = HIGH voltage level;

h = HIGH voltage level one set-up time prior to the HIGH-to-LOW CP transition;

I = LOW voltage level one set-up time prior to the HIGH-to-LOW CP transition;

# 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
V <sub>I</sub>	input voltage		[ <u>1</u> ] -0.5	+6.5	V
l <sub>OK</sub>	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	±50	mA
Vo	output voltage	output HIGH-or LOW-state	<sup>[2]</sup> -0.5	$V_{CC} + 0.5$	V
		output 3-state	[ <u>2</u> ] -0.5	+6.5	V
Io	output current	$V_O = 0 V \text{ to } V_{CC}$	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
74LVC_LVCH16374A		All information provided in this document is subject to legal discla	imers.	© NXP B.V	. 2013. All rights reserved

Product data sheet Rev. 1

Rev. 11 — 16 January 2013

6 of 20

L = LOW voltage level;

<sup>↑ =</sup> LOW-to-HIGH transition;

Z = high-impedance OFF-state.

16-bit edge-triggered D-type flip-flop; 5 V tolerant; 3-state

Table 4. Limiting values ...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P <sub>tot</sub> total power dissipation		$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$			
		(T)SSOP48 package	<u>[3]</u> _	500	mW
		HXQFN60U package	<u>[4]</u> _	1000	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
- [2] The output voltage ratings may be exceeded if the output current ratings are observed.
- [3] Above 60 °C, the value of Ptot derates linearly with 5.5 mW/K.
- [4] Above 70 °C, the value of  $P_{tot}$  derates linearly with 1.8 mW/K.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{CC}$	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
VI	input voltage		0	-	5.5	V
Vo	output voltage	active mode	0	-	$V_{CC}$	V
		power-down mode; $V_{CC} = 0 \text{ V}$	0	-	5.5	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 1.65 \text{ V to } 2.7 \text{ V}$	0	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	-	10	ns/V

### 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	<b>-40</b>	°C to +8	5 °C	–40 °C to	Unit	
			Min	Typ[1]	Max	Min	Max	
$V_{IH}$	HIGH-level	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
	input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2.0	-	-	2.0	-	V
$V_{IL}$	LOW-level	$V_{CC} = 1.2 \text{ V}$	-	-	0.12	-	0.12	V
	input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	8.0	V

 Table 6.
 Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +85	S°C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$	1					
	output voltage	$I_O = -100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	V <sub>CC</sub> - 0.2	$V_{CC}$	-	$V_{CC}-0.3$	-	V
		$I_O = -4 \text{ mA}$ ; $V_{CC} = 1.65 \text{ V}$	1.2	-	-	1.05	-	V
		$I_{O} = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.8	-	-	1.65	-	V
		$I_{O} = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	2.05	-	V
		$I_{O} = -18 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.4	-	-	2.25	-	V
		$I_{O} = -24$ mA; $V_{CC} = 3.0$ V	2.2	-	-	2.0	-	V
$V_{OL}$	LOW-level	$V_I = V_{IH}$ or $V_{IL}$						
	output voltage	$I_O = 100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	-	0	0.2	-	0.3	V
		$I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.65	V
		$I_O = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.6	-	0.8	V
		$I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	8.0	V
lı	input leakage current	$V_{CC} = 3.6 \text{ V}; V_{I} = 5.5 \text{ V or GND}$ [2]	-	±0.1	±5	-	±20	μΑ
OZ	OFF-state output current	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 3.6 \text{ V};$ $V_O = 5.5 \text{ V or GND } \boxed{2}$	-	±0.1	±5	-	±20	μΑ
OFF	power-off leakage current	$V_{CC} = 0 \text{ V}$ ; $V_{I}$ or $V_{O} = 5.5 \text{ V}$	-	±0.1	±10	-	±20	μΑ
lcc	supply current	$V_{CC} = 3.6 \text{ V}; V_I = V_{CC} \text{ or GND};$ $I_O = 0 \text{ A}$	-	0.1	20	-	80	μΑ
Δl <sub>CC</sub>	additional supply current	per input pin; $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V};$ $V_{I} = V_{CC} - 0.6 \text{ V};$ $I_{O} = 0 \text{ A}$	-	5	500	-	5000	μА
Cı	input capacitance	$V_{CC} = 0 \text{ V to } 3.6 \text{ V};$ $V_{I} = \text{GND to } V_{CC}$	-	5.0	-	-	-	pF
BHL	bus hold	$V_{CC} = 1.65$ ; $V_I = 0.58 \text{ V}$ [3][4]	10	-	-	10	-	μΑ
	LOW current	$V_{CC} = 2.3; V_I = 0.7 V$	30	-	-	25	-	μΑ
		$V_{CC} = 3.0$ ; $V_I = 0.8 \text{ V}$	75	-	-	60	-	μΑ
ВНН	bus hold	$V_{CC} = 1.65$ ; $V_I = 1.07 \text{ V}$ [3][4]	-10	-	-	-10	-	μΑ
	HIGH current	$V_{CC} = 2.3; V_I = 1.7 V$	-30	-	-	-25	-	μΑ
		$V_{CC} = 3.0$ ; $V_{I} = 2.0 \text{ V}$	-75	-	-	-60	-	μΑ
BHLO	bus hold	V <sub>CC</sub> = 1.95 V [3][5]	200	-	-	200	-	μΑ
	LOW	V <sub>CC</sub> = 2.7 V	300	-	-	300	-	μΑ
overdrive current		V <sub>CC</sub> = 3.6 V	500	-	-	500	-	μΑ

74LVC\_LVCH16374A

All information provided in this document is subject to legal disclaimers.

16-bit edge-triggered D-type flip-flop; 5 V tolerant; 3-state

Table 6. Static characteristics ... continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	–40 °C to +85 °C			-40 °C to +125 °C		
			Min	Typ[1]	Max	Min	Max		
$I_{BHHO}$	bus hold	$V_{CC} = 1.95 \text{ V} \frac{[3][5]}{}$	-200	-	-	-200	-	μΑ	
	HIGH overdrive	$V_{CC} = 2.7 \text{ V}$	-300	-	-	-300	-	μΑ	
	current	$V_{CC} = 3.6 \text{ V}$	-500	-	-	-500	-	μΑ	

- [1] All typical values are measured at  $V_{CC}$  = 3.3 V (unless stated otherwise) and  $T_{amb}$  = 25 °C.
- [2] The bus hold circuit is switched off when  $V_I > V_{CC}$  allowing 5.5 V on the input pin.
- [3] Valid for data inputs (74LVCH16374A) only; control inputs do not have a bus hold circuit.
- [4] The specified sustaining current at the data inputs holds the input below the specified V<sub>I</sub> level.
- [5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

## 10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 10.

Symbol	Parameter	Conditions		-40	°C to +8	5 °C	-40 °C to	+125 °C	Unit
				Min	Typ[1]	Max	Min	Max	
t <sub>pd</sub>	propagation	nCP to nQn; see Figure 7	[2]						
	delay	V <sub>CC</sub> = 1.2 V		-	14	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V		2.1	6.9	13.5	2.1	15.6	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V		1.5	3.7	6.7	1.5	7.7	ns
		V <sub>CC</sub> = 2.7 V		1.5	3.4	6.0	1.5	7.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V		1.5	3.1	5.4	1.5	7.0	ns
t <sub>en</sub>	enable time	nOE to nQn; see Figure 9	[2]						
		V <sub>CC</sub> = 1.2 V		-	20	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V		1.5	5.9	13.1	1.5	15.1	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V		1.5	3.4	6.9	1.5	8.0	ns
		V <sub>CC</sub> = 2.7 V		1.5	3.6	6.0	1.5	7.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V		1.0	2.7	5.2	1.0	6.5	ns
t <sub>dis</sub>	disable time	nOE to nQn; see Figure 7	[2]						
		V <sub>CC</sub> = 1.2 V		-	12	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V		2.8	4.6	9.1	2.8	10.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V		1.0	2.5	4.9	1.0	5.7	ns
		V <sub>CC</sub> = 2.7 V		1.5	3.4	5.1	1.5	6.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V		1.5	3.1	4.9	1.5	6.5	ns
t <sub>W</sub>	pulse width	nCP HIGH; see Figure 7							
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		5.0	-	-	5.0	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		4.0	-	-	4.0	-	ns
		$V_{CC} = 2.7 \text{ V}$		3.0	-	-	3.0	-	ns
		$V_{CC}$ = 3.0 V to 3.6 V		3.0	1.5	-	3.0	-	ns

74LVC\_LVCH16374A

All information provided in this document is subject to legal disclaimers.

 Table 7.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 10.

Symbol	Parameter	Conditions		-40	°C to +8	5 °C	-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
$t_{su}$	set-up time	nDn to nCP; see Figure 8							
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		4.0	-	-	4.0	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		3.0	-	-	3.0	-	ns
		$V_{CC} = 2.7 V$		1.9	-	-	1.9	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.9	0.3	-	1.9	-	ns
t <sub>h</sub>	hold time	nDn to nCP; see Figure 8							
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		3.0	-	-	3.0	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		2.5	-	-	2.5	-	ns
		$V_{CC} = 2.7 \text{ V}$		1.1	-	-	1.1	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		+1.5	-0.3	-	1.5	-	ns
f <sub>max</sub>	maximum	see Figure 7							
	frequency	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		100	-	-	80	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		125	-	-	100	-	ns
		$V_{CC} = 2.7 \text{ V}$		150	-	-	120	-	MHz
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		150	300	-	120	-	MHz
t <sub>sk(o)</sub>	output skew time	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[3]	-	-	1.0	-	1.5	ns
$C_{PD}$	power	per input; $V_I = GND$ to $V_{CC}$	<u>[4]</u>						
	dissipation	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		-	14.1	-	-	-	pF
	capacitance	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		-	16.4	-	-	-	pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		-	18.5	-	-	-	pF

<sup>[1]</sup> Typical values are measured at  $T_{amb}$  = 25 °C and  $V_{CC}$  = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

 $t_{\text{en}}$  is the same as  $t_{\text{PZL}}$  and  $t_{\text{PZH}}.$ 

 $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[4]  $C_{PD}$  is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu$ W).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz

 $C_L$  = output load capacitance in pF

V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

 $\Sigma (C_L \times V_{CC}{}^2 \times f_o)$  = sum of the outputs

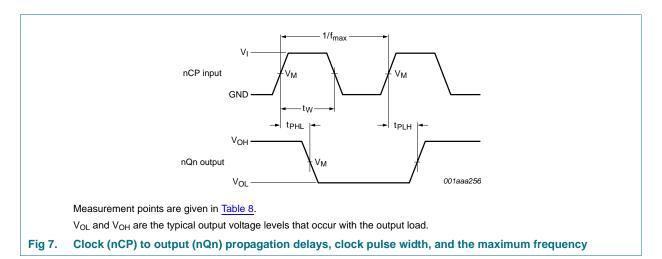
74LVC\_LVCH16374A

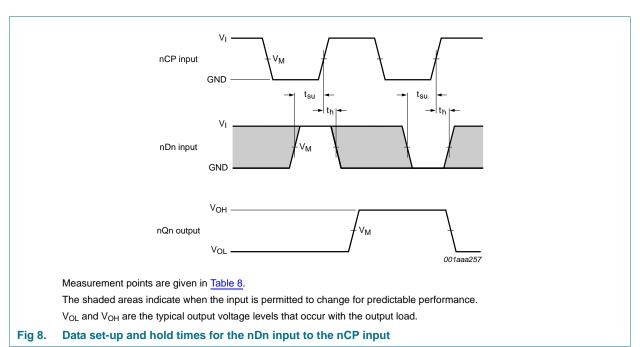
Downloaded from Elcodis.com electronic components distributor

<sup>[2]</sup>  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

<sup>[3]</sup> Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

### 11. Waveforms





74LVC\_LVCH16374A

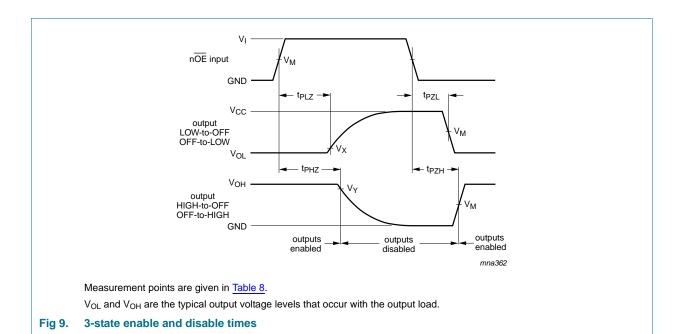
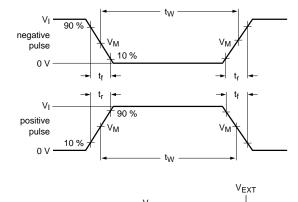
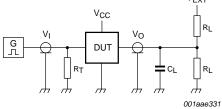


Table 8. Measurement points

Supply voltage	Input		Output				
V <sub>CC</sub>	VI	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>		
1.2 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V <sub>OL</sub> + 0.15 V	$V_{OH} - 0.15 V$		
1.65 V to 1.95 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> – 0.15 V		
2.3 V to 2.7 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V <sub>OL</sub> + 0.15 V	$V_{OH} - 0.15 V$		
2.7 V	2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	$V_{OH} - 0.3 V$		
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$		

12 of 20





Test data is given in Table 9.

Definitions for test circuit:

R<sub>L</sub> = Load resistance.

 $C_L$  = Load capacitance including jig and probe capacitance.

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

 $V_{\text{EXT}}$  = External voltage for measuring switching times.

Fig 10. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load	Load		V <sub>EXT</sub>		
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	CL	R <sub>L</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>	
1.2 V	$V_{CC}$	≤ 2 ns	30 pF	1 kΩ	open	$2\times V_{CC}$	GND	
1.65 V to 1.95 V	$V_{CC}$	≤ 2 ns	30 pF	1 kΩ	open	$2\times V_{CC}$	GND	
2.3 V to 2.7 V	V <sub>CC</sub>	≤ 2 ns	30 pF	$500 \Omega$	open	$2\times V_{CC}$	GND	
2.7 V	2.7 V	≤ 2.5 ns	50 pF	$500 \Omega$	open	$2\times V_{CC}$	GND	
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	$500 \Omega$	open	$2\times V_{CC}$	GND	

**Product data sheet** 

# 12. Package outline

#### SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

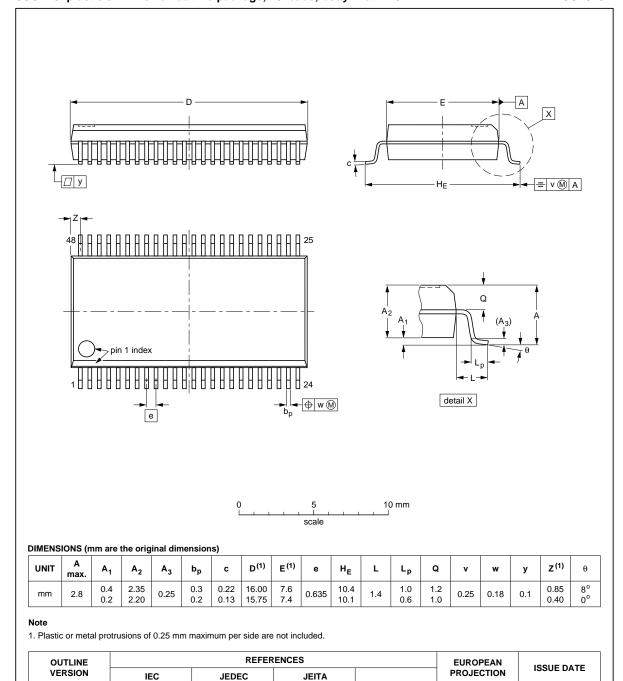


Fig 11. Package outline SOT370-1 (SSOP48)

74LVC\_LVCH16374A All information provided in this document is subject to legal disclaimers. © NXP B.V. 2013. All rights reserved.

MO-118

Product data sheet

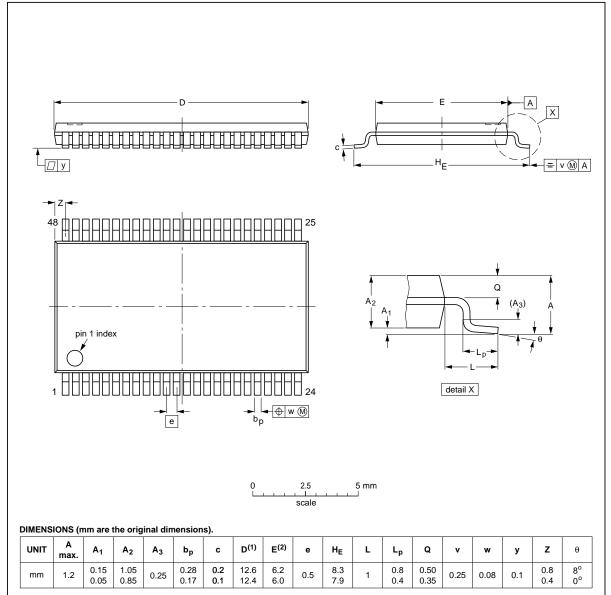
SOT370-1

99-12-27

03-02-19

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE	REFERENCES				EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT362-1		MO-153				<del>-99-12-27</del> 03-02-19

Fig 12. Package outline SOT362-1 (TSSOP48)

74LVC\_LVCH16374A All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Product data sheet

Rev. 11 — 16 January 2013

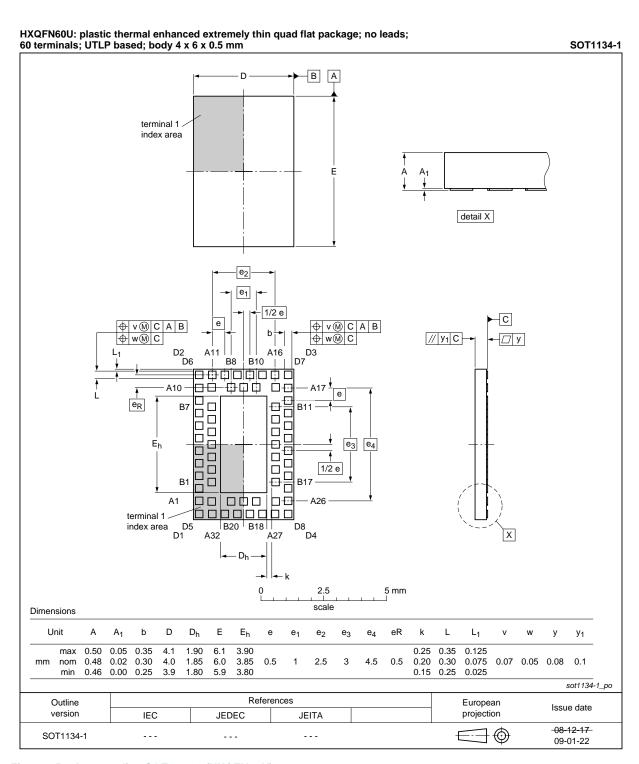


Fig 13. Package outline SOT1134-1 (HXQFN60U)

74LVC\_LVCH16374A All information provided in this document is subject to legal disclaimers. © NXP B.V. 2013. All rights reserved. Rev. 11 — 16 January 2013

**Product data sheet** 

### 13. Abbreviations

#### Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

# 14. Revision history

### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH16374A v.11	20130116	Product data sheet	-	74LVC_LVCH16374A v.10
Modifications:	Minor non-f	technical text changes an	d corrections	
	<ul> <li>Document</li> </ul>	revision history correction		
74LVC_LVCH16374A v.10	20120301	Product data sheet	-	74LVC_LVCH16374A v.9
74LVC_LVCH16374A v.9	20111219	Product data sheet	-	74LVC_LVCH16374A v.8
74LVC_LVCH16374A v.8	20110621	Product data sheet	-	74LVC_LVCH16374A v.7
74LVC_LVCH16374A v.7	20100323	Product data sheet	-	74LVC_LVCH16374A v.6
74LVC_LVCH16374A v.6	20090212	Product data sheet	-	74LVC_LVCH16374A v.5
74LVC_LVCH16374A v.5	20031212	Product specification	-	74LVC_H16374A v.4
74LVC_H16374A v.4	19980317	Product specification	-	74LVC16374A_ 74LVCH16374A v.3
74LVC16374A_ 74LVCH16374A v.3	19980317	Product specification	-	74LVC16374A v.2
74LVC16374A v.2	19970822	Product specification	-	74LVC16374A v.1
74LVC16374A v.1	-	-	-	-

### 15. Legal information

#### 15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

#### 15.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

#### 15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <a href="http://www.nxp.com/profile/terms">http://www.nxp.com/profile/terms</a>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

74LVC\_LVCH16374A

All information provided in this document is subject to legal disclaimers.

16-bit edge-triggered D-type flip-flop; 5 V tolerant; 3-state

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

#### 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

#### 16. Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

74LVC\_LVCH16374A

Product data sheet

All information provided in this document is subject to legal disclaimers.

### **NXP Semiconductors**

# 74LVC16374A; 74LVCH16374A

16-bit edge-triggered D-type flip-flop; 5 V tolerant; 3-state

### 17. Contents

1	General description
2	Features and benefits
3	Ordering information
4	Functional diagram 2
5	Pinning information 4
5.1	Pinning
5.2	Pin description 6
6	Functional description 6
7	Limiting values 6
8	Recommended operating conditions 7
9	Static characteristics 7
10	Dynamic characteristics
11	Waveforms
12	Package outline
13	Abbreviations
14	Revision history 17
15	Legal information
15.1	Data sheet status
15.2	Definitions
15.3	Disclaimers
15.4	Trademarks19
16	Contact information
17	Contents 20

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2013.

All rights reserved.

For more information, please visit: http://www.nxp.com For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 16 January 2013
Document identifier: 74LVC\_LVCH16374A