74HC00-Q100; 74HCT00-Q100

Quad 2-input NAND gate

Rev. 1 — 12 July 2012 | Product data sheet

1. General description

The 74HC00-Q100; 74HCT00-Q100 are high-speed Si-gate CMOS devices that comply with JEDEC standard no. 7A. They are pin compatible with Low-power Schottky TTL (LSTTL).

The 74HC00-Q100; 74HCT00-Q100 provides a quad 2-input NAND function.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from −40 °C to +85 °C and from −40 °C to +125 °C
- Input levels:
  - For 74HC00-Q100: CMOS level
  - For 74HCT00-Q100: TTL level
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pf, R = 0 Ω)
- Multiple package options

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC00D-Q100	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT00D-Q100				
74HC00PW-Q100	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCT00PW-Q100				
74HC00BQ-Q100	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74HCT00BQ-Q100				

4. Functional diagram

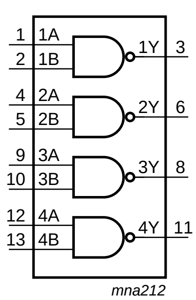


Fig 1. Logic symbol

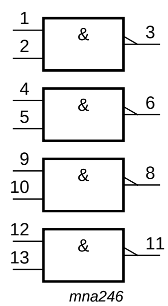


Fig 2. IEC logic symbol

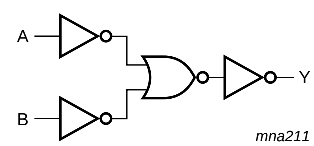


Fig 3. Logic diagram (one gate)

5. Pinning information

5.1 Pinning

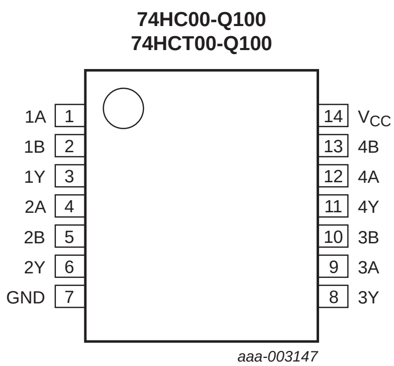
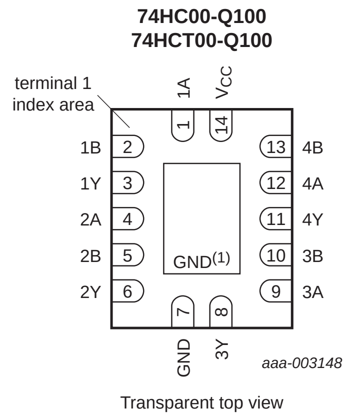


Fig 4. Pin configuration SO14 and TSSOP14



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 5. Pin configuration DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 4A	1, 4, 9, 12	data input
1B to 4B	2, 5, 10, 13	data input
1Y to 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input		Output
nA	nB	nY
L	X	H
X	L	H
H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$-0.5\ V < V_O < V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			–50	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation		[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For TSSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC00-Q100			74HCT00-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0$ V	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5$ V	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0$ V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC00-Q100										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	-	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	-	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	-	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	-	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	-	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	-	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = –20 μA; V_{CC} = 2.0 V	-	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	-	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	-	6.0	-	5.9	-	5.9	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	-	4.32	-	3.84	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	-	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	-	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	-	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	-	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	-	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	-	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	-	-	±1	-	±1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	-	-	20	-	40	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

Table 6. Static characteristics *...continued*
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT00-Q100										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = –20 µA	-	4.5	-	4.4	-	4.4	-	V
		I_O = –4.0 mA	-	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	-	-	0.1	-	0.1	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.15	-	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	-	-	±1	-	±1	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	-	-	20	-	40	µA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ – 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V	-	150	-	-	675	-	735	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics
GND = 0 V; C_L = 50 pF; for load circuit see Figure 7.

Symbol	Parameter	Conditions		25 °C			–40 °C to +125 °C		Unit
				Min	Typ	Max	Max (85 °C)	Max (125 °C)	
74HC00-Q100									
t_{pd}	propagation delay	nA, nB to nY; see Figure 6	[1]						
		V_{CC} = 2.0 V		-	25	-	115	135	ns
		V_{CC} = 4.5 V		-	9	-	23	27	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	7	-	-	-	ns
		V_{CC} = 6.0 V		-	7	-	20	23	ns
t_t	transition time	see Figure 6	[2]						
		V_{CC} = 2.0 V		-	19	-	95	110	ns
		V_{CC} = 4.5 V		-	7	-	19	22	ns
		V_{CC} = 6.0 V		-	6	-	16	19	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC}	[3]	-	22	-	-	-	pF

Table 7. Dynamic characteristics *...continued*

GND = 0 V; C_L = 50 pF; for load circuit see Figure 7.

Symbol	Parameter	Conditions		25 °C			−40 °C to +125 °C		Unit
				Min	Typ	Max	Max (85 °C)	Max (125 °C)	
74HCT00-Q100									
t_{pd}	propagation delay	nA, nB to nY; see Figure 6	[1]						
		V_{CC} = 4.5 V		-	12	-	24	29	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	10	-	-	-	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 6	[2]	-	-	-	29	22	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} − 1.5 V	[3]	-	22	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

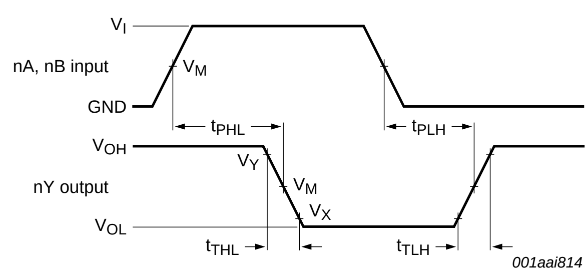
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



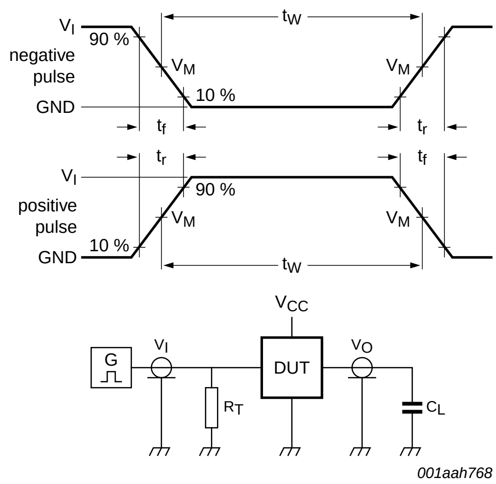
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Input to output propagation delays

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC00-Q100	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT00-Q100	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$



Test data is given in Table 9.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

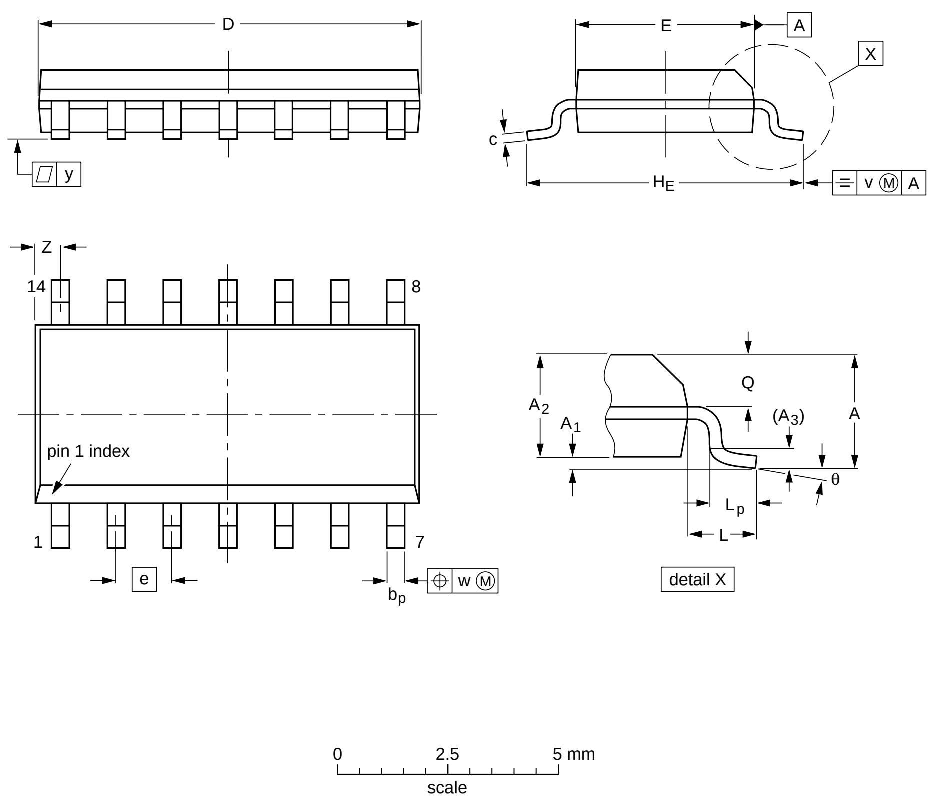
Fig 7. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC00-Q100	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT00-Q100	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

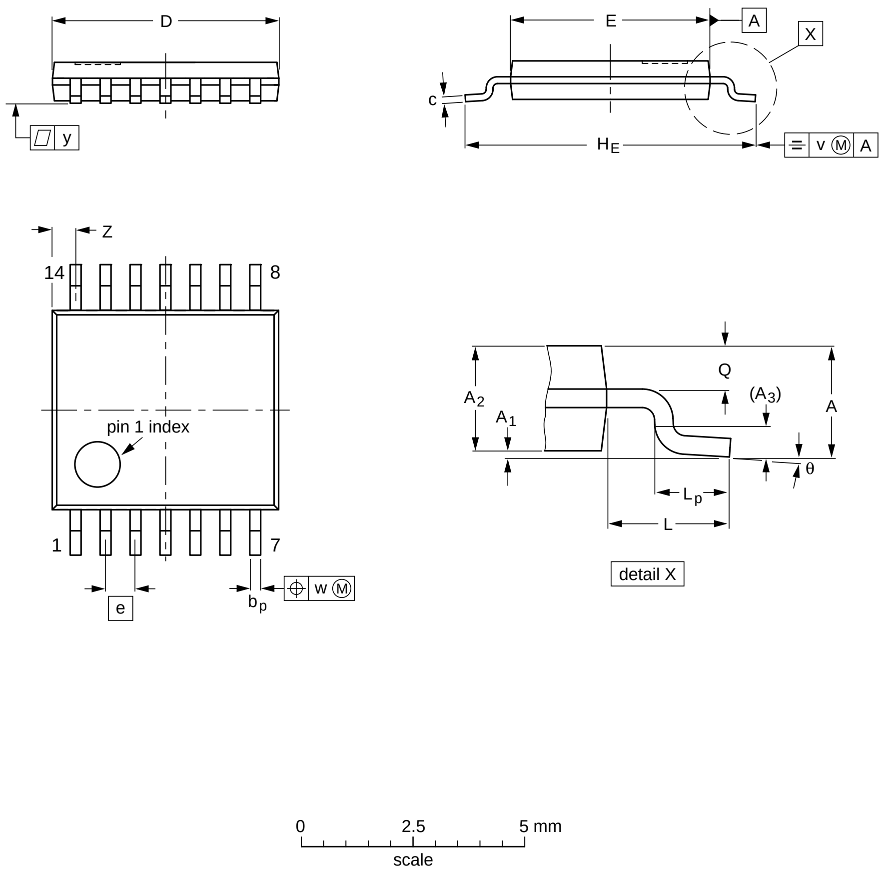
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D [(1)]	E [(2)]	e	H_E	L	L_p	Q	v	w	y	Z [(1)]	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

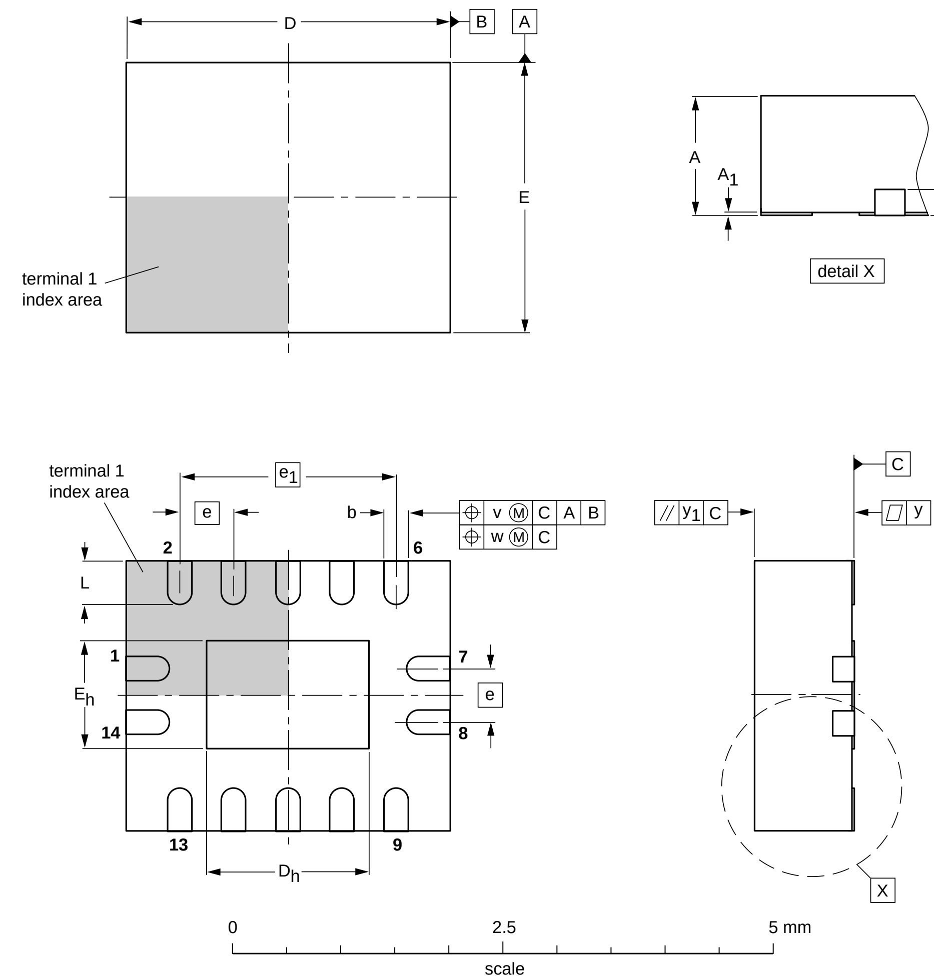
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 10. Package outline SOT762-1 (DHVQFN14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
TTL	Transistor-Transistor Logic
MIL	Military

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT00_Q100 v.1	20120712	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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16. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

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