

# 74AC299, 74ACT299

## 8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

### Features

- $I_{CC}$  and  $I_{OZ}$  reduced by 50%
- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- 3-STATE outputs for bus-oriented applications
- Outputs source/sink 24mA
- ACT299 has TTL-compatible inputs


### General Description

The AC/ACT299 is an 8-bit universal shift/storage register with 3-STATE outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops  $Q_0$ ,  $Q_7$  to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

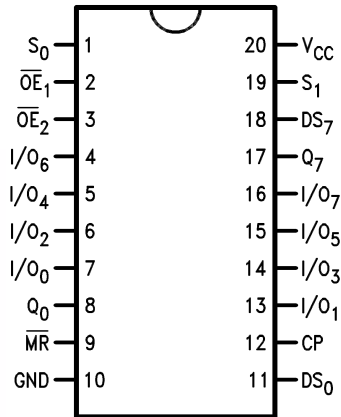
### Ordering Information

Order Number	Package Number	Package Description
74AC299SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74AC299SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC299MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC299PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT299SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT299MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT299PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

### Connection Diagram



### Pin Description

Pin Names	Description
CP	Clock Pulse Input
DS <sub>0</sub>	Serial Data Input for Right Shift
DS <sub>7</sub>	Serial Data Input for Left Shift
S <sub>0</sub> , S <sub>1</sub>	Mode Select Inputs
MR	Asynchronous Master Reset
OE <sub>1</sub> , OE <sub>2</sub>	3-STATE Output Enable Inputs
I/O <sub>0</sub> –I/O <sub>7</sub>	Parallel Data Inputs or 3-STATE Parallel Outputs
Q <sub>0</sub> , Q <sub>7</sub>	Serial Outputs

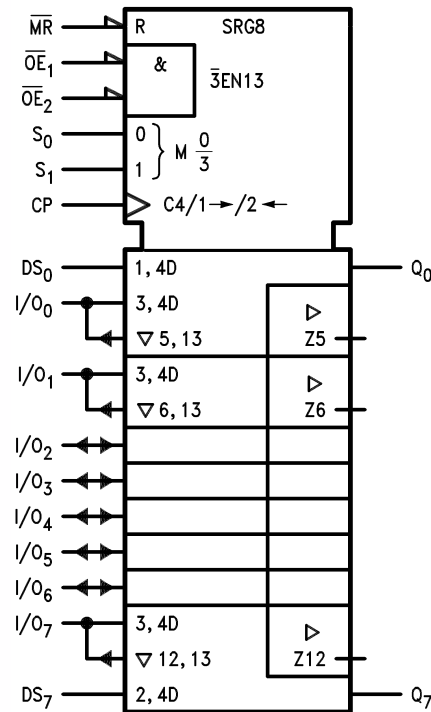
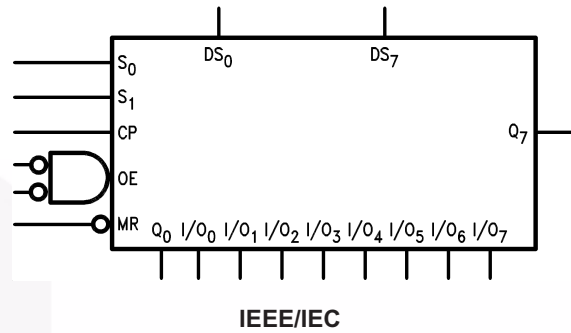
### Functional Description

The AC/ACT299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S<sub>0</sub> and S<sub>1</sub>, as shown in the Truth Table. All flip-flop outputs are brought out through 3-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q<sub>0</sub> and Q<sub>7</sub> are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on MR overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either OE<sub>1</sub> or OE<sub>2</sub> disables the 3-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-STATE buffers are also disabled by HIGH signals on both S<sub>0</sub> and S<sub>1</sub> in preparation for a parallel load operation.

### Logic Symbols



### Truth Table

Inputs				Response
MR	S <sub>1</sub>	S <sub>0</sub>	CP	
L	X	X	X	Asynchronous Reset; Q <sub>0</sub> –Q <sub>7</sub> = LOW
H	H	H	↗	Parallel Load; I/O <sub>n</sub> → Q <sub>n</sub>
H	L	H	↗	Shift Right; DS <sub>0</sub> → Q <sub>0</sub> , Q <sub>0</sub> → Q <sub>1</sub> , etc.
H	H	L	↗	Shift Left, DS <sub>7</sub> → Q <sub>7</sub> , Q <sub>7</sub> → Q <sub>6</sub> , etc.
H	L	L	X	Hold

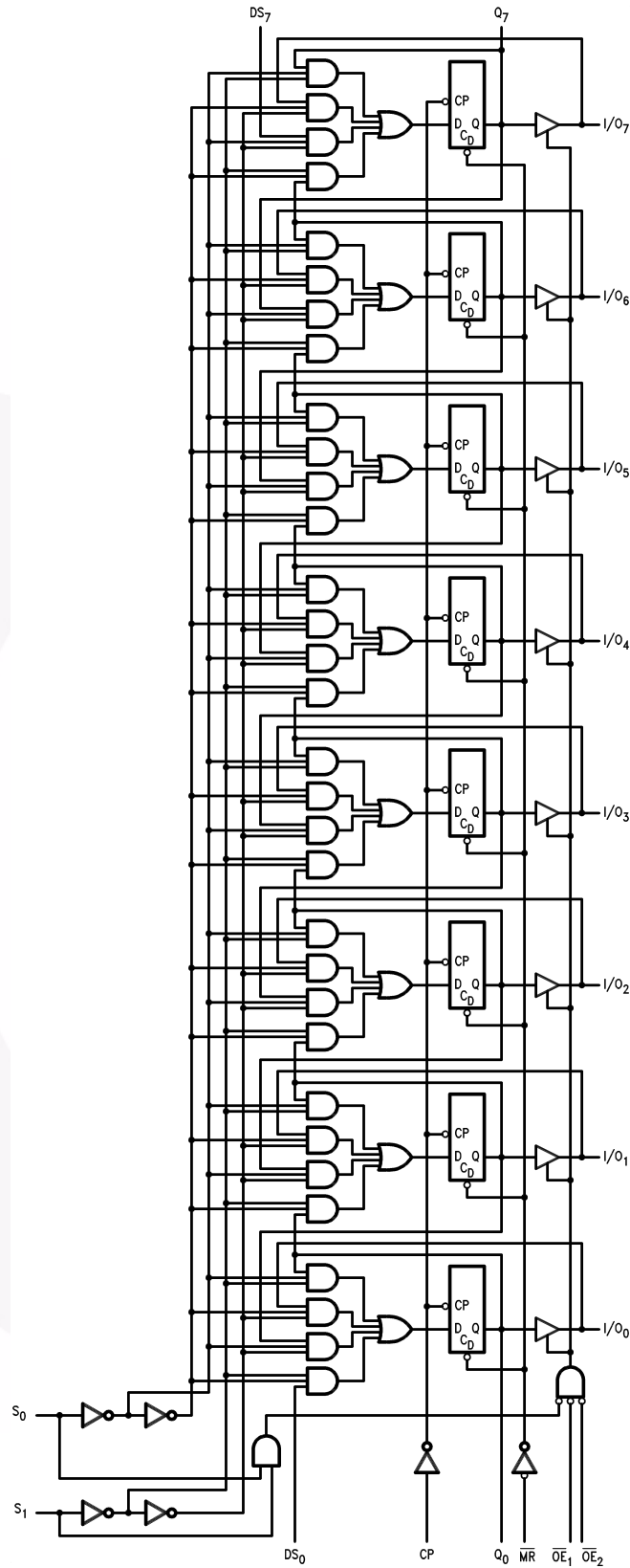
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

↗ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7.0V
$I_{IK}$	DC Input Diode Current $V_I = -0.5V$	-20mA
	$V_I = V_{CC} + 0.5$	+20mA
$V_I$	DC Input Voltage	-0.5V to $V_{CC} + 0.5V$
$I_{OK}$	DC Output Diode Current $V_O = -0.5V$	-20mA
	$V_O = V_{CC} + 0.5V$	+20mA
$V_O$	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
$I_O$	DC Output Source or Sink Current	$\pm 50mA$
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current per Output Pin	$\pm 50mA$
$T_{STG}$	Storage Temperature	-65°C to +150°C
$T_J$	Junction Temperature	140°C

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage (unless otherwise specified) AC	2.0V to 6.0V
	ACT	4.5V to 5.5V
$V_I$	Input Voltage	0V to $V_{CC}$
$V_O$	Output Voltage	0V to $V_{CC}$
$T_A$	Operating Temperature	-40°C to +85°C
$\Delta V / \Delta t$	Minimum Input Edge Rate, AC Devices: $V_{IN}$ from 30% to 70% of $V_{CC}$ , $V_{CC}$ @ 3.3V, 4.5V, 5.5V	125mV/ns
$\Delta V / \Delta t$	Minimum Input Edge Rate, ACT Devices: $V_{IN}$ from 0.8V to 2.0V, $V_{CC}$ @ 4.5V, 5.5V	125mV/ns

## DC Electrical Characteristics for AC

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units	
				Typ.	Guaranteed Limits				
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	2.1	2.1		V	
		4.5		2.25	3.15	3.15			
		5.5		2.75	3.85	3.85			
V <sub>IL</sub>	Maximum LOW Level Input Voltage	3.0	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	0.9	0.9		V	
		4.5		2.25	1.35	1.35			
		5.5		2.75	1.65	1.65			
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	3.0	I <sub>OUT</sub> = -50μA	2.99	2.9	2.9		V	
		4.5		4.49	4.4	4.4			
		5.5		5.49	5.4	5.4			
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -12mA		2.56	2.46			
		4.5		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA		3.86	3.76		
		5.5			V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA <sup>(1)</sup>		4.86		4.76
V <sub>OL</sub>	Maximum LOW Level Output Voltage	3.0	I <sub>OUT</sub> = 50μA	0.002		0.1	0.1		V
		4.5		0.001	0.1	0.1			
		5.5		0.001	0.1	0.1			
		3.0	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 12mA		0.36	0.44			
		4.5		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA		0.36	0.44		
		5.5			V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA <sup>(1)</sup>		0.36	0.44	
I <sub>IN</sub> <sup>(2)</sup>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND			±0.1	±1.0		μA
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(3)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max.			75		mA	
I <sub>OHD</sub>		5.5	V <sub>OHD</sub> = 3.85V Min.			-75		mA	
I <sub>CC</sub> <sup>(2)</sup>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		4.0	40.0		μA	
I <sub>OZT</sub>	Maximum I/O Leakage Current	5.5	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> ; V <sub>I</sub> = V <sub>CC</sub> , GND; V <sub>O</sub> = V <sub>CC</sub> , GND		±0.3	±3.0		μA	

## Notes:

- All outputs loaded; thresholds on input associated with output under test.
- I<sub>IN</sub> and I<sub>CC</sub> @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V<sub>CC</sub>.
- Maximum test duration 2.0ms, one output loaded at a time.

## DC Electrical Characteristics for ACT

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = +25°C		T <sub>A</sub> = -40°C to +85°C		Units
				Typ.	Guaranteed Limits			
V <sub>IH</sub>	Minimum HIGH Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	2.0	2.0		V
		5.5		1.5	2.0	2.0		
V <sub>IL</sub>	Maximum LOW Level Input Voltage	4.5	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1V	1.5	0.8	0.8		V
		5.5		1.5	0.8	0.8		
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	4.5	I <sub>OUT</sub> = -50μA	4.49	4.4	4.4		V
		5.5		5.49	5.4	5.4		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA	0.0001	3.86	3.76		
		5.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OH</sub> = -24mA <sup>(4)</sup>		4.86	4.76		
V <sub>OL</sub>	Maximum LOW Level Output Voltage	4.5	I <sub>OUT</sub> = 50μA	0.001	0.1	0.1		V
		5.5		0.001	0.1	0.1		
		4.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA		0.36	0.44		
		5.5	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> , I <sub>OL</sub> = 24mA <sup>(4)</sup>		0.36	0.44		
I <sub>IN</sub>	Maximum Input Leakage Current	5.5	V <sub>I</sub> = V <sub>CC</sub> , GND		±0.1	±1.0		μA
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input	5.5	V <sub>I</sub> = V <sub>CC</sub> - 2.1V	0.6		1.5		mA
I <sub>OLD</sub>	Minimum Dynamic Output Current <sup>(5)</sup>	5.5	V <sub>OLD</sub> = 1.65V Max.			75		mA
		5.5	V <sub>OHD</sub> = 3.85V Min.			-75		mA
I <sub>CC</sub>	Maximum Quiescent Supply Current	5.5	V <sub>IN</sub> = V <sub>CC</sub> or GND		4.0	40.0		μA
I <sub>OZT</sub>	Maximum I/O Leakage Current	5.5	V <sub>I</sub> (OE) = V <sub>IL</sub> , V <sub>IH</sub> ; V <sub>I</sub> = V <sub>CC</sub> , GND; V <sub>O</sub> = V <sub>CC</sub> , GND		±0.3	±3.0		μA

**Notes:**

- All outputs loaded; thresholds on input associated with output under test.
- Maximum test duration 2.0ms, one output loaded at a time.

## AC Electrical Characteristics for AC

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(6)</sup>	T <sub>A</sub> = +25°C, C <sub>L</sub> = 50pF			T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50pF		Units
			Min.	Typ.	Max.	Min.	Max.	
f <sub>MAX</sub>	Maximum Input Frequency	3.3	90	124		80		MHz
		5.0	130	173		105		
t <sub>PLH</sub>	Propagation Delay, CP to Q <sub>0</sub> or Q <sub>7</sub> (Shift Left or Right)	3.3	8.5	14.0	20.5	7.0	22.0	ns
		5.0	5.5	9.5	14.0	4.5	15.0	
t <sub>PHL</sub>	Propagation Delay, CP to Q <sub>0</sub> or Q <sub>7</sub> (Shift Left or Right)	3.3	8.5	14.5	21.5	7.0	23.0	ns
		5.0	5.5	10.0	14.5	5.0	16.0	
t <sub>PLH</sub>	Propagation Delay, $\overline{CP}$ to I/O <sub>n</sub>	3.3	9.0	14.5	20.5	7.5	22.5	ns
		5.0	6.0	10.0	14.5	5.0	16.0	
t <sub>PHL</sub>	Propagation Delay, $\overline{CP}$ to I/O <sub>n</sub>	3.3	10.0	16.0	23.0	8.5	24.5	ns
		5.0	6.5	11.0	16.0	6.0	17.5	
t <sub>PHL</sub>	Propagation Delay, $\overline{MR}$ to Q <sub>0</sub> or Q <sub>7</sub>	3.3	9.0	15.5	22.5	7.5	25.0	ns
		5.0	5.5	10.5	15.5	5.0	17.0	
t <sub>PHL</sub>	Propagation Delay, $\overline{MR}$ to I/O <sub>n</sub>	3.3	9.0	15.0	21.5	7.5	24.0	ns
		5.0	5.5	10.0	15.0	5.0	16.5	
t <sub>PZH</sub>	Output Enable Time, $\overline{OE}$ to I/O <sub>n</sub>	3.3	7.0	12.0	18.0	6.0	19.5	ns
		5.0	4.5	8.5	12.5	4.0	13.5	
t <sub>PZL</sub>	Output Enable Time, $\overline{OE}$ to I/O <sub>n</sub>	3.3	7.0	12.5	18.0	6.0	20.5	ns
		5.0	5.0	8.0	12.5	4.0	14.0	
t <sub>PHZ</sub>	Output Disable Time, $\overline{OE}$ to I/O <sub>n</sub>	3.3	6.5	13.0	18.5	5.5	19.5	ns
		5.0	3.5	9.5	14.0	3.0	15.0	
t <sub>PLZ</sub>	Output Disable Time, $\overline{OE}$ to I/O <sub>n</sub>	3.3	5.5	11.5	17.0	4.5	19.0	ns
		5.0	3.5	8.0	12.5	2.0	13.5	

**Note:**

6. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.

## AC Operating Requirements for AC

Symbol	Parameter	V <sub>CC</sub> (V) <sup>(7)</sup>	T <sub>A</sub> = +25°C, C <sub>L</sub> = 50pF		T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50pF		Units
			Typ.	Guaranteed Minimum			
t <sub>S</sub>	Setup Time, HIGH or LOW, S <sub>0</sub> or S <sub>1</sub> to CP	3.3	3.0	8.0	8.5	ns	
		5.0	2.0	5.0	5.5		
t <sub>H</sub>	Hold Time, HIGH or LOW, S <sub>0</sub> or S <sub>1</sub> to CP	3.3	-3.0	0.5	0.5	ns	
		5.0	-1.5	1.0	1.0		
t <sub>S</sub>	Setup Time, HIGH or LOW, I/O <sub>n</sub> to CP	3.3	2.0	5.5	6.0	ns	
		5.0	1.0	3.5	4.0		
t <sub>H</sub>	Hold Time, HIGH or LOW, I/O <sub>n</sub> to CP	3.3	-2.0	0	0	ns	
		5.0	-1.0	1.0	1.0		
t <sub>S</sub>	Setup Time, HIGH or LOW, DS <sub>0</sub> or DS <sub>7</sub> to CP	3.3	2.5	6.5	7.0	ns	
		5.0	1.5	4.0	4.5		
t <sub>H</sub>	Hold Time, HIGH or LOW, DS <sub>0</sub> or DS <sub>7</sub> to CP	3.3	-2.0	0	0.5	ns	
		5.0	-1.0	1.0	1.0		
t <sub>W</sub>	CP Pulse Width, LOW	3.3	3.5	4.5	5.0	ns	
		5.0	2.0	3.5	3.5		
t <sub>W</sub>	$\overline{\text{MR}}$ Pulse Width, LOW	3.3	4.0	4.5	5.0	ns	
		5.0	2.0	3.5	3.5		
t <sub>REC</sub>	Recovery Time, $\overline{\text{MR}}$ to CP	3.3	0	1.5	1.5	ns	
		5.0	0.5	1.5	1.5		

**Note:**

7. Voltage range 3.3 is 3.3V ± 0.3V. Voltage range 5.0 is 5.0V ± 0.5V.



## AC Electrical Characteristics for ACT

Symbol	Parameter	$V_{CC}$ (V) <sup>(8)</sup>	$T_A = +25^\circ\text{C}$ , $C_L = 50\text{pF}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , $C_L = 50\text{pF}$		Units
			Min.	Typ.	Max.	Min.	Max.	
$f_{MAX}$	Maximum Input Frequency	5.0	120	170		110		MHz
$t_{PLH}$	Propagation Delay, CP to $Q_0$ or $Q_7$ (Shift Left or Right)	5.0	4.0	8.5	12.5	3.0	14.0	ns
$t_{PHL}$	Propagation Delay, CP to $Q_0$ or $Q_7$ (Shift Left or Right)	5.0	4.0	9.0	13.5	3.5	15.0	ns
$t_{PLH}$	Propagation Delay, CP to $I/O_n$	5.0	4.5	8.5	12.5	4.5	13.5	ns
$t_{PHL}$	Propagation Delay, CP to $I/O_n$	5.0	5.0	9.5	15.0	4.5	16.5	ns
$t_{PHL}$	Propagation Delay, $\overline{MR}$ to $Q_0$ or $Q_7$	5.0	4.0	14.0	15.0	4.0	18.0	ns
$t_{PHL}$	Propagation Delay, $\overline{MR}$ to $I/O_n$	5.0	4.0	13.0	14.5	3.5	17.5	ns
$t_{PZH}$	Output Enable Time, $\overline{OE}$ to $I/O_n$	5.0	2.5	8.0	12.0	1.5	13.0	ns
$t_{PZL}$	Output Enable Time, $\overline{OE}$ to $I/O_n$	5.0	2.0	8.0	12.0	1.5	13.5	ns
$t_{PHZ}$	Output Disable Time, $\overline{OE}$ to $I/O_n$	5.0	2.0	8.5	12.5	2.0	13.5	ns
$t_{PLZ}$	Output Disable Time, $\overline{OE}$ to $I/O_n$	5.0	2.5	8.0	11.5	2.0	12.5	ns

## Note

8. Voltage range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ .

## AC Operating Requirements for ACT

Symbol	Parameter	$V_{CC}$ (V) <sup>(9)</sup>	$T_A = +25^\circ\text{C}$ , $C_L = 50\text{pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ , $C_L = 50\text{pF}$		Units
			Typ.	Guaranteed Minimum			
$t_S$	Setup Time, HIGH or LOW, $S_0$ or $S_1$ to CP	5.0	2.0	5.0	5.5		ns
$t_H$	Hold Time, HIGH or LOW, $S_0$ or $S_1$ to CP	5.0	-2.0	1.0	1.0		ns
$t_S$	Setup Time, HIGH or LOW, $I/O_n$ to CP	5.0	1.5	4.0	4.5		ns
$t_H$	Hold Time, HIGH or LOW, $I/O_n$ to CP	5.0	-1.0	1.0	1.0		ns
$t_S$	Setup Time, HIGH or LOW, $DS_0$ or $DS_7$ to CP	5.0	1.5	4.5	5.0		ns
$t_H$	Hold Time, HIGH or LOW, $DS_0$ or $DS_7$ to CP	5.0	-1.0	1.0	1.0		ns
$t_W$	CP Pulse Width, HIGH or LOW	5.0	2.0	4.0	4.5		ns
$t_W$	$\overline{MR}$ Pulse Width, LOW	5.0	2.0	3.5	3.5		ns
$t_{REC}$	Recovery Time, $\overline{MR}$ to CP	5.0	0	1.5	1.5		ns

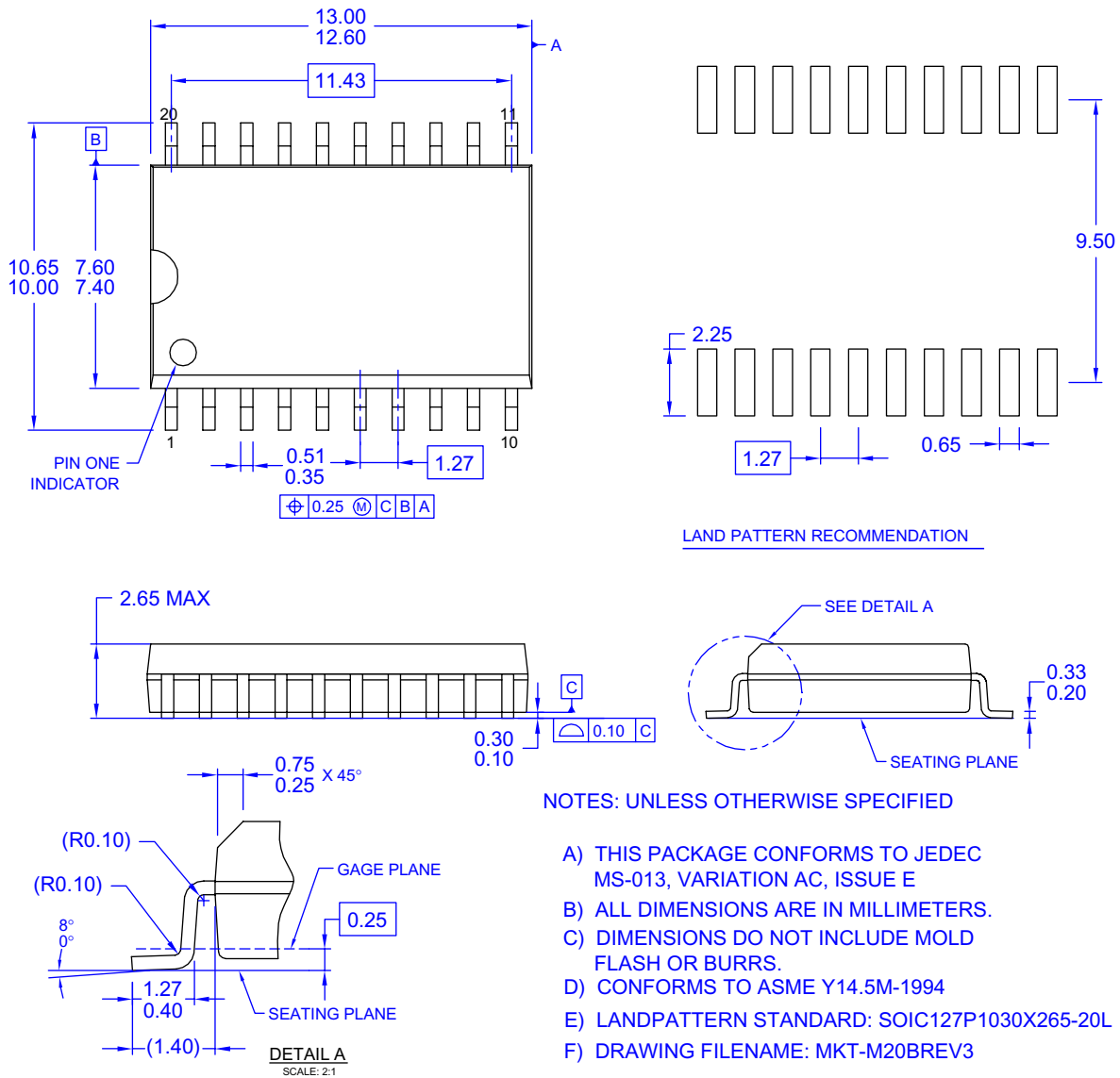
## Note

9. Voltage range 5.0 is  $5.0\text{V} \pm 0.5\text{V}$ .

## Capacitance

Symbol	Parameter	Conditions	Typ.	Units
$C_{IN}$	Input Capacitance	$V_{CC} = 5.0\text{V}$	4.5	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CC} = 5.5\text{V}$	170	pF

## Physical Dimensions



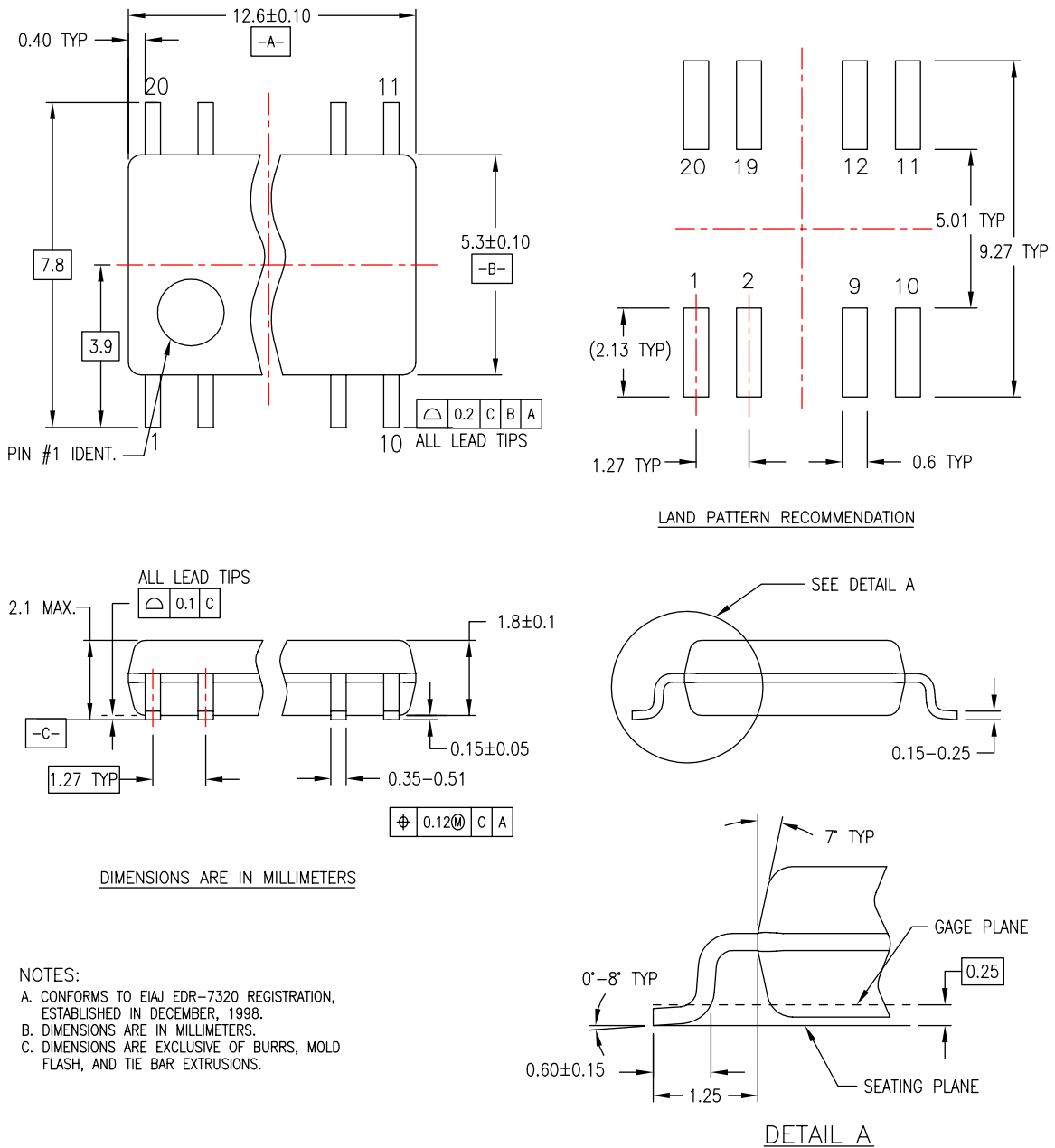
**Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide**

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Physical Dimensions (Continued)



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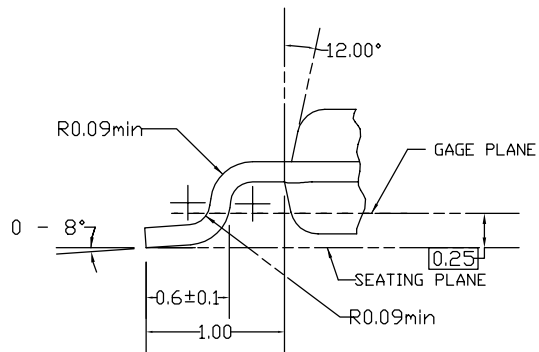
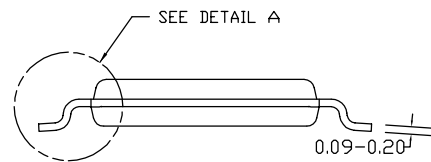
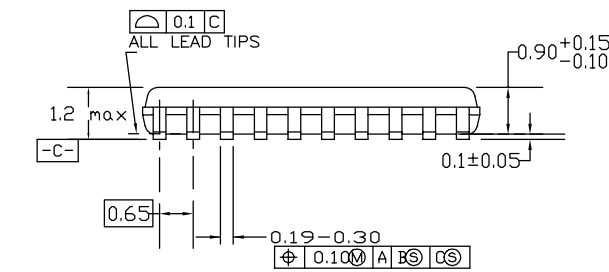
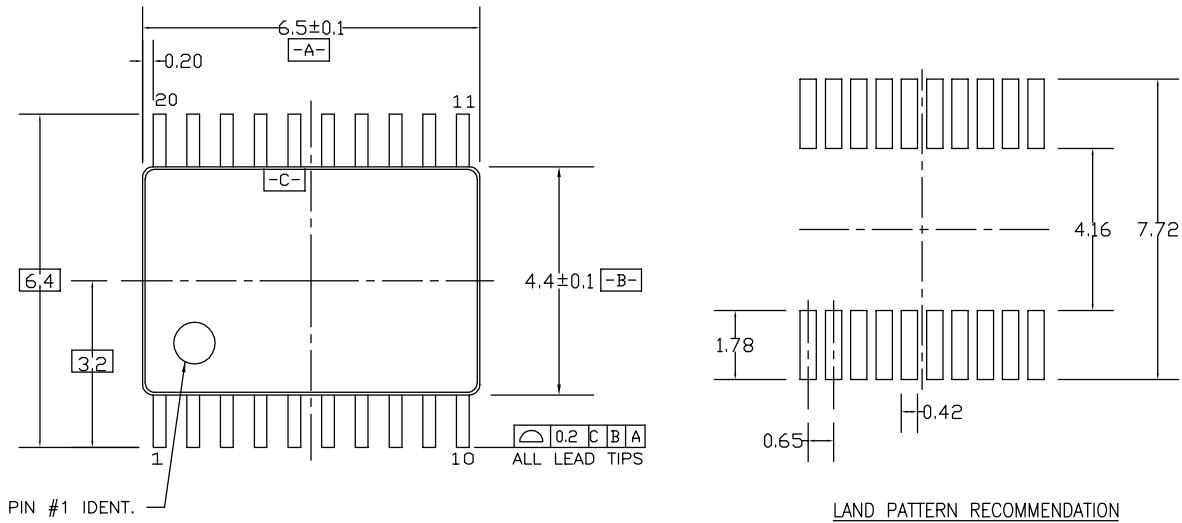
Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MD-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

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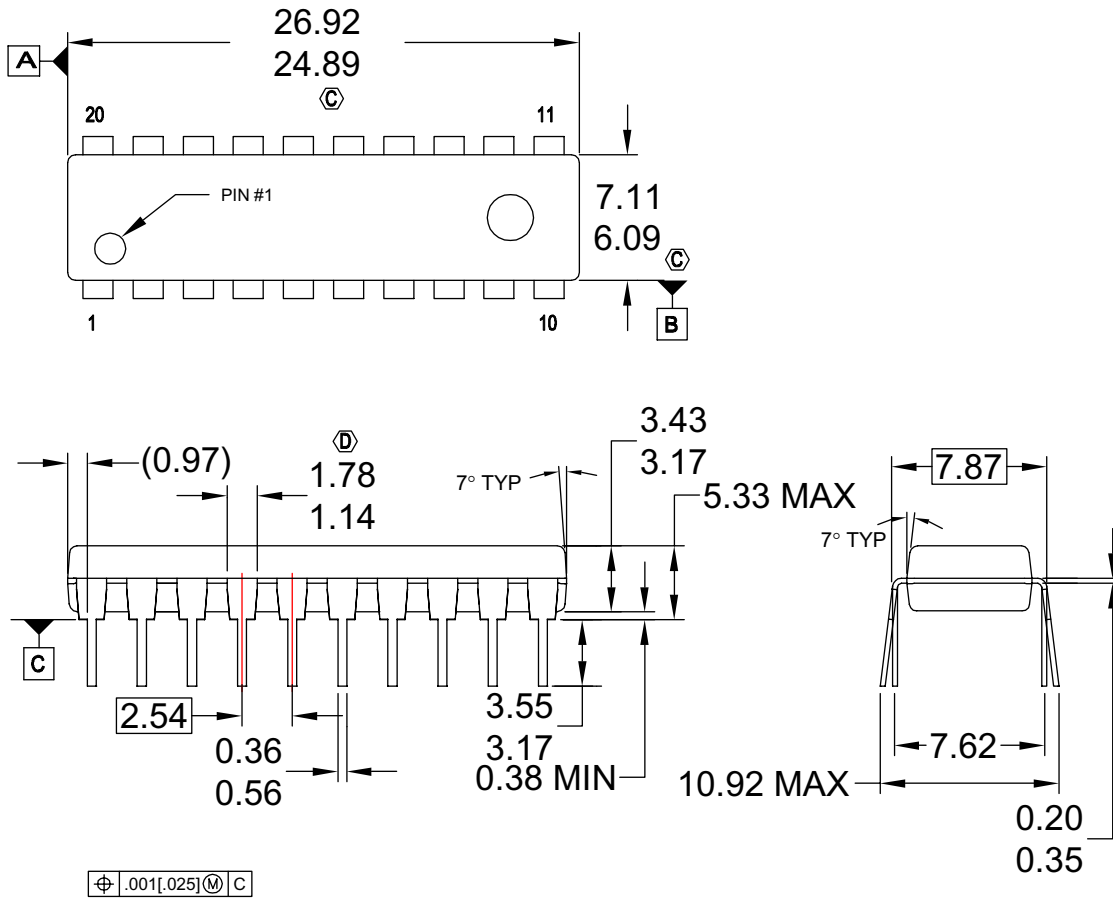
Figure 3. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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**Physical Dimensions** (Continued)



- NOTES:**
- A. CONFORMS TO JEDEC REGISTRATION MS-001, VARIATIONS AD.
  - B. ALL DIMENSIONS ARE IN MILLIMETERS
  - C. DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
  - D. DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSIONS SHALL NOT EXCEED 0.25MM.
  - E. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - F. DRAWING FILE NAME: N20AREV8

**Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**

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

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