74HC595-Q100; 74HCT595-Q100

8-bit serial-in, serial or parallel-out shift register with output latches; 3-state

Rev. 2 — 10 April 2013 Product data sheet

1. General description

The 74HC595-Q100; 74HCT595-Q100 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7A.

The 74HC595-Q100; 74HCT595-Q100 are 8-stage serial shift registers with a storage register and 3-state outputs. The registers have separate clocks. Data is shifted on the positive-going transitions of the shift register clock input (SHCP). The data in each register is transferred to the storage register on a positive-going transition of the storage register clock input (STCP). If both clocks are connected together, the shift register is always one clock pulse ahead of the storage register.

The shift register has a serial input (DS) and a serial standard output (Q7S) for cascading. It is also provided with asynchronous reset (active LOW) for all 8 shift register stages. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is LOW.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from −40 °C to +85 °C and from −40 °C to +125 °C
- 8-bit serial input
- 8-bit serial or parallel output
- Storage register with 3-state outputs
- Shift register with direct clear
- 100 MHz (typical) shift out frequency
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

3. Applications

- Serial-to-parallel data conversion
- Remote control holding register

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4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC595D-Q100	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT595D-Q100				
74HC595DB-Q100	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT595DB-Q100				
74HC595PW-Q100	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT595PW-Q100				
74HC595BQ-Q100	−40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT595BQ-Q100				

5. Functional diagram

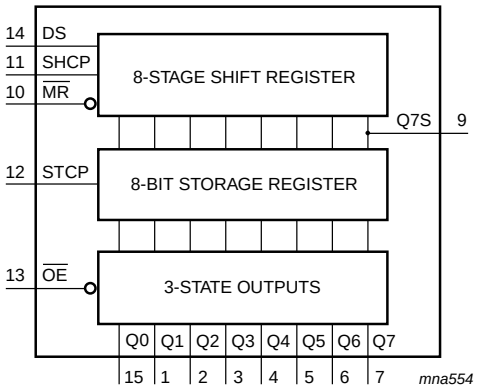

Fig 1. Functional diagram

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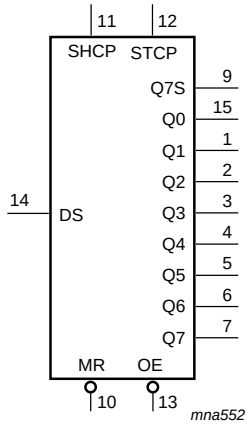

Fig 2. Logic symbol

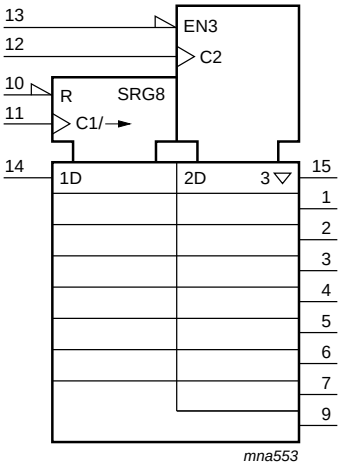

Fig 3. IEC logic symbol

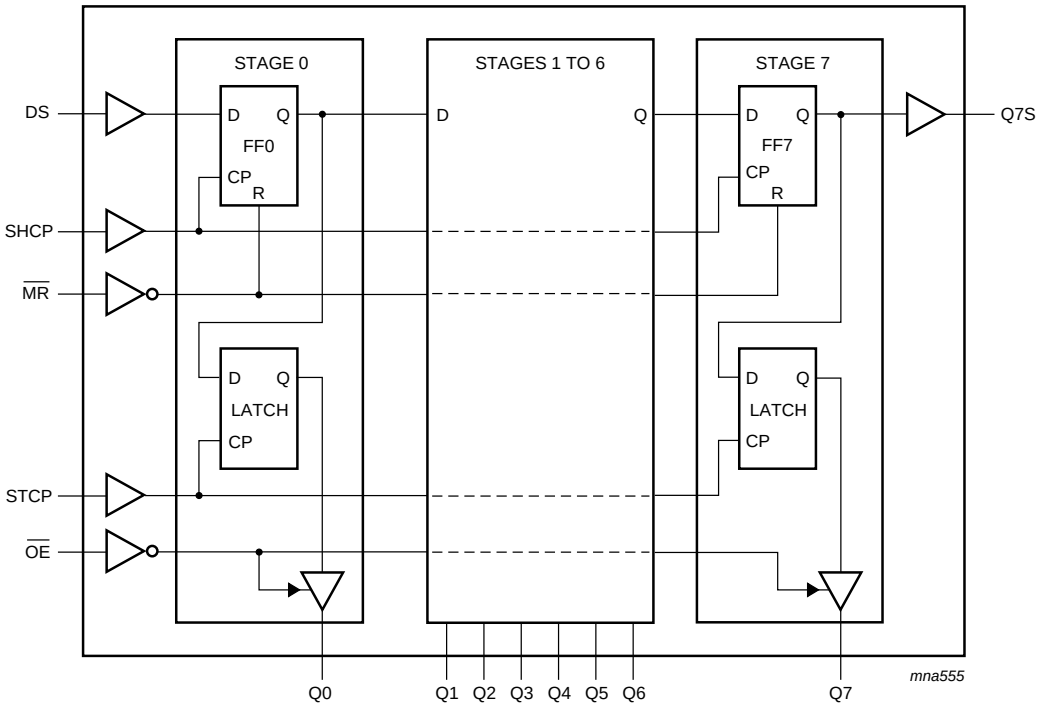

Fig 4. Logic diagram

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6. Pinning information

6.1 Pinning

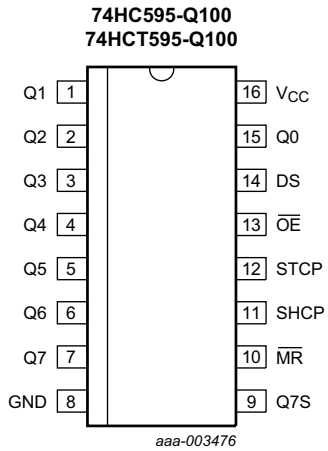


Fig 5. Pin configuration SO16

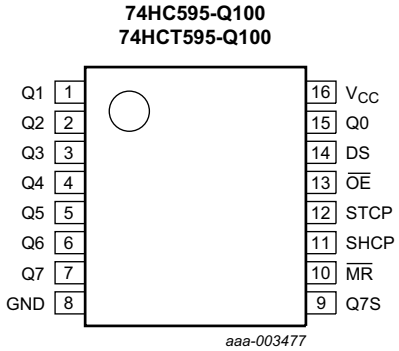
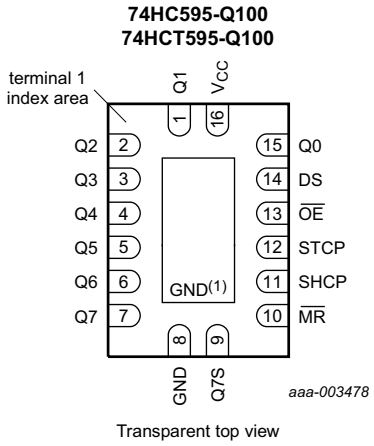


Fig 6. Pin configuration (T)SSOP16



(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig 7. Pin configuration for DHVQFN16

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6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	15, 1, 2, 3, 4, 5, 6, 7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
$\overline{MR}$	10	master reset (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
$\overline{OE}$	13	output enable input (active LOW)
DS	14	serial data input
V_{CC}	16	supply voltage

7. Functional description

Table 3. Function table[1]

Control				Input	Output		Function
SHCP	STCP	$\overline{OE}$	$\overline{MR}$	DS	Q7S	Qn	
X	X	L	L	X	L	NC	a LOW-level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Q6S	NC	logic HIGH-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

[1] H = HIGH voltage state;
L = LOW voltage state;
↑ = LOW-to-HIGH transition;
X = don't care;
NC = no change;
Z = high-impedance OFF-state.

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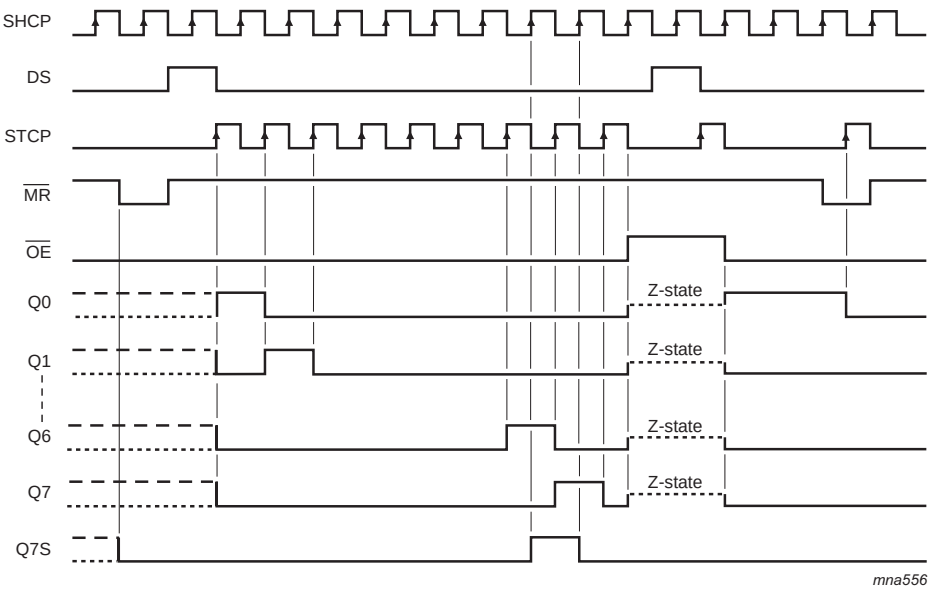

Fig 8. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V		-	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)				
		pin Q7S		-	±25	mA
		pins Qn		-	±35	mA
I_{CC}	supply current			-	70	mA
I_{GND}	ground current			−70	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation					
	SO16 package		[1]	-	500	mW
	(T)SSOP16 package		[2]	-	500	mW
	DHVQFN16 package		[3]	-	500	mW

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[2] For (T)SSOP16 package: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[3] For DHVQFN16 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

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9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC595-Q100			74HCT595-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC595-Q100								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		all outputs						
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		Q7S output						
		I_O = –4 mA; V_{CC} = 4.5 V	3.84	4.32	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.34	5.81	-	5.2	-	V
		Qn bus driver outputs						
		I_O = –6 mA; V_{CC} = 4.5 V	3.84	4.32	-	3.7	-	V
		I_O = –7.8 mA; V_{CC} = 6.0 V	5.34	5.81	-	5.2	-	V

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Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		all outputs						
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	V
		Q7S output						
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
		Qn bus driver outputs						
		I_O = 6 mA; V_{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 6.0 V; $V_O = V_{CC}$ or GND	-	-	±5.0	-	±10	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	pF

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Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HCT595-Q100								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		all outputs						
		I_O = −20 μA	4.4	4.5	-	4.4	-	V
		Q7S output						
		I_O = −4 mA	3.84	4.32	-	3.7	-	V
		Qn bus driver outputs						
		I_O = −6 mA	3.7	4.32	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V						
		all outputs						
		I_O = 20 μA	-	0	0.1	-	0.1	V
		Q7S output						
		I_O = 4.0 mA	-	0.15	0.33	-	0.4	V
		Qn bus driver outputs						
		I_O = 6.0 mA	-	0.16	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_{CC} = 5.5 V; V_O = V_{CC} or GND	-	-	±5.0	-	±10	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	80	-	160	μA
ΔI_{CC}	additional supply current	per input pin; I_O = 0 A; V_I = V_{CC} − 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V						
		pins $\overline{MR}$, SHCP, STCP, $\overline{OE}$	-	150	675	-	735	μA
		pin DS	-	25	113	-	123	μA
C_I	input capacitance		-	3.5	-	-	-	pF

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11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 14.

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
74HC595-Q100											
t_{pd}	propagation delay	SHCP to Q7S; see Figure 9	[2]								
		V_{CC} = 2 V		-	52	160	-	200	-	240	ns
		V_{CC} = 4.5 V		-	19	32	-	40	-	48	ns
		V_{CC} = 6 V		-	15	27	-	34	-	41	ns
		STCP to Qn; see Figure 10	[2]								
		V_{CC} = 2 V		-	55	175	-	220	-	265	ns
		V_{CC} = 4.5 V		-	20	35	-	44	-	53	ns
		V_{CC} = 6 V		-	16	30	-	37	-	45	ns
		$\overline{MR}$ to Q7S; see Figure 12	[3]								
		V_{CC} = 2 V		-	47	175	-	220	-	265	ns
		V_{CC} = 4.5 V		-	17	35	-	44	-	53	ns
		V_{CC} = 6 V		-	14	30	-	37	-	45	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Figure 13	[4]								
		V_{CC} = 2 V		-	47	150	-	190	-	225	ns
		V_{CC} = 4.5 V		-	17	30	-	38	-	45	ns
		V_{CC} = 6 V		-	14	26	-	33	-	38	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Figure 13	[5]								
		V_{CC} = 2 V		-	41	150	-	190	-	225	ns
		V_{CC} = 4.5 V		-	15	30	-	38	-	45	ns
		V_{CC} = 6 V		-	12	27	-	33	-	38	ns
t_W	pulse width	SHCP HIGH or LOW; see Figure 9									
		V_{CC} = 2 V		75	17	-	95	-	110	-	ns
		V_{CC} = 4.5 V		15	6	-	19	-	22	-	ns
		V_{CC} = 6 V		13	5	-	16	-	19	-	ns
		STCP HIGH or LOW; see Figure 10									
		V_{CC} = 2 V		75	11	-	95	-	110	-	ns
		V_{CC} = 4.5 V		15	4	-	19	-	22	-	ns
		V_{CC} = 6 V		13	3	-	16	-	19	-	ns
		$\overline{MR}$ LOW; see Figure 12									
		V_{CC} = 2 V		75	17	-	95	-	110	-	ns
		V_{CC} = 4.5 V		15	6	-	19	-	22	-	ns
		V_{CC} = 6 V		13	5	-	16	-	19	-	ns

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Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 14.

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
t_{su}	set-up time	DS to SHCP; see Figure 10									
		V_{CC} = 2 V		50	11	-	65	-	75	-	ns
		V_{CC} = 4.5 V		10	4	-	13	-	15	-	ns
		V_{CC} = 6 V		9	3	-	11	-	13	-	ns
		SHCP to STCP; see Figure 11									
		V_{CC} = 2 V		75	22	-	95	-	110	-	ns
		V_{CC} = 4.5 V		15	8	-	19	-	22	-	ns
		V_{CC} = 6 V		13	7	-	16	-	19	-	ns
t_h	hold time	DS to SHCP; see Figure 11									
		V_{CC} = 2 V		3	–6	-	3	-	3	-	ns
		V_{CC} = 4.5 V		3	–2	-	3	-	3	-	ns
		V_{CC} = 6 V		3	–2	-	3	-	3	-	ns
t_{rec}	recovery time	$\overline{MR}$ to SHCP; see Figure 12									
		V_{CC} = 2 V		50	–19	-	65	-	75	-	ns
		V_{CC} = 4.5 V		10	–7	-	13	-	15	-	ns
		V_{CC} = 6 V		9	–6	-	11	-	13	-	ns
f_{max}	maximum frequency	SHCP or STCP; see Figure 9 and Figure 10									
		V_{CC} = 2 V		9	30	-	4.8	-	4	-	MHz
		V_{CC} = 4.5 V		30	91	-	24	-	20	-	MHz
		V_{CC} = 6 V		35	108	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC}	[6][7]	-	115	-	-	-	-	-	pF
74HCT595-Q100; V_{CC} = 4.5 V to 5.5 V											
t_{pd}	propagation delay	SHCP to Q7S; see Figure 9	[2]	-	25	42	-	53	-	63	ns
		STCP to Qn; see Figure 10	[2]	-	24	40	-	50	-	60	ns
		$\overline{MR}$ to Q7S; see Figure 12	[3]	-	23	40	-	50	-	60	ns
t_{en}	enable time	$\overline{OE}$ to Qn; see Figure 13	[4]	-	21	35	-	44	-	53	ns
t_{dis}	disable time	$\overline{OE}$ to Qn; see Figure 13	[5]	-	18	30	-	38	-	45	ns
t_W	pulse width	SHCP HIGH or LOW; see Figure 9		16	6	-	20	-	24	-	ns
		STCP HIGH or LOW; see Figure 10		16	5	-	20	-	24	-	ns
		$\overline{MR}$ LOW; see Figure 12		20	8	-	25	-	30	-	ns
t_{su}	set-up time	DS to SHCP; see Figure 10		16	5	-	20	-	24	-	ns
		SHCP to STCP; see Figure 11		16	8	-	20	-	24	-	ns
t_h	hold time	DS to SHCP; see Figure 11		3	–2	-	3	-	3	-	ns

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Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 14.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_{rec}	recovery time	$\overline{MR}$ to SHCP; see Figure 12	10	–7	-	13	-	15	-	ns
f_{max}	maximum frequency	SHCP and STCP; see Figure 9 and Figure 10	30	52	-	24	-	20	-	MHz
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [6][7]	-	130	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage.

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] t_{pd} is the same as t_{PHL} only.

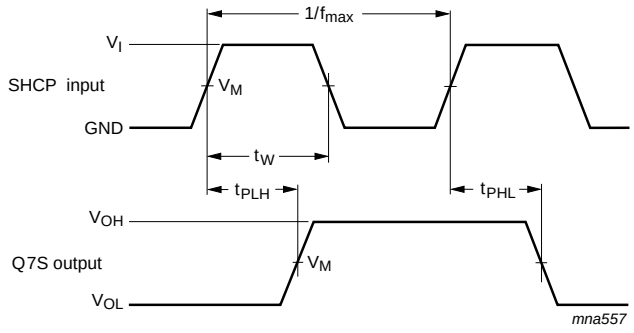
[4] t_{en} is the same as t_{PZL} and t_{PZH}.

[5] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

[7] All 9 outputs switching.

12. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. Shift clock pulse, maximum frequency and input to output propagation delays

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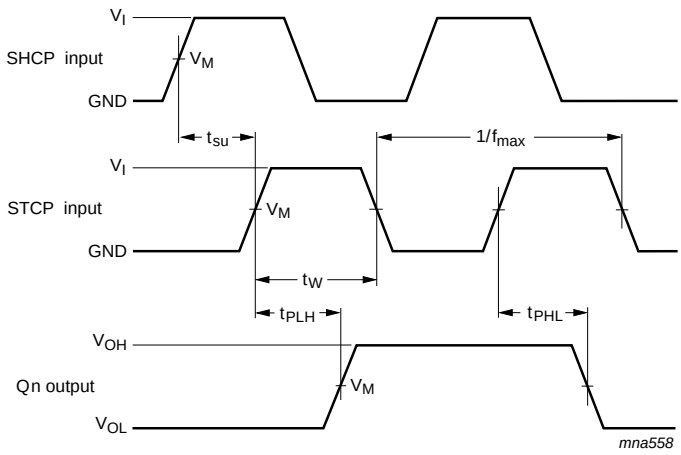
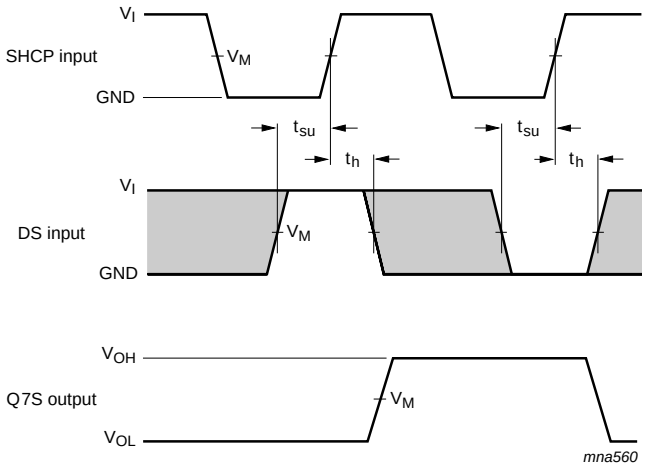


Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 10. Storage clock to output propagation delays



Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 11. Data set-up and hold times

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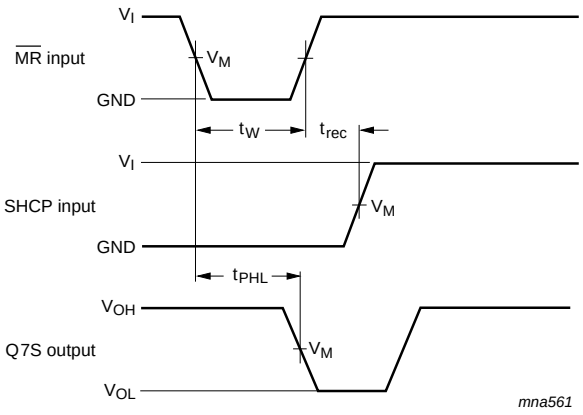
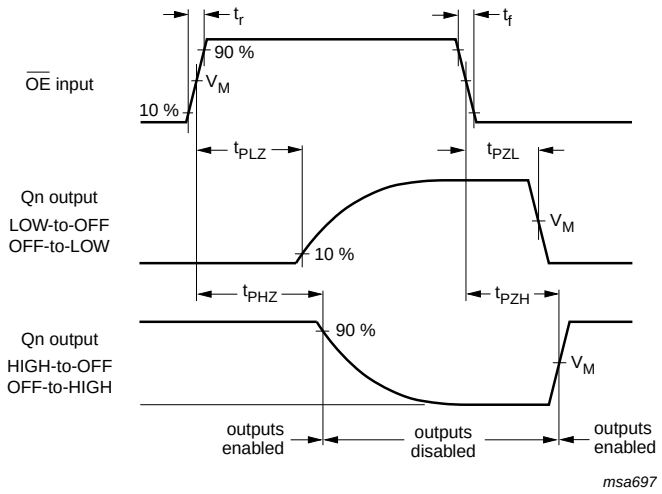


Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 12. Master reset to output propagation delays



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 13. Enable and disable times

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC595-Q100	$0.5V_{CC}$	$0.5V_{CC}$
74HCT595-Q100	1.3 V	1.3 V

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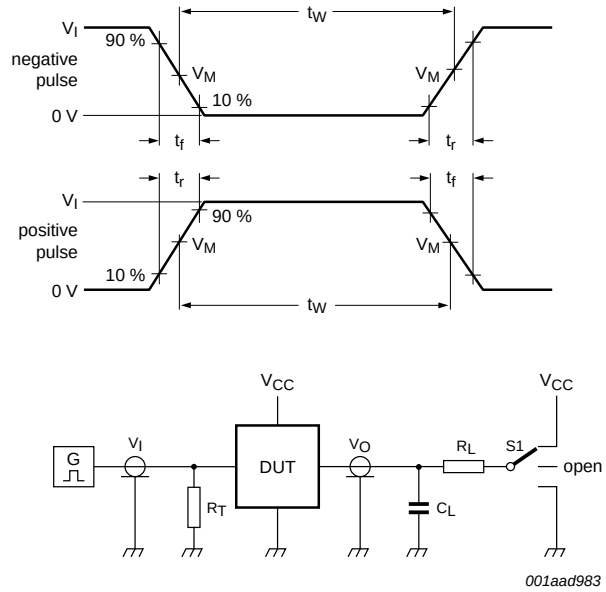

Test data is given in Table 9.

Definitions for test circuit:

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

S1 = test selection switch.

Fig 14. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC595-Q100	V_{CC}	6 ns	50 pF	1 kΩ	open	GND	V_{CC}
74HCT595-Q100	3 V	6 ns	50 pF	1 kΩ	open	GND	V_{CC}

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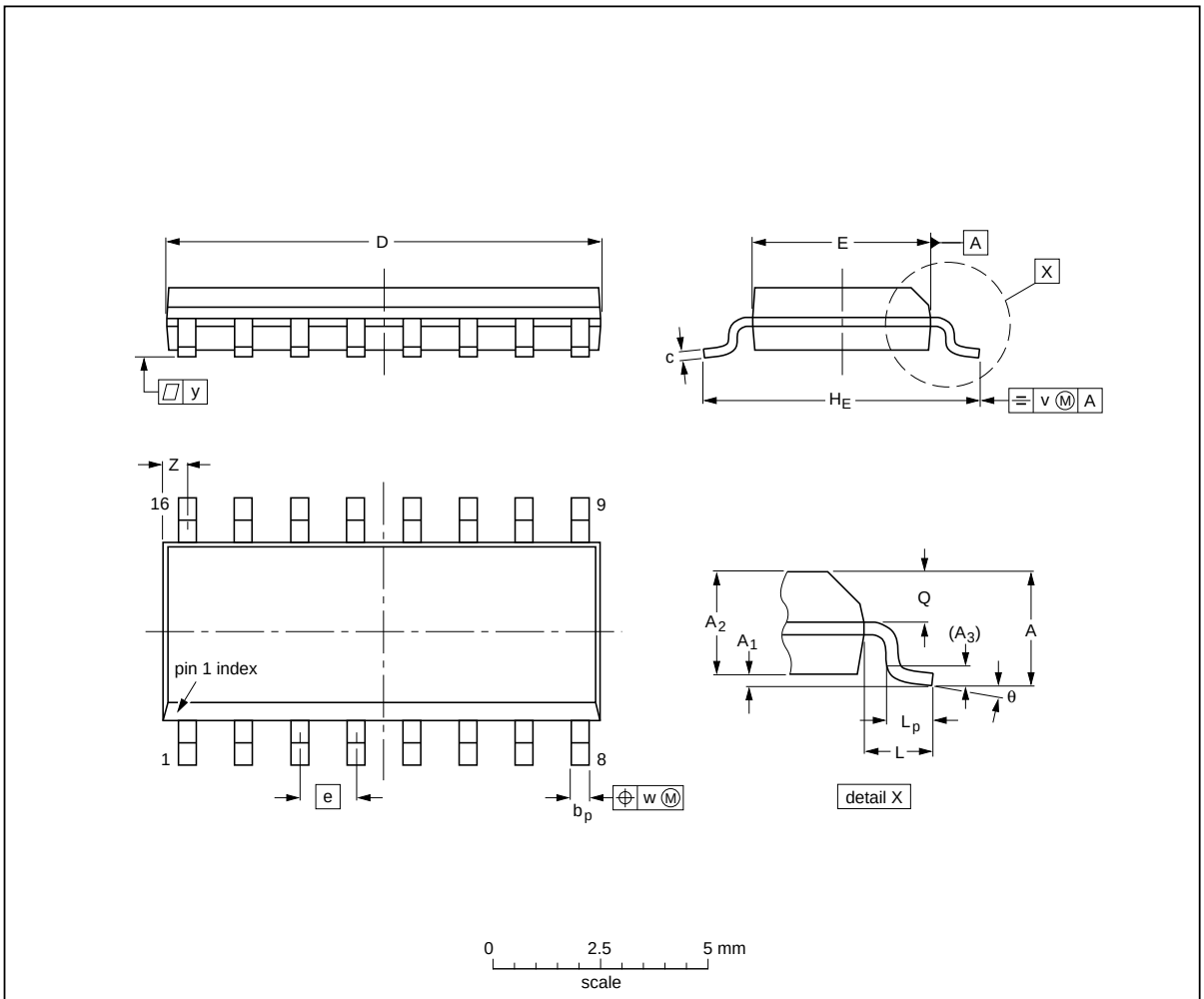
13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 15. Package outline SOT109-1 (SO16)

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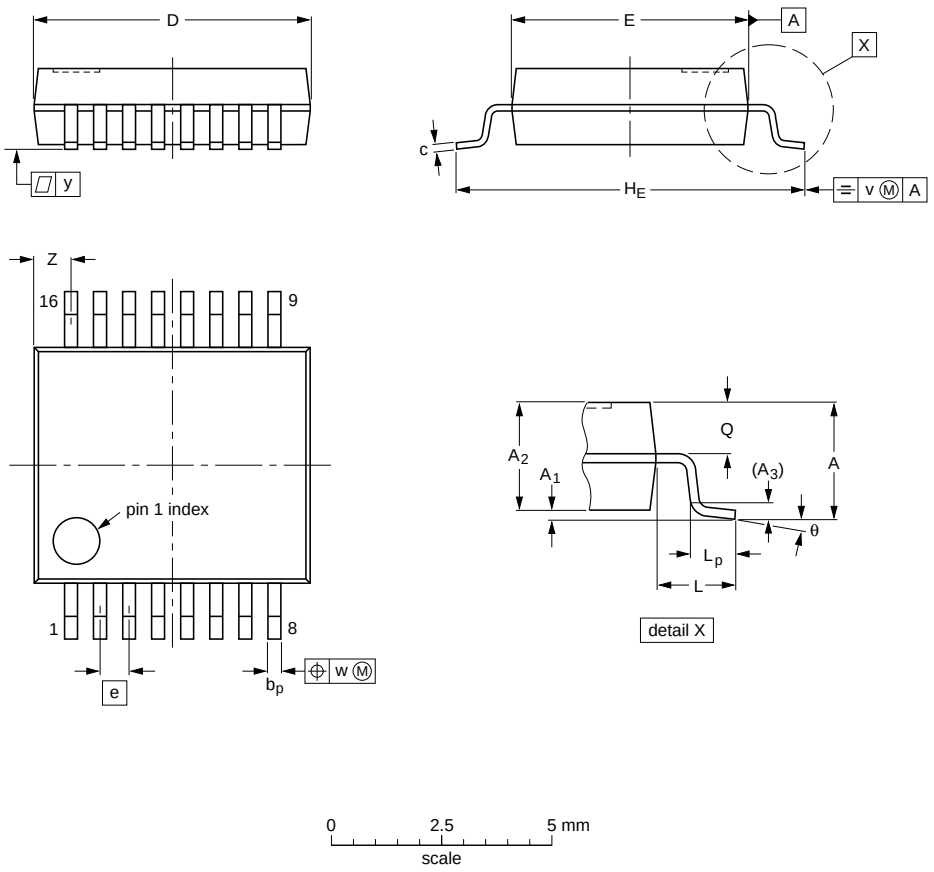
SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT338-1 (SSOP16)

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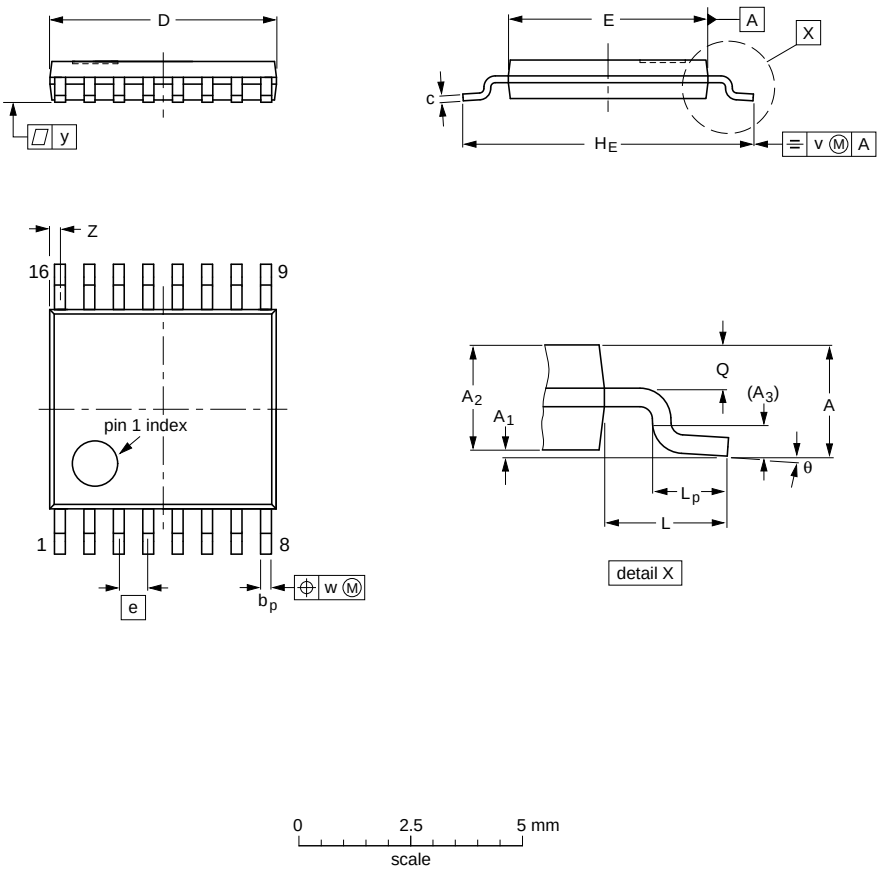
TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 17. Package outline SOT403-1 (TSSOP16)

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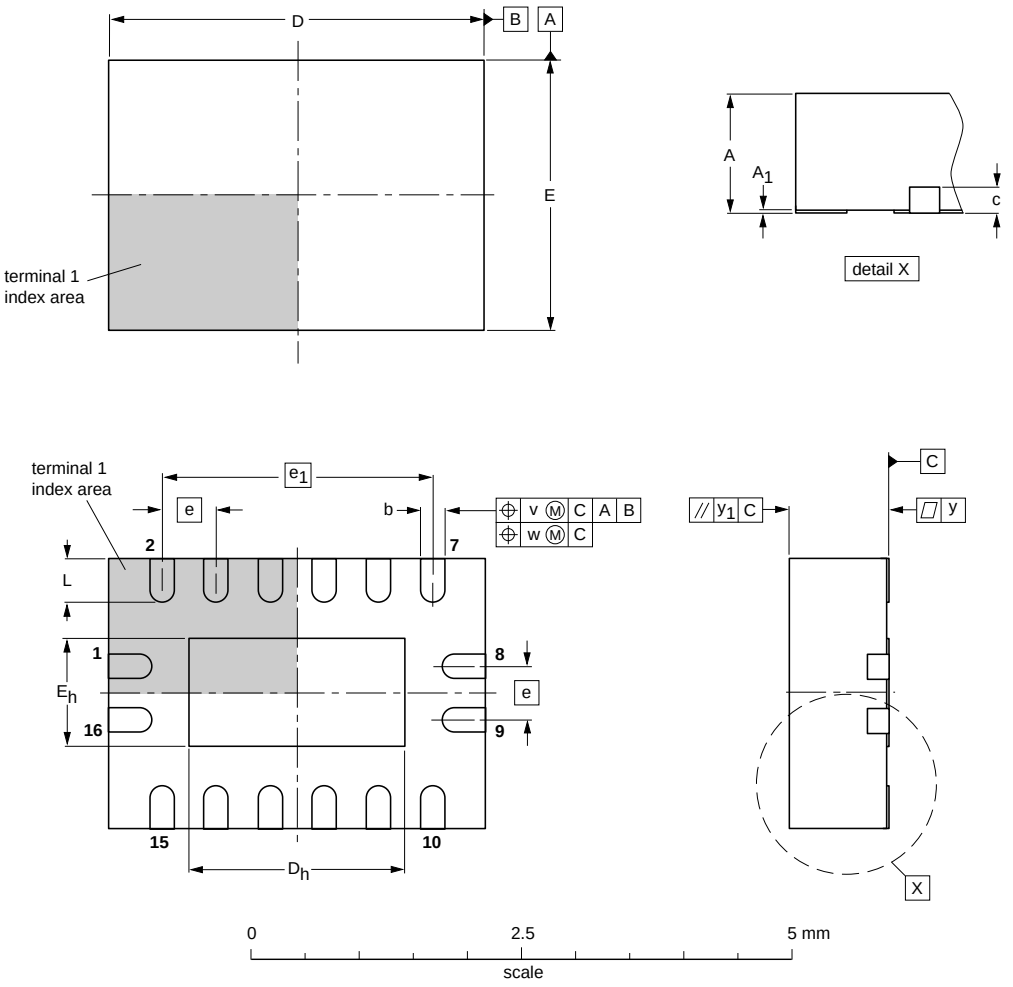
DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 18. Package outline SOT763-1 (DHVQFN16)

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14. Abbreviations

Table 10. Abbreviations

Acronym	Abbreviation
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model
MIL	Military

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT595_Q100 v.2	20130410	Product data sheet	-	74HC_HCT595_Q100 v.1
Modifications:	• 74HC595DB-Q100 and 74HCT595DB-Q100 added.			
74HC_HCT595_Q100 v.1	20120802	Product data sheet	-	-

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16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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