driven by ELMOS

E520.35

LIN SBC with Voltage Regulator and Watchdog

ADVANCE PRODUCT INFORMATION JUL 26, 2011

Features

- System basic chip (SBC) for LIN applications
- LIN transceiver V2.1, SAE-J2602, ISO9141
- Operating range 5V up to 28V, limited operating range 3.8V up to 40V
- typ. 10µA sleep current consumption
- 3.3V or 5.0V 2% in active mode, 5% in standby
- Peripheral Supply up to 100mA
- Flash mode
- TXD permanent low timeout
- Configurable µC window watchdog
- Very low bus leakage current in case of short to GND in sleep mode
- Edge triggered LIN remote wake-up
- VBAT 6:1 voltage divider
- BUS pin ESD-protected > 8 kV IEC-61000-4-2

Applications

Smart applications connected to the LIN bus

Brief functional description

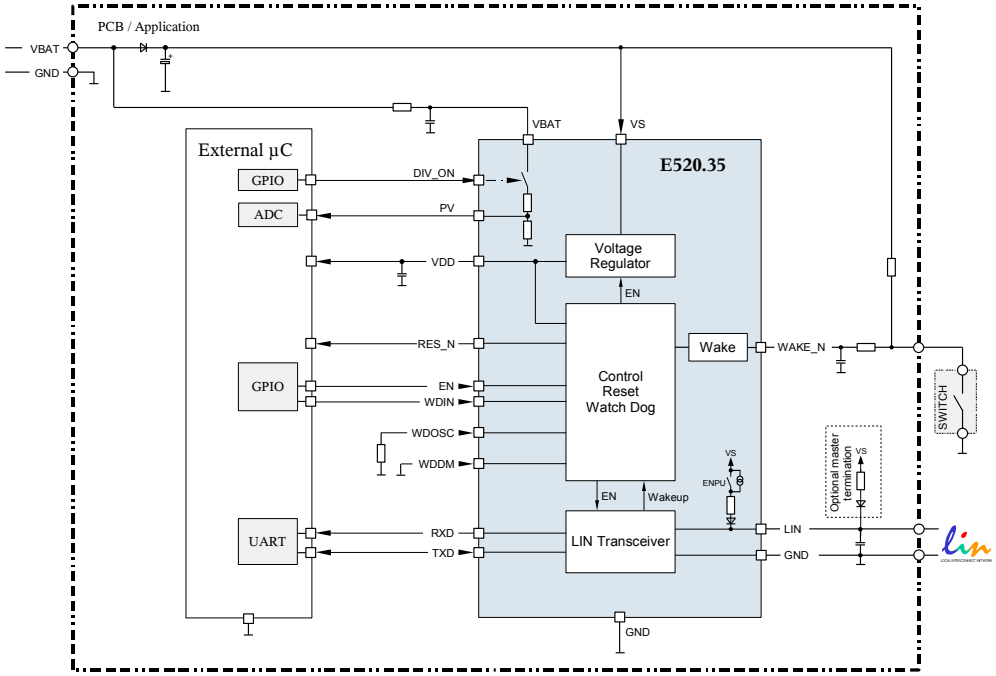
The LIN-SBC with voltage regulator provides a LIN tranceiver, the peripheral supply, reset generation for the µC and a watchdog.

The LIN SBC can be switched into standby- and sleep-mode which provides very low current consumption.

The device is capable to detect local and remote wake-up events to enable the voltage regulator. A flash mode provides higher datarate for end of line flashing.

Ordering Information

Product ID	Temp. Range	Package
E520.35	-40°C to +125°C	QFN20L5



1 Package and Pinout

1.1 Pin Description

No	*Name*	*Type*	*Description*
1	VBAT	HV_S	Battery supply for the voltage divider
2	n.c.		not connected
3	WAKE_N	A_I	local wake up input
4	n.c.		not connected
5	VS	HV_S	battery supply voltage
6	GND	HV_S	ground
7	n.c.		not connected
8	LIN	HV_A_IO	LIN bus terminal
9	n.c.		not connected
10	RES_N	D_O	reset output
11	WDIN	D_I	watchdog trigger input
12	WDOSC	A_I	watchdog cycle time configuration
13	WDDM	D_I	watchdog debug mode
14	EN	D_I	enable input
15	TXD	D_IO	data transmit input
16	RXD	D_O	receive data output
17	DIV_ON	D_I	input to switch on the internal voltage divider, active high
18	PV	A_O	voltage divider output
19	GND	HV_S	ground
20	VDD	HV_S	peripheral voltage supply

A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

Table 1: Pin Description

1.2 Package Reference

The device is assembled in a QFN20L5 package according to JEDEC standard MO-220, Issue K, as of June 2006. The referenced JEDEC variant is VHHC-2.

1.3 Package Pinout

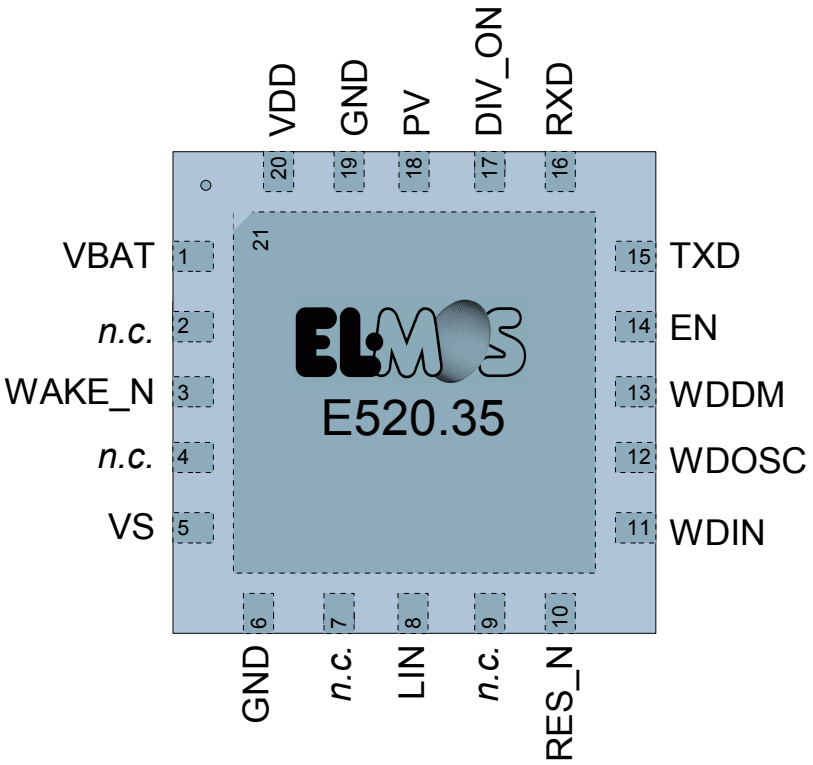


Fig. 1: Package Pinout

2 Block Diagram

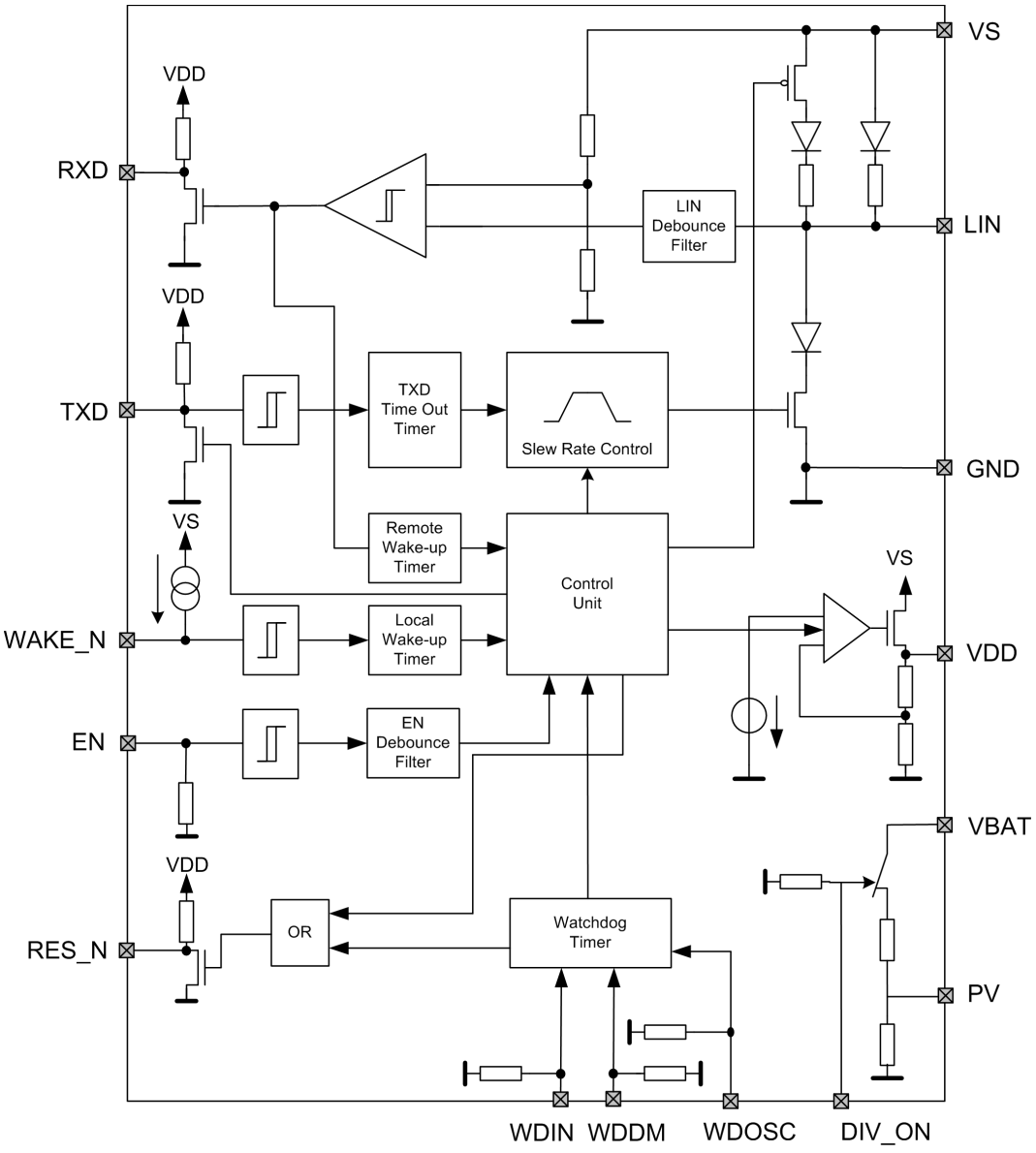


Fig. 2: Block Diagram

3 Operating Conditions

3.1 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied.
Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
All voltages referred to ground (GND). Currents flowing into terminals are signed as positive, those drawn out of a terminal are negative.

Description	*Condition*	*Symbol*	*Min*	*Max*	*Unit*
DC voltage at pin VS	continuous	$V_{S,DC}$	-0.3	40	V
Junction temperature	continuous	T_{JUNC}	-40	150	°C
Storage temperature	continuous	T_{STG}	-55	165	°C
DC voltage at pin WAKE_N	continuous, 33kΩ preresistance required	$V_{WAKE\_N,DC}$	-2	V_S + 0.3	V
DC current at pin WAKE_N	continuous	$I_{WAKE\_N,DC}$	-10	10	mA
DC voltage at pin VDD (5.0V device)	continuous	$V_{DD,DC5.0}$	-0.3	5.5	V
DC voltage at pin VDD (3.3V device)	continuous	$V_{DD,DC3.3}$	-0.3	3.6	V
DC current at pin VDD	continuous	$I_{DD,DC}$	-230	1	mA
DC input voltage at pin LIN, VBAT	continuous	$V_{LIN,DC}$	-24	40	V
TRAN input voltage at pin LIN, VBAT	pulse for max. 500ms	$V_{LIN,TRAN}$	-27	40	V
DC Voltage Level for pin EN,RES_N,RXD,TXD,WDIN,WDOSC,WDDM,DIV_ON	continuous	$V_{IO,DC}$	-0.3	$V_{DD,DC}$ +0.3	V
DC Current Level for pin EN,RES_N,RXD,TXD,WDIN,WDOSC,WDDM,DIV_ON	continuous	$I_{IO,DC}$	-10	1	mA

ESD Protection

Description	Condition	Symbol	Min	Typ	Max	Unit
ESD protection at pin LIN	AEC-Q100-002 (HBM), C=100pF, R=1.5kΩ chiplevel	$V_{LIN,ESDHBM}$ to GND	8	-	-	kV
ESD protection at pin VS	AEC-Q100-002 (HBM), C=100pF, R=1.5kΩ chiplevel	$V_{VSUP,ESDHBM}$ to GND	8	-	-	kV
ESD protection at pin LIN	IEC 61000-4-2 [1] C=150 pF, R=330Ω	$V_{LIN,ESD}$ to GND	8	-	-	kV
ESD protection at pin VS	IEC 61000-4-2 C=150 pF, R=330Ω with external C=100 nF at VS	$V_{VSUP,ESD}$ to GND	8	-	-	kV
ESD protection at all	AEC-Q100-002 (HBM), C=100pF, R=1.5kΩ chiplevel	$V_{PIN,ESDHBM}$	2	-	-	kV
ESD protection at pin WAKE_N	AEC-Q100-002 (HBM), C=100pF, R=1.5kΩ chiplevel	V_{WAKE} to GND	8	-	-	kV
ESD protection at pin WAKE_N	IEC 61000-4-2 with external R=33 kΩ	V_{WAKE} to GND	8	-	-	kV
ESD protection at all pins	AEC-Q100-011 (CDM), R=1 Ω chiplevel	$V_{PIN,ESDCDM}$	500	-	-	V
ESD protection at all pins	AEC-Q100-003 (MM), C=200 pF chiplevel	$V_{PIN,ESDMM}$	200	-	-	V

[1] verified incl. capacitance on pin LIN of 0pF and 220pF, on pin VSUP of $C_{SUP,RF}$

3.2 Recommended Operating Conditions

Within the recommended operating conditions the IC operates as described in the functional description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
functional range		$V_{S,FUNC}$	5	-	28	V
limited functional range; no system reset occures	-60mA < I_{DD}	$V_{S,FL,LR}$	3.8	-	7	V
limited functional range; no system reset occures	-60mA < I_{DD}	$V_{S,FL,HR}$	18	-	40	V
ambient temperature		T_{AMB}	-40	-	125	°C
maximum IO current at each pin, if not specified otherwise		$I_{IO,LUP}$	-10	-	10	mA

4 Thermal Characteristics

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Thermal resistance junction to ambient QFN20L5 package	according to JEDEC standard JESD-51-5	R_{TJA}	-	22	-	K/W

(1) Values are based on method according to JEDEC JESD-51-5.

5 Electrical Characteristics

(V_S = +5V to +28V, Tamb = -40°C to +125°C, unless otherwise noted.
Typical values are at V_S = +12.0V and Tamb = +25°C. Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Power Supply and References						
current consumption in active mode	LIN dominant, I_{DD}=0mA	$I_{S,ACT,DOM}$	-	-	5	mA
current consumption in active mode	LIN recessive, I_{DD}=0mA	$I_{S,ACT,REC}$	-	-	2	mA
standby current	standby mode, V_S =V_{LIN} =V_{WAKE_N} =13.5V, I_{DD}=0mA	$I_{S,STBY}$	-	70	96	µA
sleep current	sleep mode, LIN recessive, V_S =V_{LIN} =V_{WAKE_N} =13.5V	$I_{S,SLEEP}$	-	10	20	µA
sleep current, LIN is neither recessive nor dominant, not production tested	sleep mode, LIN is floating V_S =V_{WAKE_N} =13.5V, V_{LIN} > $V_{LIN,THDOM}$	$I_{S,SLEEP,LIN}$	-	-	60	µA
SBC Operating Modes						
debounce filter for active mode transition		t_{2AM}	23	25	34	µs
debounce filter for standby mode transition		t_{2STBY}	23	25	34	µs
debounce filter for sleep mode transition		t_{2SLEEP}	23	25	34	µs
debounce filter for flash mode transition		t_{2FM}	2	4	6	µs
open window for flash mode acknowledge		t_{FMACK}	5	7.5	10	µs
flash mode time out		t_{FMTO}	1.2	-	2	ms
delay for switching off the VDD regulator after entering sleep mode		$t_{DD,OFFDEL}$	64	128	-	µs

Electrical Characteristics (continued)

(V_S = +5V to +28V, Tamb = -40°C to +125°C, unless otherwise noted.
Typical values are at V_S = +12.0V and Tamb = +25°C. Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Reset Parameters						
power on reset according to pin VS		$V_{S,POR}$	4.0	-	5.0	V
power down threshold according to pin VS		$V_{S,PD}$	3.0	-	3.8	V
reset assert level at pin VDD (3.3V device)		$V_{DD,RSTA3.3}$	2.4	-	2.8	V
reset assert level at pin VDD (5.0V device)		$V_{DD,RSTA5.0}$	4.2	-	4.6	V
reset release level at pin VDD (3.3V device)		$V_{DD,RSTD3.3}$	2.6	-	3.0	V
reset release level at pin VDD (5.0V device)		$V_{DD,RSTD5.0}$	4.4	-	4.8	V
reset hysteresis at pin VDD (3.3V device), not production tested	$V_{DD,RSTD3.3}$ - $V_{DD,RSTA3.3}$	$V_{DD,HYST3.3}$	100	-	400	mV
reset hysteresis at pin VDD (5.0V device), not production tested	$V_{DD,RSTD5.0}$ - $V_{DD,RSTA5.0}$	$V_{DD,HYST5.0}$	100	-	400	mV
RES_N activation time		t_{RES_N}	2	3	5	ms
undervoltage debounce time		$t_{RES\_N,\ RSTA}$	60	-	90	µs
Monitor Parameters						
thermal shutdown flag threshold		T_{SHDN}	150	-	180	°C
thermal shutdown flag hysteresis, not production tested		T_{HYST}	5	-	22	K
voltage regulator shut down debounce time		$t_{DD,SHDN}$	-	50	-	µs
Local Wake Up						
leakage current	V_{WAKE_N}=V_S=18V	$I_{WAKE\_N,LEAK}$	-5	-	5	µA
input low level		$V_{WAKE\_N,INL}$	2.5	3.0	3.5	V
input high level		$V_{WAKE\_N,INH}$	3.0	3.5	4.0	V
input hysteresis, not production tested		$V_{WAKE\_N,HYST}$	0.2	0.5	0.8	V
pull up current	V_S < 28 V, V_{WAKE_N} = 0 V	$I_{WAKE\_N,PU}$	-30	-10	-	µA
input debouncing filter time		$t_{WAKE\_N,DB}$	-	-	25	µs

Electrical Characteristics (continued)

(V_S = +5V to +28V, Tamb = -40°C to +125°C, unless otherwise noted.
Typical values are at V_S = +12.0V and Tamb = +25°C. Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Voltage Regulator						
output voltage range (5.0V device)	active mode VS > 7V	$V_{DD,ACT5.0}$	4.9	5.0	5.1	V
output voltage range (3.3V device)	active mode	$V_{DD,ACT3.3}$	3.23	3.3	3.37	V
output current range	VDD accuracy 2%	$I_{DD,ACT}$	-60	-	-	mA
output current range	VDD accuracy TBD%	$I_{DD,ACT}$	-100	-	-	mA
output current limitation		$I_{DD,LIM}$	-230	-	-140	mA
voltage drop between pin VS and pin VDD for V_{DD} = 5 V	3.8V < V_S < ($V_{DD,ACTXX}$+ 300mV), -60mA<I_{DD}	$V_{DD,LD60m}$	-	-	300	mV
voltage drop between pin VS and pin VDD for V_{DD} = 5 V	3.8V < V_S < ($V_{DD,ACTXX}$+50mV), -5mA < I_{DD}	$V_{DD,LD5m}$	-	-	50	mV
power supply ripple rejection, not production tested	10 Hz to 100 Hz 10 uF capacitor at pin VDD, V_S = 14V, IVCC = 15 mA	PSSR	50	-	-	dB
output voltage range (5.0V device)	standby mode	$V_{DD,STBY5.0}$	4.75	5.0	5.25	V
output voltage range (3.3V device)	standby mode	$V_{DD,STBY3.3}$	3.135	3.3	3.465	V
output current range	standby mode	$I_{DD,STBY}$	-60	-	-	mA
LIN Transceiver						
functional range LIN transceiver		$V_{LIN,VS}$	7	-	18	V
recessive output voltage	TXD=1	$V_{LIN,REC}$	V_S -1V	-	V_S	V
dominant output voltage	TXD=0, V_S=7.0V, R_{LIN}=0.5kΩ to V_S	$V_{LIN,DOM}$	-	-	1.2	V
dominant output voltage	TXD=0, V_S=18V, R_{LIN}=0.5kΩ to V_S	$V_{LIN,DOM1}$	-	-	2.0	V
receiver dominant level		$V_{LIN,THDOM}$	-	-	0.4 *V_S	V
receiver recessive level		$V_{LIN,THREC}$	0.6 *V_S	-	-	V
LIN bus center voltage	$V_{LIN,BUSCNT}$= ($V_{LIN,THDOM}$+$V_{LIN,THREC}$)/2	$V_{LIN,BUSCNT}$	0.475 *V_S	-	0.525 *V_S	V
receiver hysteresis	$V_{LIN,THREC}$- $V_{LIN,THDOM}$	$V_{LIN,HYS}$	TBD	-	0.175 *V_S	V

Electrical Characteristics (continued)

(V_S = +5V to +28V, Tamb = -40°C to +125°C, unless otherwise noted.
Typical values are at V_S = +12.0V and Tamb = +25°C. Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
output current limitation	$V_{LIN} = V_{VS,MAX}$ = 18 V	$I_{LIN,LIM}$	40	-	200	mA
pull up resistance		$R_{LIN,SLAVE}$	20	33	60	kΩ
leakage current flowing into pin LIN	transmitter passive, 7V<V_S<18V, 7V<V_{LIN}<18V, V_{LIN}>V_S	$I_{LIN,BUSREC}$	-	-	20	µA
pull up current flowing out of pin LIN	transmitter passive, 7V<V_S<18V, V_{LIN}=0V	$I_{LIN,BUSDOM}$	-1	-	-	mA
leakage current, loss of ground (GND device = VS)	V_S=13.5V, 0V<V_{LIN}<18V	$I_{LIN,NOGND}$	-1	-	0.1	mA
LIN leakage current, unsupplied node	V_S=0V, 0V<V_{LIN}<18V	I_{LIN}	-	-	20	µA
LIN leakage current, unsupplied node, T = 85 °C, not production tested	V_S=0V, 0V<V_{LIN}<18V	$I_{LIN,85}$	-	-	15	µA
clamping voltage, not production tested	V_S=0V, I_{LIN}=1mA	$V_{LIN,CLAMP}$	40		-	V
input capacitance, not production tested!	7V < V_S < 18V	$C_{LIN,PIN}$	-	-	30	pF
output slew rate	C_{LIN}=1-10nF, R_{LIN}=0.5-1kΩ, 1µs<t_{LIN}<5µs, V_S=18V	$SR_{LIN,OUT}$	1	-	3	V/µs
output slew rate	C_{LIN}=1-10nF, R_{LIN}=0.5-1kΩ, 1µs<t_{LIN}<5µs, V_S=7.0V	$SR_{LIN,OUT1}$	0.5	-	3	V/µs
symmetry of rising and falling edge	V_S=18V	$t_{LIN,SYM}$	-5	-	5	µs
transmit propagation delay		$t_{TXD,PDT}$	-	-	4	µs
transmit propagation delay symmetry		$t_{TXD,SYM}$	-2	-	2	µs
receive propagation delay		$t_{RXD,PDR}$	-	-	6	µs
receive propagation delay symmetry		$t_{RXD,SYM}$	-2	-	2	µs
LIN bus puls receiver debounce time		$t_{LIN,DB}$	0.3	-	6	µs
wake-up debounce time		$t_{LIN,WU}$	70	-	150	µs

Electrical Characteristics (continued)

(V_S = +5V to +28V, Tamb = -40°C to +125°C, unless otherwise noted.
Typical values are at V_S = +12.0V and Tamb = +25°C. Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Duty cycle 1 [1)]	$V_{LIN,THREC}$(max) =0.744*V_S, $V_{LIN,THDOM}$(max) =0.581*V_S, V_S=7-18V, t_{BIT}=50us, $D_{LIN,1}$=t_{BUSREC}(min) /(2*t_{BIT})	$D_{LIN,1}$	0.396	-	-	-
Duty cycle 2 [1)]	$V_{LIN,THREC}$(min) =0.422*V_S, $V_{LIN,THDOM}$(min) =0.284*V_S, V_S=7-18V, t_{BIT}=50us, $D_{LIN,2}$=t_{BUSREC}(max)/(2*t_{BIT})	$D_{LIN,2}$	-	-	0.581	-
Duty cycle 3 [1)]	$V_{,LIN,THREC}$(max) =0.778*V_S, $V_{LIN,THDOM}$(max) =0.616*V_S, V_S=7-18V, t_{BIT}=96us, $D_{LIN,3}$=t_{BUSREC}(min) /(2*t_{BIT})	$D_{LIN,3}$	0.417	-	-	-
Duty cycle 4 [1)]	$V_{LIN,THREC}$(min) =0.389*V_S, $V_{LIN,THDOM}$(min) =0.251*V_S, V_S=7-18V, t_{BIT}=96us, $D_{LIN,4}$=t_{BUSREC}(max)/(2*t_{BIT})	$D_{LIN,4}$	-	-	0.590	-
receive data baud rate	flash mode, V_S=13V	$B_{LIN,RXD}$	-	115	-	kBaud
transmit data baud rate	flash mode, V_S=13V	$B_{LIN,TXD}$	-	250	-	kBaud

1) Bus load conditions (C_{LIN},R_{LIN}): 1nF, 1kΩ/6.8nF, 660Ω/10nF, 500Ω

Electrical Characteristics (continued)

(V_S = +5V to +28V, Tamb = -40°C to +125°C, unless otherwise noted.
Typical values are at V_S = +12.0V and Tamb = +25°C. Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
EN						
input low level range		$V_{EN,INL}$	-	-	0.25 *V_{DD}	V
input high level range		$V_{EN,INH}$	0.75 *V_{DD}	-	-	V
pull down resistor	V_{EN}=5.0V	$R_{EN,PD}$	-	120	-	kΩ
input leakage	V_{EN}=0V	$I_{EN,LEAK}$	-5	-	5	µA
TXD						
input low voltage range		$V_{TXD,INL}$	-	-	0.25 *V_{DD}	V
input high voltage range		$V_{TXD,INH}$	0.75 *V_{DD}	-	-	V
output low level range	I_{TXD}=1mA	$V_{TXD,OUT}$	-0.3	-	0.66	V
TXD pull up resistor	V_{TXD}=0V	$R_{TXD,PU}$	-	120	-	kΩ
time out detection of TXD	TXD = 0 V, active mode	$t_{TXD,TO}$	6	10	14	ms
RXD						
output low level range	I_{RXD}=1mA	$V_{RXD,OUT}$	-0.3	-	0.66	V
pull up resistance	V_{RXD}=0V	$V_{RXD,PU}$	-	5	-	kΩ
Reset						
output low level range	I_{RES_N}=1mA	$V_{RES\_N,OUT}$	-0.3	-	0.66	V
pull up resistance	V_{RES_N}=0V	$I_{RES\_N,PU}$	-	5	-	kΩ
Watchdog						
input low level range at pins WDIN, WDDM		$V_{WDIN,INL}$	-	-	0.25 * V_{DD}	V
input high level range at pins WDIN, WDDM		$V_{WDIN,INH}$	0.75 * V_{DD}	-	-	V
pull down resistor at pins WDIN, WDDM	V_{WDIN}=5.0V	$R_{WDIN,PD}$ $R_{WDDM,PD}$	-	120	-	kΩ
reference current	V_{WDOSC}=1V	$I_{WDOSC,REF}$	-	14	-	µA
reference resistor		$R_{WD,OSC}$	10		100	kΩ
watchdog oscillator periode for 10kΩ resistance	R_{WDOSC}=10kΩ	$t_{WD,OSC10k}$	8.4	10	12.3	µs
watchdog oscillator periode for 100kΩ resistance	R_{WDOSC}=100kΩ	$t_{WD,OSC100k}$	84	100	123	µs
first trigger open window	open window after RES_N is released	$t_{WD,FIRST}$	91	110	135	ms

Electrical Characteristics (continued)

(V_S = +5V to +28V, Tamb = -40°C to +125°C, unless otherwise noted.
Typical values are at V_S = +12.0V and Tamb = +25°C. Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
watchdog cycle time		$t_{WD,CYC}$	-	1024 *$t_{WD,OSC}$	-	ms
open window time		$t_{WD,OW}$	-	0.5 *$t_{WD,CYC}$	-	ms
closed window time		$t_{WD,CW}$	-	0.5 *$t_{WD,CYC}$	-	ms
watchdog reset time		$t_{WD,RES}$	414	512	645	µs
watchdog trigger pulse width		$t_{WD,CMD}$	80	100	120	µs
VBAT Voltage divider						
divider ratio	5 V < V_S < 18 V	$DR_{PV,3.3V}$	-	1:6	-	-
divider ratio	5 V < V_S < 28 V	$DR_{PV,5V}$	-	1:6	-	-
V_{BAT} range of divider linearity	V_{DD} = 3.3 V	$L_{VBAT,3.3V}$	3.3	-	18	V
V_{BAT} range of divider linearity	V_{DD} = 5 V	$L_{VBAT,5V}$	5	-	28	V
divider ratio error, not production tested		DRE_{PV}	-1.2	-	1.2	%
V_{BAT} input current	V_{BAT} = 13.8 V	I_{VBAT}	-	150	-	µA
reverse current	V_{BAT} = -24 V	I_{VBAT_REV}	-1		-	mA
Maximum output Voltage at PV	18 V < V_{BAT} < 40 V	$V_{PV,MAX,3.3V}$	-	1 *V_{DD}	-	V
Maximum output Voltage at PV	28 V < V_{BAT} < 40 V	$V_{PV,MAX,5V}$	-	1 *V_{DD}	-	V
divider temperature drift, not production testes		T_R	-	tbd	-	ppm/K
input low level range		$V_{DIV\_ON,INL}$	-	-	0.25 *V_{DD}	V
input high level range		$V_{DIV\_ON,INH}$	0.75 *V_{DD}	-	-	V
input pull down resistance	V_{DIV_ON} = 5 V	$R_{DIV\_ON,PD}$	-	120	-	kΩ

6 Functional Description

The E520.35 is the interface between the physical bus in a Local Interconnect Network (LIN) and the LIN master / slave protocol controller according to LIN 2.1 specification. The device provides local and remote wake-up capability in sleep and standby mode. A wake-up source flag can be evaluated by the microcontroller. The integrated TXD dominant clamp timeout prevents the LIN network from permanent distortion in case of hardware failure. The flash mode provides higher datarates on the LIN pin for end-of-line or in-car flashing up to 115 kBaud.

The integrated voltage regulator supplies the microcontroller and peripheral blocks with current up to 60mA (2% accuracy). A higher current up to 100mA can be supplied with lower accuracy. For applications with a permanent supplied microcontroller a standby mode with active voltage regulator and low quiecent current consumption is implemented.

The cycle time of the integrated window watchdog can be configured by external resistor. For software development purpose the watchdog can be disabled.

The integrated reverse polarity protected 6:1 voltage divider can be connected to the battery supply to measure the supply voltage with fast response time. To limit the output voltage in case of VBAT overvoltage a clamping to the microcontroller supply voltage is integrated.

6.1 Operating Modes

The E520.35 provides the following operation modes:

6.1.1 Power-off mode

The device enters Power-off mode in case the battery voltage is lower than $V_{S,PD}$ voltage level. In Power-off mode the voltage regulator is switched off. If the battery voltage rises above the power on reset threshold level $V_{S,POR}$ the device resets the system via activating pin RES_N. The device enters mode Power-On.

6.1.2 Power-on mode

When the voltage at pin VS exceeds the Power-on-reset threshold voltage $V_{S,POR}$, the device enters power-on mode. In that mode the voltage regulator is switched on. After pin VDD exceeds $V_{DD,RSTD}$, RES_N is held low for t_{RES_N}. Now with setting pin EN to active HIGH level for a time period of at least t_{2AM} the device enters active mode.
Any wake-up request from mode SLEEP is indicated by setting the pin RXD to LOW level.
The wake-up source can be recognized by the microcontroller by reading the level at pin TXD. A weak pull up indicates a remote wake-up request and strong pull down indicates a local wake-up request.
Note: The voltage regulator over temperature shut down results in a transition to Power-on mode and the regulator is switched off. The voltage regulator will be switched on if the junction temperature falls below the specified temperature hysteresis T_{HYST}.

6.1.3 Active mode

In Active mode the device is able to transmit and receive data via the LIN bus line. The receiver transfers the detected LIN bus data via pin RXD to the microcontroller: HIGH at a recessive level and LOW at a dominant level on the bus. The receiver has a debounced VS supply related threshold with hysteresis. The transmit data at the TXD input is converted by the transmitter into a LIN bus signal. The LIN bus slew rate is optimized to minimize EME. The LIN bus output pin is pulled HIGH via an internal slave termination resistor. For a master application an external termination is needed.
The device enters active mode from:

- standby mode or power-up mode whenever a HIGH level on pin EN is maintained for a time of at least t_{2AM}
- flash mode after a time out of t_{FMTO}
- active mode in case of a LOW-level on pin EN, maintained for a time of at least t_{2STBY}.

6.1.4 Standby mode

In standby mode the voltage regulator is activated. Also the slave termination resistor at pin LIN is enabled. The watch dog is switched off.
Any wake-up request is indicated by setting the pin RXD to LOW level.
The wake-up source can be recognized by the microcontroller by reading the level at pin TXD. A weak pull up indicates a remote wake-up request and strong pull down indicates a local wake-up request.

6.1.5 Sleep mode

The sleep mode is a very low power mode of the device. After entering standby mode a TXD LOW level for at least t_{2SLEEP} will result in entering sleep mode. The transition to sleep mode can be performed independently from the actual level on pin LIN or pin WAKE_N. In Sleep mode the voltage regulator is deactivated and becomes high omic after a delayed time of $t_{DD,OFFDEL}$.
The transition into mode sleep is prohibited if a wake-up request is pending. The request must be cleared via a transition to mode Active.
In sleep mode the internal slave resistor termination at LIN bus pin is switched off. A power-saving weak pull-up between pins LIN and VS is still present.
The device can be woken up remotely via pin LIN or locally via pin WAKE_N. Debounce filters prevent unwanted wake-up events due to EMI at the inputs of the wake-up sources.

6.1.6 Flash mode

The flash mode allows a higher transmit baud rate up to 115 kBds and the receive baud rate up to 250 kBds. For further information see chapter „LIN flash mode“.

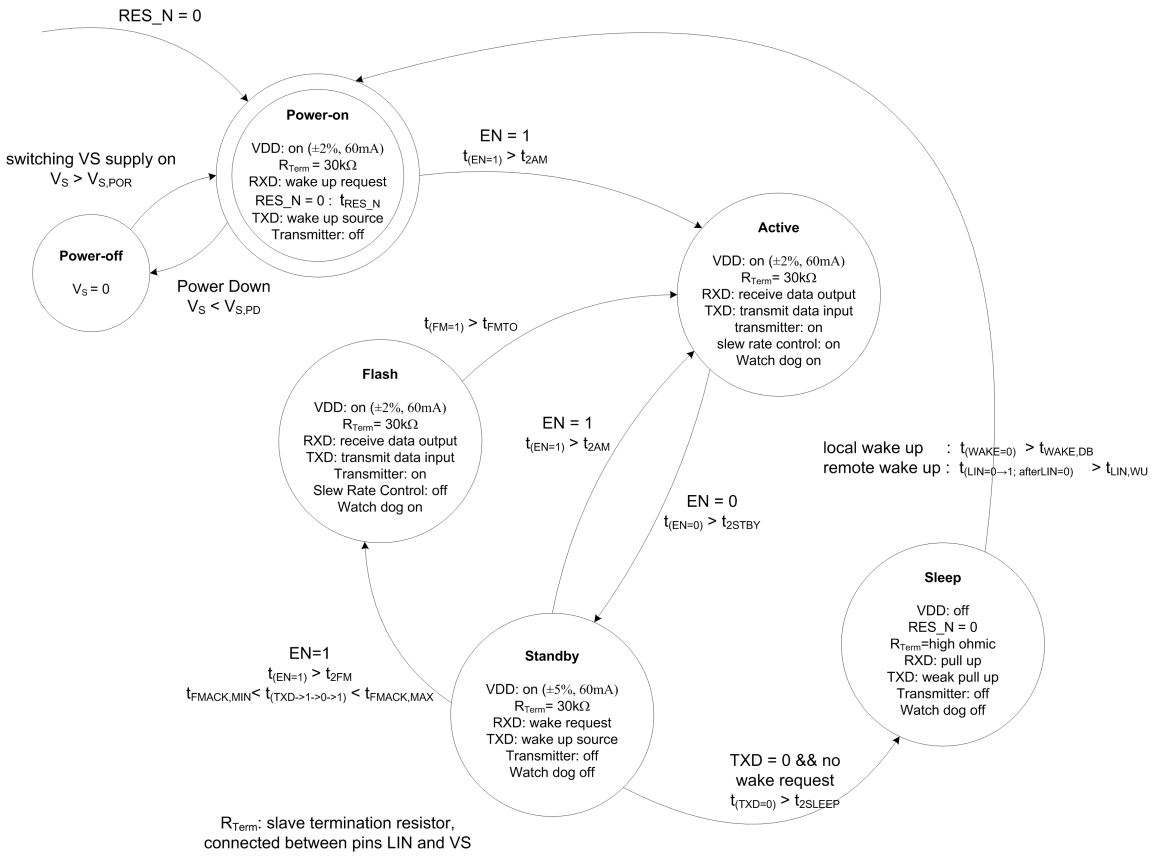


Fig. 3: SBC State Diagram

Mode	*EN*	*VDD*	*RXD*	*TXD*	*LIN*	*Watch Dog*
Power-off	high ohmic	off	high ohmic	high ohmic	high ohmic	off
Power-on	low	on	strong pull down output for wake-up request	weak pull up output if remote wake-up; strong pull down output if local wake-up	off	on after RES_N is high
Active	high	on	pull up for LIN recessive; strong pull down output for LIN dominant	high level input for LIN recessive; low level input for LIN dominant	on; slew rate control activated	on
Standby	low	on	strong pull down output for wake-up request	weak pull up output if remote wake-up; strong pull down output if local wake-up	transmitter off termination on	off
Sleep	low	off	pull up	pull down	off	off

Mode	EN	VDD	RXD	TXD	LIN	Watch Dog
Flash	high	on	pull up for LIN recessive; strong pull down output for LIN dominant	high level input for LIN recessive; low level input for LIN dominant	on; slew rate control deactivated	on

Table 2: Pin Functionality

6.2 Voltage Regulator

The on chip low drop voltage regulator provides the voltage V_{DD} (typ. 3.3V or 5.0V depending on version) at pin VDD. It supplies the peripheral circuitry of the SBC and the host MCU chip with typical 60mA (2%) or up to 100mA with lower accuracy.

The voltage regulator is activated in all operating modes except in sleep mode. In sleep mode the voltage regulator is switched off.

The voltage regulator output current is limited to $I_{DD,LIM}$. The current limitation is always activated.

6.3 LIN Transceiver

6.3.1 LIN physical layer

The LIN BUS Interface is conform to LIN Physical Layer Specification Revision 2.1 and can be used for master or slave applications. The device has an internal slave termination implemented. Master termination has to be applied externally.

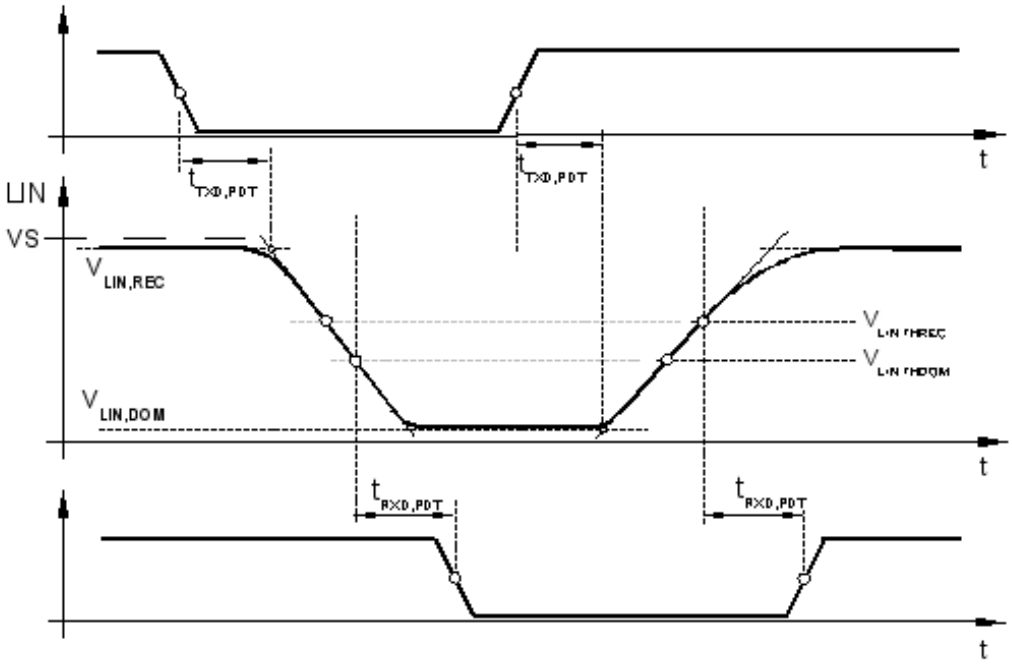


Fig. 4: LIN transceiver physical layer timing

6.3.2 LIN flash mode

In flash mode LIN bus slew rate control is disabled to support high baud rate for microcontroller flashing purposes via LIN bus. Flash mode is entered from standby mode by a rising edge on pin EN followed by a LOW pulse at pin TXD for t_{FMACK} within the time period t_{2AM}. The flash mode must be retriggered within the time out t_{FMTO} otherwise the mode is left to active mode.

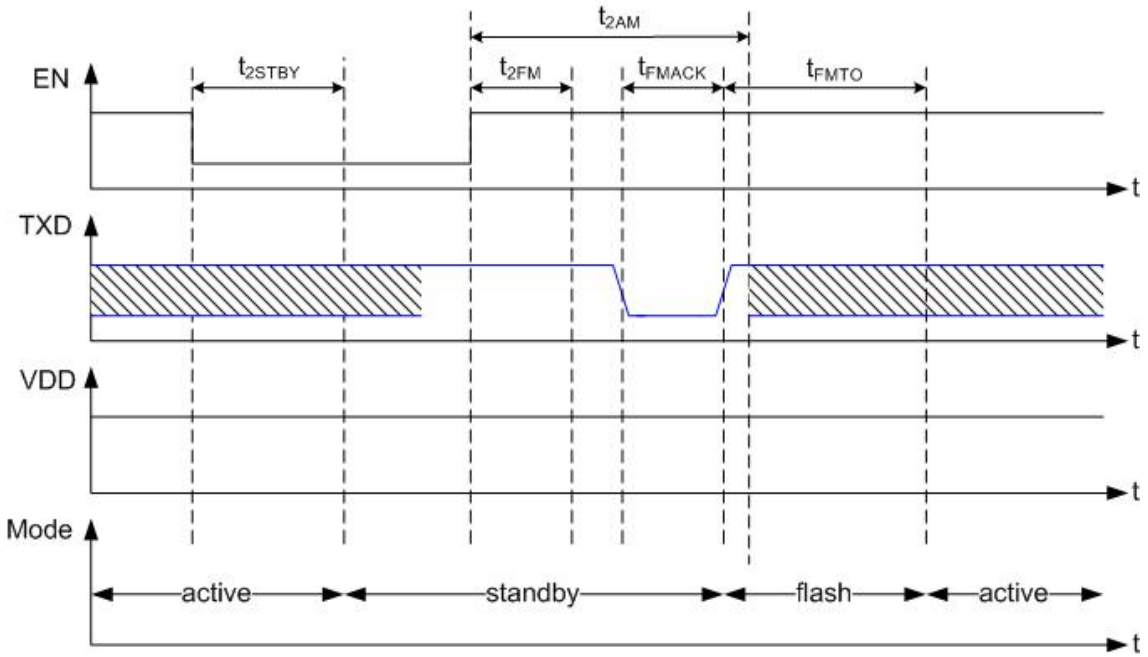


Fig. 5: Flash mode transition timing with TXD acknowledge pulse.

6.3.3 LIN TXD time out

In order to prevent the LIN bus from being permanent dominant in case of permanent LOW level at pin TXD a time-out is implemented. The LIN transmitter is disabled after $t_{TXD,TO}$. The timer is triggered by a negative edge on pin **TXD** and reset by a positive edge on pin **TXD**.

6.4 Wake-Up

In case the device is in sleep or standby mode there are 2 events to wake-up the device:

1. Local wake-up with low level at pin WAKE_N.
2. Remote wake-up by LIN

Any of these wake-up events changes the device mode from sleep mode to power-on mode.
If a remote or local wake-up occurs in standby mode the device remains in this mode and a wake-up event is signalized at pin RXD. A transition to sleep mode is prohibited.

6.4.1 Local wake-up

The device can be woken up from sleep mode via pin WAKE_N. Pulling pin WAKE_N below $V_{WAKE\_N,INL}$ level results in a local wake-up request. The wake-up event is falling edge triggered. This allows the device to enter sleep mode with pin WAKE_N pulled to low.

The pin WAKE_N is an high voltage input with pull up current source $I_{WAKE\_N,PU}$ and an input debounce filter. If the local wake-up is not used in application, the pin WAKE_N has to be connected to pin VS.

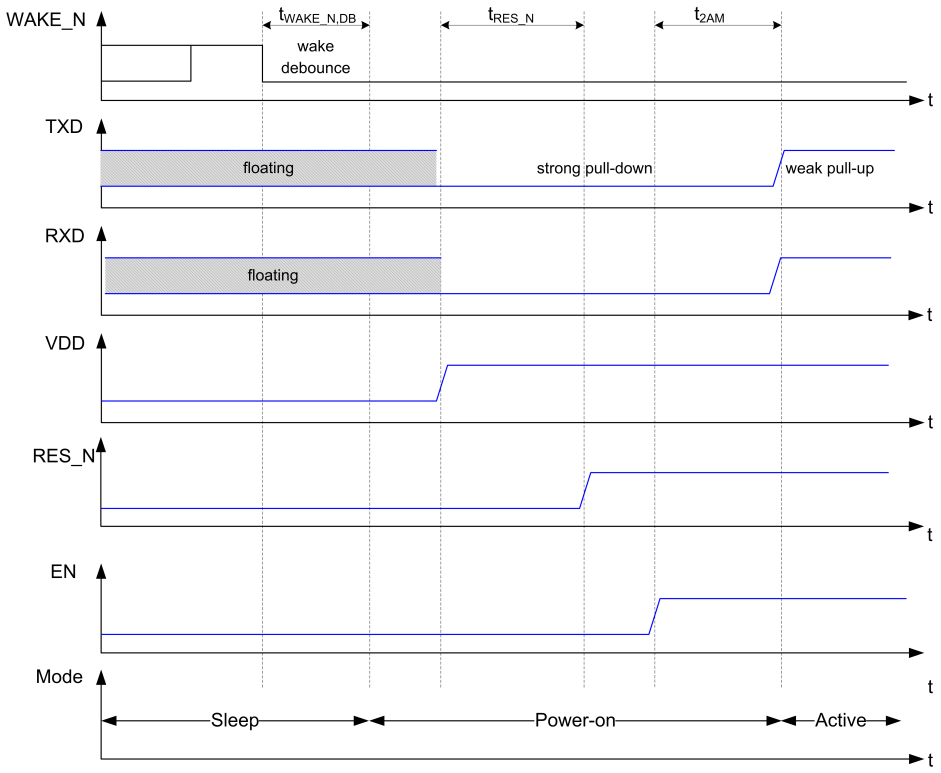


Fig. 6: Local wake-up in mode Sleep

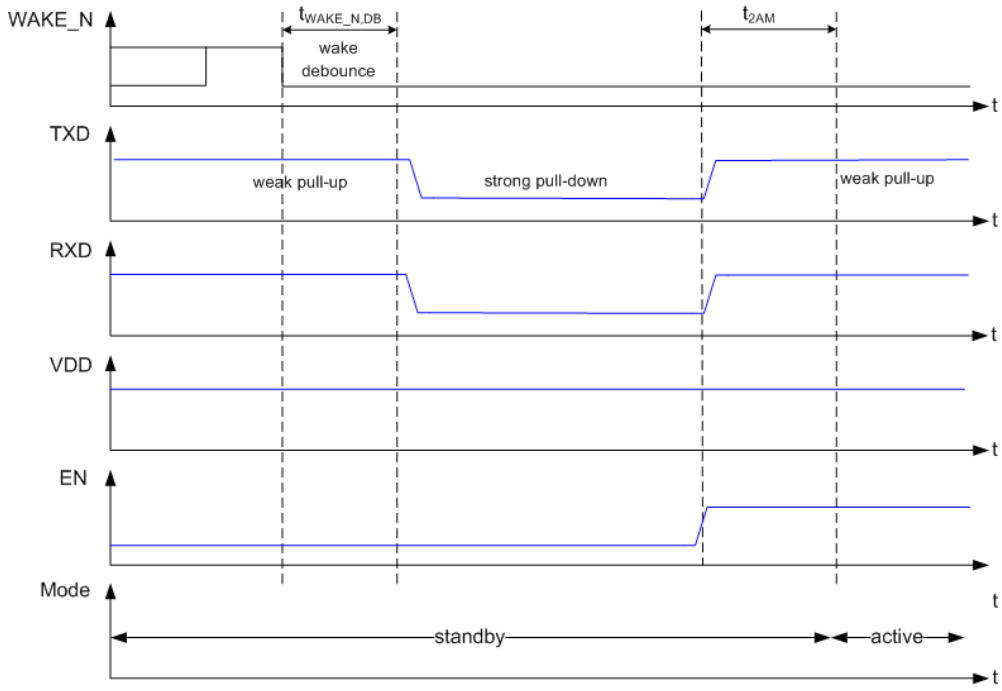


Fig. 7: Local wake-up in mode Standby

6.4.2 Remote wake-up

The device can be woke up remotely from sleep and standby mode via pin LIN.

A falling edge at the LIN pin followed by a dominant bus level $V_{LIN,DOM}$ maintained for a time period $t_{LIN,WU}$ with a following rising LIN edge result in a remote wake-up. The wake-up request is signalized to microcontroller by a low state at pin RXD.

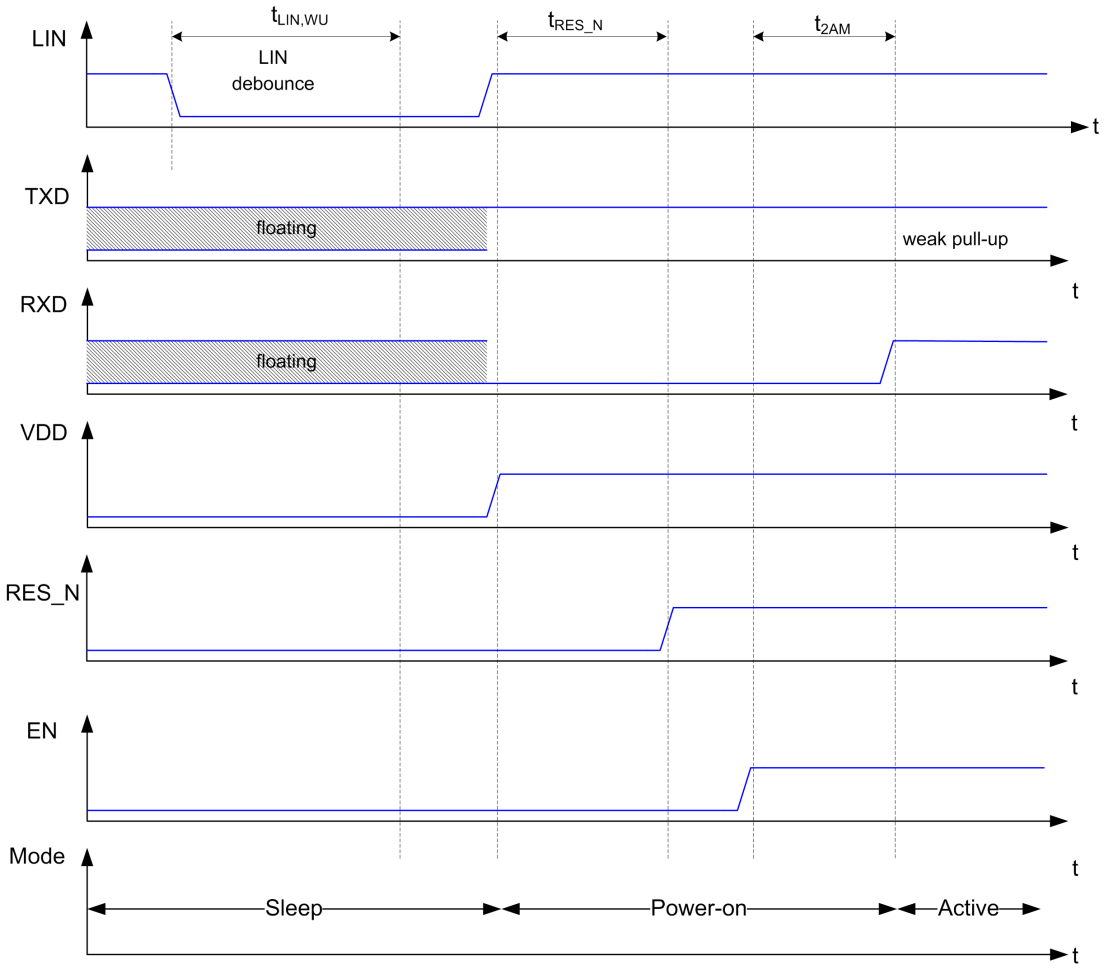


Fig. 8: Remote wake-up in mode Sleep

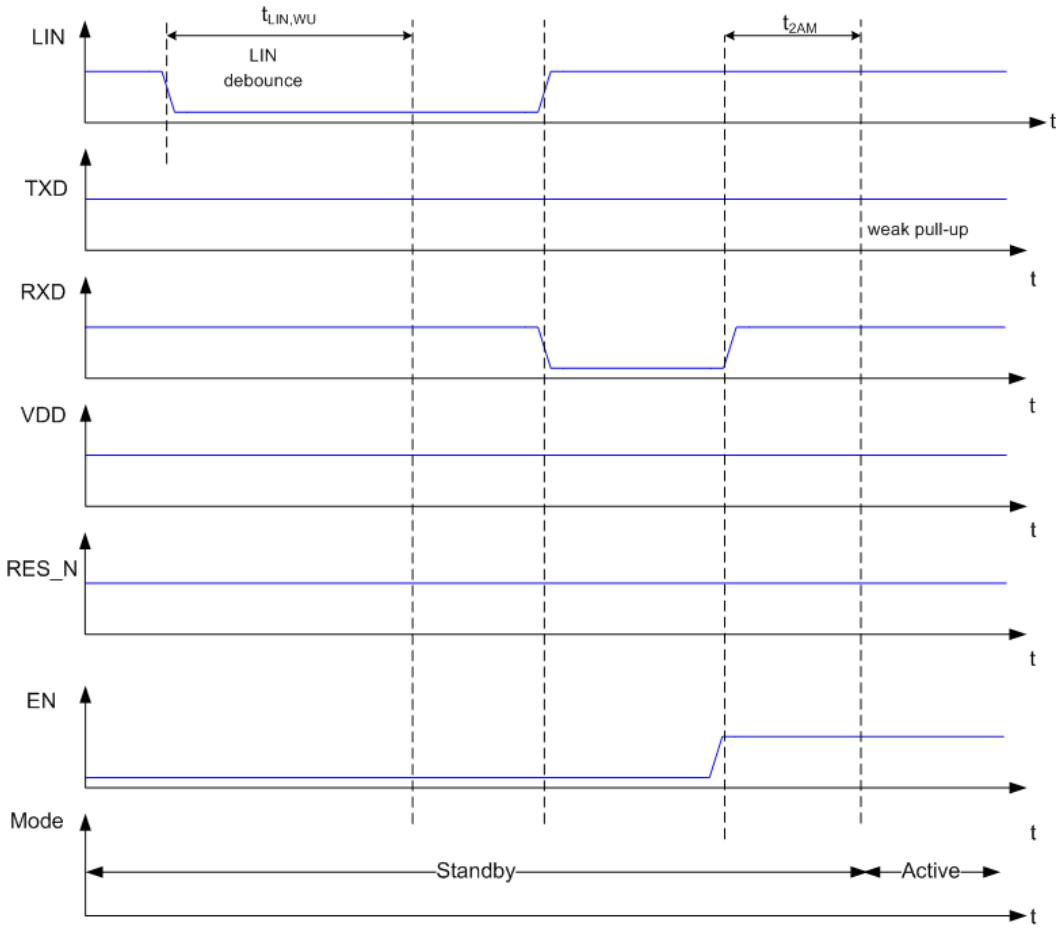


Fig. 9: Remote wake-up in mode Standby with flash mode option

6.4.3 Wake-up source signalization

The device latches the information of the wake-up source to distinguish beween a remote wake-up request via LIN bus and local wake-up via pin WAKE_N. The wake-up source can be read on pin TXD in the mode Standby and Power-on.
A HIGH level at pin TXD indicates a remote wake-up request (weak pull-up at pin TXD) and a LOW level indicates a local wake-up request (strong pull-down at pin TXD).

6.4.4 Wake-up flag reset

The wake-up request flag and the wake-up source flag are reset after entering active mode. The wake-up source signal at TXD and RXD is interrupted while pin EN is set to high in order to check flash mode request at TXD.

6.5 Watchdog

The watchdog has to be triggered by high pulses at WDIN in the open window time $t_{WD,OW}$. A correct WD-trigger command in an open window starts the next closed window. Any WD-trigger command in the closed window resets the watchdog and a reset will be activated on pin RES_N for $t_{WD,RES}$. The watchdog oscillator clock has a clock period of $t_{WD,OSCXX}$.

There is an enlarged first open window after a high transition at RES_N. The first WDIN trigger pulse is allowed to appear latest at $t_{WD,FOW}$.

The watchog is disabled in standby- and sleep mode. The watchdog starts with first open window after reentering active- or power-on mode.

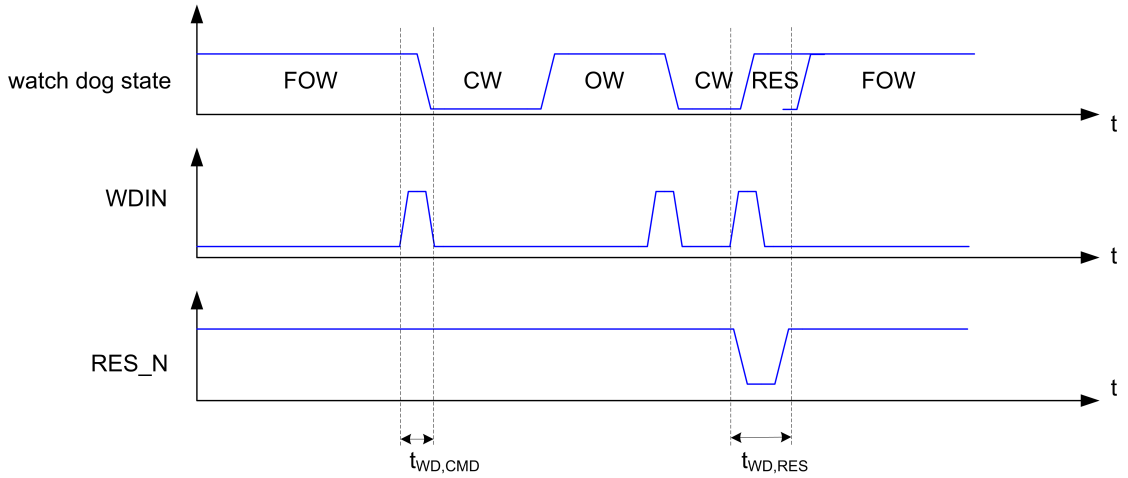


Fig. 10: Watchdowg triggger in closed window (CW)

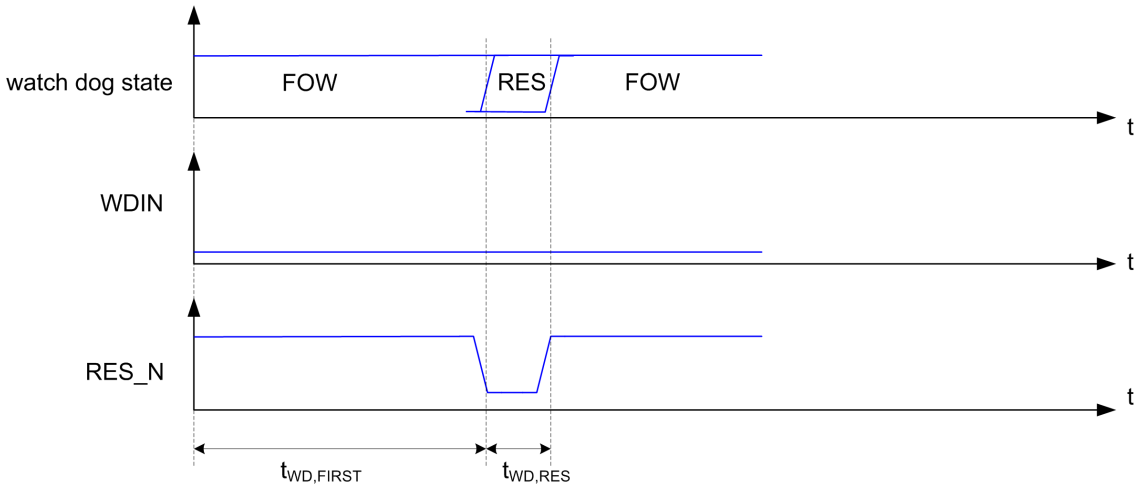


Fig. 11: No watchdowg trigger in first open window (FOW)

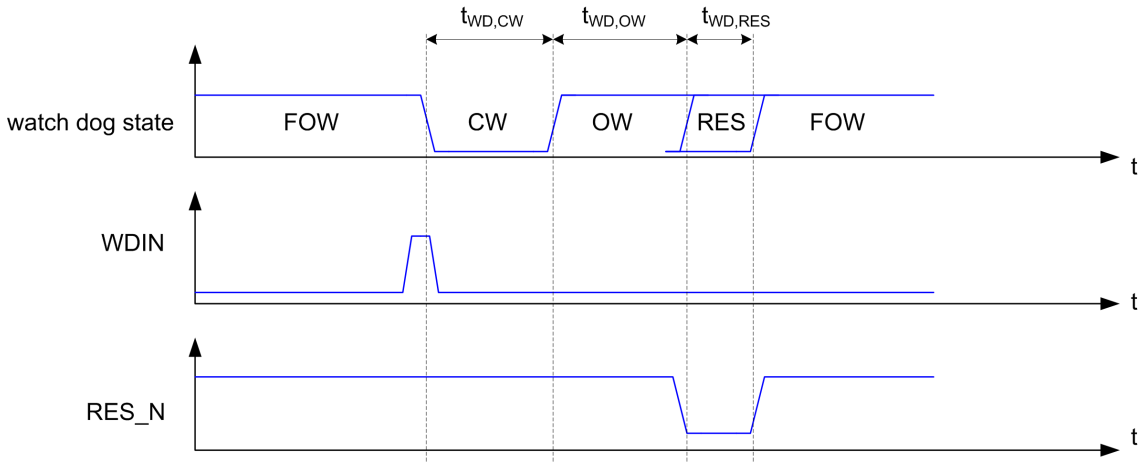


Fig. 12: No watchdowg trigger in open window (OW)

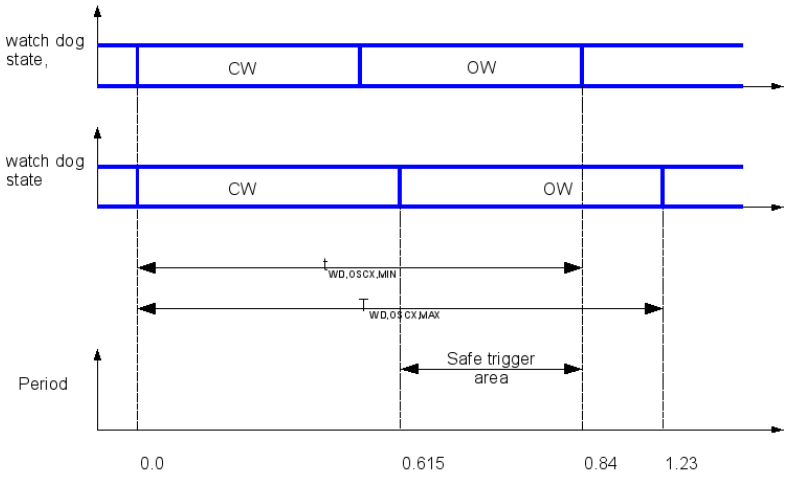


Fig. 13: Watchdog safe trigger area

6.5.1 Watchdog cycle time configuration

The watchdog cycle time can be configured via the external resistor at pin WDOSC. The typical watchdog oscillator period $t_{WD,OSC}$ is defined by the external resistance $R_{WD,OSC}$ by:

$$t_{WD,OSC} = R_{WD,OSC} \cdot \frac{\mu s}{k\Omega}$$

$R_{WD,OSC}$ / kΩ	$t_{WD,OSC}$ / µ s	$t_{WD,CYC}$ / ms
10	10	10.24
22	22	22.528
47	47	48.128
100	100	102.4

Table 3: Typical watchdog configuration examples

6.5.2 Watchdog debug mode

For debugging purposes the watchdog can be stopped running by pulling pin WDDM to HIGH. In this case the watchdog timer stopps and the actual state remains. After setting pin WDDM to low level the watchdog keeps on running.

6.6 VBAT voltage divider

The integrated reverse polarity protected 6:1 voltage divider can be connected to the battery supply to measure the supply voltage with fast response time. To limit the output voltage in case of VBAT overvoltage a clamping to the microcontroller supply voltage is integrated.

The voltage divider is activated by the digital pin DIV_ON. The divided input voltage is available at pin PV. In sleep mode the voltage divide is disabled to reduce sleep current consumption.

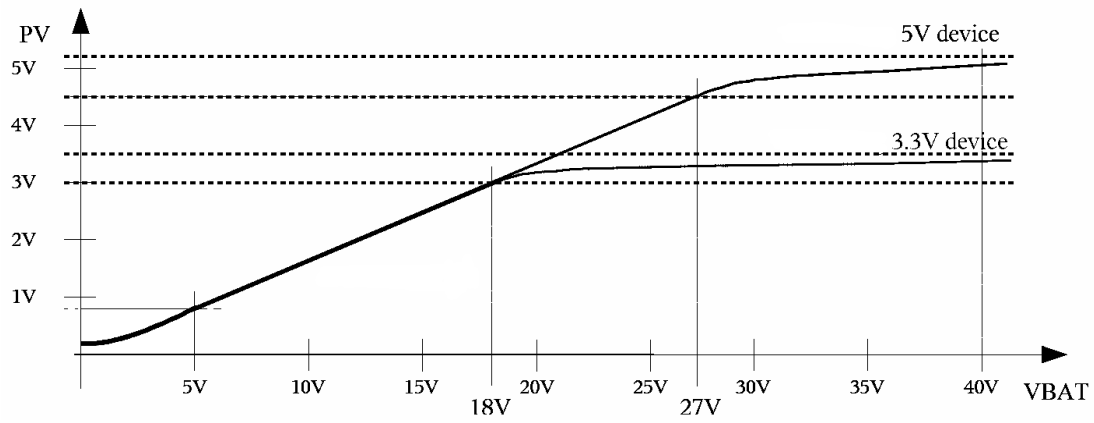


Fig. 14: Typical characteristic of the voltage divider

6.7 Fail Safe Behaviour

6.7.1 Reset parameters

The regulator is switched on if the supply input voltage VS exceeds $V_{S,POR}$ threshold and is switched off if the voltage at pin VS falls below $V_{S,PD}$ threshold. The slope of the falling edge after VDD regulator shutdown at pin VDD depends on the external buffer capacitance and the load current. The device enters power-off mode. The device powers up again if the battery voltage exceeds $V_{S,POR}$ level again.

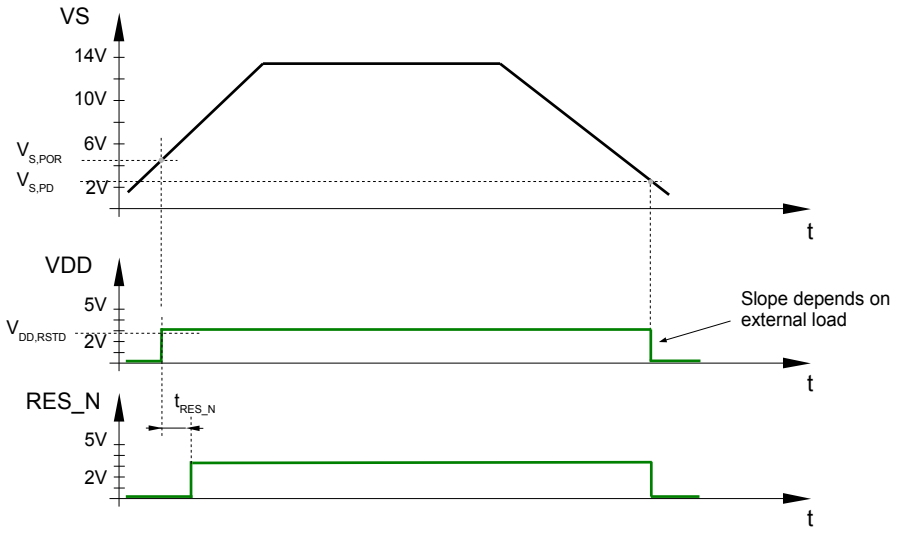


Fig. 15: Power up and power down behaviour in 3.3 V mode

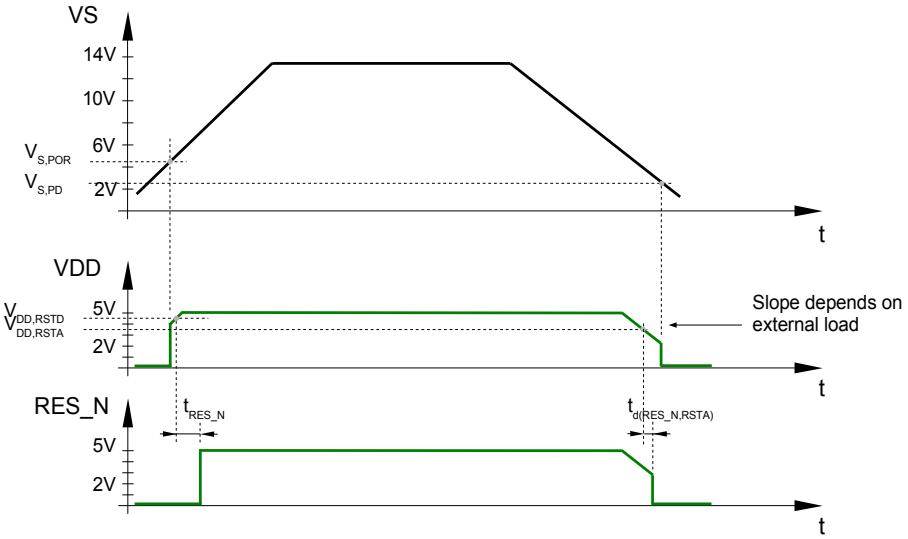


Fig. 16: Power up and down behaviour in 5 V mode

6.7.2 Digital input pullup / pulldown

The digital input pins have internal pullup or pulldown sources for fail-safe operating conditions according to the following table:

Pin	*Termination*	*Reason*
WDDM	weak pull down	set WD active in case of floating pin WDDM
TXD	weak pull up	set TXD input to defined level in case of floating pin TXD
EN	weak pull down	force SBC in Sleep mode in case of floating pin EN
WDIN	weak pull down	terminates WD trigger input in case of floating pin WDIN; results in activating RES_N

Table 4: Fail-Save Pin-Termination Table.

6.7.3 Thermal shutdown

The LIN-SBC is protected against thermal stress. In case the junction temperature exceeds the shutdown temperature T_{SHDN}, the internal SBC thermal shutdown flag is set. The flag is reset in case the junction temerature cools down by T_{HYST} .

Depending on the cause for the over temperature (voltage regulator or LIN transmitter) the SBC behaves different. In any case it shut down the detected heat source to reduce power dissipation of the SBC.

6.7.4 LIN over current protection

The output current of the LIN transmitter is limited to $I_{LIN,LIM}$ in order to protect the transmitter against short circuit to pin VS .

In case the SBC thermal shutdown flag is caused by the LIN transceiver the transmitter is disabled and the LIN over temperature flag is set.

The over temperature flag is reset and the LIN transmitter is enabled in case the junction temerature cools down by T_{HYST} . The LIN shut down does not result in any state change.

6.7.5 Voltage regulator over current protection

In case of shorts at pin VDD the output current of the voltage regulator is limited to $I_{DD,LIM}$. In order to limit power dissipation of the device the voltage regulator is shut down if the thermal shutdown flag is caused by by the voltage regulator. A debounce filter of $t_{DD,SHDN}$ is implemented.

The voltage regulator is switched on again in case the junction temperature colls down by T_{HYST} independently of pin EN. The VDD shut down causes a mode change, if the pin VDD voltage drops below the VDD reset threshold level $V_{DD,RSTAXX}$. In this case the device enters power-on mode.

6.7.6 LIN loss of ground

In case of battery voltage loss (pin VS) and ground loss (pin GND) reverse current from the LIN bus line is limited.

6.7.7 Microcontroller reset

In case the voltage at pin VDD drops below the reset threshold $V_{DD,RSTAXX}$ the SBC reset pin RES_N is activated and pulled down to GND. The reset pin RES_N is released after t_{RES_N} if the VDD voltage exceeds the reset deassert level $V_{DD,RSTDXX}$.

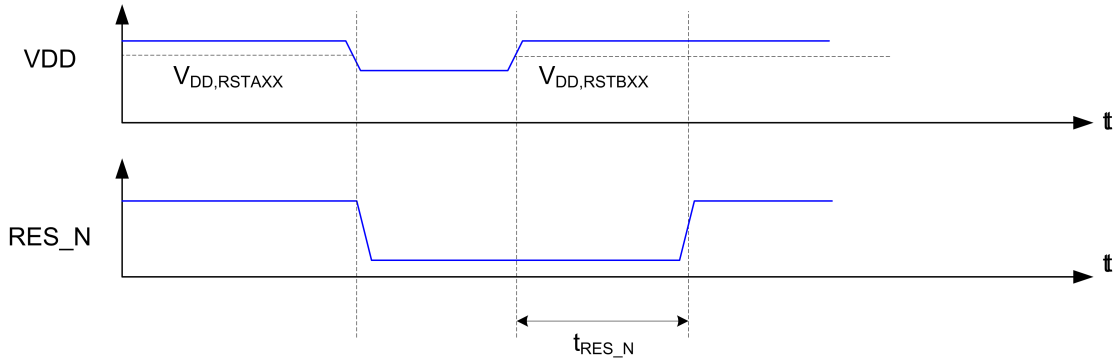


Fig. 17: RES_N in case of VDD UV events

WARNING – Life Support Applications Policy

ELMOS Semiconductor AG is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing ELMOS Semiconductor AG products, to observe standards of safety, and to avoid situations in which malfunction or failure of an ELMOS Semiconductor AG Product could cause loss of human life, body injury or damage to property. In development your designs, please ensure that ELMOS Semiconductor AG products are used within specified operating ranges as set forth in the most recent product specifications.

General Disclaimer

Information furnished by ELMOS Semiconductor AG is believed to be accurate and reliable. However, no responsibility is assumed by ELMOS Semiconductor AG for its use, nor for any infringements of patents or other rights of third parties, which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of ELMOS Semiconductor AG. ELMOS Semiconductor AG reserves the right to make changes to this document or the products contained therein without prior notice, to improve performance, reliability, or manufacturability .

Application Disclaimer

Circuit diagrams may contain components not manufactured by ELMOS Semiconductor AG, which are included as means of illustrating typical applications. Consequently, complete information sufficient for construction purposes is not necessarily given. The information in the application examples has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of ELMOS Semiconductor AG or others.

Contact Information

Headquarters
ELMOS Semiconductor AG
Heinrich-Hertz-Str. 1 • D-44227 Dortmund (Germany) ✆ +492317549100 ✉: sales@elmos.de 🌍: www.elmos.de

Regional Sales and Application Support Office Munich
ELMOS Semiconductor AG
Am Geflügelhof 12 • 85716 Unterschleißheim/Eching ✆ +49893183700

Sales Office France
ELMOS FRANCE SAS
9/11 allée de l'Arche • La Défense • 92671 Courbevoie cedex (France) ✆ +33149971591

Sales and Application Support Office North America
ELMOS NA. Inc.
32255 Northwestern Highway, Suite 45 • Farmington Hills, MI 48334 ✆ +12488653200

Sales and Application Support Office Korea and Japan
ELMOS Korea
Dongbu Root building, 16-2, Suite 509, • Sunae-dong, Bundang-gu,
Seongnam-shi, Kyonggi-do (Korea) ✆ +82317141131

Sales and Application Support Office China
ELMOS Semiconductor Technology (Shanghai) Co., Ltd.
57-01E, Lampl Business Centre, 57F, The Exchange • 1486 Nanjing W Rd.
(299 Tongren Rd) • JingAn Shanghai • P.R.China 200040 ✆ +862161717358

Sales and Application Support Office Singapore
ELMOS Semiconductor Singapore Pte Ltd.
60 Alexandra Terrace • #09-31 The Comtech • Singapore 118502 ✆ +6566351141