Document Number: MC33663
Rev. 1.0, 7/2012

RoHS

LIN 2.1 / SAEJ2602-2 Dual LIN Physical Layer

33663

DUAL LIN TRANSCEIVER

EF SUFFIX (PB-FREE)
98ASB42565B
14-PIN SOICN

The local interconnect network (LIN) is a serial communication protocol designed to support automotive networks in conjunction with controller area network (CAN). As the lowest level of a hierarchical network, LIN enables cost-effective communication with sensors and actuators when all the features of CAN are not required.

The 33663 product line integrates two physical layer LIN bus dedicated to automotive LIN sub-bus applications. The MC33663LEF and MC33663SEF devices offer normal baud rate (20 kbps) and the MC33663JEF slow baud rate (10 kbps). Both devices integrate fast baud rate (above 100 kbps) for test and programming modes. They present excellent electromagnetic compatibility (EMC) and radiated emission performance, electrostatic discharge (ESD) robustness and safe behavior, in the event of LIN bus short-to-ground or LIN bus leakage during low-power mode.

ORDERING INFORMATION		
Device (add an R2 suffix for Tape and reel orders)	**Temperature Range (T_A)**	**Package**
MC33663ALEF	-40 to 125°C	14 SOICN
MC33663AJEF		
MC33663ASEF		

Features

- Operational from V_{SUP} 7.0 to 18 V DC, functional up to 27 V DC, and handles 40 V during load dump
- Compatible with LIN protocol specification 2.1, and SAEJ2602-2
- Very high immunity against electromagnetic interference
- Low standby current in Sleep mode
- Over-temperature protection
- Permanent dominant state detection
- Fast baud rate mode selection reported by RXD
- Active bus waveshaping offering excellent radiated emission performance
- Sustains ±15.0 kV ESD IEC6100-4-2 on LIN BUS and VSUP pins
- 5.0 and 3.3 V compatible digital inputs without any external components required

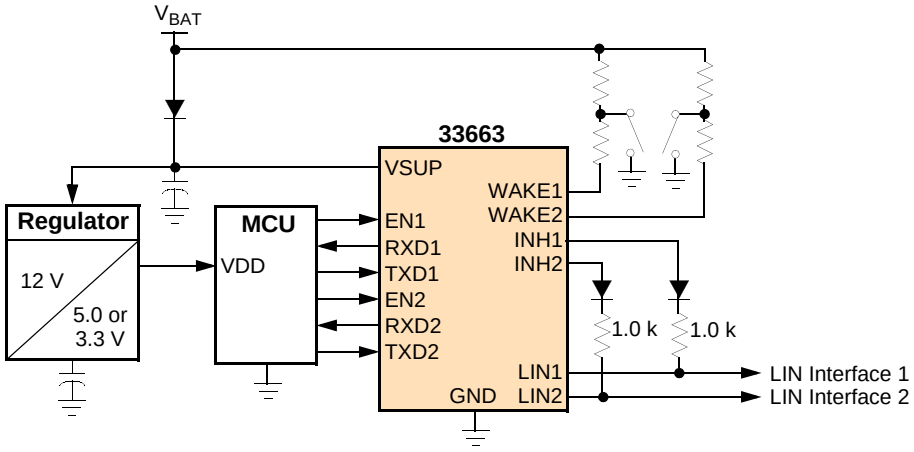


Figure 1. 33663 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

freescale™

DEVICE VARIATIONS

Table 1. Device Variations

Freescale Part No. (Add an R2 suffix for Tape and reel orders)	Maximum Baud Rate	Temperature Range (T_A)	Package
MC33663ALEF	20 kbps	-40 to 125 °C	14 SOICN
MC33663ASEF	20 kbps with restricted limits for transmitter and receiver symmetry		
MC33663AJEF	10 kbps		

INTERNAL BLOCK DIAGRAM

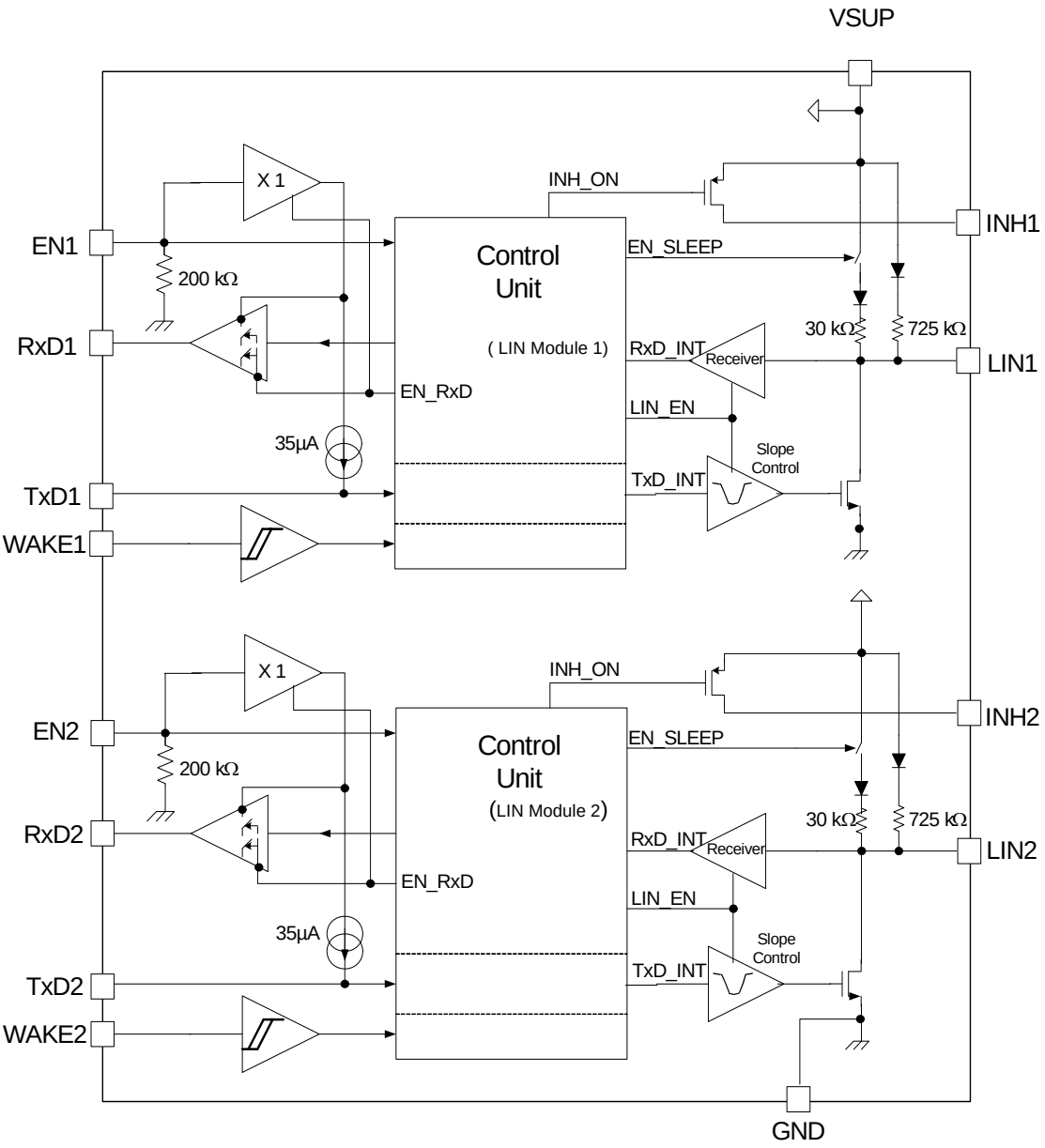


Figure 2. 33663 Simplified Internal Block Diagram

PIN CONNECTIONS

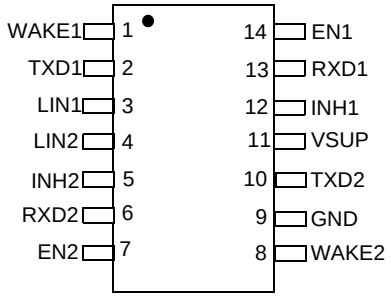


Figure 3. 33663 14-SOIC Pin Connections

Table 2. 33663 Pin Definitions

Pin	Pin Name	Formal Name	Definition
1	WAKE1	Wake Input	This pin is a high-voltage input used to wake-up the LIN1 from Sleep mode.
2	TXD1	Data Input	This pin is the transmitter input of the LIN1 interface which controls the state of the bus output.
3	LIN1	LIN Bus	This bidirectional pin represents the LIN1 single-wire bus transmitter and receiver.
4	LIN2	LIN Bus	This bidirectional pin represents the LIN2 single-wire bus transmitter and receiver.
5	INH2	Inhibit Output	This pin can have two main functions: controlling an external switchable voltage regulator having an inhibit input, or driving an external bus resistor connected to LIN2 in the master node application.
6	RXD2	Data Output	This pin is the receiver output of the LIN2 interface, which reports the state of the bus voltage to the MCU interface.
7	EN2	Enable Control	This pin controls the operation mode of the LIN2 interface.
8	WAKE2	Wake Input	This pin is a high-voltage input used to wake-up the LIN2 device from Sleep mode.
9	GND	Ground	This pin is the device ground pin.
10	TXD2	Data Input	This pin is the transmitter input of the LIN2 interface, which controls the state of the bus output.
11	VSUP	Power Supply	This pin is device battery level power supply.
12	INH1	Inhibit Output	This pin can have two main functions: controlling an external switchable voltage regulator having an inhibit input, or driving an external bus resistor connected to LIN1 in the master node application.
13	RXD1	Data Output	This pin is the receiver output of the LIN1 interface, which reports the state of the bus voltage to the MCU interface.
14	EN1	Enable Control	This pin controls the operation mode of the LIN1 interface.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage (VSUP)			V
Normal Operation (DC)	$V_{SUP(SS)}$	-0.3 to 27	
Transient input voltage with external component (according to ISO7637-2 & ISO7637-3 & "Hardware Requirements for LIN, CAN, and Flexray Interfaces in Automotive Applications" specification Rev. 1.1/December 2nd, 2009) (See Table 4 and Figure 4)			
- Pulse 1 (test up to the limit for Damage - Class A[1])	$V_{SUP(S1)}$	-100	
- Pulse 2a (test up to the limit for Damage - Class A[1])	$V_{SUP(S2A)}$	+75	
- Pulse 3a (test up to the limit for Damage - Class A[1])	$V_{SUP(S3A)}$	-150	
- Pulse 3b (test up to the limit for Damage - Class A[1])	$V_{SUP(S3B)}$	+100	
- Pulse 5b (Class A)[1]	$V_{SUP(S5B)}$	-0.3 to 40	
Logic Voltage ($RXD_{1,2}$, $TXD_{1,2}$, $EN_{1,2}$ Pins)	V_{LOG}	-0.3 to 5.5	V
WAKE (V_{WAKE1},V_{WAKE2})			V
Normal Operation with in series 2*18 kΩ resistor (DC)	$V_{WAKE(SS)}$	-27 to 40	
Transient input voltage with external component (according to ISO7637-2 & ISO7637-3 & "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications" specification Rev1.1 / December 2nd, 2009) (See Table 4 and Figure 5)			
- Pulse 1 (test up to the limit for Damage - Class D[2])	$V_{WAKE(S1)}$	-100	
- Pulse 2a (test up to the limit for Damage - Class D[2])	$V_{WAKE(S2A)}$	+75	
- Pulse 3a (test up to the limit for Damage - Class D[2])	$V_{WAKE(S3A)}$	-150	
- Pulse 3b (test up to the limit for Damage - Class D[2])	$V_{WAKE(S3B)}$	+100	
LIN Bus Voltage (V_{LIN1}, V_{LIN2})			V
Normal Operation (DC)	$V_{LIN(SS)}$	-27 to 40	
Transient (Coupled Through 1.0 nF Capacitor) (according to ISO7637-2 & ISO7637-3) (See Table 4 and Figure 6)			
- Pulse 1 (test up to the limit for Damage - Class D[2])	$V_{LIN(S1)}$	-100	
- Pulse 2a (test up to the limit for Damage - Class D[2])	$V_{LIN(S2A)}$	+75	
- Pulse 3a (test up to the limit for Damage - Class D[2])	$V_{LIN(S3A)}$	-150	
- Pulse 3b (test up to the limit for Damage - Class D[2])	$V_{LIN(S3B)}$	+100	

Notes

1. Class A: All functions of a device/system perform as designed during and after exposure to disturbance.
2. Class D: At least one function of the Transceiver stops working properly during the test and will return into proper operation automatically when the exposure to the disturbance has ended. No physical damage of the IC occurs.

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
INH Voltage/Current (V_{INH1}, V_{INH2})			V
DC Voltage	V_{INH}	-0.3 to V_{SUP} + 0.3	
Transient (Coupled Through 1.0 nF Capacitor, according to ISO7637-2 & ISO7637-3 & "Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications" specification Rev1.1 / December 2nd, 2009) (See Table 4 and Figure 7)			
- Pulse 1 (test up to the limit for Damage - Class D[3])	$V_{INH(S1)}$	-100	
- Pulse 2a (test up to the limit for Damage - Class D[3])	$V_{INH(S2a)}$	+75	
- Pulse 3a (test up to the limit for Damage - Class D[3])	$V_{INH(S3a)}$	-150	
- Pulse 3b (test up to the limit for Damage - Class D[3])	$V_{INH(S3b)}$	+100	

Notes

3. Class D: At least one function of the Transceiver stops working properly during the test and will return into proper operation automatically when the exposure to the disturbance has ended. No physical damage of the IC occurs.

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
ESD Capability			V
AECQ100			
Human Body Model - JESD22/A114 (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω)			
LIN1, LIN2 pins versus GND	V_{ESD1-1}	±10.0 k	
WAKE1, WAKE2 pins versus GND	V_{ESD1-2}	±8.0 k	
INH1, INH2 pins versus GND	V_{ESD1-3}	±8.0 k	
All other Pins	V_{ESD1-4}	±4.0 k	
Charge Device Model - JESD22/C101 (C_{ZAP} = 4.0 pF)			
Corner pins (Pins 1, 7, 8 and 14)	V_{ESD2-1}	±750	
All other pins (Pins 2-6, 9-13)	V_{ESD2-2}	±750	
Machine Model - JESD22/A115 (C_{ZAP} = 220 pF, R_{ZAP} = 0 Ω)			
All pins	V_{ESD3-1}	±200	
According to “Hardware Requirements for LIN, CAN and Flexray Interfaces in Automotive Applications” specification Rev1.1 / December 2nd, 2009 (C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω)			
Contact Discharge, Unpowered			
LIN1, LIN2 pins without capacitor	V_{ESD4-1}	±15 k	
LIN1, LIN2 pins with 220 pF capacitor	V_{ESD4-2}	±15 k	
VSUP (10 µF to ground)	V_{ESD4-3}	±25 k	
WAKE1, WAKE2 (2*18 kΩ serial resistor)	V_{ESD4-4}	±20 k	
LIN1, LIN2 pins with 220 pF capacitor and indirect ESD coupling (according to ISO10605 - Annex F)	V_{ESD4-5}	±15 k	
According to ISO10605 - Rev 2008 test specification (2.0 kΩ / 150 pF) - Unpowered - Contact discharge			
LIN1, LIN2 pins without capacitor	V_{ESD5-1}	±25 k	
LIN1, LIN2 pins with 220 pF capacitor	V_{ESD5-2}	±25 k	
VSUP (10 µF to ground)	V_{ESD5-3}	±25 k	
WAKE1, WAKE2 (2*18 kΩ serial resistor)	V_{ESD5-4}	±25 k	
(2.0 kΩ / 330 pF) - Powered - Contact discharge			
LIN1, LIN2 pins without capacitor	V_{ESD6-1}	±8 k	
LIN1, LIN2 pins with 220 pF capacitor	V_{ESD6-2}	±8 k	
VSUP (10 µF to ground)	V_{ESD6-3}	±25 k	
WAKE1, WAKE2 (2*18 kΩ serial resistor)	V_{ESD6-4}	±25 k	

Table 3. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

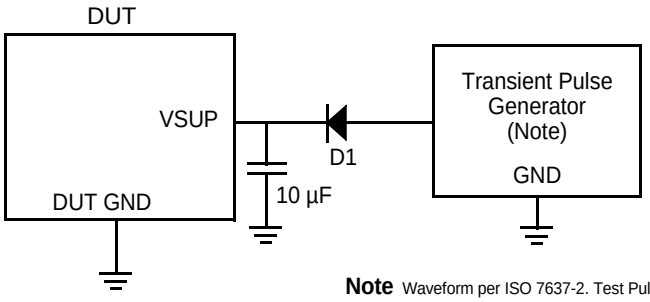
Ratings	Symbol	Value	Unit
Thermal Ratings			
Operating Temperature Ambient Junction	 T_A T_J	 -40 to 125 -40 to 150	°C
Storage Temperature	T_{STG}	-40 to 150	°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	150	°C/W
Peak package reflow temperature during reflow(4),(5)	T_{PPRT}	Note 5	°C
Thermal Shutdown Temperature	T_{SHUT}	150 to 200	°C
Thermal Shutdown Hysteresis Temperature	T_{HYST}	20	°C

Notes

4. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
5. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

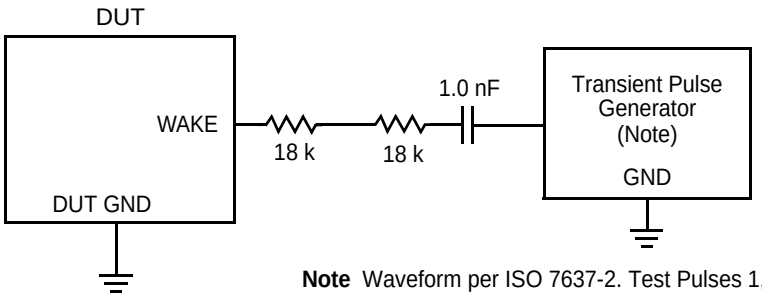
Table 4. Limits / Maximum test voltage for transient immunity tests

Test Pulse	V_S [V]	Pulse repetition frequency [Hz] ($1/T_1$)	Test duration [min]	R_i [Ω]	Remarks
1	-100	2	1 for function test 10 for damage test	10	t_2 = 0s
2a	+75	2		2	
3a	-150	10		50	
3b	+100	10		50	



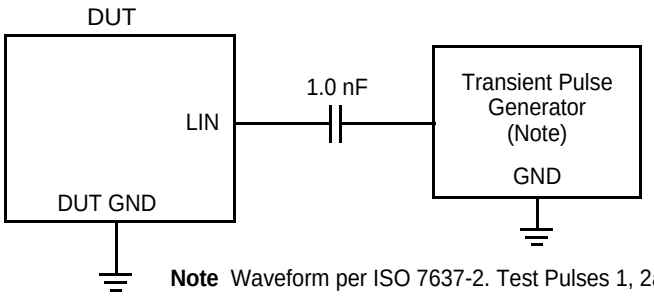
Note Waveform per ISO 7637-2. Test Pulses 1, 2a, 3a, 3b

Figure 4. Test Circuit for Transient Test Pulses (V_{SUP})



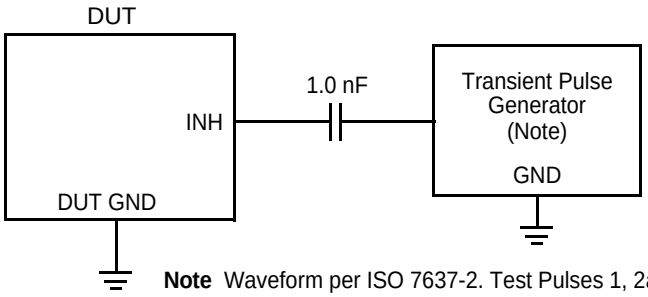
Note Waveform per ISO 7637-2. Test Pulses 1, 2a, 3a, 3b.

Figure 5. Test Circuit for Transient Test Pulses (WAKE1,WAKE2)



Note Waveform per ISO 7637-2. Test Pulses 1, 2a, 3a, 3b

Figure 6. Test Circuit for Transient Test Pulses (LIN1,LIN2)



Note Waveform per ISO 7637-2. Test Pulses 1, 2a, 3a, 3b.

Figure 7. Test Circuit for Transient Test Pulses (INH1,INH2)

STATIC ELECTRICAL CHARACTERISTICS

Table 5. Static Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
VSUP PIN (DEVICE POWER SUPPLY)					
Nominal Operating Voltage	V_{SUP}	7.0	13.5	18.0	V
Functional Operating Voltage[6]	V_{SUPOP}	6.7	–	27	V
Load Dump	V_{SUPLD}	–	–	40	V
Power-On Reset (POR) Threshold V_{SUP} Ramp Down and INH1, INH2 goes High to Low	V_{POR}	3.5	–	5.3	V
Power-On Reset (POR) Hysteresis	$V_{PORHYST}$	–	270	–	mV
V_{SUP} Under-voltage Threshold (positive and negative) Transmission disabled and LIN1,LIN2 bus goes in recessive	V_{UVL}, V_{UVH}	5.8	–	6.7	V
V_{SUP} Under-voltage Hysteresis (V_{UVL} - V_{UVH})	V_{UVHYST}	–	130	–	mV
Supply Current LIN1 and LIN2 in Sleep Mode V_{SUP} ≤ 13.5 V, Recessive State 13.5 V < V_{SUP} < 27 V V_{SUP} ≤ 13.5 V, Shorted to GND	 I_{S1} I_{S2} I_{S3}	 – – –	 12.0 – 48	 22 36 140	μA
Supply Current LIN1 Normal Mode - LIN2 Sleep Mode (and vice versa) Bus_1 Recessive, BUS_2 Sleep, Excluding INH1,INH2 OR (Bus_2 Recessive, BUS_1 Sleep, Excluding INH1,INH2) Bus_1 Dominant, BUS_2 Sleep, Excluding INH1,INH2 OR (Bus_2 Dominant, BUS_1 Sleep, Excluding INH1,INH2)	 $I_{S\_N\_REC1,2}$ $I_{S\_N\_DOM1,2}$	 – –	 4.0 6.0	 5.0 8.0	mA
Supply Current when LIN1 and LIN2 are in Normal or Slow or Fast Mode Bus_1 Recessive, Bus_2 Recessive, Excluding INH1,INH2 Output Current Bus_1 Recessive, Bus_2 Dominant, Excluding INH1,INH2 Output Current Bus_1 Dominant, Bus_2 Recessive, Excluding INH1,INH2 Output Current Bus_1 Dominant, Bus_2 Dominant, Excluding INH1,INH2 Output Current	 $I_{S(REC1,REC2)}$ $I_{S(REC1,DOM2)}$ $I_{S(DOM1,REC2)}$ $I_{S(DOM1,DOM2)}$	 – – – –	 8.0 12.0 12.0 12.0	 9.0 13.0 13.0 16.0	mA
RXD1, RXD2 OUTPUT PINS (LOGIC)					
Low Level Output Voltage I_{IN} ≤ 1.5 mA	V_{OL}	0.0	–	0.9	V
High Level Output Voltage V_{EN} = 5.0 V, I_{OUT} ≤ 250 μA V_{EN} = 3.3 V, I_{OUT} ≤ 250 μA	V_{OH}	4.25 3.0	– –	5.25 3.5	V

Notes

6. Device is functional. All features are operating. Electrical parameters are not guaranteed.

Table 5. Static Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
TXD1, TXD2 INPUT PINS (LOGIC)					
Low Level Input Voltage	V_{IL}	–	–	0.8	V
High Level Input Voltage	V_{IH}	2.0	–	–	V
Input Threshold Voltage Hysteresis	V_{INHYST}	100	300	600	mV
Pull-up Current Source V_{EN} = 5.0 V, 1.0 V < V_{TXD} < 3.5 V	I_{PU}	-60	-35	-20	µA
EN1, EN2 INPUT PINS (LOGIC)					
Low Level Input Voltage	V_{IL}	–	–	0.8	V
High Level Input Voltage	V_{IH}	2.0	–	–	V
Input Voltage Threshold Hysteresis	V_{INHYST}	100	400	600	mV
Pull-down Resistor	R_{PD}	100	230	350	kohm
LIN PHYSICAL LAYER - TRANSCEIVER LIN (LIN1, LIN2)[7]					
Operating Voltage Range[8]	V_{BAT}	8.0	–	18	V
Supply Voltage Range	V_{SUP}	7.0	–	18	V
Voltage Range (within which the device is not destroyed)	$V_{SUP\_NON\_OP}$	-0.3	–	40	V
Current Limitation for Driver Dominant State Driver ON, V_{BUS} = 18 V	I_{BUS_LIM}	40	90	200	mA
Input Leakage Current at the Receiver Driver off; V_{BUS} = 0 V; V_{BAT} = 12 V	$I_{BUS\_PAS\_DOM}$	-1.0	–	–	mA
Leakage Output Current to GND Driver Off; 8.0 V < V_{BAT} < 18 V; 8.0 V < V_{BUS} < 18 V; V_{BUS} ≥ V_{BAT}; V_{BUS} ≥ V_{SUP}	$I_{BUS\_PAS\_REC}$	–	–	20	µA
Control Unit Disconnected from Ground[9] GND_{DEVICE} = V_{SUP}; V_{BAT} = 12 V; 0 < V_{BUS} < 18 V	$I_{BUS\_NO\_GND}$	-1.0	–	1.0	mA
V_{BAT} Disconnected; V_{SUP_DEVICE} = GND; 0 V < V_{BUS} < 18 V[10]	I_{BUSNO_BAT}	–	–	10	µA
Receiver Dominant State[11]	V_{BUSDOM}	–	–	0.4	V_{SUP}
Receiver Recessive State[12]	V_{BUSREC}	0.6	–	–	V_{SUP}

Notes

7. Parameters guaranteed for 7.0 V ≤ V_{SUP} ≤ 18 V.
8. Voltage range at the battery level, including the reverse battery diode.
9. Loss of local ground must not affect communication in the residual network.
10. Node has to sustain the current that can flow under this condition. The bus must remain operational under this condition.
11. LIN threshold for a dominant state.
12. LIN threshold for a recessive state.

Table 5. Static Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Receiver Threshold Center (V_{TH_DOM} + V_{TH_REC})/2	V_{BUS_CNT}	0.475	0.5	0.525	V_{SUP}
Receiver Threshold Hysteresis (V_{TH_REC} - V_{TH_DOM})	V_{HYS}	–	–	0.175	V_{SUP}
LIN dominant level with 500 Ω, 680 Ω and 1.0 kΩ load on the LIN bus	V_{LINDOM_LEVEL}	–	–	0.3	V_{SUP}
V_{BAT}_SHIFT	V_{SHIFT_BAT}	0.0	–	11.5%	V_{BAT}
GND_SHIFT	V_{SHIFT_GND}	0.0	–	11.5%	V_{BAT}
LIN Wake-up Threshold from Sleep Mode	V_{BUSWU}	–	4.3	5.3	V
LIN Pull-up Resistor to V_{SUP}	R_{SLAVE}	20	30	60	kΩ
LIN internal capacitor(13)	C_{LIN}	–	–	30	pF
Over-temperature Shutdown(14)	T_{LINSD}	150	160	200	°C
Over-temperature Shutdown Hysteresis	T_{LINSD_HYS}	–	20	–	°C
INH1, INH2 OUTPUT PINS					
Driver ON Resistance (Normal Mode) I_{INH} = 50 mA	INH_{ON}	–	–	50	Ω
Current load capability From 7.0 V < V_{SUP} < 18 V	I_{INH_load}	–	–	30	mA
Leakage Current (Sleep Mode) 0 < V_{INH} < V_{SUP}	I_{LEAK}	-5.0	–	5.0	μA
Over-temperature Shutdown(15)	T_{INHSD}	150	160	200	°C
Over-temperature Shutdown Hysteresis	T_{INHSD_HYS}	–	20	–	°C

Notes

13. This parameter is guaranteed by process monitoring but not production tested.
14. When an over-temperature shutdown occurs, the LIN transmitter and receiver are in recessive state and INH switched off. This parameter is tested with a test mode on ATE and characterized at laboratory.
15. When an over-temperature shutdown occurs, the INH1, INH2 high side are switched off and the LIN transmitter and receiver are in recessive state. This parameter is tested with a test mode on ATE and characterized at laboratory.

Table 5. Static Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
WAKE1, WAKE2 INPUT PINS					
High to Low Detection Threshold (5.5 V < V_{SUP} < 7 V)	V_{WUHL1}	2.0	–	3.9	V
Low to High Detection Threshold (5.5 V < V_{SUP} < 7 V)	V_{WULH1}	2.4	–	4.3	V
Hysteresis (5.5 V < V_{SUP} < 7 V)	V_{WUHYS1}	0.2	–	0.8	V
High to Low Detection Threshold (7 V ≤ V_{SUP} < 27 V)	V_{WUHL2}	2.4	–	3.9	V
Low to High Detection Threshold (7 V ≤ V_{SUP} < 27 V)	V_{WULH2}	2.9	–	4.3	V
Hysteresis (7 V ≤ V_{SUP} < 27 V)	V_{WUHYS2}	0.2	–	0.8	V
Wake-up Input Current (V_{WAKE} < 27 V)	I_{WU}	–	–	5.0	µA

DYNAMIC ELECTRICAL CHARACTERISTIC

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN1, LIN2 PHYSICAL LAYER DRIVERS CHARACTERISTICS FOR NORMAL SLEW RATE - 20.0 KBIT/SEC ACCORDING TO LIN PHYSICAL LAYER SPECIFICATION(16)(17) 33663L AND 33663S DEVICE					
Duty Cycle 1: $TH_{REC(MAX)}$ = 0.744 * V_{SUP}; $TH_{DOM(MAX)}$ = 0.581 * V_{SUP} D1 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 50 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	D1	0.396	–	–	
Duty Cycle 2: $TH_{REC(MIN)}$ = 0.422 * V_{SUP}; $TH_{DOM(MIN)}$ = 0.284 * V_{SUP} D2 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 50 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	D2	–	–	0.581	
LIN1, LIN2 PHYSICAL LAYER DRIVERS CHARACTERISTICS FOR SLOW SLEW RATE - 10.4 KBIT/SEC ACCORDING TO LIN PHYSICAL LAYER SPECIFICATION(16)(18) 33663J DEVICE					
Duty Cycle 3: $TH_{REC(MAX)}$ = 0.778 * V_{SUP}; $TH_{DOM(MAX)}$ = 0.616 * V_{SUP} D3 = $t_{BUS\_REC(MIN)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.0 V ≤ V_{SUP} ≤ 18 V	D3	0.417	–	–	
Duty Cycle 4: $TH_{REC(MIN)}$ = 0.389 * V_{SUP}; $TH_{DOM(MIN)}$ = 0.251 * V_{SUP} D4 = $t_{BUS\_REC(MAX)}$/(2 x t_{BIT}), t_{BIT} = 96 µs, 7.6 V ≤ V_{SUP} ≤ 18 V	D4	–	–	0.590	
LIN1, LIN2 PHYSICAL LAYER - DRIVERS CHARACTERISTICS FOR FAST SLEW RATE					
Fast Bit Rate (Programming Mode)	BR_{FAST}	–	–	100	kBit/s
LIN1, LIN2 PHYSICAL LAYER - TRANSMITTER CHARACTERISTICS FOR NORMAL SLEW RATE - 20.0 KBIT/SEC(19) 33663S DEVICE					
Symmetry of Transmitter delay(20) t_{TRAN_SYM} = MAX ($t_{TRAN\_SYM60\%}$, $t_{TRAN\_SYM40\%}$) $t_{TRAN\_SYM60\%}$ = | $t_{TRAN\_PDF60\%}$ - $t_{TRAN\_PDR60\%}$ | $t_{TRAN\_SYM40\%}$ = | $t_{TRAN\_PDF40\%}$ - $t_{TRAN\_PDR40\%}$ |	t_{TRAN_SYM}	-7.25	–	7.25	µs

Notes

16. Bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 8.
17. See Figure 9
18. See Figure 10
19. V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 8.
20. See Figure 11

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN1, LIN2 PHYSICAL LAYER - RECEIVERS CHARACTERISTICS ACCORDING LIN2.1[21] 33663L AND 33663J AND 33663S					
Propagation Delay and Symmetry[22]					µs
Propagation Delay of Receiver, t_{REC_PD} = MAX (t_{REC_PDR}, t_{REC_PDF})	t_{REC_PD}	–	–	6.0	
Symmetry of Receiver Propagation Delay, t_{REC_PDF} - t_{REC_PDR}	t_{REC_SYM}	-2.0	–	2.0	
LIN1, LIN2 PHYSICAL LAYER: RECEIVER CHARACTERISTICS WITH TIGHTEN LIMITS[21] 33663S DEVICE					
Propagation Delay and Symmetry[22]					µs
Propagation Delay of Receiver, t_{REC_PD} = MAX (t_{REC_PDR}, t_{REC_PDF})	$t_{REC\_PD\_S}$	—	—	5.0	
Symmetry of Receiver Propagation Delay, t_{REC_PDF} - t_{REC_PDR}	$t_{REC\_SYM\_S}$	-1.3	—	1.3	
LIN1, LIN2 PHYSICAL LAYER: RECEIVER CHARACTERISTICS - LIN SLOPE 1V/ns[21] 33663S DEVICE					
Propagation Delay and Symmetry[23]					µs
Propagation Delay of Receiver, $t_{REC\_PD\_FAST}$= MAX ($t_{REC\_PDR\_FAST}$, $t_{REC\_PDF\_FAST}$)	$t_{REC\_PD\_FAST}$	—	—	6.0	
Symmetry of Receiver Propagation Delay, $t_{REC\_PDF\_FAST}$ - $t_{REC\_PDR\_FAST}$	$t_{REC\_SYM\_FAST}$	-1.3	—	1.3	
SLEEP MODE AND WAKE-UP TIMINGS					
Sleep Mode Delay Time[24] after EN High to Low to INH High to Low with 100µA load on INH	t_{SD}	50	—	91	µs
WAKE-UP TIMINGS					
Bus Wake-up Deglitcher (Sleep Mode) [25]	t_{WUF}	40	70	100	µs
EN Wake-up Deglitcher [26] EN High to INH Low to High	t_{LWUE}	—	—	15	µs
Wake-up Deglitcher [27] Wake state change to INH Low to High	t_{WF}	10	48	70	µs

Notes

21. V_{SUP} from 7.0 to 18 V, bus load R_{BUS} and C_{BUS} 1.0 nF / 1.0 kΩ, 6.8 nF / 660 Ω, 10 nF / 500 Ω. Measurement thresholds: 50% of TXD signal to LIN signal threshold defined at each parameter. See Figure 8.
22. See Figure 12
23. See Figure 13
24. See Figures 22 and 23
25. See Figures 15 and 17
26. See Figures 14, 18, 22, and 23
27. See Figures 16, 22, and 23

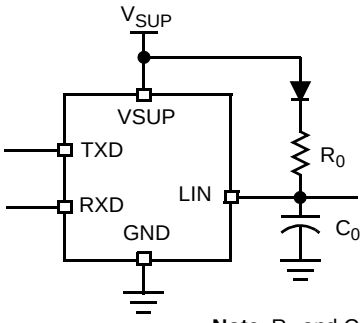
Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 7.0 V ≤ V_{SUP} ≤ 18 V, -40 °C ≤ T_A ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
TXD TIMING					
TXD Permanent Dominant State Delay[28]	t_{TXDDOM}	3.75	5.0	6.25	ms
FIRST DOMINANT BIT VALIDATION					
First dominant bit validation delay when device in Normal Mode[29]	t_{FIRST_DOM}	—	50	80	ms
FAST BAUD RATE TIMING					
EN Low Pulse Duration to Enter in Fast Baud Rate Using Toggle Function [30] EN High to Low and Low to High	t_1	—	—	45	µs
TXD Low Pulse Duration to Enter in Fast Baud Rate Using Toggle Function [30]	t_2	12.5	—	—	µs
Delay Between EN Falling Edge and TXD Falling Edge to Enter in Fast Baud Rate Using Toggle Function [30]	t_3	12.5	—	—	µs
Delay Between TXD Rising Edge and EN Rising Edge to Enter in Fast Baud Rate Using Toggle Function [30]	t_4	12.5	—	—	µs
RXD Low Level duration after EN rising edge to validate the Fast Baud Rate entrance[30]	t_5	1.875		6.25	µs

Notes
28. The LIN is in recessive state and the receiver is still active
29. See Figures 14, 15, 16, and 21
30. See Figures 19 and 20

TIMING DIAGRAMS



Note R_0 and C_0: 1.0 kΩ/1.0 nF, 660 Ω/6.8 nF, and 500 Ω/10 nF.

Figure 8. Test Circuit for Timing Measurements

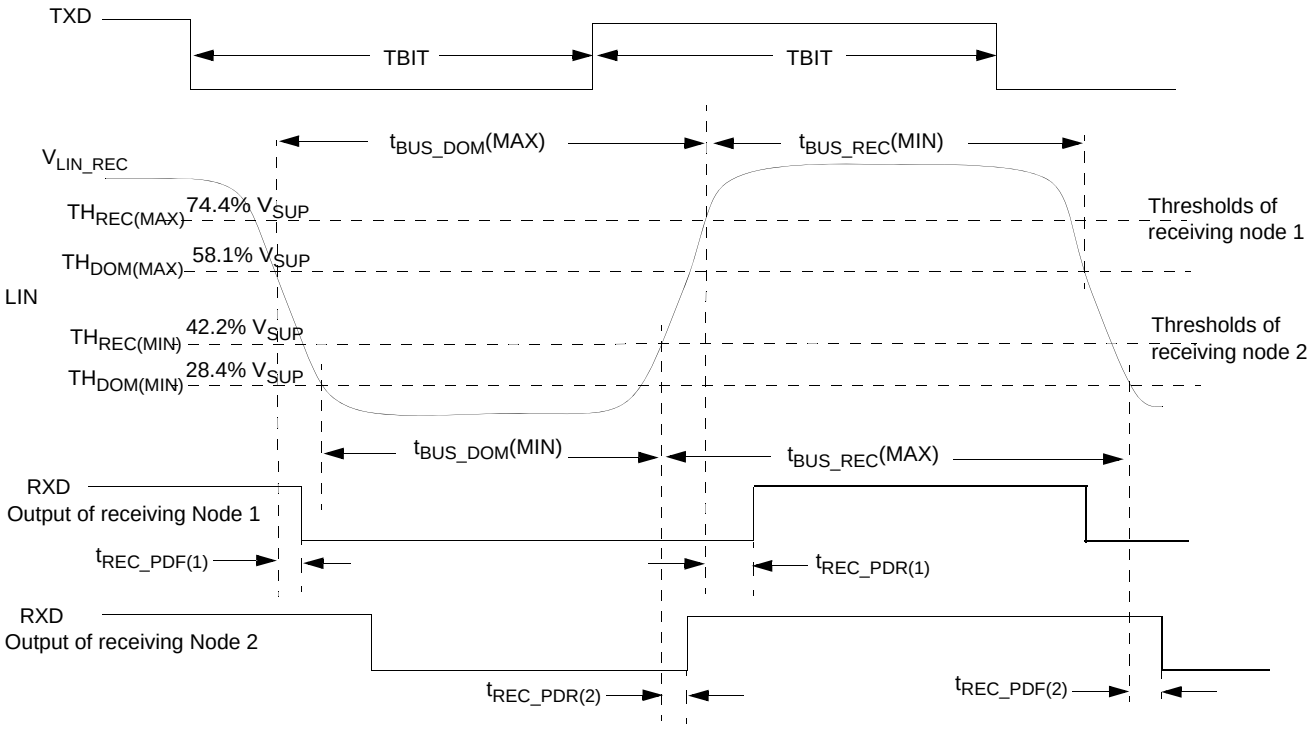


Figure 9. LIN1, LIN2 Timing Measurements for Normal Baud Rate (33663L, 33663S)

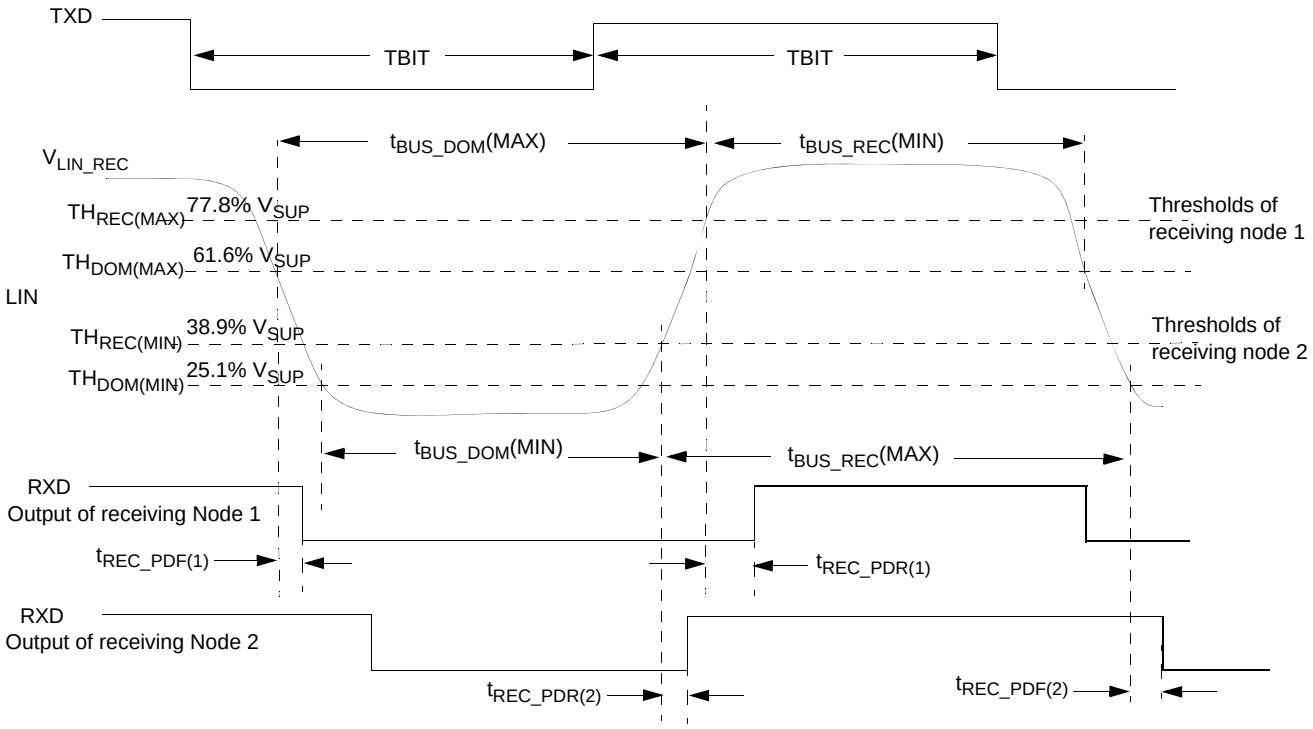


Figure 10. LIN1, LIN2 Timing Measurements for Slow Baud Rate (33663J)

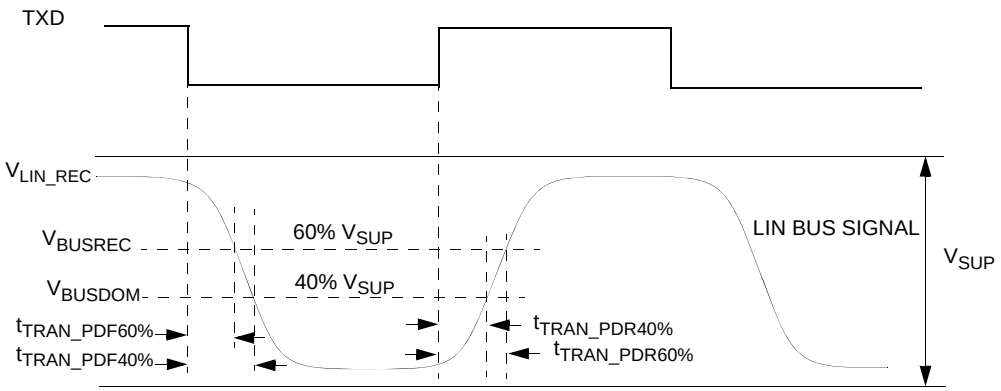


Figure 11. LIN1, LIN2 Transmitter Timing for 33663S

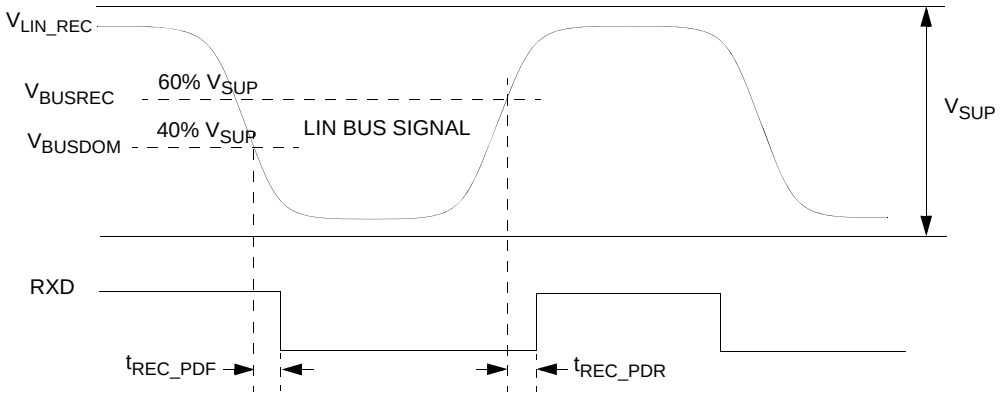


Figure 12. LIN1, LIN2 Receiver Timing

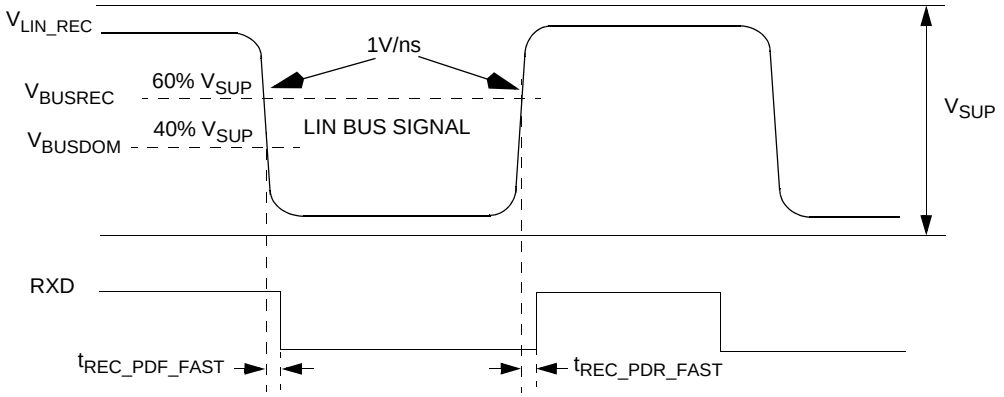


Figure 13. LIN1, LIN2 Receiver Timing LIN Slope 1.0 V/ns

FUNCTIONAL DIAGRAMS

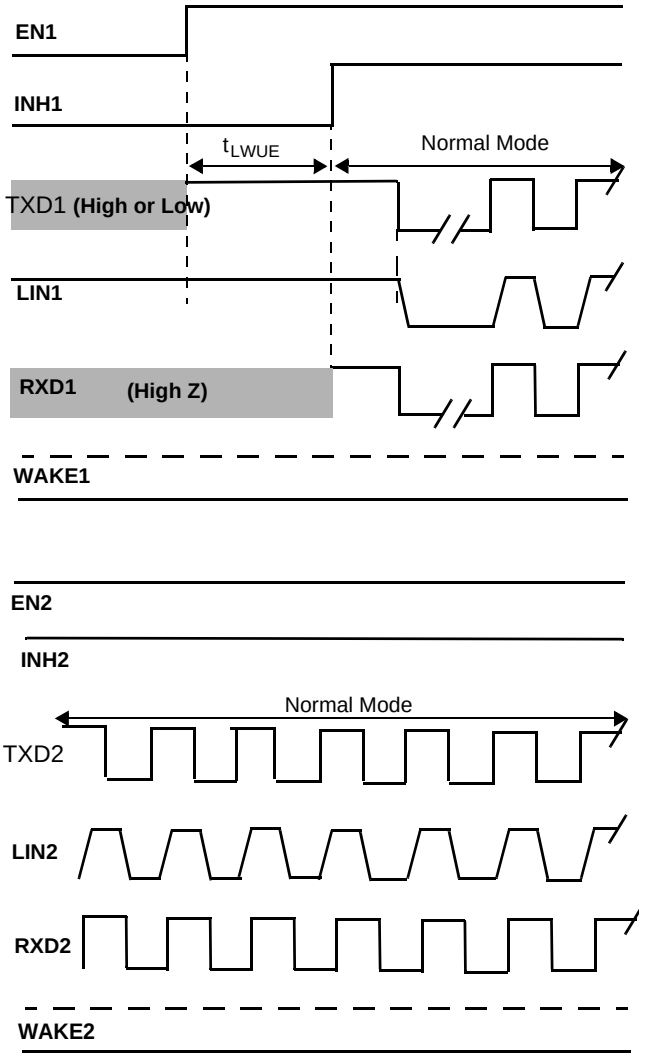


Figure 14. LIN Module 1 EN1 Pin Wake-up with TXD1 High & LIN Module 2 in Normal Mode

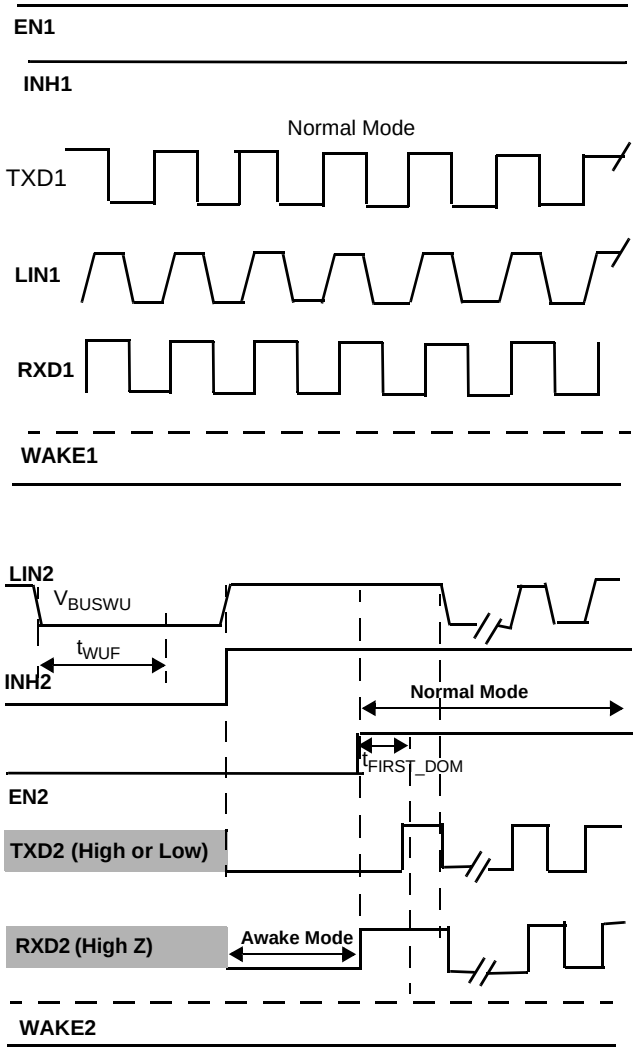


Figure 15. LIN Module 1 in Normal Mode & LIN Module 2 LIN2 Wake-up with TXD2 LOW

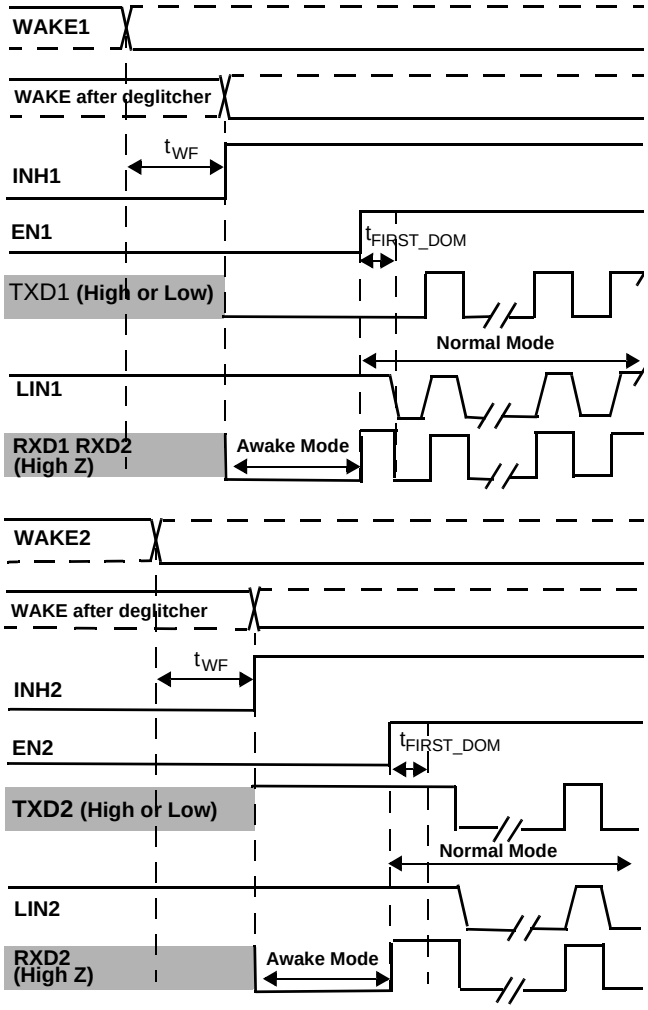


Figure 16. LIN Module 1 Wake1 Pin Wake-up with TXD1 Low & LIN Module 2 Wake2 Pin Wake-up with TXD2 High

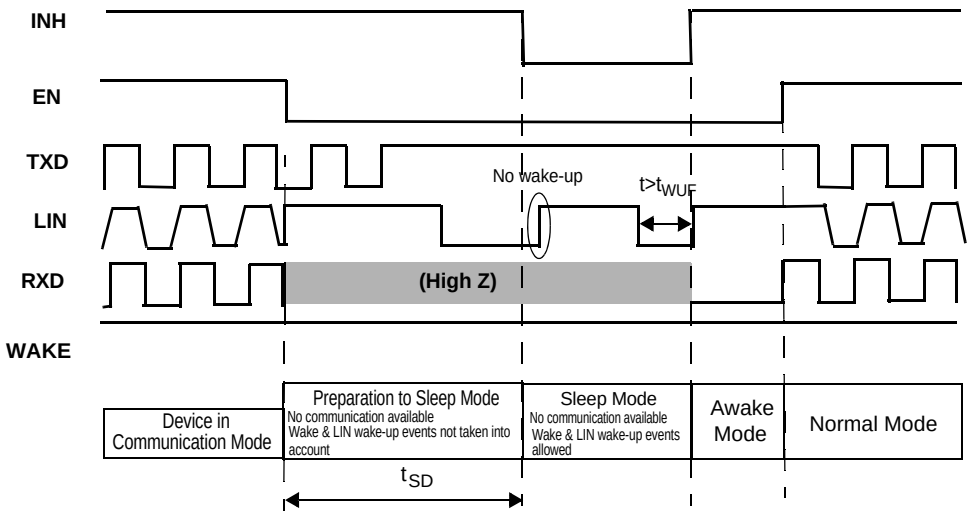


Figure 17. Bus Wake-up with LIN bus in Dominant During the Preparation to Sleep Mode (same sequence for LIN1 & LIN2)

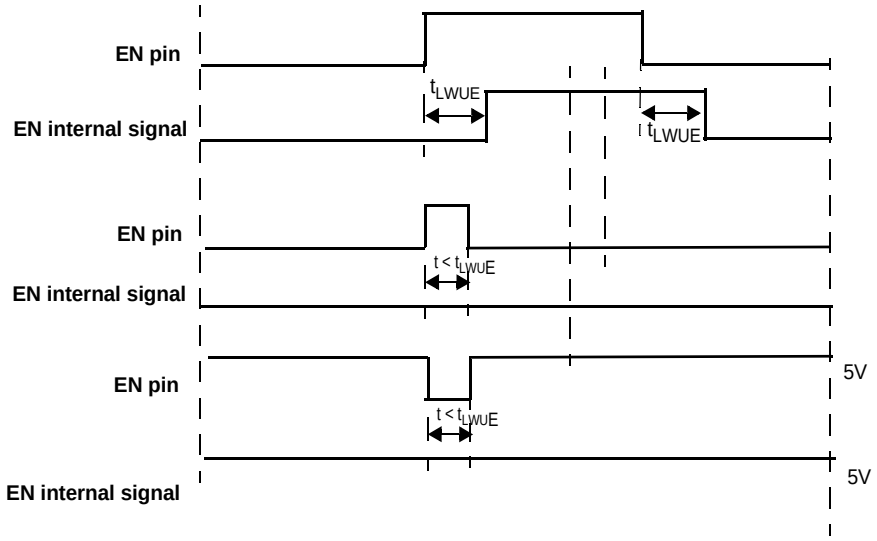


Figure 18. EN1, EN2 Pin Deglitcher

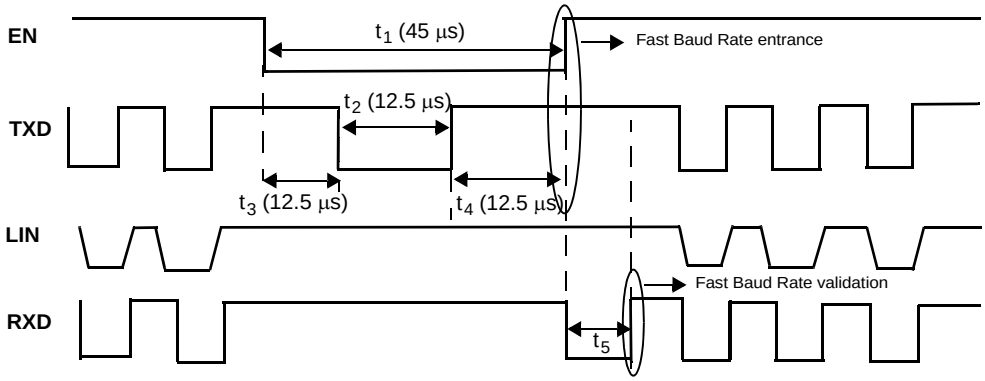


Figure 19. Fast Baud Rate Selection (Toggle Function) for LIN1 or LIN2

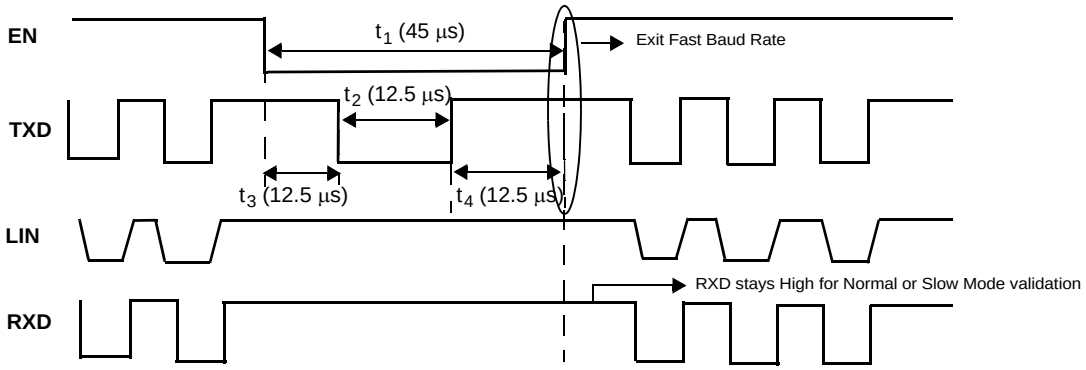


Figure 20. Fast Baud Rate Mode Exit (Back to Normal or Slow Slew Rate) for LIN1 or LIN2

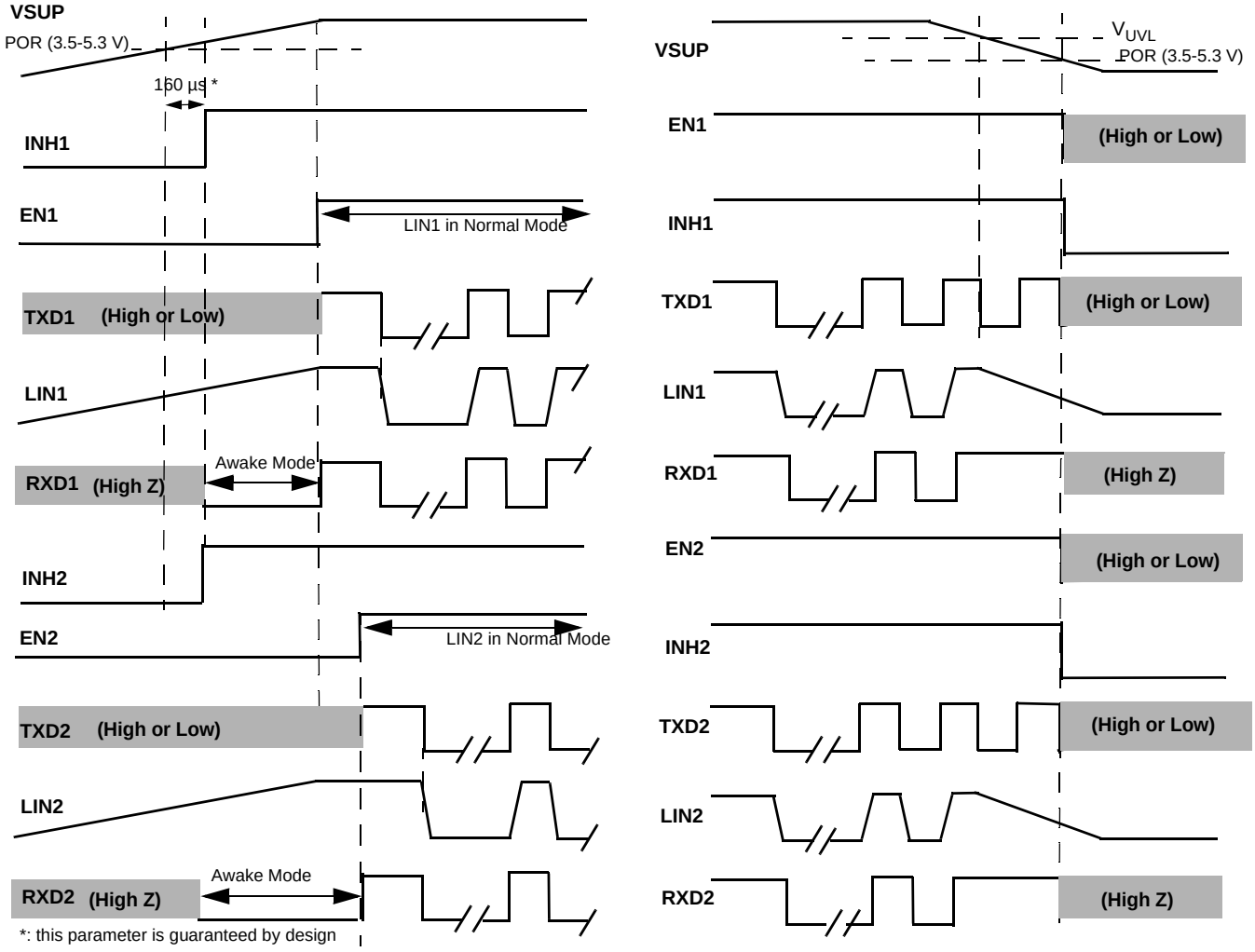


Figure 21. Power Up and Down Sequences

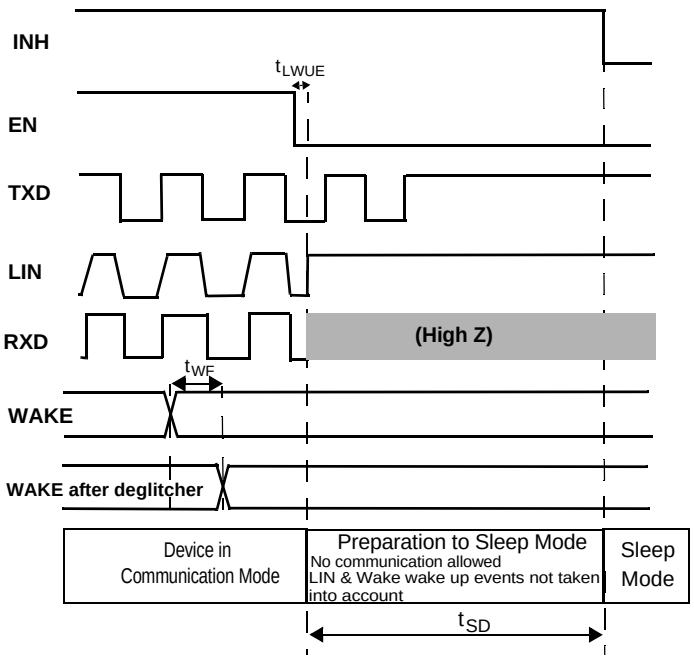


Figure 22. Sleep Mode Sequence for LIN1 or LIN2

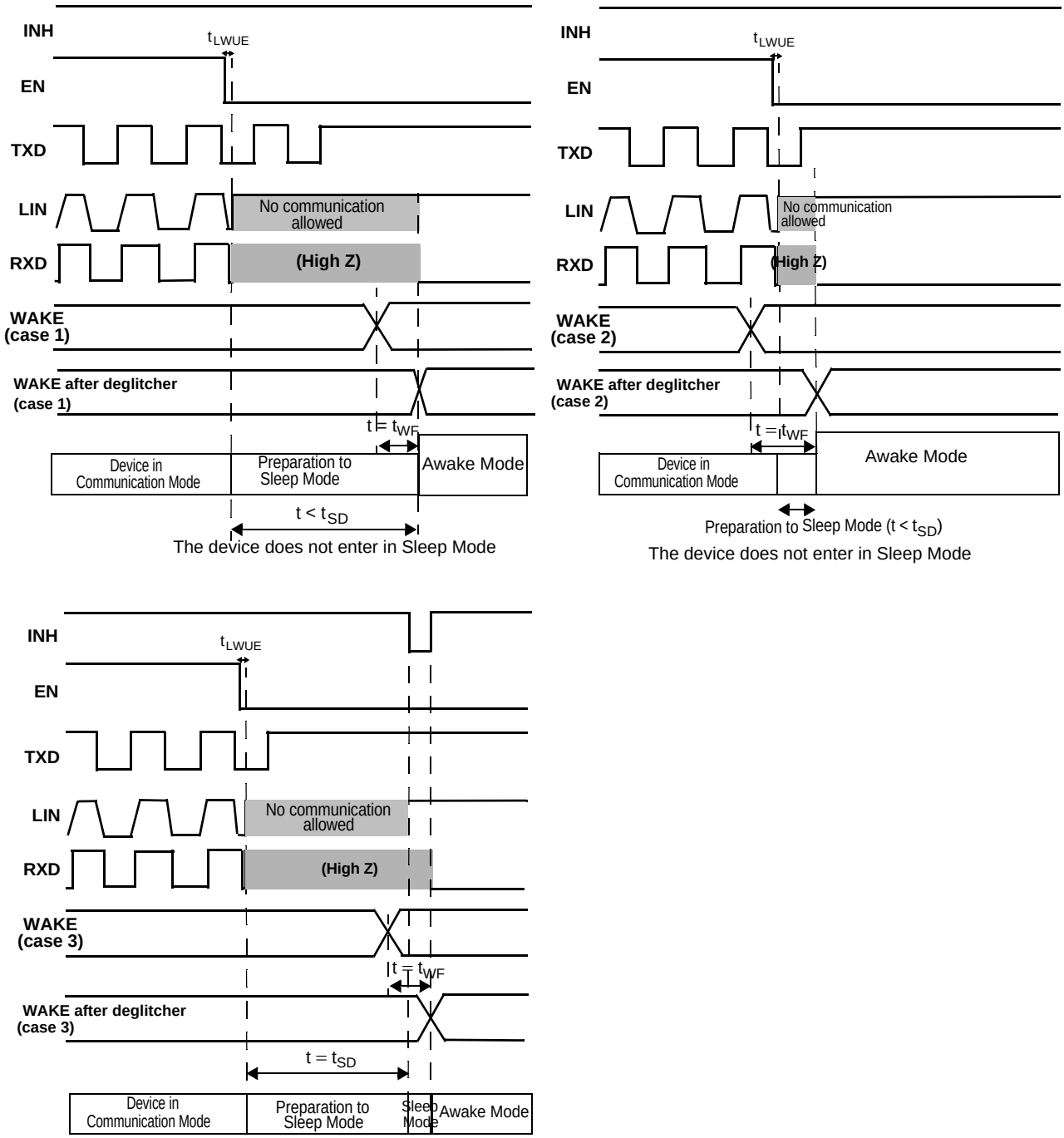


Figure 23. Examples of Sleep Mode Sequences for LIN1 or LIN2

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 33663L and 33663J are both a Physical Layer component dedicated to automotive LIN sub-bus applications.

The 33663L features include a 20 kbps baud rate and the 33663J a 10 kbps baud rate. Both integrate fast baud rate for test and programming modes, excellent ESD robustness, immunity against disturbance, and radiated emission performance. They have safe behavior, in case of a LIN bus short-to-ground, or a LIN bus leakage during low power mode.

Digital inputs are 5.0 and 3.3 V compatible without any external required components.

The INH1 and INH2 outputs may be used to control an external voltage regulator, or to drive a LIN bus pull-up resistor.

FUNCTIONAL PIN DESCRIPTION

POWER SUPPLY PIN (VSUP)

The VSUP supply pin is the power supply pin for the 33663L or 33663J. In an application, the pin is connected to a battery through a serial diode, for reverse battery protection. The DC operating voltage is from 7.0 to 18 V. This pin sustains standard automotive condition, such as 40 V during load dump. To avoid a false bus message, an under-voltage on VSUP disables the transmission path (from TXD to LIN) when V_{SUP} falls below 6.7 V. Supply current in the Sleep mode is typically 6.0 μA for one LIN Module.

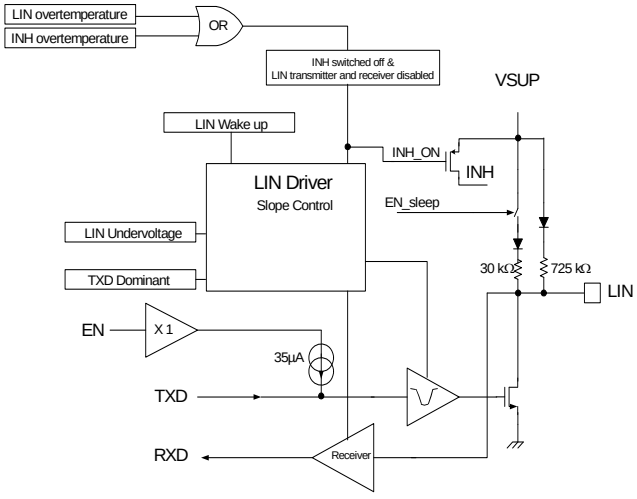
GROUND PIN (GND)

In case of a ground disconnection at the module level, the 33663L and 33663J do not have significant current consumption on the LIN bus pin when in the recessive state.

LIN BUS PIN (LIN1, LIN2)

The LIN1 and LIN2 pins represent the single-wire bus transmitter and receiver. It is suited for automotive bus systems, and is compliant to the LIN bus specification 1.3, 2.0, 2.1, and SAEJ2602-2.

The LIN interface is only active during Normal mode.



Transmitter Characteristics

The LIN driver is a low side MOSFET with internal over-current thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a slave node. An additional pull-up resistor of 1.0 kΩ must be added when the interface is used in the master node.

The LIN pin exhibits no reverse current from the LIN bus line to V_{SUP}, even in the event of a GND shift or V_{SUP} disconnection. The 33663 is tested according to the application conditions (i.e. in normal mode and recessive state during communication).

The transmitter has a 20 kbps baud rate (Normal baud rate) for the 33663L and 33663S devices, or 10 kbps baud rate (Slow baud rate) for the 33663J device.

As soon as the device enters Normal mode, the LIN transmitter will be able to send the first dominant bit only after the t_{FIRST_DOM} delay. t_{FIRST_DOM} delay has no impact on the receiver. The receiver will be enabled as soon as the device enters Normal mode.

Receiver Characteristics

The receiver thresholds are ratiometric with the device supply pin.

If the V_{SUP} voltage goes below the V_{SUP} under-voltage threshold (V_{UVL}, V_{UVH}), the bus LIN1 and bus LIN2 enter into a recessive state even if communication is sent to TXD1 or TXD2.

For the LIN Module 1, in case of LIN1 Thermal Shutdown, the transceiver and receiver are in recessive and INH1 turned off. When the temperature is below the T_{LINSD}, INH1 and LIN1 will be automatically enabled. The same behavior is valid for LIN Module 2.

For each LIN Module, the Fast Baud Rate selection is reported by the RXD pin. Fast Baud Rate is activated by the toggle function (See Figure 19). At the end of the toggle function, just after EN rising edge, RXD pin is kept low for t_5 to flag the Fast Baud Rate entry (See Figure 19).

To exit the Fast Baud Rate and return in Normal or Slow baud rate, a toggle function is needed. At the end the toggle function, RXD pin stays high to signal Fast Baud Rate exit (See Figure 20). The device enters into Fast Baud Rate at room and hot temperature.

DATA INPUT PINS (TXD1, TXD2)

The TXD1 and TXD2 inputs pins are the MCU interface to control the state of the LIN1 and LIN2 outputs. When TXD1 (TXD2) is LOW (dominant), LIN1 (LIN2) output is LOW; when TXD1 (TXD2) is HIGH (recessive), the LIN1 (LIN2) output transistor is turned OFF. TXD1/TXD2 pins thresholds are 3.3 V and 5.0 V compatible.

These pins have an internal pull-up current source to force the recessive state if the input pins are left floating.

If TXD1 (TXD2) stays low (dominant sate) more than 5.0 ms (typical value), the LIN1 (LIN2) transmitter of LIN Module goes automatically into recessive state.

DATA OUTPUT PINS (RXD1, RXD2)

Each LIN Modules integrate the same RXD output structure and functionality. Both pins are independent. The following description is the same for both.

RXD output pin is the MCU interface, which reports the state of the LIN bus voltage.

In Normal or Slow baud rate, LIN HIGH (recessive) is reported by a high voltage on RXD; LIN LOW (dominant) is reported by a low voltage on RXD. The RXD output structure is a tristate output buffer.

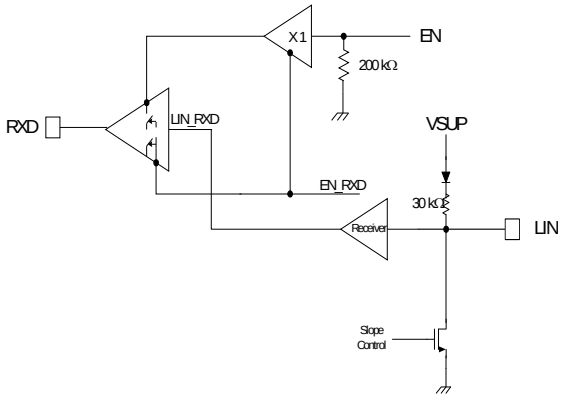


Figure 24. RXD interface

The RXD output pins are the receiver output of the LIN interface. The low level is fixed. The high level is dependent on EN voltage. If EN is set at 3.3 V, RXD V_{OH} is 3.3 V. If EN is set at 5.0 V, RXD V_{OH} is 5.0 V. The RXD1 and RXD2 V_{OH} level can be defined independently.

In sleep mode, RXD are high-impedance. When a wake-up event is recognized from the WAKE pin or from the LIN bus pin, RXD is pulled LOW to report the wake-up event. An external pull-up resistor may be needed.

ENABLE INPUT PINS (EN1, EN2)

EN1 (EN2) input pin controls the operation mode of the interface. If EN1 (EN2) = 1, the interface is in Normal mode, TXD1 (TXD2) to LIN1 (LIN2) after t_{FIRS_DOM} delay and LIN1 (LIN2) to RXD1 (RXD2) paths are both active. EN1 (EN2) pin thresholds are 3.3 V and 5.0 V compatible. RXD1 (RXD2) V_{OH} level follows EN1 (EN2) pin high level. One LIN Module enters the Sleep Mode by setting EN1 (EN2) LOW for a delay higher than t_{SD} (70 µs typ. value) and if the WAKE1 (WAKE2) pin state doesn't change during this delay. (see Figure 22). Both LIN Modules enter Sleep Mode if EN1 & EN2 LOW.

A combination of the logic levels on EN1 (EN2) and TXD1 (TXD2) pins allows the device to enter in Fast Baud Rate mode of operation (see Figure 19).

INHIBIT OUTPUT PINS (INH1, INH2)

The INH1 (INH2) output pin is connected to an internal high side power MOSFET. The pin has two possible main functions. It can be used to control an external switchable voltage regulator having an inhibit input. It can also be used to drive the LIN bus external resistor in the master node application, thanks to its high drive capability. This is illustrated in Figure 26.

In Sleep mode, INH1 (INH2) is turned OFF. If a voltage regulator inhibit input is connected to INH1 (INH2), the regulator will be disabled. If the master node pull-up resistor is connected to INH1 (INH2), the pull-up resistor will be unpowered and left floating.

In case of a INH1 (INH2) thermal shutdown, the high side is turned off and the LIN1 (LIN2) transmitter and receiver are in recessive state. An external 10 to 100 pF capacitor on INH1 (INH2) pin is advised in order to improve EMC performances.

WAKE INPUT PINS (WAKE1, WAKE2)

The WAKE1 (WAKE2) pin is a high-voltage input used to wake-up the device from the Sleep mode. WAKE1 (WAKE2) is usually connected to an external switch in the application.

The WAKE1 (WAKE2) pin has a special design structure and allows wake-up from both HIGH to LOW or LOW to HIGH transitions. When entering into Sleep mode, the corresponded LIN Module monitors the state of its WAKE pin and stores it as a reference state. The opposite state of this reference state will be the wake-up event used by the LIN Module to enter again into Normal mode.

If the WAKE1 (WAKE2) pin state changes during the Sleep mode Delay Time (t_{SD}) or before EN1 (EN2) goes low with a deglitcher lower than t_{WF}, the LIN Module will not enter in Sleep mode, but will go into Awake mode (See Figure 23).

An internal filter is implemented to avoid false wake-up event due to parasitic pulses (See Figure 16). WAKE1 (WAKE2) pin input structure exhibits a high-impedance, with extremely low input current when voltage at this pin is below 27 V. Two serial resistors should be inserted in order to limit the input current mainly during transient pulses and ESD. The total recommended resistor value is 33 kΩ. An external 10 to 100 nF capacitor is advised for better EMC and ESD performances.

Important The WAKE1 (WAKE2) pin should not be left open. If the wake-up function is not used, WAKE1 (WAKE2) should be connected to ground to avoid a false wake-up.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

As described by the following, the 33663L, 33663J, and 33663S have two operational modes, Normal and Sleep. In addition, there are two transitional modes: Awake mode which allows the device to go into Normal mode, and Preparation to Sleep mode which allows the device to go into Sleep mode.

NORMAL OR SLOW BAUD RATE

In the Normal mode, the LIN bus can transmit and receive information.

The 33663L and 33663S (20 kbps) have a slew rate and timing compatible with Normal Baud Rate and LIN protocol specification 1.3, 2.0, 2.1, and 2.2.

The 33663J (10 kbps) has a slew rate and timing compatible with Low Baud Rate.

From Normal mode, the three devices can enter into Fast Baud Rate (Toggle function).

FAST BAUD RATE

In fast baud rate, the slew rate is around 10 times faster than the normal baud rate. This allows very fast data transmission (>100 kbps) -- for example, electronic control unit (ECU) tests and microcontroller program download. The bus pull-up resistor might be adjusted to ensure a correct RC time constant in line with the high baud rate used.

The following sequence is applicable to both LIN Modules independently.

Fast baud rate is entered via a special sequence (called toggle function) as follows:

1. EN1 pin set LOW while TXD1 is HIGH
2. TXD1 stays HIGH for 12.5 µs min
3. TXD1 set LOW for 12.5 µs min
4. TXD1 pulled HIGH for 12.5 µs min
5. EN1 pin set LOW to HIGH while TXD1 still HIGH

The LIN Module enters into the fast baud rate if the delay between step 1 to step 5 is 45 µs maximum. The toggle function is described in Figures 19. Once in fast baud rate, the same toggle function just described previously is used to bring the LIN Module 1 back into normal baud rate.

Fast baud rate selection is reported to the MCU by the RXD1 pin. Once the LIN Module 1 enters in this fast baud rate, the RXD1 pin goes at low level for t_5. When LIN Module 1 returns to normal baud rate with the same toggle function, the RXD1 pin stays high. Both sequences are illustrated in Figures 19 and 20.

PREPARATION TO SLEEP MODE

The following sequence is applicable to both LIN Modules simultaneously or separately. Here it is detailed with the LIN Module 1.

To enter the Preparation to Sleep mode, EN1 must be low for a delay higher than t_{LWUE}.

- If the WAKE1 pin state doesn't change during t_{SD} and t_{LWUE}, then the LIN Module 1 goes in Sleep Mode.
- If the WAKE1 pin state changes during t_{SD} and if t_{WF} is reached after end of t_{SD}, then the LIN Module 1 goes into Sleep mode after the end of t_{SD} timing.
- If the WAKE1 pin state changes during t_{SD} and t_{WF} delay has been reached before end of t_{SD}, then the LIN Module 1 goes into Awake Mode.
- If the WAKE1 pin state changes before t_{SD} and the delay t_{WF} ends during t_{SD}, then the LIN Module 1 goes in Awake Mode.
- If EN1 goes high for a delay higher than t_{LWUE}, the LIN Module 1 returns in Normal mode.

SLEEP MODE

The following Sleep mode paragraph is applicable to both LIN Modules simultaneously or separately. LIN Module 1 is an example.

To enter into Sleep mode, EN1 must be low for a delay longer than t_{SD} and the WAKE1 pin must stay in the same state (High or Low) during this delay. The LIN Module 1 conditions to not enter Sleep mode, but enter Awake mode are detailed in the Preparation into Sleep Mode chapter. See Figure 23.

In Sleep mode, the transmission path is disabled and the LIN Module 1 is in Low Power mode. Supply current from V_{SUP} is very low. Wake-up can occur from LIN1 bus activity, from the EN1 pin and from the WAKE1 input pin. If during the preparation to Sleep mode delay (t_{SD}), the LIN1 bus goes low due to LIN1 network communication, the LIN Module 1 still enters Sleep mode. The LIN Module 1 can be awakened by a recessive to dominant start, followed by a dominant to recessive state after $t > t_{WUF}$.

After a wake-up event, the LIN Module 1 enters into Awake mode. In Sleep mode, the LIN Module 1 internal 725 kOhm pull-up resistor is connected and the 30 kOhm is disconnected.

DEVICE POWER-UP (Awake Transitional Mode)

At power-up (V_{SUP} rises from zero), when V_{SUP} is above the Power-On Reset voltage, both LIN Modules automatically switch after a 160 µs delay time to the Awake transitional mode. Both INH pins (INH1 and INH2) go to a HIGH state and RXD1and RXD2 to a LOW state. See Figure 21.

DEVICE WAKE-UP EVENTS

The 33663L, 33663J and 33663S can be awakened from Sleep mode by three wake-up events:

- Remote wake-up via LIN1 and/or LIN2 bus activity
- Via the EN1 and/or EN2 pin
- Toggling the WAKE1 and/or WAKE2 pin

Remote Wake from LIN1, LIN2 Bus (Awake Transitional Mode)

Each LIN Transceiver is awakened by its LIN dominant pulse longer than t_{WUF}. Dominant pulse means: a recessive to dominant transition, wait for $t > t_{WUF}$, then a dominant to recessive transition. This is illustrated in Figure 15. Once the wake-up is detected (during the dominant to recessive transition), the LIN Module waken up by its LIN enters into Awake mode, with its INH HIGH and RXD pulled LOW.

Once in the Awake mode, its EN pin has to be set to 3.3 V or 5.0 V (depending on the system) to enter into Normal mode. Once in Normal mode, the LIN Module has to wait t_{FIRST_DOM} delay before transmitting the first dominant bit.

Wake-up from EN1, EN2 pins

Each LIN Module can be awakened by a LOW to HIGH transition of its EN pin. When EN is switched from LOW to HIGH and stays HIGH for a delay higher than t_{LWUE}, the LIN Module is awakened and enters into Normal mode. See Figure 14. Once in Normal mode, the LIN Module has to wait t_{FIRST_DOM} delay before transmitting the first dominant bit.

Wake-up from WAKE1, WAKE2 Pins (Awake Transitional Mode)

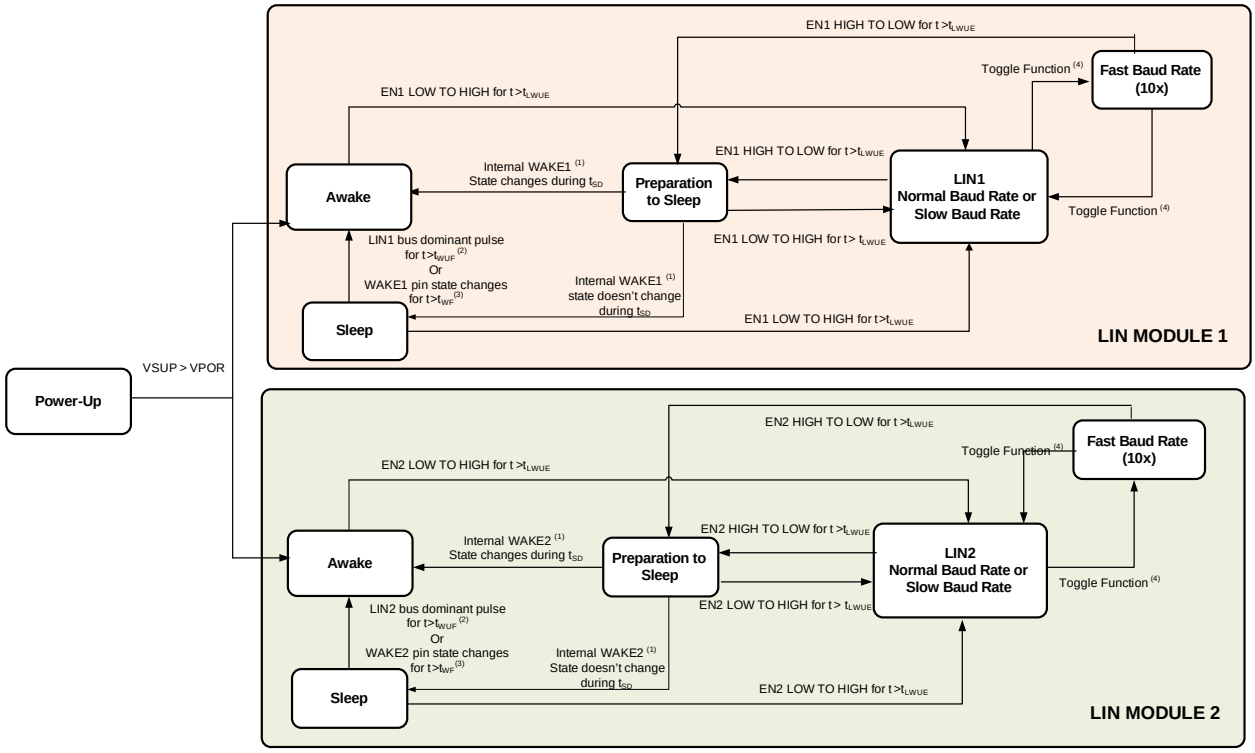
Just before entering the Sleep mode, the WAKE pin state of the concerned LIN Module is stored. A change in the level longer than the deglitcher time (70 µs maximum) will generate a wake-up, and the LIN Module enters into the Awake Transitional mode, with its INH HIGH and RXD pulled LOW. See Figure 16. The LIN Module goes into Normal mode when its EN is switched from LOW to HIGH and stays HIGH for a delay higher than t_{LWUE}. Once in Normal mode, the LIN Module has to wait t_{FIRST_DOM} delay before transmitting the first dominant bit.

FAIL-SAFE FEATURES

Tables 7 describes the 33663 protections.

Table 7. Fail Safe Features

BLOCK	FAULT	FUNCTIONAL MODE	CONDITION	FALLOUT	RECOVERY CONDITION	RECOVERY FUNCTIONALITY MODE
Power Supply	Power on Reset (POR)	All modes	V_{SUP} < 3.5 V (min) then power up	No internal supplies	Condition gone	Device goes in Awake mode whatever the previous device mode
INH1 INH2	INH1 AND/OR INH2 Thermal Shutdown. Each LIN Module has its own INH Thermal Shutdown.	For the failed LIN Module: Normal, Awake & Preparation to Sleep modes	Temperature > 160 °C (typ)	INH high side of the failed LIN Module turned off and its LIN transmitter and receiver in recessive State	Condition gone	LIN Module returns in same functional mode
LIN1 LIN2	V_{SUP} under-voltage	Normal	V_{SUP} < V_{UVL}	Both LIN transmitters in recessive state	Condition gone	Device returns in same functional mode
	TXD1 AND/OR TXD2 Pins Permanent Dominant		TXD pin low for more than 5.0 ms (typ)	LIN transmitter of the failed LIN Module in recessive state	Condition gone	LIN Module returns in same functional mode
	LIN1 AND/OR LIN2 Thermal Shutdown. Each LIN Module has its own LIN Thermal Shutdown.	Normal mode	Temperature > 160 °C (typ)	LIN transmitter and receiver of the failed LIN Module in recessive state and its INH high side turned off	Condition gone	LIN Module returns in same functional mode



(1):internal WAKE is the WAKE signal filtered by t_{WF} (WAKE deglitcher)
(2):see figures 15 and 18
(3):see figures 14 and 17
(4):the Toogle Function is guaranteed at ambiant and hot temperature

Figure 25. Operational and Transitional Modes State

Table 7. Explanation of Operational and Transitional Modes State Diagram (each transceiver)

Operational/ Transitional	LIN1, LIN2	INH1 INH2	EN1 EN2	TXD1, TXD2	RXD1, RXD2
Sleep Mode	Recessive state, driver off with 725 kΩ pull-up.	OFF (low)	LOW	X	High-impedance. HIGH if external pull-up to V_{DD}.
Awake	Recessive state, driver off. 725 kΩ pull-up active.	ON (high)	LOW	X	LOW. If external pull-up, HIGH-to-LOW transition reports wake-up.
Preparation to Sleep Mode	Recessive state, driver off with 725 kΩ pull-up	ON (high)	LOW	X	High-impedance. HIGH if external pull-up to V_{DD}.
Normal Mode	Driver active. 30 kΩ pull-up active. Normal Baud Rate for 33662L and 33662S Slow Baud Rate for 33662J Fast Baud Rate (> 100 kbps) for 33662L, 33662S & 33662J	ON (high)	HIGH	LOW to drive LIN bus in dominant HIGH to drive LIN bus in recessive.	Report LIN bus state: • Low LIN bus dominant • High LIN bus recessive

X = Don't care.

COMPATIBILITY WITH LIN1.3

Following the Consortium LIN specification Package, Revision 2.1, November 24, 2006, Chapter 1.1.7.1 Compatibility with LIN1.3 page 15:

The LIN 2.1 physical layer and is backward compatible with the LIN 1.3 physical layer, but not the other way around. The LIN 2.1 physical layer sets harder requirements, i.e. a node using the LIN 2.1 physical layer can operate in a LIN 1.3 cluster.

TYPICAL APPLICATION

The 33663 can be configured for several applications. The figure below shows LIN2 as a slave node and LIN1 as a master node application. An additional pull-up resistor of 1.0 kΩ in series with a diode must be added when the device is used in the master node.

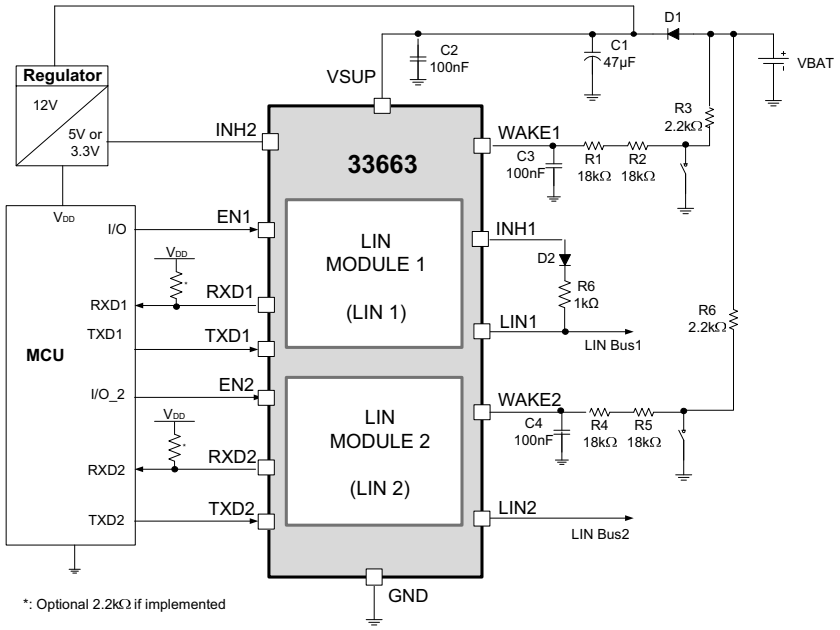
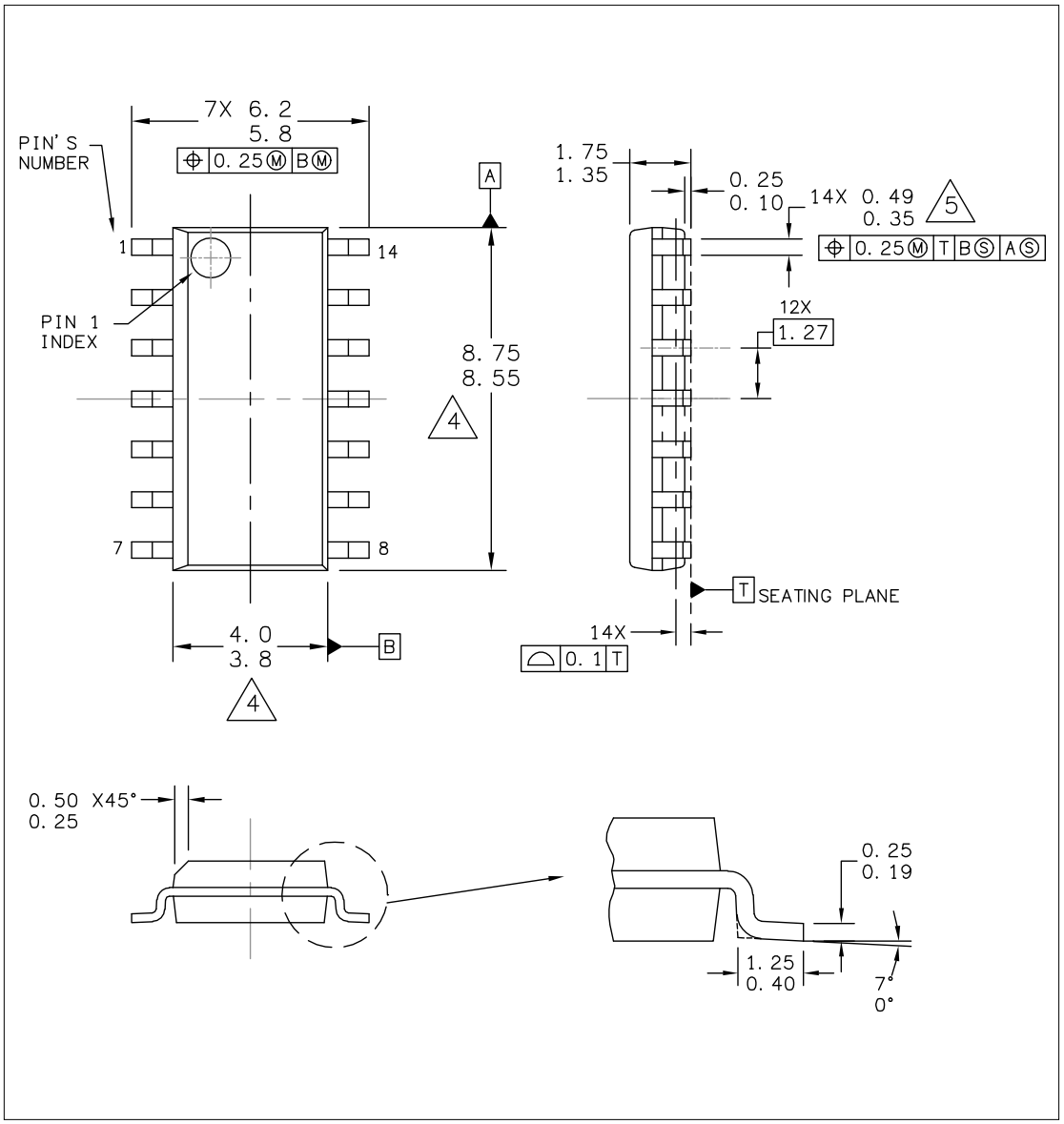


Figure 26. 33663 Typical Application

PACKAGING

PACKAGE DIMENSIONS

Important For the most current revision of the package, visit www.Freescale.com and do a keyword search on the 98A. Dimensions shown are provided for reference ONLY.



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TITLE: 14LD SOIC N/B, 1.27 PITCH CASE-OUTLINE	DOCUMENT NO: 98ASB42565B	REV: J
	CASE NUMBER: 751A-04	04 DEC 2007
	STANDARD: JECDEC MS-012AB	

EF SUFFIX
14-PIN
98ASB42565B
REVISION J

33663

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY. DATUM T IS A SURFACE.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTOAL IN EXCESS OF THE LEAD WIDTH AT MAXIMUM MATERIAL CONDITION.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASB42565B	REV: J
14LD SOIC N/B, 1.27 PITCH CASE–OUTLINE	CASE NUMBER: 751A–04	04 DEC 2007
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EF SUFFIX
14-PIN
98ASB42565B
REVISION J

33663

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	7/2012	• Initial Release.

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