Features

- Part of the FlexRay™ electrical, physical layer
- Interface between the communication controller and the transfer medium (twisted pair bus line)
- Supports data rates up to 10 MBaud
- Enhanced diagnosis capability provided via SPI with interrupt generation
- Protection against overload damage by current limitation and over temperature detection
- Bus driver outputs withstand – 27 V / + 40 V DC voltage
- Low EME due to balanced differential transmission
- TSSOP14 package

General Description

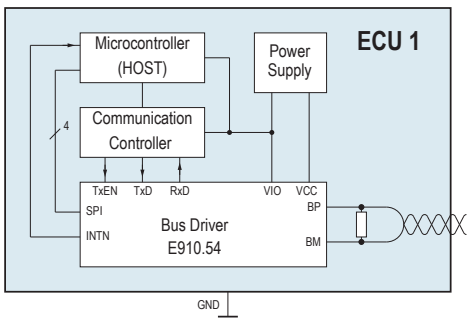
The low cost basic FlexRay™ transceiver is part of the electrical, physical layer in a FlexRay™ communication network. The E910.54 provides an interface between the twisted pair physical bus medium and a communication controller (CC). An SPI interface connects the bus driver (BD) to a host controller (HOST) to provide status information concerning failure detection on the bus lines (e.g. short-circuits, ground loss) and over temperature condition. An interrupt signal is generated whenever the failure status changes.

Applications

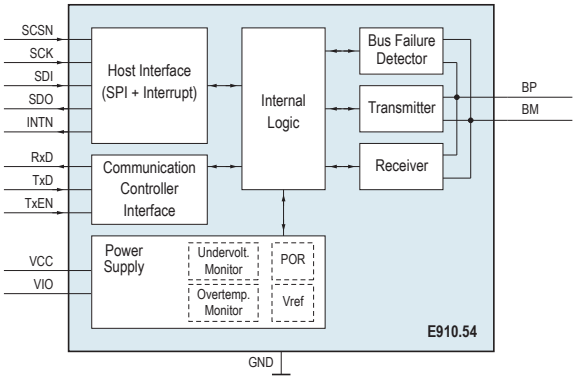
- Transceiver in FlexRay™ nodes (ECUs)

ELMOS is a member of the FlexRay consortium

Typical Application



Blockdiagram



Functional classes

The following table shows the implemented functional classes:

Functional class	Implemented
Bus driver regulator control	no
Bus driver - Bus guardian	no
Bus driver internal voltage regulator	no
Bus driver logic level adaptation	yes

1 Pinout

1.1 Pin description

Pin No.	Pin name	Pin type [1]	Pin description	Comment
1	VIO	S	IO Supply	3.3V or 5V
2	TXD	DI, PD	Transmit Data Input (from CC[2])	VIO-level
3	TXEN	DI, PU	Transmit Data Enable (from CC[2])	VIO-level (low active)
4	RXD	DO	Receive Data Output (to CC[2])	VIO-level
5	res.	S	reserved (for ELMOS internal test purposes only)	Pin may be connected to VCC, VIO or GND in the application
6	SCSN	DI, PU	Chip Select Input (from HOST)	VIO-level
7	SCK	DI, PU	SPI Clock Input (from HOST)	VIO-level
8	SDO	DO	SPI Data Output (to HOST)	VIO-level
9	SDI	DI, PD	SPI Data Input (from HOST)	VIO-level
10	INTN	DO	Failure sum signal	VIO-level (low active)
11	GND	S	Ground	
12	BM	AIO	Bus Line Minus	VCC-level but protected against HV
13	BP	AIO	Bus Line Plus	VCC-level but protected against HV
14	VCC	S	Transceiver Supply	5V

1) D = Digital
A = Analog
S = Supply
I = Input
O = Output
HV = High Voltage
PU = Pull-Up
PD = Pull-Down

2) CC = Communication controller

1.2 Pinout

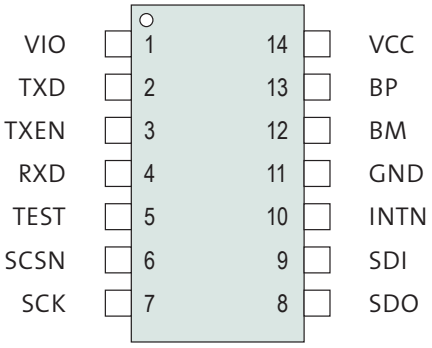


Figure 1: E910.54 pinout

2 Operating conditions

All voltages are referred to GND. Currents are positive when flowing into the node unless otherwise specified.

2.1 Absolute maximum ratings

Operating the device beyond these limits may cause permanent damage.

No.	Parameter	Condition	Symbol	Min	Max	Unit
1	Transceiver Supply Voltage		VCC	-0.3	5.5	V
2	IO Supply Voltage		VIO	-0.3	5.5	V
3	Bus Line Voltage		VBP, VBM	-27 [1)]	40	V
4	Digital IO (3.3V or 5V)		VTXEN, VTXD, VRXD, VSCSN, VSCK, VSDI, VSDO, INTN	-0.3	VIO+0.3V	V
5	ESD voltage HBM according to IEC61000-4-2 [2)] (system level)		Pin BP and BM	8		kV
6	ESD voltage HBM according to AEC-Q100 [3)] (chip level)		Pin BP and BM	8		kV
			Other pins	2		kV

1) Minimum value at -40...95°C. Minimum value at +95...125°C VBP = VBM = -17V.

2) Cs=150pF, Rd = 330Ω

3) Cs=100pF, Rd=1500Ω

4) Pulse 1, 2a, 3a, 3b according to ISO7637-1, -2 class C

No.	Parameter	Condition	Symbol	Min	Max	Unit
7	ESD voltage CDM according to AEC-Q100		Corner pins (1,6,7,14)	750		V
			Other pins (2-5, 8-13)	500		V
8	Immunity to transients [4)]		Pins BP and BM	-150	+100	V
9	Thermal Resistance Junction to ambient		R_{TJA}		100	KW^{-1}
10	Power Dissipation	Tamb ≤ 125 °C	P_{diss}		150	mW
11	Ambient Temperature		T_A	-40	125	°C
12	Junction Temperature		T_j		150	°C
13	Storage Temperature		T_{STG}	- 40	125	°C

1) Minimum value at -40...95°C. Minimum value at +95...125°C VBP = VBM = -17V.

2) Cs=150pF, Rd = 330Ω

3) Cs=100pF, Rd=1500Ω

4) Pulse 1, 2a, 3a, 3b according to ISO7637-1, -2 class C

2.2 Recommended operating conditions

Parameters are guaranteed within the range of operating conditions unless otherwise specified.

No.	Parameter	Condition	Symbol	Min	Max	Unit
1	Transceiver Supply Voltage		VCC	4.75	5.25	V
2	IO Supply Voltage [(1]	3.3V interface	VIO	3.0	3.6	V
3	IO Supply Voltage [(1]	5V interface	VIO	4.75	5.25	V
4	Operating Temperature Range		T_{op}	- 40	125	°C

1) 3.3V, optional 5V power supply

3 Detailed electrical specification

3.1 Power supplies

No.	Parameter	Condition	Symbol	Min	Typ	Max	Unit
1	Supply current at VCC	TX idle	ICCni	2.5		6	mA
2	Supply current at VCC	TX active	ICCna		30 [1)]	50 [2)]	mA
3	Supply current at VIO	TX idle	IVIO		35	60	µA
4	Power on reset at VCC	Falling edge	POR	1.6			V

1) The current consumption depends on succession of the sent frames

2) In case of a short circuit to GND only

3.2 Bus driver - Communication controller interface

No.	Parameter	Condition	Symbol	Min	Typ	Max	Unit
1	High level input voltage		VIH_TXD, VIH_TXEN	0.7·VIO			V
2	Low level input voltage		VIL_TXD, VIL_TXEN			0.3·VIO	V
3	High level output voltage	I_{load} = -2mA	VOH_RXD	0.8·VIO		VIO	V
4	Low level output voltage	I_{load} = 2mA	VOL_RXD			0.2·VIO	V
5	Pull up current	at TXEN, VIO=5V	Ipu	-50	-22	-5	µA
6	Pull down current	at TXD, VIO=5V	Ipd	5	30	50	µA

The data lines TXD and TXEN from and RXD to the Communication Controller are at VIO level.

3.3 Bus driver - Host interface

No.	Parameter	Condition	Symbol	Min	Typ	Max	Unit
1	High level input voltage		VIH_SCSN, VIH_SCK, VIH_SDI	0.7·VIO			V
2	Low level input voltage		VIL_SCSN, VIL_SCK, VIL_SDI			0.3·VIO	V
3	High level output voltage	I_{load} = -2mA	VOH_SDO, VOH_INTN	0.8·VIO		VIO	V
4	Low level output voltage	I_{load} = 2mA	VOL_SDO, VOL_INTN			0.2·VIO	V
5	SPI clock frequency		fSPI			5	MHz
6	Setup time SCSN		dspis	100			ns
7	Hold time SCSN		dspih	100			ns
8	Internal process time between 2 SPI commands		dspid	150			µs
9	Low level duration before low/high transition[1]		dScsnLow	100			µs
10	Pull up current	at SCSN, SCK VIO=5V	Ipu	-50	-22	-5	µA
11	Pull down current	at SDI, VIO=5V	Ipd	5	30	50	µA

The voltage of INTN to the host microcontroller is at VIO level.

(1 Refer to chapter 4.1.3

3.4 Bus driver - Bus signal interface

3.4.1 Receiver characteristics

All parameter values are specified at **70ns** minimum bit time.

No.	Parameter	Condition	Symbol	Min	Typ	Max	Unit
1	Upper receiver threshold for detecting activity	Idle Y Data_1	uBusActive-High	150		425	mV
2	Lower receiver threshold for detecting activity	Idle Y Data_0	uBusActiveLow	-425		-150	mV
3	Receiver threshold for detecting Data_1	Data_0 Y Data_1	uData_1	150		300	mV

No.	Parameter	Condition	Symbol	Min	Typ	Max	Unit
4	Receiver threshold for detecting Data_0	Data_1 → Data_0	uData_0	-300		-150	mV
5	Mismatch of receiver thresholds		||Data_0|-|uData_1||			30	mV
6	Receiver common mode input range	Receive function is undisturbed	uCM	-10		15	V
7	Receiver common mode input resistance	TX idle	RCM1, RCM2	10	20	40	kΩ
8	Bus bias voltage	BD_Normal, R_{load}=40Ω, C_{load}=100pF	uBias	1800	2500	3200	mV
9	Bus bias voltage	BD_Standby, R_{load}=40Ω, C_{load}=100pF	uBias	-200		200	mV
10	Idle detection time (1		dIdleDetection	50		250	ns
11	Activity detection time (1		dActivityDetection	100		300	ns
12	Idle reaction time		dBDRx_ai	50		400	ns
13	Activity reaction time		dBDRx_ia	100		450	ns
14	Receiver delay (2	negative edge	dBDRx10		40	75	ns
15	Receiver delay (2	positive edge	dBDRx01		40	75	ns
16	Receiver delay mismatch		dRxAsym (3			5	ns

(1 Guaranteed by design, only the idle and activity reaction times are tested

(2 RxD tested at 50% VIO thresholds

(3 dRxAsym=\|dBDRx10 - dBDRx01\|

3.4.2 Transmitter characteristics

All parameter values are specified at **70ns** minimum bit time.

No.	Parameter	Condition [4]	Symbol	Min	Typ	Max	Unit
1	Absolute differential voltage	$R_{load}\|\|C_{load}$= 40 Ω||100pF active	uBDTx-active	600		2000	mV
2	Absolute differential voltage	$R_{load}\|\|C_{load}$= 40 Ω||100pF idle	uBDTxidle	0		30	mV
3	Absolute output current	Shorted to GND, to -5V, to 27V [5]	iBPShort-Max, iBM-ShortMax			45	mA
4	Transmitter delay [1]	negative edge	dBDTx10		35	75	ns
5	Transmitter delay [1]	positive edge	dBDTx01		35	75	ns
6	Transmitter delay mismatch		dTxAsym [3]			4	ns
7	Fall time differential bus voltage [2]	80% to 20%, $R_{load}\|\|C_{load}$= 40 Ω||100pF	dBusTx10	3.75		18.75	ns
8	Rise time differential bus voltage [2]	20% to 80% $R_{load}\|\|C_{load}$= 40 Ω||100pF	dBusTx01	3.75		18.75	ns
9	Propagation delay idle Y active [1]	$R_{load}\|\|C_{load}$= 40 Ω||100pF	dBDTxia			100	ns
10	Propagation delay active Y idle [1]	$R_{load}\|\|C_{load}$= 40 Ω||100pF	dBDTxai			100	ns
11	Signal slope idle Y active [2]	$R_{load}\|\|C_{load}$= 40 Ω||100pF	dBusTxia			30	ns
12	Signal slope active Y idle [2]	$R_{load}\|\|C_{load}$= 40 Ω||100pF	dBusTxai			30	ns
13	Leakage current at BP/BM BD unsupplied, (VCC=0V)	T_{amb}=25°C, uVBP= uVBM= 5V			220		µA
14	Leakage current at BP/BM BD unsupplied, (VCC=0V)	T_{amb}=125°C, uVBP= uVBM= 5V	[5]		1020		µA

1) TxD, TxEN tested at 50% VIO thresholds

2) Guaranteed by design, conform to the range 10%-90% and rise and fall times 5....25ns.

3) dTxAsym= \|dBDTx10 - dBDTx01\|

4) R_{load} \|\| C_{load} means R_{load} in parallel with C_{load}

5) In accordance with the EPL 2.1a

3.5 Failure detection characteristics

No.	Parameter	Condition	Symbol	Min	Typ	Max	Unit
1	Undervoltage threshold VCC		VCCOK_N	4.3		4.7	V
2	Undervoltage threshold VIO		VIOOK_N	2.4		2.7	V
3	Overtemperature		TOVER	140		170	°C
4	Thresholds of RLOAD for under-load detection, including lost bus, lost RT		RULOAD	56		150	Ω
5	Thresholds of RLOAD for over-load detection, including shortcut BP-BM		ROLOAD	10		39	Ω
6	Timeout of a per-manent low of TxEN		dTOTxEN	5.4	7.7	10	ms
7	Undervoltage VCC reaction time		dUVCC		0.12	1	ms

4 Functional description

4.1 FlexRay bus driver in different FlexRay configurations

4.1.1 FlexRay network topologies

The simplest configuration is the point-to-point connection using two transceivers (half-duplex transmission). The load resistance for each line driver is the half of the termination resistor parallel to the differential input resistances of the receivers.

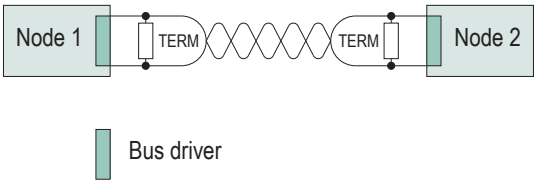


Figure 2: Bus drivers in a point-to-point connection

Normally, there are more than two nodes in a network. The best tradeoff between costs and performance is shown Fig. 3. Both ends of the cable are terminated (connected to Node1 and Node 2). All transceivers connected to other nodes are unterminated. The maximum number of stub nodes in a FlexRay passive bus is 22. If the distance between the stub splices is nearly zero, a passive star network emerges from the passive bus.

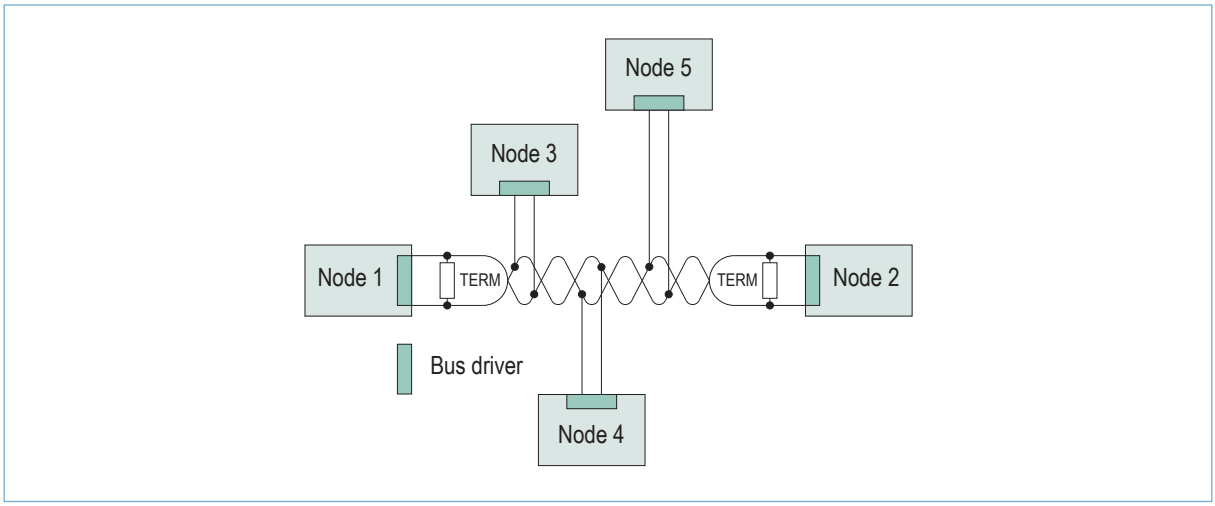


Figure 3: Bus drivers in a passive bus configuration

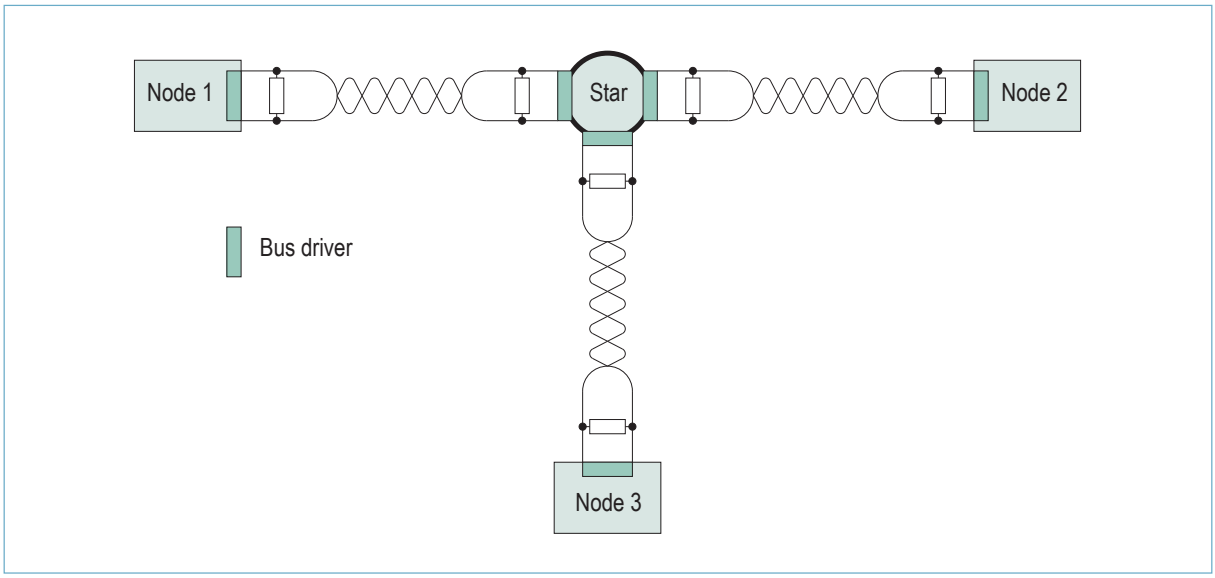


Figure 4: Bus drivers in a active star bus configuration

The active star configuration (Fig. 4) shows a better performance than a passive one. There are no unterminated nodes, all termination resistances are equal. The maximum cable length per branch may be chosen up to 24 m.

4.1.2 Node configuration

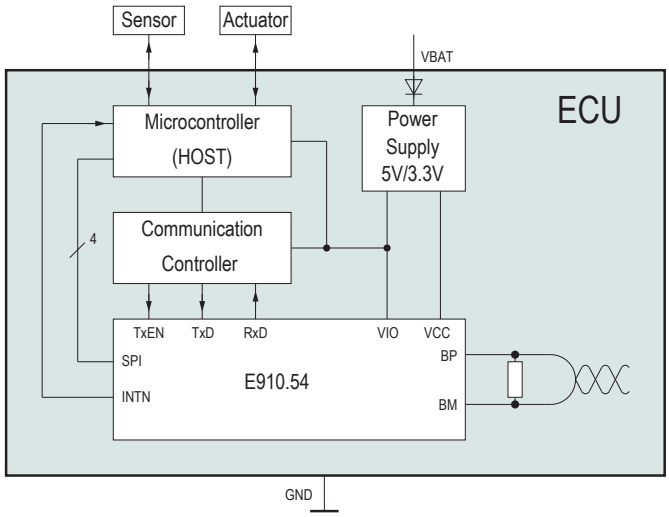


Figure 5: The E910.54 in a FlexRay node

An ECU (node) (Fig. 5) includes the host controller with its specific application (sensors, actuators), the communication part (the communication controller CC and the bus driver BD) and the local power supply (5V, 3.3V). The supply voltages are derived from the alternator voltage VBAT by means of linear or buck regulators. The main function of the bus driver is to transmit and to receive data to/from the bus lines. The communication controller CC sends the data to TxD if TxEN is active low. Received data from the bus are transferred to the CC at RxD.
Furthermore there is a Serial Parallel Interface (SPI) between the bus driver BD and the host. The function is to transmit the failure messages about the BD, the supplies and the transmission lines to the host. In addition the operation mode of the transceiver can be changed.

4.1.3 Operation modes

4.1.3.1 Normal and low-power operation modes

The basic bus driver BD supports 2 operation modes: *BD_Normal and BD_Standby* (low power mode).

BD_Normal mode
The bus driver is able to send and receive signals to and from the FlexRay bus.
The bus wires are biased to uBias via receiver input resistance.

***BD_Standby* mode**
The *BD_Standby* mode is a low power mode. The BD enters the state *BD_Standby* after VCC and VIO power on.
The BD is not able to send or receive data signals from the bus.
The power consumption is reduced compared to *BD_Normal*.
The bus wires are terminated to GND via receiver input resistance.

4.1.3.2 Operation mode transitions

Mode transitions happen upon commands from the host via the BD-host interface or due to undervoltage conditions. The host command has lower priority than the transition forced by an undervoltage condition which has the highest priority.
A detected undervoltage at VCC or VIO forces the BD from *BD_Normal* to *BD_Standby*.
The host signal for the transition *BD_Normal* to *BD_Standby* is a valid SPI command.
The host signal for the transition *BD_Standby* to *BD_Normal* is a valid SPI command or a low-high transition at the pin SCSN. The duration of the low phase is dScsnLow at least. This is a simplified hard wired method to switch the BD in the BD_Normal state if the SPI host interface is absent.
The transitions are depicted in the following operation state diagram.

4.1.3.3 Operation mode transitions state diagram

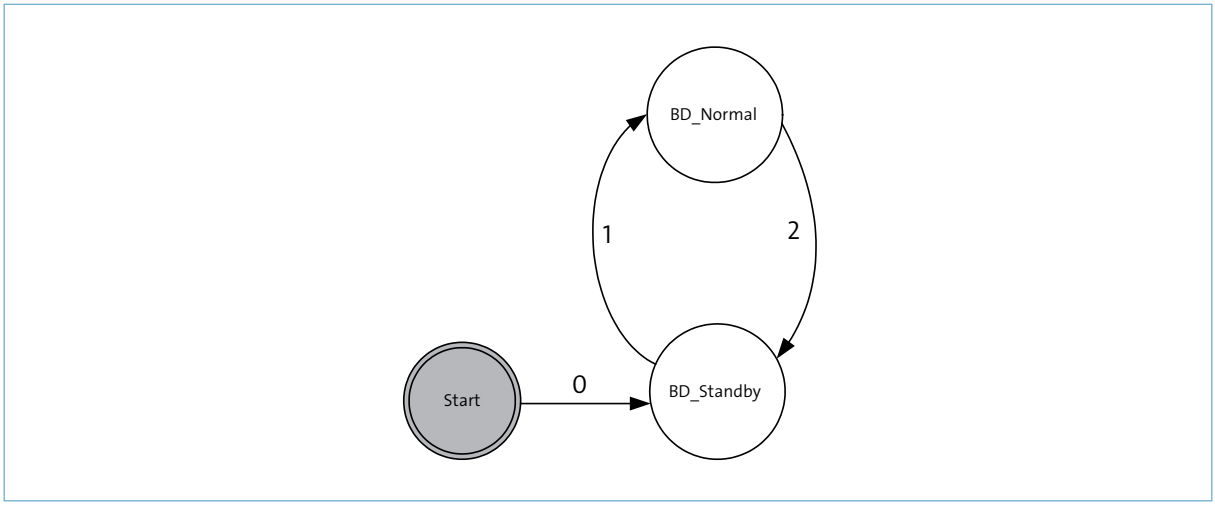


Figure 6: E910.54 operation mode state diagram

Transition	Conditions
0	VCC power on
1	SPI command (Goto_Normal bit = '1') or pulse at SCSN with low duration ≥dScsnLow [1)]
2	SPI command (Goto_Normal bit = '0') or VCCOK=0 or VIOOK=0

1) low to high transition after a low phase (minimum dScsnLow, see 3.3)

4.2 E910.54 functional blocks

4.2.1 Block diagram

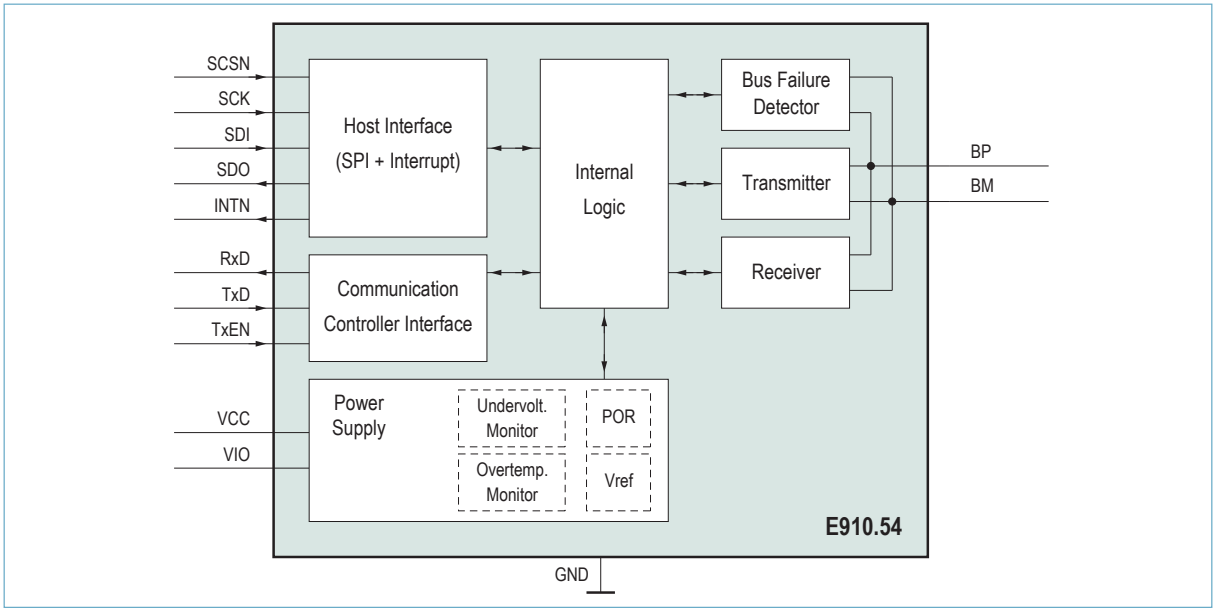


Figure 7: E910.54 simplified block diagram

4.2.2 Power supplies

The main power supply is at the VCC pin from an external voltage source. There is neither a low power mode nor power supply from the battery by means of an internal 5V regulator. The voltage pin VIO delivers the correct voltage for the I/O stages to/from communication controller and host controller. VCC (5V level) delivers the power for the transmitter and the receiver circuits and some auxiliary blocks (logic, power supply, failure detector).
VIO (3.3V level or 5V level) is the upper reference of the inputs and the outputs from/to the communication and the host controller. Internal level shifters transfer the signals from VIO level to the VCC level and vice versa. Note that all connections to the CC and the host must have the same voltage high level (all 3.3V or all 5V).

4.2.2.1 Voltage monitor

A voltage monitor compares the external voltage VCC with an internal reference voltage. If the supply voltage VCC is lower than the VCC undervoltage threshold, the output of the VCC monitor delivers the undervoltage flag VCCOK=0. The undervoltage signal is low active. It disables the transmission to the bus and sends the failure flag value to the host via SPI, if the SPI is able to work.

4.2.2.2 Temperature protection

The E910.54 provides an overtemperature supervision. In case the junction temperature rises above the overtemperature detection threshold the OTEMP flag is set in the SPI register and the INTN pin changes to ‚low'. The BD outputs send idle state to the bus.

4.2.2.3 Power-on

The Power-on provides the power on reset signal after switch on of VCC.

4.2.3 Communication controller interface

The interface concerns the pins TxEN, TxD and RxD. TxEN (low active) enables the transmit function. The TxD from the CC is an input signal of the transceiver. The line drivers of the transmitter send a balanced differential signal to the bus lines according to the TxD signal. The receiver recognizes the bus states Data_1, Data_0 and Idle. It transforms the differential bus voltage uBus to the digital signal at VIO level at the output pin RxD.

4.2.4 Host interface

Diagnosis information of the transceiver and the bus (overload, underload, short circuits, undervoltages and overtemperature) are stored in a register block. The data transfer to the host is accomplished by means of a SPI interface. Supported modes and bit order are shown in fig. 8. With this mode the output shift operation always takes place before the input sample operation. The clock polarity is fix CPOL = 0. The MSB is always transmitted / received first. Two bytes are transmitted within one SPI access. The shift out is done at the rising edge of SCK, the shift in at the falling edge of SCK.

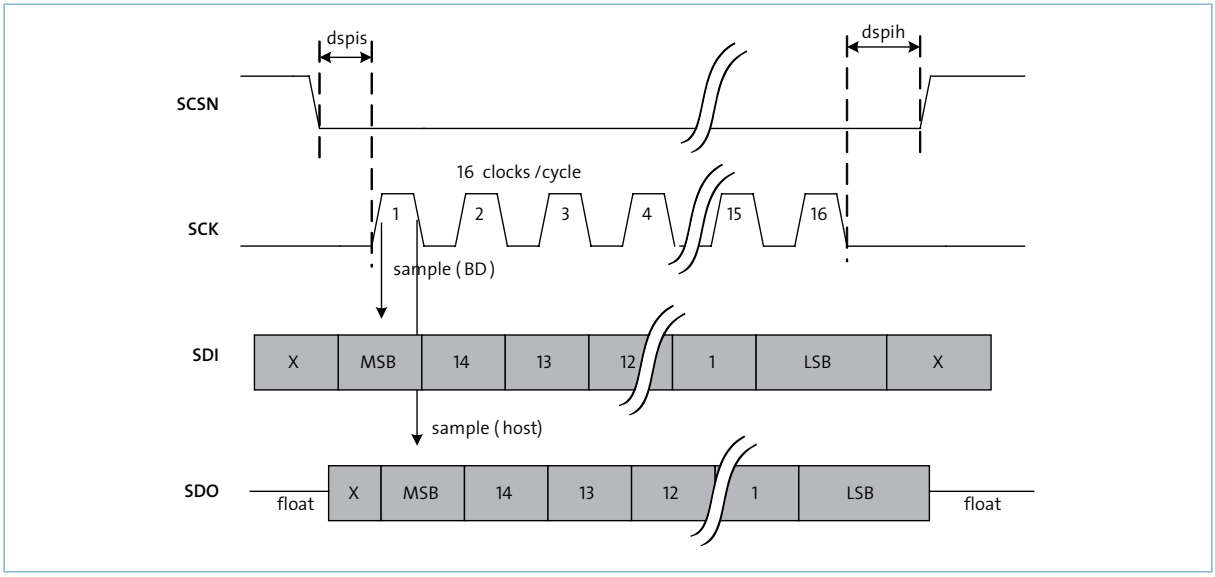


Figure 8: E910.54 SPI communication cycle

There is a minimum time span dspis between the falling edge of SCSN and the start of the first clock (rising edge). Also a minimum time dspih after the last (16th) clock (falling edge) and the rising edge of SCSN is defined. The necessary time of the internal processing between two SPI accesses is dspid.
For an efficient register access, a protocol has been defined with the following features:

- Pure master-slave protocol with host controller as master
- Frame is delimited by the status of SCSN (SCSN = frame delimiter)

SPI register entries

Following table shows a list and declaration of failures:

Failure	Failure if	Notes
Error flag	INTN=0	Failure sum signal
VCC undervoltage	VCCOK=0	Low active
VIO undervoltage	VIOOK=0	Low active
Overtemperature	OTEMP=1	Junction overtemperature
TxEN is permanently low ("babbling idiot")	TxENLOW=1	Flag is set after dTOTxEN
BP line shorted to GND	BP2GND=1	Bus error
BP line shorted to supply voltage	BP2VSUP=1	Bus error
BM line shorted to GND	BM2GND=1	Bus error
BM line shorted to supply voltage	BM2VSUP=1	Bus error
Bus overload (RDCLOAD is too low or short circuit BP-BM)	OLOAD=1	Bus error
Bus underload (Bus line connection or 1 or 2 termination resistors are interrupted)	ULOAD=1	Bus error

The registers of the most significant byte and the lower part of the second byte contain the failure messages of the transceiver (readable by the host controller). These are common failure messages as undervoltages at the supply pins (VCC, VIO), overtemperature, or permanent LOW at the TxEN as well as bus failures (bus line BP is shorted to GND (BP2GND), BM is shorted to the supply voltage (VBAT) (BM2VSUP) a.s.o.).
A valid SPI access resets the failure entries as well as the INTN state.
The mode change due to a undervoltage at the supply voltage does not change the SPI registers.

Bit	Address	SPI register READ	SPI register WRITE
15	F	Always 0	don't care [1]
14	E	Always 0	don't care [1]
13	D	Always 0	don't care [1]
12	C	Is_Normal [2]	Goto_Normal [2]
11	B	Always 0	don't care [1]
10	A	ULOAD	don't care [1]
9	9	OLOAD	don't care [1]
8	8	BM2VSUP	don't care [1]
7	7	BM2GND	don't care [1]
6	6	BP2VSUP	don't care [1]
5	5	BP2GND	don't care [1]
4	4	TxENLOW	don't care [1]

Bit	Address	SPI register READ	SPI register WRITE
3	3	OTEMP	don't care 1)
2	2	Always 1	don't care 1)
1	1	VIOOK	don't care 1)
0	0	VCCOK	don't care 1)

1) *Written values into those register addresses are ignored*
2) *Bit12=1 means BD is in BD_Normal (read) or shall go to BD_Normal (write).*
Bit12=0 means BD is in BD_Standby (read) or shall go to BD_Standby (write).

4.2.5 Bus signal interface

The basic bus driver has neither a *BD_Sleep* mode nor a remote wake up functionality. The receiver recognizes all 3 states of the bus lines (Data_0, Data_1 and Idle).
The RxD output becomes high, if an idle state is detected at the bus lines.
The RxD output becomes high, if an Data_1 state is detected at the bus lines.
The RxD output becomes low, if an Data_0 state is detected at the bus lines.

4.2.5.1 Receiver

The receiver circuit is responsible for receiving the bus signals, but also for biasing the bus lines. Figure 9 shows the principle schematic of the input behaviour of the receiver. Besides definitions of transient parameters of the receiver behavior from idle to active and vice versa are shown. The numerical values are defined in chapter 3.4.1. uBus is the differential bus voltage.

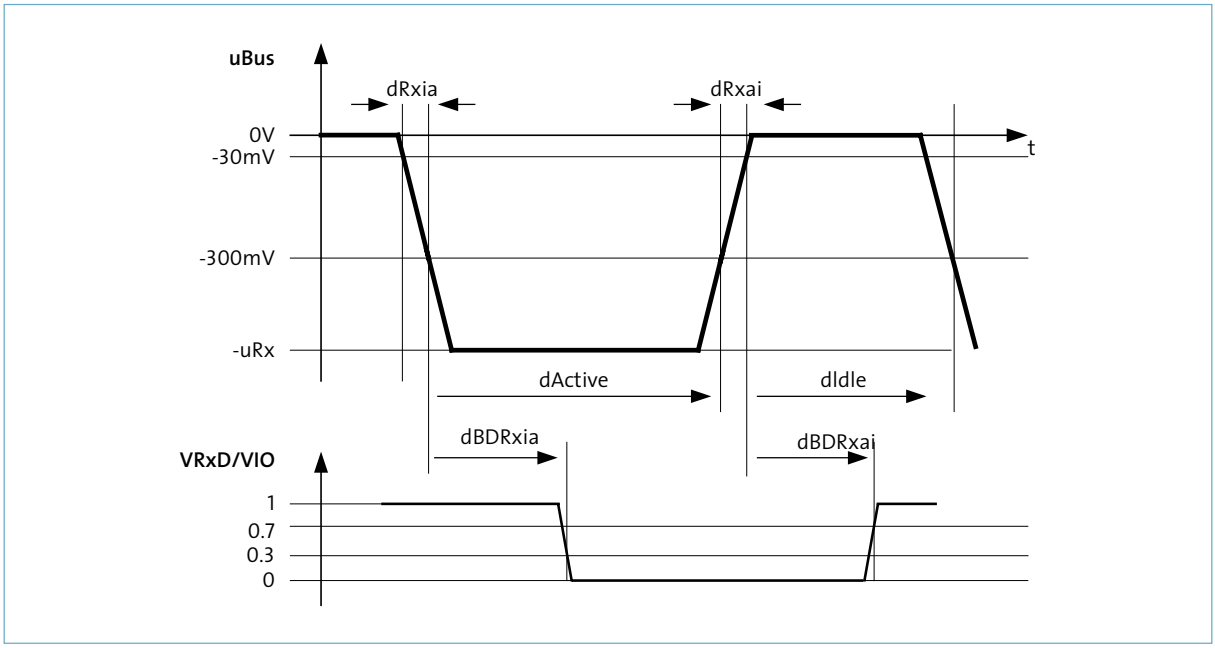


Figure 9: Receiver characteristics

The parameters of the normal receiving state are defined in figure 10. The numerical values are shown in chapter

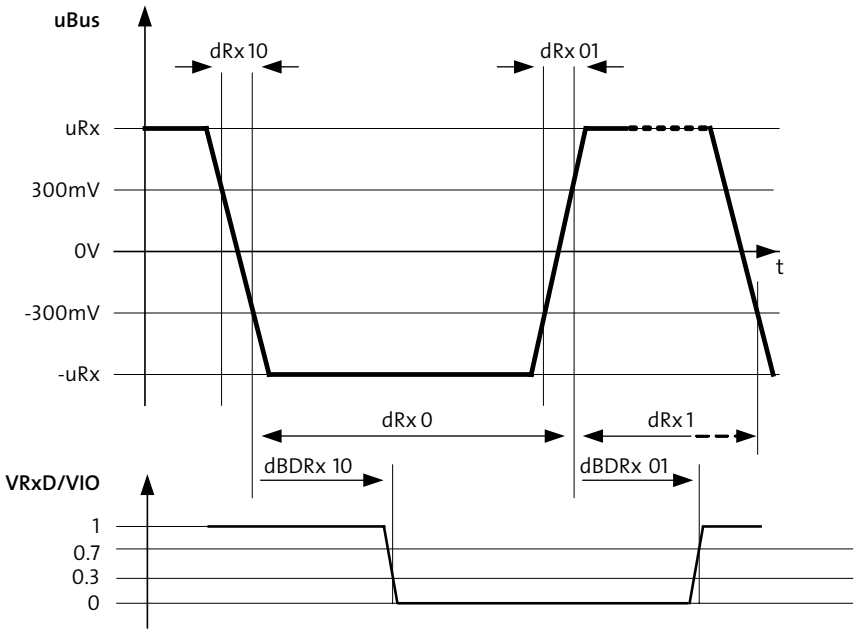


Figure 10: Receiver timing characteristics

Values for dRx10, dRx01, dRx0 and dRx1 according to the EPL 2.1a.

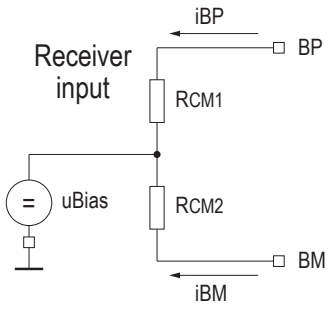


Figure 11: Biasing circuit of the receiver

4.2.5.2 Transmitter

The transmitter forms the differential bus signal from the digital TxD signal. The transmission is enabled only, if the signal TxEN is low.
The transmitter delay is defined as the duration for transferring the digital TxD signal to the analog information on the bus as depicted in the following figure. The numerical values are defined in chapter 3.4.2. uBus is the differential bus voltage.

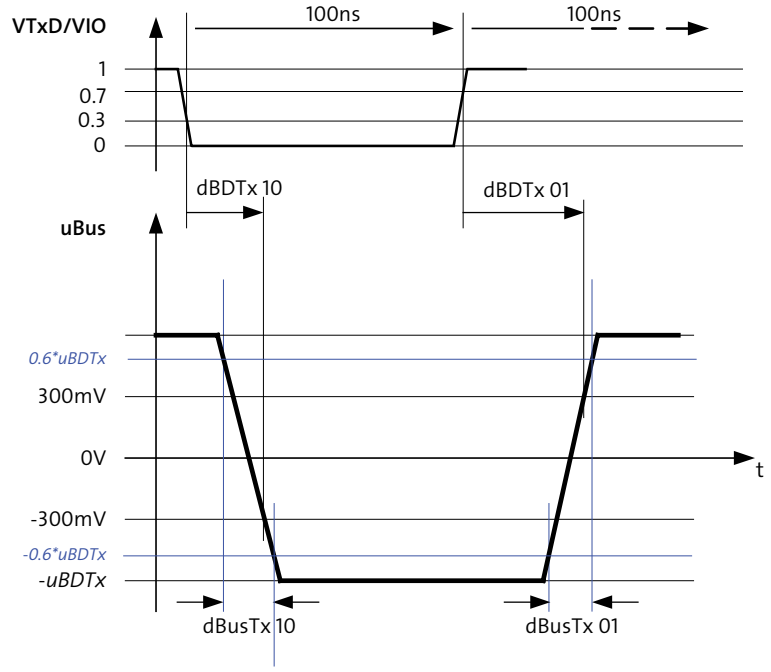


Figure 12: Transmitter characteristics

Fig. 12 shows the situation at the start and the end of the transmission. It is assumed that TxD is low (if TxD was high, the differential bus voltage would be positive). The numerical values are defined in chapter 3.4.2.

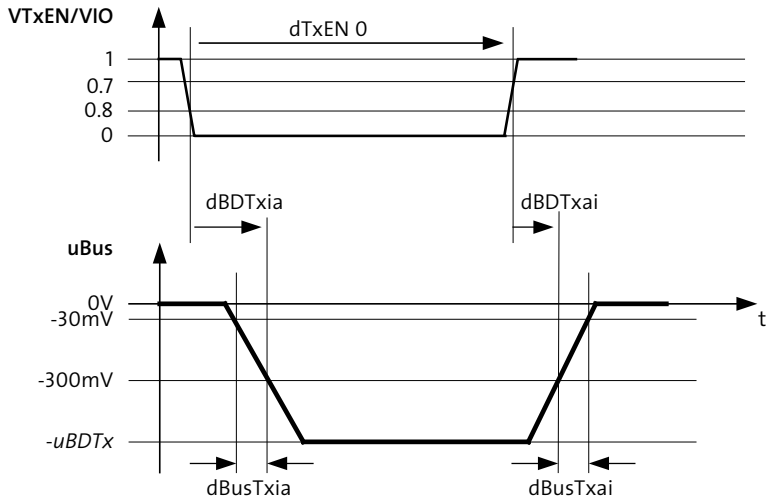


Figure 13: Transmitter timing characteristics

4.2.6 Failure Detection and Storage

4.2.6.1 Undervoltages and Overtemperature

The voltage monitor for VCC and VIO and the overtemperature detection circuit are parts of the power supply unit and described in chapter 4.2.2. The undervoltage and overtemperature failure bits are digitally debounced and stored in the failure register. The content of the register is transferred to the host via SPI.

4.2.6.2 Interface failure detection

Failures at the bus lines (short circuits to the ground, to the supply, BP to BM, lost connections and faulty termination resistors) as well as at the host or communication controller interfaces are detected and sent to host via SPI.

4.2.6.3 List of conditions, bus driver actions and signaling

No.	Fault description	Behaviour of the IC	Message
1	BD is without any supply voltage	High impedance at BP and BM	INTN permanently LOW SDO permanently LOW
2	Undervoltage on all supply voltages	High impedance at BP and BM	INTN permanently LOW SDO permanently LOW
3	BD looses connection to channel (BP and BM interrupted)	BD detects uBus at the channel which is too high	INTN changes to LOW Error flag ULOAD=1 in SPI register
4	BP line shorted to GND	BD limits the output current	INTN changes to LOW Error flag BP2GND=1 in SPI
5	BP line shorted to VSUP	BD limits the output current	INTN changes to LOW Error flag BP2VSUP=1 in SPI register
6	BM line shorted to GND	BD limits the output current	INTN changes to LOW Error flag BM2GND=1 in SPI
7	BM line shorted to VSUP	BD limits the output current	INTN changes to LOW Error flag BM2VSUP=1 in SPI register
8	BP line shorted to BM line	BD limits the output current	INTN changes to LOW Error flag OLOAD=1 in SPI register.
9	Defect of the error signaling lines INTN interrupted		No detection by BD itself. Software plausibility check with corresponding SPI failure bits.
10	Defect of the error signaling lines. INTN shorted to GND		No detection by BD itself. Software plausibility check. Comparison of the INTN level with SPI failure flags. Failure flag reset.
11	Defect of the error signaling lines. SPI lines interrupted		No detection by BD itself. Software plausibility check.

No.	Fault description	Behaviour of the IC	Message
12	Defect of the error signaling lines. SPI shorted to GND		No detection by BD itself. Software plausibility check. Analysis of the SPI response e.g. 0x0000.
13	Defect of the error signaling lines. INTN shorted to VIO or VCC		No detection by BD itself. Software plausibility check. Comparison of the INTN level with SPI failure flags.
14	TxD line becomes interrupted	BD outputs Data_0, when enabled via TxEN (internal pull down resistor)	No detection by BD itself. CC error at the receiving ECU
15	TxEN line becomes interrupted	BD outputs idle state to the channel (internal pull up resistor)	No detection by BD itself. CC error at the receiving ECU
16	TxEN signal is permanently low (“babbling idiot”)	After a timeout dTOTxEN the BD outputs idle state to the channel	After timeout (dTOTxEN) the BD sets INTN to ‘low’ and sets the bit ‘TxENLOW’=1 in the SPI register
17	BD detects an overtemperature condition	BD outputs idle state to the channel	INTN changes to LOW OTEMP=1 in SPI register
18	Bus load too low (i.e. one of two line termination units becomes disconnected from the channel)	Note: Depending on application communication will fail or might continue with degraded performance	See 3
19	Bus load too high	Note: Depending on application communication will fail or might continue with degraded performance	See 8
20	Undervoltage on VIO (VCC available)	BD outputs idle state to the channel	BD changes to BD_Standby. No data sending or receiving possible.

4.2.6.4 Bus failure detection methods

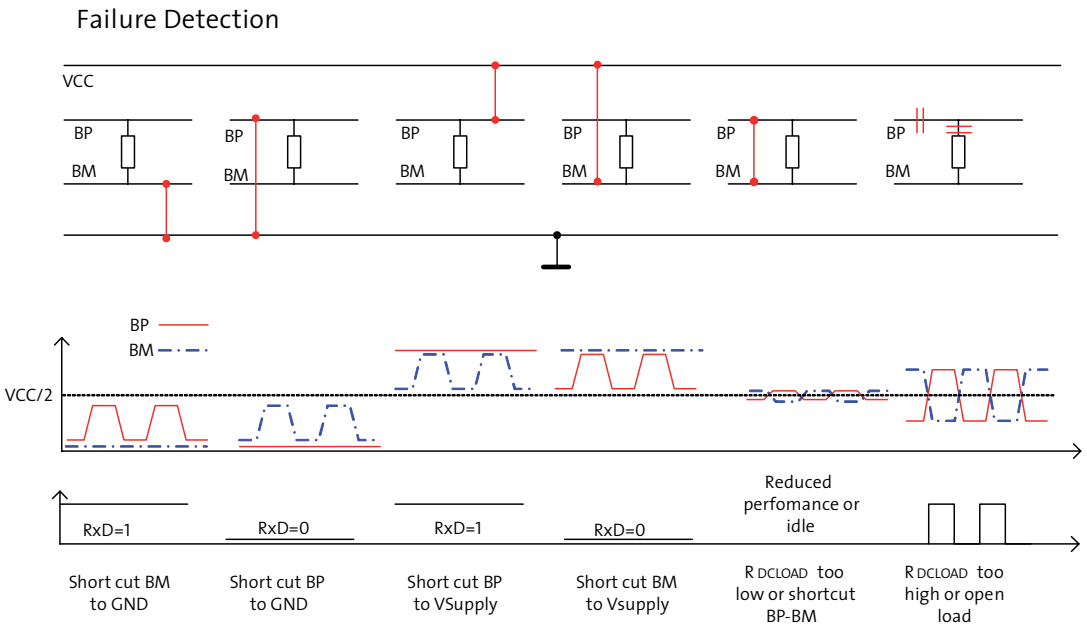


Figure 14: Possible bus failures

Fig. 14 shows the simplified diagrams of several failures of the bus lines (short circuits BP, BM to ground BP2GND, BM2GND, or to Vsupply BP2VSUP, BM2VSUP as well as bus loads which are too low or too high).The error flags are stored in the error register. Its value is read by the host microcontroller via SPI (see chapter 4.3.4).
The bus failure detection needs transmitted frames. It starts with the beginning of the transmission and it is realized within a certain number of frames sent by the transmitter. The failure detection procedure depends on the length of the Data_0 and Data_1 sequences, the resistances of the short circuits and the values of the stray inductances of common mode chokes. Large stray inductances (a few 100nH until 1µH) may prevent to recognize the bus voltages uBP and uBM during the bit times. Thus several FlexRay frames are necessary to get a valid result of the measurement. High supply voltages and very low short circuit resistances may prevent to distinguish between BP2VSUP and BM2VSUP exactly.
Furthermore, a ground shift between the nodes may be recognized as short circuit, especially if the transmitter needs a longer time to set the common mode bus voltage to its steady state value. This may occur if a split termination with capacitors in the range of nF is used.

5 ISO7637 pulse test implementation

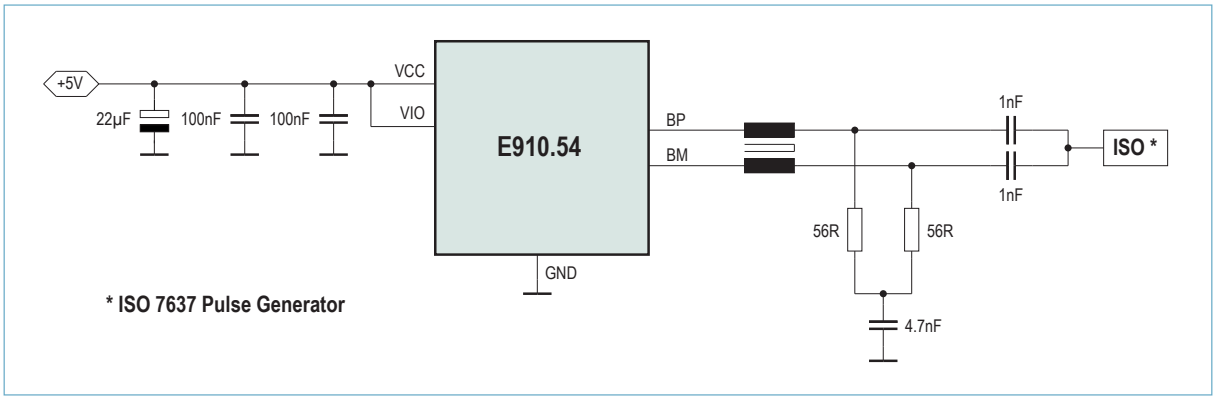


Figure 15: ISO7637 pulse test implementation

6 Package

6.1 Package outline

E910.54 package: **TSSOP14**
Package reference: **According to JEDEC MO-153-F, version AB-1**

ELMOS packages meet the requirements of the latest JEDEC outline specifications. All JEDEC outline specifications may be freely downloaded from *http://www.jedec.org* or please contact your local ELMOS key account manager.

6.2 Marking

6.2.1 Top side

9 1 0 5 4 X
X X Z Y W W
E L M

X	IC revision
XX	Lot number
Z	Assembler code
Y	Year of fabrication
WW	Week of fabrication
ELM	ELMOS abbreviation

6.2.2 Bottom side

No marking

6.3 RoHS conformance

As result of the RoHS Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 (effective July 1st, 2006) on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS), today, all ELMOS devices meet the proposed RoHS components for cadmium, mercury, hexavalent chromium, polybrominated biphenyls (PBBs), and polybrominated diphenyl ethers (PBDEs). The compound of ELMOS devices do not contain halogens (including bromine) and inorganic (red) phosphorous as an alternative flame-retardant system.
Note, this status depends on the current understanding of RoHS and ELMOS knowledge of the materials which were used for assembly.

Abbreviations

AS	Active Star
ASIC	Application Specific Integrated Circuit
ASSP	Application Specific Standard Product
BD	Bus Driver
BM	Bus Minus
BP	Bus Plus
CC	Communication Controller
CERCAP	Ceramic Capacitor
CMC	Common Mode Choke
ECU	Electronic Control Unit
ELCAP	Electrolytic Capacitor
ESR	Equivalent Series Resistance
IC	Integrated Circuit
KL15	Clamp 15 switched battery supply (German: Klemme 15)
KL30	Clamp 30 permanent battery supply (German: Klemme 30)
LWU	Local Wake-up
OEM	Original Equipment Manufacturer (car maker)
RWU	Remote Wake-up
WUS	Wake-up Symbol
WUP	Wake-up Pattern
SPI	Serial Peripheral Interface
TSS	Transmission Start Sequence

Contact

In case of any application related or general technical questions please contact **application-support@elmos.eu**.
In all other cases **info@elmos.de** or:

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