IO-Link

ELMOS is a member of the IO-Link consortium

Dual IO-Link Master Transceiver with UARTS E981.12

RoHS compliant

ADVANCE PRODUCT INFORMATION - JUL 26, 2011

Features

- 2-port IO-Link Master
- Integrated UART-Interface for each port
- Output drivers with typical 1 Ω
- Supporting external PMOS switches for IO-Link supply (L+) with current limitation
- Wake-up generation support
- Supply voltage range
  V_{DDH}: 8V – 32V / V_{DD}: 3.15V - 3.45V
- Over-current & short-circuit protection at output stages with configurable thresholds
- Digital inputs configurable for IO-LINK or IEC 61131-2 compatible interface
- SPI interface for communication, configuration, and diagnosis
- Under voltage monitor for all supplies
- Over temperature protection

Applications

- IO-Link Master application in modular SPS
- Gateway applications

Brief Functional Description

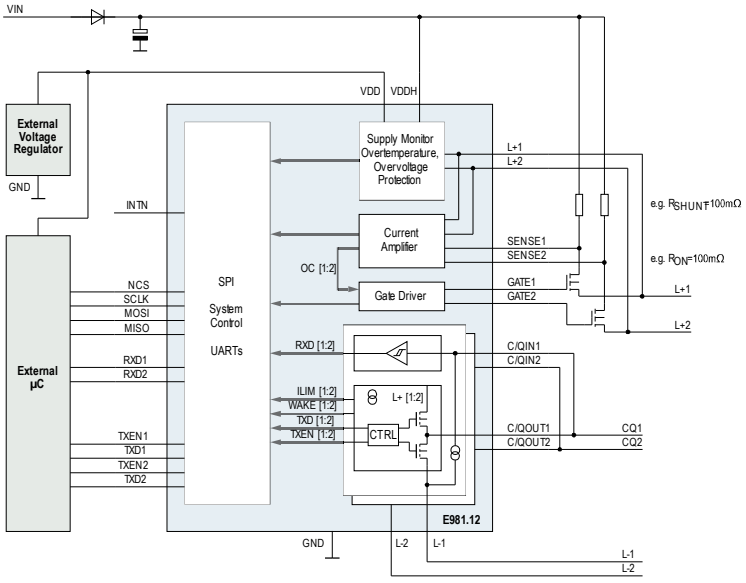
This device comes with two independently operating IO-Link MASTER PHYs which make it a perfect fit for 2/4/8/16-port Master applications. Especially for multi-port applications the integrated UARTs offer you high flexibility regarding scalability of Master ports and the choice of the µC used for the application. As the E981.12 allows the support of external MOSFETs for sensor supply, it enables cost-effective and power dissipation optimized system concepts.

The dual IO-Link Master is also available as SIP at RENESAS with embedded microcontroller for protocol handling.

Ordering Information

Product ID	Temp. Range	Package
E981.12	-40°C to +105°C	QFN44L7

Typical Application



This document contains information on a new product. ELMOS Semiconductor AG reserves the right to change specifications and information herein without notice.

1 Package and Pinout

1.1 Pin Description Dual IO-Link Master

No	*Name*	*Type*	*Description*
1	SENSE_L1	HV_A_I	Supply current sense input channel 1
2	DR_L1	HV_A_O	PMOS Gate control output channel 1
3	L1	HV_S	Transceiver supply input channel 1
4	CQ_OUT1	HV_A_O	Transmitter output channel 1
5	CQ_IN1	HV_A_I	Receiver / general purpose input channel 1
6	PGND1	HV_S	Power ground channel 1
7	PGND 2	HV_S	Power ground channel 2
8	CQ_IN2	HV_A_I	Receiver / general purpose input channel 2
9	CQ_OUT2	HV_A_O	Transmitter output channel 2
10	L2	HV_S	Transceiver supply input channel 2
11	DR_L2	HV_A_O	PMOS Gate control output channel 2
12	SENSE_L2	HV_A_I	Supply current sense input channel 2
13	GND	S	System ground
14	i.c.		Internally connected. For factory use only. Connect to GND in application
15	SCSN	D_I	SPI chip select input
16	SCLK	D_I	SPI serial clock input
17	MOSI	D_I	SPI master output slave input (data input)
18	MISO	D_O	SPI master input slave output (data output)
19	GND	S	System ground
20	VDD	S	3.3V voltage supply
21	n.c.		not connected
22	n.c.		not connected
23	n.c.		not connected
24	TXEN2	D_I	Transmitter enable channel 2
25	TXD2	D_I	Transmitter input channel 2
26	RXD2	D_O	Receiver output channel 2
27	VDD	S	3.3V voltage supply
28	GND	S	System ground
29	INTN	D_O	Interrupt output (low active)
30	TXD1	D_I	Transmitter input channel 1
31	RXD1	D_O	Receiver output channel 1
32	TXEN1	D_I	Transmitter enable channel 1
33	n.c.		not connected
34	n.c.		not connected
35	n.c.		not connected
36	n.c.		not connected
37	CLK_OUT	D_O	Clock output port
38	VDD	S	3.3V voltage supply
39	GND	S	System ground
40	XTAL_OUT	D_O	external quartz
41	XTAL_IN	D_I	external quartz

No	Name	Type	Description
42	i.c.		Internally connected. For factory use only. To be left open in application
43	n.c.		not connected
44	VDDH	S	High-voltage supply input

A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

Table 1: Pin Description

1.2 Package Reference

The device is assembled in a 7x7 mm Quad Flat Non Leaded Package with 44 pins (QFN44L7) in accordance to JEDEC standard MO-220-K, version VKKD-3.

1.3 Package Pinout

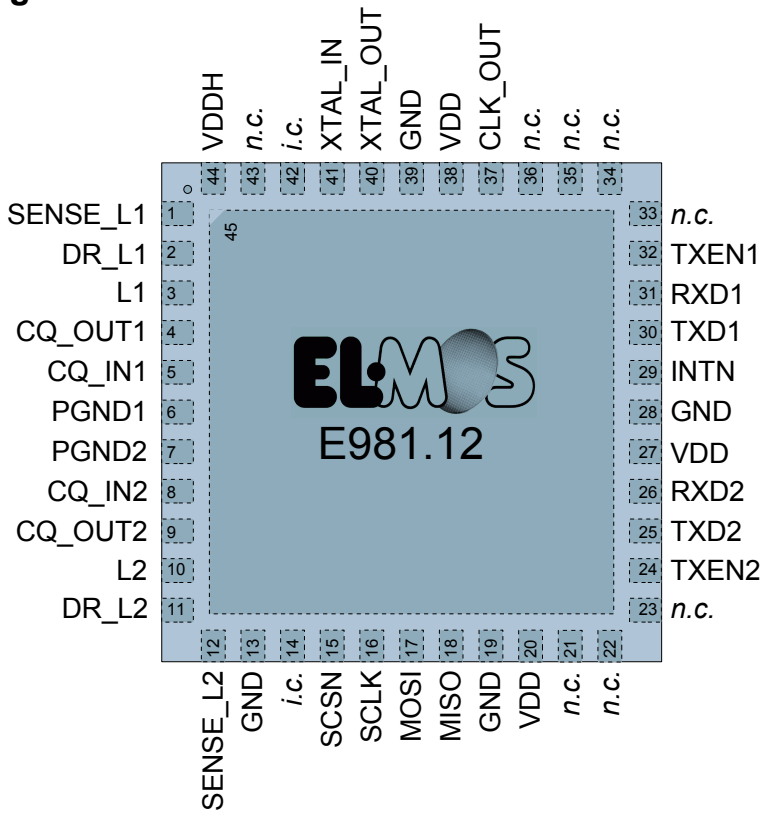


Fig. 1: Package Pinout Diagram QFN44L7

Note: Thermal package rating and electrical parameters include soldering the exposed pad to GND.

2 Block Diagram

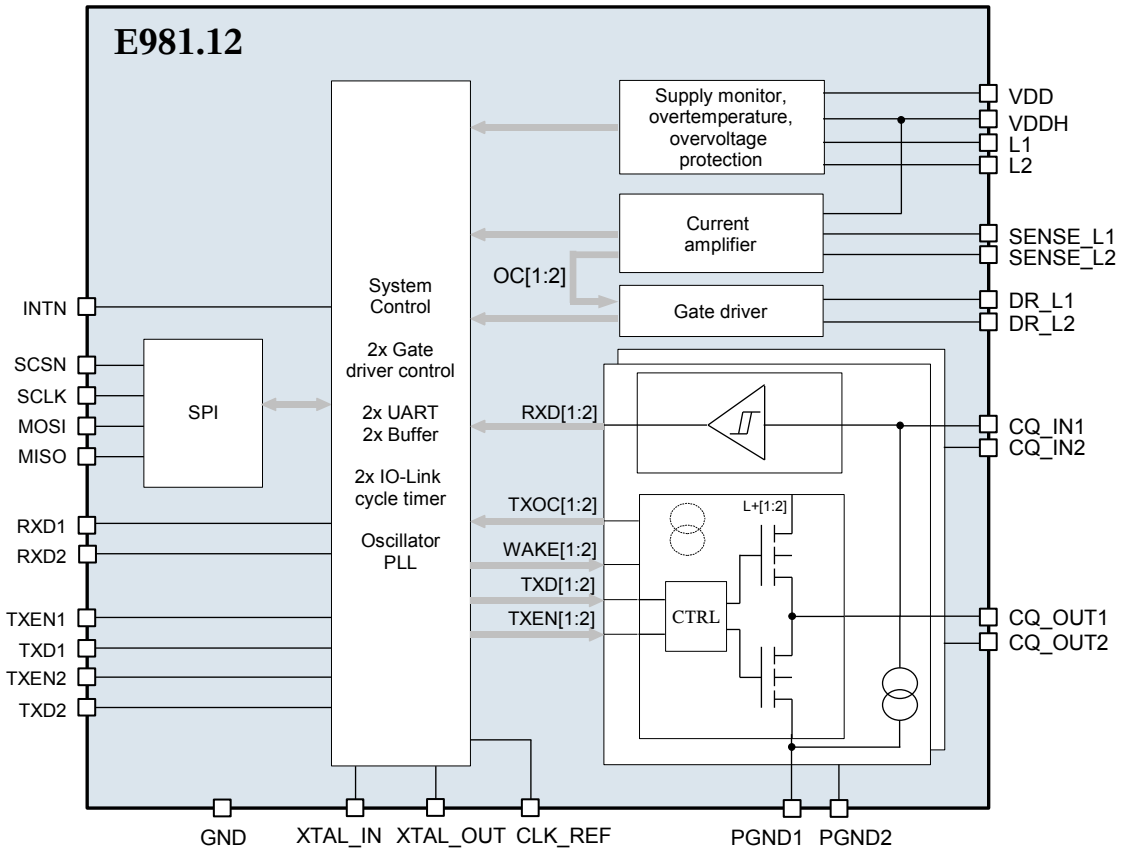


Fig. 2: Block Diagram Dual Master

3 Operating Conditions

3.1 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied.
Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
All voltages referred to ground (GND). Currents flowing into terminals are signed as positive, those drawn out of a terminal are negative.
PGND1, PGND2, GND1 and the package exposed pad must be soldered to the same GND potential.

Description	*Condition*	*Symbol*	*Min*	*Max*	*Unit*
DC voltage at pin VDDH	continuous	V_{SUP}	-0.3	40	V
Transient voltage at pin VDDH (ESD, burst, surge)	t < 500us	$V_{SUP,trans}$	-0.3	60	V
DC input voltage at pins CQ_INx	continuous	$V_{CQ\_IN\_dc}$	-5	40	V
DC input voltage at pins CQ_OUTx	continuous	$V_{CQ\_OUT\_dc}$	-0.3	V_{DDH} +0.3	V
DC voltage at pins Lx, SENSE_Lx, DR_Lx	continuous	V_{L_CTRL}	-0.3	V +0.3	V
Synchronous transient voltage at pins CQ_OUTx and Lx	t < 500us	$V_{L\_CTRL,trans}$	-0.3	60	V
Continuous DC voltage at VDD	continuous	V_{VDD}	-0.3	3.6	V
Voltage range for digital interface pins RXDx, TXDx, TXENx, INTN, MISO, MOSI, SCLK, SCSN	continuous	V_{IF}	-0.3	V_{DD} +0.3	V
Maximum IO current at each pin, if not specified otherwise		I_{IO_LUP}	-10	10	mA
Junction temperature	continuous	T_J		150	°C
Storage temperature		T_{STG}	-40	150	°C
ESD protection at pins CQ_OUTx and CQ_INx	AEC-Q100-002 R=1.5kΩ, C=100pF chip level test	$V_{CQ\_ESD\_HBM}$	6		kV
ESD protection at pin VDDH	AEC-Q100-002 R=1.5kΩ, C=100pF chip level test	$V_{VDDH\_ESD\_HBM}$	6		kV
ESD protection at pins CQ_OUTx and CQ_INx	IEC 61000-4-2 R=330Ω, C=150pF	V_{CQ_ESD}	6		kV
ESD protection at pin VDDH	IEC 61000-4-2 R=330Ω, C=150pF	V_{VDDH_ESD}	6		kV
ESD protection at all other pins	AEC-Q100-002 R=1.5kΩ, C=100pF chip level test	$V_{pin\_ESD\_HBM}$	2		kV

Table 2: Absolute Maximum Ratings

3.2 Recommended Operating Conditions

Within the recommended operating conditions the IC operates as described in the functional description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Supply voltage at pin VDDH	SIO Mode	V_{DDH}	8	24	32	V
Supply voltage at pin VDDH for IOLINK communication	IO_Link Mode	V_{DDH}	18	24	32	V
Supply voltage at pin VDD		V_{DD}	3.15	3.3	3.45	V
Operating ambient temperature range		T_{OP}	-40		105	°C

Table 3: Recommended Operating Conditions

4 Thermal Characteristics

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Thermal resistance junction to case	QFN44L7 (1)	$R_{TH\_JC\_7\_ABS}$		5		K/W
Thermal resistance junction to ambient, high conductivity	QFN44L7 (1)	$R_{TH\_JAH\_7\_ABS}$		25		K/W

(1) Values are based on multilayer PCB according to JEDEC JESD-51-5.

5 Electrical Characteristics

(V_{DDH} = +8V to +32V for SIO mode, V_{DD}=3.15V to 3.45V, Tamb = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DDH} = +24V, V_{DD} = +3.3V and Tamb = +25°C.
Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Power supplies						
Supply voltage at pin VDDH for SIO mode	SIO mode	V_{supSIO}	8	24	32	V
Supply voltage at pin VDDH for IOLINK communication		$V_{supIOLINK}$	18	24	32	V
Supply voltage at pin VDD		V_{DD}	3.15	3.3	3.45	V
supply current at pin VDDH		I_{DDH}		1.0	2.0	mA
supply current at pin VDD		I_{DD}		3.5	5.5	mA
Supply Monitors						
Under voltage threshold VDDH, L1, L2 to switch-off the transmitters or the external P-FETs		UV_{OFF}	6.5	7	7.5	V
Under voltage monitor threshold at L1 and L2		UV_{IOLINK}	16	17	18	V
Debounce time for under voltage detection at VDDH, L1 and L2		t_{deb_UV}	50		250	µs
VDD undervoltage threshold		V_{DDUV}	2.7		3	V
Hysteresis of VDDUV threshold		$V_{DDUVhyst}$		0.1		V
Debounce time for VDDUV		t_{deb_VDDUV}	50		250	µs
Hysteresis of VDDPOR signal		$V_{DDPORhyst}$		0.1		V
VDDPOR threshold		V_{DDPOR}	2.2		2.7	V
voltage difference between VDDUV threshold and POR		$\Delta(V_{DDUV}$-$V_{DDPOR})$		0.3		V
IO-Link Transmitter						
Driver ON resistance	V(Lx) >14V tested at |Iout| = 200mA	R_{ON}		1	2	Ω
Driver ON resistance at low supply voltage	8V < V(Lx) < 14V tested at |Iout| = 200mA	$R_{ON\_low\_supply}$		2	3	Ω
Over current limitation threshold for CQ_OUT=Low		I_{LIM_L}	550	750	1200	mA
Over current limitation threshold for CQ_OUT=High		I_{LIM_H}	-1200	-750	-550	mA

Electrical Characteristics (continued)

(V_{DDH} = +8V to +32V for SIO mode, V_{DD}=3.15V to 3.45V, Tamb = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DDH} = +24V, V_{DD} = +3.3V and Tamb = +25°C.
Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
first (default) configurable over current limitation threshold for CQ_OUT=Low		$I_{THL\_OFF\_CONF1}$	300	500	700	mA
second configurable over current limitation threshold for CQ_OUT=Low		$I_{THL\_OFF\_CONF2}$	150	250	375	mA
third configurable over current limitation threshold for CQ=Low		$I_{THL\_OFF\_CONF3}$	75	150	225	mA
fourth configurable over current limitation threshold for CQ_OUT=Low		$I_{THL\_OFF\_CONF4}$	40	100	150	mA
first (default) configurable over current limitation threshold for CQ_OUT= High		$I_{THH\_OFF\_CONF1}$	-700	-500	-300	mA
second configurable over current limitation threshold for CQ_OUT=High		$I_{THH\_OFF\_CONF2}$	-375	-250	-150	mA
third configurable over current limitation threshold for CQ_OUT=High		$I_{THH\_OFF\_CONF3}$	-225	-150	-75	mA
fourth configurable over current limitation threshold for CQ_OUT=High		$I_{THH\_OFF\_CONF4}$	-150	-100	-50	mA
Output voltage rise time in fast mode (bit FAST="1" in CH_CFG	C_{load}= 1-5nF, R_{load}=20kΩ to GND, C/Q H/L transition, 10% - 90%	$t_{rhspeed}$	100		896	ns
output voltage rise time in slow mode (bit FAST="0" in CH_CFG)	C_{load}= 1-5nF, R_{load}=20kΩ to GND, C/Q H/L transition, 10% - 90%	$t_{rlspeed}$	0.8		5,2	µs
Output voltage fall time in fast mode (bit FAST="1" in CH_CFG	C_{load}= 1-5nF, R_{load}=20kΩ to GND, C/Q L/H transition, 10% - 90%	$t_{fhspeed}$	100		896	ns
Output voltage fall time in slow mode (bit FAST="0" in CH_CFG)	C_{load}= 1-5nF, R_{load}=20kΩ to GND, C/Q L/H transition, 10% - 90%	$t_{flspeed}$	0.8		5,2	µs

Electrical Characteristics (continued)

(V_{DDH} = +8V to +32V for SIO mode, V_{DD}=3.15V to 3.45V, Tamb = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DDH} = +24V, V_{DD} = +3.3V and Tamb = +25°C.
Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Transmit propagation delay from TXD to CQ_OUT	V(Lx)= 24V bit FAST="0"	t_{pd_lspeed}			4.5	µs
Transmit propagation delay from TXD to CQ_OUT	V(Lx)= 24V bit FAST="1"	t_{pd_hspeed}			1.7	µs
Wake-up pulse duration	Wake-up request	t_{WU}	75	80	85	µs
OFF time after wake-up pulse	wake-up procedure	t_{dOFF_WU}		350	400	µs
ON time with overload		t_{dON_OL}	85	100	115	µs
First OFF time after first ON or wake-up pulse		t_{dOFF1_OL}		200 *t_{dON_OL}		µs
OFF time after overload detection, default value	TDOFF1,2= „00"	$t_{dOFF2\_OL\_CONF1}$		200 *t_{dON_OL}		µs
OFF time after overload detection, configured	TDOFF1,2= „01"	$t_{dOFF2\_OL\_CONF2}$		120 *t_{dON_OL}		µs
OFF time after overload detection, configured	TDOFF1,2= „10"	$t_{dOFF2\_OL\_CONF3}$		64 *t_{dON_OL}		µs
OFF time after overload detection, configured	TDOFF1,2= „11"	$t_{dOFF2\_OL\_CONF4}$		320 *t_{dON_OL}		µs
Debounce time for over current detection		t_{debOL}		15		µs
IO-Link Receiver						
Input threshold high for IEC61131-2 type 2	18V < V_{Lx} < 30V	$V_{THHsIEC2}$	9	10	11	V
Input threshold high for IOLINK and IEC61131-2 type 1	18V < V_{Lx} < 30V	$V_{THHsIOLINK}$	11	12	13	V
Input threshold low	18V < V_{Lx} < 30V	V_{THLs}	8	9	10	V
Input threshold hysteresis for IEC61131-2 type 2	18V < V_{Lx} < 30V	$V_{HYSsIEC2}$	0.5	1	1.5	V
Input threshold hysteresis for IOLINK and IEC61131-2 type 1	18V < V_{Lx} < 30V	V_{HYSs_IOLINK}	2	3	4	V
Receiver input debounce filter time	t_{BIT} depends on BD1/BD0	t_{CQ_deb}		1/9*t_{BIT}		ns
Input pull down current 1 for input IEC61131-2 type 2	PD-Source enabled V_{CQ_INx} > 5 V	I_{pdown1}	6	8	12	mA
Input pull down current 2 for input IEC61131-2 type 2	PD-Source enabled V_{CQ_INx} > 5 V	I_{pdown2}	2	4	7	mA
UART						
UART master tolerance		$UART_{TOL}$			0.1	%
UART receiver detects IDLE after $N_{BIT,IDLE}$ * bit times	at least one byte UART reception before	$N_{BIT,IDLE}$		5		
TRX buffer memory size		n_{MEM}		127		byte

Electrical Characteristics (continued)

(V_{DDH} = +8V to +32V for SIO mode, V_{DD}=3.15V to 3.45V, Tamb = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DDH} = +24V, V_{DD} = +3.3V and Tamb = +25°C.
Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
IO-Link Cycle Timer						
IO-Link Cycle Time	UART of channel enabled	T_{CYC}	0.5		348	ms
Granularity of T_{CYC}	depending on PRSC[1:0]	T_{CYC_STEP}	0.5		4	ms
Low pulse @ pin SCSN for synchronization event	no SCK pulse	t_{IOSYNC}	10			µs
Oscillator						
Internal oscillator frequency		$f_{OSC,INT}$	-5%	8	+5%	MHz
Oscillator frequency accuracy with external quarz	external chrystal 50ppm	$f_{OSC,QUARTZ}$	-0.01%		+0.01%	MHz
PLL						
Internal synchronization clock	Quarz enabled or XTAL_IN insertion	f_{sync}		1.0125		kHz
Synchronization clock frequency applied at pin XTAL_IN	Quarz disabled, XTAL_OUT n.c.	$f_{XTAL,sync}$	-0.02%	f_{sync}	+0.02%	
Frequency of CLK_OUT port, C_{sync}	Output enabled, Quarz enabled	f_{CLK_OUT}	-0.02%	1.0125	+0.02%	kHz
Temperature Monitor						
Shut off over temperature threshold		T_{OT}	150			deg. C
Electrical hysteresis of over-temperature shut-off		T_{OT_hyst}		12		deg. C
Host Interface						
High level input voltage		V_{IH}	0.7*V_{DD}			V
Low level input voltage		V_{IL}			0.3*V_{DD}	V
High level output voltage	Iload=2mA	V_{OH}	0.8*V_{DD}			V
Low level output voltage	Iload=-2mA	V_{OL}			0.2*V_{DD}	V
Input pull-down current	Vpin=V_{DD}	I_{pd}	10		80	uA
Input pull-up current	Vpin=0V	I_{pu}	-80		-10	uA
time between rising edge of SCSN and high impedance at MISO		t_{MISO_Z}			100	ns
MISO data valid time	C_{MISO} < 20 pF	t_{valid}			35	ns
SCK pulsewidth		t_{P_SCK}	125			ns

Electrical Characteristics (continued)

(V_{DDH} = +8V to +32V for SIO mode, V_{DD}=3.15V to 3.45V, Tamb = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DDH} = +24V, V_{DD} = +3.3V and Tamb = +25°C.
Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
time between falling SCSN edge and first rising SCK edge		t_{LS1}	50		2000	ns
time between last falling SCK edge and rising SCSN edge		t_{LS2}	50			ns
inter byte gap relevant for two byte access between address and data byte only		t_{IBG}	550			ns
MOSI data setup time		t_{setup}	30			ns
MOSI data hold time		t_{hold}	20			ns
Number of data bytes during burst access to TRX buffers		$N_{SPI,burst}$	1		127	
IO-Link Supply Control						
Shutdown delay 1 including delay of current regulation	PDR_CFG1 [7:6]=00 Power FET dependent	t_{d_OFF1}		1		ms
Shutdown delay 2 including delay of current regulation	PDR_CFG1 [7:6]=01 Power FET dependent	t_{d_OFF2}		4		ms
Shutdown delay 3 including delay of current regulation	PDR_CFG1 [7:6]=10 Power FET dependent	t_{d_OFF3}		10		ms
Shutdown duration 1	PDR_CFG1 [5:4]=00	t_{OFF1}		5		ms
Shutdown duration 2	PDR_CFG1 [5:4]=01	t_{OFF2}		20		ms
Shutdown duration 3	PDR_CFG1 [5:4]=10	t_{OFF3}		50		ms
Over current detection threshold at shunt resistor		V_{IN_OCCOMP}	60	90	120	mV
Voltage drop across shunt in over current limitation state		V_{IN_OC}	70	100	130	mV
Over current debounce time		t_{deb_OCCOMP}		8		µs
Input current at pin SENSE_Lx	V_{SENSE_Lx}=VDDH	I_{SENSE}	6	10	20	uA
Pull up resistance at Pins DR_L1 and DR_L2 in OFF state	V_{DR_Lx}>V_{DDH} - V_{THR_OFF}	R_{PU_OFFSW}		300	500	Ω

Electrical Characteristics (continued)

(V_{DDH} = +8V to +32V for SIO mode, V_{DD}=3.15V to 3.45V, Tamb = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DDH} = +24V, V_{DD} = +3.3V and Tamb = +25°C.
Positive currents flow into the device pins.)

Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
Output voltage at Pins DR_L1 and DR_L2 to switch external PMOS ON		V_{GATE_min}	V_{DDH}-15	V_{DDH}-12	V_{DDH}-5	V
Output voltage at Pins DR_L1 and DR_L2 to switch external PMOS OFF		V_{GATE_max}	V_{DDH}-0,4	V_{DDH}-0,1	V_{DDH}	V
Threshold V_{DDH}-V_{DR_Lx} for OFF-state detection of external power FET		V_{THR_OFF}	0.8	1.3	1.8	V
Maximum switch-off current for gate of external PMOS	PMOS active V_{DR_L}=V_{DDH} - 4V V_{shunt}=300mV	I_{max_OFF}	-2	-3.8	-7	mA
Switch-on gate current for gate of external PMOS	PMOS active V_{DR_L}=V_{DDH} - 4V V_{shunt}=55mV	I_{min_NORM}	0.5	1	2.5 TBD	mA
Transient response time OFF->ON	PMOS active C_{DR_L}=0.8nF	t_{pd_ON}		10		µs
Transient response time ON->OFF	PMOS active C_{DR_L}=0.8nF	t_{pd_OFF}		10		µs

6 Functional Description

6.1 Power supplies

The device has got four supply input pins:

- VDDH – 24V supply
- L1, L2 – 24V supply for the transceivers
- VDD – 3.3V supply for the digital blocks

VDDH is the general high-voltage supply pin. It supplies an internal low-voltage regulator for safe power up, internal references and the voltage monitors.

Each of the transmitter supply pins L1 and L2 supplies one of the two internal transmitters.
This supply can be controlled by external PMOS transistors. The IC provides the gate voltage for these external transistors and a current monitor to be able to limit the maximum current. If no external current limitated switches are needed the pins L1 and L2 has to be connected to the VDDH supply.

Pin VDD has to be supplied by an external voltage supply with nominal 3.3V. VDD supplies the host interface, the logic block and various other internal blocks. The logic block is set to its initial ("reset") state by a power-on-reset signal, delivered by the VDD monitor.

6.2 Supply Monitor

The supply monitor provides status information of the supply voltages VDD, VDDH, L1 and L2 in SPI register VMON STAT. For each flag an interrupt enable bit (IE) can be configured in register VMON IE. Read access to register VMON STAT will clear the interrupts.

6.2.1 VDDH, L1, L2 Monitor

If the supply voltage at L1 or L2 falls below the UV_{IOLINK} threshold this condition is set in the corresponding SPI register only and an interrupt is generated if configured. The transmitters keep active.

If the supply voltage at L1 or L2 falls below the UV_{OFF} threshold the transmitters are disabled.
If the VDDH supply voltage falls below the UV_{OFF} threshold the external PMOS-FETs are switched-off.

6.2.2 VDD Monitor

If the VDD supply voltage falls below the V_{DDUV} threshold a bit in the register VMON STAT is set. If VDD falls below V_{DDPOR} threshold a power-on-reset is generated.

6.2.3 Status and Control Registers

Register Name	*Address*	*Description*
VMON STAT	0x02	
VMON IE	0x03	

Table 4: Voltage Monitoring Register Table

Register **VMON STAT** (0x02)

	MSB							*LSB*
Content	-	-	-	-	L2UV	L1UV	VDDHUV	VDDUV
Reset value	0	0	0	0	1	1	1	1
Access	R	R	R	R	R	R	R	R
Bit Description	**L2UV** : 1 = Under voltage at L2 **L1UV** : 1 = Under voltage at L1 **VDDHUV** : 1 = Under voltage at VDDH **VDDUV** : 1 = Under voltage at VDD							

Table 5: VMON STAT

Register **VMON IE** (0x03)

	MSB							*LSB*
Content	-	-	-	-	L2IE	L1IE	VDDHIE	VDDIE
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W
Bit Description	**L2IE** : 1 = Interrupt enable L2 **L1IE** : 1 = Interrupt enable L1 **VDDHIE** : 1 = Interrupt enable VDDH **VDDIE** : 1 = Interrupt enable VDD							

Table 6: VMON IE

6.3 IO-Link-Transceiver

The device contains two channels with a high-voltage digital transmitter (output: CQ_OUTx) and receiver (input: CQ_INx). The transmitter and receiver are accessible by both – a parallel interface (TXD, TXEN, RXD) and by SPI in IO-Link or SIO mode. The digital pins are supplied by VDD voltage. The input thresholds and output levels are referenced to this voltage.

It can be used in the following ways:
a) CQ_OUTx is used as standard output (SIO) to drive ohmic loads, inductive loads or bulb lamps
b) CQ_INx is used as standard digital input type 2 according to IEC 61131-2
c) CQ_OUTx and CQ_INx are used together as IO-LINK port for data transfer rates of 4,8 kBaud, 38,4 kBaud or 230,4 kBaud.

6.3.1 IO-Link-Transmitter

The push-pull transmitter is activated with high level on pin TXEN and drives the CQ_OUT pin Low or High in accordance to the inverted logic level on pin TXD. A slope control limits EMC emission.

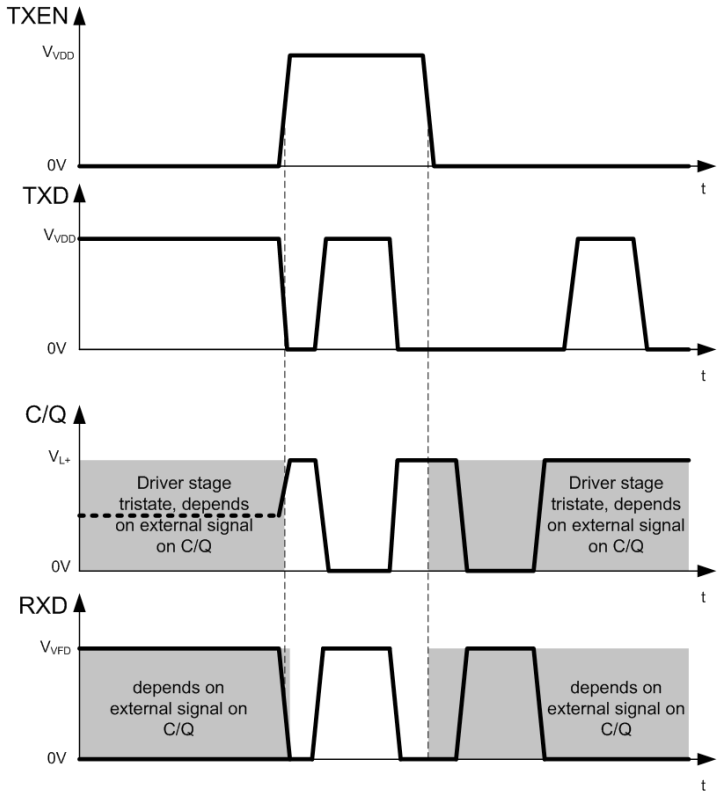


Fig. 3: Transmitter polarity

The transition times can be set for two different slope modes using register CH CFG. The transmitter is operable only if VDD, L+ and chip temperature are within their specified limits. Otherwise the transmitter is disabled.

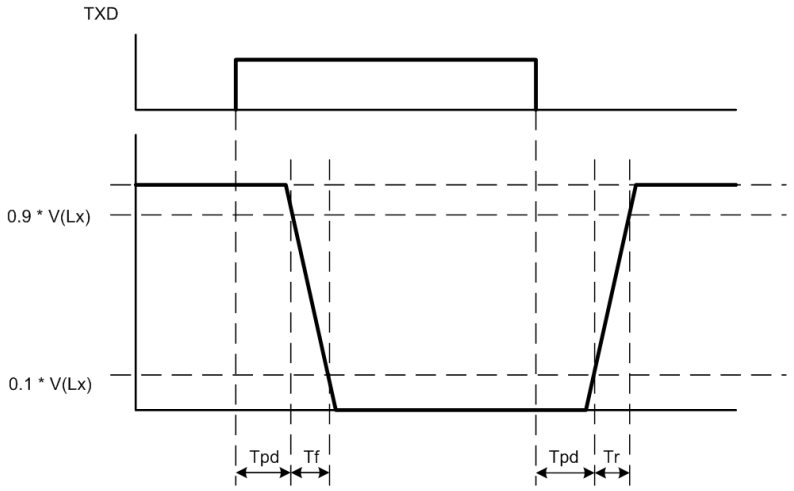


Fig. 4: Transmitter characteristics

6.3.1.1 Transmitter Overload

In case of high power dissipation (e.g. due to short circuit of the driver) the chip temperature will increase. To protect the device, an internal over temperature sensor for each driver is implemented. In case of over temperature, the affected driver is disabled. The other output driver can operate independently.

The transmitters are switched on after a the over temperature condition disappeared. The over temperature flag is set in CH STAT, to generate an interrupt use bit **OTIE** in TRX CFG

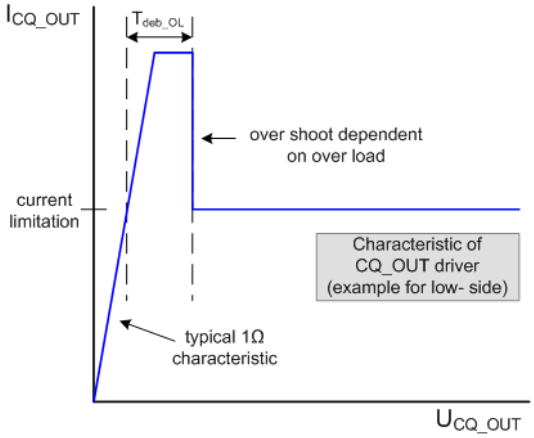


Fig. 5: Transmitter characteristics at overload

In case of an over current is detected directly after the transmitter is activated by setting the pin TXEN to high (or Bit STXEN=1), the output current is limited to an over current threshold I_{LIM_x}. The transmitter remains active for $T_{dON\_OL.}$ After this time the transmitter is disabled for $T_{dOFF1\_OL.}$ After this first sequence a cyclic overcurrent shutdown with a configurable current limitation ($I_{THx\_OFF\_CONFx}$) and dutycycle (T_{dON_OL} / $T_{dOFF2\_OL\_CONFx}$) is implemented (see Fig. 6).

The configured dutycycle must not exceed the power dissipation limits of the device.

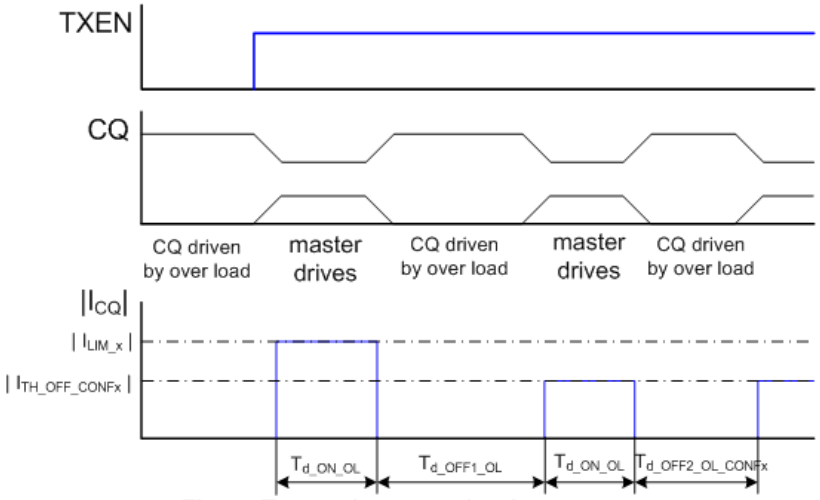


Fig. 6: Transmitter over load sequence

If an overload occurs while the transmitter was already active, it will turn off immediately after a debounce time T_{deb_OL} for $T_{d\_Off2\_OL}$, followed by the sequence described above using off times $T_{d\_Off2\_OL\_confx}$ (see Fig. 7).

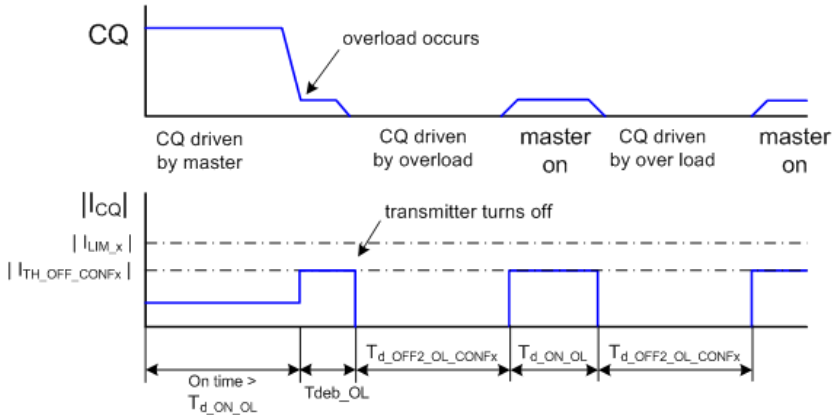


Fig. 7: Over load while driver was already active

6.3.1.2 Transmitter Loads

In SIO mode the external load at CQ_OUT may have resistive, capacitive or inductive characteristic or can be a bulb lamp. The loads can be connected between CQ_OUTx and Lx or between CQ_OUTx and PGNDx.

It is possible to switch the load in the following ways:

TXEN = constant High, switching with TXD

In this case CQ_OUT is driven as push-pull output.
TXD = Low: high-side driver active
TXD = High: low-side driver active

In case of inductive loads the complemantary driver acts as free-wheeling element.

TXD constant, switching with TXEN

In this case the high-side driver (if TXD = Low) or the low-side driver (if TXD = High) is used, so the load is switched either between " Active Low" and "Tristate" or between "Active High" and "Tristate".
In case of inductive loads inherent diodes of the drivers act as free-wheeling elements.

6.3.2 IOLINK-Receiver

The receiver converts the voltage level at the CQ_IN pin to an inverted logic receive signal which is available at pin RXD and the internal UART. The receiver filter times depends on the configured baudrate. The receiver functionality is available in the specified IO-Link supply range.

The receiver can be configured by bit IEC-2 in TRX CFG either as standard IO-LINK / IEC61131-2 input or as standard IEC61131-1 input.

The input current source can be activated by bit PDEN in register TRX CFG. Setting bit PDAUTO the current source is disabled while the driver stage is active during SIO mode or communication mode (TXEN=1) in order to reduce power dissipation.

6.3.3 SIO-Mode

Each C/Q channel can be used as an input or output, while the output can be configured to switch between high side, low side and HiZ.

SIO mode can be used by pins TXEN, TXD, RXD or by SPI control. The mode can be configured by register CH_CFG. If bit SIO is set to „1“ the output control is done by SPI access to register TRX_CFG bits STXD and STXEN. The receiver status can be read by register CH_STAT bit RXD.

6.3.4 Transceiver UART

The IO-Link Master IC has two integrated UART interfaces. The UART provides the media access and bit decoding / encoding and byte framing capabilities as well. UART timing accuracy of 0.1% depends on the oscillatior configuration described in chapter „Oscillator“.

UART mode is activated by SPI register CH_CFG bit UART. For UART mode the bit „SIO“ has to be „0“. The UART baudrate has to be configured in register CH_CFG independently for each channel.

The UART byte frame consists of:
- one start bit (value "0")
- eight data bits (LSB first)
- an even parity bit and
- one stop bit (value "1").

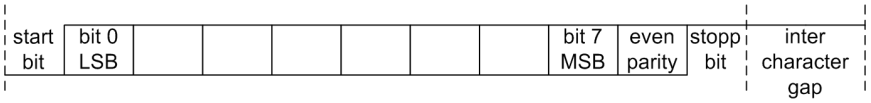


Fig. 8: Uart byte frame

Transmission and receive is controlled by the integrated IO-Link cycle timer. For UART communication the internal cycle timer must be configured and enabled (see chapter „IO-Link cycle timer“).

Each received byte is checked for correct parity and right framing (stop bit). In case of receive errors the corresponding error flags are set in register RX_STAT and TIM STAT.

The E981.12 provides a 127 byte shared TRX buffer to store transmit and receive frames.
The number of bytes to be transmitted and received must be configured in register UART_TXNUM and UART_RXNUM. As soon as the configured number of bytes was successfully send and the response was received bit RDY in register TIM_STAT is set. Optionally an interrupt can be enabled by RDYIE in register TIM_IE.

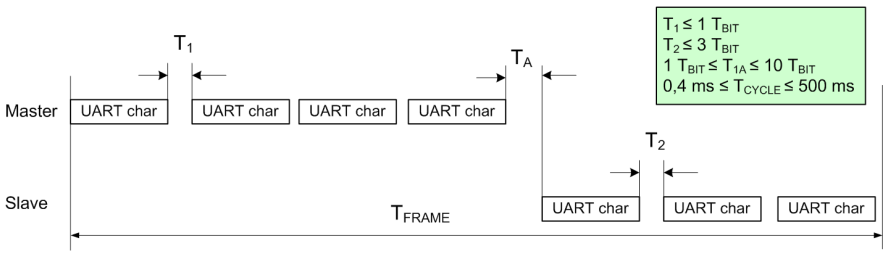


Fig. 9: IO-Link frame and cycle timing

If no further UART characters are observed for longer than T_2, IDLE is detected. If the number of received characters differs from the value in UART_RXNUM (as well as no reception at all was observed), the error flag NUME will be set in register TIM_STAT. Optionally an interrupt can be enabled by NUMIE in register TIM IE. The interrupt is cleared by read access to TIM STAT.

6.3.4.1 Host - PHY Communication

The timing diagram in Fig. 10 shows the communication between host microcontroller and IO-Link Master TRX buffer within one cycle when using the internal UARTs. Before writing or reading the corresponding buffer the UART hast to be enabled.

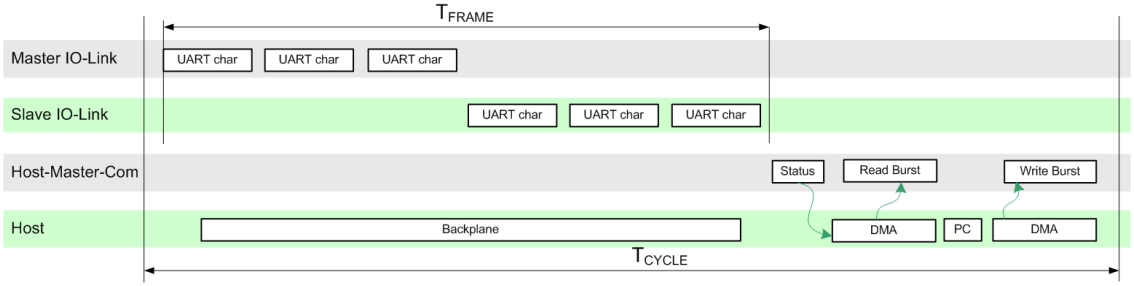


Fig. 10: Host-PHY communication

After reading the response frame of the current cycle the host has to write the master frame for the next cycle to be transmitted before the current cycle has been ended. The buffered IO-Link master frame is sent by E981.12 starting with the next communication cycle (see chapter „IO-Link cycle timer“). The host microcontroller has to ensure to fill the TRX buffer with the master frame before the next cycle starts. If the TRX buffer access is not finished till the next cycle start (cycle boundary violation), the transmission is started delayed.

The TX bytes written to the TRX buffer by SPI are checked by XOR checksum. If the checksum fails the E981.12 does not transmit data in the next cycle.
The TRX buffer access is implemented as SPI burst access to reduce the SPI communication overhead (see Chapter SPI Interface).

burst write access to TRx buffer

	MOSI								MISO							
byte 1	0	1	0	0	B3	B2	B1	B0	0	0	0	0	0	0	0	0
	write	burst			buffer[3:0]											
byte 2	0	N6	N5	N4	N3	N2	N1	N0	0	1	0	0	B3	B2	B1	B0
		bytenum[6:0]							command							
byte 3	D7	D6	D5	D4	D3	D2	D1	D0	0	N6	N5	N4	N3	N2	N1	N0
	data0									bytenum						
byte 4	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
	data1								data0							
...	...								...							
byte N+2	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
	dataN-1								dataN-2							
byte N+3	X7	X6	X5	X4	X3	X2	X1	X0	D7	D6	D5	D4	D3	D2	D1	D0
	xor_byte								dataN-1							

Fig. 11: UART buffer burst write access

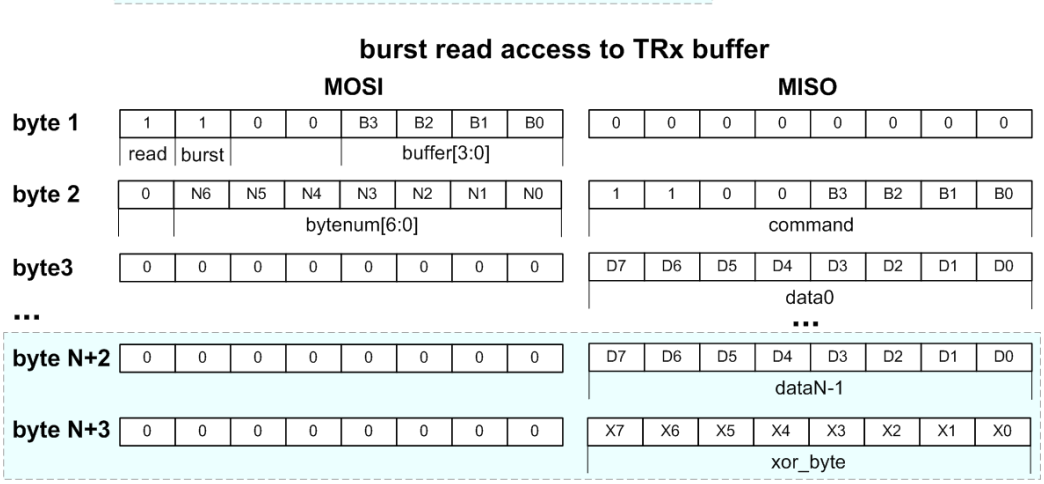


Fig. 12: UART buffer burst read access

The buffer is selected by bits [B3:B0]. Channel 1 is selected by 0x5 (0101b). The buffer for channel 2 is selected by 0xA (1010b).

This buffer selection code must not be interpreted as starting address. The buffer read or write access always starts with data byte 0. It is not needed to read or write all 127 bytes. The application has to ensure that the buffer content matches to the number of bytes to be transmitted in register UART_TXNUM.

For further information about SPI access see chapter SPI Interface.

6.3.5 Channel Status and Configuration Registers

Register Name	*Address*	*Description*
Channel 1		
CH CFG	0x10	Channel 1 configuration
CH STAT	0x11	Channel 1 status and error register
TRX CFG	0x12	Transceiver config channel 1
TX OCCFG	0x13	Transmitter over current configuration register channel 1
UART TXNUM	0x14	Number of Bytes for TX channel 1
UART RXNUM	0x15	Number of Bytes for RX channel 1
RX STAT	0x1A	Receiver status and error register channel 1
Channel 2		
CH CFG	0x20	Channel 2 configuration
CH STAT	0x21	Channel 2 status and error register
TRX CFG	0x22	Transceiver config channel 2
TX OCCFG	0x23	Transmitter over current configuration register channel 2
UART TXNUM	0x24	Number of Bytes for TX channel 2
UART RXNUM	0x25	Number of Bytes for RX channel 2
RX STAT	0x2A	Receiver status and error register channel 2

Table 7: Transceiver Register Table

Register **CH CFG**
Channel 1 (0x10)
Channel 2 (0x20)

	MSB							*LSB*
Content	-	FAST	BD1	BD0	-	-	SIO	UART
Reset value	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R	R	R/W	R/W
Bit Description	**FAST** : Transmitter slope control 1 = fast slopes **BD1 / BD0** : Baud rate selection and receiver filter configuration 00 = 4.8 kBaud 01 = 38.4 kBaud 10 = 230.4 kBaud 11 = analog mode (TXEN, TXD, RXD is used for communication) **SIO** : 1 = SIO Mode with register values 0 = SIO with TXEN, TXD, RXD **UART** : 1 = internal UART is used if bit „SIO“ is not set to „1“ (SIO has priority) 0 = UART disabled (TXEN, TXD, RXD is used for communication)							

Table 8: Channel configuration

Register **CH STAT**
Channel 1 (0x11)
Channel 2 (0x21)

	MSB							***LSB***
Content	-	-	-	-	TXOC	TXOT	-	RXD
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**TXOC** : 1 = Transmitter Overcurrent detected, cleared by read access **TXOT** : 1 = Transmitter Over Temp. detected, cleared by read access **RXD** : 1 = Current value of filtered receiver status							

Table 9: Channel status and error register

Register **TRX CFG**
Channel 1 (0x12)
Channel 2 (0x22)

	MSB							***LSB***
Content	IEC-2	IPD	PDAUTO	PDEN	OCIE	OTIE	STXD	STXEN
Reset value	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	RR/W	R/W	R/W	R/W	RR/W
Bit Description	**IEC-2** : 1 = Receiver threshold for input IEC61131-2 type 2 0 = Receiver threshold for IO-Link communication **IPD** : 1 = Receiver channel 1 pull down current 1 I_{pdown1} 0 = Receiver channel 1 pull down current 2 I_{pdown2} **PDAUTO** : 1 = automatic control of Receiver pull down source 0 = Receiver channel 1 pull down controlled by PDEN **PDEN** : 1 = Receiver channel 1 pull down enabled 0 = Receiver channel 1 pull down disabled **OCIE** : 1 = Over Current IRQ enable **OTIE** : 1 = Over Temp IRQ enable **STXD** : 1 = LS active (in SIO mode only) 0 = HS active (in SIO mode only) **STXEN** : 1 = Transmitter enabled (in SIO mode only)							

Table 10: Transceiver config

Register **TX OCCFG**
Channel 1 (0x13)
Channel 2 (0x23)

	MSB							***LSB***
Content	-	-	TDOFF1	TDOFF0	-	DISOCTH	OCTHR1	OCTHR0
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R	R/W	R/W	R/W
Bit Description	**TDOFF1 / TDOFF0** : configuration for $Td_{OFF2\_OL\_CONFx}$ 00 = $T_{dOFF2\_OL\_CONF1}$ 01 = $T_{dOFF2\_OL\_CONF2}$ 10 = $T_{dOFF2\_OL\_CONF3}$ 11 = $T_{dOFF2\_OL\_CONF4}$ **DISOCTH** : 1 = Disable over current threshold configuration with OCTHR[1:0], threshold ILIM_H/L valid **OCTHR1/OCTHR0**: configuration of Over current threshold $I_{THx\_OFF\_CONFx}$ 00 = $I_{THx\_OFF\_CONF1}$ 01 = $I_{THx\_OFF\_CONF2}$ 10 = $I_{THx\_OFF\_CONF3}$ 11 = $I_{THx\_OFF\_CONF4}$							

Table 11: Transmitter over current configuration register

Register **UART TXNUM**
Channel 1 (0x14)
Channel 2 (0x24)

	MSB							***LSB***
Content	-	NUM6	NUM5	NUM4	NUM3	NUM2	NUM1	NUM0
Reset value	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**NUM6 .. NUM0** : Number of Bytes to be transmitted							

Table 12: Number of Bytes for TX

Register **UART RXNUM**
Channel 1 (0x15)
Channel 2 (0x25)

	MSB							***LSB***
Content	-	NUM6	NUM5	NUM4	NUM3	NUM2	NUM1	NUM0
Reset value	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**NUM6 .. NUM0**: Number of Bytes to be received							

Table 13: Number of Bytes for RX

Register **RX STAT**
Channel 1 (0x1A)
Channel 2 (0x2A)

	MSB							***LSB***
Content	-	-	-	-	-	-	FE	PE
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**FE** : 1 = Framing error (no stop bit), cleared by read access **PE** : 1 = Parity error, cleared by read access							

Table 14: Receiver status and error register

6.3.6 IO-Link Cycle Timer

The IO-Link cycle timer generates the communication cycle. It can be configured in range of 0.4 ms up to 132.8 ms in register TIM_PER. The cycle time is configured by selecting one range out of three as shown in Table 15.

PRSC[1:0]	T_{CYC_STEP}	T_{CYC_OFFSET}	T_{CYC}
00b	0.1 ms	N.A.	0.4 ... 6.3 ms
01b	0.4 ms	6.4 ms Offset included	6.4 ... 31.6 ms
10b	1.6 ms	32 ms Offset included	32 ... 132.8 ms
11b	not used		

Table 15: IO-Link cycle time

$T_{CYC} = T_{CYC\_OFFSET} + T_{CYC\_STEP} \cdot$ TIM_PER[5:0]

6.3.6.1 Cycle Synchronisation

In applications with several channels the device has implemented a cycle synchronization capability. To enable the cycle snchronization feature set bit SYNC in register TIM CFG to „1“.

Because of independent internal oscillator of several devices in multi port applications the synchronization has to be repeated after certain period of time. This period of time depends on oscillator accuracy and application needs. The cycle timer can be configured to run for a number of cycles determined by bits CNUM[2:0] in register TIM CFG (see Table 16 for details).

CNUM[2:0]	*Number of free running cycles*
000b	2
001b	4
010b	6
011b	8
100b	10
101b	12
110b	16
111b	32

Table 16: Number of cycles without resynchronization in SYNC mode

If this number of cycles is reached, the bit WAIT4S in register TIM STAT is set and the cycle timer waits for a resynchronization event from the host controller. Optionally an interrupt can be activated by bit SYNCIE in register TIM IE to indicate that the device is waiting for an resynchronization event (WAIT4S in TIM STAT). This interrupt is set after the number of free running cycles is reached under two conditions:

- the slave response frame is received (number of received characters is equal UART_RXNUM)
- idle is detected

The interrupt is cleard by reading TIM STAT.
The synchronization event is generated by the host micro controller using pin SCSN. If pin SCSN is driven low for T_{IOSYNC} and no SCK pulse is detected during this period the IO-Link Master IC will interpret this low pulse as synchronization event and will start the IO-Link cycle timer for the configured number of cycles immediately.

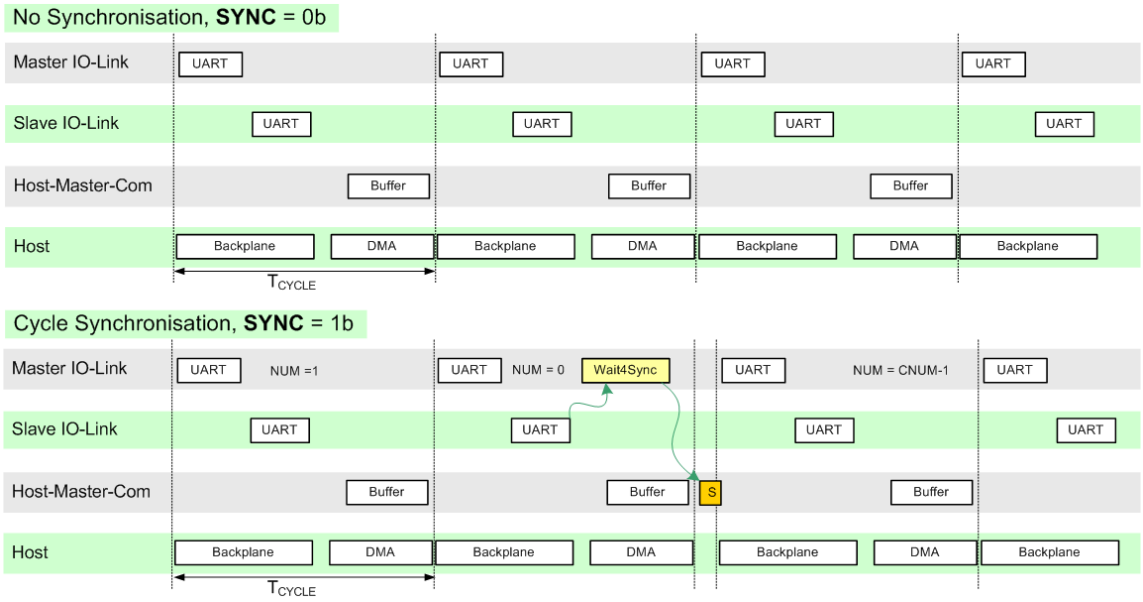


Fig. 13: IO-Link cycle timing with and without synchronisation

6.3.6.2 Configuration and Status Register

Register Name	*Address*	*Description*
Channel 1		
TIM CFG	0x16	Timer config channel 1
TIM IE	0x17	Timer Interrupt enable register channel 1
TIM STAT	0x18	IO-Link Cycle Timer status register channel 1
TIM PER	0x19	IO-Link Cycle Timer Period and Prescale configuration channel 1
Channel 2		
TIM CFG	0x26	Timer config channel 2
TIM IE	0x27	Timer Interrupt enable register channel 2
TIM STAT	0x28	IO-Link Cycle Timer status register channel 2
TIM PER	0x29	IO-Link Cycle Timer Period and Prescale configuration channel 2

Table 17: IO-Link Cycle Timer Register Table

Register **TIM CFG**
Channel 1 (0x16)
Channel 2 (0x26)

	MSB							*LSB*
Content	-	-	-	CNUM2	CNUM1	CNUM0	SYNC	EN
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit Description	**CNUM2 / CNUM1 / CNUM0** : Number of cycles between syncronisation 000 = 2 cycles 001 = 4 cycles 010 = 6 cycles 011 = 8 cycles 100 = 10 cycles 101 = 12 cycles 110 = 16 cycles 111 = 32 cycles **SYNC** : 1 = Enable syncronisation **EN** : 1 = Enable timer							

Table 18: Timer config

Register **TIM IE**
Channel 1 (0x17)
Channel 2 (0x27)

	MSB							***LSB***
Content	NUMIE	RDYIE	SYNCIE	ACCIE	RXEIE	-	-	-
Reset value	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R	R	R
Bit Description	**NUMIE** : 1 = Enable RXNUM Error interrupt **RDYIE** : 1 = Enable RDY interrupt **SYNCIE** : 1 = Enable SYNC interrupt **ACCIE** : 1 = Enable Access Error interrupt **RXEIE** : 1 = Enable RX Error (FE, PE) interrupt							

Table 19: Timer Interrupt enable registe

Register **TIM STAT**
Channel 1 (0x18)
Channel 2 (0x28)

	MSB							***LSB***
Content	NUME	RDY	WAIT4S	ACCE	RXE	IDLE	RX	TX
Reset value	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R
Bit Description	**NUME** : 1 = RX Number Error: Number of RX character is smaller than value in UART_RXNUM or no reception at all in current cycle **RDY** : 1 = Transmission and Reception completed **WAIT4S** : 1 = Cycle timer waits for synchronization in SYNC mode **ACCE** : 1 = Buffer Access Error: micro controller write access to TRX buffer while active transmission or reception **RXE** : 1 = UART Rx error detected (PE, FE) **IDLE** : 1 = Cycle timer in idle phase **RX** : 1 = Cycle timer running, Reception ongoing **TX** : 1 = Cycle timer running, Transmission ongoing							

Table 20: IO-Link Cycle Timer status register

Register **TIM PER**
Channel 1 (0x19)
Channel 2 (0x29)

	MSB							***LSB***
Content	PRSC1	PRSC0	PER5	PER4	PER3	PER2	PER1	PER0
Reset value	0	0	0	0	0	0	0	0
Internal access	R/W	R/W R/W		R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**PRSC1 / PRSC0** : Cycle timer prescaler 00 = 0.4ms .. 6.3ms (T_{CYC_STEP} = 0.1ms) 01 = 6.4ms .. 31.6ms (T_{CYC_STEP} = 0.4ms) 10 = 32.0ms .. 132.8ms (T_{CYC_STEP} = 1.6ms) 11 = reserved **PER5 .. PER0** : Timer period configuration in n · T_{CYC_STEP}							

Table 21: IO-Link Cycle Timer Period and Prescale configuration

6.3.7 Wake-Up

The wakeup signal can be generated by external microcontroller using the parallel interface (TXEN, TXD, RXD) or integrated wakeup support.

If the wake-up generation support for the port is enabled in WTIM CFG, the device will generate a signal at CQ_OUTx depending on the CQ_INx level. To apply a wake-up, select Wake-up support register for channel x. The exact pulse timing is generated internally. For details see chapter 6.3.7.1.

The delay between RXDx evaluation and Wake-up pulse is minimized to reduce collisions by level change of external devices (race condition of wakeup signal and fast changes of device SIO-mode signal)

If the IOLINK master is requested to send a wake-up symbol, the transmitter is turned on for a time T_{d_WU} in order to perform a level inversion at pin CQ_OUTx. A maximum current (limit I_{LIM_L} or I_{LIM_H}) will be delivered for time T_{d_WU}. The slave is expected to release the C/Q bus during this time. Afterwards the transmitter drives pin CQ_OUTx to the pre- wake-up pulse level and then turns off for a recovery time of $T_{d\_off\_WU}$.

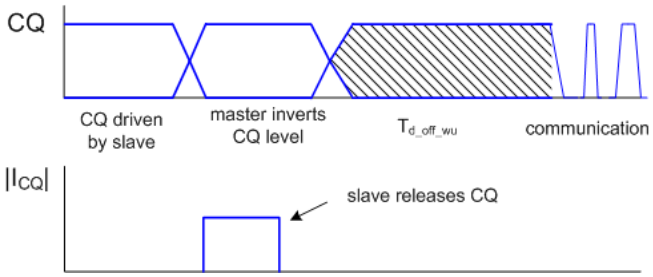


Fig. 14: Wake up procedure

The WURQ timer generates the specified IO-Link wake up request signal for both IO-Link channels selected by bits CH1 / CH2 in register WTIM_CFG.

The wake up sequence is started immediately after SPI setting bit START in register **WTIM_CFG**. The host micro controller can poll WURQ status information or enable a „wakeup completed interrupt“.

After $T_{d\_off\_wu}$ the transmitter is ready to transmit and responds to requests from either TXENx and TXDx or the UART.

6.3.7.1 WURQ Status and Control Registers

Register Name	*Address*	*Description*
WTIM CFG	0x04	WURQ configuration and status register

Table 22: WURQ Timer Register Table

Register **WTIM CFG** (0x04)

	MSB							*LSB*
Content	RDY	BUSY	CH2	CH1	RDYIE	-	-	START
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R	R	R	R/W
Bit Description	**RDY** : 1 = Wake up sequence completed. cleared by new START or read access to this register **BUSY** : 1 = Wake up sequence ongoing **CH2** : 1 = Wake up sequence enabled for channel 2 **CH1** : 1 = Wake up sequence enabled for channel 1 **RDYIE** : 1 = Interrupt for RDY (wake up sequence completed) enabled **START** : 1 = start a wake up signal at channel (always read as '0')							

Table 23: WURQ configuration and status register

6.4 Oscillator

The oscillator provides the clock for internal and external digital circuitry. The required oscillator accuracy depends on the application concept.

In applications using the parallel communication interface (TXEN, TXD, RXD) the external microcontroller provides the needed bit time accuracy. In this case the internal oscillator (OSC_{RC}) is sufficient for system control and wakeup pulse generation and no external components are needed.

6.4.1 PLL

In applications using the internal UARTs and IO-Link cycle timer the system clock accuracy has to be better than 0.1%. The clock system structure is shown in Fig. 15.

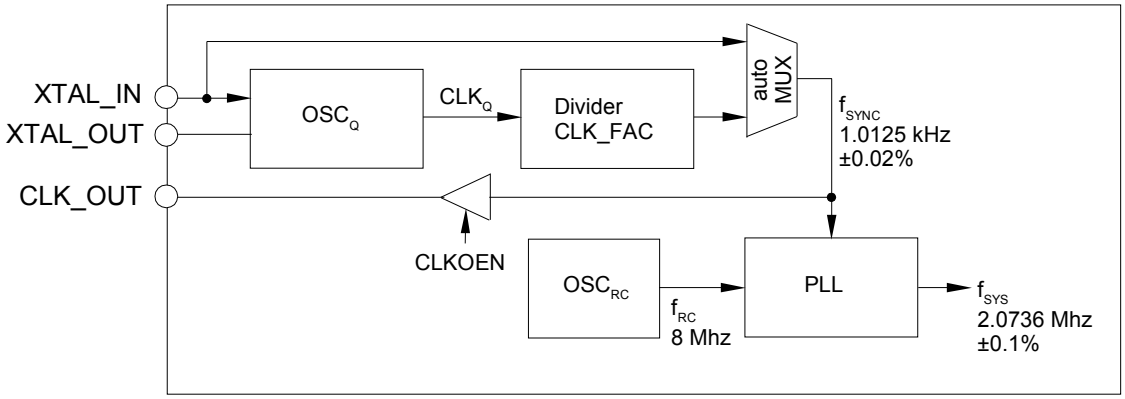


Fig. 15: Clock system structure

Clock accuracy can be reached by applying either an:

- external quartz at XTAL_IN and XTAL_OUT. No external capacitors are necessary. To increase the robustness to EMI the input XTAL_IN shall be connected to GND if the quartz oscillator is not used.
- or an digital clock signal from an external clock source provided by an external microcontroller or by the CLK_OUT signal of other E981.12 devices used in multi port applications.

This external signal is used to synchronize the internal PLL block.
If f_{XTAL_IN} it is excatly f_{SYNC} = 1.0125 kHz the multiplexer automatically switches directly to the XTAL_IN signal path. In this case there is no need to configure the CLK_FAC divider.
In case of higher input frequencies f_{XTAL_IN} is divided by the CLK_FAC divider block to get the 1.0125 kHz f_{SYNC} signal. The internal multiplexer automatically switches to this signal path.

Register CLK_CTRL configures the XTAL input stage.Bit ENX enables the XTAL input/output stage. Bit EXTQ enables the quartz oscillator. If the quartz oscillator is not needed it can be disabled to reduce power dissipation.

The CLK_FAC divider has a reset value of 0x1C71 (7281d). Using other quartz frequencies than 7.3728 MHz the CLK_FAC value has to be changed to CLK_FAC = f_{Quartz} / C_{sync} - 1
The CLK_FAC can be in range of 0x0400 (2048d) up to 0x3FFF (16383d) which allows a wide range of the input frequency. It is recommended to configure the CLK_FAC registers reset condition of the IO-LINK Master IC.

Bit „LOCK“ in register CLK_STAT indicates a locked PLL. The PLL has a locking tolerance of approximately 10%. Incorrect CLK_FAC configuration results in locked PLL but incorrect system communication timing.

Register Name	*Address*	*Description*
CLK_STAT	0x0C	Clock status register
CLK_CTRL	0x0D	Clock system control
CLK_FAC_LO	0x0E	Clock divider register
CLK_FAC_HI	0x0F	Clock divider register

Table 24: Clock Register Table

Register **CLK_CTRL** (0x0D)

	MSB							*LSB*
Content	-	-	-	EXTQ	-	-	CLKOE	ENX
Reset value	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R/W	R	R	R/W	R/W
Bit Description	**EXTQ** : 1 = XTAL_IN is used as clock input from extern clock source, XTAL_OUT is disabled (leave open) 0 = a quartz is connected to XTAL_IN and XTAL_OUT **CLKOE** : 1 = Clock output CLK_OUT enabled 0 = Clock output CLK_OUT disabled **ENX** : 1 = XTAL stage enabled 0 = XTAL stage disabled							

Table 25: Clock system control

Register **CLK_FAC_LO** (0x0E)

	MSB							*LSB*
Content	FAC7	FAC6	FAC5	FAC4	FAC3	FAC2	FAC1	FAC0
Reset value	0	1	1	1	0	0	0	1
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**FAC7** : Clock divider low byte							

Table 26: Clock divider register

Register **CLK_FAC_HI** (0x0F)

	MSB							*LSB*
Content	-	-	FAC13	FAC12	FAC11	FAC10	FAC9	FAC8
Reset value	0	0	0	1	1	1	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**FAC13** : Clock divider high byte							

Table 27: Clock divider register

Register **CLK_STAT** (0x0C)

	MSB							***LSB***
Content	-	-	-	PLLE	-	-	-	LOCK
Reset value	0	0	0	0	0	0	0	0
Internal access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
External access	R	R	R	R	R	R	R	R
Bit Description	**PLLE** : 1 = PLL error, cleared by read access **LOCK** : 1 = PLL locked							

Table 28: Clock status register

6.4.2 Clock Distribution

This feature can be used in multi IO-Link channel systems with more than one E981.12 devices. Using output pin CLK_OUT the accurate f_{sync} clock can be distributed to XTAL_IN of other devices on the PCB. The host has to configure the other master devices accordingly in CLK_CTRL.
The CLK_OUT port should be enabled after the IO-Link Master device completely configured to ensure the correct output frequency at system startup.

6.5 SPI Interface

The SPI interface is used for configuration, diagnostic and data transfer purposes. The SPI provides 16 bit read and write access as well as burst access to the internal transceiver (TRX) buffers.

The SPI interface consists of the pins SCSN, SCLK, MOSI, MISO, INTN supplied by VDD voltage. The input thresholds and output levels are referenced to this voltage. Digital input pins have pull-up/-down circuits described in chapter „Pinout description“

Several consecutive bytes are transfered during active chip select form a SPI access. SPI characters are transfered MSB first. The E981.12 uses two different SPI access types:

- Standard register access (16 bit)
- TRX buffer burst access

The first byte of a SPI access is the command byte. It contains:

- Bit 7: 0 = read or 1 = write access
- Bit 6: 0 = single or 1 = burst access
- Bits 5/4: always 0
- Bits 3..0: register or buffer code

:

6.5.1 Standard Register Access

The standard register access is used for all configuration and status registers. An interbyte gap of t_{IBG} has to be ensured by the host.

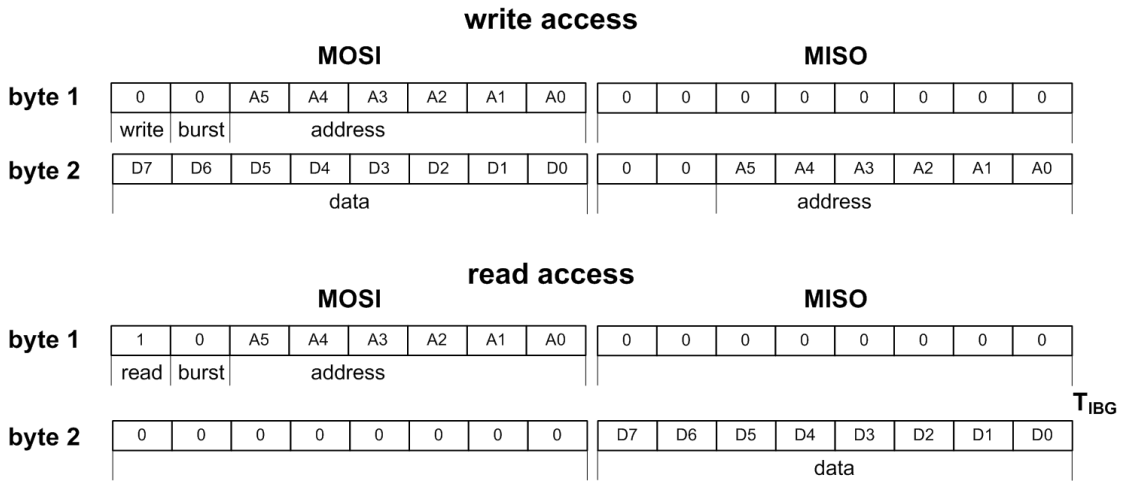


Fig. 16: SPI single read and write access

6.5.2 TRX Buffer Burst Access

This access type is used for the UART TRX buffer (see chapter „Transceiver UART“).
During burst access the second byte will contain the information about the number of data bytes which are read or written during SPI communication.

SPI transfer is secured by a XOR checksum to detect SPI communication errors. The last byte of the host transmission contains the XOR checksum byte. For host write acces the E981.12 compares this checksum with the calculated checksum. For host read access the host has to compare this checksum with the calculated checksum.

Transmission error is indicated by an interrupt XORIRQ in register ISTAT. This interrupt can not be masked.

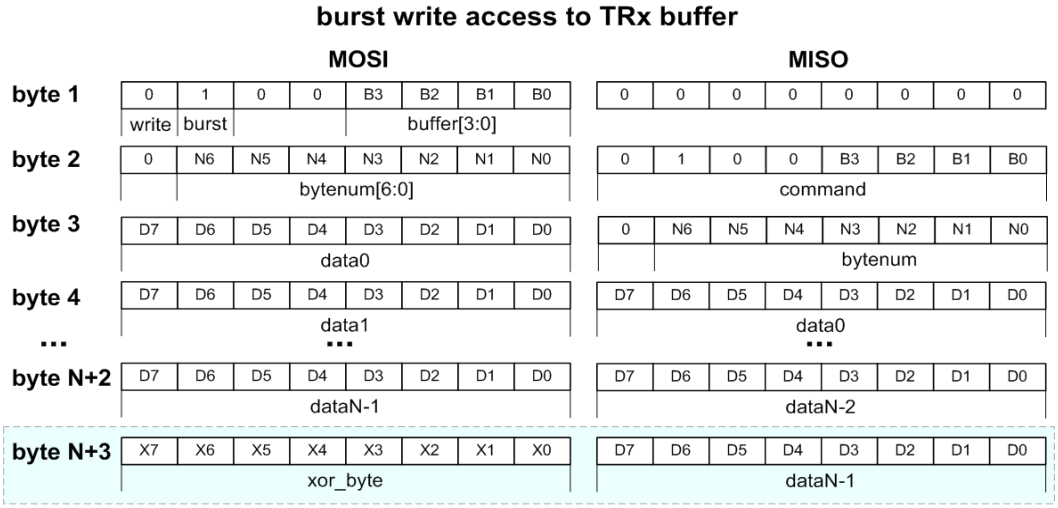


Fig. 17: UART buffer burst write access

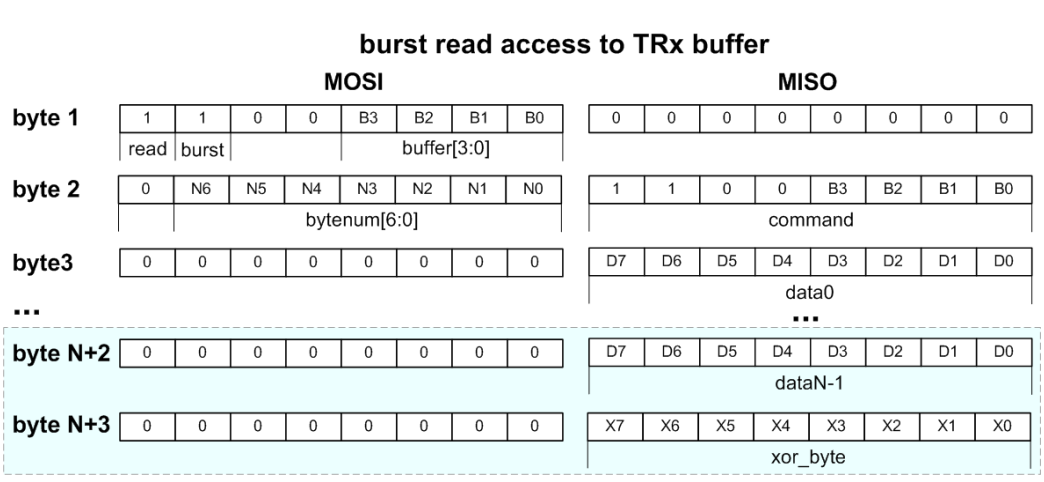


Fig. 18: UART buffer burst read access

6.5.3 SPI Timing

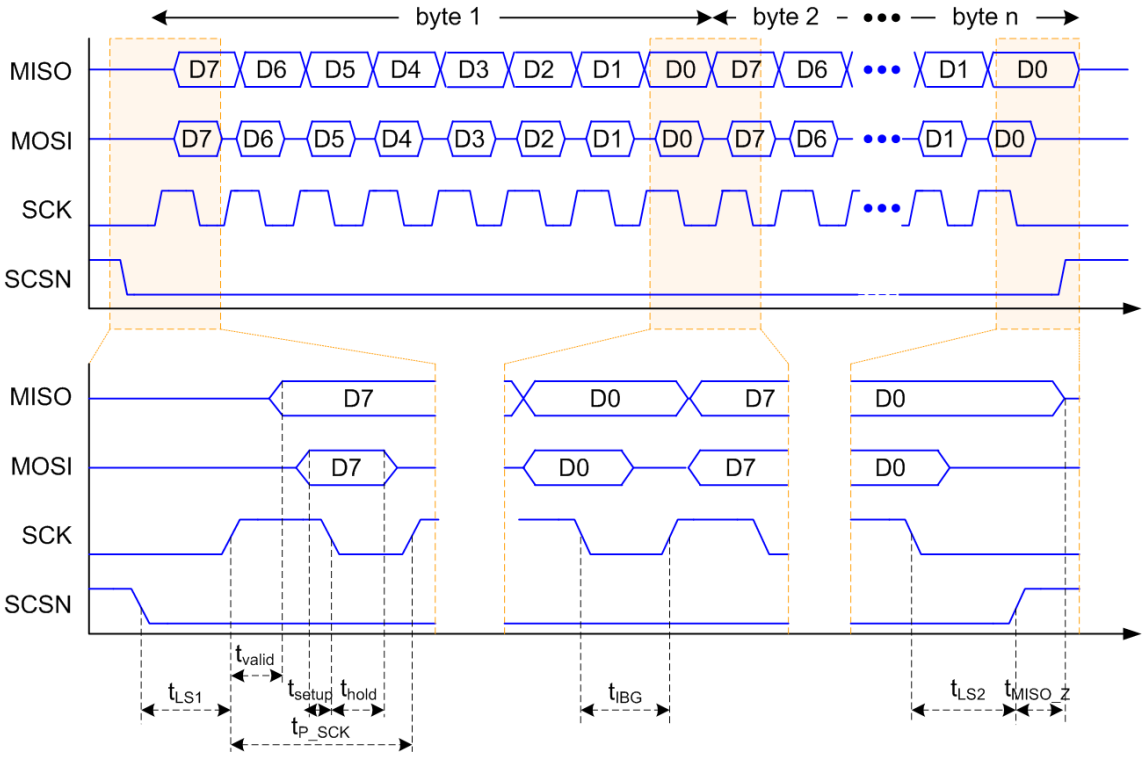


Fig. 19: SPI timing

6.6 Interrupt Controller

The interrupt controller generates the output signal at pin INTN. All interrupt sources except of XORIRQ can be masked. ISTAT is the interrupt status register. The interrupt is kept active until the corresponding status register has been read. If all interrupts are masked the software is still able to recognize interrupts by polling the status register.

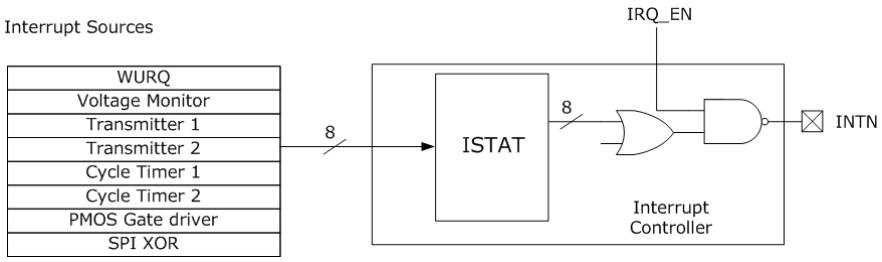


Fig. 20: IRQ sources and generation

The following Table 29 lists all modules which can generate interrupts. The interrupts are explained in detail in the corresponding chapters.

Interrupt	*Module*	*Description*
UART & Timer Interrupt	Transceiver UART and IO-Link cycle timer	wait for Timer SYNC, RXNUM-Error, RDY and Buffer access violation
VMON interrupt	Voltage monitoring	One of the voltages not in specified range
Transmitter interrupt	Transmitter	Over current or Over temperature at CQ_OUTx
Gate driver interrupt	PMOS gate driver	PMOS Gate driver over current
SPI error interrupt	Host interface	Error during SPI burst access (XOR checksum not correct)
Wakeup ready interrupt	WURQ timer	Wakeup pulse completed

Table 29: Interrupt Sources

Register Name	*Address*	*Description*
ISTAT	0x00	

Table 30: Interrupt source register

Register **ISTAT** (0x00)

	MSB							*LSB*
Content	WUIRQ	XORIRQ	PDIRQ	VMIRQ	TXIRQ2	TXIRQ1	TIRQ2	TIRQ1
Reset value	0	0	0	0	0	0	0	0
External access	R	R	R	R	R	R	R	R
Bit Description	**WUIRQ** : 1 = WURQ sequence IRQ **XORIRQ** : 1 = SPI error IRQ - XOR checksum not correct **PDIRQ** : 1 = PMOS gate driver IRQ **VMIRQ** : 1 = Voltage monitoring IRQ **TXIRQ2** : 1 = Transmitter 2 IRQ **TXIRQ1** : 1 = Transmitter 1 IRQ **TIRQ2** : 1 = IO-Link cycle timer 2 IRQ **TIRQ1** : 1 = IO-Link cycle timer 1 IRQ							

Table 31: ISTAT

6.7 IO-Link Supply Control

The IO-Link Supply Control controls the supply voltage Lx using an external PMOS power MOSFETs The following figure (Fig. 21) shows the principle.

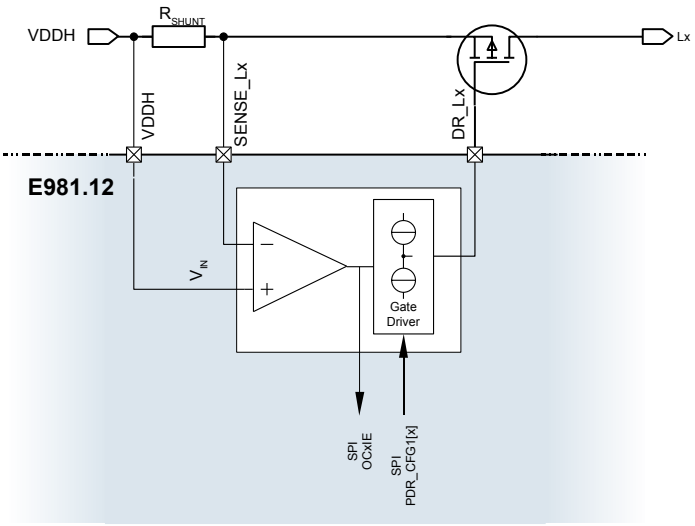


Fig. 21: IO-Link Supply Control

The FET can be activated or deactivated by SPI register PDR_CFG1.

To limit the current in case of failures the current is measured using an external shunt resistor. If a certain voltage drop is detected at the shunt resistor the overcurrent condition is set in SPI register and optionally an interrupt can be generated. The overcurrent detection threshold is scaled by the external shunt resistor. $I_{TH(OC)}$ is typically V_{IN_OCCOMP} / R_{shunt} (e.g. I_{LIM} typically 90mV / 100mOhm = 0.9A).

The gate of the external FET is controlled to limit the current. The current limit is calculated by the external shunt resistor. $I_{TH(LIM)}$ is calculated as V_{IN_OC} / R_{shunt} (e.g. $I_{TH(LIM)}$ typically 100mV / 100mOhm = 1A). The external FET is switched off after a configurable time to limit power dissipation in this state. This event can be signalled by interrupt if enabled by OcxIE in register PDR_CFG2.

After a configurable off-time the driver is switched on automatically. The dutycycle of this cyclic switching must be configured in register PDR_CFG1 to keep the external FET within the safe operating area. By configuring this register both - automatic switch-off and automatic switch-on can be disabled. If automatic switch-on is disabled the FET can be enabled after a shutdown by reading the register PDR_STAT.

If the bit HARDSW in the register PDR_CFG2 is set, the PMOS-Driver works simply as a switch. In case of detecting overcurrent at the external shunt the external FET is switched off immidiately. In this mode cyclic switching is disbled. To enable the FET after a shutdown register PDR_STAT has to be read.

6.7.1 Status and Control Registers

Register Name	*Address*	*Description*
PDR_CFG1	0x09	Configuration of PMOS gate control
PDR_CFG2	0x0A	Gate control interrupt enable
PDR_STAT	0x0B	Gate control status register

Table 32: PMOS gate driver register table

Register **PDR_CFG1** (0x09)

	MSB							*LSB*
Content	SHO1	SHO0	SHD1	SHD0	-	-	DR2	DR1
Reset value	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**SHO1** / **SHO0**: Shutdown delay, parameter t_{d_offx} **SHD1** / **SHD0**: Shutdown duration, parameter t_{offx} **DR2** : 1 = Driver L2 enabled 0 = Driver L2 disabled **DR1** : 1 = Driver L1 enabled 0 = Driver L1 disabled							

Table 33: Configuration of PMOS gate control

Register **PDR_CFG2** (0x0A)

	MSB							*LSB*
Content	-	-	OC2IE	-	-	-	OC1IE	HARDSW
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R/W	R	R	R	R/W	R/W
Bit Description	**OC2IE** : 1 = Over current interrupt enable channel 2 **OC1IE** : 1 = Over current interrupt enable channel 1 **HARDSW** : 1 = External driver hard on/off switching							

Table 34: Gate control interrupt enable

Register **PDR_STAT** (0x0B)

	MSB							*LSB*
Content	-	-	OC2IRQ	L2ON	-	-	OC1IRQ	L1ON
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**OC2IRQ** : 1 = OC at L2 shunt interrupt flag. Cleared after read access. **L2ON** : 1 = Driver for L2 enabled 0 = Driver for L2 disabled (by register or OC) **OC1IRQ** : 1 = OC at L1 shunt interrupt flag. Cleared after read access. **L1ON** : 1 = Driver for L1 enabled 0 = Driver for L1 disabled by overcurrent							

Table 35: Gate control status register

7 Register Table

Register Name	Address	Reference	Description
ISTAT	0x00	Page 40 Table 31	Interrupt source register
VMON STAT	0x02	Page 14 Table 5	Voltage monitor status register
VMON IE	0x03	Page 14 Table 6	Voltage monitor interrupt enable register
WTIM CFG	0x04	Page 32 Table 23	WURQ configuration and status register
PDR_CFG1	0x09	Page 42 Table 33	Configuration of PMOS gate control
PDR_CFG2	0x0A	Page 42 Table 34	Gate control interrupt enable
PDR_STAT	0x0B	Page 42 Table 35	Gate control status register
CLK_STAT	0x0C	Page 35 Table 28	Clock status register
CLK_CTRL	0x0D	Page 34 Table 25	Clock system control
CLK_FAC_LO	0x0E	Page 34 Table 26	Clock divider register
CLK_FAC_HI	0x0F	Page 34 Table 27	Clock divider register
CH CFG	0x10	Page 22 Table 8	Channel 1 configuration
CH STAT	0x11	Page 23 Table 9	Channel 1 status and error register
TRX CFG	0x12	Page 23 Table 10	Transceiver config channel 1
TX OCCFG	0x13	Page 24 Table 11	Transmitter over current configuration register channel 1
UART TXNUM	0x14	Page 24 Table 12	Number of Bytes for TX channel 1
UART RXNUM	0x15	Page 24 Table 13	Number of Bytes for RX channel 1
TIM CFG	0x16	Page 28 Table 18	Timer config channel 1
TIM IE	0x17	Page 29 Table 19	Timer Interrupt enable register channel 1
TIM STAT	0x18	Page 29 Table 20	IO-Link Cycle Timer status register channel 1
TIM PER	0x19	Page 30 Table 21	IO-Link Cycle Timer Period and Prescale configuration channel 1
RX STAT	0x1A	Page 25 Table 14	Receiver status and error register channel 1
CH CFG	0x20	Page 22 Table 8	Channel 2 configuration
CH STAT	0x21	Page 23 Table 9	Channel 2 status and error register
TRX CFG	0x22	Page 23 Table 10	Transceiver config channel 2
TX OCCFG	0x23	Page 24 Table 11	Transmitter over current configuration register channel 2
UART TXNUM	0x24	Page 24 Table 12	Number of Bytes for TX channel 2
UART RXNUM	0x25	Page 24 Table 13	Number of Bytes for RX channel 2
TIM CFG	0x26	Page 28 Table 18	Timer config channel 2
TIM IE	0x27	Page 29 Table 19	Timer Interrupt enable register channel 2
TIM STAT	0x28	Page 29 Table 20	IO-Link Cycle Timer status register channel 2
TIM PER	0x29	Page 30 Table 21	IO-Link Cycle Timer Period and Prescale configuration channel 2
RX STAT	0x2A	Page 25 Table 14	Receiver status and error register channel 2

Table 36: Register Table

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