PCA9509A

Low power level translating I²C-bus/SMBus repeater

Rev. 1 — 29 February 2012 Product data sheet

1. General description

The PCA9509A is a level translating I²C-bus/SMBus repeater with two voltage supplies that enables processor low voltage 2-wire serial bus to interface with standard I²C-bus or SMBus I/O. While retaining all the operating modes and features of the I²C-bus system during the level shifts, it also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling the I²C-bus or SMBus maximum capacitance of 400 pF on the higher voltage side. Port A allows a voltage range from 0.8 V to 1.5 V and requires no external pull-up resistors due to the internal current source. Port B allows a voltage range from 2.3 V to 5.5 V and is overvoltage tolerant. Both port A and port B SDA and SCL pins are high-impedance when the PCA9509A is unpowered.

The bus port B drivers are compliant with SMBus I/O levels, while port A uses an offset LOW which prevents bus lock-up and allows the bidirectional nature of the device. Port A uses a current source for pull-up and an offset pull-down driver. This results in a LOW on the port A accommodating smaller voltage swings. The output pull-down on the port A internal buffer LOW is set for approximately $0.2V_{CC(A)}$, while the input threshold of the internal buffer is set about 50 mV lower than that of the output voltage LOW. When the port A I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the port B drives a hard LOW and the input level is set at 30 % of SMBus or I²C-bus voltage level which enables port B to connect to any other I²C-bus devices or buffer.

The PCA9509A drivers are not enabled unless $V_{CC(A)}$ is above 0.7 V and $V_{CC(B)}$ is above 1.7 V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.

The PCA9509A is similar to the PCA9509 but offers lower A port voltage range to 0.8 V to accommodate lower voltage processors and disables the current mirrors when disabled to reduce standby power.

1.1 Selection recommendations

The PCA9509A is recommended for all applications except in the following cases:

- PCA9509P should be used if an external A-port pull-up resistor is required to adjust current for noise margin considerations or to reduce operating current consumption even more.
- The PCA9509 should be used if instant on from disable is required with A Port voltage greater than 1.0 V and larger standby current is not a concern.

Table 1. Device selection recommendation

Concern	Recommended device		
	PCA9509	PCA9509A	PCA9509P
A-port — lowest voltage	0.95 V with limitations	0.80 V	0.80 V
A-port — current source[1]	yes — 1 mA	yes — 270 μA	no — external pull-up
operating current[2]	< 6.1 mA	< 1.9 mA	< 0.95 mA
standby current EN = LOW	< 2 mA	< 10 μA max.	< 10 μA max.

[1] The PCA9509 current mirrors do not shut down when the device is disabled allowing instant turn-on, but at the cost of the higher standby current. The PCA9509A and PCA9509P current mirrors are turned off when disabled for lowest standby power consumption, but sufficient delay (10 μs) after enable is needed before resuming operation.

[2] Operating currents do not include the current consumed by the external pull-ups on B-port or the external pull-ups on the A-port of the PCA9509P.

2. Features and benefits

- Bidirectional buffer isolates capacitance and allows 400 pF on port B of the device
- Voltage level translation from port A (0.8 V to 1.5 V) to port B (2.3 V to 5.5 V)
- Requires no external pull-up resistors on lower voltage port A
- Active HIGH repeater enable input disables current mirrors and current source to reduce standby power
- Open-drain port B inputs/outputs
- Lock-up free operation
- Supports arbitration and clock stretching across the repeater
- Accommodates Standard-mode and Fast-mode I²C-bus devices and multiple masters
- Powered-off high-impedance I²C-bus pins
- Operating supply voltage range of 0.8 V to 1.5 V on port A, 2.3 V to 5.5 V on port B
- All pins are 5 V tolerant with respect to ground pin
- 0 Hz to 400 kHz clock frequency

  Remark: The maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater.
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: TSSOP8, XQFN8

3. Ordering information

Table 2. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9509ADP	9509A	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9509AGM	9AX[1]	XQFN8	plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 × 1.6 × 0.5 mm	SOT902-2

[1] 'X' will change based on date code.

4. Functional diagram

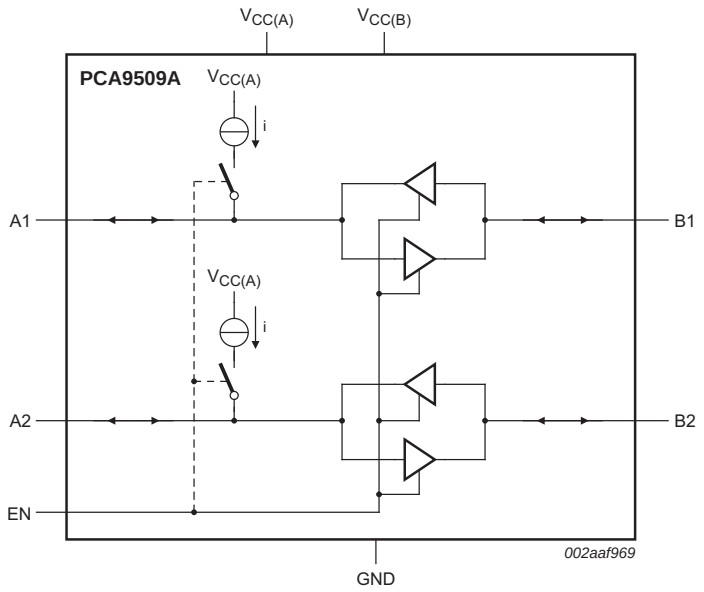


Fig 1. Functional diagram of PCA9509A

5. Pinning information

5.1 Pinning

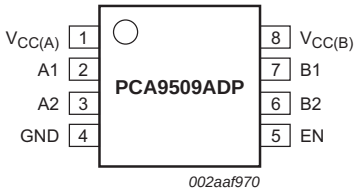


Fig 2. Pin configuration for TSSOP8

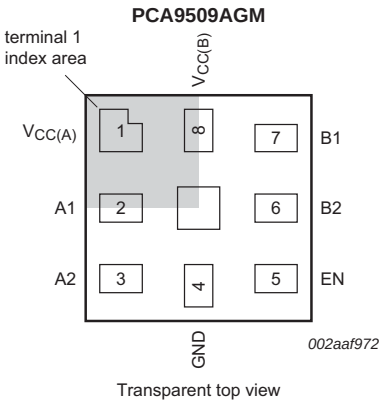


Fig 3. Pin configuration for XQFN8

5.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
$V_{CC(A)}$	1	port A power supply
A1[1]	2	port A (lower voltage side)
A2[1]	3	port A (lower voltage side)
GND	4	ground (0 V)
EN	5	enable input (active HIGH)
B2[1]	6	port B (SMBus/I²C-bus side)
B1[1]	7	port B (SMBus/I²C-bus side)
$V_{CC(B)}$	8	port B power supply

[1] Port A and port B can be used for either SCL or SDA.

6. Functional description

Refer to Figure 1 “Functional diagram of PCA9509A”.

The PCA9509A enables I²C-bus or SMBus translation down to $V_{CC(A)}$ as low as 0.8 V without degradation of system performance. The PCA9509A contains 2 bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage and 3.3 V SMBus or 5 V I²C-bus. The port A and port B I/Os are overvoltage tolerant to 5.5 V even when the device is unpowered. Due to the current source on port A the voltage on the pins should not be above $V_{CC(A)}$ when the device is powered.

The PCA9509A includes a power-up circuit that keeps the output drivers turned off until $V_{CC(B)}$ is above 1.7 V and the $V_{CC(A)}$ is above 0.7 V. $V_{CC(B)}$ and $V_{CC(A)}$ can be applied in any sequence at power-up. After power-up and with the EN pin HIGH, a LOW level on port A (below approximately $0.15V_{CC(A)}$) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to about 0 V. When port A rises above approximately $0.15V_{CC(A)}$, the port B pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When port B falls first and goes below $0.3V_{CC(B)}$, the port A driver is turned on and port A pulls down to $0.2V_{CC(A)}$ (typical). The port B pull-down is not enabled unless the port A voltage goes below V_{IL}. If the port A low voltage goes below V_{IL}, the port B pull-down driver is enabled until port A rises above approximately $0.15V_{CC(A)}$ (V_{IL}), then port B, if not externally driven LOW, will continue to rise being pulled up by the external pull-up resistor.

Remark: Ground offset between the PCA9509A ground and the ground of devices on port A of the PCA9509A must be avoided.

The reason for this cautionary remark is that a CMOS/NMOS open-drain capable of sinking 3 mA of current at 0.4 V has an output resistance of 133 Ω or less (R = E / I). Such a driver shares enough current with the port A output pull-down of the PCA9509A to be seen as a LOW as long as the ground offset is zero. If the ground offset is greater than 0 V, then the driver resistance must be less. Since V_{IL} can be as low as 80 mV at cold temperatures and the low end of the current distribution, the maximum ground offset should not exceed 40 mV.

Bus repeaters that use an output offset are not interoperable with the port A of the PCA9509A as their output LOW levels are not recognized by the PCA9509A as a LOW. If the PCA9509A is placed in an application where the V_{IL} of port A of the PCA9509A does not go below its V_{IL}, the port B does not go LOW.

Port B provides normal I²C-bus voltage levels and is interoperable with all I²C-bus slaves, masters and repeaters.

6.1 Enable

The EN pin is active HIGH and allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I²C-bus operation because disabling during a bus operation hangs the bus and enabling part way through a bus cycle could confuse the I²C-bus parts being enabled. The EN also puts the PCA9509A in a standby condition to reduce power consumption.

The enable pin should only change state when the bus and the repeater port are in an idle state to prevent system failures.

Because the enable pin (EN) can put the PCA9509A in Standby mode, and when in standby the current sources and current mirrors are turned OFF to save power, the recovery from the disabled/standby state is slow so that the current sources and current mirrors can return to full current before the channels are enabled.

Remark: The system design should allow sufficient time after STOP before disabling the PCA9509A so that both sides of the SDA and SCL channels are HIGH. It should also allow sufficient time before the START such that the channel is disabled before the SDA goes LOW. The PCA9509A should only be enabled during a bus idle state and there also needs to be sufficient time allowed before the START such that the PCA9509A is fully active before the falling edge of the SDA that defines a START.

6.2 I²C-bus systems

As with the standard I²C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I²C-bus). The size of these pull-up resistors depends on the system. Each of the port A I/Os has an internal pull-up current source and does not require the external pull-up resistor. Port B is designed to work with Standard-mode and Fast-mode I²C-bus devices in addition to SMBus devices. Standard-mode I²C-bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I²C-bus system where Standard-mode devices and multiple masters are possible. Under certain conditions higher termination currents can be used.

6.3 Edge rate control

The PCA9509A includes circuitry that slows down the falling edge of both the A side and B side open-drain output pull-downs. This slowdown reduces system noise and undershoot when the signal reflects off of the end of the bus. The slew rate control circuit limits the maximum slew rate, and is relatively insensitive to the load capacitance, the bus high voltage and to the pull-up value. The rising edge slew rate on the A side is controlled by the pull-up current source and the load capacitance. The rising edge slew rate on the B side is controlled by RC time constant of the bus pull-up resistor and the bus capacitance, which are system level considerations and not under the control of the PCA9509A. The B side pull-up resistor should be chosen based on the total B side bus capacitance to result in a reasonable rising edge transition time that is less than the maximum allowed rise time, and slow enough not to make system level noise problems.

6.4 Bus pull-up resistor selection

The AC test load for the B side of the PCA9509A is 1.35 kΩ and 50 pF total capacitance. This results in a rise time of approximately 60 ns. The 1.35 kΩ resistor is chosen to provide a little less than 3 mA in a 3.3 V application so it is compatible with Standard-mode I²C-bus devices as well as Fast-mode devices. The B side output pull-down is a strong driver and is capable of sinking Fast-mode Plus (Fm+) currents, however the pull-up must be sized for the weakest part in the system, so if Standard-mode I²C-bus parts are present on the B side, the pull-up must be limited to less than 3 mA. If only Fm+ parts are used on the B side, the maximum pull-up current may be up to 30 mA. The pull-up resistor should always be sized to provide less than the rated pull-up current for the weakest part on the bus under the maximum bus voltage expected in the system.

When the bus capacitance is high, the current should be set near the maximum current drive for the weakest part. However, if the bus capacitance is low a lower current/higher resistor value should be used to keep the rise time from getting so fast that it causes problems. The A side does not need a pull-up resistor. If one is added, care must be taken to keep the LOW-level voltage at the A side input below $0.1V_{CC(A)}$.

7. Application design-in information

A typical application is shown in Figure 4. In this example, the CPU is running on a 0.9 V I²C-bus while the slave is connected to a 3.3 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

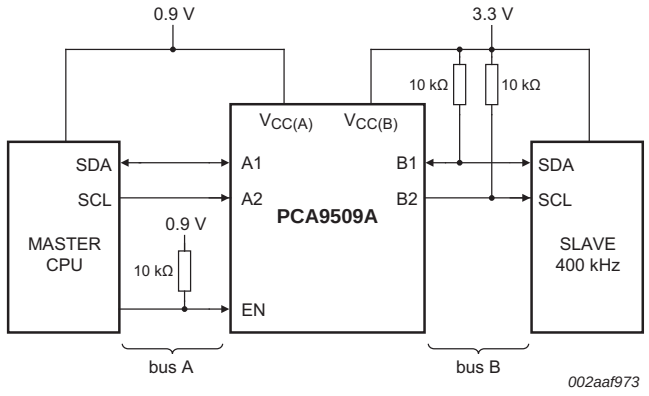


Fig 4. Typical application

When port B of the PCA9509A is pulled LOW by a driver on the I²C-bus, a CMOS hysteresis input detects the falling edge when it goes below $0.3V_{CC(B)}$ and causes the internal driver on port A to turn on, causing port A to pull down to about $0.2V_{CC(A)}$. When port A of the PCA9509A falls, a comparator detects the falling edge when it falls below $0.15V_{CC(A)}$ and causes the internal driver on port B to turn on and pull the port B pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 5 and Figure 6. If the bus master in Figure 4 were to write to the slave through the PCA9509A, waveforms shown in Figure 5 would be observed on the B bus. This looks like a normal I²C-bus transmission.

On the A bus side of the PCA9509A, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PCA9509A. After the eighth clock pulse, the data line will be pulled to the V_{OL} of the master device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the PCA9509A for a short delay while the B bus side rises above $0.5V_{CC(B)}$, then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the A bus side at the input of the PCA9509A (V_{IL}) is below $0.1V_{CC(A)}$ to be recognized by the PCA9509A and then transmitted to the B bus side.

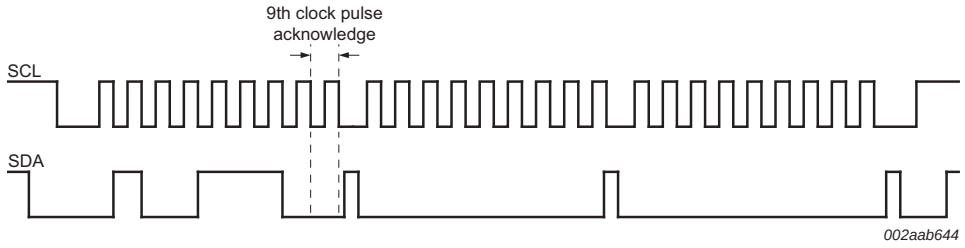


Fig 5. Bus B SMBus/I²C-bus waveform

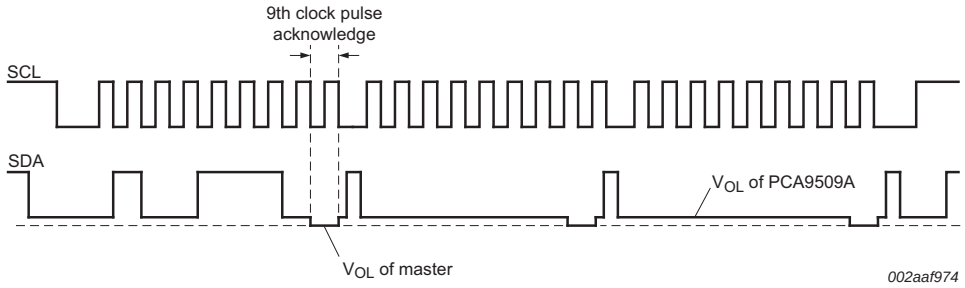


Fig 6. Bus A lower voltage waveform

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(B)}$	supply voltage port B			−0.5	+6.0	V
$V_{CC(A)}$	supply voltage port A			−0.5	+6.0	V
$V_{I/O}$	voltage on an input/output pin	port A	[1]	−0.5	+6.0	V
		port B; enable pin (EN)	[1]	−0.5	+6.0	V
$I_{I/O}$	input/output current			-	±20	mA
I_{OL}	LOW-level output current	A-side I/O active LOW		-	20	mA
		B-side I/O active LOW		-	40	mA
I_I	input current			-	±20	mA
P_{tot}	total power dissipation			-	100	mW
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature	operating in free air		−40	+85	°C
T_j	junction temperature			-	+125	°C
T_{sp}	solder point temperature	10 s max.		-	300	°C

[1] With I/O pins OFF. If active, see I_{OL}.

9. Static characteristics

Table 5. Static characteristics

GND = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Supplies							
$V_{CC(B)}$	supply voltage port B	see Table note [2]		2.3[2]	-	5.5	V
$V_{CC(A)}$	supply voltage port A	see Table note [2]		0.8[3]	-	1.5[2]	V
$I_{CC(A)}$	supply current port A	all port A static HIGH or LOW		2	5	12	μA
$I_{CC(B)}$	supply current port B	all port B static HIGH		200	500	850	μA
		all port B static LOW		0.4	1.1	1.9	mA
$I_{CC(B)stb}$	standby port B supply current	EN = LOW; all port B static HIGH or LOW		0.5	1.5	10	μA
Input and output of port A (A1 to A2)							
V_{IH}	HIGH-level input voltage	port A		$0.2V_{CC(A)}$	-	$V_{CC(A)}$	V
V_{IL}	LOW-level input voltage			−0.5	-	$+0.1V_{CC(A)}$	V
V_{IK}	input clamping voltage	I_L = −18 mA		−1.5	-	−0.5	V
I_{LI}	input leakage current	$V_I = V_{CC(A)}$ + 0.1 V; EN = HIGH; B1 = HIGH		−10	-	+10	μA
		EN = GND		−1	-	+1	μA
I_{IL}	LOW-level input current	V_I = 30 mV	[4]	−450	−270	−100	μA
V_{OL}	LOW-level output voltage	$V_{CC(A)}$ = 0.8 V to ($V_{CC(B)}$ − 1 V); I_{load} = 100 μA	[5] [6]	-	$0.2V_{CC(A)}$	$0.25V_{CC(A)}$	V
$V_{OL}-V_{IL}$	difference between LOW-level output and LOW-level input voltage		[7]	-	$0.05V_{CC(A)}$	-	mV
C_{io}	input/output capacitance	disabled		-	7	-	pF
Input and output of port B (B1 to B2)							
V_{IH}	HIGH-level input voltage	port B		$0.7V_{CC(B)}$	-	$V_{CC(B)}$	V
V_{IL}	LOW-level input voltage	port B		−0.5	-	$+0.3V_{CC(B)}$	V
V_{IK}	input clamping voltage	I_L = −18 mA		−1.5	-	−0.5	V
I_{LI}	input leakage current	V_I = 5.5 V with An input HIGH		−1.0	-	+1.0	μA
I_{IL}	LOW-level input current	V_I = 200 mV; $V_{CC(B)}$ = 5.5 V; $V_{CC(A)}$ = 1.5 V; port A = open		−10	-	+10	μA
V_{OL}	LOW-level output voltage	I_{OL} = 6 mA		-	0.1	0.2	V
		I_{OL} = 30 mA at $V_{CC(B)}$ = 3.0 V		-	0.2	0.5	V
C_{io}	input/output capacitance	disabled		-	3	5	pF
Enable							
V_{IL}	LOW-level input voltage			−0.5	-	$+0.2V_{CC(A)}$	V
V_{IH}	HIGH-level input voltage			$0.8V_{CC(A)}$	-	$V_{CC(B)}$	V
$I_{IL(EN)}$	LOW-level input current on pin EN	V_I = 0.2 V; $V_{CC(B)}$ = 5.5 V; $V_{CC(A)}$ = 1.5 V		−10	-	+1	μA
I_{LI}	input leakage current	$V_I = V_{CC(A)}$		−1	-	+1	μA
C_i	input capacitance	V_I = 3.0 V		-	2	3	pF

[1] Typical values with $V_{CC(A)}$ = 1.1 V, $V_{CC(B)}$ = 3.3 V.

[2] $V_{CC(A)}$ must be ≤ $V_{CC(B)}$ − 1 V, that is, $V_{CC(A)}$ = 1.5 V and $V_{CC(B)}$ = 2.3 V is not a valid combination.

[3] Care must be taken to minimize the resistance in series with the ground pin of the PCA9509A to the ground reference point of the $V_{CC(A)}$ supply because there is only 80 mV margin between the power good threshold and the 0.8 V minimum supply voltage at cold temperature (−40 °C). Because the B-side I_{OL} of up to 30 mA flows through the resistance causing a voltage drop that effectively reduces the $V_{CC(A)}$ to chip ground voltage and when $V_{CC(A)}$ is less than the power good voltage ~0.72 V, the PCA9509A is disabled. For example, if the resistance is 1.4 Ω, then 1.4 Ω × 60 mA = 84 mV and 0.8 V − 0.084 V = 0.716 V, which is less than the power good threshold, so the PCA9509A disables when both outputs drive LOW.

[4] The port A current source has a typical value of about 270 μA, but varies with both $V_{CC(A)}$ and $V_{CC(B)}$.

[5] As long as the chip ground is common with the input ground reference the driver resistance may be as large as 120 Ω. However, ground offset rapidly decreases the maximum allowed driver resistance.

[6] Current load is a requirement for ATE testing, not part operation.

[7] Guaranteed by design.

10. Dynamic characteristics

Table 6. Dynamic characteristics

$V_{CC(A)}$ = 0.8 V to 1.5 V; $V_{CC(B)}$ = 2.3 V to 5.5 V; GND = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.[1][2]

Symbol	Parameter	Conditions		Min	Typ[3]	Max	Unit
$V_{CC(A)}$ = 1.1 V; $V_{CC(B)}$ = 3.3 V							
t_{PLH}	LOW to HIGH propagation delay	port B to port A	[1]	76	146	257	ns
t_{PHL}	HIGH to LOW propagation delay	port B to port A	[1]	106	162	259	ns
SR_r	rising slew rate	port A; 0.3$V_{CC(A)}$ to 0.7$V_{CC(A)}$	[1]	0.001	0.005	0.009	V/ns
SR_f	falling slew rate	port A; 0.7$V_{CC(A)}$ to 0.3$V_{CC(A)}$	[1]	0.007	0.015	0.03	V/ns
t_{PLH}	LOW to HIGH propagation delay	port A to port B	[1]	−79	−144	−228	ns
t_{PLH2}	LOW to HIGH propagation delay 2	port A to port B; measured from 0.15$V_{CC(A)}$ on port A to 0.5$V_{CC(B)}$ on port B	[1]	54	147	356	ns
t_{PHL}	HIGH to LOW propagation delay	port A to port B	[1]	56	96	494	ns
SR_f	falling slew rate	port B; 0.7$V_{CC(B)}$ to 0.3$V_{CC(B)}$	[1]	0.02	0.05	0.11	V/ns
t_{en}	enable time	EN HIGH to enabled	[4]	10	-	-	μs
t_{dis}	disable time	EN LOW to disabled	[4]	300	-	-	ns

[1] Load capacitance = 50 pF; load resistance on port B = 1.35 kΩ. Port A = no pull-up, and an input falling slew rate of 0.05 V/ns.

[2] $V_{CC(A)}$ + 1.0 V ≤ $V_{CC(B)}$.

[3] Typical values were measured with $V_{CC(A)}$ = 1.1 V; $V_{CC(B)}$ = 3.3 V at T_{amb} = 25 °C, unless otherwise noted.

[4] Enable pin (EN) should only change state when the bus and the repeater port are in an idle state, that is, the t_{en} should be considered the set-up time before START and t_{dis} should be considered the hold time after STOP.

10.1 AC waveforms

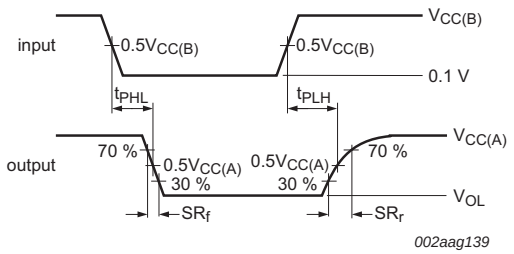


Fig 7. Propagation delay times and slew rate; port B to port A

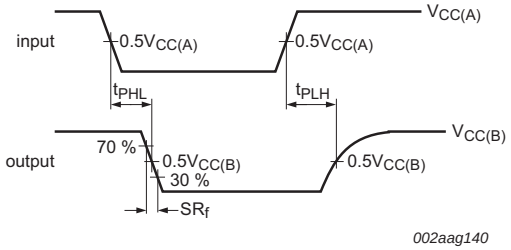


Fig 8. Propagation delay times and slew rate; port A to port B

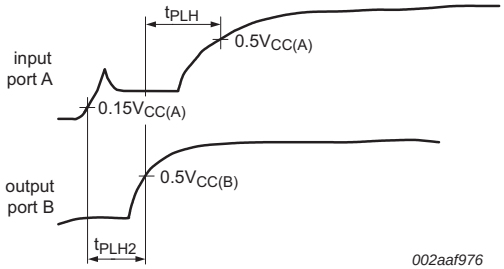
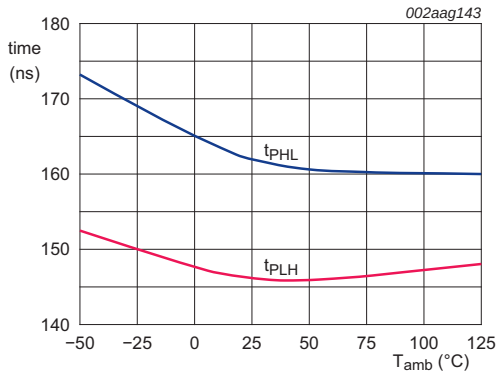


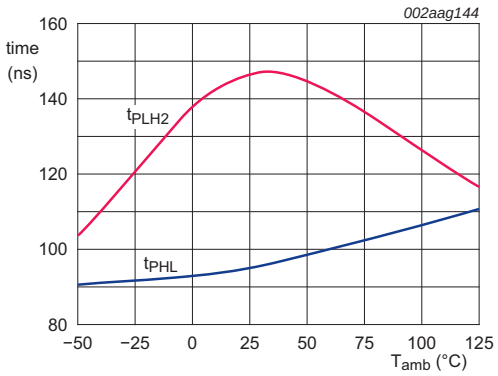
Fig 9. Propagation delay from the port A external driver switching off to port B LOW-to-HIGH transition; port A to port B

10.2 Performance curves



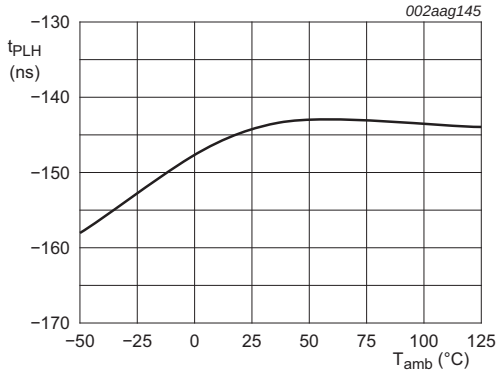
$V_{CC(A)}$ = 1.1 V; $V_{CC(B)}$ = 3.3 V

Fig 10. Typical port B to port A propagation delay versus ambient temperature



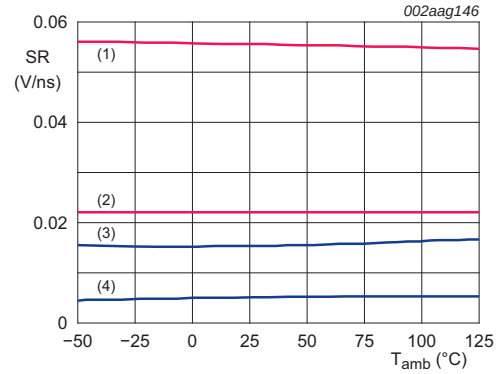
$V_{CC(A)}$ = 1.1 V; $V_{CC(B)}$ = 3.3 V

Fig 11. Typical port A to port B port propagation delay versus ambient temperature



$V_{CC(A)}$ = 1.1 V; $V_{CC(B)}$ = 3.3 V

Fig 12. Typical port A to port B LOW to HIGH propagation delay versus ambient temperature



$V_{CC(A)}$ = 1.1 V; $V_{CC(B)}$ = 3.3 V

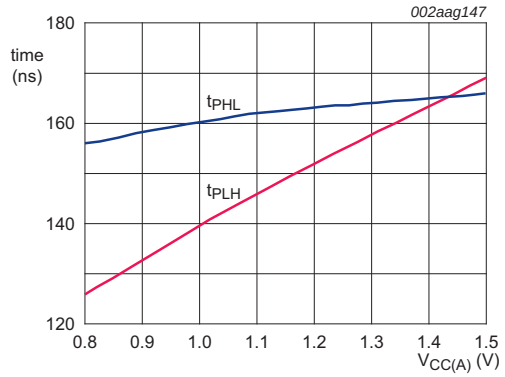
(1) Slew rate of falling signal, port B

(2) Slew rate of rising signal, port B

(3) Slew rate of falling signal, port A

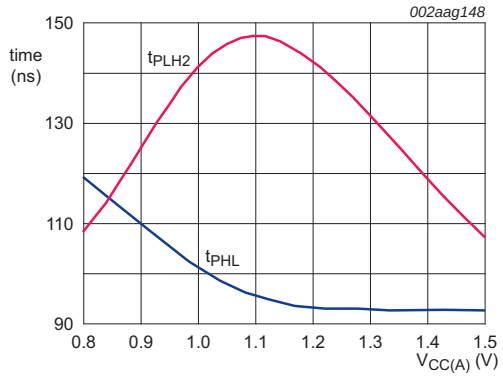
(4) Slew rate of rising signal, port A

Fig 13. Typical slew rate versus ambient temperature



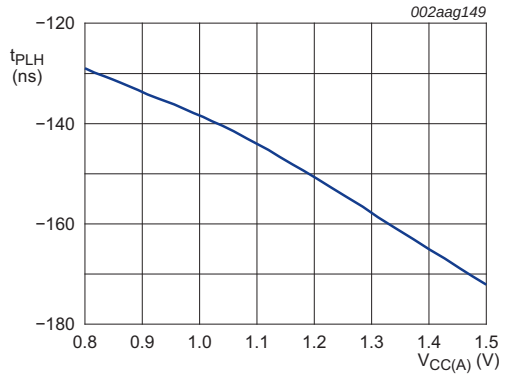
T_{amb} = 27 °C; $V_{CC(B)}$ = 3.3 V

Fig 14. Typical port B to port A propagation delay versus port A supply voltage



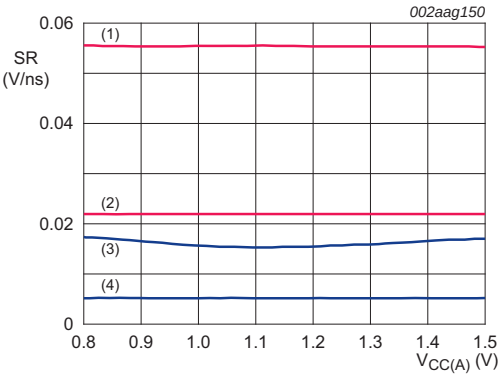
T_{amb} = 27 °C; $V_{CC(B)}$ = 3.3 V

Fig 15. Typical port A to port B propagation delay versus port A supply voltage



T_{amb} = 27 °C; $V_{CC(B)}$ = 3.3 V

Fig 16. Typical port A to port B LOW to HIGH propagation delay versus port A supply voltage



T_{amb} = 27 °C; $V_{CC(B)}$ = 3.3 V

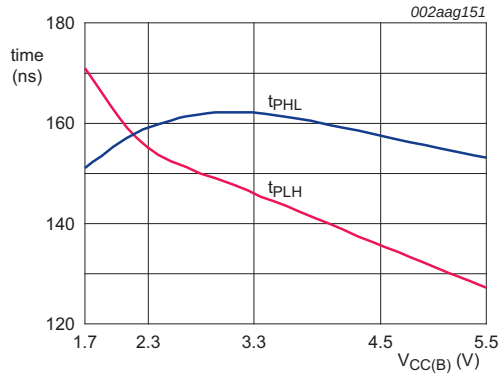
(1) Slew rate of falling signal, port B

(2) Slew rate of rising signal, port B

(3) Slew rate of falling signal, port A

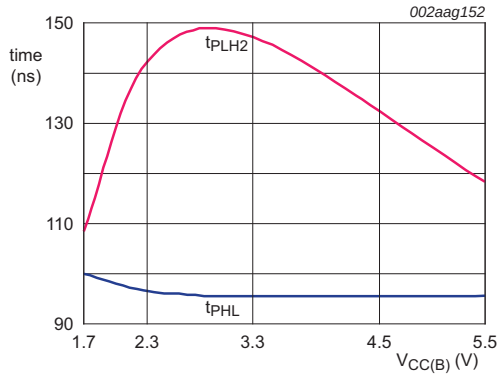
(4) Slew rate of rising signal, port A

Fig 17. Typical slew rate versus port A supply voltage



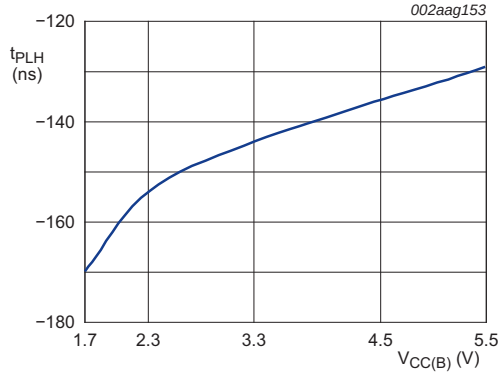
T_{amb} = 27 °C; $V_{CC(A)}$ = 1.1 V

Fig 18. Typical port B to port A propagation delay versus port B supply voltage



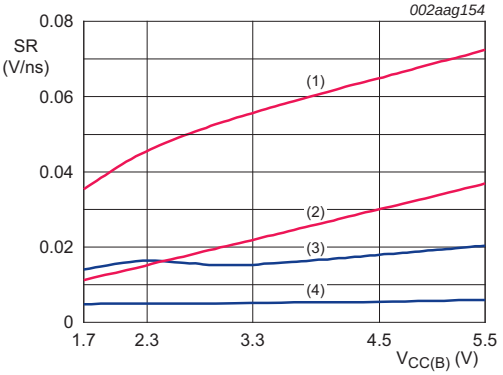
T_{amb} = 27 °C; $V_{CC(A)}$ = 1.1 V

Fig 19. Typical port A to port B propagation delay versus port B supply voltage



T_{amb} = 27 °C; $V_{CC(A)}$ = 1.1 V

Fig 20. Typical port A to port B LOW to HIGH propagation delay versus port B supply voltage



T_{amb} = 27 °C; $V_{CC(A)}$ = 1.1 V

(1) Slew rate of falling signal, port B

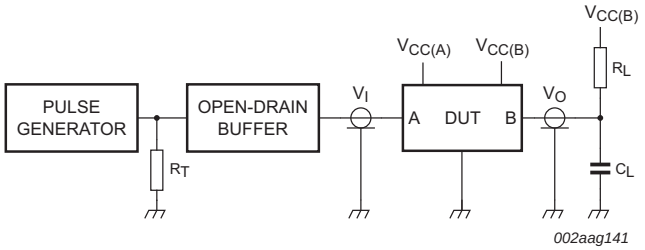
(2) Slew rate of rising signal, port B

(3) Slew rate of falling signal, port A

(4) Slew rate of rising signal, port A

Fig 21. Typical slew rate versus port B supply voltage

11. Test information

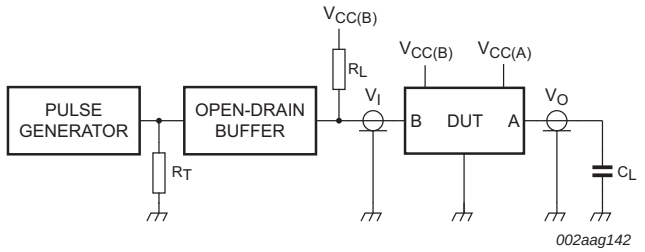


R_L = load resistor; 1.35 kΩ on port B

C_L = load capacitance includes jig and probe capacitance; 50 pF

R_T = termination resistance should be equal to Z_o of pulse generators

Fig 22. Test circuit for open-drain outputs A to B



R_L = load resistor; 1.35 kΩ on port B

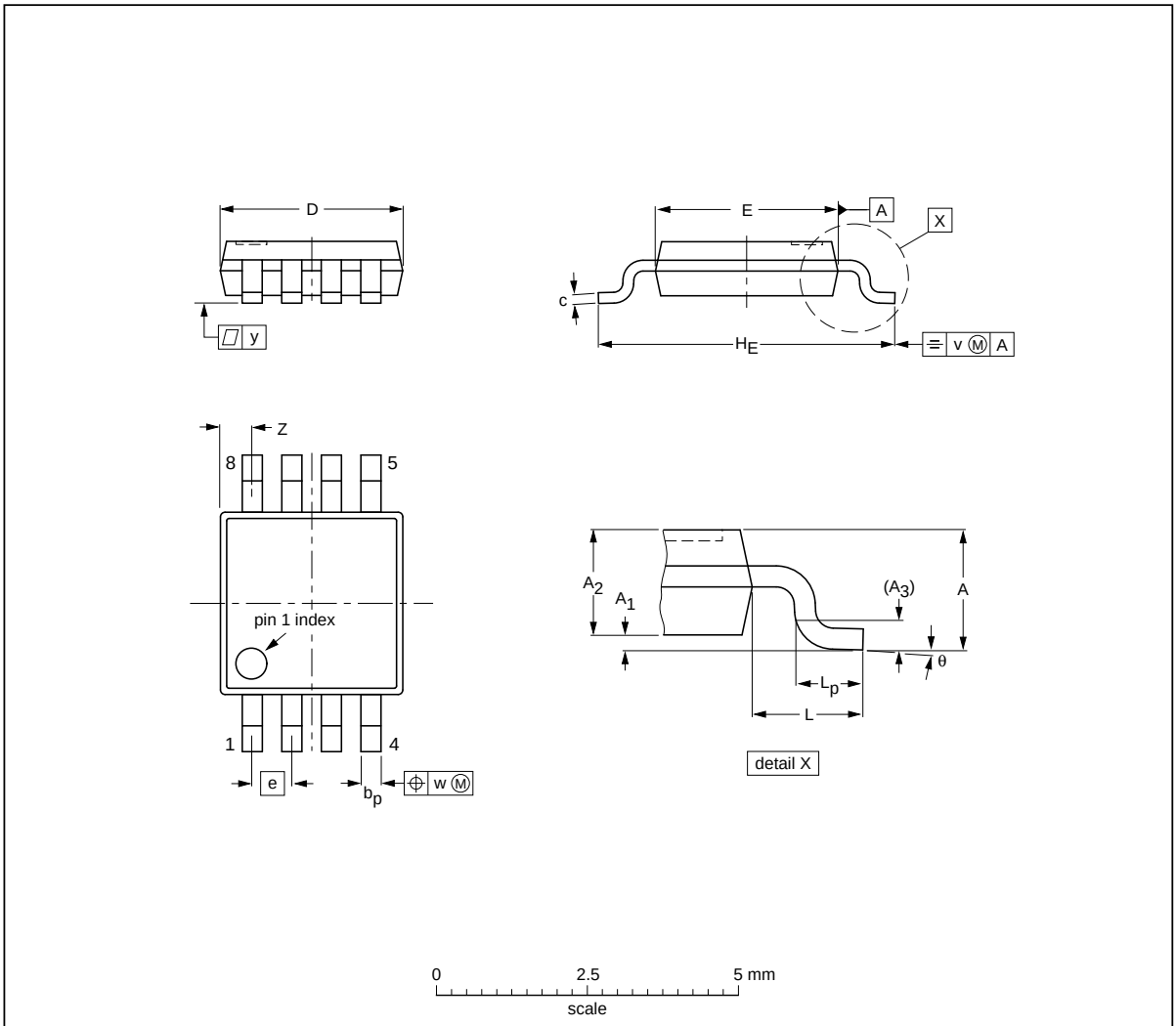
C_L = load capacitance includes jig and probe capacitance; 50 pF

R_T = termination resistance should be equal to Z_o of pulse generators

Fig 23. Test circuit for open-drain outputs B to A

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

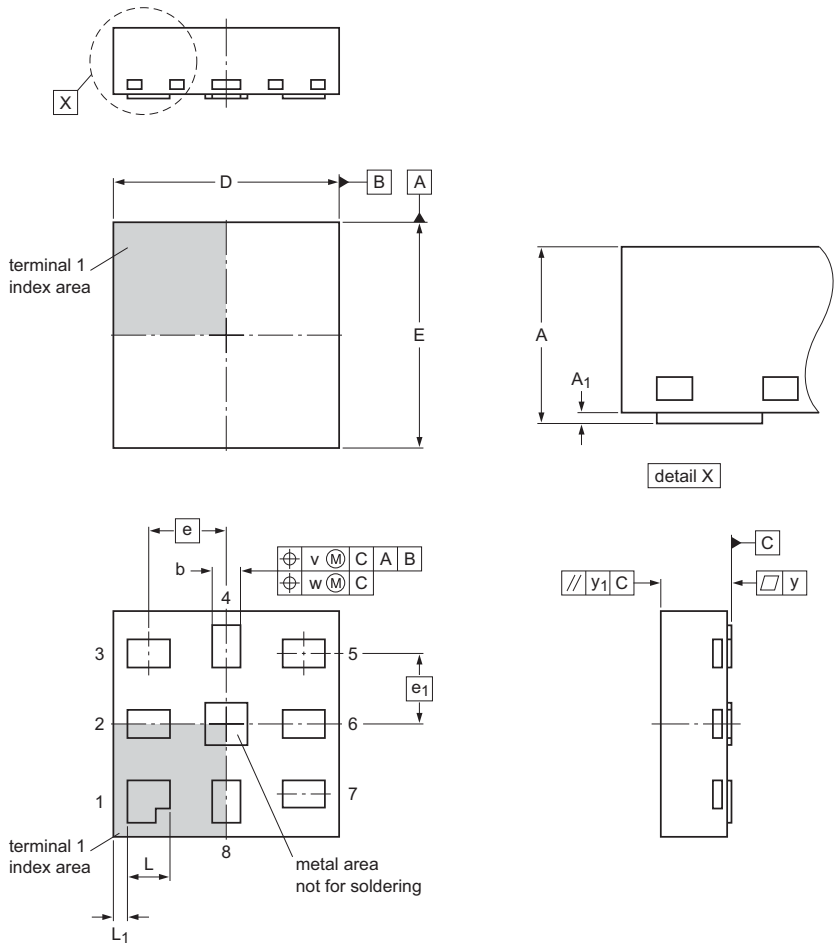
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 24. Package outline SOT505-1 (TSSOP8)

XQFN8: plastic, extremely thin quad flat package; no leads; 8 terminals; body 1.6 x 1.6 x 0.5 mm **SOT902-2**



Dimensions

Unit(1)		A	A_1	b	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	max	0.5	0.05	0.25	1.65	1.65			0.35	0.15				
	nom			0.20	1.60	1.60	0.55	0.5	0.30	0.10	0.1	0.05	0.05	0.05
	min		0.00	0.15	1.55	1.55			0.25	0.05				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot902-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT902-2	- - -	MO-255	- - -			~~10-11-02~~ 11-03-31

Fig 25. Package outline SOT902-2 (XQFN8)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 26) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7 and 8

Table 7. SnPb eutectic process (from J-STD-020C)

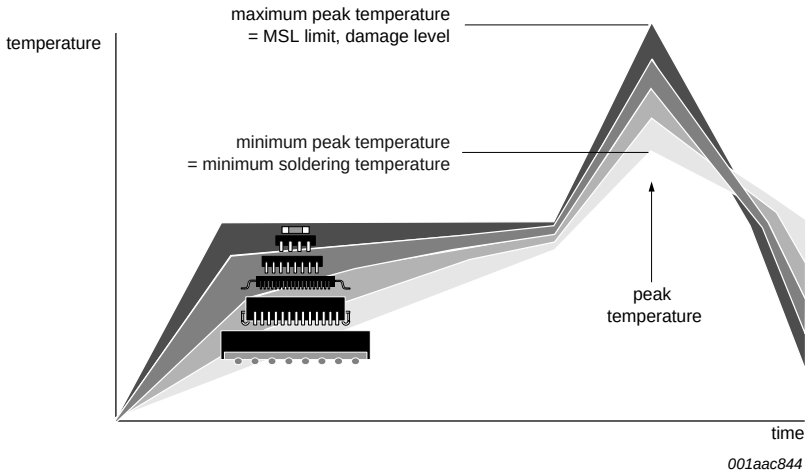
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 8. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 26.



MSL: Moisture Sensitivity Level

Fig 26. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 9. Abbreviations

Acronym	Description
ATE	Automated Test Equipment
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
ESD	ElectroStatic Discharge
HBM	Human Body Model
I/O	Input/Output
I²C-bus	Inter-Integrated Circuit bus
NMOS	Negative-channel Metal-Oxide Semiconductor
RC	Resistor-Capacitor network
SMBus	System Management Bus

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9509A v.1	20120229	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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