



# 16:1 Serializer, 3.3V, 2.5Gbps, SDH/SONET, with Clock Synthesis and LVPECL Inputs

## ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)

V<sub>CC</sub> .....-0.5V to +5.0V  
All Inputs, FIL+, FIL- .....-0.5V to (V<sub>CC</sub> + 0.5V)

Output Currents

PECL Outputs (SDO±, SCLKO±, PCLKO±) .....50mA  
CML Outputs (SLBO±).....15mA

Continuous Power Dissipation (T<sub>A</sub> = +85°C)

64-Pin TQFP-EP (derate 45.5mW/°C above +85°C) .....2.9W

Operating Temperature Range .....-40°C to +85°C

Storage Temperature Range .....-60°C to +150°C

Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(V<sub>CC</sub> = +3.0V to +3.6V, PECL loads = 50Ω ±1% to (V<sub>CC</sub> - 2V), CML loads = 50Ω ±1% to V<sub>CC</sub>, T<sub>A</sub> = -40°C to +85°C. Typical values are at V<sub>CC</sub> = +3.3V and T<sub>A</sub> = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I <sub>CC</sub>	PECL outputs unterminated, SOS = iow		150	230	mA
<b>PECL OUTPUTS (SDO±, SCLKO±, PCLKO±)</b>						
Output Voltage High	V <sub>OH</sub>	T <sub>A</sub> = 0°C to +85°C	V <sub>CC</sub> - 1.025		V <sub>CC</sub> - 0.88	V
		T <sub>A</sub> = -40°C	V <sub>CC</sub> - 1.085		V <sub>CC</sub> - 0.88	
Output Voltage Low	V <sub>OL</sub>	T <sub>A</sub> = 0°C to +85°C	V <sub>CC</sub> - 1.81		V <sub>CC</sub> - 1.62	V
		T <sub>A</sub> = -40°C	V <sub>CC</sub> - 1.83		V <sub>CC</sub> - 1.555	
<b>PECL INPUTS (PDI<sub>-</sub>, PCLKI±, RCLK±)</b>						
Input High Voltage	V <sub>IH</sub>		V <sub>CC</sub> - 1.16		V <sub>CC</sub> - 0.88	V
Input Low Voltage	V <sub>IL</sub>		V <sub>CC</sub> - 1.81		V <sub>CC</sub> - 1.48	V
Input Current High PDI <sub>-</sub> , RCLKI±	I <sub>IH</sub>		-10		+10	μA
Input Current Low PDI <sub>-</sub> , RCLKI±	I <sub>IL</sub>		-10		+10	μA
Input Current High PCLKI±	I <sub>IH</sub>		-60		+60	μA
Input Current Low PCLKI±	I <sub>IL</sub>		-60		+60	μA
<b>PROGRAMMING INPUT (CLKSET)</b>						
CLKSET Input Current	I <sub>CLKSET</sub>	CLKSET = GND or V <sub>CC</sub>			±500	μA
<b>TTL INPUT (SOS)</b>						
TTL Input High Voltage	V <sub>IH</sub>		2.0			V
TTL Input Low Voltage	V <sub>IL</sub>				0.8	V
TTL Input High Current	I <sub>IH</sub>		-10		+10	μA
TTL Input Low Current	I <sub>IL</sub>		-10		+10	μA
<b>CURRENT MODE LOGIC (CML) OUTPUTS (SLBO±)</b>						
CML Differential Output Voltage Swing	V <sub>OD</sub>	R <sub>L</sub> = 50 Ω to V <sub>CC</sub>	100		400	mV
CML Single-Ended Output Impedance	R <sub>O</sub>			50		Ω

# 16:1 Serializer, 3.3V, 2.5Gbps, SDH/SONET, with Clock Synthesis and LVPECL Inputs

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC} = +3.0V$  to  $+3.6V$ , PECL loads =  $50\Omega \pm 1\%$  to  $(V_{CC} - 2V)$ , CML loads =  $50\Omega \pm 1\%$  to  $V_{CC}$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ . Typical values are at  $T_A = +25^\circ C$  and  $V_{CC} = +3.3V$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Rate	f <sub>SCLK</sub>			2.488		GHz
Parallel Data Setup Time	t <sub>SU</sub>	(Notes 2, 3)	300			ps
Parallel Data-Hold Time	t <sub>H</sub>	(Notes 2, 3)	700			ps
PCLKO to PCLKI Skew	t <sub>SKEW</sub>	Figure 1	0		+4.0	ns
Output Jitter Generation (SCLKO±)		Jitter bandwidth = 12kHz to 20MHz			3	psRMS
PECL Differential Output (SDO±, SCLKO±) Rise/Fall Time	t <sub>R</sub> , t <sub>F</sub>	20% to 80%			120	ps
Parallel Input Clock Rate	f <sub>PCLKI</sub>			155.52		MHz
Reference Clock Input (RCLK±) Rise/Fall Time	t <sub>R</sub> , t <sub>F</sub>	20% to 80%, f = 155.52MHz			1.0	ns
Parallel Clock Output (PCLKO±) Rise/Fall Time	t <sub>R</sub> , t <sub>F</sub>	20% to 80%			1.0	ns
Serial-Clock Output (SCLKO±) to Serial-Data Output (SDO±) Delay	t <sub>SCLK-SD</sub>	SCLKO rising edge to SDO edge	110		290	ps

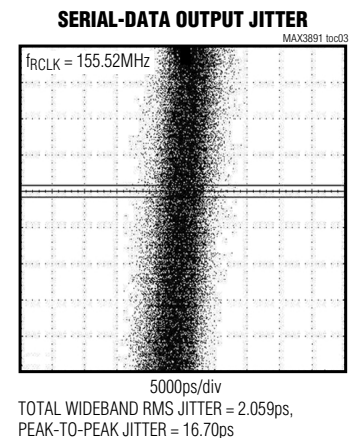
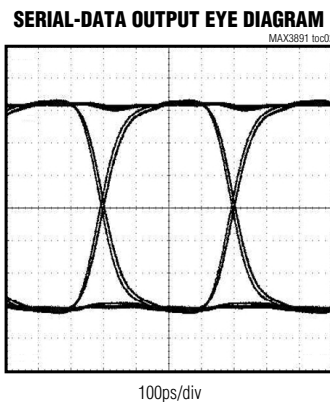
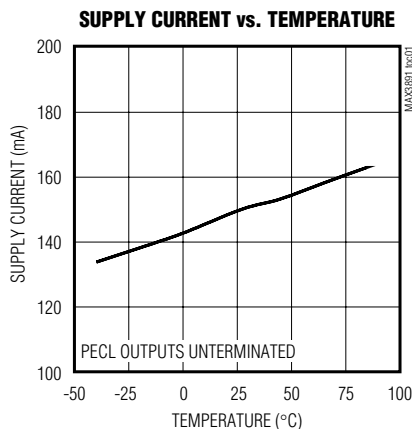
**Note 1:** AC characteristics are guaranteed by design and characterization.

**Note 2:** Setup and hold times are relative to the rising edge of PCLKI+, measured by applying a 155.52MHz differential parallel clock with rise/fall time = 1ns (20% to 80%). See Figure 1.

**Note 3:** Setup and hold time measurements assume that the PCLKI and PDI signals are from the same source and have identical common-mode voltages, swings, and slew rates.

## Typical Operating Characteristics

( $V_{CC} = +3.3V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# 16:1 Serializer, 3.3V, 2.5Gbps, SDH/SONET, with Clock Synthesis and LVPECL Inputs

## Pin Description

PIN	NAME	FUNCTION
1, 17, 33, 48, 49, 63	GND	Ground
2, 5, 7, 10, 13, 14, 19, 21, 23, 25, 27, 29, 31, 32, 35, 37, 39, 41, 43, 45, 47, 51, 53, 56, 60, 64	VCC	+3.3V Supply Voltage
3	SLBO-	System Loopback Negative Output. Enabled when SOS is high.
4	SLBO+	System Loopback Positive Output. Enabled when SOS is high.
6	SOS	System Loopback Output Select, TTL Input. System loopback disabled when low.
8	SCLKO-	Negative PECL Serial Clock Output
9	SCLKO+	Positive PECL Serial Clock Output
11	SDO-	Negative PECL Serial Data Output
12	SDO+	Positive PECL Serial Data Output
15	PCLKI+	Positive PECL Parallel Clock Input. Connect the incoming parallel-clock signal to the PCLKI inputs. Note that data is updated on the positive transition of the PCLKI signal.
16	PCLKI-	Negative PECL Parallel Clock Input. Connect the incoming parallel-clock signal to the PCLKI inputs. Note that data is updated on the positive transition of the PCLKI signal.
18, 20, 22, 24, 26, 28, 30, 34, 36, 38, 40, 42, 44, 46, 50, 52	PDI15 to PDIO	Single-Ended PECL Parallel Data Inputs. Data is clocked on the PCLKI positive transition. PDI15 is transmitted first.
54	PCLKO+	Positive PECL Parallel Clock Output. Use positive transition of PCLKO to clock the overhead management circuit.
55	PCLKO-	Negative PECL Parallel Clock Output. Use positive transition of PCLKO to clock the overhead management circuit.
57	RCLK+	Positive Reference Clock Input. Connect a PECL-compatible crystal reference clock to the RCLK inputs.
58	RCLK-	Negative Reference Clock Input. Connect a PECL-compatible crystal reference clock to the RCLK inputs.
59	CLKSET	Reference Clock Rate Programming Pin: CLKSET = VCC: Reference Clock Rate = 155.52MHz CLKSET = Open: Reference Clock Rate = 77.76MHz CLKSET = 20k $\Omega$ to GND: Reference Clock Rate = 51.84MHz CLKSET = GND: Reference Clock Rate = 38.88MHz
61	FIL-	Filter Capacitor Input. Connect a 0.33 $\mu$ F capacitor between FIL+ and FIL-
62	FIL+	Filter Capacitor Input. Connect a 0.33 $\mu$ F capacitor between FIL+ and FIL-
EP	Exposed Pad	Ground. This must be soldered to a circuit board for proper electrical and thermal performance (see exposed pad package information).

# 16:1 Serializer, 3.3V, 2.5Gbps, SDH/SONET, with Clock Synthesis and LVPECL Inputs

MAX3891

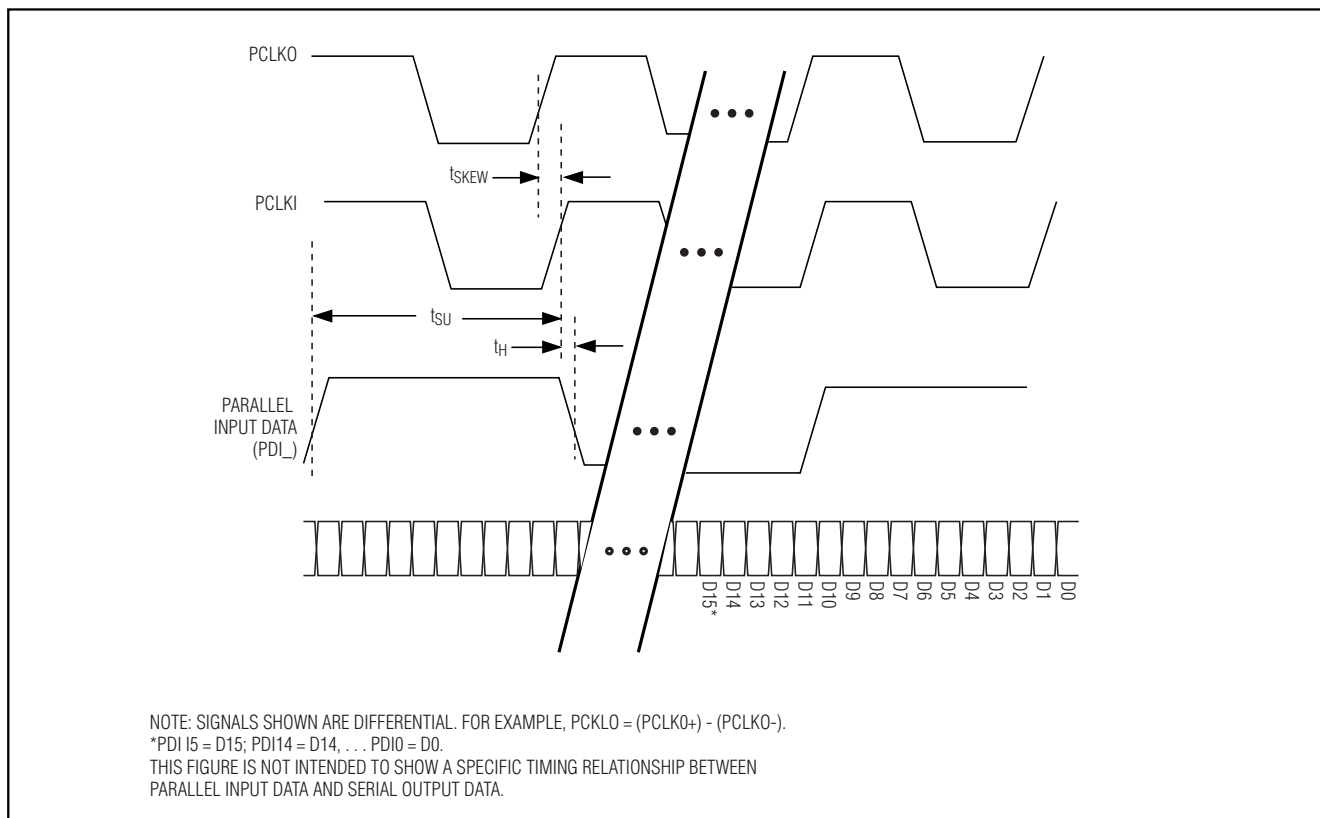


Figure 1. Timing Diagram

## Detailed Description

The MAX3891 converts 16-bit wide, 155Mbps data to 2.5Gbps serial data (Figure 2). The MAX3891 is composed of a 16-bit parallel input register, a 16-bit shift register, control and timing logic, PECL output buffers and a frequency-synthesizing PLL, consisting of a phase/frequency detector, loop filter/amplifier, voltage-controlled oscillator, and prescaler.

The PLL synthesizes an internal 2.5Gbps reference used to clock the output shift register. This clock is generated from the external 155.52MHz, 77.76MHz, 51.84MHz, or 38.88MHz reference-clock signal (RCLK).

The incoming parallel data is clocked into the MAX3891 on the rising transition of the parallel clock-input signal (PCLKI). Proper operation is ensured if the parallel-input register is latched within a window of time ( $t_{\text{SKEW}}$ ),

defined with respect to the parallel clock-output signal (PCLKO). PCLKO is the synthesized 2.488Gbps internal serial-clock signal divided by 16. The allowable PCLKO to PCLKI skew is 0ns to 4ns. This defines a timing window after the PCLKO rising edge, during which a PCLKI rising edge may occur (Figure 1).

## System Loopback

The MAX3891 is designed to provide system loopback testing. The loopback outputs (SLBO) of the MAX3891 may be directly connected to the loopback inputs of a deserializer (MAX3881) for system diagnostics. To enable the SLBO outputs, apply a TTL logic-high signal to the SOS input. The same signal that controls the SOS enable input may also be used to control the SIS enable input on the MAX3881.

# 16:1 Serializer, 3.3V, 2.5Gbps, SDH/SONET, with Clock Synthesis and LVPECL Inputs

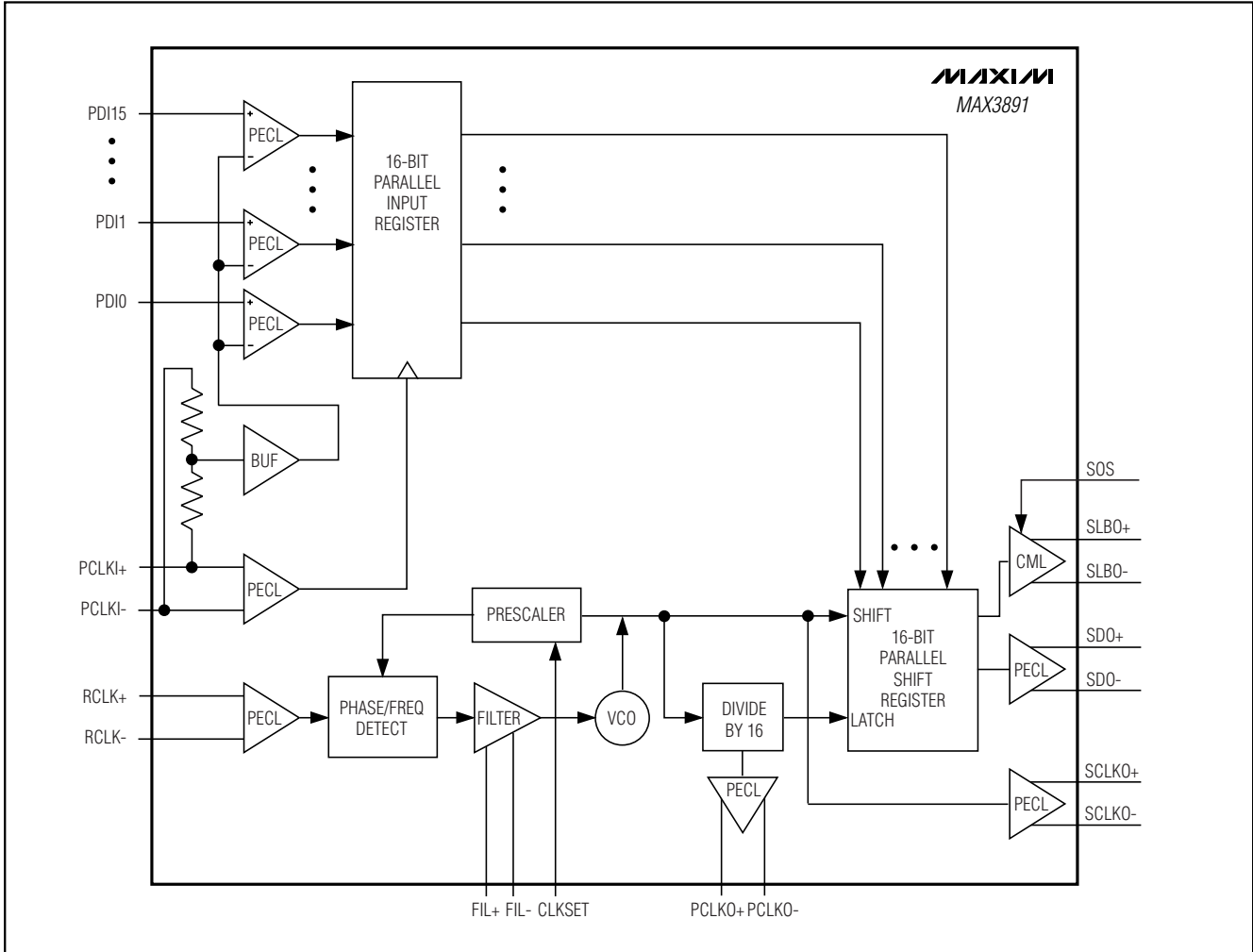


Figure 2. Functional Block Diagram

## Applications Information

### Setup and Hold Time Requirements

The setup and hold-time specifications assume that the parallel clock-input signal (PCLKI) and parallel-data input signal (PDI<sub>-</sub>) are from the same source. They should have identical common-mode voltages, signal amplitudes, and slew rates. If PCLKI and PDI<sub>-</sub> differ significantly, the setup and hold-time requirements must be modified to account for these differences. Define  $t_{DEG}$  as the adjustment to the setup and hold-time requirement when there are significant differences between PCLKI and PDI<sub>-</sub>.

$$t_{DEG} = V_{CM\_DIFF} \times \left( \frac{t_T}{V_{OH} - V_{OL}} \right)$$

where  $t_T$  is the transition time (20%–80%) of the parallel-data and clock-input signals,  $V_{OH}$  and  $V_{OL}$  are the input high and low voltage, respectively, of the parallel-data and clock-input signals, and  $V_{CM\_DIFF}$  is the difference in common-mode voltages of the parallel-data and clock-input signals.

# 16:1 Serializer, 3.3V, 2.5Gbps, SDH/SONET, with Clock Synthesis and LVPECL Inputs

The adjusted setup ( $t_{SUADJ}$ ) and hold-time ( $t_{HADJ}$ ) requirements become

$$t_{SUADJ} \text{ (or } t_{HADJ}) = t_{SU} \text{ (or } t_H) + t_{DEG}$$

## PECL Input and Output Terminations

It is important to bias the MAX3891's PECL data and clock IOs appropriately. Figures 3 and 4 show alternative PECL output termination methods. A circuit that provides  $50\Omega$  to  $(V_{CC} - 2V)$  should be used in conjunction with controlled impedance transmission lines for proper termination. Use Thevenin equivalent termination when a  $(V_{CC} - 2V)$  supply is not available. If AC-coupling is necessary, make sure that the coupling capacitor follows the  $50\Omega$  or Thevenin equivalent DC termination. To ensure best performance, the differential outputs ( $SDO_{\pm}$  and  $PCLKO_{\pm}$ ) must have balanced loads.

## Current-Mode Logic Outputs

The system loopback outputs (SLBO) of the MAX3891 are CML compatible. The configuration of the MAX3891 current-mode logic (CML) output circuit includes internal  $50\Omega$  back termination to  $V_{CC}$  (Figure 5). These outputs are intended to drive a terminated  $50\Omega$  transmission line.

## Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies and keep ground connections short. Use multiple vias where possible. Use controlled impedance transmission lines to interface with the MAX3891 clock and data inputs and outputs.

## Exposed Pad Package

The 64-pin exposed pad (EP) TQFP incorporates features that provide a very low thermal-resistance path for heat removal. The MAX3891 EP must be soldered directly to a ground plane with good thermal conductance.

## Chip Information

TRANSISTOR COUNT: 1712

PROCESS: Bipolar

# 16:1 Serializer, 3.3V, 2.5Gbps, SDH/SONET, with Clock Synthesis and LVPECL Inputs

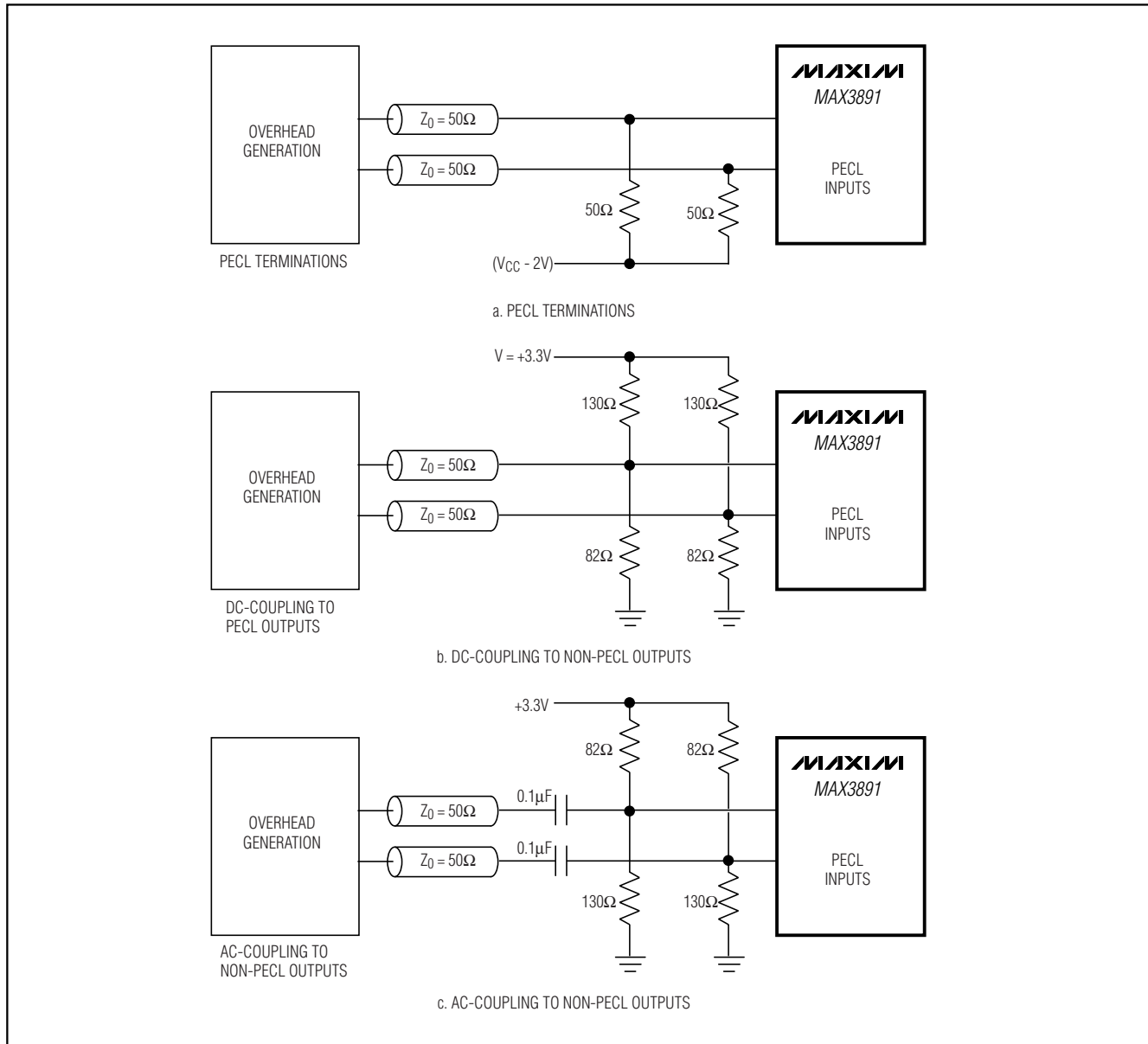


Figure 3. Alternative PECL-Input Termination



# 16:1 Serializer, 3.3V, 2.5Gbps, SDH/SONET, with Clock Synthesis and LVPECL Inputs

MAX3891

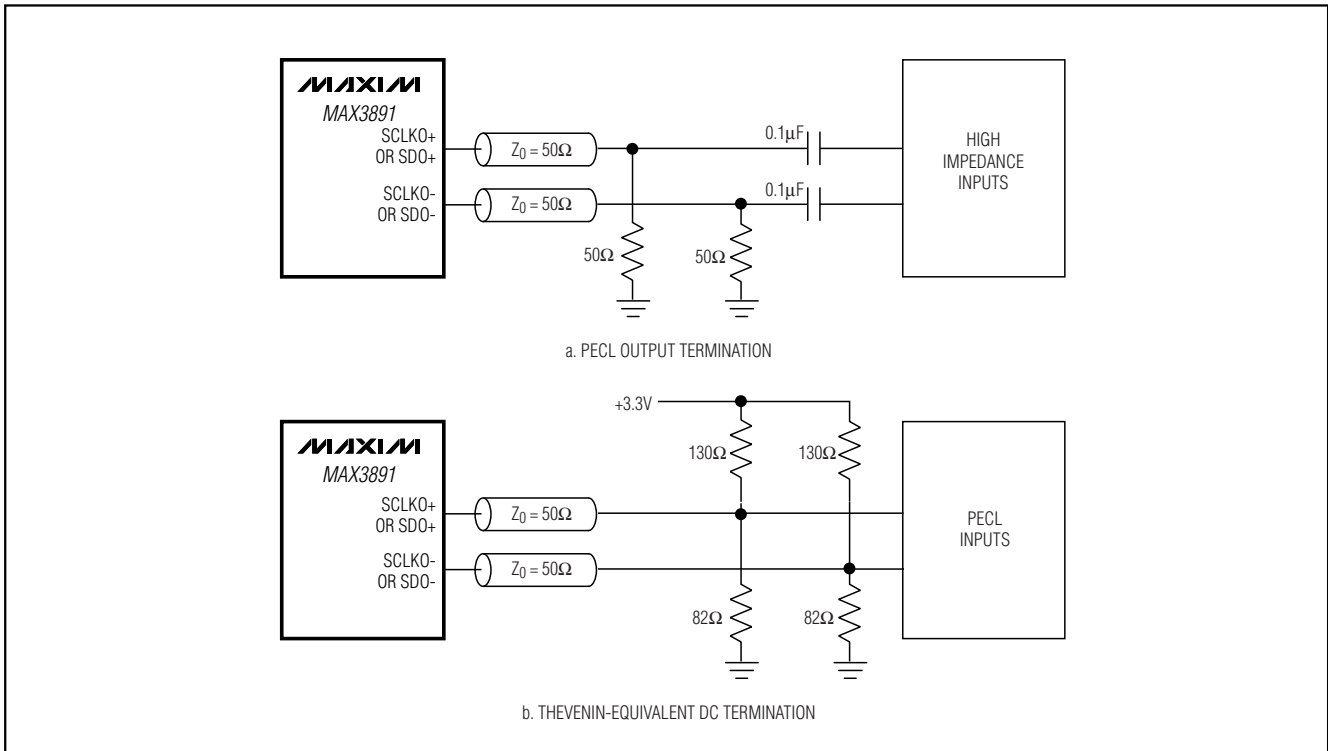


Figure 4. Alternative PECL-Output Termination

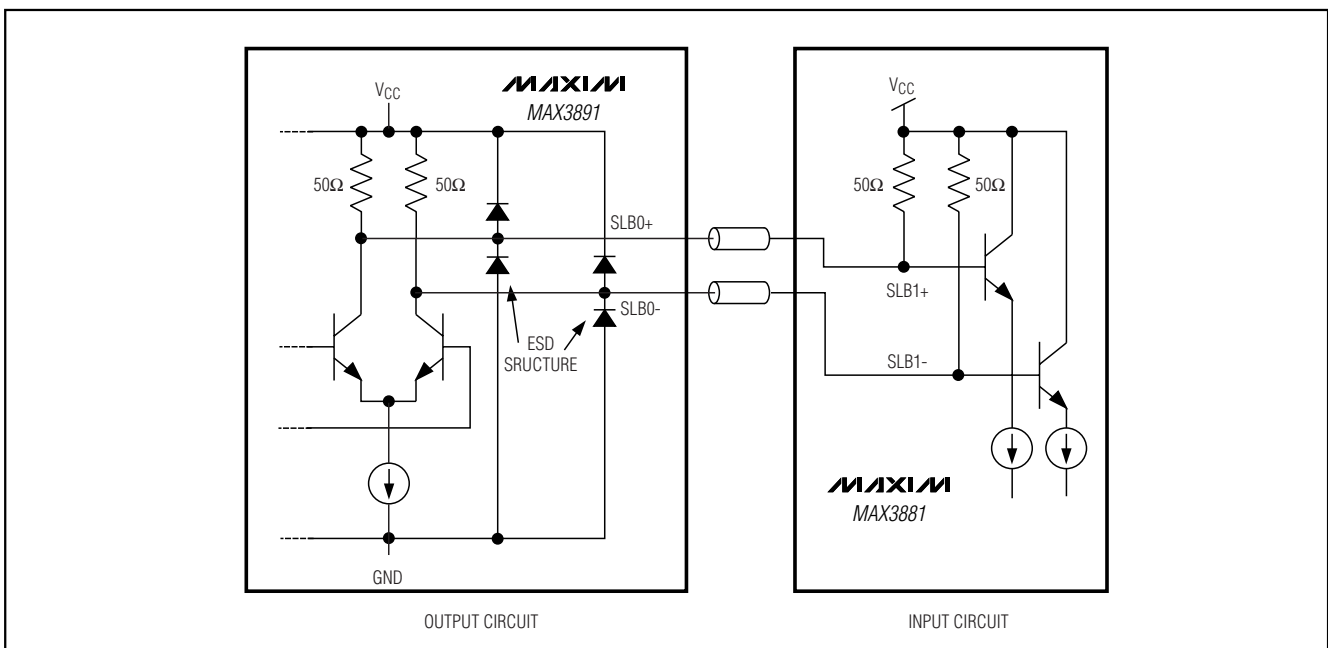


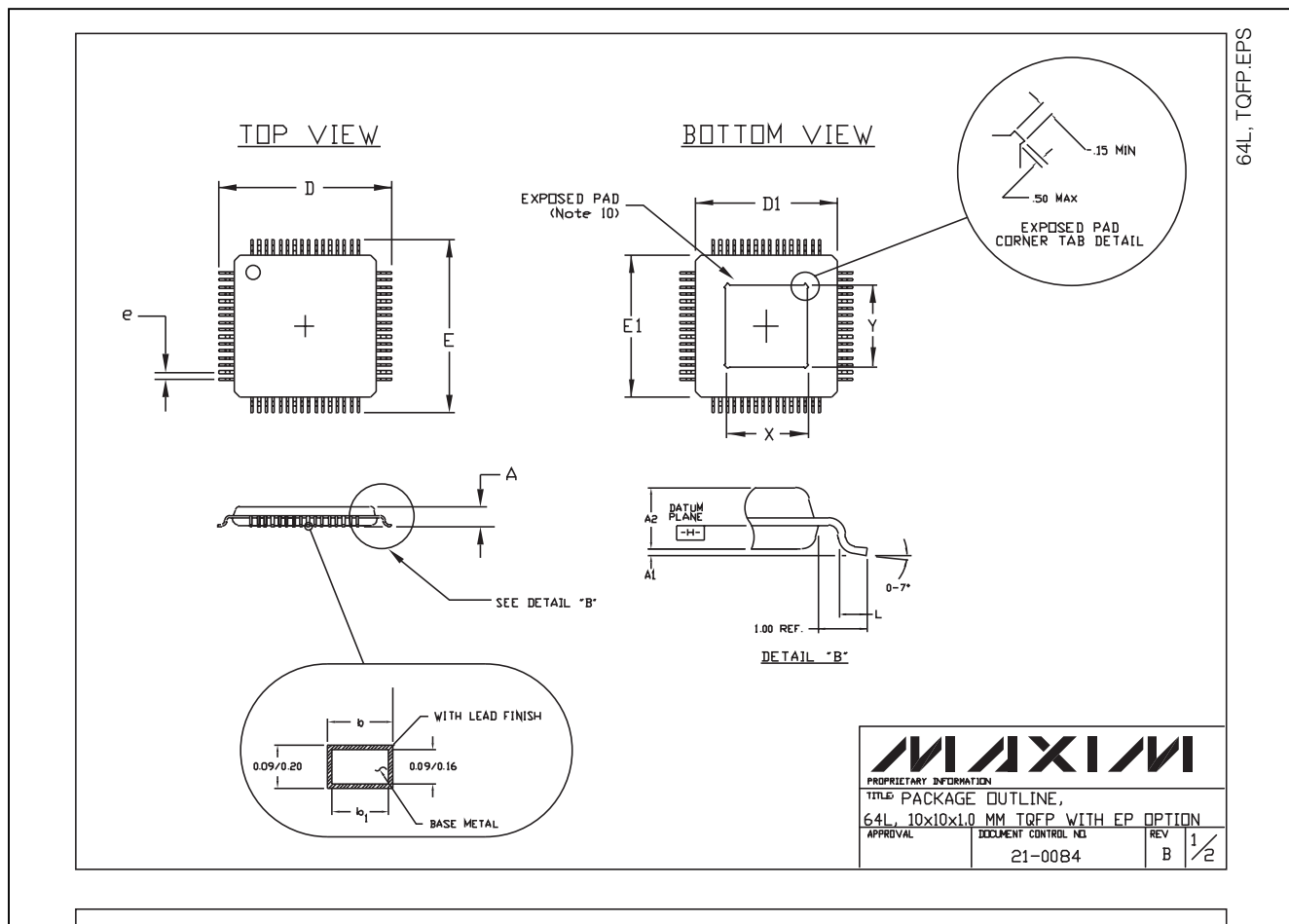
Figure 5. Current-Mode Logic



# 16:1 Serializer, 3.3V, 2.5Gbps, SDH/SONET, with Clock Synthesis and LVPECL Inputs

## Package Information

MAX3891



# 16:1 Serializer, 3.3V, 2.5Gbps, SDH/SONET, with Clock Synthesis and LVPECL Inputs

## Package Information (continued)

**NOTES:**

1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE [-H-] IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.  
ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION AJ.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. DIMENSIONS X & Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY. SEE INDIVIDUAL PRODUCT DATASHEET TO DETERMINE IF A PRODUCT USES EXPOSED PAD PACKAGE.

SYMBOL	JEDEC VARIATION	
	ALL DIMENSIONS IN MILLIMETERS	
	AJ	
	MIN.	MAX.
A	~	1.20
A <sub>1</sub>	0.05	0.15
A <sub>2</sub>	0.95	1.05
D	12.00 BSC.	
D <sub>1</sub>	10.00 BSC.	
E	12.00 BSC.	
E <sub>1</sub>	10.00 BSC.	
L	0.45	0.75
N	64	
e	0.50 BSC.	
b	0.17	0.27
b <sub>1</sub>	0.17	0.23
*X	4.7	5.30
*Y	4.70	5.30

\* EXPOSED PAD (Note 10)

<small>PROPRIETARY INFORMATION</small>		
TITLE: PACKAGE OUTLINE, 64L, 10x10x1.0 MM TQFP WITH EP OPTION		
APPROVAL	DOCUMENT CONTROL NO. 21-0084	REV B 2/2

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

12 \_\_\_\_\_ **Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600**