19-5644; Rev 1; 3/11

EVALUATION KIT AVAILABLE

MAXIM

HDCP Gigabit Multimedia Serial Link Serializer/Deserializer

General Description

The MAX9263/MAX9264 chipset extends Maxim's gigabit multimedia serial link (GMSL) technology to include high-bandwidth digital content protection (HDCP) encryption for content protection of DVD and Blu-ray™ video and audio data. The MAX9263 serializer, or any HDCP-GMSL serializer, pairs with the MAX9264 deserializer, or any HDCP-GMSL deserializer, to form a digital serial link for the transmission of control data and HDCP encrypted video and audio data. GMSL is an HDCP technology approved protocol by Digital Content Protection (DCP), LLC.

The parallel interface is programmable for 24-bit or 32-bit width and operates with a pixel clock of 8.33MHz to 104MHz (24 bit) or 6.25MHz to 78MHz (32 bit). When programmed for 24-bit or 32-bit width, three inputs are for I^2S audio, supporting a sampling frequency from 8kHz to 192kHz and a sample depth of 4 bits to 32 bits. The embedded control channel forms a full-duplex differential 9.6kbps to 1Mbps UART link between the serializer and deserializer. An electronic control unit (ECU), or microcontroller (µC), can be located on the serializer side of the link (typical for video display), on the deserializer side of the link (typical for image sensing), or on both sides (typical for HDCP video display repeaters). The control channel enables ECU/µC control of peripherals on the remote side, such as backlight control, touch screen, and perform HDCP-related operations.

The serial link signaling is AC-coupled CML with 8b/10b coding. For driving longer cables, the serializer has programmable pre/deemphasis, and the deserializer has a programmable channel equalizer. The GMSL devices have programmable spread spectrum on the serial (serializer) and parallel (deserializer) output. The serial link input and output meet ISO 10605 and IEC 61000-4-2 ESD standards. The serializer core supply is 1.8V and the deserializer core supply is 3.3V. The I/O supply is 1.8V to 3.3V. Both devices are available in a 64-pin TQFP package with an exposed pad and are specified over the -40°C to +105°C automotive temperature range.

Applications

High-Resolution Automotive Navigation

Rear-Seat Infotainment

Megapixel Camera Systems

Blu-ray is a trademark of Blu-ray Disc Association.

Features

- **HDCP Encryption Enable/Disable Programmable Through Control Channel**
- **Control Channel Handles All HDCP Protocol Transactions—Separate Control Bus Not Required**
- **HDCP Keys Preprogrammed in Secure Nonvolatile Memory**
- **2.5Gbps Payload Data Rate (3.125Gbps with Overhead)**
- **AC-Coupled Serial Link with 8b/10b Line Coding**
- **8.33MHz to 104MHz (24-Bit Mode) or 6.25MHz to 78MHz (32-Bit Mode) Pixel Clock**
- **4-Bit to 32-Bit Word Length, 8kHz to 192kHz I^2S Audio Channel Supports High-Definition Audio**
- **Embedded Half-/Full-Duplex Bidirectional Control Channel**
  - **Base Mode: 9.6kbps to 1Mbps**
  - **Bypass Mode: 9.6kbps to 1Mbps**
- **Interrupt Supports Touch-Screen Displays**
- **Remote-End I^2C Master for Peripherals**
- **Programmable Pre/Deemphasis and Channel Equalizer for 15m Cable Drive at 3.125Gbps**
- **Programmable Spread Spectrum on Serial or Parallel Output Reduces EMI**
- **Deserializer Serial-Data Clock Recovery Eliminates External Reference Clock**
- **Auto Data-Rate Detection Allows On-The-Fly Data-Rate Change**
- **Bypassable PLL on Serializer Pixel Clock Input for Jitter Attenuation**
- **Built-In PRBS Generator/Checker for BER Testing of the Serial Link**
- **Fault Detection of Serial Link Shorted Together, to Ground, to Battery, or Open**
- **ISO 10605 and IEC 61000-4-2 ESD Tolerance**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9263GCB/V+	-40°C to +105°C	64 TQFP-EP*
MAX9263GCB/V+T	-40°C to +105°C	64 TQFP-EP*
MAX9264GCB/V+	-40°C to +105°C	64 TQFP-EP*
MAX9264GCB/V+T	-40°C to +105°C	64 TQFP-EP*

/V denotes an automotive qualified product.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

HDCP Gigabit Multimedia Serial Link Serializer/Deserializer

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND
- MAX9263 .... -0.5V to +1.9V
- MAX9264 .... -0.5V to +3.9V

DVDD to GND (MAX9263) .... -0.5V to +1.9V
DVDD to DGND (MAX9264) .... -0.5V to +3.9V
IOVDD to GND (MAX9263) .... -0.5V to +3.9V
IOVDD to IOGND (MAX9264) .... -0.5V to +3.9V
Any Ground to Any Ground .... -0.5V to +0.5V
OUT+, OUT- to AGND (MAX9263) .... -0.5V to +1.9V
IN+, IN- to AGND (MAX9264) .... -0.5V to +1.9V
LMN_ to AGND (MAX9263)
(15mA current limit) .... -0.5V to +3.9V
All Other Pins to GND (MAX9263) ...... -0.5V to (V_{IOVDD} + 0.5V)
All Other Pins to IOGND (MAX9264) ... -0.5V to (V_{IOVDD} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
64-Pin TQFP (derate 31.3mW/°C above +70°C) 2507.8mW
Operating Temperature Range .... -40°C to +105°C
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

64 TQFP-EP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 39.1°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .... 1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

MAX9263 DC ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (DIN_, PCLKIN, SD, SCK, WS, $\overline{AUTOS}$, MS, CDS, $\overline{PWDN}$, SSEN, DRS, ES, BWS)						
High-Level Input Voltage	V_{IH1}	DIN_, PCLKIN, $\overline{AUTOS}$, MS, CDS, SSEN, DRS, ES, BWS	0.65 x V_{IOVDD}			V
		SD, SCK, WS	0.7 x V_{IOVDD}			
Low-Level Input Voltage	V_{IL1}				0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0 to V_{IOVDD}	-10		+10	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA			-1.5	V
SINGLE-ENDED OUTPUT (INT)						
High-Level Output Voltage	V_{OH1}	I_{OUT} = -2mA	V_{IOVDD} - 0.2			V
Low-Level Output Voltage	V_{OL1}	I_{OUT} = 2mA			0.2	V
OUTPUT Short-Circuit Current	I_{OS}	V_O = V_{GND}, V_{IOVDD} = 3.0V to 3.6V	16	35	64	mA
		V_O = V_{GND}, V_{IOVDD} = 1.7V to 1.9V	3	12	21	
I^2C/UART, I/O, AND OPEN-DRAIN OUTPUTS (RX/SDA, TX/SCL, $\overline{LFLT}$)						
High-Level Input Voltage	V_{IH2}		0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}				0.3 x V_{IOVDD}	V

MAX9263 DC ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Current	I_{IN2}	V_{IN} = 0 to V_{IOVDD} (Note 2)		-110		+5	µA
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
DIFFERENTIAL OUTPUT (OUT+, OUT-)							
Differential Output Voltage	V_{OD}	Preemphasis off (Figure 1)		300	400	500	mV
		3.3dB preemphasis setting (Figure 2)		350		610	
		3.3dB deemphasis setting (Figure 2)		240		425	
Change in V_{OD} Between Complementary Output States	ΔV_{OD}					15	mV
Output Offset Voltage (V_{OUT+} + V_{OUT-})/2 = V_{OS}	V_{OS}	Preemphasis off		1.1	1.4	1.56	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}					15	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V		-60			mA
		V_{OUT+} or V_{OUT-} = 1.9V				25	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V				25	mA
Output Termination Resistance (Internal)	R_O	From OUT+, OUT- to V_{AVDD}		45	54	63	Ω
REVERSE CONTROL-CHANNEL RECEIVER (OUT+, OUT-)							
High Switching Threshold	V_{CHR}					27	mV
Low Switching Threshold	V_{CLR}			-27			mV
LINE-FAULT-DETECTION INPUTS (LMN_)							
Short-to-GND Threshold	V_{TG}	Figure 3				0.3	V
Normal Thresholds	V_{TN}	Figure 3		0.57		1.07	V
Open Thresholds	V_{TO}	Figure 3		1.45		V_{IO} + 60mV	V
Open Input Voltage	V_{IO}	Figure 3		1.47		1.75	V
Short-to-Battery Threshold	V_{TE}	Figure 3		2.47			V
POWER SUPPLY							
Worst-Case Supply Current (Figure 4, Note 3)	I_{WCS}	BWS = GND	f_{PCLKIN} = 16.6MHz		105	132	mA
			f_{PCLKIN} = 33.3MHz		110	152	
			f_{PCLKIN} = 66.6MHz		120	160	
			f_{PCLKIN} = 104MHz		145	188	
Sleep Mode Supply Current	I_{CCS}				45	225	µA
Power-Down Supply Current	I_{CCZ}	$\overline{PWDN}$ = GND			7	180	µA

MAX9263 DC ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ESD PROTECTION							
OUT+, OUT-	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF (Note 4)			±8		kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF (Note 5)	Contact discharge		±10		
			Air discharge		±12		
		ISO 10605, R_D = 2kΩ, C_S = 330pF (Note 5)	Contact discharge		±10		
			Air discharge		±25		
All Other Pins	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF (Note 4)			±4		kV

MAX9263 AC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUT TIMING (PCLKIN)						
Clock Frequency	f_{PCLKIN}	BWS = GND, V_{DRS} = V_{IOVDD}	8.33		16.66	MHz
		BWS = GND, DRS = GND	16.66		104	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{IOVDD}	6.25		12.5	
		V_{BWS} = V_{IOVDD}, DRS = GND	12.5		78	
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T (Figure 5, Note 6)	35	50	65	%
Clock Transition Time	t_R, t_F	(Figure 5, Note 6)			4	ns
Clock Jitter	t_J	3.125Gbps, 300kHz sinusoidal jitter (Note 6)			800	$ps_{(P-P)}$
I^2C/UART PORT TIMING						
I^2C/UART Bit Rate			9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}	20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}	20		150	ns
Input Setup Time	t_{SET}	I^2C only (Figure 6, Note 6)	100			ns
Input Hold Time	t_{HOLD}	I^2C only (Figure 6, Note 6)	0			ns
SWITCHING CHARACTERISTICS						
Differential Output Rise/Fall Time	t_R, t_F	20% to 80%, V_{OD} ≥ 400mV, R_L = 100Ω, serial-bit rate = 3.125Gbps (Note 6)		90	150	ps
Total Serial Output Jitter	t_{TSOJ1}	3.125Gbps PRBS signal, measured at V_{OD} = 0V differential, preemphasis disabled (Figure 7)		0.25		UI

MAX9263 AC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Deterministic Serial Output Jitter	t_{DSOJ2}	3.125Gbps PRBS signal			0.15		UI
Parallel Data Input Setup Time	t_{SET}	(Figure 8, Note 6)		1			ns
Parallel Data Input Hold Time	t_{HOLD}	(Figure 8, Note 6)		1.5			ns
Serializer Delay (Notes 6, 7) (Figure 1)	t_{SD}	(Figure 9)	Spread spectrum enabled			2830	Bits
			Spread spectrum disabled			270	
Link Start Time	t_{LOCK}	(Figure 10)				3.5	ms
Power-Up Time	t_{PU}	(Figure 11)				6	ms
I^2S INPUT TIMING							
WS Frequency	f_{WS}	See Table 4		8		192	kHz
Sample Word Length	n_{WS}	See Table 4		4		32	bits
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times 2$		(8 x 4) x 2		(192 x 32) x 2	kHz
SCK Clock High Time	t_{HC}	$V_{SCK} \geq V_{IH}$, $t_{SCK} = 1/f_{SCK}$		0.35 x t_{SCK}			ns
SCK Clock Low Time	t_{LC}	$V_{SCK} \leq V_{IL}$, $t_{SCK} = 1/f_{SCK}$		0.35 x t_{SCK}			ns
SD, WS Setup Time	t_{SET}	(Figure 12)		2			ns
SD, WS Hold Time	t_{HOLD}	(Figure 12)		2			ns

MAX9264 DC ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS ($\overline{ENABLE}$, BWS, INT, CDS, ES, EQS, DCS, MS, $\overline{PWDN}$, SSEN, DRS)							
High-Level Input Voltage	V_{IH1}			0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0 to V_{IOVDD}		-10		+10	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA				-1.5	V
SINGLE-ENDED OUTPUTS (WS, SCK, SD, DOUT_, PCLKOUT)							
High-Level Output Voltage	V_{OH1}	I_{OUT} = -2mA	DCS = IOGND	V_{IOVDD} - 0.3			V
			V_{DCS} = V_{IOVDD}	V_{IOVDD} - 0.2			
Low-Level Output Voltage	V_{OL1}	I_{OUT} = 2mA	DCS = IOGND			0.3	V
			V_{DCS} = V_{IOVDD}			0.2	

MAX9264 DC ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
OUTPUT Short-Circuit Current	I_{OS}	WS, SCK, SD, DOUT_	V_O = 0V, DCS = IOGND	V_{IOVDD} = 3.0V to 3.6V	14	25	39	mA
OUTPUT Short-Circuit Current	I_{OS}	WS, SCK, SD, DOUT_	V_O = 0V, DCS = IOGND	V_{IOVDD} = 1.7V to 1.9V	3	7	13	mA
OUTPUT Short-Circuit Current	I_{OS}	WS, SCK, SD, DOUT_	V_O = 0V, V_{DCS} = V_{IOVDD}	V_{IOVDD} = 3.0V to 3.6V	20	35	63	mA
OUTPUT Short-Circuit Current	I_{OS}	WS, SCK, SD, DOUT_	V_O = 0V, V_{DCS} = V_{IOVDD}	V_{IOVDD} = 1.7V to 1.9V	5	10	21	mA
OUTPUT Short-Circuit Current	I_{OS}	PCLKOUT	V_O = 0V, DCS = IOGND	V_{IOVDD} = 3.0V to 3.6V	15	33	50	mA
OUTPUT Short-Circuit Current	I_{OS}	PCLKOUT	V_O = 0V, DCS = IOGND	V_{IOVDD} = 1.7V to 1.9V	4	10	17	mA
OUTPUT Short-Circuit Current	I_{OS}	PCLKOUT	V_O = 0V, V_{DCS} = V_{IOVDD}	V_{IOVDD} = 3.0V to 3.6V	30	54	97	mA
OUTPUT Short-Circuit Current	I_{OS}	PCLKOUT	V_O = 0V, V_{DCS} = V_{IOVDD}	V_{IOVDD} = 1.7V to 1.9V	9	16	32	mA
I²C/UART, I/O, AND OPEN-DRAIN OUTPUTS (GPIO_, RX/SDA, TX/SCL, $\overline{ERR}$, LOCK)								
High-Level Input Voltage	V_{IH2}				0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}						0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	V_{IN} = 0 to V_{IOVDD} (Note 2)	RX/SDA, TX/SCL		-100		+1	µA
			LOCK, $\overline{ERR}$, GPIO_		-80		+1	
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA	V_{IOVDD} = 1.7V to 1.9V				0.4	V
			V_{IOVDD} = 3.0V to 3.6V				0.3	
DIFFERENTIAL OUTPUT FOR REVERSE CONTROL CHANNEL (IN+, IN-)								
Differential High Output Peak Voltage, (V_{IN+}) - (V_{IN-})	V_{ROH}	No high-speed data transmission (Figure 13)			30		60	mV
Differential Low Output Peak Voltage, (V_{IN+}) - (V_{IN-})	V_{ROL}	No high-speed data transmission (Figure 13)			-60		-30	mV
DIFFERENTIAL INPUTS (IN+, IN-)								
Differential High Input Threshold (Peak) Voltage, (V_{IN+}) - (V_{IN-})	$V_{IDH(P)}$	Figure 14				40	90	mV
Differential Low Input Threshold (Peak) Voltage, (V_{IN+}) - (V_{IN-})	$V_{IDL(P)}$	Figure 14			-90	-40		mV
Input Common-Mode Voltage ((V_{IN+}) + (V_{IN-}))/2	V_{CMR}				1	1.3	1.6	V
Differential Input Resistance (Internal)	R_I				80	100	130	Ω

MAX9264 DC ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Worst-Case Supply Current (Figure 15, Note 3)	I_{WCS}	BWS = IOGND, $f_{PCLKOUT}$ = 16.6MHz	2% spread spectrum active		132	186	mA
			Spread spectrum disabled		125	175	
		BWS = IOGND, $f_{PCLKOUT}$ = 33.3MHz	2% spread spectrum active		145	204	
			Spread spectrum disabled		133	188	
		BWS = IOGND, $f_{PCLKOUT}$ = 66.6MHz	2% spread spectrum active		174	241	
			Spread spectrum disabled		157	220	
		BWS = IOGND, $f_{PCLKOUT}$ = 104MHz	2% spread spectrum active		210	275	
			Spread spectrum disabled		186	242	
Sleep Mode Supply Current	I_{CCS}				80	230	µA
Power-Down Current	I_{CCZ}	$\overline{PWDN}$ = IOGND			25	156	µA
ESD PROTECTION							
IN+, IN-	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF (Note 4)			±8		kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF (Note 5)	Contact discharge		±10		
			Air discharge		±12		
		ISO 10605, R_D = 2kΩ, C_S = 330pF (Note 5)	Contact discharge		±8		
			Air discharge		±20		
All Other Pins	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF (Note 4)			±4		kV

MAX9264 AC ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PARALLEL CLOCK OUTPUT (PCLKOUT)							
Clock Frequency	$f_{PCLKOUT}$	BWS = IOGND, V_{DRS} = V_{IOVDD}		8.33		16.66	MHz
		BWS = IOGND, DRS = IOGND		16.66		104	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{IOVDD}		6.25		12.5	
		V_{BWS} = V_{IOVDD}, DRS = IOGND		12.5		78	
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T (Figure 16, Note 6)		40	50	60	%
Clock Jitter	t_J	Period jitter, RMS, spread off, 3.125Gbps, PRBS pattern, UI = $1/f_{PCLKOUT}$ (Note 6)			0.05		UI
I²C/UART PORT TIMING							
I²C/UART Bit Rate				9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		150	ns
Input Setup Time	t_{SET}	I²C only (Figure 6, Note 6)		100			ns
Input Hold Time	t_{HOLD}	I²C only (Figure 6, Note 6)		0			ns
SWITCHING CHARACTERISTICS (NOTE 6)							
PCLKOUT Rise-and-Fall Time	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V	V_{DCS} = V_{IOVDD}, C_L = 10pf	0.4		2.2	ns
			DCS = IOGND, C_L = 5pF	0.5		2.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.25		1.7	
			DCS = IOGND, C_L = 5pF	0.3		2.0	
Parallel Data Rise-and-Fall Time (Figure 17)	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V	V_{DCS} = V_{IOVDD}, C_L = 10pf	0.5		3.1	ns
			DCS = IOGND, C_L = 5pF	0.6		3.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.3		2.2	
			DCS = IOGND, C_L = 5pF	0.4		2.4	
Deserializer Delay	t_{SD}	(Figure 18, Note 7)	Spread spectrum enabled			2880	Bits
			Spread spectrum disabled			750	
Reverse Control-Channel Output Rise Time	t_R	No forward channel data transmission (Figure 13)		180		400	ns
Reverse Control-Channel Output Fall Time	t_F	No forward channel data transmission (Figure 13)		180		400	ns

MAX9264 AC ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Lock Time	t_{LOCK}	Figure 19	Spread spectrum enabled			1.5	ms
			Spread spectrum disabled			1	
Power-Up Time	t_{PU}	Figure 20				2.5	ms
I²S OUTPUT TIMING (NOTE 6)							
WS Jitter	t_{AJ-WS}	t_{WS} = 1/f_{WS}, rising (falling) edge to falling (rising) edge	f_{WS} = 48kHz or 44.1kHz		0.4e - 3 x t_{WS}	0.5e - 3 x t_{WS}	ns
			f_{WS} = 96kHz		0.8e - 3 x t_{WS}	1e - 3 x t_{WS}	
			f_{WS} = 192kHz		1.6e - 3 x t_{WS}	2e - 3 x t_{WS}	
SCK Jitter	t_{AJ-SCK}	t_{SCK} = 1/f_{SCK}, rising edge to rising edge	n_{WS} = 16 bits, f_{WS} = 48kHz or 44.1kHz		13e - 3 x t_{SCK}	16e - 3 x t_{SCK}	ns
			n_{WS} = 24 bits, f_{WS} = 96kHz		39e - 3 x t_{SCK}	48e - 3 x t_{SCK}	
			n_{WS} = 32 bits, f_{WS} = 192kHz		0.1 x t_{SCK}	0.13 x t_{SCK}	
Audio Skew Relative to Video	t_{ASK}	Video and audio synchronized			3 x t_{WS}	4 x t_{WS}	µs
SCK, SD, WS Rise-and-Fall Time	t_R, t_F	20% to 80%, C_L = 10pF	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.3		3.1	ns
			DCS = IOGND, C_L = 5pF	0.4		3.8	
SD, WS Valid Time Before SCK	t_{DVB}	t_{SCK} = 1/f_{SCK} (Figure 21)		0.35 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK	t_{DVA}	t_{SCK} = 1/f_{SCK} (Figure 21)		0.35 x t_{SCK}	0.5 x t_{SCK}		ns

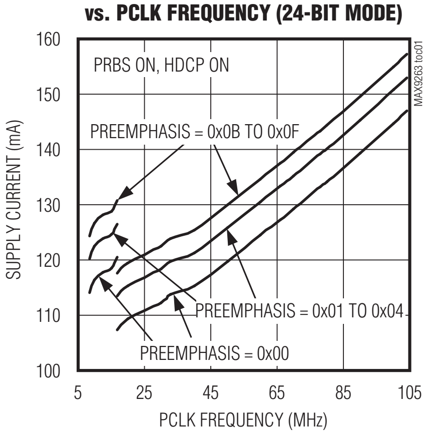
Note 2: Minimum I_{IN} due to voltage drop across the internal pullup resistor.
Note 3: HDCP enabled.
Note 4: Tested terminal to all grounds.
Note 5: Tested terminal to AGND.
Note 6: Guaranteed by design and not production tested.
Note 7: Measured in CML bit times. Bit time = 1/(30 x $f_{PCLKOUT}$) for BWS = GND. Bit time = 1/(40 x $f_{PCLKOUT}$) for V_{BWS} = V_{IOVDD}.

HDCP Gigabit Multimedia Serial Link Serializer/Deserializer

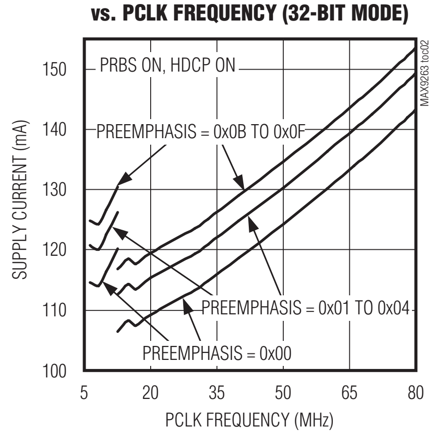
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V (MAX9263), V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V (MAX9264), T_A = +25°C, unless otherwise noted.)

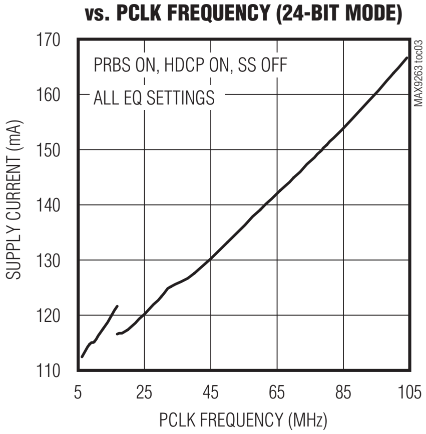
MAX9263 SUPPLY CURRENT vs. PCLK FREQUENCY (24-BIT MODE)



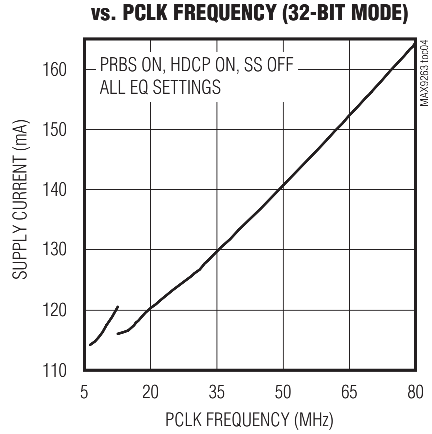
MAX9263 SUPPLY CURRENT vs. PCLK FREQUENCY (32-BIT MODE)



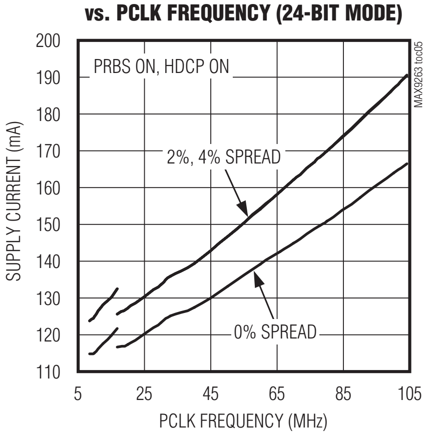
MAX9264 SUPPLY CURRENT vs. PCLK FREQUENCY (24-BIT MODE)



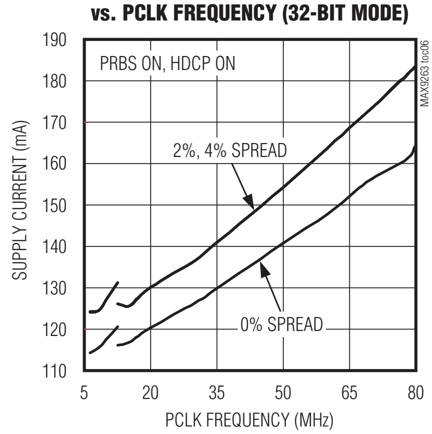
MAX9264 SUPPLY CURRENT vs. PCLK FREQUENCY (32-BIT MODE)



MAX9264 SUPPLY CURRENT vs. PCLK FREQUENCY (24-BIT MODE)



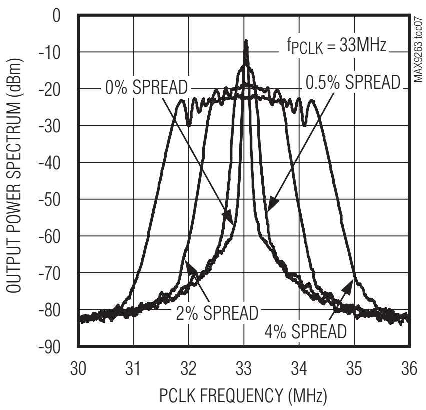
MAX9264 SUPPLY CURRENT vs. PCLK FREQUENCY (32-BIT MODE)



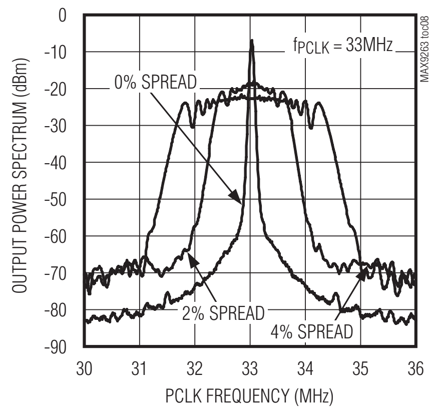
Typical Operating Characteristics (continued)

($V_{AVDD} = V_{DVDD} = V_{IOVDD}$ = 1.8V (MAX9263), $V_{AVDD} = V_{DVDD} = V_{IOVDD}$ = 3.3V (MAX9264), T_A = +25°C, unless otherwise noted.)

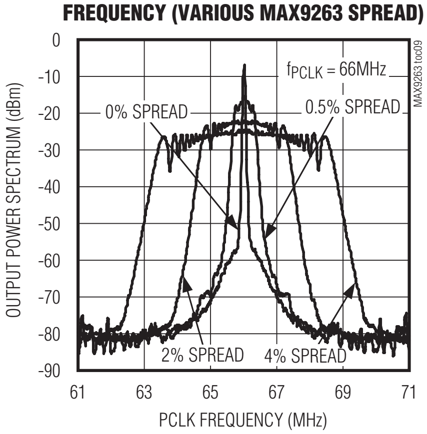
OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY (VARIOUS MAX9263 SPREAD)



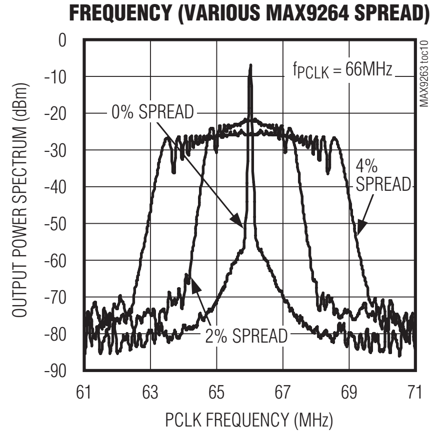
OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY (VARIOUS MAX9264 SPREAD)



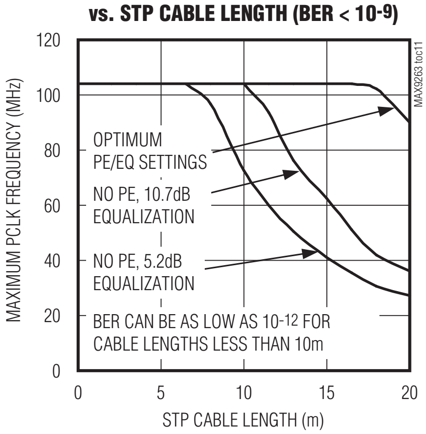
OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY (VARIOUS MAX9263 SPREAD)



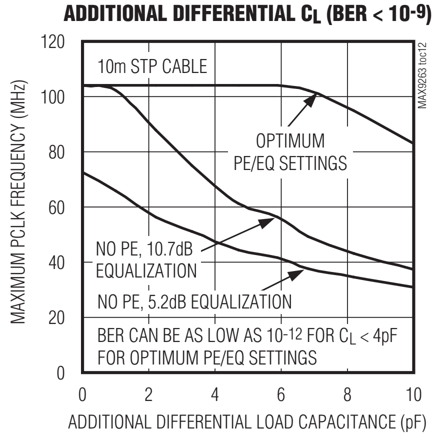
OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY (VARIOUS MAX9264 SPREAD)



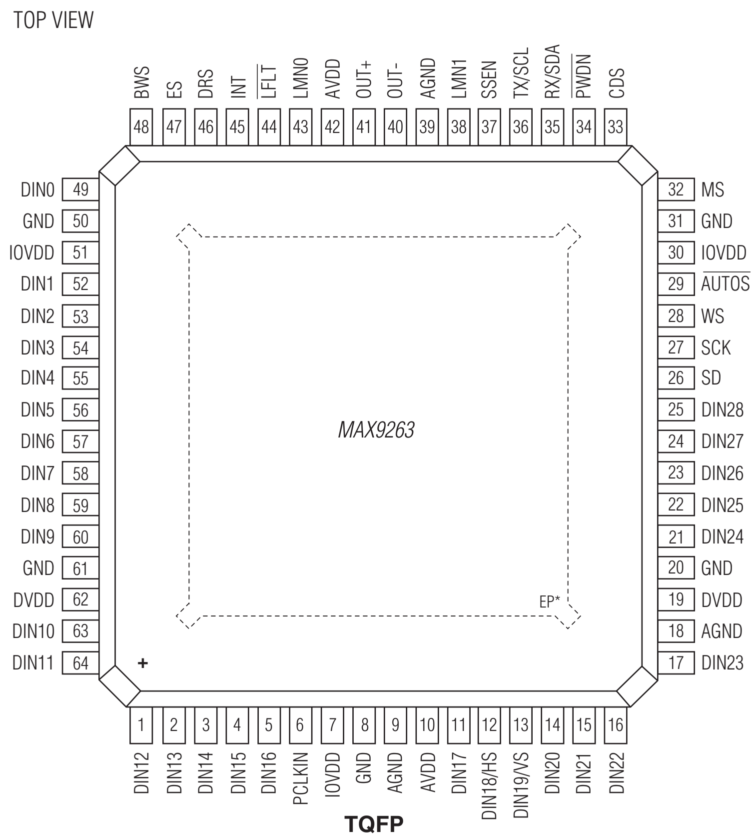
MAXIMUM PCLK FREQUENCY vs. STP CABLE LENGTH (BER < 10^{-9})



MAXIMUM PCLK FREQUENCY vs. ADDITIONAL DIFFERENTIAL C_L (BER < 10^{-9})



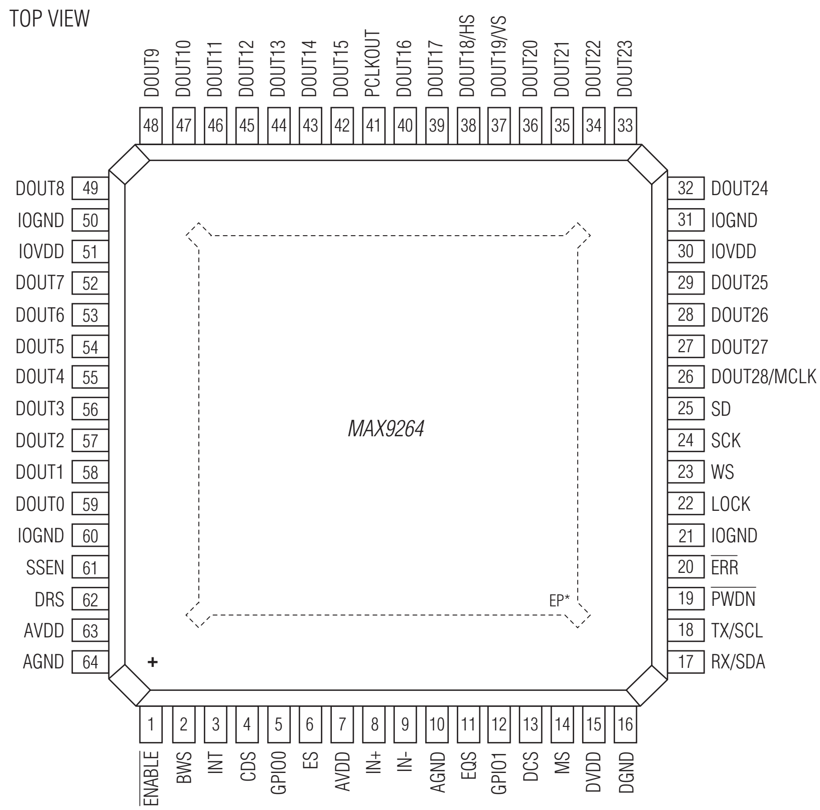
Pin Configurations



TQFP

*CONNECT EXPOSED PAD TO AGND

Pin Configurations (continued)



TQFP

*CONNECT EXPOSED PAD TO AGND

HDCP Gigabit Multimedia Serial Link Serializer/Deserializer

MAX9263 Pin Description

PIN	NAME	FUNCTION
1–5	DIN[12:16]	Data Input [12:16]. Parallel data inputs with internal pulldown to GND. Encrypted when HDCP is enabled (see Table 3).
6	PCLKIN	Parallel Clock Input. Latches parallel data inputs and provides the PLL reference clock.
7, 30, 51	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to IOVDD.
8, 20, 31, 50, 61	GND	Digital and I/O Ground
9, 18, 39	AGND	Analog Ground
10, 42	AVDD	1.8V Analog Power Supply. Bypass AVDD to AGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
11	DIN17	Data Input 17. Parallel data input with internal pulldown to GND. Encrypted when HDCP is enabled (see Table 3).
12	DIN18/HS	Data Input 18/HSYNC. Parallel data input with internal pulldown to GND. Use DIN18/HS for HSYNC when HDCP is enabled (Table 3).
13	DIN19/VS	Data Input 19/VSYNC. Parallel data input with internal pulldown to GND. Use DIN19/VS for VSYNC when HDCP is enabled (Table 3).
14	DIN20	Data Input 20. Parallel data input with internal pulldown to GND. DIN20 is not encrypted when HDCP is enabled (see Table 3).
15, 16, 17	DIN[21:23]	Data Input [21:23]. Parallel data inputs with internal pulldown to GND. DIN[21:23] are not used in 24-bit mode. Set BWS = high (32-bit mode) to use [DIN21:23]. Encrypted when HDCP is enabled (Table 3).
19, 62	DVDD	1.8V Digital Power Supply. Bypass DVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to DVDD.
21, 22, 23	DIN[24:26]	Data Input [24:26]. Parallel data inputs with internal pulldown to GND. DIN[24:26] are not used in 24-bit mode. Set BWS = high (32-bit mode) to use [DIN24:26]. Encrypted when HDCP is enabled (see Table 3).
24, 25	DIN[27:28]	Data Input [27:28]. Parallel data inputs with internal pulldown to GND. DIN[27:28] are not used in 24-bit mode. Set BWS = high (32-bit mode) to use [DIN27:28]. DIN[27:28] are not encrypted when HDCP is enabled (see Table 3).
26	SD	I^2S Serial-Data Input with Internal Pulldown to GND. Disable I^2S to use SD as an additional control/data input latched on the selected edge of PCLKIN. Encrypted when HDCP is enabled.
27	SCK	I^2S Serial-Clock Input with Internal Pulldown to GND
28	WS	I^2S Word-Select Input with Internal Pulldown to GND
29	$\overline{\text{AUTOS}}$	Active-Low Autostart Setting. $\overline{\text{AUTOS}}$ requires an external pulldown or pullup resistor. Set $\overline{\text{AUTOS}}$ = high to power up the device with no link active. Set $\overline{\text{AUTOS}}$ = low to have the serializer power up the serial link with autorange detection (see Tables 13 and 14).
32	MS	Mode Select. Control link mode-selection input requires an external pulldown or pullup resistor. Set MS = low to select base mode. Set MS = high to select the bypass mode.
33	CDS	Control Direction Selection. Control link direct selection input requires external pulldown or pullup resistor. Set CDS = low for UART connection of a µC as a control master. Set CDS = high for peripheral connection as a control-channel I^2C or UART slave.

MAX9263 Pin Description (continued)

PIN	NAME	FUNCTION
34	$\overline{\text{PWDN}}$	Active-Low, Power-Down Input. $\overline{\text{PWDN}}$ requires external pulldown or pullup resistor.
35	RX/SDA	Receive/Serial Data. UART receive or I²C serial-data input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the serializer's UART. In I²C mode, RX/SDA is the SDA input/output of the serializer's I²C master. RX/SDA has an open-drain driver and requires a pullup resistor.
36	TX/SCL	Transmit/Serial Clock. UART transmit or I²C serial-clock output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the serializer's UART. In I²C mode, TX/SCL is the SCL output of the serializer's I²C master. TX/SCL is an open-drain driver and requires a pullup resistor.
37	SSEN	Spread-Spectrum Enable. Serial link spread-spectrum enable input requires external pulldown or pullup resistor. The state of SSEN latches upon power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). Set SSEN = high for ±0.5% spread spectrum on the serial link. Set SSEN = low to use the serial link without spread spectrum.
38	LMN1	Line-Fault Monitor Input 1. See Figure 3 for details.
40, 41	OUT-, OUT+	Differential CML Output ±. Differential outputs of the serial link.
43	LMN0	Line-Fault Monitor Input 0. See Figure 3 for details.
44	$\overline{\text{LFLT}}$	Line Fault, Active-Low Open-Drain Line-Fault Output. $\overline{\text{LFLT}}$ has a 60kΩ internal pullup resistor. $\overline{\text{LFLT}}$ = low indicates a line fault. $\overline{\text{LFLT}}$ is high impedance when $\overline{\text{PWDN}}$ = low.
45	INT	Interrupt Output. Indicates remote-side interrupt requests. INT = low upon power-up and when PWDN = low. A transition on the INT input of the deserializer toggles the serializer's INT output.
46	DRS	Data-Rate Select. Data-rate range-selection input requires external pulldown or pullup resistor. The state of DRS latches upon power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). Set DRS = high for PCLKIN frequencies of 8.33MHz to 16.66MHz (24-bit mode) or 6.25MHz to 12.5MHz (32-bit mode). Set DRS = low for PCLKIN frequencies of 16.66MHz to 104MHz (24-bit mode) or 12.5MHz to 78MHz (32-bit mode).
47	ES	Edge Select. PCLKIN trigger edge selection requires external pulldown or pullup resistor. Set ES = low to trigger on the rising edge of PCLKIN. Set ES = high to trigger on the falling edge of PCLKIN.
48	BWS	Bus-Width Select. BWS requires external pulldown or pullup resistor. Set BWS = low for 24-bit mode. Set BWS = high for 32-bit mode.
49	DIN0	Data Input 0. Parallel data input with internal pulldown to GND. Encrypted when HDCP is enabled (Table 3).
52–60	DIN[1:9]	Data Input [1:9]. Parallel data inputs with internal pulldown to GND. Encrypted when HDCP is enabled (Table 3).
63, 64	DIN[10:11]	Data Input [10:11]. Parallel data inputs with internal pulldown to GND. Encrypted when HDCP is enabled (Table 3).
—	EP	Exposed Pad. EP is internally connected to AGND. **MUST** externally connect EP to the AGND plane for proper thermal and electrical performance.

HDCP Gigabit Multimedia Serial Link Serializer/Deserializer

MAX9264 Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{ENABLE}}$	Active-Low Parallel Output-Enable Input. Requires an external pulldown or pullup resistor. Set $\overline{\text{ENABLE}}$ = low to enable PCLKOUT, SD, SCK, WS, and DOUT_. Set $\overline{\text{ENABLE}}$ = high to put PCLKOUT, SD, SCK, WS, and DOUT_ into high impedance.
2	BWS	Bus-Width Select. BWS requires an external pulldown or pullup resistor. Set BWS = low for 24-bit mode. Set BWS = high for 32-bit mode.
3	INT	Interrupt Input. INT requires an external pullup or pulldown resistor. A transition on the deserializer's INT input toggles the serializer's INT output.
4	CDS	Control Direction Selection. Control link direction selection input requires external pulldown or pullup resistor. Set CDS = high for UART connection of a µC as control-channel master. Set CDS = low for peripheral connection as a control-channel I²C or UART slave.
5	GPIO0	GPIO0. Open-drain general-purpose input/output with an internal 60kΩ pullup resistor to IOVDD. GPIO0 is high impedance during power-up and when $\overline{\text{PWDN}}$ = low.
6	ES	Edge Select. PCLKOUT edge-selection input requires an external pulldown or pullup resistor. Set ES = low for a rising-edge trigger. Set ES = high for a falling-edge trigger.
7, 63	AVDD	3.3V Analog Power Supply. Bypass AVDD to AGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
8, 9	IN+, IN-	Differential CML Input ±. Differential inputs of the serial link.
10, 64	AGND	Analog Ground
11	EQS	Equalizer Select Input Requires an External Pulldown or Pullup Resistor. The state of EQS latches upon power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). Set EQS = low for 10.7dB equalizer boost (EQTUNE = 1001). Set EQS = high for 5.2dB equalizer boost (EQTUNE = 0100).
12	GPIO1	GPIO1. Open-drain general-purpose input/output with an internal 60kΩ pullup resistor to IOVDD. GPIO1 is high impedance during power-up and when $\overline{\text{PWDN}}$ = low.
13	DCS	Drive Current Select. Driver current-selection input requires an external pulldown or pullup resistor to IOVDD. Set DCS = high for stronger parallel data and clock output drivers. Set DCS = low for normal parallel data and clock drivers. See the *MAX9264 DC Electrical Characteristics* table.
14	MS	Mode Select. Control-channel mode selection input requires an external pulldown or pullup resistor. MS sets the control-link mode when CDS = high. See the *Control-Channel and Register Programming* section. MS sets autostart mode when CDS = low. See Table 13.
15	DVDD	3.3V Digital Power Supply. Bypass DVDD to DGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to DVDD.
16	DGND	Digital Ground
17	RX/SDA	Receive/Serial Data. UART receive or I²C serial-data input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the deserializer's UART. In I²C mode, RX/SDA is the SDA input/output of the deserializer's I²C master. RX/SDA has an open-drain driver and requires a pullup resistor.
18	TX/SCL	Transmit/Serial Clock. UART transmit or I²C serial-clock output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the deserializer's UART. In I²C mode, TX/SCL is the SCL output of the deserializer's I²C master. TX/SCL is an open-drain driver and requires a pullup resistor.

MAX9264 Pin Description (continued)

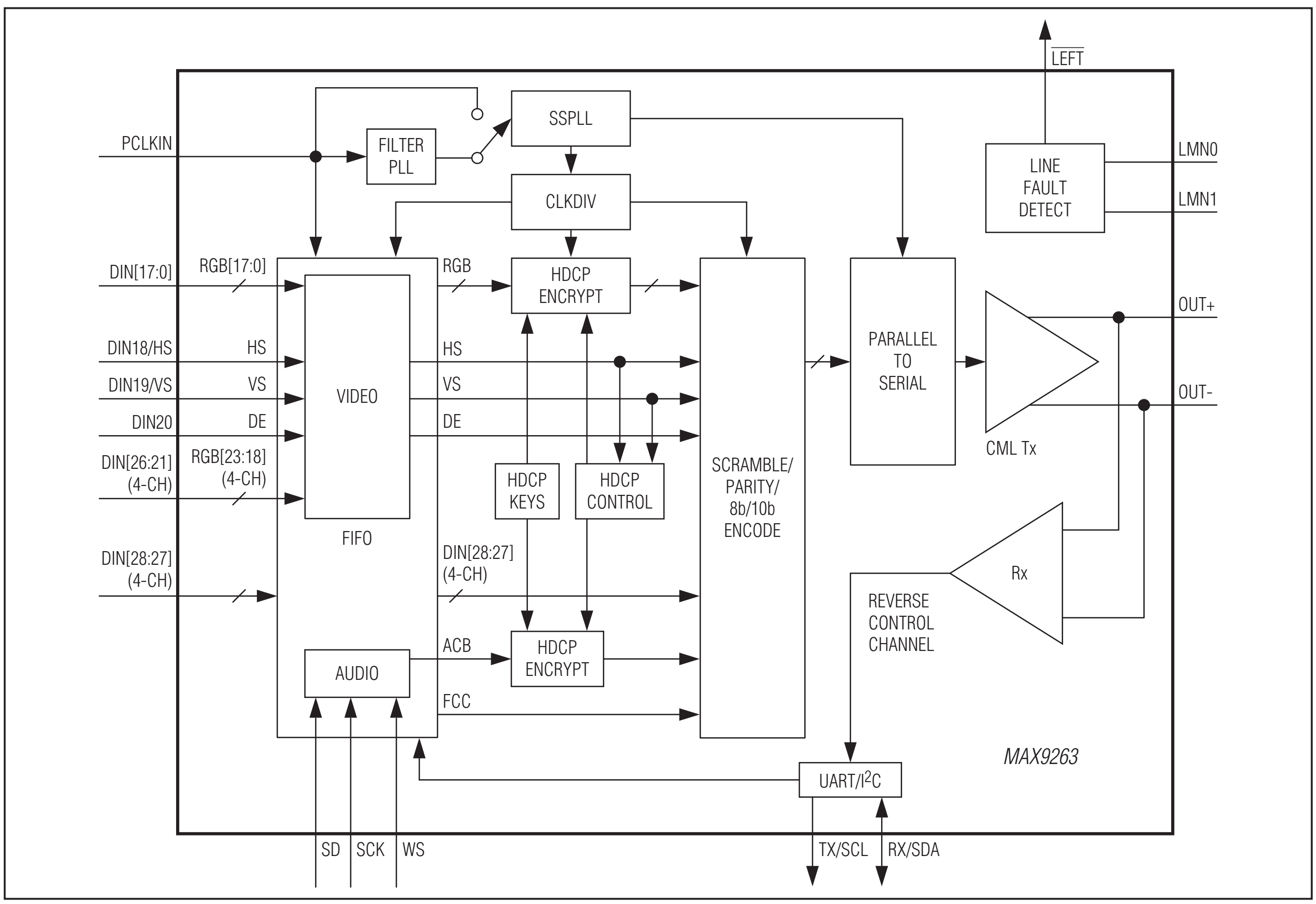
PIN	NAME	FUNCTION
19	$\overline{PWDN}$	Active-Low, Power-Down Input. $\overline{PWDN}$ requires an external pulldown or pullup resistor.
20	$\overline{ERR}$	Active-Low Open-Drain Video Data Error Output with Internal 60kΩ Pullup to IOVDD. $\overline{ERR}$ goes low when the number of decoding errors during normal operation exceed a programmed error threshold or when at least one PRBS error is detected during PRBS test. $\overline{ERR}$ is high impedance when $\overline{PWDN}$ = low. $\overline{ERR}$ is an open-drain driver and requires a pullup resistor.
21, 31, 50, 60	IOGND	Input/Output Ground
22	LOCK	Open-Drain Lock Output with Internal 60kΩ Pullup to IOVDD. LOCK = high indicates PLLs are locked with correct serial-word-boundary alignment. LOCK = low indicates PLLs are not locked or incorrect serial-word-boundary alignment. LOCK remains low when the configuration link is active. LOCK is high impedance when $\overline{PWDN}$ = low. LOCK is an open-drain driver and requires a pullup resistor.
23	WS	I^2S Word-Select Output
24	SCK	I^2S Serial-Clock Output
25	SD	I^2S Serial-Data Output. Disable I^2S to use SD as an additional control output latched on the selected edge of PCLKOUT. Encrypted when HDCP is enabled.
26	DOUT28/ MCLK	Data Output 28/MCLK. Parallel data or master clock output. Output data can be strobed on the selected edge of PCLKOUT. DOUT28 is not used in 24-bit mode and remains low. Set BWS = high (32-bit mode) to use DOUT28. DOUT28/MCLK is not encrypted when HDCP is enabled (Table 3). DOUT28/MCLK can be used to output MCLK. See the *Additional MCLK Output for Audio Applications* section.
27	DOUT27	Data Output 27. Parallel data output. Output data can be strobed on the selected edge of PCLKOUT. DOUT27 is not used in 24-bit mode and remains low. Set BWS = high (32-bit mode) to use DOUT27. DOUT27 is not encrypted when HDCP is enabled. See Table 3.
28, 29	DOUT[26:25]	Data Output [26:25]. Parallel data outputs. Output data can be strobed on the selected edge of PCLKOUT. DOUT[26:25] are not used in 24-bit mode and remain output low. Set BWS = high (32-bit mode) to use DOUT[26:25]. Encrypted when HDCP is enabled. See Table 3.
30, 51	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to IOGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to IOVDD.
32–35	DOUT[24:21]	Data Output [24:21]. Parallel data outputs. Output data can be strobed on the selected edge of PCLKOUT. DOUT[24:21] are not used in 24-bit mode and remain low. Set BWS = high (32-bit mode) to use DOUT[24:21]. Encrypted when HDCP is enabled. See Table 3.
36	DOUT20	Data Output 20. Parallel data output. Output data can be strobed on the selected edge of PCLKOUT. DOUT20 is not encrypted when HDCP is enabled. See Table 3.
37	DOUT19/VS	Data Output 19/VSYNC. Parallel data output. Output data can be strobed on the selected edge of PCLKOUT. Use DOUT19/VS for VSYNC when HDCP is enabled. See Table 3.
38	DOUT18/HS	Data Output 18/HSYNC. Parallel data output. Output data can be strobed on the selected edge of PCLKOUT. Use DOUT18/HS for HSYNC when HDCP is enabled. See Table 3.
39, 40	DOUT[17:16]	Data Output [17:16]. Parallel data outputs. Output data can be strobed on the selected edge of PCLKOUT. Encrypted when HDCP is enabled. See Table 3.
41	PCLKOUT	Parallel Clock Output. Used for DOUT[28:0].
42–49	DOUT[15:8]	Data Output [15:8]. Parallel data outputs. Output data can be strobed on the selected edge of PCLKOUT. Encrypted when HDCP is enabled. See Table 3.

HDCP Gigabit Multimedia Serial Link Serializer/Deserializer

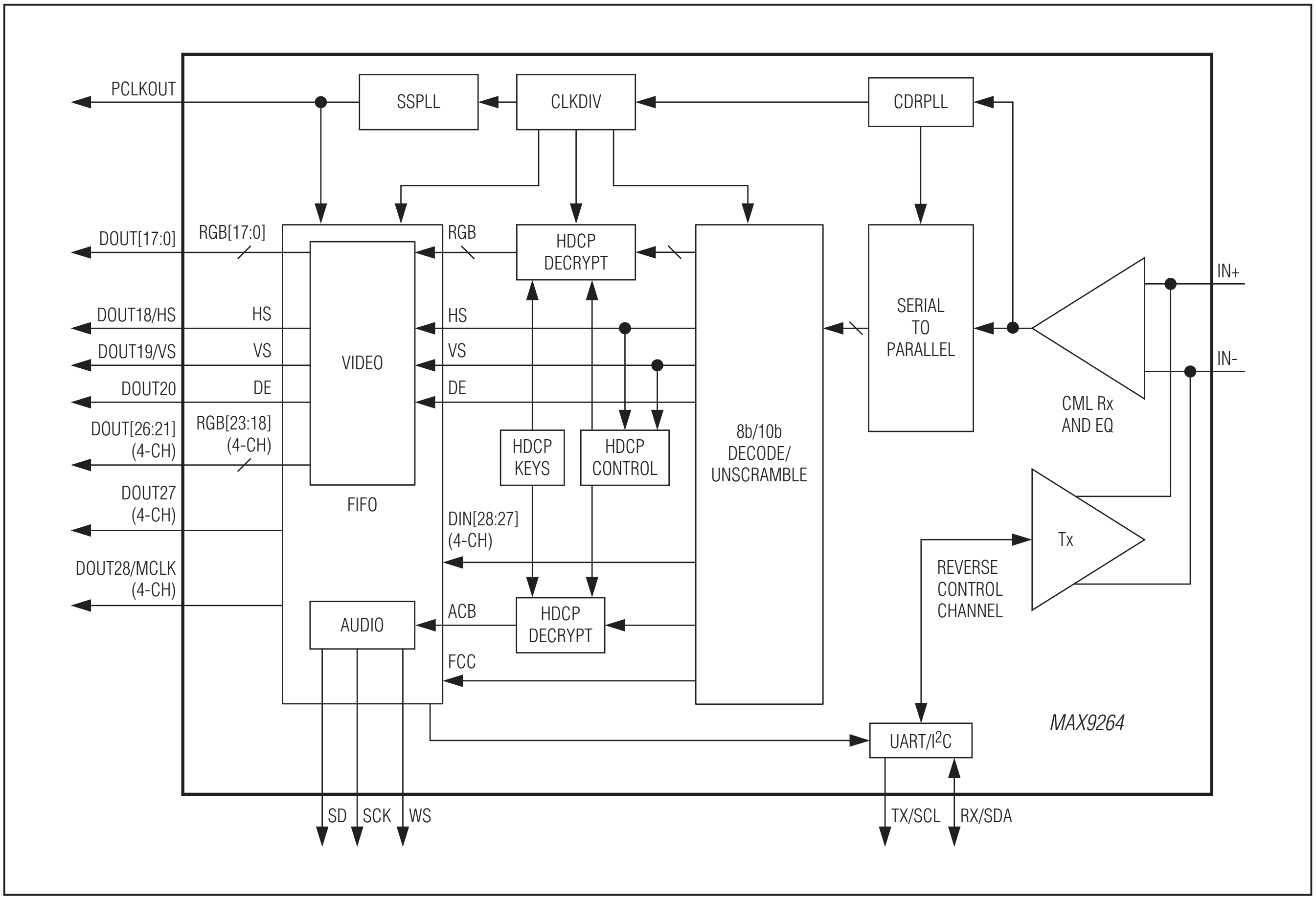
MAX9264 Pin Description (continued)

PIN	NAME	FUNCTION
52–59	DOUT[7:0]	Data Output [7:0]. Parallel data outputs. Output data can be strobed on the selected edge of PCLKOUT. Encrypted when HDCP is enabled. See Table 3.
61	SSEN	Spread-Spectrum Enable Input. Serial link spread-spectrum enable input requires an external pulldown or pullup resistor. The state of SSEN latches upon power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). Set SSEN = high for ±2% spread spectrum on parallel outputs. Set SSEN = low to use the parallel outputs without spread spectrum.
62	DRS	Data-Rate Select. Data-rate range-selection input requires an external pulldown or pullup resistor. The state of DRS latches upon power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). Set DRS = high for PCLKOUT frequencies of 8.33MHz to 16.66MHz (24-bit mode) or 6.25MHz to 12.5MHz (32-bit mode). Set DRS = low for PCLKOUT frequencies of 16.66MHz to 104MHz (24-bit mode) or 12.5MHz to 78MHz (32-bit mode).
—	EP	Exposed Pad. EP is internally connected to AGND. **MUST** externally connect EP to the AGND plane for proper thermal and electrical performance.

Functional Diagrams



Functional Diagrams (continued)



HDCP Gigabit Multimedia Serial Link Serializer/Deserializer

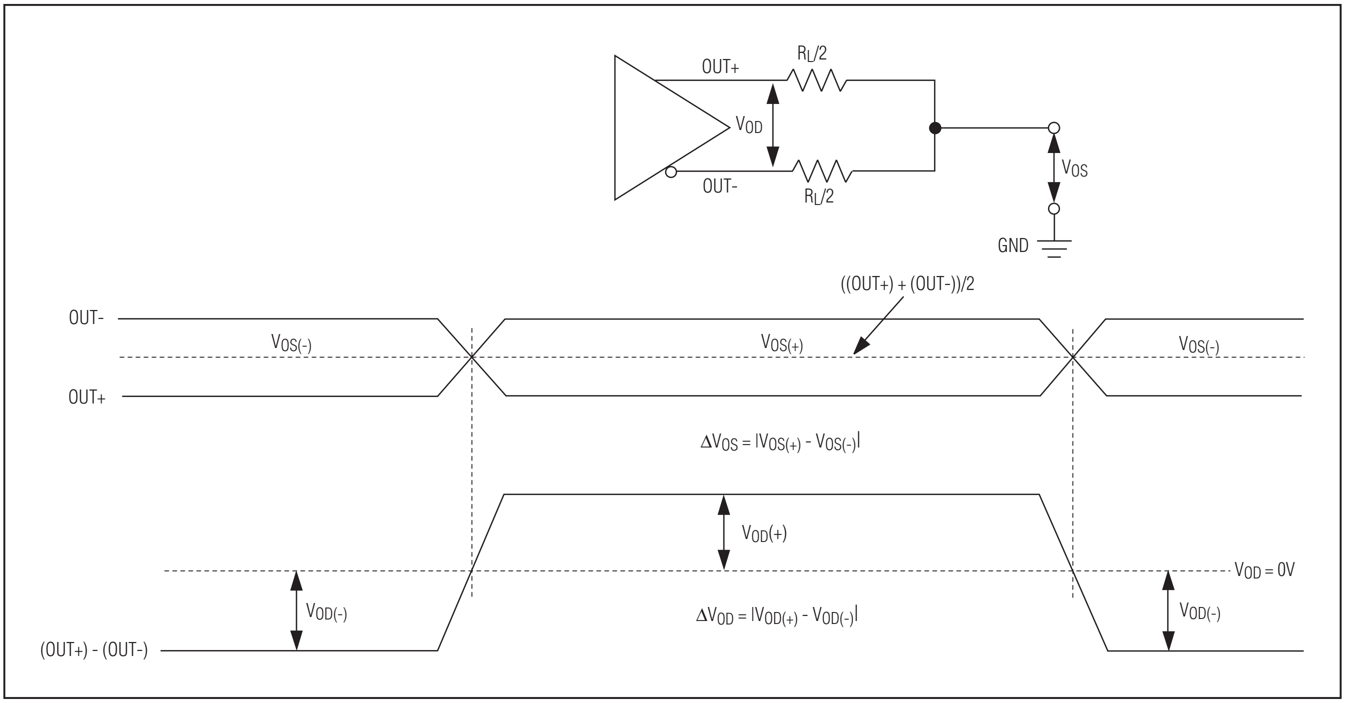


Figure 1. Serializer Serial-Output Parameters

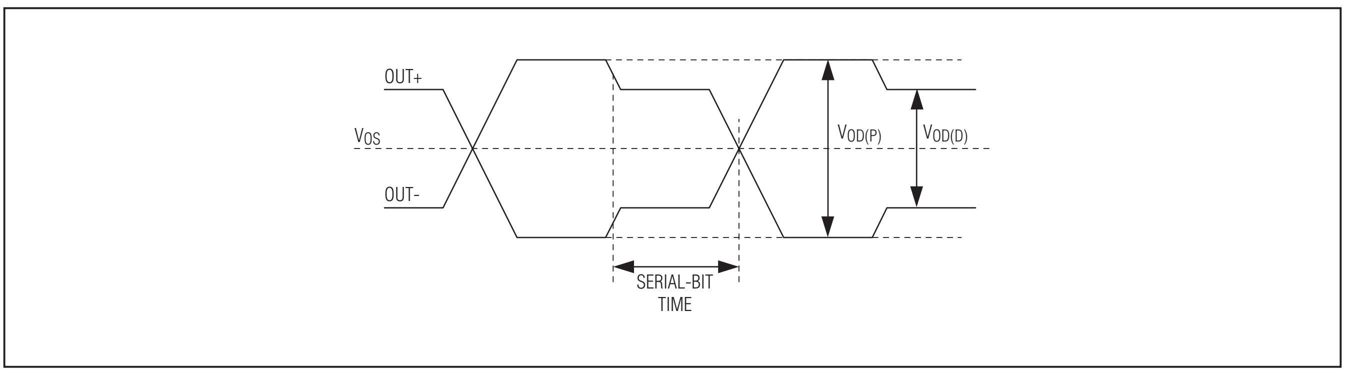


Figure 2. Serializer Output Waveforms at OUT+, OUT-

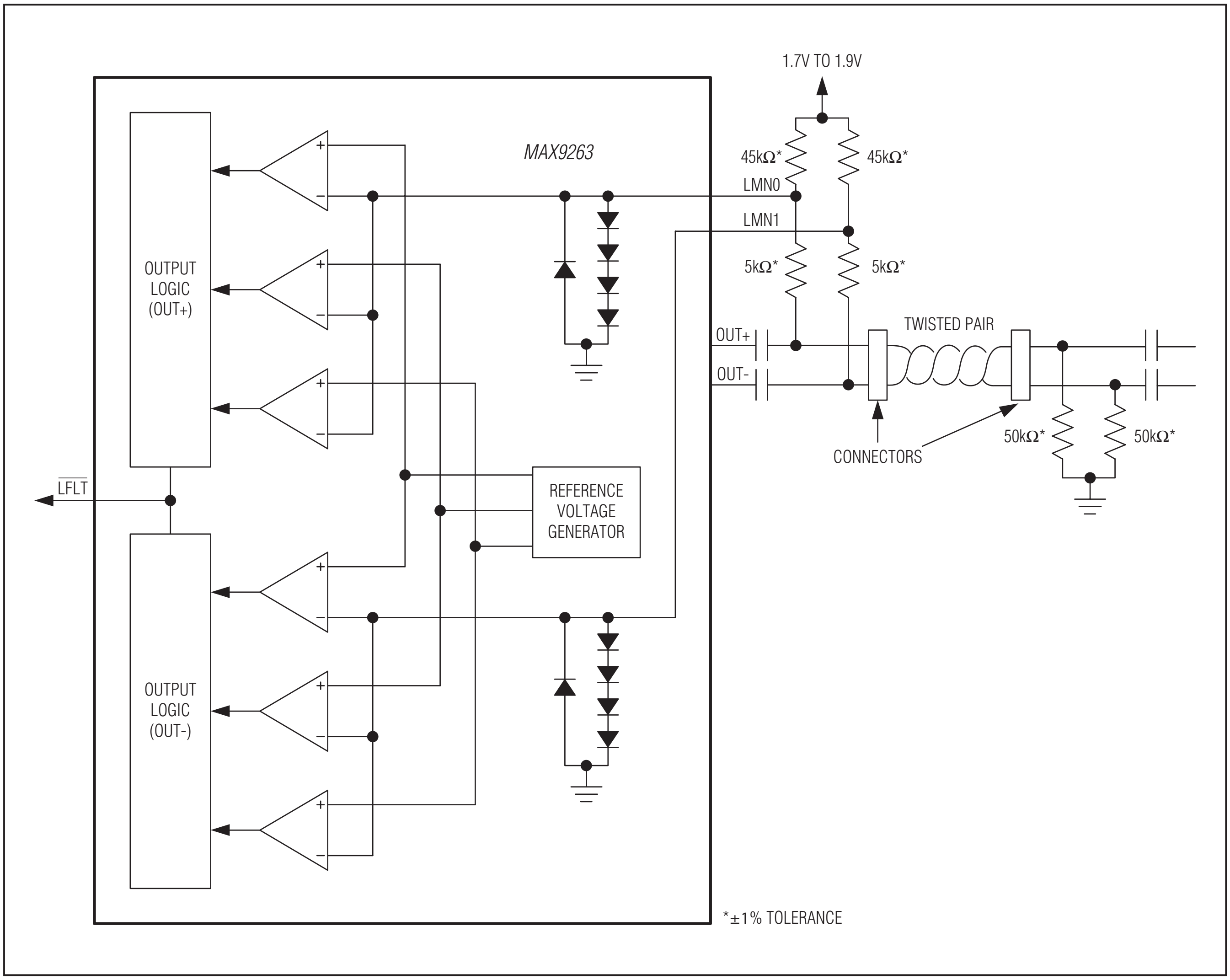


Figure 3. Line-Fault Detector Circuit

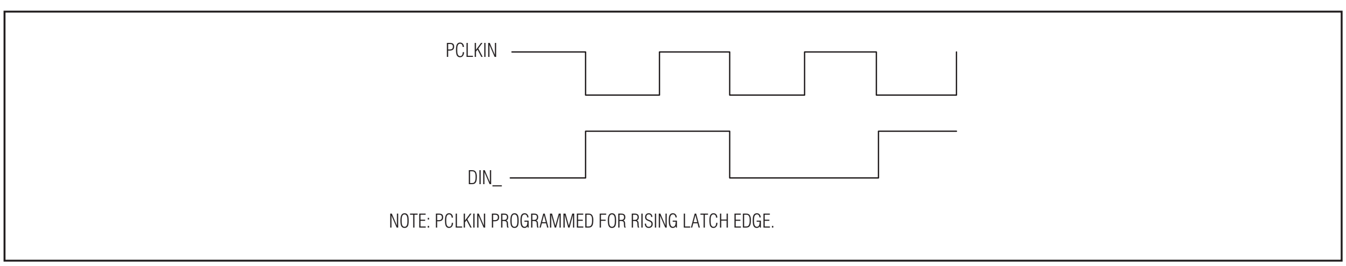


Figure 4. Serializer Worst-Case Pattern Input

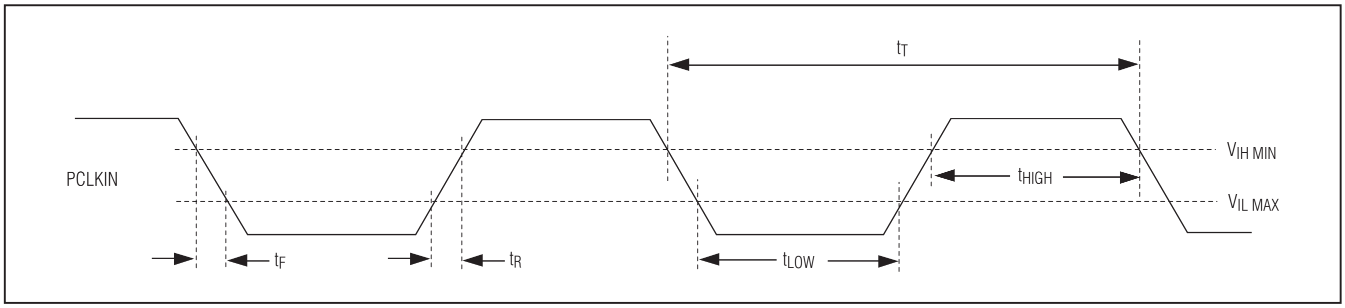


Figure 5. Serializer Parallel Input Clock Requirements

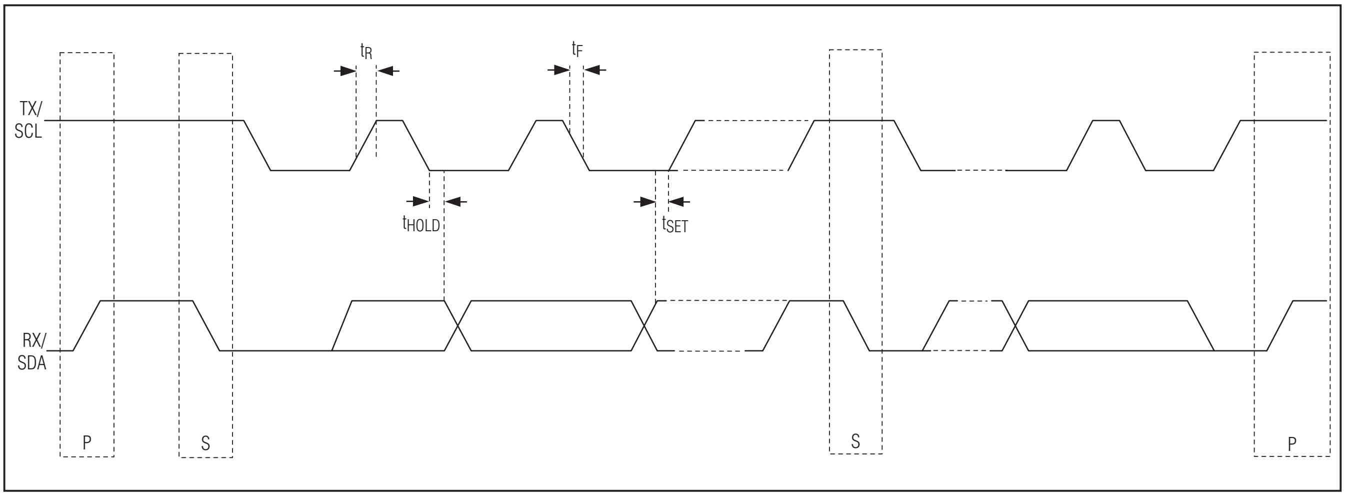


Figure 6. I²C Timing Parameters

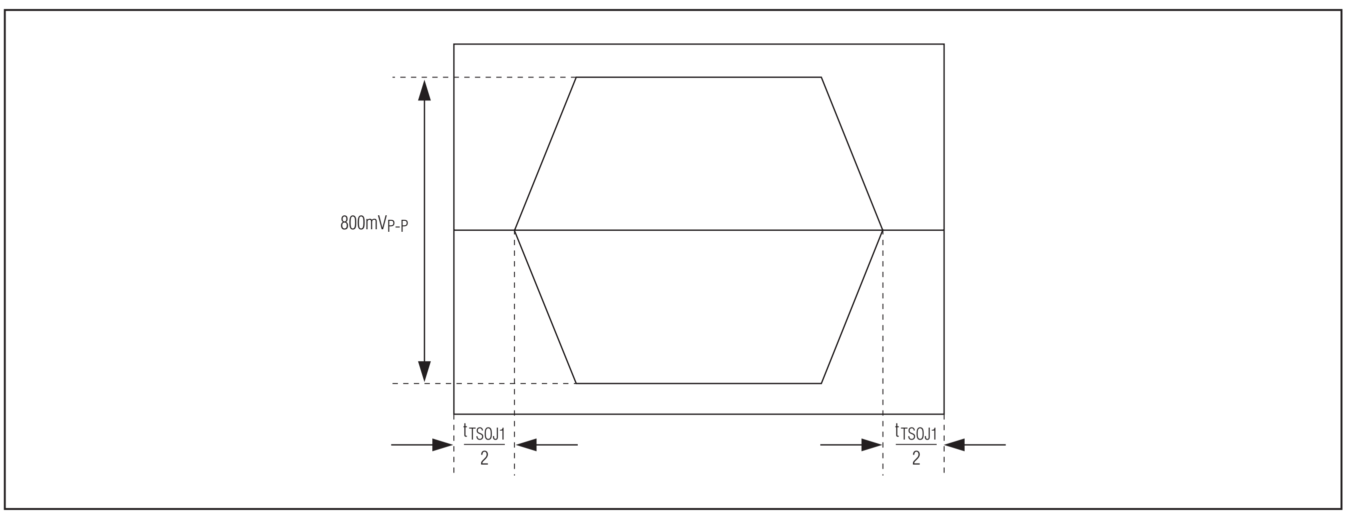


Figure 7. Serializer Differential Output Template

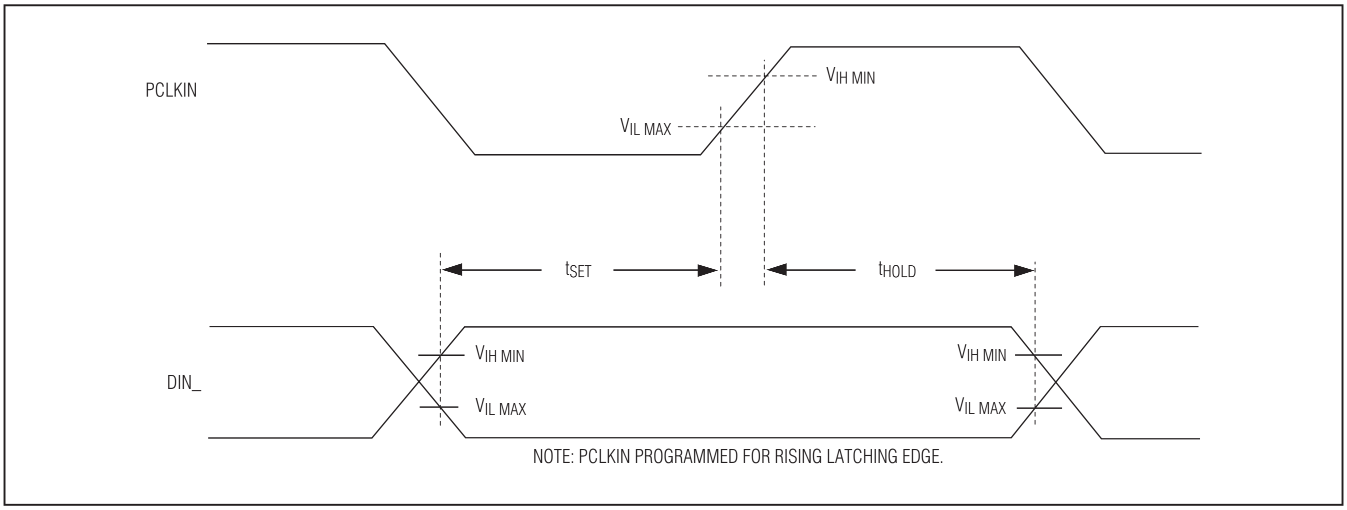


Figure 8. Serializer Input Setup and Hold Times

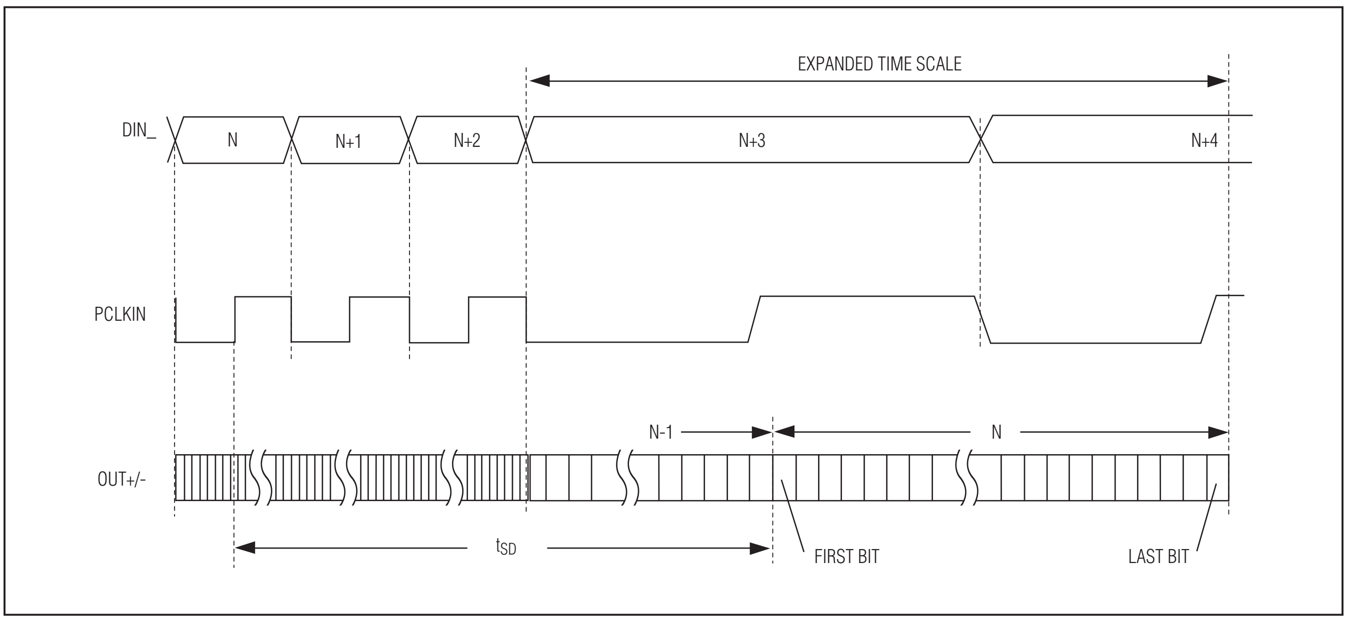


Figure 9. Serializer Delay

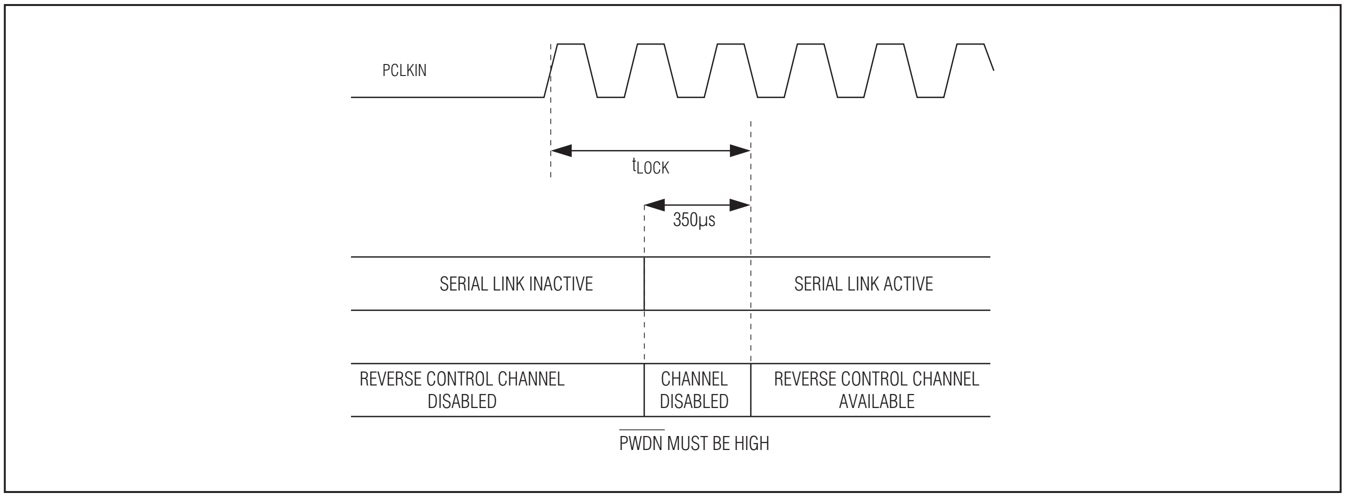


Figure 10. Serializer Link Startup Time

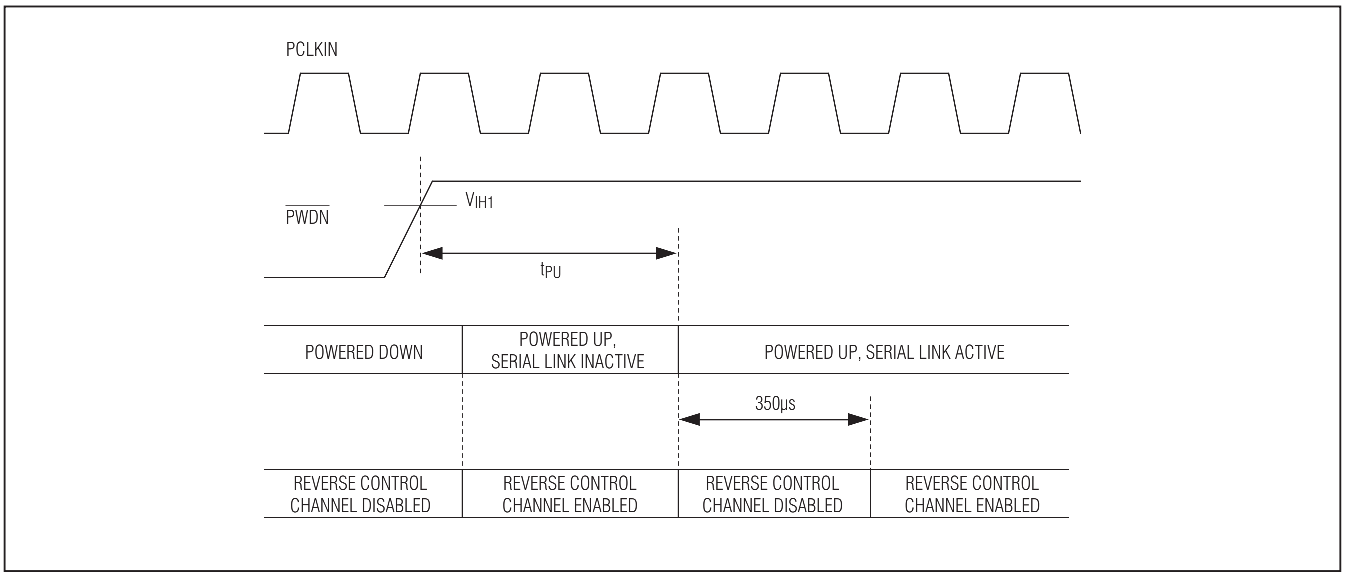


Figure 11. Serializer Power-Up Delay

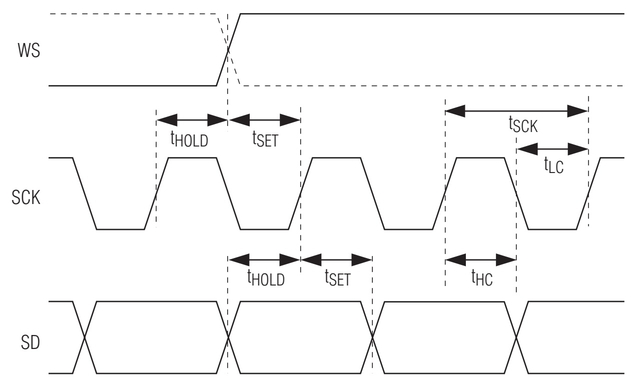


Figure 12. Input I2S Timing Parameters

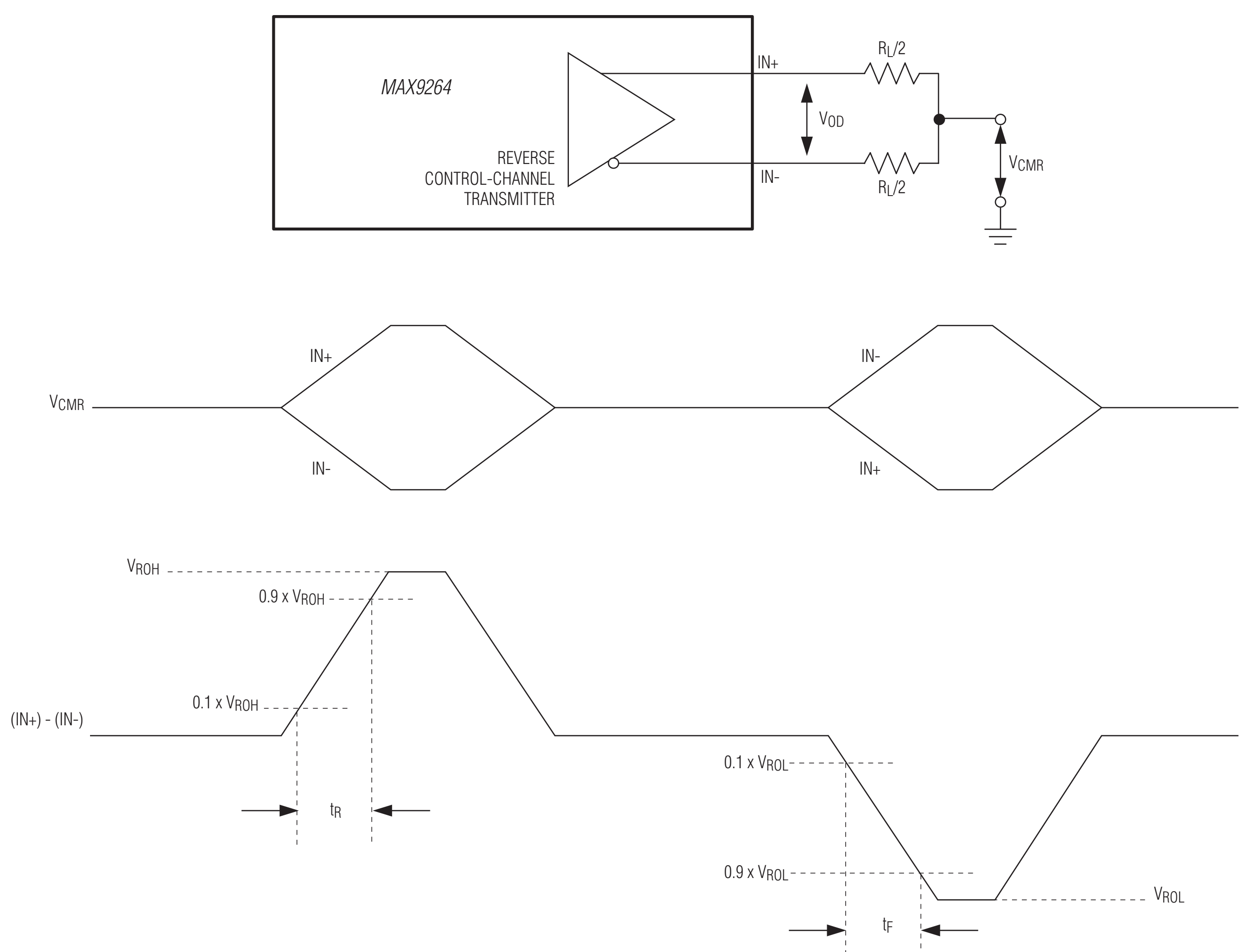


Figure 13. Reverse Control-Channel Output Parameters

HDCP Gigabit Multimedia Serial Link Serializer/Deserializer

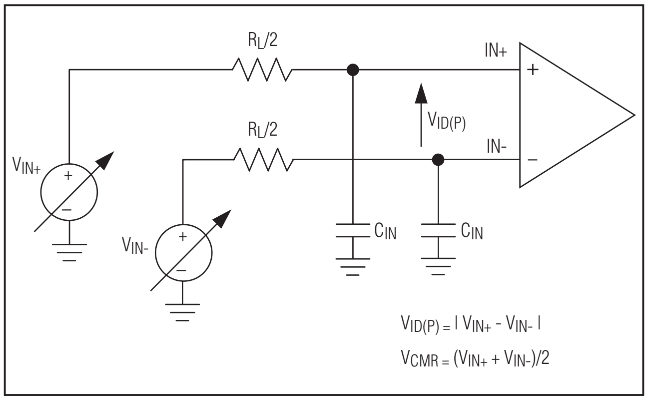


Figure 14. Test Circuit for Differential Input Measurement

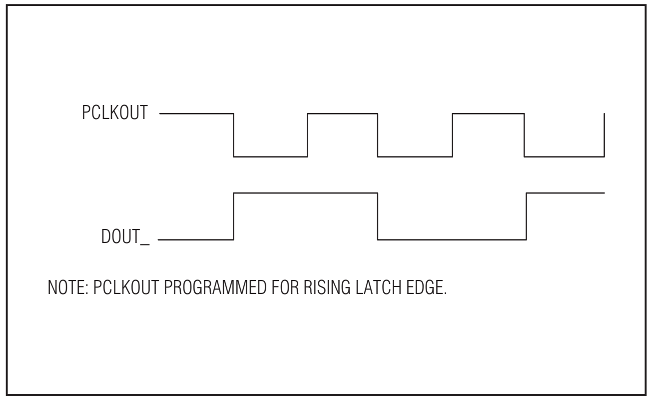


Figure 15. Deserializer Worst-Case Pattern Output

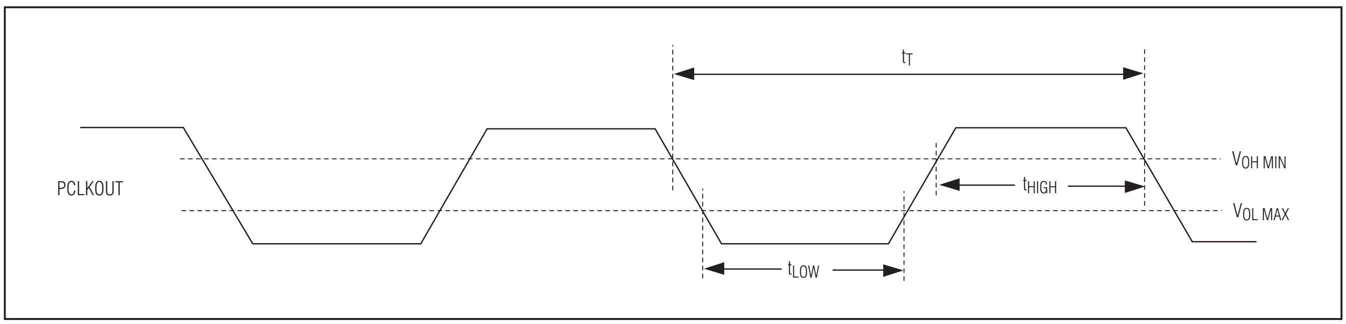


Figure 16. Deserializer Clock Output High and Low Times

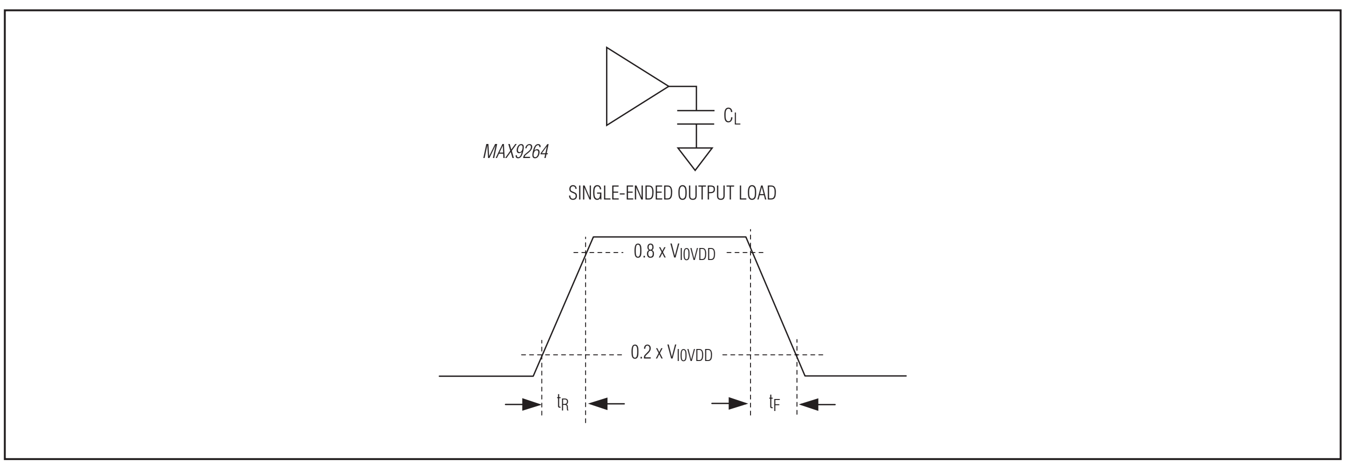


Figure 17. Deserializer Output Rise and Fall Times

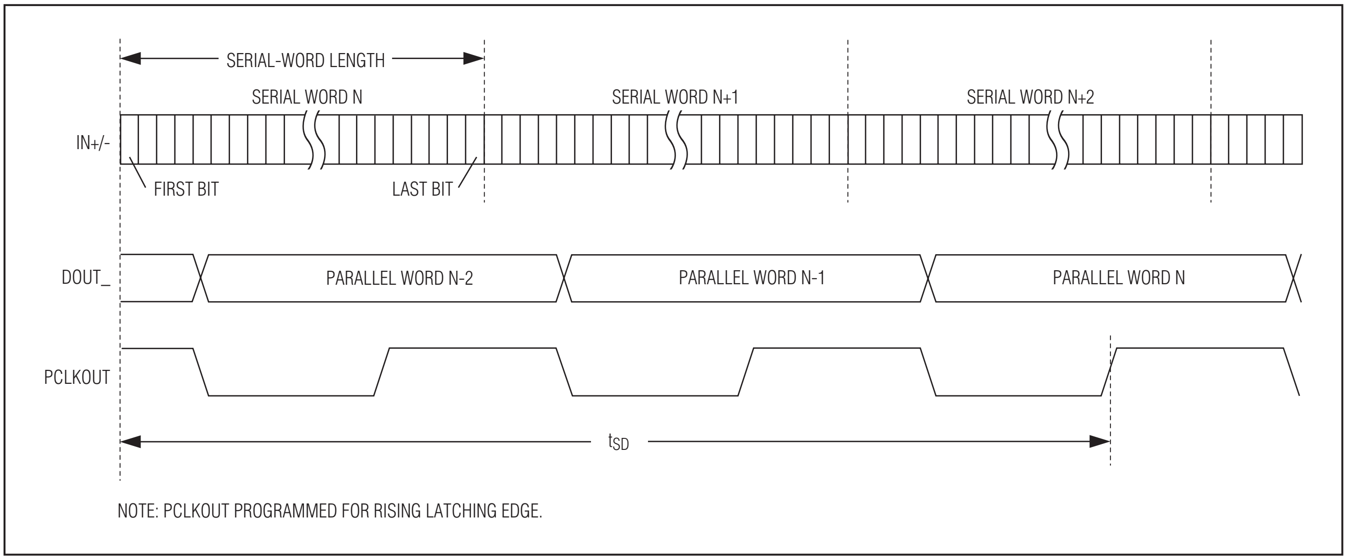


Figure 18. Deserializer Delay

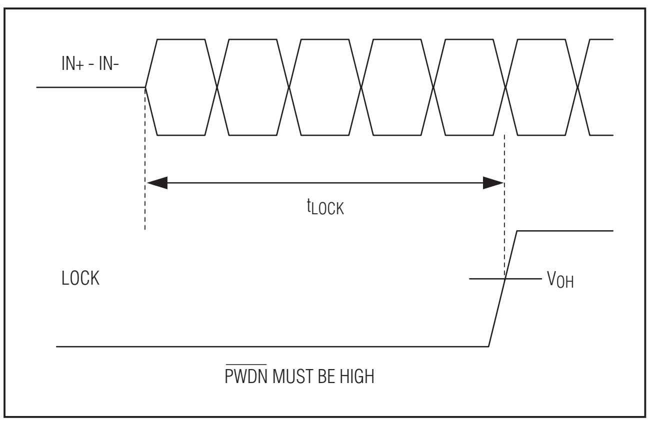


Figure 19. Deserializer Lock Time

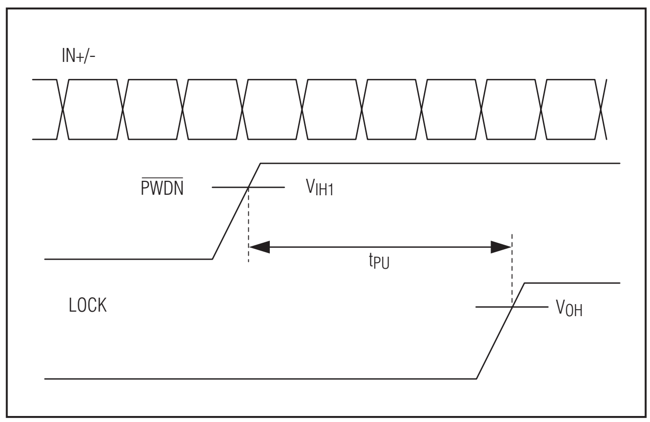


Figure 20. Deserializer Power-Up Delay

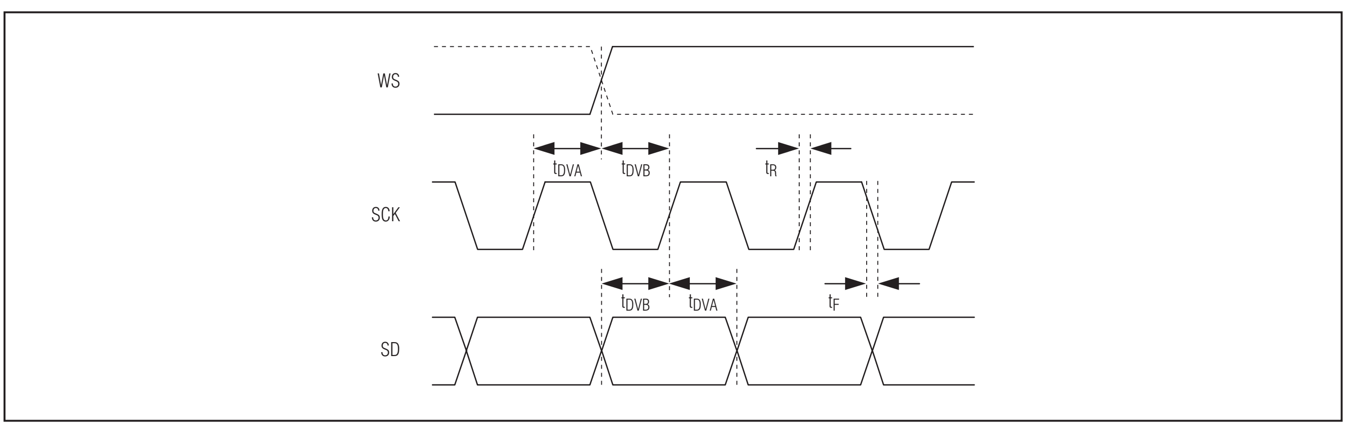


Figure 21. Deserializer Output I^2S Timing Parameters

Detailed Description

The MAX9263/MAX9264 serializer/deserializer chipset utilizes Maxim's GMSL technology and HDCP. When HDCP is enabled, the serializer/deserializer encrypt video and audio data on the serial link. The serializer/deserializer are backward compatible with the MAX9259/MAX9260 serializer/deserializer.

The serializer/deserializer have a maximum serial payload data rate of 2.5Gbps for 15m or more of STP cable. The serializer/deserializer pair operates up to a maximum pixel clock of 104MHz for 24-bit mode, or 78MHz for 32-bit mode, respectively. This serial link supports a wide range of display panels, from QVGA (320 x 240) to WXGA (1280 x 800) and higher with 24-bit color.

The 24-bit mode handles 21 bits of high-speed data, UART control signals, and three audio signals. The 32-bit mode handles 29 bits of high-speed data, UART control signals, and three audio signals. The three audio signals are a standard I²S interface, supporting sample rates from 8kHz to 192kHz and audio word lengths of 4 bits to 32 bits. The embedded control channel forms a full-duplex, differential 9.6kbps to 1Mbps UART link between the serializer and deserializer for HDCP-related control operations. In addition, the control channel enables electronic control unit (ECU), or microcontroller (µC) control of peripherals in the remote side, such as backlight control, grayscale gamma correction, camera module, and touch screen. An ECU/µC, can be located on the serializer side of the link (typical for video display), on the deserializer side of the link (typical for image sensing), or on both sides. Base-mode communication with peripherals uses either I²C or the GMSL UART format. A bypass mode enables full-duplex communication using a user-defined UART format.

The serializer pre/deemphasis, along with the deserializer channel equalizer, extends the link length and enhances the link reliability. Spread spectrum is available to reduce EMI on the serial and parallel outputs. The serial link connections comply with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

The µC configures various operating conditions of the serializer and the deserializer through internal registers. The default device address of the serializer is 0x80 and default device address of the deserializer is 0x90 (Tables 1 and 2). Write to registers 0x00 or 0x01 in both devices to change the device address of the serializer or the deserializer.

Table 1. Power-Up Default Register Map (see Tables 22 and 24)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x00	0x80	SERID = 1000000, serializer device address is 1000 000 CFGBLOCK = 0, registers 0x00 to 0x1F are read/write
0x01	0x90	DESID = 1001000, deserializer device address is 1001 000 RESERVED = 0
0x02	0x1F, 0x3F	SS = 000 (SSEN = low), SS = 001 (SSEN = high), spread-spectrum settings depend on SSEN pin state at power-up AUDIOEN = 1, I²S channel enabled PRNG = 11, automatically detect the pixel clock range SRNG = 11, automatically detect serial-data rate
0x03	0x00	AUTOFM = 00, calibrate spread-modulation rate only once after locking SDIV = 000000, autocalibrate sawtooth divider
0x04	0x03, 0x13, 0x83, or 0x93	SEREN = 0 ($\overline{\text{AUTOS}}$ = high), SEREN = 1 ($\overline{\text{AUTOS}}$ = low), serial link enable default depends on $\overline{\text{AUTOS}}$ pin state at power-up CLINKEN = 0, configuration link disabled PRBSEN = 0, PRBS test disabled SLEEP = 0 or 1, sleep mode state depends on CDS and $\overline{\text{AUTOS}}$ pin state at power-up (see the *Link Startup Procedure* section) INTTYPE = 00, base mode uses I²C REVCCEN = 1, reverse control channel active (receiving) FWDCCEN = 1, forward control channel active (sending)

Table 1. Power-Up Default Register Map (see Tables 22 and 24) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x05	0x70	I2CMETHOD = 0, I^2C packets include register address DISFPLL = 1, filter PLL disabled CMLLVL = 11, 400mV CML signal level PREEMP = 0000, preemphasis disabled
0x06	0x40	RESERVED = 01000000
0x07	0x22	RESERVED = 00100010
0x08	0x0A (read only)	RESERVED = 0000 LFNEG = 10, no faults detected LFPOS = 10, no faults detected
0x0C	0x70	RESERVED = 01110000
0x0D	0x0F	SETINT = 0, interrupt output set to low INVVSYNC = 0, serializer does not invert DIN19/VS INVHSYNC = 0, serializer does not invert DIN18/HS RESERVED = 0000
0x1E	0x05 (read only)	ID = 00000101, device ID is 0x05
0x1F	0x1X (read only)	RESERVED = 000 CAPS = 1, serializer is HDCP capable REVISION = XXXX, Revision number
0x80 to 0x84	0x0000000000	BKSV = 0x0000000000, HDCP receiver KSV is 0x0000000000
0x85, 0x86	0x0000	RI = 0x0000, RI of the transmitter is 0x0000
0x87	0x00	PJ = 0x00, PJ of the transmitter is 0x00
0x88 to 0x8F	0x0000000000000000 (read only)	AN = 0x0000000000000000, session random number (read only)
0x90 to 0x94	0xXXXXXXXXXX (read only)	AKSV = 0xXXXXXXXXXXXXXXXX, HDCP transmitter KSV is 0xXXXXXXXXXX (read only)
0x95	0x00	PD_HDCP = 0, HDCP circuits powered up EN_INT_COMP = 0, internal link verification disabled FORCE_AUDIO = 0, normal I^2S audio operation FORCE_VIDEO = 0, normal video link operation RESET_HDCP = 0, normal HDCP operation START_AUTHENTICATION = 0, HDCP authentication not started VSYNC_DET = 0, VSYNC rising edge not detected ENCRYPTION_ENABLE = 0, HDCP encryption disabled
0x96	0x01 (read only)	RESERVED = 0000 V_MATCHED = 0, SHA-1 hash value not matched PJ_MATCHED = 0, enhanced link verification response not matched R0_RI_MATCHED = 0, link verification response not matched BKSV_INVALID = 1, invalid receiver KSV
0x97	0x00	RESERVED = 0000000 REPEATER = 0, HDCP receiver is not a repeater

Table 1. Power-Up Default Register Map (see Tables 22 and 24) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x98 to 0x9C	0x0000000000	ASEED = 0x0000000000, optional RNG seed value is 0x0000000000
0x9D to 0x9F	0x000000	DFORCE = 0x000000, video data forced to 0x000000 when FORCE_VIDEO = 1
0xA0 to 0xA3	0x00000000	H0 part of SHA-1 hash value is 0x00000000
0xA4 to 0xA7	0x00000000	H1 part of SHA-1 hash value is 0x00000000
0xA8 to 0xAB	0x00000000	H2 part of SHA-1 hash value is 0x00000000
0xAC to 0xAF	0x00000000	H3 part of SHA-1 hash value is 0x00000000
0xB0 to 0xB3	0x00000000	H4 part of SHA-1 hash value is 0x00000000
0xB4	0x00	Reserved = 0000 MAX_CASCADE_EXCEEDED = 0, 7 or fewer cascaded HDCP devices attached DEPTH = 000, device cascade depth is zero
0xB5	0x00	MAX_DEVS_EXCEEDED = 0, 14 or fewer HDCP devices attached DEVICE_COUNT = 0000000, zero attached devices
0xB6	0x00	GPMEM = 00000000, 0x00 stored in general-purpose memory
0xB7 to 0xB9	0x000000	Reserved = 0x000000
0xBA to 0xFF	All zero	KSV_LIST = all zero, no KSVs stored

X = Indeterminate.

Table 2. Power-Up Default Register Map (see Tables 23 and 25)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x00	0x80	SERID = 1000000, serializer device address is 1000 000 RESERVED = 0
0x01	0x90	DESID = 1001000, deserializer device address is 1001 000 CFGBLOCK = 0, registers 0x00 to 0x1F are read/write
0x02	0x1F or 0x5F	SS = 00 (SSEN = low), SS = 01 (SSEN = high), spread-spectrum settings depend on SSEN pin state at power-up RESERVED = 0 AUDIOEN = 1, I^2S channel enabled PRNG = 11, automatically detect the pixel clock range SRNG = 11, automatically detect serial-data rate
0x03	0x00	AUTOFM = 00, calibrate spread-modulation rate only once after locking RESERVED = 0 SDIV = 00000, autocalibrate sawtooth divider
0x04	0x03, 0x13, 0x43, 0x53	LOCKED = 0, LOCK output is low (read only) OUTENB = 0 ($\overline{ENABLE}$ = low), OUTENB = 1 ($\overline{ENABLE}$ = high), OUTENB default depends on ENABLE pin state at power-up PRBSEN = 0, PRBS test disabled SLEEP = 0 or 1, SLEEP setting default depends on CDS and MS pin state at power-up (see the *Link Startup Procedure* section) INTTYPE = 00, base mode uses I^2C REVCCEN = 1, reverse control channel active (sending) FWDCCEN = 1, forward control channel active (receiving)

Table 2. Power-Up Default Register Map (see Tables 23 and 25) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x05	0x24 or 0x29	I2CMETHOD = 0, I²C master sends the register address HPFTUNE = 01, 3.75MHz equalizer highpass cutoff frequency PDHF = 0, high-frequency boosting disabled EQTUNE = 0100 (EQS = high, 5.2dB), EQTUNE = 1001 (EQS = low, 10.7dB), EQTUNE default setting depends on EQS pin state at power-up
0x06	0x0F	DISSTAG = 0, outputs are staggered AUTORST = 0, error registers/output autoreset disabled DISINT = 0, INT transmission enabled INT = 0, INT output is low (read only) GPIO1OUT = 1, GPIO1 output set to high GPIO1 = 1, GPIO1 input = high (read only) GPIO0OUT = 1, GPIO0 output set to high GPIO0 = 1, GPIO0 input = high (read only)
0x07	0x54	RESERVED = 01010100
0x08	0x30	RESERVED = 001100 DISVSFILT = 0, DOUT19/VS glitch filter active DISHSFILT = 0, DOUT18/HS glitch filter active
0x09	0xC8	RESERVED = 11001000
0x0A	0x12	RESERVED = 00010010
0x0B	0x20	RESERVED = 00100000
0x0C	0x00	ERRTHR = 00000000, error threshold set to zero for decoding errors
0x0D	0x00 (read only)	DECERR = 00000000, zero decoding errors detected
0x0E	0x00 (read only)	PRBSERR = 00000000, zero PRBS errors detected
0x12	0x00	MCLKSRC = 0, MCLK is derived from PCLK (see Table 5) MCLKDIV = 0000000, MCLK output is disabled
0x13	0x10	RESERVED = 00010000
0x14	0x09	INVVSYNC = 0, deserializer does not invert DOUT19/VS INVHSYNC = 0, deserializer does not invert DOUT18/HS RESERVED = 001001
0x1E	0x06 (read only)	ID = 00000100, device ID is 0x06
0x1F	0x1X (read only)	RESERVED = 000 CAPS = 1 HDCP capable REVISION = XXXX
0x80 to 0x84	0xXXXXXXXXXX (read only)	BKSV = 0xXXXXXXXXXX, HDCP receiver KSV is 0xXXXXXXXXXX
0x85, 0x86	0xXXXX (read only)	RI’ = 0xXXXX, RI’ of the transmitter is 0xXXXX

HDCP Gigabit Multimedia Serial Link Serializer/Deserializer

Table 2. Power-Up Default Register Map (see Tables 23 and 25) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x87	0xXX (read only)	PJ' = 0xXXXX, PJ' of the transmitter is 0xXX
0x88 to 0x8F	0x00000000 00000000	AN = 0000000000000000, session random number is 0000000000000000
0x90 to 0x94	0x00000000 00000000	AKSV = 0x0000000000, HDCP transmitter KSV is 0x0000000000000000
0x95	0x00	PD_HDCP = 0, HDCP circuits powered up RESERVED = 000 GPIO1_FUNCTION = 0, normal GPIO1 function GPIO0_FUNCTION = 0, normal GPIO0 function AUTH_STARTED = 0, HDCP authentication not started ENCRYPTION_ENABLE = 0, HDCP encryption disabled
0x96	0x00	RESERVED = 000000 NEW_DEV_CONN = 0, no new devices connected KSV_LIST_READY = 0, KSV list is not ready
0x97	0x00	RESERVED = 0000000 REPEATER = 0, HDCP receiver is not a repeater
0x98 to 0x9F	0x00000000 00000000 (read only)	RESERVED = 0x0000000000000000
0xA0 to 0xA3	0xXXXXXXXX (read only)	H0 part of SHA-1 hash value is 0xXXXXXXXX
0xA4 to 0xA7	0xXXXXXXXX (read only)	H1 part of SHA-1 hash value is 0xXXXXXXXX
0xA8 to 0xAB	0xXXXXXXXX (read only)	H2 part of SHA-1 hash value is 0xXXXXXXXX
0xAC to 0xAF	0xXXXXXXXX (read only)	H3 part of SHA-1 hash value is 0xXXXXXXXX
0xB0 to 0xB3	0xXXXXXXXX (read only)	H4 part of SHA-1 hash value is 0xXXXXXXXX
0xB4	0x00	Reserved = 0000 MAX_CASCADE_EXCEEDED = 0, 7 or fewer cascaded HDCP devices attached DEPTH = 000, device cascade depth is zero
0xB5	0x00	MAX_DEVS_EXCEEDED = 0, 14 or fewer HDCP devices attached DEVICE_COUNT = 0000000, zero attached devices
0xB6	0x00	GPMEM = 00000000, 0x00 stored in general-purpose memory
0xB7 to 0xB9	0x000000 (read only)	Reserved = 0x000000
0xBA to 0xFF	All zero	KSV_LIST = all zero, no KSVs stored

X = Indeterminate.

HDCP Bitmapping and Bus-Width Selection

The parallel input/outputs have two selectable modes, 24-bit mode and 32-bit mode. In 24-bit mode, DIN[28:21] are not available. For both modes, the SD, SCK, and WS pins are for I^2S audio. The serializer/deserializer use pixel clock rates from 8.33MHz to 104MHz for 24-bit mode and 6.25MHz to 78MHz for 32-bit mode.

Table 3 lists the HDCP bit mapping for the parallel inputs. DIN18/HS and DIN19/VS are reserved for HSYNC and VSYNC, respectively. The serializer/deserializer have HDCP encryption on DIN[17:0] and the I^2S input. 32-bit mode has additional HDCP encryption on DIN[26:21].

DIN[28:27] and DIN20 do not have HDCP encryption. SD, when used as an additional data input (AUDIOEN = 0), also does not have HDCP encryption.

Serial Link Signaling and Data Format

The serializer uses CML signaling with programmable pre/deemphasis and AC-coupling. The deserializer uses AC-coupling and programmable channel equalization. Together, the GMSL link can operate at full speed over STP cable lengths to 15m or more.

The serializer scrambles and encodes the input data and sends the 8b/10b coded signal through the serial link. The deserializer recovers the embedded serial clock and then samples, decodes, and descrambles before outputting the data. Figures 22 and 23 show the serial-data packet format after unscrambling and 8b/10b decoding. In 24-bit or 32-bit mode, 21 or 29 bits map to the parallel outputs. The audio channel bit (ACB) contains an encoded audio signal derived from the three I^2S signals (SD, SCK, and WS). The forward control channel (FCC)

Table 3. HDCP Mapping and Bus Width Selection

INPUT BITS	24-BIT MODE (BWS = LOW)		32-BIT MODE (BWS = HIGH)	
	HDCP MAPPING*	HDCP ENCRYPTION CAPABILITY	HDCP MAPPING*	HDCP ENCRYPTION CAPABILITY
DIN[17:0]	RGB	Yes	RGB	Yes
DIN18/HS	HS	No	HS	No
DIN19/VS	VS	No	VS	No
DIN20	DE	No	DE	No
DIN[26:21]	Not Available	—	RGB	Yes
DIN[28:27]	Not Available	—	CNTL	No
SD	SD	I^2S**	SD	I^2S**

**Bit assignments of DIN[28:0] are interchangeable if HDCP is not used.*

***HDCP encryption on SD when used as an I^2S signal.*

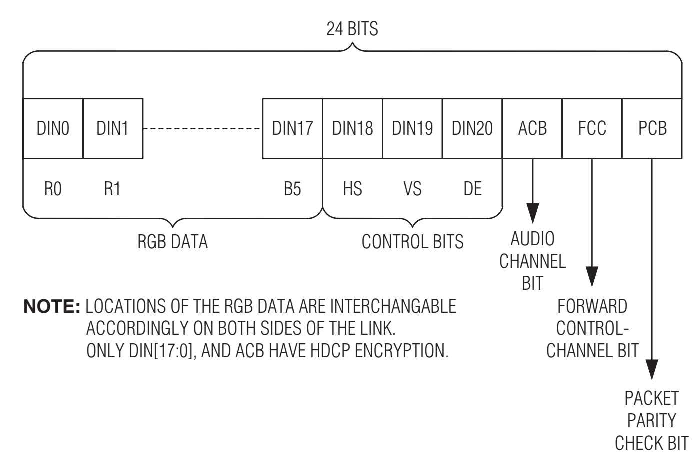


Figure 22. 24-Bit Mode Serial Link Data Format

HDCP Gigabit Multimedia Serial Link Serializer/Deserializer

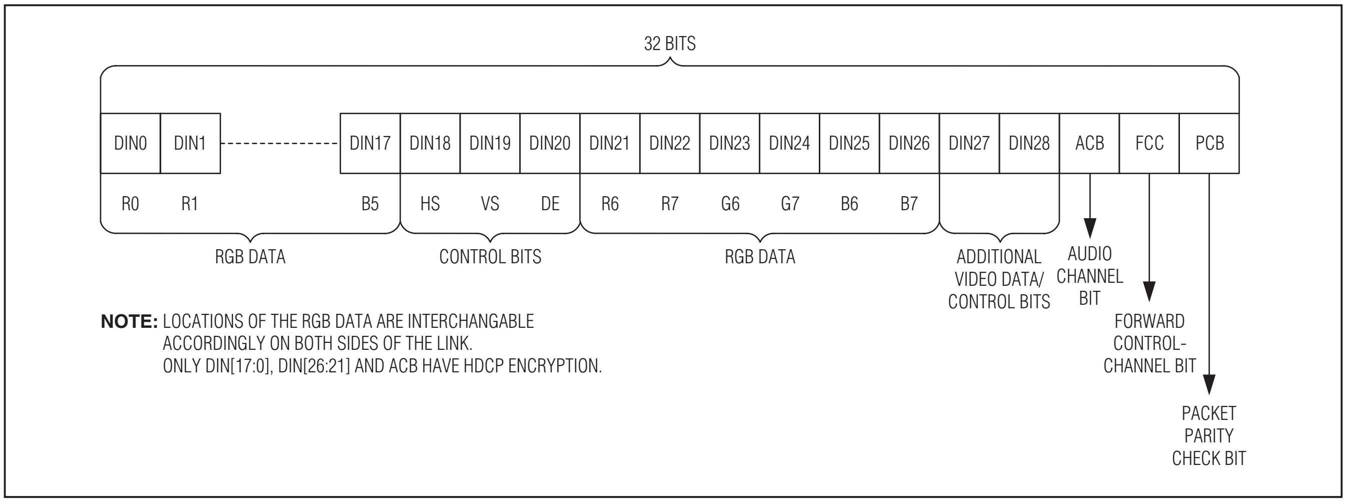


Figure 23. 32-Bit Mode Serial Link Data Format

Table 4. Maximum Audio WS Frequency (kHz) for Various PCLKIN Frequencies

WORD LENGTH (bits)	PCLKIN FREQUENCY (DRS = LOW) (MHz)				PCLKIN FREQUENCY (DRS = HIGH) (MHz)			
	12.5	15	16.6	> 20	6.25	7.5	8.33	> 10
8	> 192	> 192	> 192	> 192	> 192	> 192	> 192	> 192
16	> 192	> 192	> 192	> 192	> 192	> 192	> 192	> 192
18	185.5	> 192	> 192	> 192	185.5	> 192	> 192	> 192
20	174.6	> 192	> 192	> 192	174.6	> 192	> 192	> 192
24	152.2	182.7	> 192	> 192	152.2	182.7	> 192	> 192
32	123.7	148.4	164.3	> 192	123.7	148.4	164.3	> 192

bit carries the forward control data. The last bit (PCB) is the parity bit of the previous 23 or 31 bits.

Reverse Control Channel

The serializer uses the reverse control channel to receive I^2C/UART and interrupt signals from the deserializer in the opposite direction of the video stream. The reverse control channel and forward video data coexist on the same twisted pair forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 500µs after power-up. The serializer temporarily disables the reverse control channel for 350µs after starting/stopping the forward serial link.

Data-Rate Selection

The serializer/deserializer use the DRS input to set the PCLKIN frequency range. Set DRS high for a PCLKIN frequency range of 6.25MHz to 12.5MHz (32-bit mode) or 8.33MHz to 16.66MHz (24-bit mode). Set DRS low for normal operation with a PCLKIN frequency range of 12.5MHz to 78MHz (32-bit mode) or 16.66MHz to 104MHz (24-bit mode).

Audio Channel

The I^2S audio channel supports audio sampling rates from 8kHz to 192kHz and audio word lengths from 4 bits to 32 bits. The audio bit clock (SCK) does not have to be synchronized with PCLKIN. The serializer automatically encodes audio data into a single bit stream synchronous with PCLKIN. The deserializer decodes the audio stream and stores audio words in a FIFO. Audio rate detection uses an internal oscillator to continuously determine the audio data rate and output the audio in I^2S format. The audio channel is enabled by default. When the audio channel is disabled, the audio data on the serializer and deserializer are treated as an additional parallel signal (DIN_/DOUT_).

Since the audio data sent through the serial link is synchronized with PCLKIN, low PCLKIN frequencies limit the maximum audio sampling rate. Table 4 lists the maximum audio sampling rate for various PCLKIN frequencies. Spread-spectrum settings do not affect the I^2S data rate or WS clock frequency.

Additional MCLK Output for Audio Applications

Some audio DACs, such as the MAX9850, do not require a synchronous main clock (MCLK), while other DACs require MCLK to be a specific multiple of WS. If an audio DAC chip needs the MCLK to be a multiple of WS, use an external PLL to regenerate the required MCLK from PCLKOUT or SCK.

For audio applications that cannot directly use PCLKOUT, the MAX9264 provides a divided MCLK output on DOUT28/MCLK at the expense of one less control line in 32-bit mode (24-bit mode is not affected). By default, DOUT28/MCLK operates as a parallel data output, and MCLK is turned off. Set MCLKDIV (MAX9264 register 0x12, D[6:0]) to a non-zero value to enable the MCLK output. Set MCLKDIV to 0x00 to disable MCLK and set DOUT28/MCLK as a parallel data output.

The output MCLK frequency is:

$$f_{MCLK} = \frac{f_{SRC}}{MCLKDIV}$$

where f_{SRC} is the MCLK source frequency (Table 5)

MCLKDIV is the divider ratio from 1 to 127

Choose MCLKDIV values so that f_{MCLK} is not greater than 60MHz. MCLK frequencies derived from PCLKIN (MCLKSRC = 0) are not affected by spread-spectrum settings in the deserializer. Enabling spread spectrum in the serializer, however, introduces spread spectrum into MCLK. Spread-spectrum settings of either device do not affect MCLK frequencies derived from the internal oscillator. The internal oscillator frequency ranges from 100MHz to 150MHz over all process corners and operating conditions.

Control Channel and Register Programming

The control channel is available for the µC to send and receive control data over the serial link simultaneously with the high-speed data. Configuring the CDS pin allows the µC to control the link from either the serializer or the deserializer side to support video-display or image-sensing applications. The control channel between the µC and serializer or deserializer runs in base mode or bypass mode according to the mode selection (MS) input of the device connected to the µC. Base mode is a half-duplex control channel and the bypass mode is a full-duplex control channel.

Base Mode

In base mode, the µC is the host and can access the core and HDCP registers of both the serializer and deserializer from either side of the link by using the GMSL UART protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer, with the UART packets converted to I^2C by the device on the remote side of the link (deserializer for LCD or serializer for image-sensing applications). The µC communicates with a UART peripheral in base mode (through INTTYPE register settings), using the half-duplex default GMSL UART protocol of the serializer/deserializer. The device addresses of the serializer and deserializer in base mode are programmable. The default value is 0x80 for the serializer and 0x90 for the deserializer.

When the peripheral interface uses I^2C (default), the serializer/deserializer convert packets to I^2C that have device addresses different from those of the serializer or deserializer. The converted I^2C bit rate is the same as the original UART bit rate.

The deserializer uses a proprietary differential line coding to send signals back towards the serializer. The speed of the control channel ranges from 9.6kbps to

Table 5. Deserializer f_{SRC} Settings

MCLKSRC SETTING (REGISTER 0x12, D7)	DATA RATE SETTING	BIT WIDTH SETTING	MCLK SOURCE FREQUENCY (f_{SRC})
0	High speed	24-bit mode	3 x f_{PCLKIN}
		32-bit mode	4 x f_{PCLKIN}
	Low speed	24-bit mode	6 x f_{PCLKIN}
		32-bit mode	8 x f_{PCLKIN}
1	—	—	Internal oscillator (120MHz typ)

1Mbps in both directions. The serializer and deserializer automatically detect the control-channel bit rate in base mode. Packet bit rates can vary up to 3.5x from the previous bit rate. See the *Changing the Clock Frequency* section.

Figure 24 shows the UART protocol for writing and reading in base mode between the µC and the serializer/deserializer.

Figure 25 shows the UART data format. Figures 26 and 27 detail the formats of the SYNC byte (0x79) and the ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK byte, respectively. Events such as device wake-up and interrupt generate transitions on the control channel that should be ignored by the µC. Data written to the serializer/deserializer registers do not take effect until after the acknowledge byte is sent. This allows the µC to verify write commands received without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the host UART data rate automatically. If the INT or MS inputs of the deserializer toggle while there is control-channel communication, the control-channel communication can be corrupted.

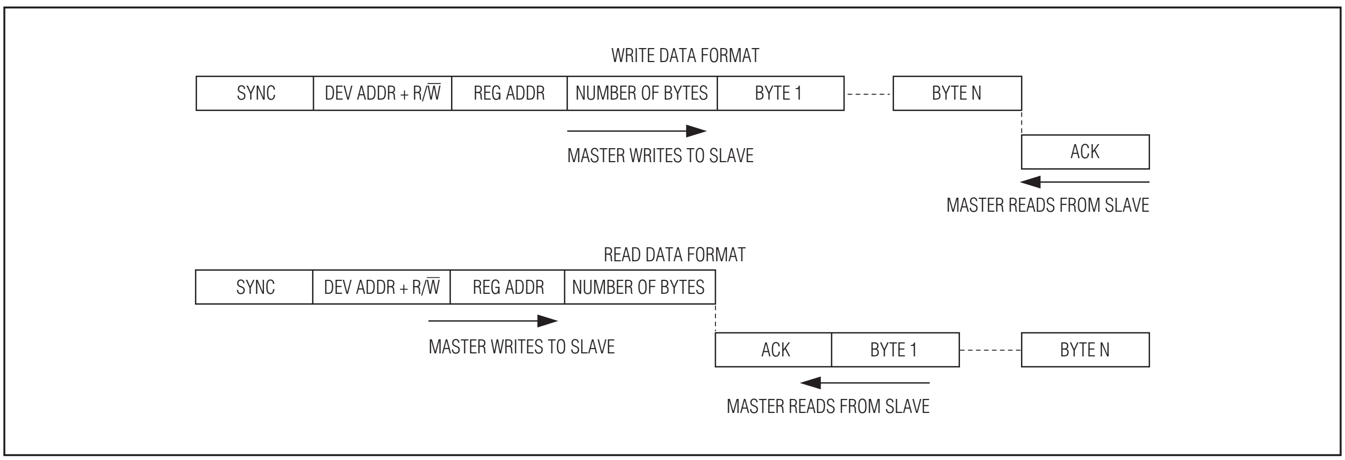


Figure 24. GMSL UART Protocol for Base Mode

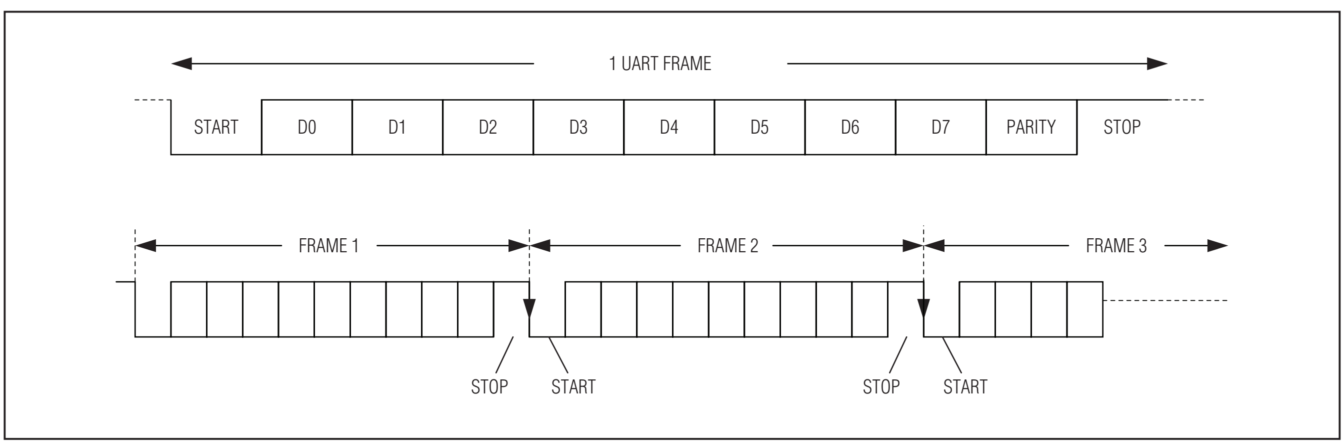


Figure 25. GMSL UART Data Format for Base Mode

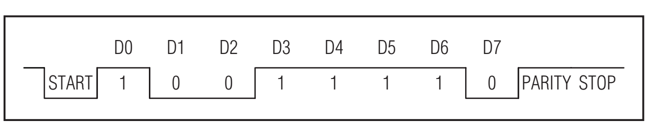


Figure 26. SYNC Byte (0x79)

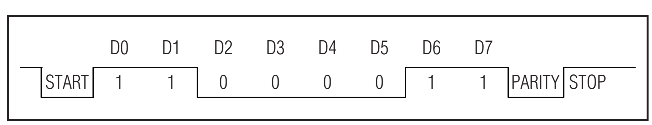


Figure 27. ACK Byte (0xC3)

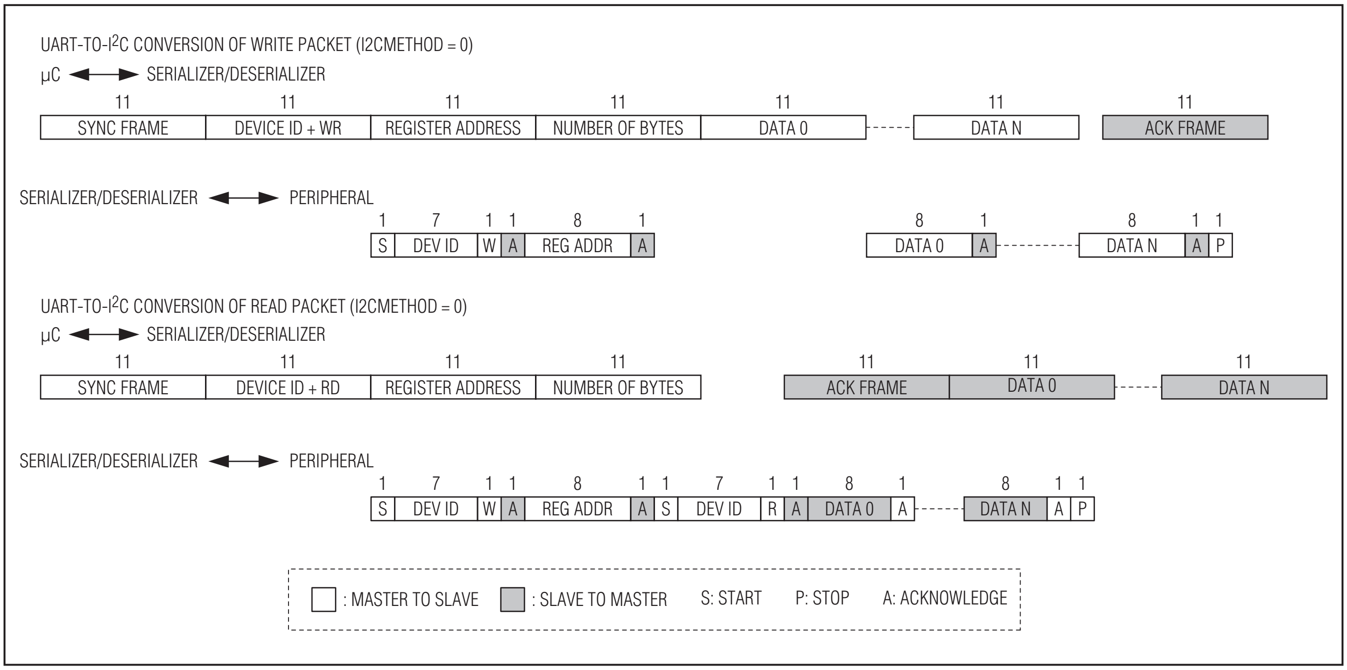


Figure 28. Format Conversion Between GMSL UART and I2C with Register Address (I2CMETHOD = 0)

In the event of a missed acknowledge, the μC should assume there was an error in the packet when the slave device receives it, or that an error occurred during the response from the slave device. In base mode, the μC must keep the UART Tx/Rx lines high for 16 bit-times before starting to send a new packet.

As shown in Figure 28, the remote-side device converts the packets going to or coming from the peripherals from the UART format to the I2C format and vice versa. The remote device removes the byte number count and adds or receives the ACK between the data bytes of I2C. The I2C's data rate is the same as the UART data rate.

Interfacing Command-Byte-Only I2C Devices

The serializer and deserializer UART-to-I2C conversion interfaces with devices that do not require register addresses, such as the MAX7324 GPIO expander. In this mode, the I2C master ignores the register address byte and directly reads/writes the subsequent data bytes (Figure 29). Change the communication method of the I2C master using the I2CMETHOD bit. I2CMETHOD = 1 sets command-byte-only mode, while I2CMETHOD = 0 sets normal mode where the first byte in the data stream is the register address.

Bypass Mode

In bypass mode, the serializer/deserializer ignore UART commands from the μC and the μC communicates with the peripherals directly using its own defined UART protocol. The μC cannot access the serializer/deserializer's registers in this mode. Peripherals accessed through the forward control channel using the UART interface need to handle at least one PCLKIN period ±10ns of jitter due to the asynchronous sampling of the UART signal by PCLKIN. Set MS = high to put the control channel into bypass mode. For applications with the μC connected to the deserializer, (CDS is high) there is a 1ms wait time between setting MS high and the bypass control channel being active. There is no delay time when switching to bypass mode when the μC is connected to the serializer (CDS = low). Do not send a logic-low value longer than 100μs to ensure proper interrupt functionality. Bypass mode accepts bit rates down to 10kbps in either direction. See the *Interrupt Control* section for interrupt functionality limitations. The control-channel data pattern should not be held low longer than 100μs if interrupt control is used.

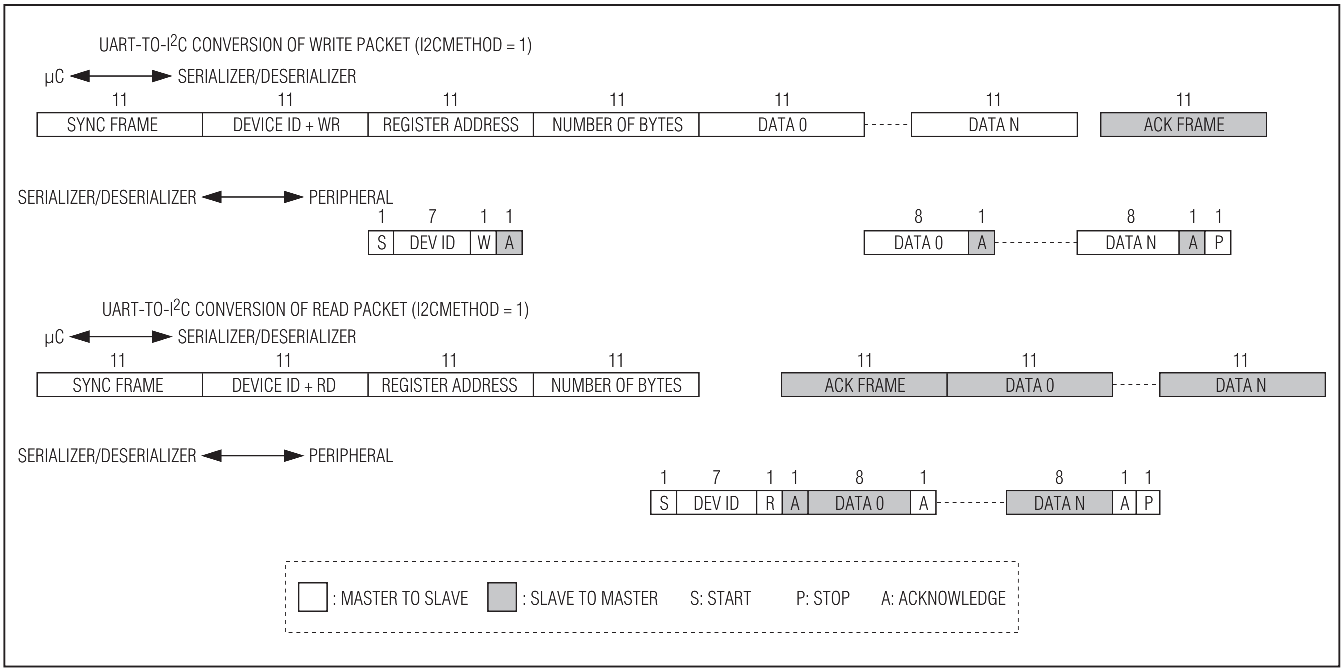


Figure 29. Format Conversion Between GMSL UART and I2C with Register Address (I2CMETHOD = 1)

Interrupt Control

The INT pin of the serializer is the interrupt output and the INT pin of the deserializer is the interrupt input. The interrupt output on the serializer follows the transitions at the interrupt input. This interrupt function supports remote-side functions such as touch-screen peripherals, remote power-up, or remote monitoring. Interrupts that occur during periods where the reverse control channel is disabled, such as link startup/shutdown, are automatically resent once the reverse control channel becomes available again. Bit D4 of register 0x06 in the deserializer also stores the interrupt input state. The INT output of the serializer is low after power-up. In addition, the µC can set the INT output of the serializer by writing to the SETINT register bit. In normal operation, the state of the interrupt output changes when the interrupt input on the deserializer toggles. Do not send a logic-low value longer than 100µs in either base or bypass mode to ensure proper interrupt functionality.

Pre/Deemphasis Driver

The serial line driver in the serializer employs current-mode logic (CML) signaling. The driver can generate an adjustable waveform according to the cable length and characteristics. There are 13 preemphasis settings as shown in Table 6. Negative preemphasis levels are deemphasis levels in which the preemphasized swing level is the same as normal swing, but the no-transition data is deemphasized. Program the preemphasis levels through register 0x05 D[3:0] of the serializer. This preemphasis function compensates the high frequency loss of the cable and enables reliable transmission over longer link distances. Additionally, a lower power drive mode can be entered by programming CMLLVL bits (0x05, D[5:4]) to reduce the driver strength down to 75% (CMLLVL = 10) or 50% (CMLLVL = 01) from 100% (CMLLVL = 11, default).

Table 6. Serializer CML Driver Strength (Default Level, CMLLVL = 11)

PREEMPHASIS LEVEL (dB)*	PREEMPHASIS SETTING (0x05, D[3:0])	I_{CML} (mA)	I_{PRE} (mA)	SINGLE-ENDED VOLTAGE SWING	
				MAX (mV)	MIN (mV)
-6.0	0100	12	4	400	200
-4.1	0011	13	3	400	250
-2.5	0010	14	2	400	300
-1.2	0001	15	1	400	350
0	0000	16	0	400	400
1.1	1000	16	1	425	375
2.2	1001	16	2	450	350
3.3	1010	16	3	475	325
4.4	1011	16	4	500	300
6.0	1100	15	5	500	250
8.0	1101	14	6	500	200
10.5	1110	13	7	500	150
14.0	1111	12	8	500	100

Negative preemphasis levels denote deemphasis.

Table 7. Deserializer Cable Equalizer Boost Levels

BOOST SETTING (0x05 D[3:0])	TYPICAL BOOST GAIN (dB)
0000	2.1
0001	2.8
0010	3.4
0011	4.2
0100	5.2 **Power-Up Default** **(EQS = high)**
0101	6.2
0110	7
0111	8.2
1000	9.4
1001	10.7 **Power-Up Default** **(EQS = low)**
1010	11.7
1011	13

Line Equalizer

The deserializer includes an adjustable line equalizer to further compensate cable attenuation at high frequencies. The cable equalizer has 11 selectable levels of compensation from 2.1dB to 13dB (Table 7). The EQS input selects the default equalization level at power-up. The state of EQS is latched upon power-up or when resuming from power-down mode. To select other equalization levels, set the corresponding register bits in the deserializer (0x05 D[3:0]). Use equalization in the deserializer, together with preemphasis in the serializer, to create the most reliable link for a given cable.

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Spread Spectrum

To reduce the EMI generated by the transitions on the serial link and parallel outputs, both the serializer and deserializer support spread spectrum. Turning on spread spectrum on the deserializer spreads the parallel video outputs. Turning on spread spectrum on the serializer spreads the serial link, along with the deserializer parallel outputs. Do not enable spread for both the serializer and deserializer. The six selectable spread-spectrum rates at the serializer serial output are ±0.5%, ±1%, ±1.5%, ±2%, ±3%, and ±4% (Table 8). Some spread-spectrum rates can only be used at lower PCLK_ frequencies (Table 9). There is no PCLK_ frequency limit for the 0.5% spread rate. The two selectable spread-spectrum rates at the deserializer parallel output are ±2% and ±4% (Table 10).

Set the serializer SSEN input high to select 0.5% spread at power-up and SSEN input low to select no spread at power-up. Set the deserializer SSEN input high to select 2% spread at power-up and SSEN input low to select no spread at power-up. The state of SSEN is latched upon power-up or when resuming from power-down mode.

Whenever the serializer spread spectrum is turned on or off, the serial link automatically restarts and remains unavailable while the deserializer relocks to the serial data. Turning on spread spectrum on the serializer or deserializer does not affect the audio data stream. Changes in the serializer spread settings only affect the deserializer MCLK output if it is derived from PCLK_ (MCLKSRC = 0).

The serializer/deserializer include a sawtooth divider to control the spread-modulation rate. Auto detection or manual programming of the PCLKIN operation range guarantees a spread-spectrum modulation frequency within 20kHz to 40kHz. Additionally, manual configuration of the sawtooth divider (SDIV: 0x03, D[5:0]) allows the user to set a modulation frequency according to the PCLKIN frequency. Always keep the modulation frequency between 20kHz to 40kHz to ensure proper operation.

Table 8. Serializer Serial Output Spread

SS	SPREAD (%)
000	No spread spectrum. **Power-up default when SSEN = low.**
001	±0.5% spread spectrum. **Power-up default when SSEN = high.**
010	±1.5% spread spectrum.
011	±2% spread spectrum.
100	No spread spectrum.
101	±1% spread spectrum.
110	±3% spread spectrum.
111	±4% spread spectrum.

Table 9. Serializer Spread Rate Limitations

24-BIT MODE PCLK_ FREQUENCY (MHz)	32-BIT MODE PCLK_ FREQUENCY (MHz)	SERIAL LINK BIT-RATE (Mbps)	AVAILABLE SPREAD RATES
< 33.3	< 25	< 1000	All rates available
33.3 to < 66.7	20 to < 50	1000 to < 2000	1.5%, 1.0%, 0.5%
66.7+	50+	2000+	0.5%

Table 10. Deserializer Parallel Output Spread

SS	SPREAD (%)
00	No spread spectrum. **Power-up default when SSEN = low.**
01	±2% spread spectrum. **Power-up default when SSEN = high.**
10	No spread spectrum.
11	±4% spread spectrum.

Manual Programming of the Spread-Spectrum Divider

The modulation rate for the serializer/deserializer relates to the PCLK_ frequency as follows:

$$f_M = (1 + DRS)\frac{f_{PCLK\_}}{MOD \times SDIV}$$

where:

f_M = Modulation frequency

DRS = DRS pin input value (0 or 1)

$f_{PCLK\_}$ = PCLK_ frequency

MOD = Modulation coefficient given in Table 11 or 12

SDIV = 6- or 5-bit SDIV setting, manually programmed by the µC

To program the SDIV setting, first look up the modulation coefficient according to the part number and desired bus-width and spread-spectrum settings. Solve the above equation for SDIV using the desired pixel clock and modulation frequencies. If the calculated SDIV value is larger than the maximum allowed SDIV value in Table 11 or 12, set SDIV to the maximum value.

Sleep Mode

The serializer/deserializer include a low-power sleep mode to reduce power consumption on the device not attached to the µC (the deserializer in LCD applications and the serializer in camera applications). Set the corresponding remote IC's SLEEP bit to 1 to initiate sleep mode. The serializer sleeps immediately after setting its SLEEP = 1. The deserializer sleeps after serial link inactivity or 8ms (whichever arrives first) after setting its SLEEP = 1. See the *Link Startup Procedure* section for details on waking up the device for different µC and starting conditions.

The µC side device cannot enter into sleep mode. If an attempt is made to program the µC side device for sleep, the SLEEP bit remains 0. Use the $\overline{PWDN}$ input pin to bring the µC side device into a low-power state. Entering sleep mode resets the HDCP registers, but not the configuration registers.

Power-Down Mode

The serializer/deserializer include a power-down mode to further reduce power consumption. Set $\overline{PWDN}$ low to enter power-down mode. While in power-down mode, the

Table 11. Serializer Modulation Coefficients and Maximum SDIV Settings

BIT-WIDTH MODE	SPREAD-SPECTRUM SETTING (%)	MODULATION COEFFICIENT MOD (dec)	SDIV UPPER LIMIT (dec)
32 bit	1	104	40
	0.5	104	63
	3	152	27
	1.5	152	54
	4	204	15
	2	204	30
24 bit	1	80	52
	0.5	80	63
	3	112	37
	1.5	112	63
	4	152	21
	2	152	42

Table 12. Deserializer Modulation Coefficients and Maximum SDIV Settings

SPREAD-SPECTRUM SETTING (%)	MODULATION COEFFICIENT (dec)	SDIV UPPER LIMIT (dec)
4	208	15
2	208	30

outputs of the device remain high impedance. Entering power-down mode resets the internal registers of the device. In addition, upon exiting power-down mode, the serializer/deserializer relatch the state of external pins SSEN, DRS, $\overline{\text{AUTOS}}$, and EQS.

Configuration Link Mode

The GMSL includes a low-speed configuration link to allow control-data connection between the two devices in the absence of a valid clock input. In either display or camera applications, the configuration link can be used to program equalizer/preemphasis or other registers before establishing the video link. An internal oscillator provides PCLKIN for establishing the serial configuration link between the serializer and deserializer. Set CLINKEN = 1 on the serializer to turn on the configuration link. The configuration link remains active as long as the video link has not been enabled. The video link overrides the configuration link and attempts to lock when SEREN = 1.

Link Startup Procedure

Table 13 lists four startup cases for video-display applications. Table 14 lists two startup cases for image-sensing applications. In either video-display or image-sensing applications, the control link is always available after the high-speed data link or the configuration link is established and the serializer/deserializer registers or the peripherals are ready for programming.

Video-Display Applications

For the video-display application, with a remote display unit, connect the µC to the serializer and set CDS = low for both the serializer and deserializer. Table 13 summarizes the four startup cases based on the settings of $\overline{\text{AUTOS}}$ and MS.

Case 1: Autostart Mode

After power-up or when $\overline{\text{PWDN}}$ transitions from low to high for both the serializer and deserializer, the serial link establishes if a stable clock is present. The serializer locks to the clock and sends the serial data to the deserializer. The deserializer then detects activity on the serial link and locks to the input serial data.

Case 2: Standby Start Mode

After power-up or when $\overline{\text{PWDN}}$ transitions from low to high for both the serializer and deserializer, the deserializer starts up in sleep mode, and the serializer stays in standby mode (does not send serial data). Use the µC and program the serializer to set SEREN = 1 to establish a video link or CLINKEN = 1 to establish the configuration link. After locking to a stable clock (for SEREN = 1) or the internal oscillator (for CLINKEN = 1), the serializer sends a wake-up signal to the deserializer. The deserializer exits sleep mode after locking to the serial data and sets SLEEP = 0. If after 8ms the deserializer does not lock to the input serial data, the deserializer goes back to sleep, and the internal sleep bit remains set (SLEEP = 1).

Table 13. Start Mode Selection for Display Applications (CDS = Low)

CASE	$\overline{\text{AUTOS}}$ (SERIALIZER)	SERIALIZER POWER-UP STATE	MS (DESERIALIZER)	DESERIALIZER POWER-UP STATE	LINK STARTUP MODE
1	Low	Serialization enabled	Low	Normal (SLEEP = 0)	Both devices power up with serial link active (autostart).
2	High	Serialization disabled	High	Sleep mode (SLEEP = 1)	Serial link is disabled and the deserializer powers up in sleep mode. Set SEREN = 1 or CLINKEN = 1 in the serializer to start the serial link and wake up the deserializer.
3	High	Serialization disabled	Low	Normal (SLEEP = 0)	Both devices power up in normal mode with the serial link disabled. Set SEREN = 1 or CLINKEN = 1 in the serializer to start the serial link.
4	Low	Serialization enabled	High	In sleep mode (SLEEP = 1)	The deserializer starts in sleep mode. Link autostarts upon serializer power-up. Use this case when the deserializer powers up before the serializer.

Case 3: Remote Side Autostart Mode

After power-up or when $\overline{\text{PWDN}}$ transitions from low to high, the remote device (deserializer) starts up and tries to lock to an incoming serial signal with sufficient power. The host side (serializer) is in standby mode and does not try to establish a link. Use the µC and program the serializer to set SEREN = 1 (and apply a stable clock signal) to establish a video link or CLINKEN = 1 to establish the configuration link. In this case, the deserializer ignores the short wake-up signal sent from the serializer.

Case 4: Remote Side in Sleep Mode

After power-up or when $\overline{\text{PWDN}}$ transitions from low to high, the remote device (deserializer) starts up in sleep mode. The high-speed link establishes automatically after the serializer powers up with a stable clock signal and sends a wake-up signal to the deserializer. Use this mode in applications where the deserializer powers up before the serializer.

Image-Sensing Applications

For image-sensing applications, connect the µC to the deserializer and set CDS = high for both the serializer and deserializer. The deserializer powers up normally (SLEEP = 0) and continuously tries to lock to a valid serial input. Table 14 summarizes both startup cases, based on the state of the serializer's $\overline{\text{AUTOS}}$ pin.

Case 1: Autostart Mode

After power-up, or when $\overline{\text{PWDN}}$ transitions from low to high, the serializer locks to a stable input clock and sends the high-speed data to the deserializer. The deserializer locks to the serial data and outputs the video data and clock.

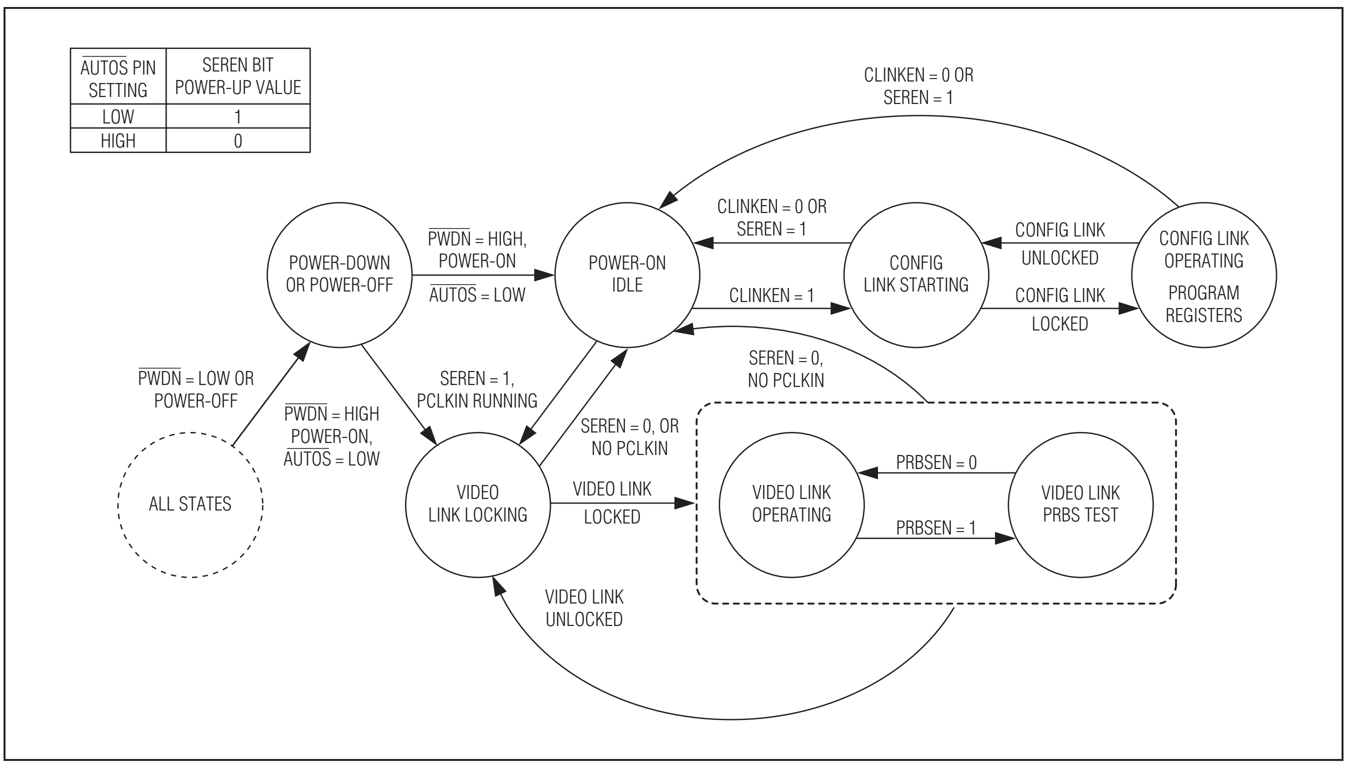

Figure 30. Serializer State Diagram, CDS = Low (LCD Application)

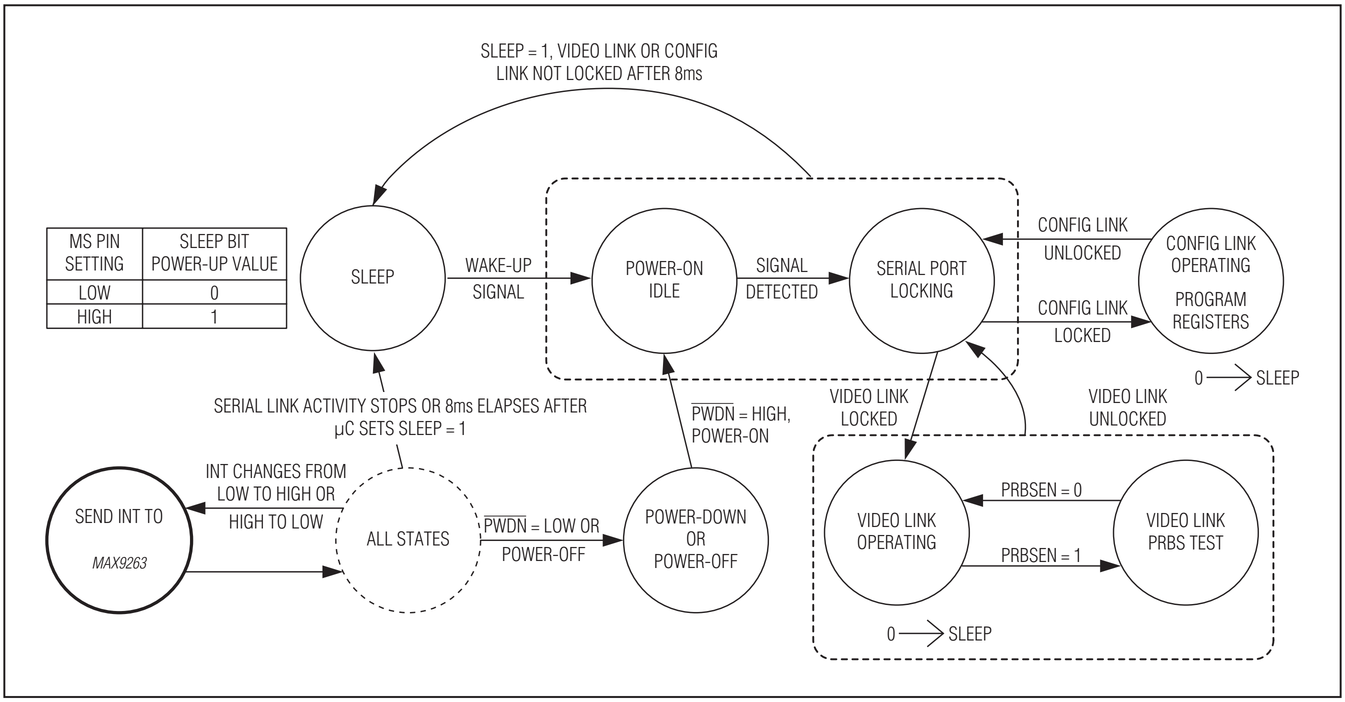

Figure 31. Deserializer State Diagram, CDS = Low (LCD Application)

Table 14. Start Mode Selection for Image-Sensing Application (CDS = High)

CASE	$\overline{\text{AUTOS}}$ (SERIALIZER)	SERIALIZER POWER-UP STATE	DESERIALIZER POWER-UP STATE	LINK STARTUP MODE
1	Low	Serialization enabled	Normal (SLEEP = 0)	Autostart
2	High	Sleep mode (SLEEP = 1)	Normal (SLEEP = 0)	The serializer is in sleep mode. Wake up the serializer through the control channel (µC attached to deserializer).

Case 2: Sleep Mode

After power-up or when $\overline{\text{PWDN}}$ transitions from low to high, the serializer starts up in sleep mode. To wake up the serializer, use the µC to send a GMSL protocol UART frame containing at least three rising edges (e.g., 0x66), at a bit rate no greater than 1Mbps. The low-power wake-up receiver of the serializer detects the wake-up frame over the reverse control channel and powers up. Reset the sleep bit (SLEEP = 0) of the serializer using a regular control-channel write packet to power up the device fully. Send the sleep bit write packet at least 500µs after the wake-up frame. The serializer goes back to sleep mode if its sleep bit is not cleared within 5ms (min) after detecting a wake-up frame.

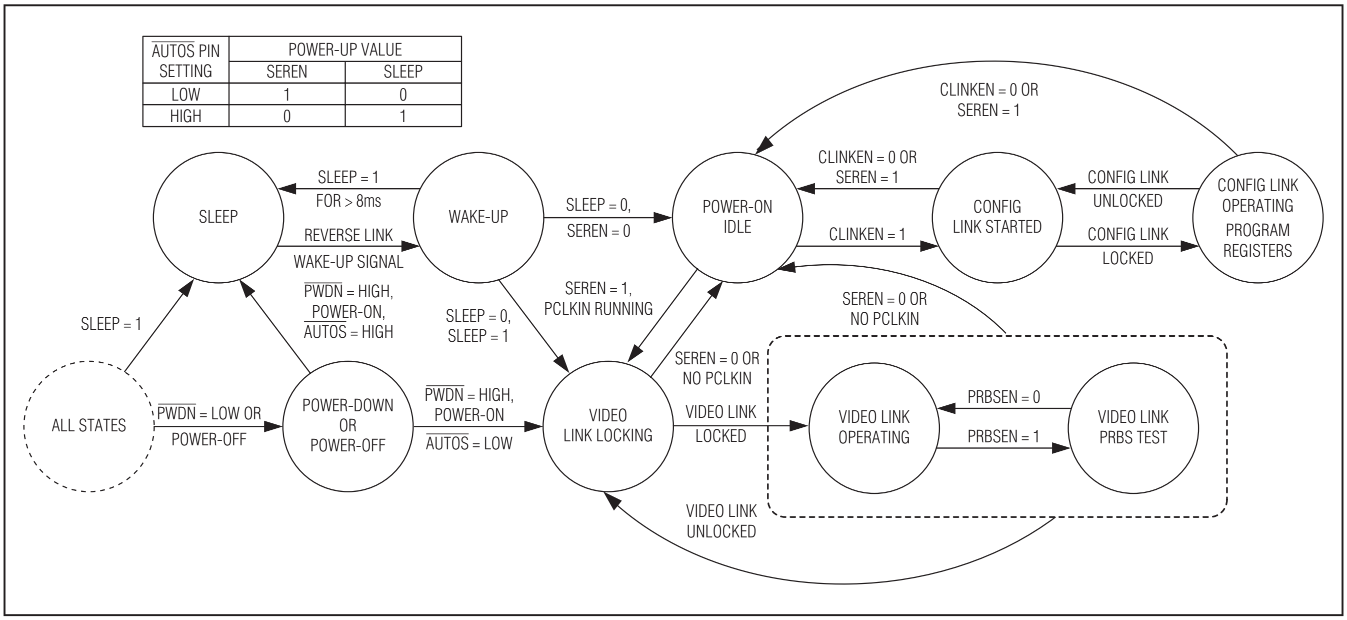

Figure 32. Serializer State Diagram, CDS = High (Camera Application)

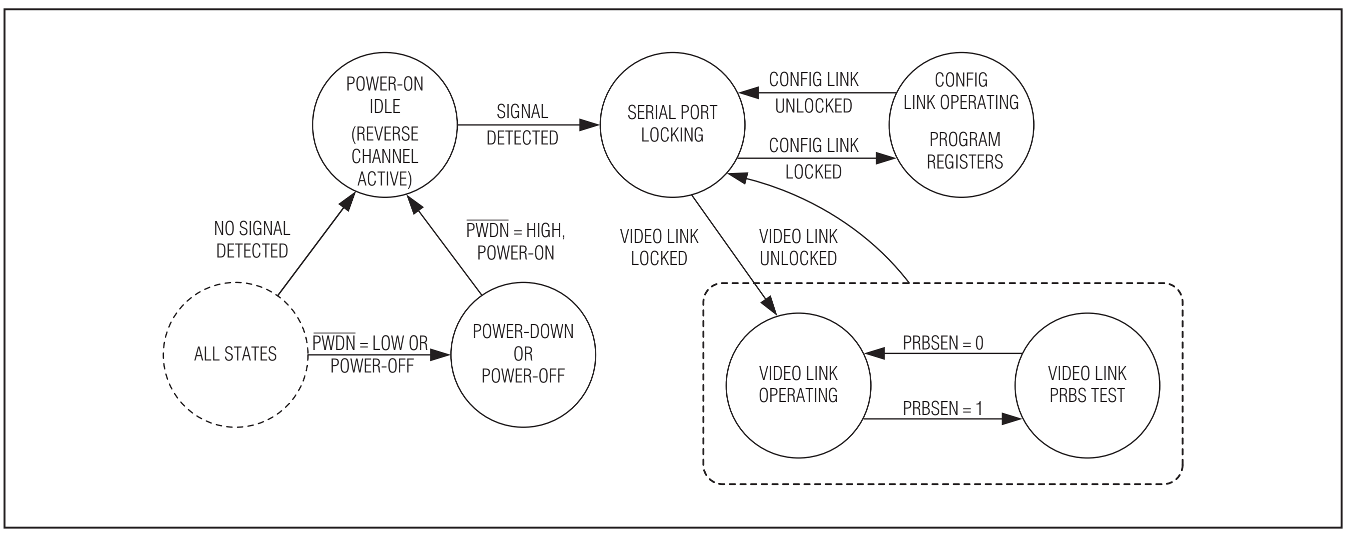

Figure 33. Deserializer State Diagram, CDS = High (Camera Application)

High-Bandwidth Digital Content Protection (HDCP)

Note: The explanation of HDCP operation in this data sheet is given as a guide for general understanding. Implementation of HDCP in a product must meet the requirements given in the *HDCP System v1.3 Amendment for GMSL* available from DCP, LLC.

HDCP uses two main phases of operation: authentication and the link integrity check. The µC starts authentication by writing to the START_AUTHENTICATION bit in the serializer. The serializer generates a 64-bit random number. The host µC first reads the 64-bit random number from the serializer and writes it to the deserializer. The µC then reads the serializer public key selection vector (AKSV) and writes it to the deserializer. The µC

HDCP Gigabit Multimedia Serial Link Serializer/Deserializer

then reads the deserializer KSV (BKSV) and writes it to the serializer. The µC begins checking BKSV against the revocation list. Using the cipher, the serializer and deserializer calculate a 16-bit response value, R0 and R0', respectively. The GMSL amendment for HDCP reduces the 100ms minimum wait time allowed for the receiver to generate R0' (specified in HDCP rev 1.3) to 128 pixel clock cycles in the GMSL amendment.

There are two response value comparison modes: internal comparison and µC comparison. Set EN_INT_COMP = 1 to select internal comparison mode. Set EN_INT_COMP = 0 to select µC comparison mode. In internal comparison mode, the µC reads the deserializer response R0' and writes it to the serializer. The serializer compares R0' to its internally generated response value R0, and sets R0_RI_MATCHED. In µC comparison mode, the µC reads and compares the R0/R0' values from the serializer/deserializer.

During response value generation and comparison, the host µC checks for a valid BKSV (having 20 1's and 20 0's, which is also reported in BKSV_INVALID) and checks BKSV against the revocation list. If BKSV is not on the list, and the response values match, the host authenticates the link. If the response values do not match, the µC resamples the response values (as described in *HDCP rev 1.3 Appendix C*). If resampling fails, the µC restarts authentication by setting the RESET_HDCP bit in the serializer. If BKSV appears on the revocation list, the host cannot transmit data that requires protection. The host knows when the link is authenticated and decides when to output data requiring protection. The µC performs a link integrity check every 128 frames or every 2 seconds ±0.5 seconds. The serializer/deserializer generate response values every 128 frames. These values are compared internally (internal comparison mode) or can be compared in the host µC.

In addition, the serializer/deserializer provide response values for the enhanced link verification. Enchanced link verification is an optional method of link verification for faster detection of loss of synchronization. For this option, the serializer and deserializer generate 8-bit enhanced link verification response values, PJ and PJ', every 16 frames. The host must detect three consecutive PJ/PJ' mismatches before resampling.

Encryption Enable

The GMSL link transfers either encrypted or nonencrypted data. To encrypt data, the host µC sets the encryption enable (ENCRYPTION_ENABLE) bit in both the serializer and deserializer. The µC must set ENCRYPTION_ENABLE in the same VSYNC cycle in both the serializer and deserializer (no internal VSYNC falling edges between the two writes). The same timing applies when clearing ENCRYPTION_ENABLE to disable encryption.

Note: ENCRYPTION_ENABLE enables/disables encryption on the GMSL irrespective of the content. To comply with HDCP, the µC must not allow content requiring encryption to cross the GMSL unencrypted. See the *Force Video/Force Audio Data* section.

The µC must complete the authentication process before enabling encryption. In addition, encryption must be disabled before starting a new authentication session.

VSYNC Detection

If the µC cannot detect the VSYNC falling edge, it can use the serializer's VSYNC_DET register bit. The host µC first writes 0 to the VSYNC_DET bit. The serializer then sets VSYNC_DET = 1 once it detects an internal VSYNC falling edge (which may correspond to an external VSYNC rising edge if INVVSYNC of the serializer is set). The µC continuously reads VSYNC_DET and waits for the next internal VSYNC falling edge before setting ENCRYPTION_ENABLE. Poll VSYNC_DET fast enough to allow time to set ENCRYPTION_ENABLE in both the serializer/deserializer within the same VSYNC cycle.

Synchronization of Encryption

The video vertical sync (VSYNC) synchronizes the start of encryption. Once encryption has started, the GMSL generates a new encryption key for each frame and each line, with the internal falling edge of VSYNC and HSYNC. Rekeying is transparent to data and does not disrupt the encryption of video or audio data.

Repeater Support

The serializer/deserializer have features to build an HDCP repeater. An HDCP repeater receives and decrypts HDCP content and then encrypts and transmits on one or more downstream links. A repeater can also use decrypted HDCP content (for example to display on a screen). To support HDCP repeater authentication protocol, the deserializer has a REPEATER register bit. This register bit must be set to 1 by a µC (most likely on repeater module). Both the serializer and deserializer use SHA-1 hash value calculation over the assembled KSV lists. HDCP GMSL links support a maximum 15 receivers (total number including the ones in repeater modules). If the total number of downstream receivers exceeds 14, the µC must set the MAX_DEVS_EXCEEDED register bit when it assembles the KSV list.

Force Video/Force Audio Data

The serializer masks audio and video data through two control bits: FORCE_AUDIO and FORCE_VIDEO. Set FORCE_VIDEO = 1 to transmit the 24-bit data word in the DFORCE register instead of the video data received at the serializer video inputs. Set FORCE_AUDIO = 1 to transmit 0 instead of the SD input (SCK and WS continue to be output from the deserializer). Use these features to blank out the screen and mute the audio.

HDCP Authentication Procedures

The serializer generates a 64-bit random number exceeding the HDCP requirement. The serializer/deserializer internal one-time programmable (OTP) memories contain unique HDCP keyset programmed at the factory. The host μC initiates and controls the HDCP authentication procedure. The serializer and deserializer generate HDCP authentication response values for the verification of authentication. Use the following procedures to authenticate the HDCP-GMSL encryption. Refer to the *HDCP 1.3 Amendment for GMSL* for details. The μC must perform link integrity checks while encryption is enabled. See the *Link Integrity Check* section. Any event that indicates that the deserializer has lost link synchronization should retrigger authentication. The μC must first write 1 to RESET_HDCP bit in the serializer before starting a new authentication attempt.

HDCP Protocol Summary

Tables 15, 16, and 17 list the summaries of the HDCP protocol. These tables serve as an implementation guide only. Meet the requirements in the GMSL amendment for HDCP to be in full compliance.

Table 15. Startup, HDCP Authentication, and Normal Operation (Deserializer is Not a Repeater)—First Part of the HDCP Authentication Protocol

NO.	μC	SERIALIZER	DESERIALIZER
1	Initial state after power-up.	Powers up waiting for HDCP authentication.	Powers up waiting for HDCP authentication.
2	Makes sure that A/V data not requiring protection (low-value content) is available at the serializer inputs (such as blue or informative screen). Alternatively, uses the FORCE_VIDEO and FORCE_AUDIO bits of the serializer to mask A/V data at the input of the serializer. Starts the link by writing SEREN = H or the link starts automatically if $\overline{\text{AUTOS}}$ is low.	—	—
3	—	Starts serialization and transmits low-value content A/V data.	Locks to incoming data stream and outputs low-value content A/V data.
4	Reads the locked bit of the deserializer and ensures that the link is established.	—	—
5	Optionally writes a random-number seed to the serializer.	Combines the seed with an internally generated random number. If no seed is provided, only internal random number is used.	—
6	If HDCP encryption is required, starts authentication by writing 1 to the START_AUTHENTICATION bit of the serializer.	Generates (stores) AN and resets the START_AUTHENTICATION bit to 0.	—
7	Reads AN and AKSV from the serializer and writes to the deserializer.	—	Generates R0’ triggered by the μC’s write of AKSV.

Table 15. Startup, HDCP Authentication, and Normal Operation (Deserializer is not a Repeater)—First Part of the HDCP Authentication Protocol (continued)

NO.	µC	SERIALIZER	DESERIALIZER
8	Reads the BKSV and REPEATER bit from the deserializer and writes to the serializer.	Generates R0, triggered by the µC's write of BKSV.	—
9	Reads the INVALID_BKSV bit of the serializer and continues with authentication if it is 0. Authentication can be restarted if it fails (set RESET_HDCP = 1 before restarting authentication).	—	—
10	Reads R0' from the deserializer and reads R0 from the serializer. If they match, continues with authentication; otherwise, retries up to two more times (optionally, the serializer comparison can be used to detect if R0/R0' match). Authentication can be restarted if it fails (set the RESET_HDCP = 1 before restarting authentication).	—	—
11	Waits for the VSYNC falling edge (internal to the serializer) and then sets the ENCRYPTION_ENABLE bit to 1 in the deserializer and the serializer (if the µC is not able to monitor VSYNC, it can utilize the VSYNC_DET bit in the deserializer).	Encryption is enabled after the next VSYNC falling edge.	Decryption is enabled after the next VSYNC falling edge.
12	Checks that BKSV is not in the Key Revocation list and continues if it is not. Authentication can be restarted if it fails. **Note:** Revocation list check can start after BKSV is read in step 8.	—	—
13	Starts transmission of A/V content that needs protection.	Performs HDCP encryption on high-value content A/V data.	Performs HDCP decryption on high-value content A/V data.

Table 16. Link Integrity Check (Normal)—Performed Every 128 Frames After Encryption is Enabled

NO.	µC	SERIALIZER	DESERIALIZER
1	—	Generates Ri and updates the RI register every 128 VSYNC cycles.	Generates Ri' and updates the RI' register every 128 VSYNC cycles.
2	—	Continues to encrypt and transmit A/V data.	Continues to receive, decrypt, and output A/V data.
3	Every 128 video frames (VSYNC cycles) or every 2s.	—	—
4	Reads RI from the serializer.	—	—
5	Reads RI' from the deserializer.	—	—
6	Reads RI again from the serializer and ensures it is stable (matches the previous RI that it has read from the serializer). If RI is not stable, go back to step 5.	—	—
7	If RI matches RI', link integrity check is successful, go back to step 3.	—	—

Table 16. Link Integrity Check (Normal)—Performed Every 128 Frames After Encryption is Enabled (continued)

NO.	µC	SERIALIZER	DESERIALIZER
8	If RI does not match RI', link integrity check fails. After the detection of failure of link integrity check, the µC ensures that A/V data not requiring protection (low-value content) is available at the serializer inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of the serializer can be used to mask the A/V data input of the serializer.	—	—
9	Writes 0 to the ENCRYPTION_ENABLE bit of the serializer and deserializer.	Disables encryption and transmits low-value content A/V data.	Disables decryption and outputs low-value content A/V data.
10	Restarts authentication by writing 1 to the RESET_HDCP bit followed by writing 1 to the START_AUTHENTICATION bit in the serializer.	—	—

Table 17. Optional Enhanced Link Integrity Check—Performed Every 16 Frames After Encryption is Enabled

NO.	µC	SERIALIZER	DESERIALIZER
1	—	Generates Pj and updates PJ register every 16 VSYNC cycles.	Generates Pj' and updates PJ' register every 16 VSYNC cycles.
2	—	Continues to encrypt and transmit A/V data.	Continues to receive, decrypt, and output A/V data.
3	Every 16 video frames: Reads PJ from the serializer and PJ' from the deserializer.	—	—
4	If PJ matches PJ', the enhanced link integrity check is successful, go back to step 3.	—	—
5	If there is a mismatch, retry up to two more times from step 3. Enhanced link integrity check fails after three mismatches. After the detection of failure of enhanced link integrity check, the µC ensures that the A/V data not requiring protection (low-value content) is available at the serializer inputs (such as blue or informative screen). Alternatively, the FORCE_VIDEO and FORCE_AUDIO bits of the serializer can be used to mask the A/V data input of the serializer.	—	—
6	Writes 0 to the ENCRYPTION_ENABLE bit of the serializer and the deserializer.	Disables encryption and transmits low-value content A/V data.	Disables decryption and outputs low-value content A/V data.
7	Restarts authentication by writing 1 to the RESET_HDCP bit followed by writing 1 to the START_AUTHENTICATION bit in the serializer.	—	—

HDCP Gigabit Multimedia Serial Link Serializer/Deserializer

Example Repeater Network—Two µCs

The following example has one repeater and two µCs (Figure 34). Table 18 summarizes the authentication operation.

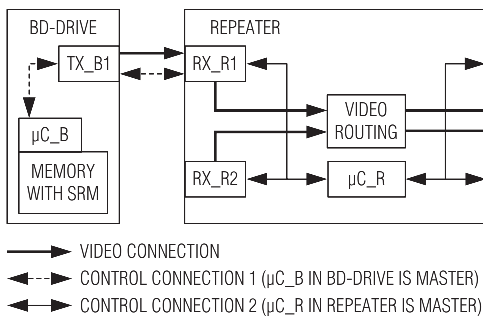

Figure 34. Example Network with One Repeater and Two µCs—TXs are for the Serializer, RXs are for the Deserializer

Table 18. HDCP Authenticaion and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol

NO.	µC_B	µC_R	SERIALIZER (TX_B1, TX_R1, TX_R2)	DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0
1	Initial state after power-up.	Initial state after power-up.	All: Power-up waiting for HDCP authentication.	All: Power-up waiting for HDCP authentication.
2	—	Writes REPEATER = 1 in RX_R1. Retries until proper acknowledge frame is received. **Note:** This step must be completed before the first part of authentication is started between TX_B1 and RX_R1 by µC_B (step 7). To satisfy this requirement, for example: RX_R1 can be held at power-down until µC_R is ready to write the REPEATER bit. Or, the µC_B can poll µC_R before starting authentication.	—	—

Table 18. HDCP Authenticaion and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	SERIALIZER (TX_B1, TX_R1, TX_R2)	DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0
3	Makes sure that the A/V data not requiring protection (low-value content) is available at the TX_B1 inputs (such as blue or informative screen). Alternatively, the FORCE_ VIDEO and FORCE_AUDIO bits of TX_B1 can be used to mask the A/V data input of TX_B1. Starts the link between TX_B1 and RX_R1 by writing SEREN = H to TX_B1, or link starts automatically if $\overline{\text{AUTOS}}$ is low.	—	TX_B1: Starts serialization and transmits low-value content A/V data.	RX_R1: Locks to incoming data stream and outputs low-value content A/V data.
4	—	Starts all downstream links by writing SEREN = H to TX_R1, TX_R2, or links start automatically if $\overline{\text{AUTOS}}$ of transmitters are low.	TX_R1, TX_R2: Starts serialization and transmits low-value content A/V data.	RX_D1, RX_D2: Locks to incoming data stream and outputs low-value content A/V data.
5	Reads the locked bit of RX_R1 and ensures that link between TX_B1 and RX_R1 is established.	Reads the locked bit of RX_D1 and makes sure that link between TX_R1 and RX_D1 is established. Reads the locked bit of RX_D2 and ensures that link between TX_R2 and RX_D2 is established.	—	—
6	Optionally, writes a random-number seed to TX_B1.	Writes 1 to the GPIO_0_FUNCTION and GPIO_1_FUNCTION bits in RX_R1 to change the GPIO functionality to be used for HDCP purpose. Optionally, writes a random-number seed to TX_R1 and TX_R2.	—	—
7	Starts and completes the first part of the authentication protocol between TX_B1, RX_R1. See steps 6–10 in Table 15.	—	TX_B1: According to the commands from µC_B, generates AN, computes R0.	RX_R1: According to the commands from µC_B, computes R0'.
8	—	When GPIO_1 = 1 is detected, starts and completes the first part of the authentication protocol between (TX_R1, RX_D1) and (TX_R2, RX_D2) links. See steps 6–10 in Table 15.	TX_R1, TX_R2: According to the commands from µC_R, generates AN, computes R0.	RX_D1, RX_D2: According to the commands from µC_R, computes R0'.

Table 18. HDCP Authenticaion and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

<table>
<tr><th rowspan="2">NO.</th><th rowspan="2">µC_B</th><th rowspan="2">µC_R</th><th>SERIALIZER (TX_B1, TX_R1, TX_R2)</th><th>DESERIALIZER (RX_R1, RX_D1, RX_D2)</th></tr>
<tr><th>TX_B1 CDS = 0
TX_R1 CDS = 0
TX_R2 CDS = 0</th><th>RX_R1 CDS = 1
RX_D1 CDS = 0
RX_D2 CDS = 0</th></tr>
<tr><td>9</td><td>Waits for the VSYNC falling edge and then enables encryption on the (TX_B1, RX_R1) link. Full authentication is not yet complete, so it ensures that A/V content that needs protection is not transmitted. Since REPEATER = 1 was read from RX_R1, the second part of authentication is required.</td><td>—</td><td>TX_B1: Encryption is enabled after the next VSYNC falling edge.</td><td>RX_R1: Decryption is enabled after the next VSYNC falling edge.</td></tr>
<tr><td>10</td><td>—</td><td>When GPIO_0 = 1 is detected, enables encryption on the (TX_R1, RX_D1) and (TX_R2, RX_D2) links.</td><td>TX_R1, TX_R2: Encryption is enabled after the next VSYNC falling edge.</td><td>RX_D1, RX_D2: Decryption is enabled after the next VSYNC falling edge.</td></tr>
<tr><td>11</td><td rowspan="3">Waits for some time to allow µC_R to make the KSV list ready in RX_R1. Then polls (reads) the KSV_LIST_READY bit of RX_R1 regularly until the proper acknowledge frame is received and the bit is read as 1.</td><td>Blocks the control channel from the µC_B side by setting REVCCEN = FWDCCEN = 0 in RX_R1. Retries until the proper acknowledge frame is received.</td><td>—</td><td>RX_R1: Control channel from the serializer side (TX_B1) is blocked after FWDCCEN = REVCCEN = 0 is written.</td></tr>
<tr><td>12</td><td>Writes BKSVs of RX_D1 and RX_D2 to the KSV list in RX_R1. Then calculates and writes the BINFO register of RX_R1.</td><td>—</td><td>RX_R1: Triggered by µC_R’s write of BINFO, calculates the hash-value, V’, on the KSV list, BINFO, and the secret-value M0’.</td></tr>
<tr><td>13</td><td>Writes 1 to the KSV_LIST_READY bit of RX_R1 and then unblocks the control channel from the µC_B side by setting REVCCEN = FWDCCEN = 1 in RX_R1.</td><td>—</td><td>RX_R1: Control channel from the serializer side (TX_B1) is unblocked after FWDCCEN = REVCCEN = 1 is written.</td></tr>
</table>

Table 18. HDCP Authenticaion and Normal Operation (One Repeater, Two µCs)—First and Second Parts of the HDCP Authentication Protocol (continued)

NO.	µC_B	µC_R	SERIALIZER (TX_B1, TX_R1, TX_R2)	DESERIALIZER (RX_R1, RX_D1, RX_D2)
			TX_B1 CDS = 0 TX_R1 CDS = 0 TX_R2 CDS = 0	RX_R1 CDS = 1 RX_D1 CDS = 0 RX_D2 CDS = 0
14	Reads the KSV list and BINFO from RX_R1 and writes them to TX_B1. If any of the MAX_DEVS_EXCEEDED or MAX_CASCADE_EXCEEDED bits is 1, then authentication fails. **Note:** BINFO must be written after the KSV list.	—	TX_B1: Triggered by µC_B's write of BINFO, calculates hash-value V on the KSV list, BINFO, and the secret-value M0.	—
15	Reads V from TX_B1 and V' from RX_R1. If they match, continues with authentication; otherwise, retries up to two more times.	—	—	—
16	Searches for each KSV in the KSV list and BKSV of RX_R1 in the Key Revocation list.	—	—	—
17	If keys are not revoked, the second part of the authentication protocol is completed.	—	—	—
18	Starts transmission of A/V content that needs protection.	—	All: Perform HDCP encryption on high-value A/V data.	All: Perform HDCP decryption on high-value A/V data.

Detection and Action Upon New Device Connection

When a new device is connected to the system, the device must be authenticated and the device's KSV checked against the revocation list. The downstream µCs can set the NEW_DEV_CONN bit of the upstream receiver and invoke an interrupt to notify upstream µCs.

Notification of Start of Authentication and Enable of Encryption to Downstream Links

HDCP repeaters do not immediately begin authentication upon startup or detection of a new device, but instead wait for an authentication request from the upstream transmitter/repeaters.

Use the following procedure to notify downstream links of the start of a new authentication request:

1) Host µC begins authentication with the HDCP repeater's input receiver.
2) When AKSV is written to HDCP repeater's input receiver, its AUTH_STARTED bit is automatically set and its GPIO1 goes high (if GPIO1_FUNCTION is set to high).
3) HDCP repeater's µC waits for a low to high transition on HDCP repeater input receiver's AUTH_STARTED bit and/or GPIO1 (if configured) and starts authentication downstream.
4) HDCP repeater's µC resets AUTH_STARTED bit.

Set GPIO0_FUNCTION to high to have GPIO0 follow the ENCRYPTION_ENABLE bit of the receiver. The repeater µC can use this function to be notified when encryption is enabled/disabled by an upstream µC.

HDCP Gigabit Multimedia Serial Link Serializer/Deserializer

Applications Information

Error Checking

The deserializer checks the serial link for errors and stores the number of detected decoding errors in the 8-bit register DECERR (0x0D). If a large number of 8b/10b decoding or parity errors are detected within a short duration (error rate ≥ 1/4), the deserializer loses lock and stops the error counter. The deserializer then attempts to relock to the serial data. DECERR resets upon successful video link lock, successful readout of DECERR (through UART), or whenever auto error reset is enabled. The deserializer does not check for decoding or parity errors during the internal PRBS test, and DECERR is reset to 0x00.

$\overline{\text{ERR}}$ Output

The deserializer has an open-drain $\overline{\text{ERR}}$ output. This output asserts low whenever the number of decoding errors exceeds the error threshold ERRTHR (0x0C) during normal operation, or when at least 1 PRBS error is detected during PRBS test. $\overline{\text{ERR}}$ reasserts high whenever DECERR (0x0D) resets, due to DECERR readout, video link lock, or auto error reset.

Auto Error Reset

The default method to reset errors is to read the respective error registers in the deserializer (0x0D, 0x0E). Auto error reset clears the decoding error counter DECERR and the $\overline{\text{ERR}}$ output ~1µs after ERR goes low. Auto error reset is disabled on power-up. Enable auto error reset through AUTORST (0x06, D6). Auto error reset does not run when the device is in PRBS test mode.

PRBS Self-Test

The serializer/deserializer link includes a PRBS pattern generator and bit-error verification function. First, disable the glitch filters (set DISVSFILT, DISHSFILT to 1) in the deserializer. Next, disable VSYNC/HSYNC inversion in both the serializer and deserializer (set INVVSYNC, INVHSYNC to 0). Then, set PRBSEN = 1 (0x04, D5) in the serializer and then the deserializer to start the PRBS test. Set PRBSEN = 0 (0x04, D5) first in the deserializer and then the serializer to exit the PRBS self-test. The deserializer uses an 8-bit register (0x0E) to count the number of detected errors. The control link also controls the start and stop of the error counting. During PRBS mode, the device does not count decoding errors and the deserializer's $\overline{\text{ERR}}$ output reflects PRBS errors only.

Microcontrollers on Both Sides of the GMSL Link (Dual µC Control)

Usually the microcontroller is either on the serializer side for video-display applications or on the deserializer side for image-sensing applications. For the former case, both the CDS pins of the serializer/deserializer are set to low, and for the later case, the CDS pins are set to high. However, if the CDS pin of the serializer is low and the same pin of the deserializer is high, then the serializer/deserializer connect to both µCs simultaneously. In such a case, the µCs on either side can communicate with the serializer and deserializer.

Contentions of the control link can happen if the µCs on both sides are using the link at the same time. The serializer/deserializer do not provide the solution for contention avoidance. The serializer/deserializer do not send an acknowledge frame when communication fails due to contention. Users can always implement a higher layer protocol to avoid the contention. In addition, if UART communication across the serial link is not required, the µCs can disable the forward and reverse control channel through the FWDCCEN and REVCCEN bits (0x04, D[1:0]) in the serializer/deserializer. UART communication across the serial link is stopped and contention between µCs no longer occurs. During dual µCs operation, if one of the CDS pins on either side changes state, the link resumes the corresponding state described in the *Link Startup Procedure* section.

As an example of dual µC use in an image-sensing application, the serializer can be in sleep mode and waiting for wake-up by the deserializer. After wake-up, the serializer-side µC sets the serializer's CDS pin low and assumes master control of the serializer's registers.

HSYNC/VSYNC Glitch Filter

The deserializer contains one-cycle glitch filters on HSYNC and VSYNC. This eliminates single-cycle glitches in HSYNC and VSYNC that can cause a loss of HDCP synchronization between the serializer and deserializer while encryption is enabled. The glitch filters are on by default. Write to D[1:0] of register 0x08 in the deserializer to disable the glitch filters for HSYNC or VSYNC.

The glitch filter, when active, suppresses all single-cycle wide pulses sent. Disable the glitch filter before running PRBS BER tests. The internal BER checker assumes that the incoming bit stream is unaltered PRBS data.

Jitter-Filtering PLL

In some applications, the parallel bus input clock to the serializer (PCLKIN) includes noise, which reduces link reliability. The serializer has a narrowband jitter-filtering PLL to attenuate frequency components outside the PLL's bandwidth (< 100kHz typ). Enable the jitter-filtering PLL by setting DISFPLL = 0 (0x05, D6).

Changing the Clock Frequency

Both the video clock rate ($f_{PCLK\_}$) and the control-channel clock rate (f_{UART}) can be changed on-the-fly to support applications with multiple clock speeds. It is recommended to enable the serial link after the video clock stabilizes. Stop the video clock for 5µs and restart the serial link or toggle SEREN after each change in the video clock frequency to recalibrate any automatic settings if a clean frequency change cannot be guaranteed. The reverse control channel remains unavailable for 350µs after serial link start or stop. Limit on-the-fly changes in f_{UART} to factors of less than 3.5 at a time to ensure that the device recognizes the UART sync pattern. For example, when lowering the UART frequency from 1Mbps to 100kbps, first send data at 333kbps and then at 100kbps to have reduction ratios of 3 and 3.333, respectively.

Do not interrupt PCLKIN or change its frequency while encryption is enabled. Otherwise HDCP synchronization is lost and authentication must be repeated. To change the PCLK frequency, stop the high value content A/V data. Then disable encryption in the serializer/deserializer within the same VSYNC cycle—encryption stops at the next VSYNC falling edge. PCLKIN can now be changed/stopped. Reenable encryption before sending any high value content A/V data.

Fast Detection of Loss-of-Synchronization

A measure of link quality is the recovery time from loss of HDCP synchronization. With the GMSL, it is likely that HDCP synchronization will not be lost unless the GMSL synchronization is lost. The host can be quickly notified of loss-of-lock by connecting the deserializer's LOCK output to the INT input. If other sources use the interrupt input, such as a touch-screen controller, the µC can implement a routine to distinguish between interrupts from loss-of-sync and normal interrupts. Reverse control-channel communication does not require an active forward link to operate and accurately tracks the LOCK status of the GMSL link. LOCK asserts for video link only and not for the configuration link.

Programming the Device Addresses

Both the serializer and the deserializer have programmable device addresses. This allows multiple GMSL devices, along with I^2C peripherals, to coexist on the same control channel. The serializer device address is stored in register 0x00 of each device, while the deserializer device address is stored in register 0x01 of each device. To change the device address, first write to the device whose address changes (register 0x00 of the serializer for serializer device address change, or register 0x01 of the deserializer for deserializer device address change). Then write the same address into the corresponding register on the other device (register 0x00 of the deserializer for serializer device address change, or register 0x01 of the serializer for deserializer device address change).

Configuration Blocking

The serializer/deserializer can block changes to their non-HDCP registers. Set CFGBLOCK to make all non-HDCP registers as read only. Once set, the registers remain blocked until the supplies are removed or until $\overline{\text{PWDN}}$ is low.

Backward Compatibility

The serializer and deserializer are backward compatible with the non-HDCP MAX9259 and MAX9260. The pinouts and packages are the same for both devices. See Table 3 and the *Pin Description* section for backward-compatible pin mapping.

Key Memory

Each device has a unique HDCP key set that is stored in secure on-chip nonvolatile memory (NVM). The HDCP key set consists of forty 56-bit private keys and one 40-bit public key. The NVM is qualified for automotive applications.

GPIOs

The deserializer has two open-drain GPIOs available. When not used for HDCP purposes, GPIO1OUT and GPIO0OUT (0x06, D3 and D1) set the output state of the GPIOs. See the *Notification of Start of Authentication and Enable of Encryption to Downstream Links* section. The GPIO input buffers are always enabled. The input states are stored in GPIO1 and GPIO0 (0x06, D2 and D0). Set GPIO1OUT/GPIO0OUT to 1 when using GPIO1/GPIO0 as an input.

Line-Fault Detection

The line-fault detector in the serializer monitors for line failures such as short to ground, short to battery, and open link for system fault diagnosis. Figure 3 shows the required external resistor connections. $\overline{\text{LFLT}}$ = low when a line fault is detected and $\overline{\text{LFLT}}$ goes high when the line returns to normal. The line-fault type is stored in 0x08, D[3:0] of the serializer. Filter $\overline{\text{LFLT}}$ with the µC to reduce the detector's susceptibility to brief ground shifts. The fault detector threshold voltages are referenced to the serializer ground. Additional passive components set the DC level of the cable (Figure 3). If the serializer and deserializer grounds are different, the link DC voltage during normal operation can vary and cross one of the fault detection thresholds. For the fault detection circuit, select the resistor's power rating to handle a short to the battery.

To detect the short-together case, refer to Application Note 4709: *GMSL line-fault detection*. Table 19 lists the mapping for line-fault types.

Staggered Parallel Data Outputs

The deserializer staggers the parallel data outputs to reduce EMI and noise. Staggering outputs also reduces the power-supply transient requirements. By default, the deserializer staggers outputs according to Table 20. Disable output staggering through the DISSTAG bit (0x06, D7).

Internal Input Pulldowns

The control and configuration inputs on the serializer/deserializer include a pulldown resistor to GND. Pulldowns are disabled when the device is shut down ($\overline{\text{PWDN}}$ = low) or put into sleep mode. Keep all inputs driven or use external pullup/pulldown resistors to prevent additional current consumption and undesired configuration due to undefined inputs.

Choosing I²C/UART Pullup Resistors

Both I²C/UART open-drain lines require pullup resistors to provide a logic-high level. There are tradeoffs between power dissipation and speed, and a compromise made in choosing pullup resistor values. Every device connected to the bus introduces some capacitance even when the device is not in operation. I²C specifies 300ns rise times to go from low to high (30% to 70%) for fast mode, which is defined for data rates up to 400kbps (see the I²C specifications in the *Electrical Characteristics* table for details). To meet the fast-mode rise-time requirement, choose the pullup resistors so that rise time t_R = 0.85 x R_{PULLUP} x C_{BUS} < 300ns. The waveforms are not recognized if the transition time becomes too slow. The serializer/deserializer support I²C/UART rates up to 1Mbps.

Table 19. Serializer Line-Fault Mapping*

REGISTER ADDRESS	BITS	NAME	VALUE	LINE-FAULT TYPE
0x08	D[3:2]	LFNEG	00	Negative cable wire shorted to supply voltage.
			01	Negative cable wire shorted to ground.
			10	Normal operation.
			11	Negative cable wire disconnected.
	D[1:0]	LFPOS	00	Positive cable wire shorted to supply voltage.
			01	Positive cable wire shorted to ground.
			10	Normal operation.
			11	Positive cable wire disconnected.

**For the short-together case, refer to* Application Note 4709: MAX9259 GMSL line-fault detection.

Table 20. Staggered Output Delay

OUTPUT	OUTPUT DELAY RELATIVE TO DOUT0 (ns)	
	DISSTAG = 0	DISSTAG = 1
DOUT0–DOUT5, DOUT21, DOUT22	0	0
DOUT6–DOUT10, DOUT23, DOUT24	0.5	0
DOUT11–DOUT15, DOUT25, DOUT26	1	0
DOUT16–DOUT20, DOUT27, DOUT28	1.5	0
PCLKOUT	0.75	0

AC-Coupling

AC-coupling isolates the receiver from DC voltages up to the voltage rating of the capacitor. Four capacitors—two at the serializer output and two at the deserializer input—are needed for proper link operation and to provide protection if either end of the cable is shorted to a high voltage. AC-coupling blocks low-frequency ground shifts and low-frequency common-mode noise.

Selection of AC-Coupling Capacitors

Voltage droop and the digital sum variation (DSV) of transmitted symbols cause signal transitions to start from different voltage levels. Because the transition time is finite, starting the signal transition from different voltage levels causes timing jitter. The time constant for an AC-coupled link needs to be chosen to reduce droop and jitter to an acceptable level. The RC network for an AC-coupled link consists of the CML receiver termination resistor (R_{TR}), the CML driver termination resistor (R_{TD}), and the series AC-coupling capacitors (C). The RC time constant for four equal-value series capacitors is $(C \times (R_{TD} + R_{TR}))/4$. R_{TD} and R_{TR} are required to match the transmission line impedance (usually 100Ω). This leaves the capacitor selection to change the system time constant. Use at least 0.2µF high-frequency surface-mount ceramic capacitors, with sufficient voltage rating to withstand a short to battery, to pass the lower speed reverse control-channel signal. Use capacitors with a case size less than 3.2mm x 1.6mm to have lower parasitic effects to the high-speed signal.

Power-Supply Circuits and Bypassing

The serializer uses an AVDD and DVDD of 1.7V to 1.9V, while the deserializer uses an AVDD and DVDD of 3.0V to 3.6V. All single-ended inputs and outputs on the serializer/deserializer derive power from an IOVDD of 1.7V to 3.6V, which scale with IOVDD. Proper voltage-supply bypassing is essential for high-frequency circuit stability.

Cables and Connectors

Interconnect for CML typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Twisted-pair and shielded twisted-pair cables tend to generate less EMI due to magnetic-field canceling effects. Balanced cables pick up noise as common-mode rejected by the CML receiver. Table 21 lists the suggested cables and connectors used in the GMSL link.

Table 21. Suggested Connectors and Cables for GMSL

VENDOR	CONNECTOR	CABLE
JAE	MX38-FF	A-BW-Lxxxxx
Nissei	GT11L-2S	F-2WME AWG28
Rosenberger	D4S10A-40ML5-Z	Dacar 538

Board Layout

Separate the digital signals and CML high-speed signals to prevent crosstalk. Use a four-layer PCB with separate layers for power, ground, CML, and digital signals. Layout PCB traces close to each other for a 100Ω differential characteristic impedance. The trace dimensions depend on the type of trace used (microstrip or stripline). Note that two 50Ω PCB traces do not have 100Ω differential impedance when brought close together—the impedance goes down when the traces are brought closer.

Route the PCB traces for a CML channel (there are two conductors per CML channel) in parallel to maintain the differential characteristic impedance. Avoid vias. Keep PCB traces that make up a differential pair equal length to avoid skew within the differential pair.

ESD Protection

The serializer/deserializer ESD tolerance is rated for Human Body Model, IEC 61000-4-2, and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards specify ESD tolerance for electronic systems. The serial link I/O are tested for ISO 10605 ESD protection and IEC 61000-4-2 ESD protection. All pins are tested for the Human Body Model. The Human Body Model discharge components are C_S = 100pF and R_D = 1.5kΩ (Figure 35). The IEC 61000-4-2 discharge components are C_S = 150pF and R_D = 330Ω (Figure 36). The ISO 10605 discharge components are C_S = 330pF and R_D = 2kΩ (Figure 37).

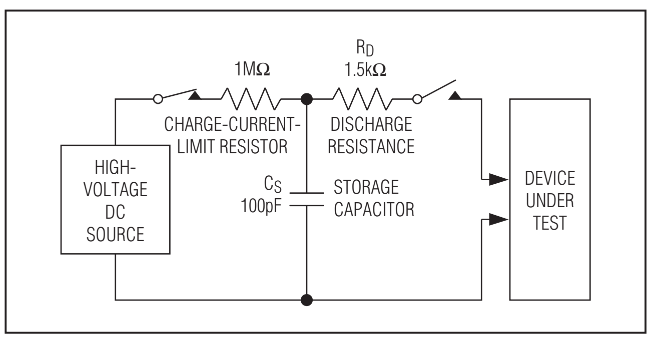

Figure 35. Human Body Model ESD Test Circuit

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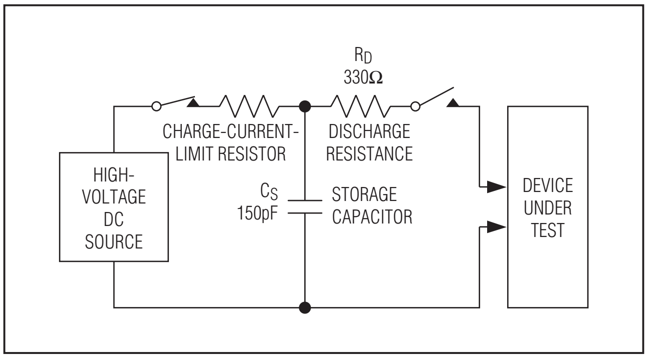

Figure 36. IEC 61000-4-2 Contact Discharge ESD Test Circuit

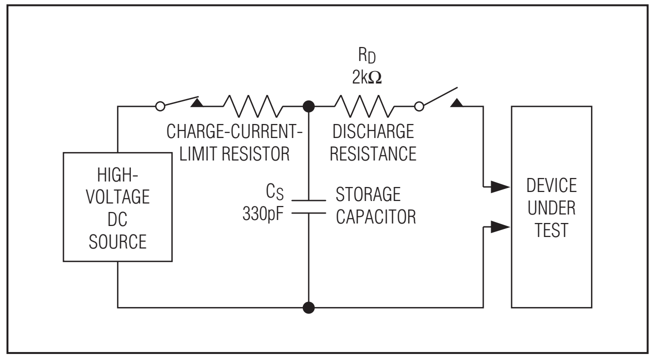

Figure 37. ISO 10605 Contact Discharge ESD Test Circuit

Table 22. Serializer GMSL Core Register Table (See Table 1)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:1]	SERID	XXXXXXX	Serializer device address.	1000000
	D0	CFGBLOCK	0	Normal operation.	0
			1	Registers 0x00 to 0x1F are read only.	
0x01	D[7:1]	DESID	XXXXXXX	Deserializer device address.	1001000
	D0	—	0	Reserved.	0
0x02	D[7:5]	SS	**000**	No spread spectrum. **Power-up default when SSEN = low.**	000, 001
			001	±0.5% spread spectrum. **Power-up default when SSEN = high.**	
			010	±1.5% spread spectrum.	
			011	±2% spread spectrum.	
			100	No spread spectrum.	
			101	±1% spread spectrum.	
			110	±3% spread spectrum.	
			111	±4% spread spectrum.	
	D4	AUDIOEN	0	Disable I^2S channel.	1
			1	Enable I^2S channel.	
	D[3:2]	PRNG	00	12.5MHz to 25MHz pixel clock.	11
			01	25MHz to 50MHz pixel clock.	
			10	50MHz to 104MHz pixel clock.	
			11	Automatically detect the pixel clock range.	
	D[1:0]	SRNG	00	0.5Gbps to 1Gbps serial-bit rate.	11
			01	1Gbps to 2Gbps serial-bit rate.	
			10	2Gbps to 3.125Gbps serial-bit rate.	
			11	Automatically detect serial-bit rate.	

Table 22. Serializer GMSL Core Register Table (See Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x03	D[7:6]	AUTOFM	00	Calibrate spread-modulation rate only once after locking.	00
			01	Calibrate spread-modulation rate every 2ms after locking.	
			10	Calibrate spread-modulation rate every 16ms after locking.	
			11	Calibrate spread-modulation rate every 256ms after locking.	
	D[5:0]	SDIV	000000	Autocalibrate sawtooth divider.	000000
			XXXXXX	Manual SDIV setting. See the *Manual Programming of Spread-Spectrum Divider* section.	
0x04	D7	SEREN	**0**	Disable serial link. **Power-up default when $\overline{\text{AUTOS}}$ = high.** Reverse control-channel communication remains unavailable for 350µs after the serializer starts/stops the serial link.	0, 1
			1	Enable serial link. **Power-up default when $\overline{\text{AUTOS}}$ = low.** Reverse control-channel communication remains unavailable for 350µs after the serializer starts/stops the serial link.	
	D6	CLINKEN	0	Disable configuration link.	0
			1	Enable configuration link.	
	D5	PRBSEN	0	Disable PRBS test.	0
			1	Enable PRBS test.	
	D4	SLEEP	0	Normal mode (default value depends on CDS and $\overline{\text{AUTOS}}$ pin values at power-up).	0, 1
			1	Activate sleep mode (default value depends on CDS and $\overline{\text{AUTOS}}$ pin values at power-up).	
	D[3:2]	INTTYPE	00	Base mode uses I^2C peripheral interface.	00
			01	Base mode uses UART peripheral interface.	
			10, 11	Base mode peripheral interface disabled.	
	D1	REVCCEN	0	Disable reverse control channel from deserializer (receiving).	1
			1	Enable reverse control channel from deserializer (receiving).	
	D0	FWDCCEN	0	Disable forward control channel to deserializer (sending).	1
			1	Enable forward control channel to deserializer (sending).	

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Table 22. Serializer GMSL Core Register Table (See Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x05	D7	I2CMETHOD	0	I2C conversion sends the register address.	0
			1	Disable sending of I2C register address (command-byte-only mode).	
	D6	DISFPLL	0	Filter PLL active.	1
			1	Filter PLL disabled.	
	D[5:4]	CMLLVL	00	Do not use.	11
			01	200mV CML signal level.	
			10	300mV CML signal level.	
			11	400mV CML signal level.	
	D[3:0]	PREEMP	0000	Preemphasis off.	0000
			0001	-1.2dB preemphasis.	
			0010	-2.5dB preemphasis.	
			0011	-4.1dB preemphasis.	
			0100	-6.0dB preemphasis.	
			0101	Do not use.	
			0110	Do not use.	
			0111	Do not use.	
			1000	1.1dB preemphasis.	
			1001	2.2dB preemphasis.	
			1010	3.3dB preemphasis.	
			1011	4.4dB preemphasis.	
			1100	6.0dB preemphasis.	
			1101	8.0dB preemphasis.	
			1110	10.5dB preemphasis.	
			1111	14.0dB preemphasis.	
0x06	D[7:0]	—	01000000	Reserved.	01000000
0x07	D[7:0]	—	00100010	Reserved.	00100010
0x08	D[7:4]	—	0000	Reserved.	0000 (read only)
	D[3:2]	LFNEG	00	Negative cable wire shorted to supply voltage.	10 (read only)
			01	Negative cable wire shorted to ground.	
			10	Normal operation.	
			11	Negative cable wire disconnected.	
	D[1:0]	LFPOS	00	Positive cable wire shorted to supply voltage.	10 (read only)
			01	Positive cable wire shorted to ground.	
			10	Normal operation.	
			11	Positive cable wire disconnected.	
0x0C	D[7:0]	—	01110000	Reserved.	01110000

Table 22. Serializer GMSL Core Register Table (See Table 1) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x0D	D7	SETINT	0	Set INT low when SETINT transitions from 1 to 0.	0
			1	Set INT high when SETINT transitions from 0 to 1.	
	D6	INVVSYNC	0	Serializer does not invert DIN19/VS.	0
			1	Serializer inverts DIN19/VS.	
	D5	INVHSYNC	0	Serializer does not invert DIN18/HS.	0
			1	Serializer inverts DIN18/HS.	
	D[4:0]	—	00000	Reserved.	00000
0x1E	D[7:0]	ID	00000101	Device identifier (MAX9263 = 0x05).	00000101 (read only)
0x1F	D[7:5]	—	000	Reserved.	000 (read only)
	D4	CAPS	0	Not HDCP capable.	1 (read only)
			1	HDCP capable.	
	D[3:0]	REVISION	XXXX	Device revision.	(read only)

Table 23. Deserializer GMSL Core Register Table (See Table 2)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x00	D[7:1]	SERID	XXXXXXX	Serializer device address.	1000000
	D0	—	0	Reserved.	0
0x01	D[7:1]	DESID	XXXXXXX	Deserializer device address.	1001000
	D0	CFGBLOCK	0	Normal operation.	0
			1	Registers 0x00 to 0x1F are read only.	
0x02	D[7:6]	SS	**00**	No spread spectrum. **Power-up default when SSEN = low.**	00, 01
			01	±2% spread spectrum. **Power-up default when SSEN = high.**	
			10	No spread spectrum.	
			11	±4% spread spectrum.	
	D5	—	0	Reserved.	0
	D4	AUDIOEN	0	Disable I²S channel.	1
			1	Enable I²S channel.	
	D[3:2]	PRNG	00	12.5MHz to 25MHz pixel clock.	11
			01	25MHz to 50MHz pixel clock.	
			10	50MHz to 104MHz pixel clock.	
			11	Automatically detect the pixel clock range.	
	D[1:0]	SRNG	00	0.5Gbps to 1Gbps serial-data rate.	11
			01	1Gbps to 2Gbps serial-data rate.	
			10	2Gbps to 3.125Gbps serial-data rate.	
			11	Automatically detect serial-data rate.	

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Table 23. Deserializer GMSL Core Register Table (See Table 2) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x03	D[7:6]	AUTOFM	00	Calibrate spread-modulation rate only once after locking.	00
			01	Calibrate spread-modulation rate every 2ms after locking.	
			10	Calibrate spread-modulation rate every 16ms after locking.	
			11	Calibrate spread-modulation rate every 256ms after locking.	
	D5	—	0	Reserved.	0
	D[4:0]	SDIV	00000	Autocalibrate sawtooth divider.	00000
			XXXXX	Manual SDIV setting. See the *Manual Programming of Spread-Spectrum Divider* section.	
0x04	D7	LOCKED	0	LOCK output is low.	0 (read only)
			1	LOCK output is high.	
	D6	OUTENB	0	Enable outputs.	0
			1	Disable outputs.	
	D5	PRBSEN	0	Disable PRBS test.	0
			1	Enable PRBS test.	
	D4	SLEEP	0	Normal mode. Default value depends on CDS and MS pin values at power-up.	0, 1
			1	Activate sleep mode. Default value depends on CDS and MS pin values at power-up.	
	D[3:2]	INTTYPE	00	Base mode uses I^2C peripheral interface.	00
			01	Base mode uses UART peripheral interface.	
			10, 11	Base mode peripheral interface disabled.	
	D1	REVCCEN	0	Disable reverse control channel to serializer (sending).	1
			1	Enable reverse control channel to serializer (sending).	
	D0	FWDCCEN	0	Disable forward control channel from serializer (receiving).	1
			1	Enable forward control channel from serializer (receiving).	

Table 23. Deserializer GMSL Core Register Table (See Table 2) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x05	D7	I2CMETHOD	0	I^2C conversion sends the register address.	0
			1	Disable sending of I^2C register address (command-byte-only mode).	
	D[6:5]	HPFTUNE	00	7.5MHz equalizer highpass cutoff frequency.	01
			01	3.75MHz cutoff frequency.	
			10	2.5MHz cutoff frequency.	
			11	1.87MHz cutoff frequency.	
	D4	PDHF	0	High-frequency boosting enabled.	0
			1	High-frequency boosting disabled.	
	D[3:0]	EQTUNE	0000	2.1dB equalizer boost gain.	0100, 1001
			0001	2.8dB equalizer boost gain.	
			0010	3.4dB equalizer boost gain.	
			0011	4.2dB equalizer boost gain.	
			0100	5.2dB equalizer boost gain. **Power-up default when EQS = high.**	
			0101	6.2dB equalizer boost gain.	
			0110	7dB equalizer boost gain.	
			0111	8.2dB equalizer boost gain.	
			1000	9.4dB equalizer boost gain.	
			1001	10.7dB equalizer boost gain. **Power-up default when EQS = low.**	
			1010	11.7dB equalizer boost gain.	
			1011	13dB equalizer boost gain.	
			11XX	Do not use.	
0x06	D7	DISSTAG	0	Enable staggered outputs.	0
			1	Disable staggered outputs.	
	D7	—	0	Reserved.	0
	D6	AUTORST	0	Do not automatically reset error registers and outputs.	0
			1	Automatically reset error registers and outputs.	
	D5	DISINT	0	Enable interrupt transmission to serializer.	0
			1	Disable interrupt transmission to serializer.	
	D4	INT	0	INT input = low (read only).	0 (read only)
			1	INT input = high (read only).	
	D3	GPIO1OUT	0	Output low to GPIO1.	1
			1	Output high to GPIO1.	
	D2	GPIO1	0	GPIO1 is low.	1 (read only)
			1	GPIO1 is high.	
	D1	GPIO0OUT	0	Output low to GPIO0.	1
			1	Output high to GPIO0.	
	D0	GPIO0	0	GPIO0 is low.	1 (read only)
			1	GPIO0 is high.	

Table 23. Deserializer GMSL Core Register Table (See Table 2) (continued)

REGISTER ADDRESS	BITS	NAME	VALUE	FUNCTION	DEFAULT VALUE
0x07	D[7:0]	—	01010100	Reserved.	01010100
0x08	D[7:2]	—	001100	Reserved.	001100
	D1	DISVSFILT	0	VSYNC glitch filter active.	0
			1	VSYNC glitch filter disabled.	
	D0	DISHSFILT	0	HSYNC glitch filter active.	0
			1	HSYNC glitch filter disabled.	
0x09	D[7:0]	—	11001000	Reserved.	11001000
0x0A	D[7:0]	—	00010010	Reserved.	00010010
0x0B	D[7:0]	—	00100000	Reserved.	00100000
0x0C	D[7:0]	ERRTHR	XXXXXXXX	Error threshold for decoding errors. $\overline{ERR}$ = low when DECERR > ERRTHR.	00000000
0x0D	D[7:0]	DECERR	XXXXXXXX	Decoding error counter. This counter remains zero while the device is in PRBS test mode.	00000000 (read only)
0x0E	D[7:0]	PRBSERR	XXXXXXXX	PRBS error counter.	00000000 (read only)
0x12	D7	MCLKSRC	0	MCLK derived from PCLK. See Table 5.	0
			1	MCLK derived from internal oscillator.	
	D[6:0]	MCLKDIV	0000000	MCLK disabled.	0000000
			XXXXXXX	MCLK divider.	
0x13	D[7:0]	—	00010000	Reserved.	00010000
0x14	D7	INVVSYNC	0	Deserializer does not invert DOUT19/VS.	0
			1	Deserializer inverts DOUT19/VS.	
	D6	INVHSYNC	0	Deserializer does not invert DOUT18/HS.	0
			1	Deserializer inverts DOUT18/HS.	
	D[5:0]	—	001001	Reserved.	001001
0x1E	D[7:0]	ID	00000110	Device identifier (MAX9264 = 0x06).	00000110 (read only)
0x1F	D[7:5]	—	000	Reserved.	000 (read only)
	D4	CAPS	0	Not HDCP capable.	1 (read only)
			1	HDCP capable.	
	D[3:0]	REVISION	XXXX	Device revision.	(read only)

X = Don't care.

Table 24. Serializer HDCP Register Table (See Table 1)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/WRITE	FUNCTION	DEFAULT VALUE (hex)
0x80 to 0x84	5	BKSV	Read/write	HDCP receiver KSV	0x0000000000
0x85 to 0x86	2	RI/RI’	Read/write	RI (read only) of the transmitter when EN_INT_COMP = 0 RI’ (read/write) of the receiver when EN_INT_COMP = 1	0x0000
0x87	1	PJ/PJ’	Read/write	PJ (read only) of the transmitter when EN_INT_COMP = 0 PJ’ (read/write) of the receiver when EN_INT_COMP = 1	0x00
0x88 to 0x8F	8	AN	Read only	Session random number	(Read only)
0x90 to 0x94	5	AKSV	Read only	HDCP transmitter KSV	(Read only)
0x95	1	ACTRL	Read/write	D7 = PD_HDCP 1 = Power down HDCP circuits 0 = HDCP circuits normal	0x00
				D6 = EN_INT_COMP 1 = Internal comparison mode 0 = µC comparison mode	
				D5 = FORCE_AUDIO 1 = Force audio data to 0 0 = Normal operation	
				D4 = FORCE_VIDEO 1 = Force video data DFORCE value 0 = Normal operation	
				D3 = RESET_HDCP 1 = Reset HDCP circuits, automatically set to 0 upon completion 0 = Normal operation	
				D2 = START_AUTHENTICATION 1 = Start authentication, automatically set to 0 once authentication starts 0 = Normal operation	
				D1 = VSYNC_DET 1 = Internal falling edge on DIN19/VS detected 0 = No falling edge detected	
				D0 = ENCRYPTION_ENABLE 1 = Enable encryption 0 = Disable encryption	

Table 24. Serializer HDCP Register Table (See Table 1) (continued)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0x96	1	ASTATUS	Read only	D[7:4] = Reserved	0x00 (read only)
				D3 = V_MATCHED 1 = V matches V' (when EN_INT_COMP = 1) 0 = V does not match V' or EN_INT_COMP = 0	
				D2 = PJ_MATCHED 1 = PJ matches PJ' (when EN_INT_COMP = 1) 0 = PJ does not match PJ' or EN_INT_COMP = 0	
				D1 = R0_RI_MATCHED 1 = RI matches RI' (when EN_INT_COMP = 1) 0 = RI does not match RI' or EN_INT_COMP = 0	
				D0 = BKSV_INVALID 1 = BKSV is not valid 0 = BKSV is valid	
0x97	1	BCAPS	Read/write	D[7:1] = Reserved	0x00
				D0 = REPEATER 1 = Set to 1 if device is a repeater 0 = Set to 0 if device is not a repeater	
0x98 to 0x9C	5	ASEED	Read/write	Internal random-number generator optional seed value	0x0000000000
0x9D to 0x9F	3	DFORCE	Read/write	Forced video data transmitted when FORCE_VIDEO = 1 R[7:0] = DFORCE[7:0] G[7:0] = DFORCE[15:8] B[7:0] = DFORCE[23:16]	0x000000
0xA0 to 0xA3	4	V.H0, V'.H0	Read/write	H0 part of SHA-1 hash value V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xA4 to 0xA7	4	V.H1, V'.H1	Read/write	H1 part of SHA-1 hash value V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xA8 to 0xAB	4	V.H2, V'.H2	Read/write	H2 part of SHA-1 hash value V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xAC to 0xAF	4	V.H3, V'.H3	Read/write	H3 part of SHA-1 hash value V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000

Table 24. Serializer HDCP Register Table (See Table 1) (continued)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0xB0 to 0xB3	4	V.H4, V'.H4	Read/write	H4 part of SHA-1 hash value V (read only) of the transmitter when EN_INT_COMP = 0 V' (read/write) of the receiver when EN_INT_COMP = 1	0x00000000
0xB4 to 0xB5	2	BINFO	Read/write	D[15:12] = Reserved D11 = MAX_CASCADE_EXCEEDED 1 = Set to 1 if more than 7 cascaded devices attached 0 = Set to 0 if 7 or fewer cascaded devices attached D[10:8] = DEPTH Depth of cascaded devices D7 = MAX_DEVS_EXCEEDED 1 = Set to 1 if more than 14 devices attached 0 = Set to 0 if 14 or fewer devices attached D[6:0] = DEVICE_COUNT Number of devices attached	0x0000
0xB6	1	GPMEM	Read/write	General-purpose memory byte	0x00
0xB7 to 0xB9	3	—	Read only	Reserved	0x000000
0xBA to 0xFF	70	KSV_LIST	Read/write	List of KSV's downstream repeaters and receivers (maximum of 14 devices)	All zero

Table 25. Deserializer HDCP Register Table (See Table 2)

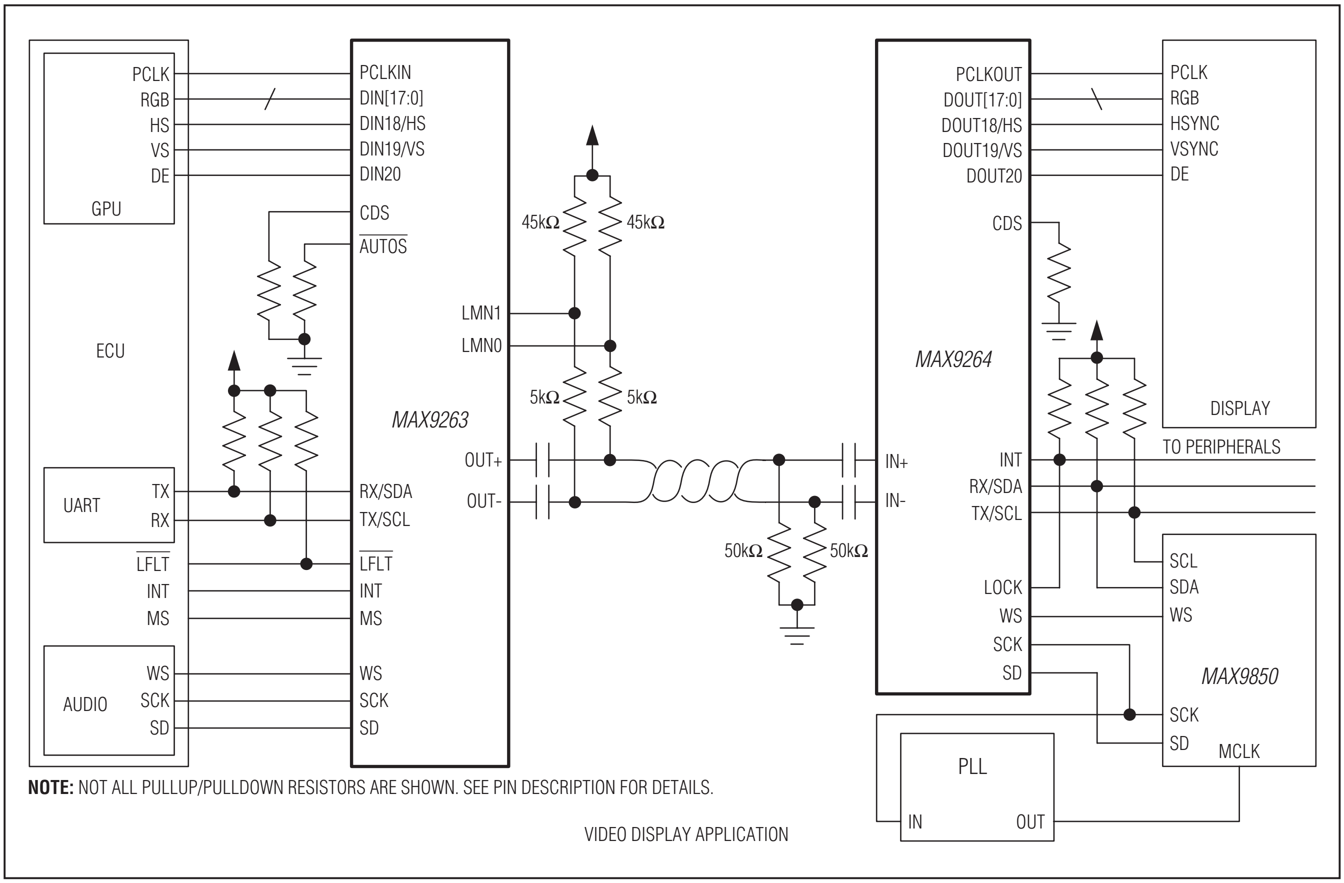
REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0x80 to 0x84	5	BKSV	Read only	HDCP receiver KSV	(Read only)
0x85 to 0x86	2	RI’	Read only	Link verification response	(Read only)
0x87	1	PJ’	Read only	Enhanced link verification response	(Read only)
0x88 to 0x8F	8	AN	Read/write	Session random number	0x0000000000000000
0x90 to 0x94	5	AKSV	Read/write	HDCP transmitter KSV	0x0000000000
0x95	1	BCTRL	Read/write	D7 = PD_HDCP 1 = Power down HDCP circuits 0 = HDCP circuits normal	0x00
				D[6:4] = Reserved	
				D3 = GPIO1_FUNCTION 1 = GPIO1 mirrors AUTH_STARTED 0 = Normal GPIO1 operation	
				D2 = GPIO0_FUNCTION 1 = GPIO0 mirrors ENCRYPTION_ENABLE 0 = Normal GPIO0 operation	
				D1 = AUTH_STARTED 1 = Authentication started (triggered by write to AKSV) 0 = Authentication not started	
				D0 = ENCRYPTION_ENABLE 1 = Enable encryption 0 = Disable encryption	
0x96	1	BSTATUS	Read/write	D[7:2] = Reserved	0x00
				D1 = NEW_DEV_CONN 1 = Set to 1 if a new connected device is detected 0 = Set to 0 if no new device is connected	
				D0 = KSV_LIST_READY 1 = Set to 1 if KSV list and BINFO is ready 0 = Set to 0 if KSV list or BINFO is not ready	
0x97	1	BCAPS	Read/write	D[7:1] = Reserved	0x00
				D0 = REPEATER 1 = Set to 1 if device is a repeater 0 = Set to 0 if device is not a repeater	
0x98 to 0x9F	8	—	Read only	Reserved	0x0000000000000000 (read only)
0xA0 to 0xA3	4	V’.H0	Read/write	H0 part of SHA-1 hash value	0x00000000
0xA4 to 0xA7	4	V’.H1	Read/write	H1 part of SHA-1 hash value	0x00000000
0xA8 to 0xAB	4	V’.H2	Read/write	H2 part of SHA-1 hash value	0x00000000
0xAC to 0xAF	4	V’.H3	Read/write	H3 part of SHA-1 hash value	0x00000000
0xB0 to 0xB3	4	V’.H4	Read/write	H4 part of SHA-1 hash value	0x00000000

Table 25. Deserializer HDCP Register Table (See Table 2) (continued)

REGISTER ADDRESS	SIZE (Bytes)	NAME	READ/ WRITE	FUNCTION	DEFAULT VALUE (hex)
0xB4 to 0xB5	2	BINFO	Read/write	D[15:12] = Reserved	0x0000
				D11 = MAX_CASCADE_EXCEEDED 1 = Set to 1 if more than 7 cascaded devices attached 0 = Set to 0 if 7 or fewer cascaded devices attached	
				D[10:8] = DEPTH Depth of cascaded devices	
				D7 = MAX_DEVS_EXCEEDED 1 = Set to 1 if more than 14 devices attached 0 = Set to 0 if 14 or fewer devices attached	
				D[6:0] = DEVICE_COUNT Number of devices attached	
0xB6	1	GPMEM	Read/write	General-purpose memory byte	0x00
0xB7 to 0xB9	3	—	Read only	Reserved	0x000000
0xBA to 0xFF	70	KSV_LIST	Read/write	List of KSV's downstream repeaters and receivers (maximum of 14 devices)	All zero

HDCP Gigabit Multimedia Serial Link Serializer/Deserializer

Typical Application Circuit



Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
64 TQFP-EP	C64E+10	21-0084	90-0329

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—
1	3/11	Updated the MAX9263 SCK and WS pin descriptions	14

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