

2.488Gbps 1:4 Demultiplexer with Clock and Data Recovery and Limiting Amplifier

General Description

The MAX3882A is a deserializer combined with clock and data recovery and limiting amplifier ideal for converting 2.488Gbps serial data to 4-bit-wide, 622Mbps parallel data for SDH/SONET applications. The device accepts serial NRZ input data as low as 10mV_{p-p} of 2.488Gbps and generates four parallel LVDS data outputs at 622Mbps. Included is an additional high-speed serial data input for system loopback diagnostic testing. For data acquisition, the MAX3882A does not require an external reference clock. However, if needed, the loopback input can be connected to an external reference clock of 155MHz or 622MHz to maintain a valid clock output in the absence of input data transitions. Additionally, a TTL-compatible loss-of-lock output is provided. The device provides a vertical threshold adjustment to compensate for optical noise generated by EDFAs in WDM transmission systems. The MAX3882A operates from a single +3.3V supply and consumes 610mW.

The MAX3882A's jitter performance exceeds all SDH/SONET specifications. The device is available in a 6mm x 6mm, 36-pin TQFN package.

Applications

SDH/SONET Receivers and Regenerators
 Add/Drop Multiplexers
 Digital Cross-Connects
 SDH/SONET Test Equipment
 DWDM Transmission Systems

Typical Application Circuits appear at end of data sheet.

Features

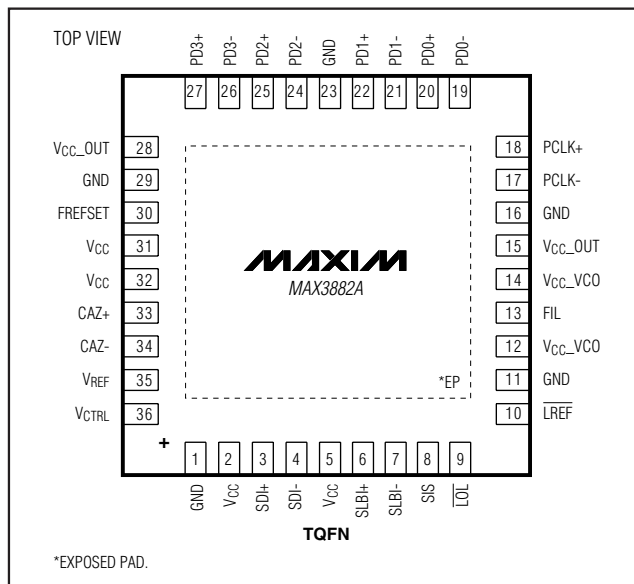
- ◆ No Reference Clock Required for Data Acquisition
- ◆ Serial Input Rate: 2.488Gbps
- ◆ Fully Integrated Clock and Data Recovery with Limiting Amplifier and 1:4 Demultiplexer
- ◆ Parallel Output Rate: 622Mbps
- ◆ Differential Input Range: 10mV_{p-p} to 1.6V_{p-p} without Threshold Adjust
- ◆ Differential Input Range: 50mV_{p-p} to 600mV_{p-p} with Threshold Adjust
- ◆ 0.65UI High-Frequency Jitter Tolerance
- ◆ Loss-of-Lock (LOL) Indicator
- ◆ Wide Input Threshold Adjust Range: ±170mV
- ◆ Maintain Valid Clock Output in Absence of Data Transitions
- ◆ System Loopback Input Available for System Diagnostic Testing
- ◆ Operating Temperature Range -40°C to +85°C
- ◆ Low Power Dissipation: 610mW at +3.3V

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3882AETX+	-40°C to +85°C	36 TQFN-EP*

+ Denotes a lead(Pb)-free/RoHS-compliant package.
 *EP = Exposed pad.

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} -0.5 to +5.0V
 Input Voltage Levels
 (SDI+, SDI-, SLBI+, SLBI-) ($V_{CC} - 1.0V$) to ($V_{CC} + 0.5V$)
 Input Current Levels (SDI+, SDI-, SLBI+, SLBI-) $\pm 20mA$
 LVDS Output Voltage Levels
 (PCLK \pm , PD \pm) -0.5V to ($V_{CC} + 0.5V$)
 Voltage at LOL, SIS, LREF, VREF, FIL, CAZ+,
 CAZ-, VCTRL, FREFSET -0.5V to ($V_{CC} + 0.5V$)

Continuous Power Dissipation ($T_A = +70^\circ C$)
 36-Pin TQFN (derate 35.7mW/ $^\circ C$ above $+70^\circ C$) 2856mW
 Operating Temperature Range $-40^\circ C$ to $+85^\circ C$
 Storage Temperature Range $-55^\circ C$ to $+150^\circ C$
 Lead Temperature (soldering, 10s) $+300^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0$ to $+3.6V$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $+3.3V$ and at $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}			185	230	mA
Single-Ended Input Voltage Range	V_{IS}	Figure 1	$V_{CC} - 0.8$		$V_{CC} + 0.4$	V
Input Common-Mode Voltage Range		Figure 1	$V_{CC} - 0.4$		V_{CC}	V
Input Termination to V_{CC}	R_{IN}		42.5	50	57.5	Ω
Differential Input Voltage Range with Threshold Adjust Enabled SDI+, SDI-		Figure 2	100		600	mV _{P-P}
Threshold Adjustment Range	V_{TH}	Figure 2	-170		+170	mV
Threshold-Control Voltage	V_{CTRL}	(Note 2)	0.302		2.097	V
Threshold-Control Linearity				± 5		%
Threshold Setting Accuracy		Figure 2	-18		+18	mV
Threshold Setting Stability		$15mV \leq V_{TH} \leq 80mV$	-6		+6	mV
		$80mV < V_{TH} \leq 170mV$	-12		+12	
V_{REF} Voltage Output		$R_L = 50k\Omega$	2.14	2.2	2.24	V
LVDS Output High Voltage	V_{OH}				1.475	V
LVDS Output Low Voltage	V_{OL}		0.925			V
LVDS Differential Output Voltage	$ V_{ODI} $		250		400	mV
LVDS Change in Magnitude of Differential Output Voltage for Complementary States	$\Delta V_{ODI} $				25	mV
LVDS Offset Output Voltage			1.125		1.275	V
LVDS Change in Magnitude of Output Offset Voltage for Complementary States	$\Delta V_{OSI} $				25	mV

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +3.0$ to $+3.6V$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $+3.3V$ and at $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS Differential Output Impedance			80		120	Ω
LVDS Output Current		Short together or short to GND			12	mA
LVTTTL Input High Voltage	V_{IH}		2.0			V
LVTTTL Input Low Voltage	V_{IL}				0.8	V
LVTTTL Input Current			-10		+10	μA
LVTTTL Output High Voltage	V_{OH}	$I_{OH} = +20\mu A$	2.4			V
LVTTTL Output Low Voltage	V_{OL}	$I_{OL} = -1mA$			0.4	V

Note 1: At $-40^\circ C$, DC characteristics are guaranteed by design and characterization.

Note 2: Voltage applied to V_{CTRL} pin is from 0.302V to 2.097V when input threshold is adjusted from +170mV to -170mV.

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.0$ to $+3.6V$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $+3.3V$ and at $T_A = +25^\circ C$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Input Data Rate				2.488		Gbps
Differential Input Voltage Threshold Adjust Disabled SDI+, SDI-	V_{ID}	(Note 4) Figure 1	10		1600	mV _{P-P}
Differential Input Voltage SLBI+, SLBI-			50		800	mV _{P-P}
Jitter Peaking	J_P	$f \leq 2MHz$			0.1	dB
Jitter Transfer Bandwidth	J_{BW}			1.7	2.0	MHz
Sinusoidal Jitter Tolerance		$f = 100kHz$	3.1	4.1		UI _{P-P}
		$f = 1MHz$	0.62	1.0		
		$f = 10MHz$	0.44	0.6		
Sinusoidal Jitter Tolerance with Threshold Adjust Enabled (Note 5)		$f = 100kHz$		4.1		UI _{P-P}
		$f = 1MHz$		0.75		
		$f = 10MHz$		0.41		
Jitter Generation	J_{GEN}	(Note 6)		2.7		psRMS
Differential Input Return Loss	$20\log S_{11} $	100kHz to 2.5GHz		17		dB
		2.5GHz to 4.0GHz		15		
Tolerated Consecutive Identical Digits		BER = 10^{-10}		2000		Bits
Acquisition Time (Note 7) Figure 4		0011 pattern		0.6		ms
		PRBS 223 - 1 pattern		0.62	1.5	
\overline{LOL} Assert Time		Figure 4	2.3		100.0	μs
Low-Frequency Cutoff for DC Offset Cancellation Loop		CAZ = $0.1\mu F$		4		kHz

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AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +3.0$ to $+3.6V$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are at $+3.3V$ and at $T_A = +25^\circ C$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Clock Frequency		FREFSET = V_{CC}		155		MHz
		FREFSET = GND		622		
Reference Clock Accuracy				± 100		ppm
VCO Frequency Drift		(Note 8)		400		ppm
Data Output Rate				622		Mbps
Clock Output Frequency				622		MHz
Output Clock-to-Data Delay	t_{CK-Q}	(Note 9)	-80		+80	ps
Clock Output Duty Cycle			45	50	55	%
Clock and Data Output Rise/Fall Time	t_R, t_F	20% to 80%	100		250	ps
LVDS Differential Skew	t_{SKEW1}	Any differential pair			50	ps
LVDS Channel-to-Channel Skew	t_{SKEW2}	PD_{\pm}			100	ps

Note 3: AC characteristics are guaranteed by design and characterization.

Note 4: Jitter tolerance is guaranteed ($BER \leq 10^{-10}$) within this input voltage range. Input threshold adjust is disabled when V_{CTRL} is connected to V_{CC} .

Note 5: Measured with the input amplitude set at 100mV_{p-p} differential swing with a 20mV offset and an input edge speed of 145ps (4th-order Bessel filter with $f_{3dB} = 1.8GHz$).

Note 6: Measured with 10mV_{p-p} OC-48 differential input with PRBS $2^{23} - 1$ and BW = 12kHz to 20MHz.

Note 7: Measured at OC-48 data rate using a 0.068 μF loop-filter capacitor.

Note 8: Under LOL condition, the CDR clock output is set by the external reference clock.

Note 9: Relative to the falling edge of PCLK+. See Figure 3.

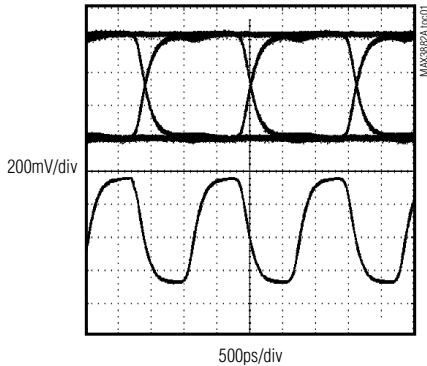
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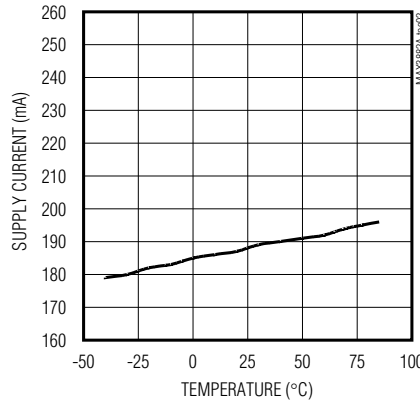
Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

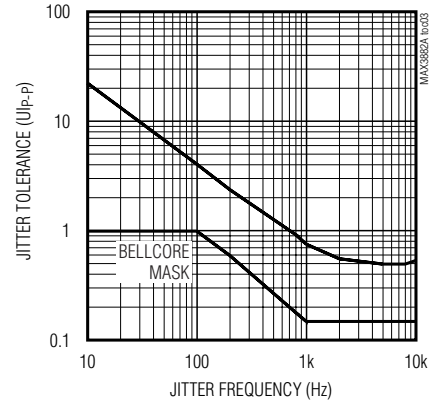
RECOVERED CLOCK AND DATA
(INPUT = 2.488Gbps, $2^{23} - 1$ PATTERN, $V_{IN} = 10\text{mV}_{P-P}$)



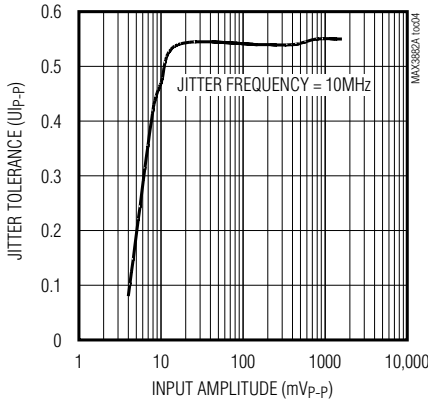
SUPPLY CURRENT vs. TEMPERATURE



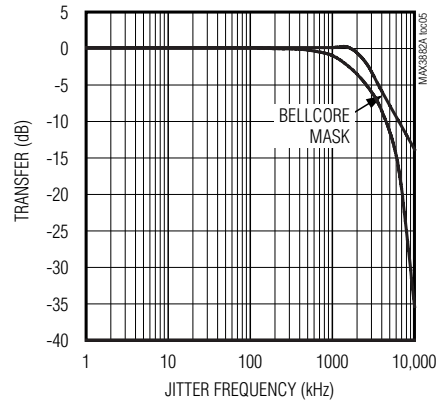
JITTER TOLERANCE
(2.48832Gbps, $2^{23} - 1$ PATTERN, $V_{IN} = 16\text{mV}_{P-P}$ WITH ADDITIONAL 0.15UI DETERMINISTIC JITTER)



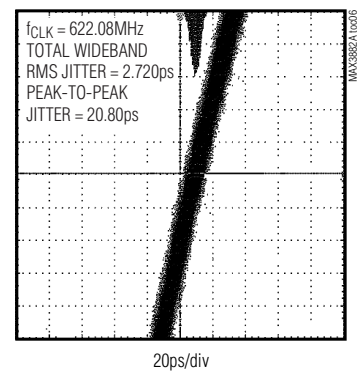
JITTER TOLERANCE vs. INPUT AMPLITUDE
(2.48832Gbps, $2^{23} - 1$ PATTERN, WITH ADDITIONAL 0.15UI DETERMINISTIC JITTER)



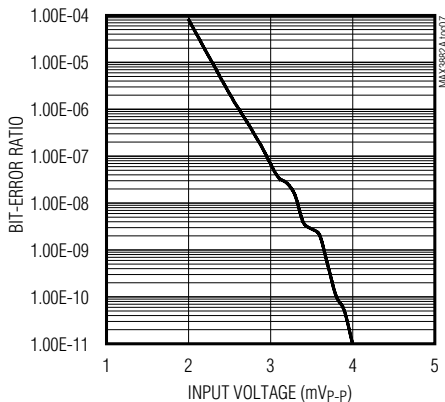
JITTER TRANSFER



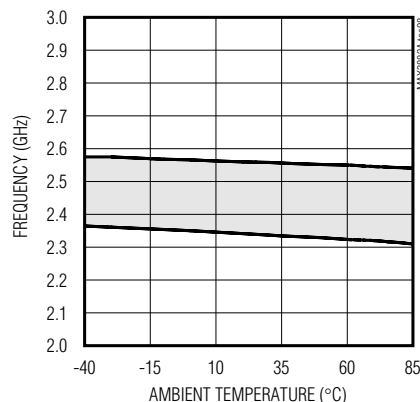
PARALLEL CLOCK OUTPUT JITTER



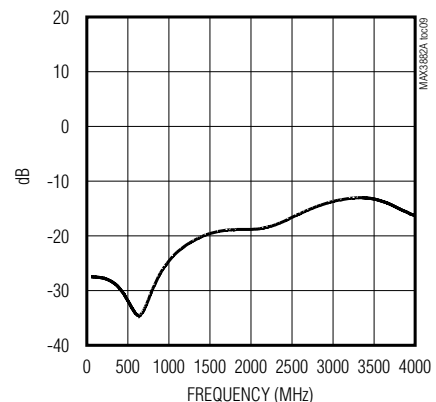
BIT-ERROR RATE vs. INPUT AMPLITUDE



PULLIN RANGE



S11



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Pin Description

PIN	NAME	FUNCTION
1, 11, 16, 23, 29	GND	Supply Ground
2, 5, 31, 32	V _{CC}	+3.3V Supply Voltage
3	SDI+	Positive Data Input. 2.488Gbps serial data stream, CML.
4	SDI-	Negative Data Input. 2.488Gbps serial data stream, CML.
6	SLBI+	Positive System Loopback Input or Positive Reference Clock Input, CML
7	SLBI-	Negative System Loopback Input or Negative Reference Clock Input, CML
8	SIS	Signal Input Selection, LVTTTL. Low for normal data, high for system loopback.
9	$\overline{\text{LOL}}$	Loss-of-Lock Output, LVTTTL, Active Low
10	$\overline{\text{LREF}}$	TTL Control Input for PLL Clock Holdover. Low for PLL lock to reference clock, high for PLL lock to input data.
12, 14	V _{CC_VCO}	Supply Voltage for the VCO
13	FIL	PLL Loop-Filter Capacitor Input. Connect a 0.068 μ F loop-filter capacitor between FIL and V _{CC_VCO} .
15, 28	V _{CC_OUT}	Supply Voltage for LVDS Output Buffers
17	PCLK-	Negative Clock Output, LVDS
18	PCLK+	Positive Clock Output, LVDS
19	PD0-	Negative Data Output, LVDS
20	PD0+	Positive Data Output, LVDS
21	PD1-	Negative Data Output, LVDS
22	PD1+	Positive Data Output, LVDS
24	PD2-	Negative Data Output, LVDS
25	PD2+	Positive Data Output, LVDS
26	PD3-	Negative Data Output, LVDS, MSB
27	PD3+	Positive Data Output, LVDS, MSB
30	FREFSET	Sets Reference Frequency. LVTTTL low for 622MHz/667MHz reference, high for 155MHz/167MHz reference.
33	CAZ+	Positive Capacitor Input for DC Offset-Cancellation Loop. Connect a 0.1 μ F capacitor between CAZ+ and CAZ-.
34	CAZ-	Negative Capacitor Input for DC Offset-Cancellation Loop. Connect a 0.1 μ F capacitor between CAZ+ and CAZ-.
35	VREF	2.2V Bandgap Reference Voltage Output. Optionally used for threshold adjustment.
36	VCTRL	Analog Control Input for Threshold Adjustment. Connect to V _{CC} to disable threshold adjust.
—	EP	Exposed Pad. The exposed pad must be soldered to the circuit board ground for proper thermal and electrical performance.

2.488Gbps 1:4 Demultiplexer with Clock and Data Recovery and Limiting Amplifier

Detailed Description

The MAX3882A deserializer with clock and data recovery and limiting amplifier converts 2.488Gbps serial data to clean 4-bit-wide, 622Mbps LVDS parallel data. The device combines a limiting amplifier with a fully integrated phase-locked loop (PLL), data retiming block, 4-bit demultiplexer, clock divider, and LVDS output buffer (Figure 5). The PLL consists of a phase/frequency detector (PFD), loop filter, and voltage-controlled oscillator (VCO). The MAX3882A is designed to deliver the best combination of jitter performance and power dissipation by using a fully differential signal architecture and low-noise design techniques.

The input signal to the device (SDI) passes through a DC offset control block, which balances the input signal to a zero crossing at 50%. The PLL recovers the serial clock from the serial input data stream and produces the properly aligned data and the buffered recovered clock. The frequency of the recovered clock is divided by four and converted to differential LVDS parallel output PCLK. The demultiplexer generates 4-bit-wide 622Mbps parallel data.

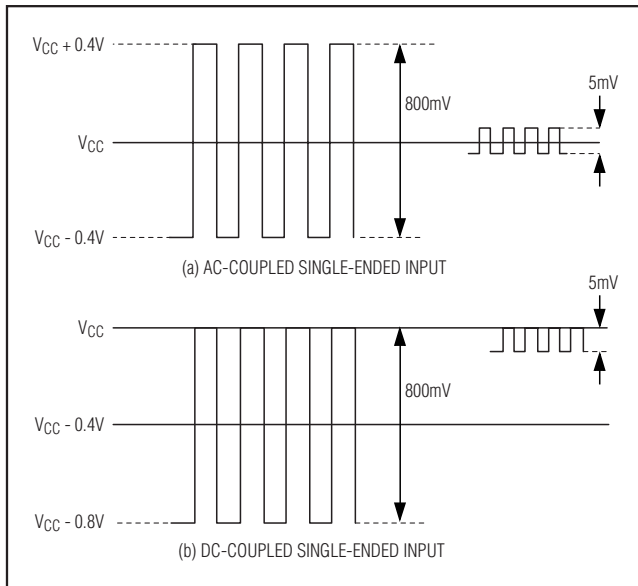


Figure 1. Definition of Input Voltage Swing

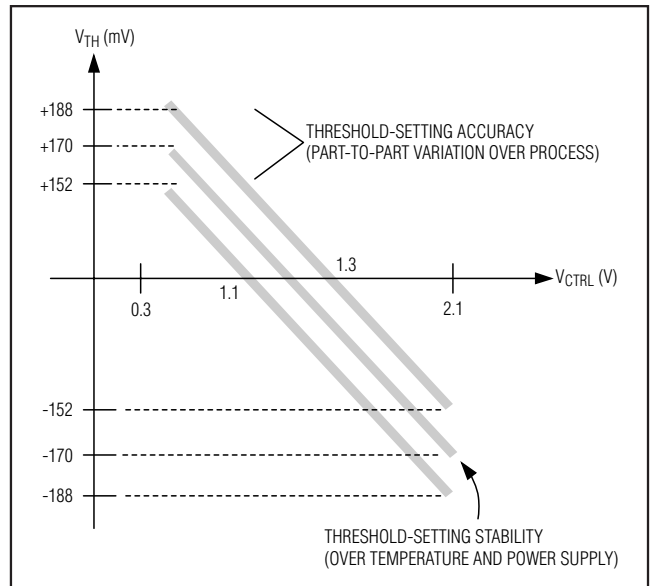


Figure 2. Relationship Between Control Voltage and Threshold Voltage

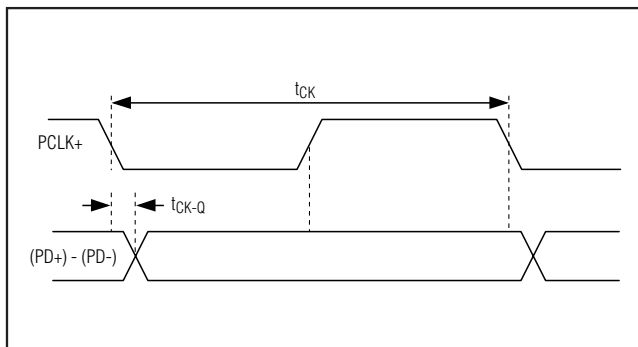


Figure 3. Definition of Clock-to-Q Delay

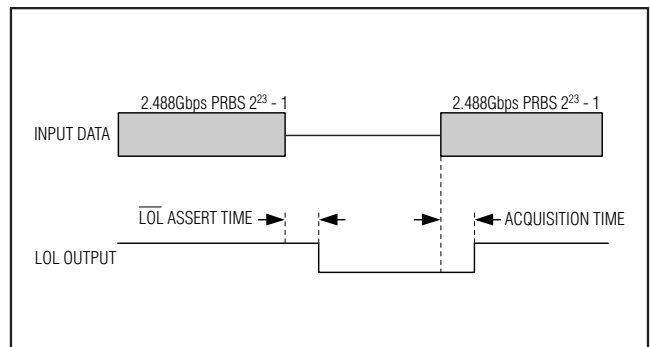


Figure 4. $\overline{\text{LOL}}$ Assert Time and PLL Acquisition Time Measurement

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Input Amplifier

The SDI inputs of the MAX3882A accept serial NRZ data at 2.488Gbps with 10mV_{P-P} to 1600mV_{P-P} amplitude. The input sensitivity is 10mV_{P-P}, at which the jitter tolerance is met for a BER of 10⁻¹⁰ when the threshold adjust is not used. The input sensitivity is as low as 4mV_{P-P} for a BER of 10⁻¹⁰. The MAX3882A is designed to directly interface with a transimpedance amplifier (MAX3277).

For applications when vertical threshold adjustment is needed, the MAX3882A can be connected to the output of an AGC amplifier (MAX3861). Here, the input voltage range is 50mV_{P-P} to 600mV_{P-P}. See the *Design Procedure* section for decision threshold adjust.

Phase Detector

The phase detector in the MAX3882A produces a voltage proportional to the phase difference between the incoming data and the internal clock. Because of its feedback nature, the PLL drives the error voltage to zero, aligning the recovered clock to the center of the incoming data eye for retiming.

Frequency Detector

The digital frequency detector (FD) acquires frequency lock without using an external reference clock. The frequency difference between the received data and the VCO clock is derived by sampling the in-phase and quadrature VCO outputs on both edges of the data input signal. Depending on the polarity of the frequency difference, the FD drives the VCO until the frequency difference is reduced to zero. Once frequency acquisition is complete, the FD returns to a neutral state. False locking is eliminated by this digital frequency detector.

Loop Filter and VCO

The fully integrated PLL has a second-order transfer function, with a loop bandwidth (f_L) fixed at 1.7MHz. An external capacitor between V_{CC_VCO} and FIL sets the damping of the PLL. All jitter specifications are based on the C_{FIL} capacitor being 0.068μF. Note that the PLL

jitter transfer bandwidth does not change as the external capacitor changes, but the jitter peaking, acquisition time, and loop stability are affected.

For an overdamped system ($f_z/f_L < 0.25$), the jitter peaking (J_p) of a second-order system can be approximated by:

$$J_p = 20 \log(1 + f_z/f_L)$$

The PLL zero frequency (f_z) is a function of the external capacitor (C_{FIL}) and can be approximated according to:

$$f_z = 1/2\pi(650)C_{FIL}$$

Figures 6 and 7 show the open-loop and closed-loop transfer functions. The PLL acquisition time is also directly proportional to the external capacitor C_{FIL}.

Loss-of-Lock Monitor

The \overline{LOL} output indicates a PLL lock failure, either due to excessive jitter present at data input or due to loss of input data. In the case of loss of input data, the \overline{LOL} indicates a loss-of-signal condition. The \overline{LOL} output is asserted low when the PLL loses lock.

Output LVDS Interface: PD, PCLK

The MAX3882A's clock and data outputs are LVDS compatible to minimize power dissipation, speed transition time, and improve noise immunity. These outputs comply with the IEEE LVDS specification. The differential output signal magnitude is 250mV to 400mV.

Design Procedure

The MAX3882A provides a differential output clock (PCLK). Table 1 shows the pin configuration for choosing the type of operation mode.

Decision Threshold Adjust

Decision threshold adjust is available for WDM applications where optical amplifiers are used, generating spontaneous optical noise at data logic high. The decision threshold adjust range is ±170mV. Use the provided 2.2V bandgap reference V_{REF} pin or an outside source, such as an output from a DAC to control the

Table 1. Operation Modes

FREFSET	\overline{LREF}	SIS	OPERATION MODE DESCRIPTION
X	1	0	Normal operation: PLL locked to data input at 2.488Gbps
X	1	1	System loopback: PLL lock frequency at 2.488Gbps
1	0	X	Clock holdover: PLL locked to reference frequency at 155MHz
0	0	X	Clock holdover: PLL locked to reference frequency at 622MHz

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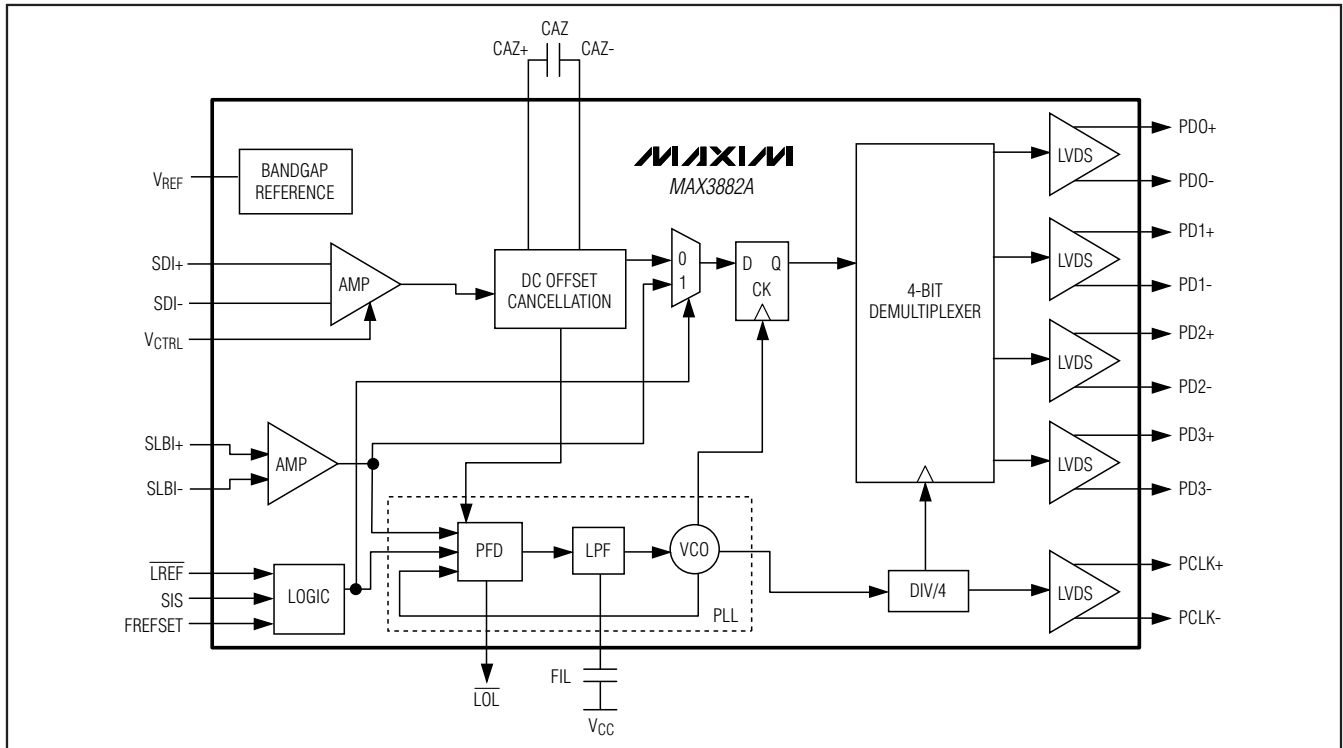


Figure 5. Functional Diagram

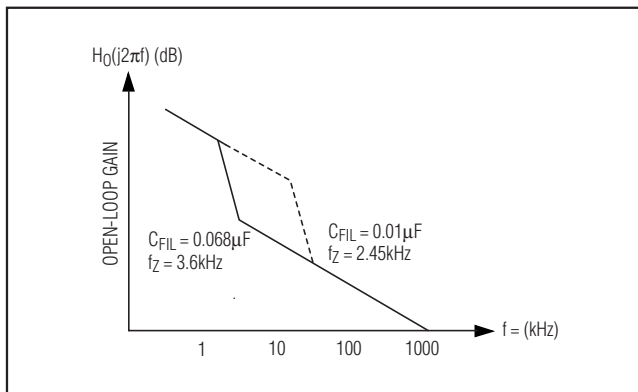


Figure 6. Open-Loop Transfer Function

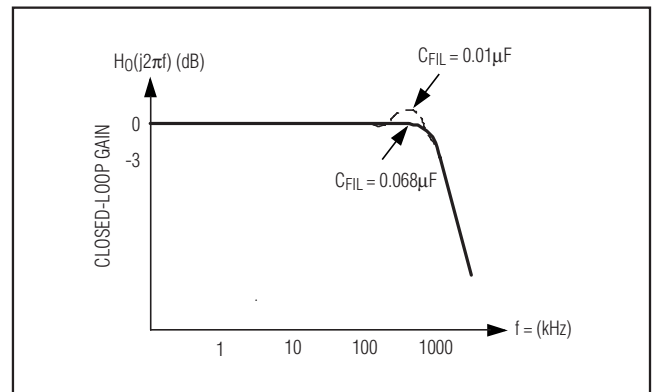


Figure 7. Closed-Loop Transfer Function

threshold voltage. The +170mV to -170mV threshold offset can be accomplished by varying the VCTRL voltage from 0.3V to 2.1V, respectively. See Figure 2. When using the VREF to generate voltage for threshold setting, see Figure 8. Connect VCTRL directly to VCC to disable threshold adjust.

DC-Offset Cancellation Loop Filter

A DC-offset cancellation loop is implemented to remove the DC offset of the limiting amplifier. To minimize the low-frequency pattern-dependent jitter associated with this DC-cancellation loop, the low-frequency cutoff is 10kHz typical with CAZ = 0.1μF, connected across CAZ+ and CAZ-.

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Applications Information

Clock Holdover Capability

Clock holdover is required in some applications where a valid clock needs to be provided to the upstream device in the absence of data transitions. To provide this function, an external reference clock rate of 155MHz or 622MHz must be applied to the SLBI input. Control input FREFSET selects which reference clock rate to use. The control $\overline{\text{LREF}}$ selects whether the PLL locks to the input data stream (SDI) or the reference clock (SLBI). When $\overline{\text{LREF}}$ is low, the input is switched to the reference clock input. This $\overline{\text{LREF}}$ input can be driven by connecting the $\overline{\text{LOL}}$ output pin directly or connecting to any other power monitor signal from the system.

System Loopback

The MAX3882A is designed to allow system loopback testing. The user can connect the serializer output (MAX3892) directly to the SLBI \pm inputs of the MAX3882A for system diagnostics. See Table 1 for selecting the system loopback operation mode. During system loopback, $\overline{\text{LOL}}$ cannot be connected to $\overline{\text{LREF}}$.

Interfacing the MAX3882A

To correctly interface with the MAX3882A's CML input and LVDS outputs, refer to Application Note 291: *HFAN-1.0: Introduction to LVDS, PECL, and CML*.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies, keep ground connections short, and use multiple vias where possible. Use controlled-impedance transmission lines to interface with the MAX3882A high-speed inputs and outputs. Power-supply decoupling should be placed as close to the VCC as possible. To reduce feedthrough, isolate input signals from output signals.

Exposed-Paddle Package

The exposed pad, 36-pin TQFN incorporates features that provide a very low thermal-resistance path for heat removal from the IC. The pad is electrical ground on the MAX3882A and should be soldered to the circuit board for proper thermal and electrical performance.

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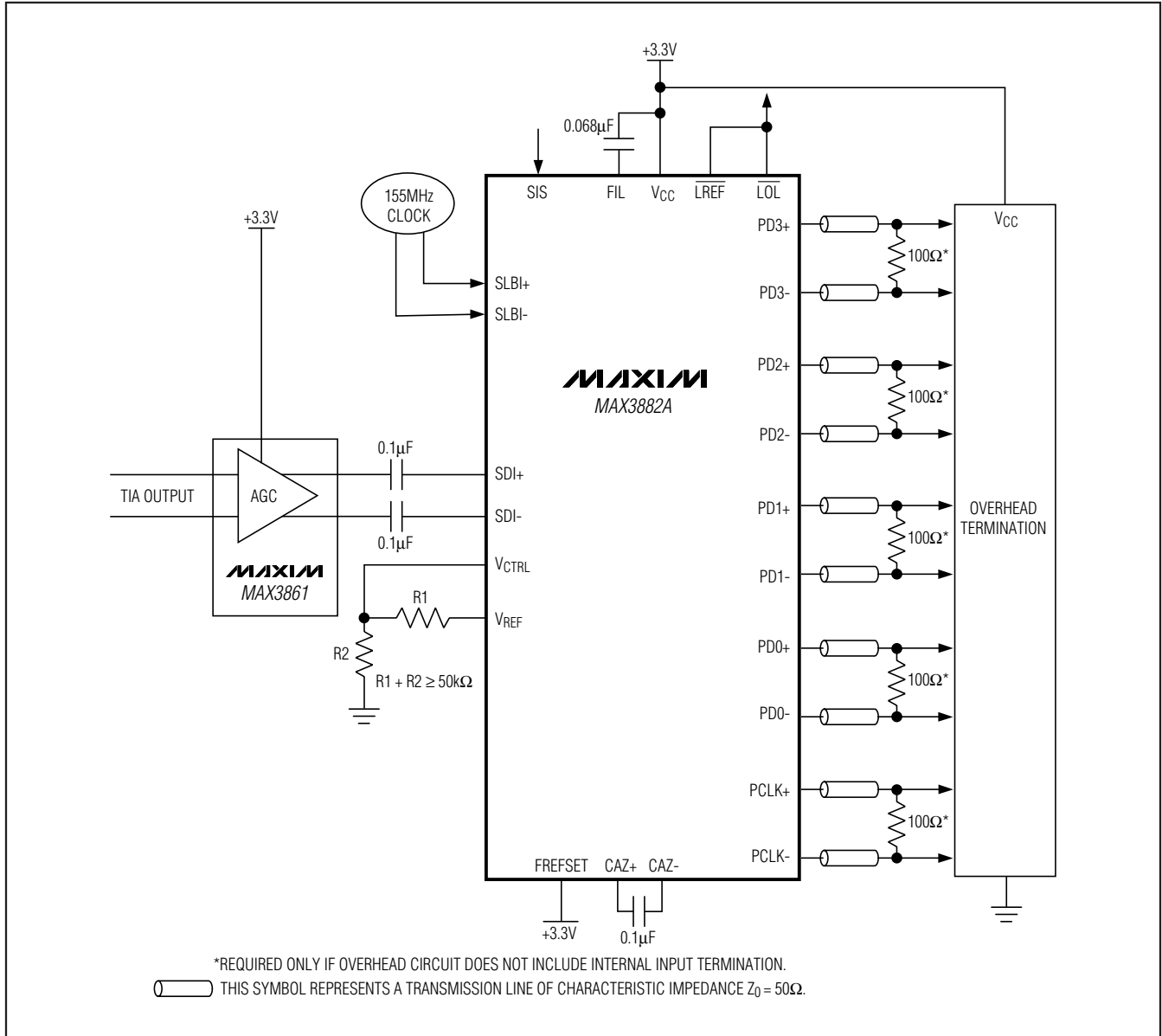
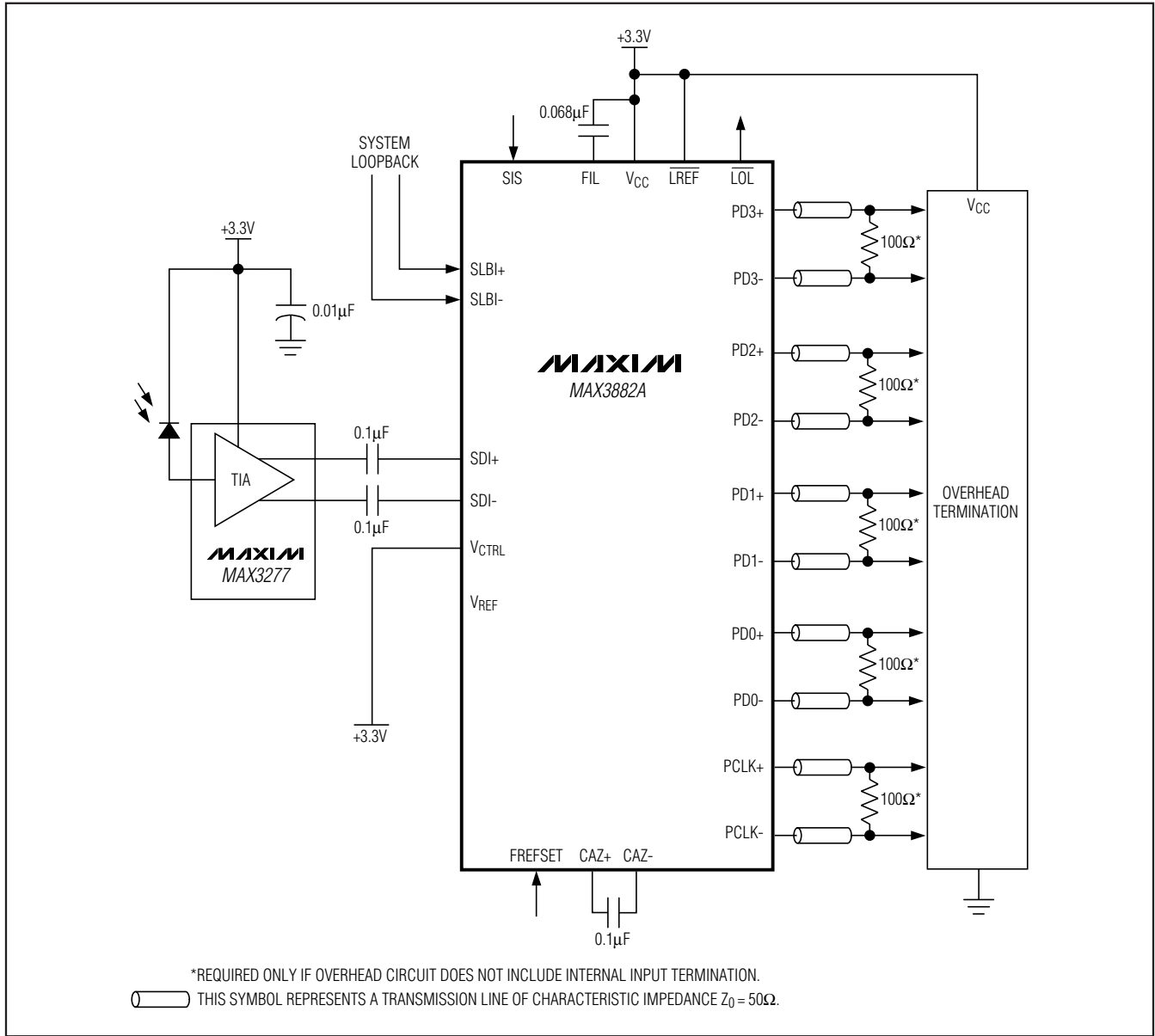


Figure 8. Connecting the MAX3882A with Threshold Adjust and Clock Holdover Enabled

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Typical Application Circuit



Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
36 TQFN-EP	T3666-2	21-0141

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/03	Initial release (MAX3882 only).	—
1	11/05	Added the MAX3882A.	All
2	4/09	Removed the MAX3882.	All

MAX3882A

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