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Data Sheet Specifications

TC35420XLG TransferJet™ Close-Proximity, Wireless Transfer Technology Compliant IC

General Description

TC35420XLG is a wireless IC that supports the TransferJet™ close-proximity, wireless standard devised by the TransferJet Consortium. The TC35420XLG integrates a built-in RF circuit, digital control logic, a host interface and memory interface on a monolithic die and uses an LGA81 package enabling a small design footprint ideal for battery-powered consumer electronic devices.

Features

- TransferJet Specification compliant (PCL-NCL Specification 1.1 compliant)
  - Output frequency: 4.48 GHz
  - Transmit output: up to -42.5 dBm (-70 dBA/MHz)
  - Transfer speed: 522 Mbps (max.)
- External reference clock: 20 MHz/40 MHz(Xtal)
- Host Interface: SDIO device I/F (High-speed UHS-I supports)
- SPI for memory interface: EEPROM (optional)
- Power Supply Management Unit (PMU)
- 10KHz CR oscillatior
- Low-power consumption

- Low-power mode support
  - Shut down mode
  - Deep sleep mode
  - Sleep mode
  - Dormant mode
- Power supply voltage (built-in LDO)
  - Single power supply operation: 1.8V
  - Double power supply operation: 1.8V/3.3V
- Package: P-XFLGA81-0404-0.40

TransferJet Specification Compliant (PCL-NCL Specification 1.1 Compliant)
— Output frequency: 4.48 GHz

Built-in SDIO Device Controller
— Built-in SDIO device controller for host CPU interface.
— Supported "SDA SDIO device specification Ver3.00" (corresponding to 4-bit/1-bit)
— Output frequency: 4.48 GHz

Built-in SDIO CNL Buffer
— CNL buffer for data transfer.
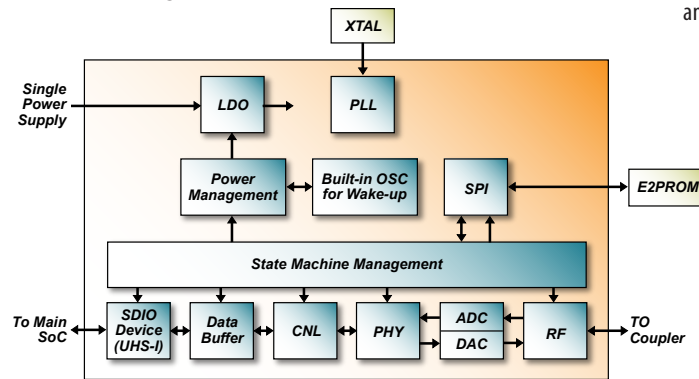
Built-in LDO for Internal Circuit

Clock
— TC35420 starts operation after power on and CROSC (10 kHz) clock supply.
— Internal clock during TranferJet operation is generated by external Xtal: crystal 20 MHz or 40 MHz, Power Management Unit controls oscillation enable and disable.
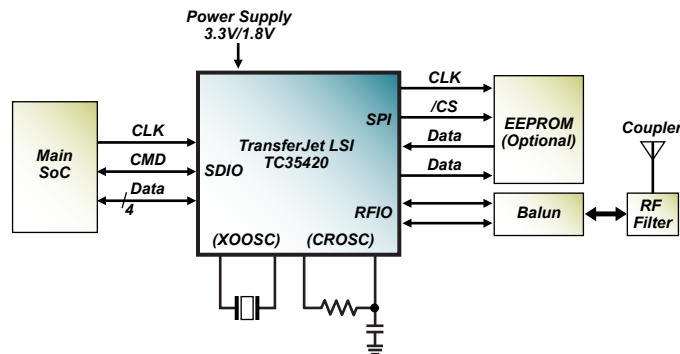
TC35420 Block Diagram

TC35420 Example System Configuration Diagram

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Built-in Power Management Unit (PMU)
— Control power supply for inner circuit depending on mode transition of TC35420.

Built-in RF Circuit
— RF input (reception) and output (transmission) is differential type.

Built-in Serial Peripheral Interface (SPI)
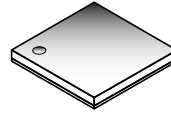— Built-in SPI for EEPROM interface.

Built-in High-Speed ADC / DAC
— Built-in high-speed ADC, enables the RF signal to input directly to the TC35420.
— Built-in DAC for RF output, RF signal can output directly to the TC35420.

PHY
— Modulation and coding scheme: Pi/2 shift BPSK + DSSS ½ Convolutional Code + Reed-Solomon Code.
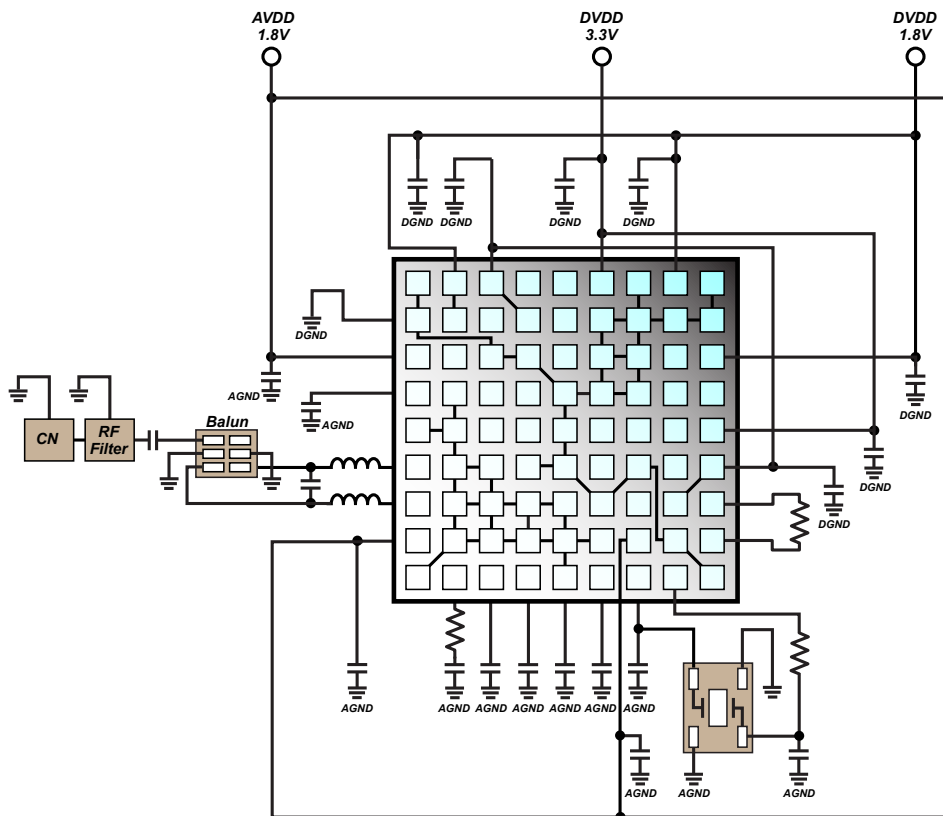
Small Package
— 81-pin LGA package.

Low-Power Consumption
— TC35420 can provide a low-power consumption state by standby operation with software set up or shutdown operation with set up.

Other
— Keep 3.3V and 1.8V power on and off seqence specification.

Example Application Circuit Diagram

Example Application Circuit

— The analog GND should be separated from the digital GND. Each should be completely grounded with low impedance.
— The crystal and the oscillation capacitor should be placed close to the XO_IN and XO_OUT pins using the shortest possible distance.

— As in the above figure, the power supply bypass capacitor is indicated in a simplified form. The digital power supply should be bypassed to DGND and the analog power supply to AGND with a capacitor closest to the pin.

— Using dumping resistors in a series with digital signal output may be effective in reducing spurious output.
— It is recommended the RF power supply (RFVDD: 1.8V), analog power supply (ADAVDD: 1.8V) and digital power supply (DVDD: 1.8V) be provided separately.

— It is recommended to have characteristics matching the mounterd PCB, components, and connected coupler for the RF portion of the circuit.
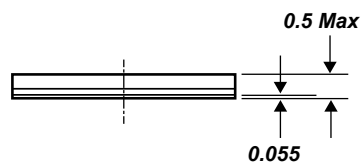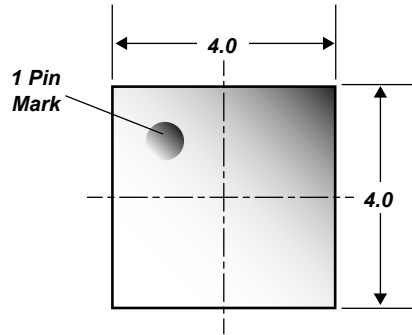
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Package

TC35420XLG Package is
P-XFLGA81-0404-0.40.
Unit: mm

Top View

Bottom View
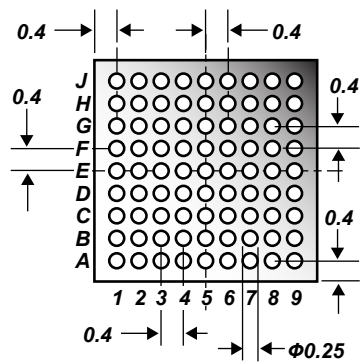
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