The GLS85LP1008B NANDrive™ solid-state drive (SSD) combines a NAND controller and 8 GBytes of NAND flash in a multi-chip package. It provides complete ATA/IDE hard disk drive functionality in a small package for easy, space-saving mounting to a system motherboard. This makes the GLS85LP1008B NANDrive SSD the ideal data storage solution for mobile and embedded electronic products that require smaller and more reliable storage.

Features

- **Industry Standard ATA/IDE Bus Interface**
  – Host Interface: 16-bit access
  – Supports up to PIO Mode-6
  – Supports up to Multi-word DMA Mode-4
  – Supports up to Ultra DMA Mode-6

- **Low Power, 3.3V Power Supply**

- **Low Current Operation:**
  – Active mode: 125 mA typical
  – Sleep mode: 700 µA typical

- **Power Management Unit**
  – Immediate disabling of unused circuitry without host intervention
  – Zero wake-up latency

- **Expanded Data Protection**
  – WP#/PD# pin configurable by firmware for prevention of data overwrites
  – Data security through user-selectable protection zones with advanced NAND management technology

- **20-byte Unique ID for Enhanced Security**
  – Factory Pre-programmed 10-byte Unique ID
  – User-Programmable 10-byte ID

- **Integrated Voltage Detector**
  – Prevents inadvertent Write operations due to unexpected power-down or brownout.

- **Pre-programmed Embedded Firmware**
  – Executes industry standard ATA/IDE commands
  – Implements advanced wear-leveling algorithms to substantially increase the longevity of flash media
  – Embedded Flash File System

- **Robust Built-in ECC**
  – Corrects up to 24 random bits of error

- **Multi-tasking Technology Enables Fast Sustained Write Performance**
  – Up to 12 MByte/sec

- **Fast Sustained Read Performance**
  – Up to 55 MByte/sec

- **Commercial Temperature Range**
  – 0°C to 70°C

- **91-ball LBGA package**
  – 14mm x 24mm x 1.3mm

- **All non-Pb (lead-free) Devices are RoHS Compliant**

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Product Description

The GLS85LP1008B NANDrive™ solid-state drive (SSD) is a high-performance, fully-integrated, embedded flash solid state drive. It combines an integrated NAND Controller and 8 GByte of MLC NAND Flash in a multi-chip package. This product is ideal for solid state mass storage applications offering new and expanded functionality while enabling cost effective designs.

ATA-based solid state mass storage technology is widely used in portable and desktop computers, digital cameras, music players, handheld data collection scanners, cellular phones, PCS phones, PDAs, handy terminals, personal communicators, robotics, audio recorders, monitoring devices, and set-top boxes.

Greenliant NANDrive is a solid state drive designed for embedded ATA/IDE protocol systems and supports standard ATA/IDE protocol with up to PIO Mode-6, Multi-word DMA Mode-4 and Ultra DMA Mode-6 interface. The built in microcontroller and file management firmware communicates with ATA standard interfaces; thereby eliminating the need for additional or proprietary software, such as Flash File System (FFS), on the host.

The GLS85LP1008B NANDrives provide complete IDE Hard Disk Drive functionality and compatibility in a 14mm x 24mm LBGA package for easy, space saving mounting to a system motherboard. It is a perfect solution for portable, consumer electronic products requiring smaller and more reliable data storage.

The NANDrive provides a WP#/PD# pin to protect critical information stored in the flash media from unauthorized overwrites.

Pre-programmed with a 10-byte unique serial ID, NANDrive allows users to program an additional 10 Bytes of ID space to create a unique, 20-byte ID for greater system security.

NANDrive SSD is available with advanced NAND management technology, a NAND memory management technology that enhances data security, significantly improves endurance, and accurately predicts the rated life span of NAND flash devices. Advanced NAND management technology combines NAND controller hardware error correction, advanced wear leveling algorithms, and bad block management to extend the life of the product.

General Description

Each NANDrive contains an integrated NAND Controller and NAND Flash dies in a LBGA package. Refer to Figure 1 for the NANDrive block diagram.

Performance-optimized NANDrive

The heart of the NANDrive is the NAND Controller which translates standard ATA signals into flash media data and control signals. The following components contribute to the NANDrive's operation.

Microcontroller Unit (MCU)

The 32-bit RISC architecture transfers the ATA/IDE commands into data and control signals required for flash media operation.

Power Management Unit (PMU)

The power management unit controls the power consumption of the NANDrive. The PMU dramatically reduces the power consumption of the NANDrive by putting the part of the circuitry that is not in operation into sleep mode.

The Flash File System handles inadvertent power interrupts and has auto-recovery capability to insure NANDrive data integrity. For regular power management, the Host must send an Idle_Immediate command and wait for command ready before powering down the NANDrive.

SRAM Buffer

A contributor to the NANDrive performance is an SRAM buffer. The buffer optimizes the host's data transfer to and from the flash media.

Embedded Flash File System

The embedded flash file system is an integral part of the NANDrive. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads.

2. Provides flash media wear leveling to spread the flash writes across all memory address space to increase the longevity of flash media.

3. Keeps track of data file structures.

4. Stores the data in Flash media upon completion of a Write command. The NANDrive does not do Post-Write operations, except for when the write cache is enabled by the Host command.

Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed for manufacturing error reporting. During the design process, always provide access to the SCI interface in the PCB design to aid in design validation.

Multi-tasking Interface

The multi-tasking interface enables fast, sustained write performance by allowing concurrent Read, Program, and Erase operations to multiple flash media devices.

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Error Correction Code (ECC)

High performance is achieved through optimized hardware error detection and correction.

Internal Direct Memory Access (DMA)

The NANDrive uses internal DMA allowing instant data transfer from buffer to flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

NAND Flash

The NANDrive family utilize standard NAND Flash for data storage. Because the re-flow process can alter the NANDrive content, do not program the GLS85LP1008B NAND before the reflow process.

Advanced NAND Management Technology

Advanced NAND management technology balances the wear on erased blocks with an advanced wear-leveling scheme which provides a minimum of 7 million host write cycles. Advanced NAND management technology tracks the number of program/erase cycles within a group. When the host updates data, higher priority is given to the less frequently written erase blocks; thereby, evenly distributing host writes within a wear-leveling group.

The product also supports a global wear-leveling feature which can be enabled or disabled by the Host command. When the global wear-leveling is enabled, the wear-leveling is performed both across and within the groups. Please contact Greenliant for more information about this feature. By default, global wear-leveling is enabled.

Advanced NAND management technology enhances NANDrive security with password protection and four independent protection zones which can be set to Read-only or Hidden.

Functional Blocks
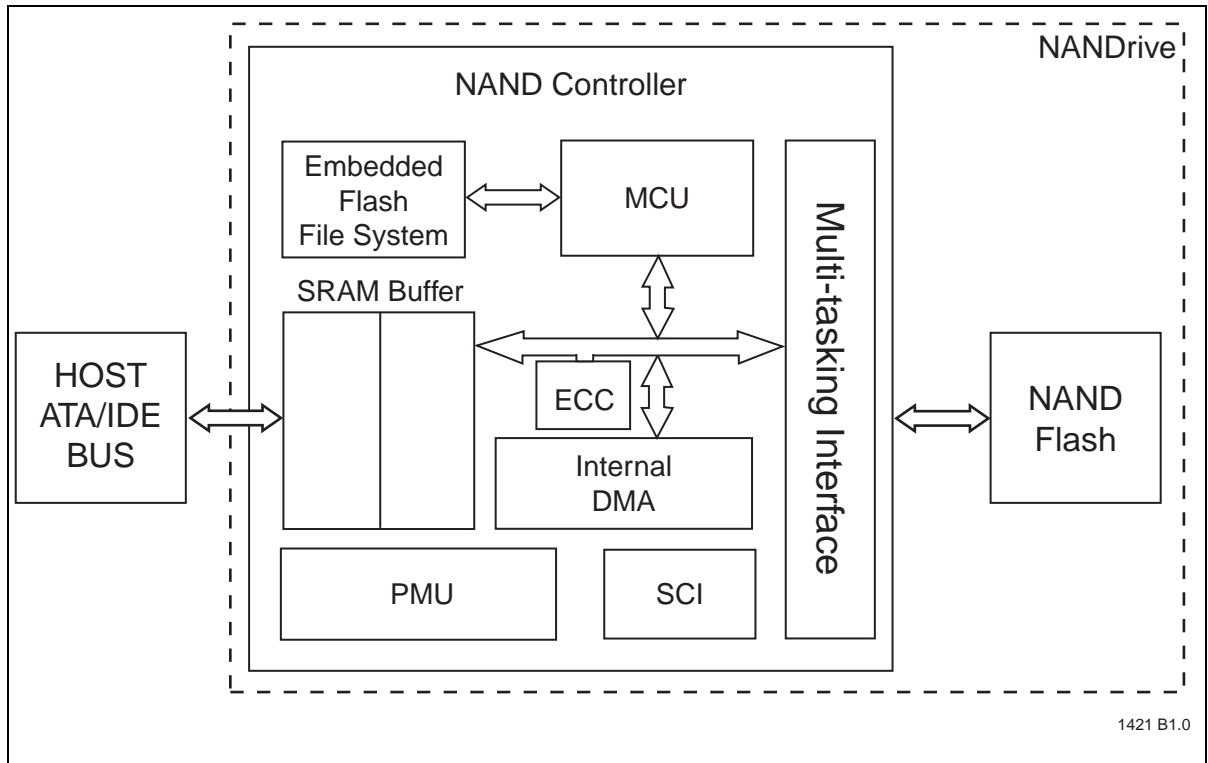
Figure 1: NANDrive Block Diagram

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Advance Information

Pin Assignments

The signal/pin assignments are listed in Figure 2. Low active signals have a "#" suffix. Pin types are Input, Output, or Input/Output. Signals whose source is the host are designated as inputs while signals that the NANDrive sources are outputs.

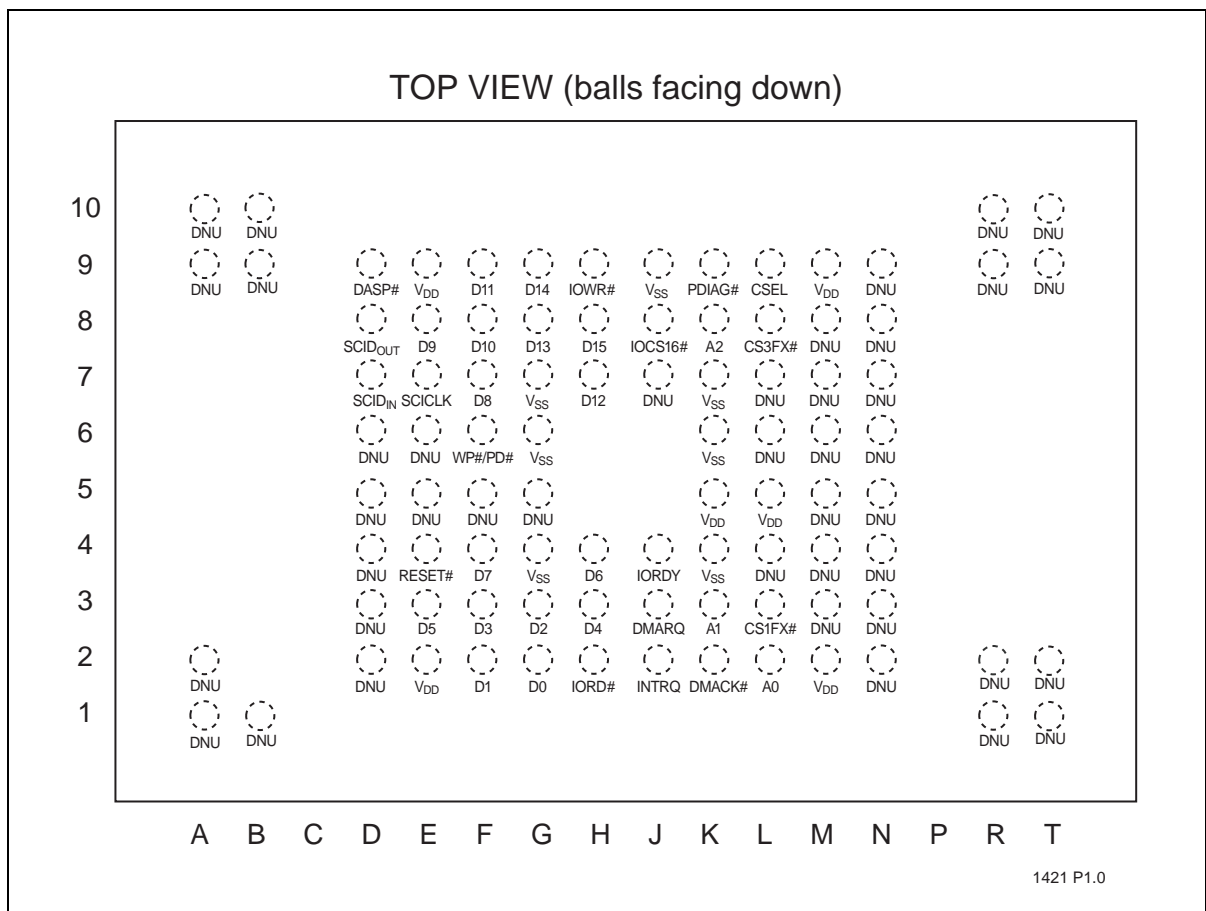The NANDrive functions in ATA mode, which is compatible with IDE hard disk drives.

Figure 2: Pin Assignments for 91-Ball LBGA

Greenliant™

Table 1: Pin Assignments (1 of 2)

Symbol	Pin No. 91-LBGA	Pin Type	I/O Type	Name and Functions
Host Side Interface				
A2	K8			
A1	K3	I	I1Z	A[2:0] are used to select one of eight registers in the Task File.
A0	L2			
D15	H8			
D14	G9			
D13	G8			
D12	H7			
D11	F9			
D10	F8			
D9	E8			
D8	F7	I/O	I1Z/O2	D[15:0] Data bus
D7	F4			
D6	H4			
D5	E3			
D4	H3			
D3	F3			
D2	G3			
D1	F2			
D0	G2			
DMACK#	K2	I	I2U	DMA Acknowledge - input from host
DMARQ	J3	O	O2	DMA Request to host
CS1FX#	L3			CS1FX# is the chip select for the task file registers
CS3FX#	L8	I	I2Z	CS3FX# is used to select the alternate status register and the Device Control register.
CSEL	L9	I	I1U	This internally pulled-up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave. The pin setting should remain the same from Power-on to Power-down.
IORD#	H2	I	I2Z	IORD#: This is an I/O Read Strobe generated by the host. When Ultra DMA mode is not active, this signal gates I/O data from the device. (This pin supports three functions)
				HDMARDY#: In Ultra DMA mode when DMA Read is active, this signal is asserted by the host to indicate that the host is ready to receive Ultra DMA data-in bursts. The host may negate HDMARDY# to pause an Ultra DMA transfer.
				HSTROBE: When DMA Write is active, this signal is the data-out strobe generated by the host. Both the rising and falling edges of HSTROBE cause data to be latched by the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
IOWR#	H9	I	I2Z	IOWR#: This is an I/O Write Strobe generated by the host. When Ultra DMA mode is not active, this signal is used to clock I/O data into the device. (This pin supports two functions)
				STOP: When Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst

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Table 1: Pin Assignments (Continued) (2 of 2)

Symbol	Pin No. 91-LBGA	Pin Type	I/O Type	Name and Functions
IORDY	J4	O	O2	IORDY: When in PIO mode, the device is not ready to respond to a data transfer request. This signal is negated to extend the Host transfer cycle from the assertion of IORD# or IOWR#. However, it is never negated by this controller. (This pin supports three functions)
				DDMARDY#: When Ultra DMA mode DMA Write is active, this signal is asserted by the device to indicate that the device is ready to receive Ultra DMA data-out bursts. The device may negate DDMARDY# to pause an Ultra DMA transfer.
				DSTROBE: When Ultra DMA mode DMA Read is active, this signal is the data-in strobe generated by the device. Both the rising and falling edges of DSTROBE cause data to be latched by the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-in burst.
IOCS16#	J8	O	O3	This output signal is asserted low when the device is indicating a word data transfer cycle.
INTRQ	J2	O	O2	This signal is the active high Interrupt Request to the host.
PDIAG#	K9	I/O	I1U/O2	The Pass Diagnostic signal in the Master/Slave handshake protocol.
DASP#	D9	I/O	I1U/O4	The Drive Active/Slave Present signal in the Master/Slave handshake protocol.
RESET#	E4	I	I2U	This input pin is the active low hardware reset from the host.
Serial Communication Interface (SCI)				
$SCID_{OUT}$	D8	O	O2	SCI interface data output
$SCID_{IN}$	D7	I	I1U	SCI interface data input
SCICLK	E7	I	I1D	SCI interface clock
Miscellaneous				
WP#/PD#	F6	I	I2U	The WP#/PD# pin can be used for either the Write Protect mode or Power-down mode, but only one mode is active at any time. The Write Protect or Power-down modes can be selected through the host command. The Write Protect mode is the factory default setting.
V_{SS}[1]	G4, G6, G7, K4, K6, K7, J9	PWR		Ground
V_{DD}[1]	E2, E9, K5, L5, M2, M9	PWR		V_{DD} (3.3V)
DNU	A1, A2, A9, A10, B1, B9, B10,D2, D3, D4, D5, D6, E5,E6, F5, G5, J7, L4, L6, L7, M3, M4, M5, M6, M7, M8, N2, N3, N4, N5, N6, N7, N8, N9, R1, R2, R9, R10, T1, T2, T9, T10			Do not use.

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1. Any VSS or V_{DD} pin must not be left open or floating.

Capacity Specification

Table 2 shows the default capacity and specific settings for heads, sectors, and cylinders. At production time, the manufacturer can change the default settings in the drive ID table by changing the Cylinders-Heads Sectors configuration. If the total number of bytes configured is less than the default amount, the remaining space could be used as spare blocks to increase the flash drive endurance. It should also be noted that if the initialized total flash drive capacity exceeds the total bytes shown in Table 2, the flash drive endurance will be reduced.

Table 2: Default NANDrive Settings

Capacity	Total Bytes	Cylinders	Heads	Sectors	Max LBA
8 GByte	7,314,628,608	14173	16	63	14,286,384

T2.0 1421

Table 3: Sustained Performance

Product	Write Performance	Read Performance
GLS85LP1008B-M-C-LFTE	Up to 12 MByte/sec	Up to 55 MByte/sec

T3.0 1421

Table 4: Supported ATA Modes

Products	PIO	MWDMA	UltraDMA
GLS85LP1008B-M-C-LFTE	Up to Mode-6	Up to Mode-4	Up to Mode-6

T4.0 1421

Configurable Write Protect/Power-down Modes

The WP#/PD# pin can be used for either Write Protect mode or Power-down mode, but only one mode is active at any time. Either mode can be selected through the host command, Set-WP#/PD#-Mode.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

Write Protect Mode

When the device is configured in the Write Protect mode, the WP#/PD# pin offers extended data protection. This feature can be either selected through a jumper or host logic to protect the stored data from inadvertent system writes or erases, and viruses. The Write Protect feature protects the full address space of the data stored on the flash media.

In the Write Protect mode, assert the WP#/PD# pin prior to issuing all destructive commands: Erase-Sector, Format-Track, Write-DMA, Write-Multiple, Write-Sector(s), or Write-Verify. This will force the NANDrive to reject any destructive commands from the ATA interface. All destructive commands will return 51H in the Status register and 04H in the Error register signifying an invalid command. All non-destructive commands will be executed normally.

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Power-down Mode

When the device is configured in the Power-down mode, if the WP#/PD# pin is asserted during a command, the NANDrive stops the ongoing command and immediately enters power-down mode. Afterwards, the device will not accept any other commands. Both a software or a hardware reset will bring the device to normal operation with the WP#/PD# pin de-asserted.

Power-on Initialization

NANDrive is self-initialized during the first power-up. As soon as the power is applied to the NANDrive it reports busy for typically up to seven seconds while performing bad blocks search and low level format. This initialization is a one time event.

During the first self-initialization, the NANDrive firmware scans all connected flash media devices and reads their device ID. If the device ID matches the listed flash media devices, the NANDrive performs drive recognition based on the algorithm provided by the flash media suppliers, including setting up the bad block table, executing all the necessary handshaking routines for flash media support, and, finally, performing the low-level format.

If the drive initialization fails, and a visual inspection is unable to determine the problem, Greenliant provides a comprehensive interface for manufacturing flow debug. This interface not only allows debug of the failure and manual reset of the initialization process, but also allows customization of user definable options.

ATA/IDE Host Interface

The ATA/IDE host interface can be used for NANDrive manufacturing support. Greenliant provides an example of a DOS- and Windows™-based solution (an executable routine) for manufacturing debug and rework.

Serial Communication Interface   (SCI)

For additional manufacturing flexibility, the SCI bus can be used for manufacturing error reporting and for accessing the status of the controller's internal activities. The SCI consists of 3 active signals: SCID$_{OUT}$, SCID$_{IN}$, and SCICLK. Always provide access to the SCI interface in the PCB design to aid in design validation.

Lifetime Expectancy

NANDrive with advanced NAND management technology significantly extends the life of a product with its extensive ECC and advanced wear-leveling.

For applications where data security is essential, NANDrive with advanced NAND management technology offers two additional protection features—protection zones and password protections.

Protection zones - Up to four independent protection zones can be enabled as either Read-only or Hidden (Read/Write protected). If the zones are not enabled, the data is unprotected (default configuration).

Password Protection - Requires a customer-unique password to access information within the protected zones.

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Power-on and Brown-out Reset Characteristics

Figure 3 and Table 5 detail the Power-on and Brown-out reset characteristics of the GLS85LP1008B.
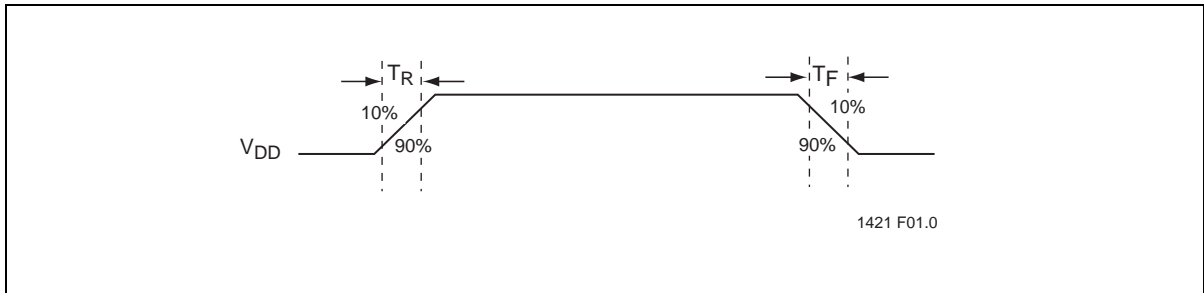
Figure 3: Power-on and Brown-out Reset Timing

Table 5: Power-on and Brown-out Reset Timing

Item	Symbol	Min	Max	Units
V_{DD} Rise Time	T_R		250	ms
V_{DD} Fall Time	T_F		250	ms

T5.0 1421

I/O Transfer Function

The default operation for the NANDrive is 16-bit. However, if the host issues a Set-Feature command to enable 8-bit mode, the NANDrive permits 8-bit data access.

The following table defines the function of various operations.

Table 6: I/O Function

Function Code	CS3FX#	CS1FX#	A0-A2	IORD#	IOWR#	D15-D8	D7-D0
Invalid Mode	V_{IL}	V_{IL}	X	X	X	Undefined	Undefined
Standby Mode	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Task File Write	V_{IH}	V_{IL}	1-7H	V_{IH}	V_{IL}	X	Data In
Task File Read	V_{IH}	V_{IL}	1-7H	V_{IL}	V_{IH}	High Z	Data Out
Data Register Write	V_{IH}	V_{IL}	0	V_{IH}	V_{IL}	In[1]	In
Data Register Read	V_{IH}	V_{IL}	0	V_{IL}	V_{IH}	Out[1]	Out
Control Register Write	V_{IL}	V_{IH}	6H	V_{IH}	V_{IL}	X	Control In
Alt Status Read	V_{IL}	V_{IH}	6H	V_{IL}	V_{IH}	High Z	Status Out

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1. If 8-bit data transfer mode is enabled.
   In 8-bit data transfer mode, High Byte is undefined for Data Out. For Data In, X can be V_{IH} or V_{IL}, but no other value.

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Software Interface

NANDrive Command Description

This section defines the software requirements and the format of the commands the host sends to the NANDrive. Commands are issued to the NANDrive by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register. With the exception of commands listed in Sections "Idle - 97H or E3H", "Set-Sleep-Mode - 99H or E6H", and "Set-WP#/PD#-Mode - 8BH", NANDrive complies with ATA-7 Specifications.

NANDrive Command Set

Table 7 summarizes the NANDrive command set.

Table 7: NANDrive Command Set (1 of 2)

Command	Code	FR[1,2]	SC[2,3]	SN[2,4]	CY[2,5]	DH[6,7]	LBA[2,8]
Check-Power-Mode	E5H or 98H	-	-	-	-	D	-
Execute-Drive-Diagnostic	90H	-	-	-	-	D	-
Flush-Cache	E7H	-	-	-	-	D	-
Flush-Cache-EXT	EAH	-	-	-	-	D	-
Identify-Drive	ECH	-	-	-	-	D	-
Idle	E3H or 97H	-	Y	-	-	D	-
Idle-Immediate	E1H or 95H	-	-	-	-	D	-
Initialize-Drive-Parameters	91H	-	Y	-	-	Y	-
NOP	00H	-	-	-	-	D	-
Read-Buffer	E4H	-	-	-	-	D	-
Read-DMA	C8H or C9H	-	Y	Y	Y	Y	Y
Read-DMA-EXT	25H	-	Y	Y	Y	Y	Y
Read-Multiple	C4H	-	Y	Y	Y	Y	Y
Read-Multiple-EXT	29H	-	Y	Y	Y	Y	Y
Read-Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
Read-Sector(s)-EXT	24H	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
Read-Verify-Sector(s)-EXT	42H	-	Y	Y	Y	Y	Y
Recalibrate	1XH	-	-	-	-	D	-
Security-Disable-Password	F6H	-	-	-	-	D	-
Security-Erase-Prepare	F3H	-	-	-	-	D	-
Security-Erase-Unit	F4H	-	-	-	-	D	-
Security-Freeze-Lock	F5H	-	-	-	-	D	-
Security-Set-Password	F1H	-	-	-	-	D	-
Security-Unlock	F2H	-	-	-	-	D	-
Seek	7XH	-	-	Y	Y	Y	Y
Set-Features	EFH	Y	-	-	-	D	-
SMART	B0H	Y	Y	Y	Y	D	-
Set-Multiple-Mode	C6H	-	Y	-	-	D	-
Set-Sleep-Mode	E6H or 99H	-	-	-	-	D	-
Set-WP#/PD#-Mode	8BH	Y	-	-	-	D	-

Advance Information

Table 7: NANDrive Command Set (Continued) (2 of 2)

Command	Code	FR[1,2]	SC[2,3]	SN[2,4]	CY[2,5]	DH[6,7]	LBA[2,8]
Standby	E2H or 96H	-	-	-	-	D	-
Standby-Immediate	E0H or 94H	-	-	-	-	D	-
Write-Buffer	E8H	-	-	-	-	D	-
Write-DMA	CAH or CBH	-	Y	Y	Y	Y	Y
Write-DMA-EXT	35H	-	Y	Y	Y	Y	Y
Write-Multiple	C5H	-	Y	Y	Y	Y	Y
Write-Multiple-EXT	39H	-	Y	Y	Y	Y	Y
Write-Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
Write-Sector(s)-EXT	34H	-	Y	Y	Y	Y	Y
Write-Verify	3CH	-	Y	Y	Y	Y	Y

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1. FR - Features register
2. Y - The register contains a valid parameter for this command.
3. SC - Sector Count register
4. SN - Sector Number register
5. CY - Cylinder registers
6. For the Drive/Head register:Y means both the Drive and Head parameters are used;
   D means only the Drive parameter is valid and not the Head parameter.
7. DH - Drive/Head register
8. LBA - Logical Block Address mode supported (see command descriptions for use)

Identify-Drive - ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify-Drive command enables the host to receive parameter information from the NAN-Drive. This command has the same protocol as the Read-Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 8. All reserved bits or words are zero. Table 8 gives the definition for each field in the Identify-Drive information.

Table 8: Identify-Drive Information (1 of 3)

Word Address	Default Value[1]	Total Bytes	Data Field Type Information
0	044AH	2	General configuration bit
1	bbbbH[2]	2	Default number of cylinders
2	0000H	2	Reserved
3	bbbbH[2]	2	Default number of heads
4	0000H	2	Reserved
5	0000H	2	Reserved
6	bbbbH[2]	2	Default number of sectors per track

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Table 8: Identify-Drive Information (Continued) (2 of 3)

Word Address	Default Value[1]	Total Bytes	Data Field Type Information
7-8	bbbbH[3]	4	Number of sectors per device (Word 7 = MSW, Word 8 = LSW)
9	xxxxH	2	Vendor Unique
10-14	eeeeH[4]	10	User-programmable serial number in ASCII
15-19	ddddH[5]	10	Greenliant preset, unique ID in ASCII
20	0000H	2	Retired
21	xxxxH	2	Vendor Unique
22	xxxxH	2	Vendor Unique
23-26	aaaaH[6]	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	ccccH[7]	40	User Definable Model number
47	8001H	2	Maximum number of sectors on Read/Write-Multiple command
48	0000H	2	Reserved
49	0B00H	2	Capabilities
50	010xH	2	Reserved
51	0200H	2	PIO Data Transfer Cycle Timing Mode
52	0000H	2	Reserved
53	0007H	2	Translation parameters are valid
54	nnnnH	2	Current numbers of cylinders
55	nnnnH	2	Current numbers of heads
56	nnnnH	2	Current sectors per track
57-58	nnnnH	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)
59	010xH	2	Multiple sector setting
60-61	nnnnH	4	Total number of sectors addressable in LBA mode
62	0000H	2	Reserved
63	xx07H	2	DMA data transfer is supported in NAND Controller
64	0003H	2	Advanced PIO Transfer mode supported
65	0078H	2	120 ns cycle time support for Multi-word DMA Mode-2
66	0078H	2	120 ns cycle time support for Multi-word DMA Mode-2
67	0078H	2	PIO Mode-4 supported
68	0078H	2	PIO Mode-4 supported
69-79	0000H	22	Reserved
80	00FEH	2	ATA major version number
81	0021H	2	ATA minor version number
82	706BH	2	Features/command sets supported
83	7408H	2	Features/command sets supported
84	4000H	2	Features/command sets supported
85-87	xxxxH	6	Features/command sets enabled
88	007FH	2	UDMA modes
89	xxxxH	2	Time required for security erase unit completion
90	xxxxH	2	Time required for enhanced security erase unit completion
91	0000H	2	Advanced Power Management Level. This always returns 0000H.
92	0000H	2	Reserved
93	bbbbH	2	Hardware reset result
94-99	0000H	12	Reserved
100-103	nnnnH	8	Maximum user LBA for 48-bit Address feature set

Table 8: Identify-Drive Information (Continued) (3 of 3)

Word Address	Default Value[1]	Total Bytes	Data Field Type Information
104-127	0000H	48	Reserved
128	xxxxH	2	Security Status
129-159	0000H	62	Vendor unique bytes
160-216	0000H	114	Reserved
217	0001H	2	Nominal media rotation rate of the device
218-254	0000H	74	Reserved
255	bbA5H	2	Integrity word [15-8 Checksum, 7-0 Signature (A5H)]

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1. xxxx = Don't care. This field is subject to change by the host or the device.
2. bbbb - default value set by controller. The selections could be user programmable.
3. n - calculated data based on product configuration
4. eeee - the default value is '0000000000'
5. dddd - unique number of each device
6. aaaa - any unique Greenliant firmware revision
7. cccc - default value is "xxxMB NANDrive" or "xxxGB NANDrive" where xxx is the flash drive capacity.
   The user has an option to change the model number during manufacturing.

Word 0: General Configuration

This field informs the host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10 MByte/sec and is not MFM encoded.

Word 1: Default Number of Cylinders

This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

Word 3: Default Number of Heads

This field contains the number of translated heads in the default translation mode.

Word 6: Default Number of Sectors per Track

This field contains the number of sectors per track in the default translation mode.

Word 7-8: Number of Sectors

This field contains the number of sectors per NANDrive. This double word value is also the first invalid address in LBA translation mode. This field is only required by CF feature set support.

Word 10-19: Serial Number

The contents of this field are right justified and padded with spaces (20H). The right-most ten bytes are a Greenliant preset, unique ID. The left-most ten bytes are a user-programmable value with a default value of 0000000000.

Word 23-26: Firmware Revision

This field contains the revision of the firmware for this product.

Word 27-46: Model Number

This field is reserved for the model number for this product.

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Word 47: Read-/Write-Multiple Sector Count

This field contains the maximum number of sectors that can be read or written per interrupt using the Read-Multiple or Write-Multiple commands. Only a value of '1' is supported.

Word 49: Capabilities

Bit	Function
13	Standby Timer 0: forces sleep mode when host is inactive.
11	IORDY Support 1: NANDrive supports PIO Mode-4.
9	LBA support 1: NANDrive supports LBA mode addressing.
8	DMA Support 1: DMA mode is supported.

Word 51: PIO Data Transfer Cycle Timing Mode

This field contains the mode for PIO data transfer. NANDrive supports PIO Mode-4.

Word 53: Translation Parameters Valid

Bit	Function
0	1: words 54-58 are valid and reflect the current number of cylinders, heads and sectors.
1	1: words 64-70 are valid to support PIO Mode-3 and -4.
2	1: words 88 are valid to support Ultra DMA data transfer.

Word 54-56: Current Number of Cylinders, Heads, Sectors/Track

These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

Word 57-58: Current Capacity

This field contains the product of the current cylinders times heads times sectors.

Word 59: Multiple Sector Setting

This field contains a validity flag in the Odd Byte and the current number of sectors that can be transferred per interrupt for Read/Write Multiple in the Even Byte. The Odd Byte is always 01H which indicates that the Even Byte is always valid.

The Even Byte value depends on the value set by the Set Multiple command. The Even Byte of this word by default contains a 00H which indicates that Read/Write Multiple commands are not valid.

Word 60-61: Total Sectors Addressable in LBA Mode

This field contains the number of sectors addressable for the NANDrive in LBA mode only.

Word 63: Multi-word DMA Transfer Mode

This field identifies the multi-word DMA transfer modes supported by the NANDrive and indicates the mode that is currently selected. Only one DMA mode can be selected at any given time.

Bit	Function

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15-11	Reserved
10	Multi-word DMA mode 2 selected 1: Multi-word DMA mode 2 is selected and bits 8 and 9 are cleared to 0 0: Multi-word DMA mode 2 is not selected.
9	Multi-word DMA mode 1 selected 1: Multi-word DMA mode 1 is selected and 8 and 10 should be cleared to 0. 0: Multi-word DMA mode 1 is not selected.
8	Multi-word DMA mode 0 selected 1: Multi-word DMA mode 0 is selected and bits 9 and 10 are cleared to 0. 0: Multi-word DMA mode 0 is not selected.
7-3	Reserved
2	Multi-word DMA mode 2 supported 1: Multi-word DMA mode 2 and below are supported and Bits 0 and 1 are set to 1.
1	Multi-word DMA mode 1 supported 1: Multi-word DMA mode 1 and below are supported.
0	Multi-word DMA mode 0 supported 1: Multi-word DMA mode 0 is supported.

Word 64: Advanced PIO Data Transfer Mode

Bits [7:0] is defined as the PIO data and register transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the PIO modes the device is capable of supporting. Of these bits, bits [7:2] are Reserved for future PIO modes.

Bit	Function
0	1: NANDrive supports PIO Mode-3.
1	1: NANDrive supports PIO Mode-4.

Word 65: Minimum Multi-word DMA Transfer Cycle Time Per Word

This field defines the minimum Multi-word DMA transfer cycle time per word. This field defines, in nanoseconds, the minimum cycle time that the NANDrive supports when performing Multi-word DMA transfers on a per word basis. NANDrive supports up to Multi-word DMA Mode-2, so this field is set to 120ns.

Note: NANDrive is capable of supporting Multi-word DMA Mode-4 cycle time of 80ns (0050H). Contact Greenliant sales for more details.

Word 66: Device Recommended Multi-word DMA Cycle Time

This field defines the NANDrive recommended Multi-word DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE DMA command for any location on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the NANDrive may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result. NANDrive supports Multi-word DMA Mode-2, so this field is set to 120ns.

Note: NANDrive is capable of supporting Multi-word DMA Mode-4 cycle time of 80ns (0050H). Contact Greenliant sales for more details.

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Word 67: Minimum PIO Transfer Cycle Time Without Flow Control

This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one.NANDrive supports PIO Mode-4, so this field is set to 120ns.

Note: NANDrive is capable of supporting PIO Mode-6 cycle time of 80ns (0050H). Contact Greenliant sales for more details.

Word 68: Minimum PIO Transfer Cycle Time With IORDY

This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data transfers while utilizing IORDY flow control. If this field is supported, Bit 1 of word 53 shall be set to one. NANDrive supports PIO Mode-4, so this field is set to 120ns.

Note: NANDrive is capable of supporting PIO Mode-6 cycle time of 80ns (0050H). Contact Greenliant sales for more details.

Word 80: Major Version Number

If not 0000H or FFFFH, the device claims compliance with the major version(s) as indicated by bits [6:1] being set to one. Since ATA standards maintain downward compatibility, a device may set more than one bit. GLS85LP1008B supports ATA-1 to ATA-7.

Word 81: Minor Version Number

If an implementer claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to the ATA-3 standard, word 81 should be 0000H or FFFFH.

A value of 0021H reported in word 81 indicates ATA-7 T13/1532D volume 1, revision 4b guided the implementation.

Words 82-84: Features/command sets supported

Words 82, 83, and 84 indicate the features and command sets supported. A value of 706BH is reported.

Word 82

Bit	Function
15	0: Obsolete
14	1: NOP command is supported
13	1: Read Buffer command is supported
12	1: Write Buffer command is supported
11	0: Obsolete
10	0: Host Protected Area feature set is not supported
9	0: Device Reset command is not supported
8	0: Service interrupt is not supported
7	0: Release interrupt is not supported
6	1: Look-ahead is supported
5	1: Write cache is supported
4	0: Packet Command feature set is not supported

3	1: Power Management feature set is supported
2	0: Removable Media feature set is not supported
1	1: Security Mode feature set is supported
0	1: SMART feature set is supported

Word 83

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are not valid
14	1: Provides indication that the features/command sets supported words are valid
13	1: Flush Cache Ext command supported
12	1: Mandatory Flush Cache command supported
11	0: Device Configuration Overlay feature set not supported
10	1: 48-bit Address feature set supported
9	0: Reserved
8	0: Set-Max security extension is not supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not supported
3	1: Advanced Power Management feature set is supported. However, it is No Operation (NOP) and word 91 will always return 0000H.
2	0: CFA feature set is not supported
1	0: Read DMA Queued and Write DMA Queued commands are not supported
0	0: Download Microcode command is not supported

Word 84

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are valid
14	1: Provides indication that the features/command sets supported words are valid
13-0	0: Reserved

Words 85-87: Features/command sets enabled

Words 85, 86, and 87 indicate features/command sets enabled.
The host can enable/disable the features or command set only if they are supported in Words 82-84.

Word 85

Bit	Function
15	0: Obsolete
14	0: NOP command is not enabled 1: NOP command is enabled
13	0: Read Buffer command is not enabled 1: Read Buffer command is enabled

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12	0:Write Buffer command is not enabled
	1: Write Buffer command is enabled
11	0: Obsolete
10	1: Host Protected Area feature set is enabled
9	0: Device Reset command is not enabled
8	0: Service interrupt is not enabled
7	0: Release interrupt is not enabled
6	0: Look-ahead is not enabled
	1: Look-ahead is enabled
5	0: Write cache is not enabled
	1: Write cache is enabled
4	0: Packet Command feature set is not enabled
3	0: Power Management feature set is not enabled
	1: Power Management feature set is enabled
2	0: Removable Media feature set is not enabled
1	0: Security Mode feature set has not been enabled via the Security Set Password command
	1: Security Mode feature set has been enabled via the Security Set Password command
0	0: SMART feature set is not enabled

Word 86

Bit	Function
15-14	0: Reserved
13	1: Flush Cache Ext command supported
12	1: Mandatory Flush Cache command supported
11	0: Device Configuration Overlay feature set not supported
10	1: 48-bit Address feature set supported
9	0: Reserved
8	1: Set-Max security extension supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not enabled
3	0: Advanced Power Management feature set is not enabled
2	0: CFA feature set is disabled
1	0: Read DMA Queued and Write DMA Queued commands are not enabled
0	0: Download Microcode command is not enabled

Word 87

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are valid
14	1: Provides indication that the features/command sets supported words are valid
13-0	0: Reserved

Word 88

Bit	Function
15	Reserved
14	1: Ultra DMA mode 6 is selected
	0: Ultra DMA mode 6 is not selected
13	1: Ultra DMA mode 5 is selected
	0: Ultra DMA mode 5 is not selected
12	1: Ultra DMA mode 4 is selected
	0: Ultra DMA mode 4 is not selected
11	1: Ultra DMA mode 3 is selected
	0: Ultra DMA mode 3 is not selected
10	1: Ultra DMA mode 2 is selected
	0: Ultra DMA mode 2 is not selected
9	1: Ultra DMA mode 1 is selected
	0: Ultra DMA mode 1 is not selected
8	1: Ultra DMA mode 0 is selected
	0: Ultra DMA mode 0 is not selected
7	Reserved
6	1: Ultra DMA mode 6 and below supported
5	1: Ultra DMA mode 5 and below supported
4	1: Ultra DMA mode 4 and below are supported
3	1: Ultra DMA mode 3 and below are supported
2	1: Ultra DMA mode 2 and below are supported
1	1: Ultra DMA mode 1 and below are supported
0	1: Ultra DMA mode 0 is supported

Word 89: Time required for Security erase unit completion

Word 89 specifies the time required for the Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

Word 90: Time required for Enhanced security erase unit completion

Word 90 specifies the time required for the Enhanced Security Erase Unit command to complete.

Value	Time
0	Value not specified
1-254	(Value * 2) minutes
255	>508 minutes

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Word 93: Hardware reset result

Bit   Function

The contents of bits [12:0] of this word will change only during the execution of the hardware reset.

15   Shall be cleared to zero

14   Shall be set to one

13   1: Device detected CBLID - above VIH

        0: Device detected CBLIP - below VIL

12-8   Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows:

        12   Reserved.

        11   0: Device 1 did not assert PDIAG-.

                    1: Device 1 asserted PDIAG-.

        10-9   These bits indicate how Device 1 determined the device number:

                    00: Reserved.

                    01: A jumper was used.

                    10: The CSEL signal was used.

                    11: Some other method was used or the method is unknown.

        8   Shall be set to one.

7-0   Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows:

        7   Reserved.

        6   0: Device 0 does not respond when Device 1 is selected.

                    1: Device 0 responds when Device 1 is selected.

        5   0: Device 0 did not detect the assertion of DASP-.

                    1: Device 0 detected the assertion of DASP-.

        4   0: Device 0 did not detect the assertion of PDIAG-.

                    1: Device 0 detected the assertion of PDIAG-.

        3   0: Device 0 failed diagnostics.

                    1: Device 0 passed diagnostics.

        2-1   These bits indicate how Device 0 determined the device number:

                    00: Reserved.

                    01: A jumper was used.

                    10: The CSEL signal was used.

                    11: Some other method was used or the method is unknown.

        0   Shall be set to one.

Word 128: Security Status

Bit   Function

8   Security Level

        1: Security mode is enabled and the security level is maximum

        0: and security mode is enabled, indicates that the security level is high

5   Enhanced security erase unit feature supported

        1: Enhanced security erase unit feature set is supported

4	Expire
	1: Security count has expired and Security Unlock and Security Erase Unit are command aborted until a Power-on reset or hard reset
3	Freeze
	1: Security is frozen
2	Lock
	1: Security is locked
1	Enable/Disable
	1: Security is enabled
	0: Security is disabled
0	Capability
	1: NANDrive supports security mode feature set
	0: NANDrive does not support security mode feature set

Word 217: Nominal Media Rotation Rate

Word 217 indicates the nominal media rotation rate of the device. For NANDrive, the value is always 0001H for this field to indicate non-rotating media.

Word 255: Integrity Word

Word 255 is optional. When bits [7:0] of this word contain the signature A5h, bits [15:8] contain the data-structure checksum. The data-structure checksum value is the two's complement of the sum of all bytes in words [254:0] and the byte consisting of bits [7:0] in word 255. Add each byte with unsigned arithmetic, and ignore overflow. When the checksum is correct, the sum of all 512 bytes is zero.

Set-Features - EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command is used by the host to establish or select certain features. Table 9 defines all features that are supported.

Table 9: Features Supported

Feature	Operation
01H	Enable 8-bit data transfers.
02H	Enable Write cache
03H	Set transfer mode based on value in Sector Count register. Table 10 defines the values.
05H	Enable Advanced Power Management
09H	Enable Extended Power Operations
55H	Disable Read Look Ahead.

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Table 9: Features Supported

Feature	Operation
66H	Disable Power-on Reset (POR) establishment of defaults at software reset.
69H	NOP - Accepted for backward compatibility.
81H	Disable 8-bit data transfer.
82H	Disable Write Cache
85H	Disable Advanced Power Management
89H	Disable Extended Power operations
96H	NOP - Accepted for backward compatibility.
97H	Accepted for backward compatibility. Use of this Feature is not recommended.
AAH	Enable Read-Look-Ahead
CCH	Enable Power-on Reset (POR) establishment of defaults at software reset.

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Features 01H and 81H are used to enable and clear 8-bit data transfer mode. If the 01H feature command is issued all data transfers will occur on the low order D_7-D_0 data bus and the IOCS16# signal will not be asserted for data register accesses.

Features 02H and 82H allow the host to enable or disable write cache in the NANDrives that implement write cache. When the subcommand Disable-Write-Cache is issued, the NANDrive should initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03H allows the host to select the transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode is selected at all times. The host may change the selected modes by the Set-Features command.

Feature 55H is the default feature for the NANDrive. Therefore, the host does not have to issue Set-Features command with this feature unless it is necessary for compatibility reasons.

Features 66H and CCH can be used to enable and disable whether the Power-on Reset (POR) Defaults will be set when a software reset occurs.

Table 10: Transfer Mode Values

Mode	Bits [7:3]	Bits [2:0]
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode[1]
Multi-word DMA mode	00100b	mode[1]
Ultra-DMA mode	01000b	mode[1]
Reserved	Other	N/A

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1. Mode = transfer mode number, all other values are not valid

Idle - 97H or E3H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97H or E3H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							

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Bit ->	7	6	5	4	3	2	1	0
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

This command causes the NANDrive to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic Power-down mode is enabled. If the sector count is zero, the automatic Power-down mode is also enabled, the timer count is set to 3, with each count being 5 ms. Note that this time base (5 msec) is different from the ATA specification.

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Set-Sleep-Mode - 99H or E6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	99H or E6H							
C/D/H (6)		X		Drive		X		
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the NANDrive to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 15 milliseconds.

Set-WP#/PD#-Mode - 8BH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	8BH							
C/D/H (6)		X		Drive		X		
Cyl High (5)	6EH							
Cyl Low (4)	44H							
Sec Num (3)	72H							
Sec Cnt (2)	50H							
Feature (1)	55H or AAH							

This command configures the WP#/PD# pin for either the Write Protect mode or the Power-down mode. When the host sends this command to the device with the value AAH in the feature register, the WP#/PD# pin is configured for the Write Protect mode. The Write Protect mode is the factory default setting. When the host sends this command to the device with the value 55H in the feature register, WP#/PD# is configured for the Power-down mode.

All values in the C/D/H register, the Cylinder Low register, the Cylinder High register, the Sector Number register, the Sector Count register, and the Feature register need to match the values shown above, otherwise, the command will be treated as an invalid command.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

Error Posting

The following table summarizes the valid status and error values for the NANDrive command set.

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Table 11: Error and Status Register[1]

Command	ICRC/BBK	UNC	IDNF	ABRT	AMNF	RDY	DWF	DSC	CORR	ERR
Check-Power-Mode				V		V	V	V		V
Execute-Drive-Diagnostic[2]						V		V		V
Flush-Cache				V		V	V	V		V
Flush-Cache-EXT				V		V	V	V		V
Identify-Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle-Immediate				V		V	V	V		V
Initialize-Drive-Parameters						V		V		V
NOP				V		V	V			V
Read-Buffer				V		V	V	V		V
Read-DMA	V	V	V	V	V	V	V	V	V	V
Read-DMA-EXT	V	V	V	V	V	V	V	V	V	V
Read-Multiple	V	V	V	V	V	V	V	V	V	V
Read-Multiple-EXT	V	V	V	V	V	V	V	V	V	V
Read-Sector(s)	V	V	V	V	V	V	V	V	V	V
Read-Sector(s)-EXT	V	V	V	V	V	V	V	V	V	V
Read-Verify-Sector(s)	V	V	V	V	V	V	V	V	V	V
Read-Verify-Sector(s)-EXT	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Security-Disable-Password				V		V	V	V		V
Security-Erase-Prepare				V		V	V	V		V
Security-Erase-Unit				V		V	V	V		V
Security-Freeze-Lock				V		V	V	V		V
Security-Set-Password				V		V	V	V		V
Security-Unlock				V		V	V	V		V
Seek			V	V		V	V	V		V
Set-Features				V		V	V	V		V
Set-Multiple-Mode				V		V	V	V		V
Set-Sleep-Mode				V		V	V	V		V
Set-WP#/PD#-Mode				V		V		V		V
SMART				V		V		V		V
Standby				V		V	V	V		V
Standby-Immediate				V		V	V	V		V
Write-Buffer				V		V	V	V		V
Write-DMA	V		V	V	V	V	V	V		V
Write-DMA-EXT	V		V	V	V	V	V	V		V
Write-Multiple	V		V	V	V	V	V	V		V
Write-Multiple-EXT	V		V	V	V	V	V	V		V
Write-Sector(s)	V		V	V	V	V	V	V		V
Write-Sector(s)-EXT	V		V	V	V	V	V	V		V
Write-Verify	V		V	V	V	V	V	V		V
Invalid-Command-Code				V		V	V	V		V

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1. The host is required to reissue any media access command (such as Read-Sector and Write Sector) that ends with an error condition.
2. See Table 8

V = valid on this command.

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Electrical Specifications

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Storage Temperature . . . . -55°C to +125°C

D.C. Voltage on Pins[1] I1, I2, O2, O3, and O4 to Ground Potential . . . . -0.5V to V_{DD}+0.5V

Transient Voltage (<20 ns) on Pins[1] I1, I2, O2, O3, and O4 to Ground Potential . . . . -2.0V to V_{DD}+2.0V

Package Power Dissipation Capability (T_A = 25°C) 1.0W

Surface Mount Solder Reflow Temperature . . . . 260°C for 10 seconds

Output Short Circuit Current[2] . . . . .60 mA

1. Refer to Table 1 for pin assignment information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

Table 12: Absolute Maximum Power Pin Stress Ratings

Parameter	Symbol	Conditions
Input Power	V_{DD}	-0.3V min to 4.0V max
Voltage on all other pins with respect to V_{SS}		-0.5V min to V_{DD} + 0.5V max

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Table 13: Operating Range

Range	Ambient Temperature	V_{DD}	
		3.3V	
		Min	Max
Commercial	0°C to +70°C	3.135V	3.465V

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Table 14: AC Conditions of Test[1]

Input Rise/Fall Time	Output Load
5 ns	C_L = 100 pF

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1. See Figure 4

Table 15: Recommended System Power-on Timing

Symbol	Parameter	Typical	Maximum	Units
$T_{PU-INITIAL}$	Drive Initialization to Ready	7	50	sec
$T_{PU-READY1}$[1]	Host Power-on/Reset to Ready Operation	700	2000	ms
$T_{PU-WRITE1}$[1]	Host Power-on/Reset to Write Operation	700	2000	ms

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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Table 16: Capacitance (Ta = 25°C, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	15 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	9 pF

T16.1 1421

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 17: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

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DC Characteristics

Table 18: DC Characteristics for Host Interface

Symbol	Type	Parameter	Min	Max	Units	Conditions
V_{IH1}	I1	Input Voltage	2		V	$V_{DD}=V_{DD}$ Max
V_{IL1}				0.8	V	$V_{DD}=V_{DD}$ Min
I_{IL1}	I1Z	Input Leakage Current	-10	10	µA	$V_I =V_{DD}$ Max or 0V
I_{D1}	I1D	Input Pull-Down Current	20	120	µA	$V_{DD}=V_{DD}$ Max, $V_{IN} = V_{DD}$ Max
I_{U1}	I1U	Input Pull-Up Current	-120	-20	µA	$V_{DD}=V_{DD}$ Max, $V_{IN} = GND$
V_{T+}	I2	Input Voltage Schmitt Trigger		1.75	V	$V_{DD} = V_{DD}$ Max
V_{T-}			1.09		V	$V_{DD} = V_{DD}$ Min
I_{IL2}	I2Z	Input Leakage Current	-10	10	µA	$V_I = V_{DD}$ Max or 0V
I_{U2}	I2U	Input Pull-Up Current	-120	-20	µA	$V_{DD}=V_{DD}$ Max, $V_{IN} = GND$
V_{OH2}	O2	Output Voltage	2.4		V	$I_{OH2}=I_{OH2}$ Min
V_{OL2}				0.4	V	$I_{OL2}=I_{OL2}$ Max
I_{OH2}		Output Current	-4		mA	$V_{DD}=V_{DD}$ Min
I_{OL2}				4	mA	$V_{DD}=V_{DD}$ Min
V_{OH3}	O3	Output Voltage	2.4		V	$I_{OH3}=I_{OH3}$ Min
V_{OL3}				0.4	V	$I_{OL3}=I_{OL3}$ Max
I_{OH3}		Output Current	-8		mA	$V_{DD}=V_{DD}$ Min
I_{OL3}				8	mA	$V_{DD}=V_{DD}$ Min
V_{OH4}	O4	Output Voltage	2.4		V	$I_{OH4}=I_{OH4}$ Min
V_{OL4}				0.4	V	$I_{OL4}=I_{OL4}$ Max
I_{OH4}		Output Current	-12		mA	$V_{DD}=V_{DD}$ Min
I_{OL4}				8	mA	$V_{DD}=V_{DD}$ Min

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Table 19: Power Consumption

Symbol	Type	Device	Parameter	Min	Max	Units	Conditions
I_{DD}[1,2]	PWR	GLS85LP1008B	Power supply current (T_A = 0°C to +70°C)		230	mA	$V_{DD}=V_{DD}$ Max
I_{SP}	PWR	GLS85LP1008B	Sleep/Standby/Idle current (T_A = 0°C to +70°C)		3.3	mA	$V_{DD}=V_{DD}$ Max

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1. Sequential data transfer from host interface and write data to media.
2. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
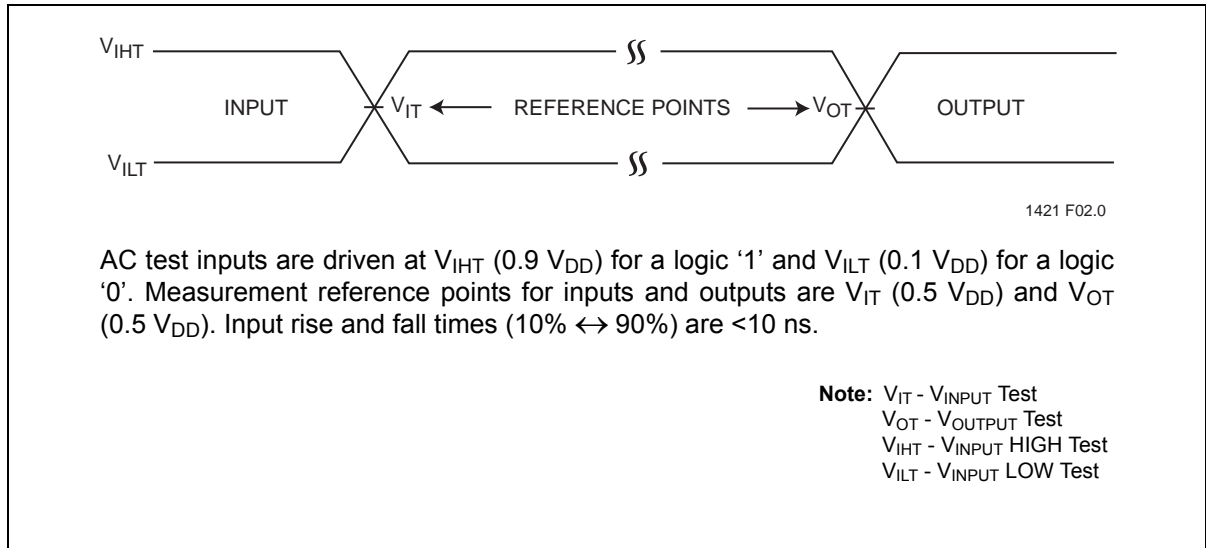
AC Characteristics

AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic '1' and V_{ILT} (0.1 V_{DD}) for a logic '0'. Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

Figure 4: AC Input/Output Reference Waveforms

Appendix

Differences Between the Greenliant NANDrive and ATA Specifications

Idle Timer

The Idle timer uses an incremental value of 5 ms, rather than the 5 sec minimum increment value specified in ATA specifications.

Recovery from Sleep Mode

For NANDrive devices, recovery from sleep mode is accomplished by simply issuing another command to the device. A hardware or software reset is not required.

Advance Information

Product Ordering Information

GLS **85 LP 1 008B - M - C - LFTE**
XX XX X XXXX - X - X - XXXX

Environmental Attribute
E[1] = non-Pb

Package Modifier
T = 88 ball positions (nearest letter code to total ball count of 91)

Package Type
LF= LBGA

Operation Temperature
C = Commercial: 0°C to +70°C

NAND Type
M = MLC

Version
B = 2nd Version

Capacity
008 = 8 GByte

MByte or GByte Designator
1 = GByte

Interface
P= Parallel ATA/IDE Interface

Voltage
L = 3.3V

Product Series
85 = NANDrive

1. Environmental suffix "E" denotes non-Pb solder. Greenliant non-Pb solder devices are "RoHS Compliant".

Valid Combinations

GLS85LP1008B-M-C-LFTE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Greenliant sales representative to confirm availability of valid combinations and to determine availability of new combinations.
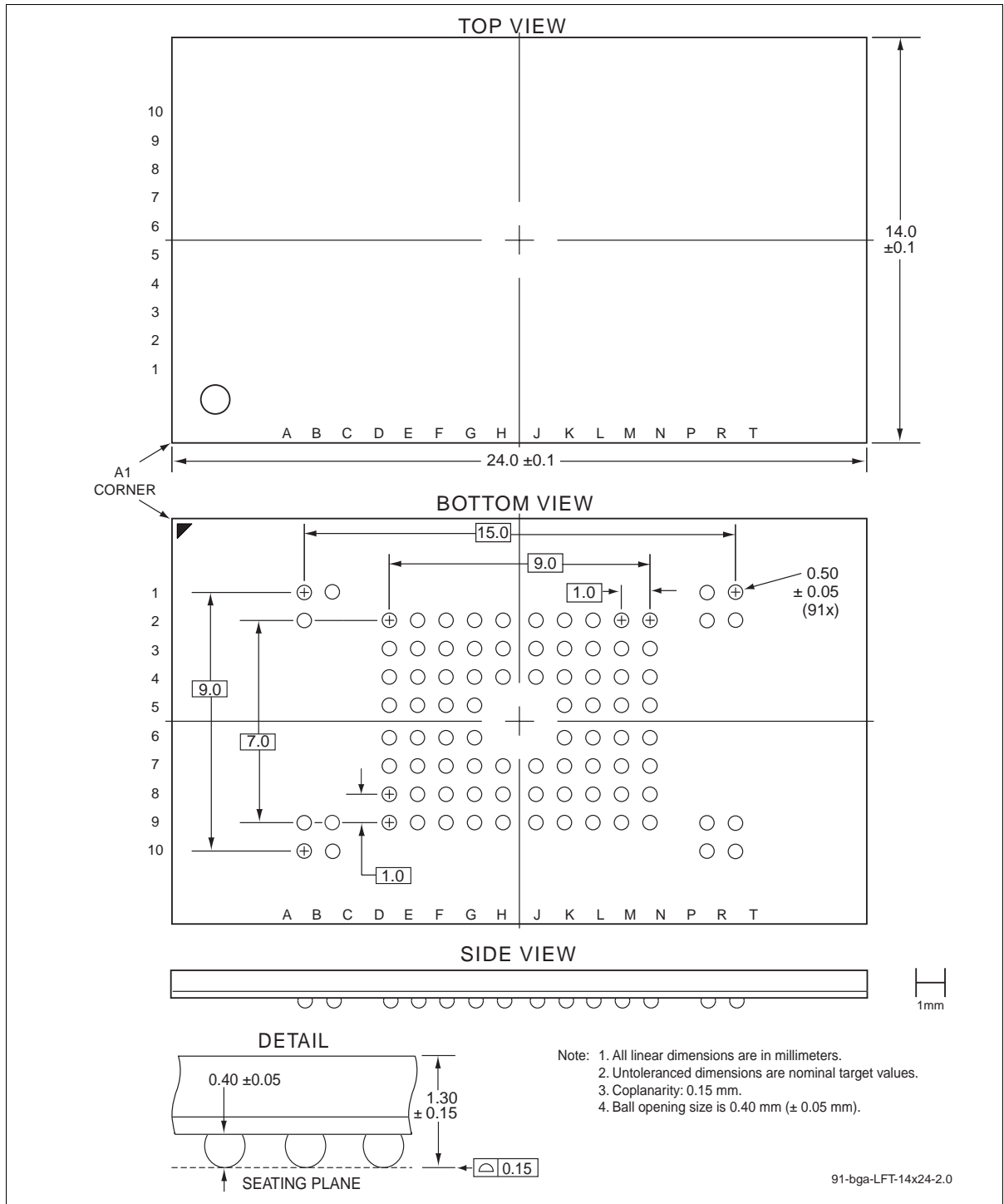
Packaging Diagram

TOP VIEW

14.0 ±0.1

A B C D E F G H J K L M N P R T

24.0 ±0.1

A1 CORNER

BOTTOM VIEW

15.0

9.0

1.0

0.50 ± 0.05 (91x)

9.0

7.0

1.0

A B C D E F G H J K L M N P R T

SIDE VIEW

1mm

DETAIL

0.40 ±0.05

1.30 ± 0.15

0.15

SEATING PLANE

Note: 1. All linear dimensions are in millimeters.
2. Untoleranced dimensions are nominal target values.
3. Coplanarity: 0.15 mm.
4. Ball opening size is 0.40 mm (± 0.05 mm).

91-bga-LFT-14x24-2.0

Figure 5: NANDrive 91-Ball, Low-profile Ball Grid Array (LBGA)
Greenliant Package Code: LFT

Advance Information

Table 20: Revision History

Number	Description	Date
00	• Initial release of S71421 for SST85LP1008B.	Jan 2010
01	• Updated "Features" • Minor revision to "General Description" on page 3 • Revised Figure 2 on page 6 and Table 1 on page 7 • Updated Tables 3, 5, 8, 9, 12, 13, 15, 18, and 19 • Modified "NANDrive Command Description", starting on page 12 • Updated "Absolute Maximum Stress Ratings" on page 28 • Updated Figure 5. • Applied new copyright notice and address on page 36.	Apr 2010
02	• Transferred from SST to Greenliant	May 2010