LatticeECP2 Family Data Sheet

Version 01.0, February 2006

LatticeECP2 Family Data Sheet Introduction

February 2006 **Advance Data Sheet**

Features

- **High Logic Density for System Integration**
  - 6K to 68K LUTs
  - 192 to 628 I/Os
- **sysDSP™ Block**
  - 3 to 22 blocks for high performance multiply and accumulate
  - 12 to 88 18x18 multipliers
  - Each block supports
    - One 36x36 multiplier or four 18X18 or eight 9X9 multipliers
- **Flexible Memory Resources**
  - 55Kbits to 1032Kbits sysMEM™ Embedded Block RAM (EBR) 18-Kbit block
    - Single, pseudo dual and true dual port
  - 12K to 136Kbits distributed RAM
    - Single port and pseudo dual port
- **sysCLOCK Analog PLLs And DLLs**
  - Two GPLLs and up to four SPLLs per device
    - Clock multiply, divide, phase adjust and delay adjust
  - Two general purpose DLLs per device
- **Pre-Engineered Source Synchronous I/O**
  - Dedicated DQS support
  - DDR registers in I/O cells
  - Dedicated gearing logic
  - Source synchronous standards support
    - SPI4.2, SFI4, XGMII
    - High Speed ADC/DAC devices
  - Dedicated DDR and DDR2 memory support
    - DDR1 400 (200MHz)
    - DDR2 400 (200MHz)
- **Programmable sysIO™ Buffer Supports Wide Range Of Interfaces**
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 3/2/18 I, II
  - HSTL15 I and HSTL18 I, II
  - PCI and Differential HSTL, SSTL
  - LVDS, RSDS, Bus-LVDS, MLVDS, LVPECL
- **Flexible Device Configuration**
  - 1149.1 Boundary Scan compliant
  - Dedicated bank for configuration for I/Os
  - SPI boot flash interface
  - Dual boot images supported
  - Encrypted bit stream support
  - TransFR™ I/O for simple field updates
  - Optional Soft Error Detect macro embedded
- **Optional Bitstream Encryption**
- **System Level Support**
  - ispTRACY™ internal logic analyzer capability
  - Onboard oscillator for initialization and general use
  - 1.2V power supply

Table 1. LatticeECP2 Family Selection Guide

Device	ECP2-6	ECP2-12	ECP2-20	ECP2-35	ECP2-50	ECP2-70
LUTs (K)	6	12	21	32	48	68
Distributed RAM (Kbits)	12	24	42	64	96	136
EBR SRAM (Kbits)	55	221	276	332	387	1032
EBR SRAM Blocks	3	12	15	18	21	56
sysDSP Blocks	3	6	7	8	18	22
18x18 Multipliers	12	24	28	32	72	88
GPLL + SPLL + GDLL	2+0+2	2+0+2	2+0+2	2+0+2	2+2+2	2+4+2
Maximum Available I/O	192	297	363	452	500	628
Packages and I/O Combinations						
144-pin TQFP (20 x 20 mm)	95	95				
208-pin PQFP (28 x 28 mm)		127	127			
256-ball fpBGA (17 x 17 mm)	192	192	192			
484-ball fpBGA (23 x 23 mm)		297	332	332	339	
672-ball fpBGA (27 x 27 mm)			363	452	500	500
900-ball fpBGA (31 x 31 mm)						628

Introduction

The LatticeECP2 family of FPGA devices has been optimized to deliver high performance features such as advanced DSP blocks and high speed source synchronous interfaces in an economical FPGA fabric. This combination was achieved through advances in device architecture and the use of 90nm technology.

The LatticeECP2 FPGA fabric was optimized for the new technology from the outset with high performance low cost in mind. The LatticeECP2 devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP blocks and advanced configuration support, including encryption and dual-boot capabilities.

The ispLEVER® design tool from Lattice allows large complex designs to be efficiently implemented using the LatticeECP2 family of FPGA devices. Synthesis library support for LatticeECP2 is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP2 device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP2 family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

LatticeECP2 Family Data Sheet Architecture

February 2006 **Advance Data Sheet**

Architecture Overview

Each LatticeECP2 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and rows of sysDSP™ Digital Signal Processing blocks as shown in Figure 2-1.

There are two kinds of logic blocks, the Programmable Functional Unit (PFU) and Programmable Functional Unit without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

The LatticeECP2 family of devices contain up to two rows of sysMEM EBR blocks. sysMEM EBRs are large dedicated 18K fast memory blocks. Each sysMEM block can be configured in variety of depths and widths of RAM or ROM. In addition, LatticeECP2 devices contain up to two rows of DSP Blocks. Each DSP block has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities

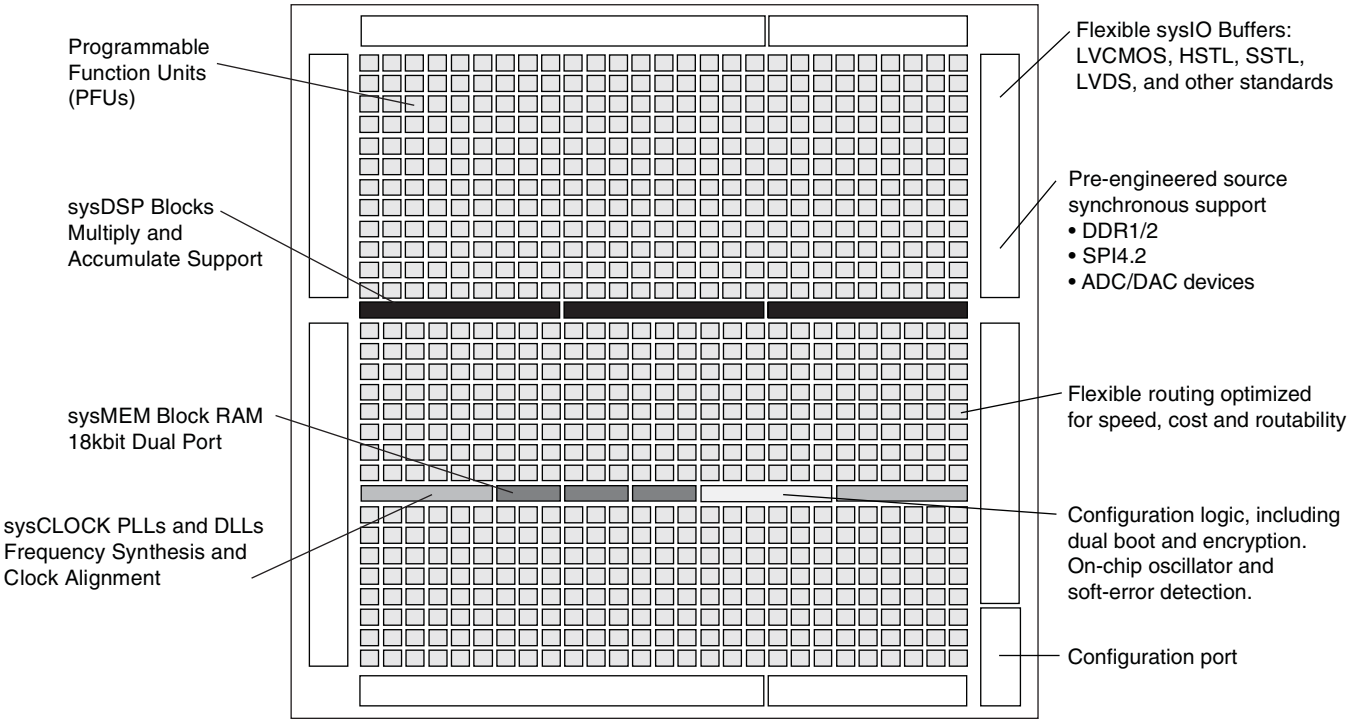
Each PIC block encompasses two PIOs (PIO pairs) with their respective sysIO buffers. The sysIO buffers of the LatticeECP2 devices are arranged into eight banks, allowing the implementation of a wide variety of I/O standards. In addition, a separate I/O bank is provided for the programming interfaces. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of the high speed source synchronous standards such as SPI4.2 along with memory interfaces including DDR2.

Other blocks provided include PLLs, DLLs and configuration functions. The LatticeECP2 architecture provides two General PLLs (GPLL) and up to four Standard PLLs (SPLL) per device. In addition, each LatticeECP2 family member provides two DLLs per device. The GPLLs and DLLs blocks are located in pairs at the end of the bottom-most EBR row; the DLL block located towards the edge of the device. The SPLL blocks are located at the end of the other EBR/DSP rows.

The configuration block that supports features such as configuration bit-stream de-encryption, transparent updates and dual boot support is located toward the center of this EBR row. Every device in the LatticeECP2 family supports a sysCONFIG™ port located in the corner between banks four and five, which allows for serial or parallel device configuration.

In addition, every device in the family has a JTAG port. This family also provides an on-chip oscillator and soft error detect capability. The LatticeECP2 devices use 1.2V as their core voltage.

Figure 2-1. Simplified Block Diagram, ECP2-6 Device (Top Level)

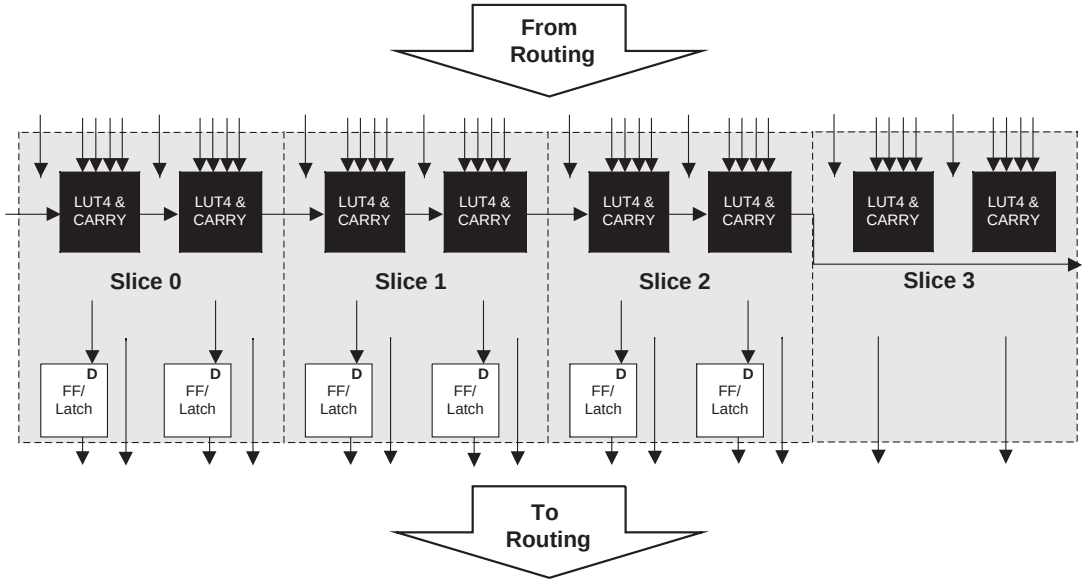


PFU Blocks

The core of the LatticeECP2 device consists of PFU blocks which are provided in two forms, the PFU and PFF. The PFUs can be programmed to perform Logic, Arithmetic, Distributed RAM and Distributed ROM functions. PFF blocks can be programmed to perform Logic, Arithmetic and ROM functions. Except where necessary, the remainder of this data sheet will use the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered 0-3 as shown in Figure 2-2. All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

Figure 2-2. PFU Diagram



Slice

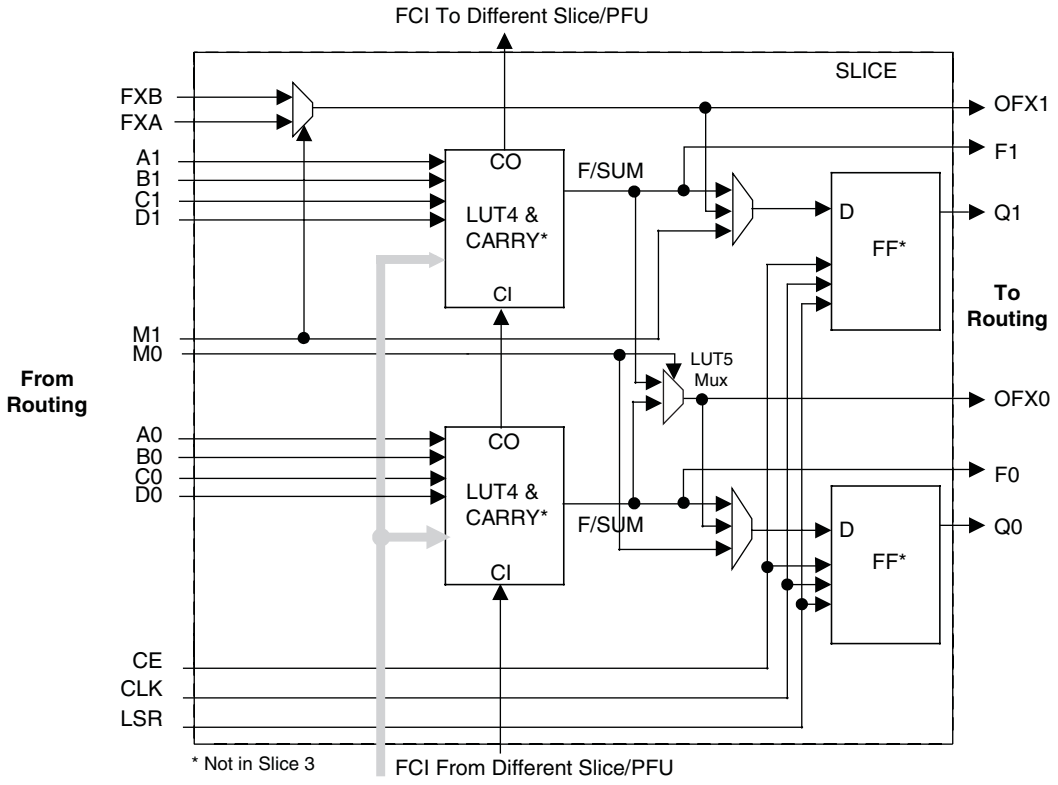
Slice 0 through Slice 2 contain two LUT4s feeding two registers, whereas Slice 3 contains two LUT4s only. For PFUs, Slice 0 and Slice 2 can also be configured as distributed memory, a capability not available in the PFF. Table 2-1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains some logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2-3 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Table 2-1. Resources and Modes Available per Slice

Slice	PFU BLock		PFF Block	
	Resources	Modes	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM	2 LUT4s and 2 Registers	Logic, Ripple, ROM
Slice 3	2 LUT4s	Logic, ROM	2 LUT4s	Logic, ROM

Slices 0, 1 and 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 13 input signals from routing and four signals to routing. Table 2-2 lists the signals associated with Slice 0 to Slice 2.

Figure 2-3. Slice Diagram



For Slices 0 and 2, memory control signals are generated from Slice 1 as follows:

WCK is CLK
WRE is from LSR
DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data
WAD [A:D] is a 4bit address from slice 1 LUT input

Table 2-2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCIN	Fast Carry-in[1]
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6 and LUT7
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6 and LUT7
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Slice 2 of each PFU is the fast carry chain output[1]

1. See Figure 2-3 for connection details.
2. Requires two PFUs.

Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

Ripple Mode

Ripple mode allows the efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/Subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with Async clear
- Up/Down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
  - A greater-than-or-equal-to B

– A not-equal-to B
– A less-than-or-equal-to B

Two additional signals: Carry Generate and Carry Propagate are generated per slice in this mode, allowing fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit pseudo dual port RAM (PDPR) memory is created by using one slice as the read-write port and the other companion slice as the read-only port.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software will construct these using distributed memory primitives that represent the capabilities of the PFU. Table 2-3 shows the number of slices required to implement different distributed RAM primitives. For more information on using RAM in LatticeECP2 devices, please see details of additional technical documentation at the end of this data sheet.

Table 2-3. Number of Slices Required For Implementing Distributed RAM

	SPR 16X4	PDPR 16X4
Number of slices	3	3

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in the ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

Routing

There are many resources provided in the LatticeECP2 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) and x6 (spans seven PFU). The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered allowing both short and long connections routing between PFUs.

The LatticeECP2 family has an enhanced routing architecture that produces a compact design. The ispLEVER design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

sysCLOCK Phase Locked Loops (GPLL/SPLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All the devices in the LatticeECP2 family support two General Purpose PLLs (GPLLs) which are full-featured PLLs. In addition, some of the larger devices have two to four Standard PLLs (SPLLs) that have a subset of GPLL functionality.

General Purpose PLL (GPLL)

The architecture of the GPLL is shown in Figure 2-4. A description of the GPLL functionality follows.

CLKI is the reference frequency (generated either from the pin or from routing) for the PLL. CLKI feeds into the Input Clock Divider block. The CLKFB is the feedback signal (generated from CLKOP or from a user clock PIN/logic). This signal feeds into the Feedback Divider. The Feedback Divider is used to multiply the reference frequency.

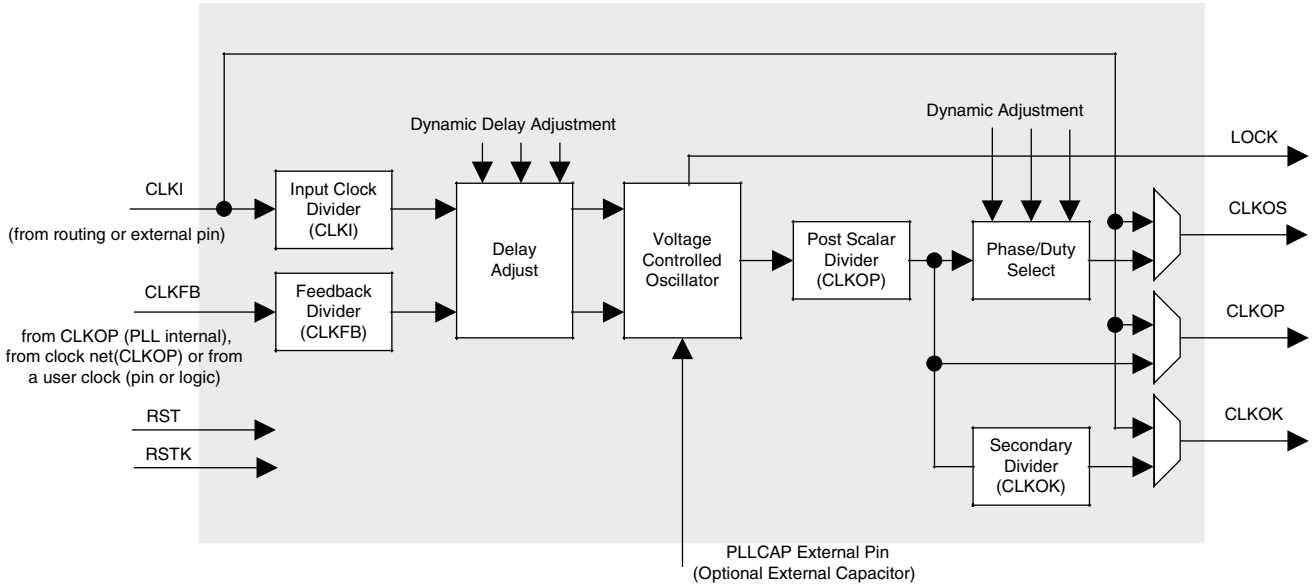
The Delay Adjust Block adjusts either the delays of the reference or feedback signals. The Delay Adjust Block can either be programmed during configuration or can be adjusted dynamically. The setup, hold or clock-to-out times of the device can be improved by programming a delay in the feedback or input path of the PLL which will advance or delay the output clock with reference to the input clock.

Following the Delay Adjust Block, both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. In this block the difference between the input path and feedback signals is used to control the frequency and phase of the oscillator. A LOCK signal is generated by the VCO to indicate that VCO has locked onto the input clock signal. In dynamic mode, the PLL may lose lock after a dynamic delay adjustment and not relock until the t_{LOCK} parameter has been satisfied. LatticeECP2 devices have two dedicated pins on the left and right edges of the device for connecting optional external capacitors to the VCO. This allows the PLLs to operate at a lower frequency. This is a shared resource which can only be used by one PLL (GPLL or SPLL) per side.

The output of the VCO then enters the post-scalar divider. The post-scalar divider allows the VCO to operate at higher frequencies than the clock output (CLKOP), thereby increasing the frequency range. A secondary divider takes the CLKOP signal and uses it to derive lower frequency outputs (CLKOK). The Phase/Duty Select block adjusts the phase and duty cycle of the CLKOP signal and generates the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The primary output from the post scalar divider CLKOP along with the outputs from the secondary divider (CLKOK) and Phase/Duty select (CLKOS) are fed to the clock distribution network.

Figure 2-4. General Purpose PLL (GPLL) Diagram



Standard PLL (SPLL)

Some of the larger devices have two to four Standard PLLs (SPLLs). SPLLs have the same features as GPLLs but without delay adjustment capability. SPLLs also provide different parametric specifications. For more information, please see details of additional technical documentation at the end of this data sheet.

Table 2-4 provides a description of the signals in the GPLL and SPLL blocks.

Table 2-4. GPLL and SPLL Blocks Signal Descriptions

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic)
RST	I	"1" to reset PLL counters, VCO, charge pumps and M-dividers
RSTK	I	"1" to reset K-divider
CLKOS	O	PLL output clock to clock tree (phase shifted/duty cycle changed)
CLKOP	O	PLL output clock to clock tree (no phase shift)
CLKOK	O	PLL output to clock tree through secondary clock divider
LOCK	O	"1" indicates PLL LOCK to CLKI
DDAMODE[1]	I	Dynamic Delay Enable. "1": Pin control (dynamic), "0": Fuse Control (static)
DDAIZR[1]	I	Dynamic Delay Zero. "1": delay = 0, "0": delay = on
DDAILAG[1]	I	Dynamic Delay Lag/Lead. "1": Lead, "0": Lag
DDAIDEL[2:0][1]	I	Dynamic Delay Input
DPA MODES	I	DPA (Dynamic Phase Adjust/Duty Cycle Select) mode
DPHASE [3:0]	I	DPA Phase Adjust inputs
DDDUTY [3:0]	—	DPA Duty Cycle Select inputs

1. These signals are not available in SPLL.

Delay Locked Loops (DLL)

In addition to PLLs, the LatticeECP2 family of devices has two DLLs per device.

CLKI is the input frequency (generated either from the pin or routing) for the DLL. CLKI feeds into the output muxes block to bypass the DLL, directly to the DELAY CHAIN block and (directly or through divider circuit) to the reference input of the Phase Frequency Detector (PFD) input mux. The reference signal for the PFD can also be generated from the Delay Chain and CLKFB signals. The feedback input to the PFD is generated from the CLKFB pin, CLKI or from tapped signal from the Delay chain.

The PFD produces a binary number proportional to the phase and frequency difference between the reference and feedback signals. This binary output of the PFD is feed into a Arithmetic Logic Unit (ALU). Based on these inputs, the ALU determines the correct digital control codes to send to the delay chain in order to better match the reference and feedback signals. This digital code from the ALU is also transmitted via the Digital Control bus (DCNTL) bus to its associated DLL_DEL delay block. The ALUHOLD input allows the user to suspend the ALU output at its current value. The UDDCNTL signal allows the user to latch the current value on the DCNTL bus.

The DLL has two independent clock outputs, CLKOP and CLKOS. These outputs can individually select one of the outputs from the tapped delay line. The CLKOS has optional fine phase shift and divider blocks to allow this output to be further modified, if required. The fine phase shift block allows the CLKOS output to phase shifted a further 45, 22.5 or 11.25 degrees relative to its normal position. Both the CLKOS and CLKOP outputs are available with optional duty cycle correction. Divide by two and divide by four frequencies are available at CLKOS. The LOCK output signal is asserted when the DLL is locked. Figure 2-5 shows the DLL block diagram and Table 2-5 provides a description of the DLL inputs and outputs.

The sysCLOCK DLL is configured at power-up and, if desired, can be reconfigured dynamically through the Serial Memory Interface (SMI) bus. Users can drive the SMI interface from routing using Lattice software tools.

The user can configure the DLL for many common functions such as time reference delay mode and clock injection removal mode. Lattice provides primitives in its design tools for these functions. For more information on the DLL, please see details of additional technical documentation at the end of this data sheet.

Figure 2-5. Delay Locked Loop Diagram (DLL)

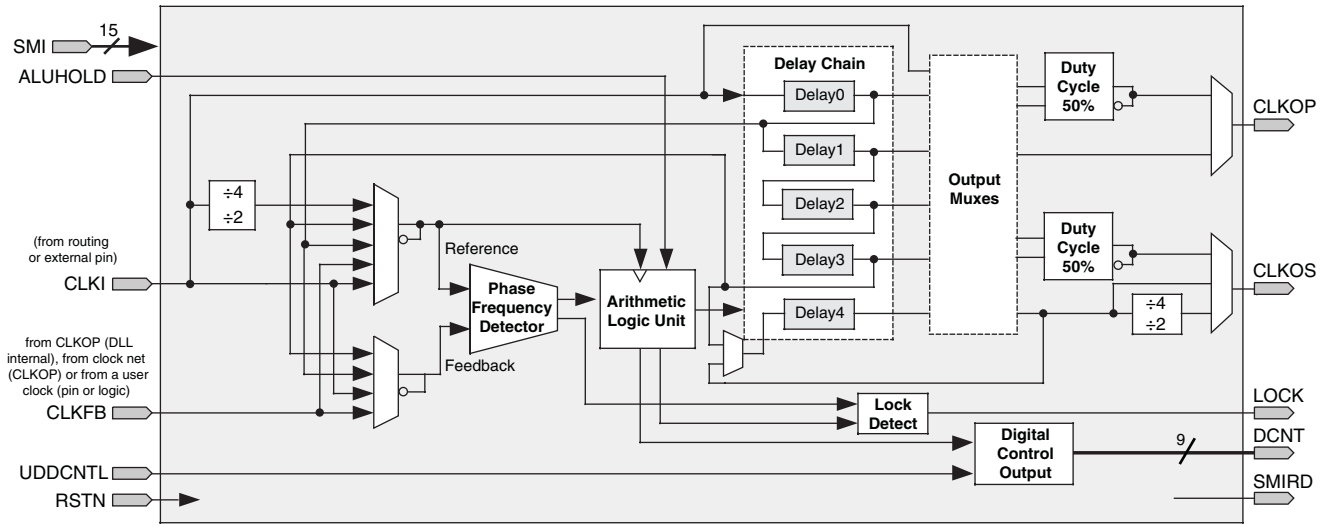


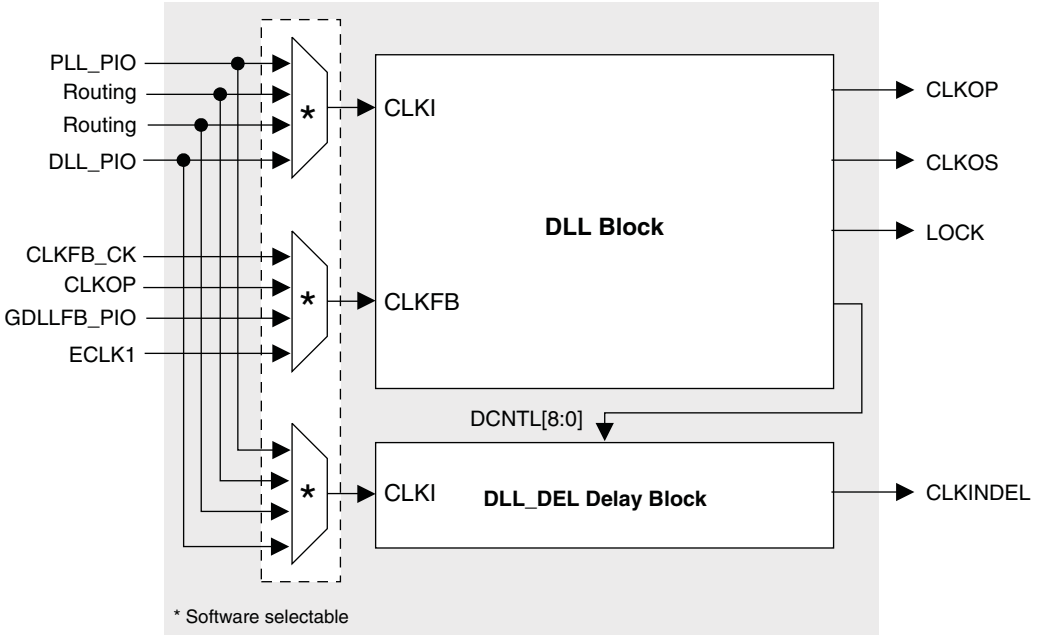
Table 2-5. DLL Signals

Signal	I/O	Description
CLKI	I	Clock input from external pin or routing
CLKFB	I	DLL feed input from DLL output, clock net, routing or external pin
RSTN	I	Active low synchronous reset
ALUHOLD	I	Active high freezes the ALU
UDDCNTL	I	Synchronous enable signal (hold high for two cycles) from routing
DCNTL[8:0]	O	Encoded digital control signals for PIC INDEL and slave delay calibration
CLKOP	O	The primary clock output
CLKOS	O	The secondary clock output with fine phase shift and/or division by 2 or by 4
LOCK	O	Active high phase lock indicator
SMIADDR[9:0]	I	SMI Address
SMICLK	I	SMI Clock
SMIRSTN	I	SMI Reset (Active low)
SMIRD	I	SMI Read
SMIWDATA	I	SMI Write Data
SMIWR	I	SMI Write
SMIRDATA	O	SMI Read Data

DLL_DEL Delay Block

Closely associated with each DLL is a DLL_DEL block. This is a delay block consisting of a delay line with taps and a selection scheme that selects one of the taps. The DCNTL[8:0] bus controls the delay of the CLKINDEL signal. Typically this is the delay setting that the DLL uses to achieve phase alignment. This results in the delay providing a calibrated 90° phase shift that is useful in centering a clock in the middle of a data cycle for source synchronous data. Note that it is possible to make small adjustments to the delay by programming registers available via the SMI bus. The CLKINDEL signal feeds the edge clock network. Figure 2-6 shows the connections between the DLL block and the DLL_DEL delay block. For more information, please see details of additional technical documentation at the end of this data sheet.

Figure 2-6. DLL_DEL Delay Block



PLL/DLL Cascading

LatticeECP2 devices have been designed to allow certain combinations of PLL (GPLL and SPLL) and DLL cascading. The allowable combinations are as follows:

- PLL to PLL supported
- PLL to DLL supported

The DLLs in the LatticeECP2 are used to shift the clock in relation to the data for source synchronous inputs. PLLs are used for frequency synthesis and clock generation for source synchronous interfaces. Cascading PLL and DLL blocks allows applications to utilize the unique benefits of both DLLs and PLLs.

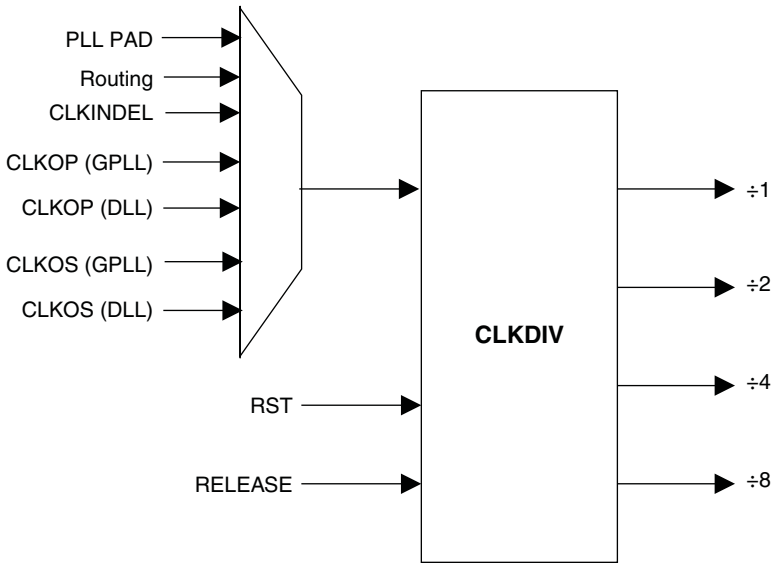
For further information on the DLL, please see details of additional technical documentation at the end of this data sheet.

Clock Dividers

LatticeECP2 devices have two clock dividers on the left and right sides of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a ÷2, ÷4 or ÷8 mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from selected PLL/DLL outputs, DLL_DEL delay blocks, routing or from an external clock input. The clock divider outputs serve as primary clock sources and feed into the

clock distribution network. The Reset (RST) control signal resets input and synchronously forces all outputs to low. The RELEASE signal releases outputs synchronously to the input clock. For further information on clock dividers, please see details of additional technical documentation at the end of this data sheet. Figure 2-7 shows the clock divider connections.

Figure 2-7. Clock Divider Connections



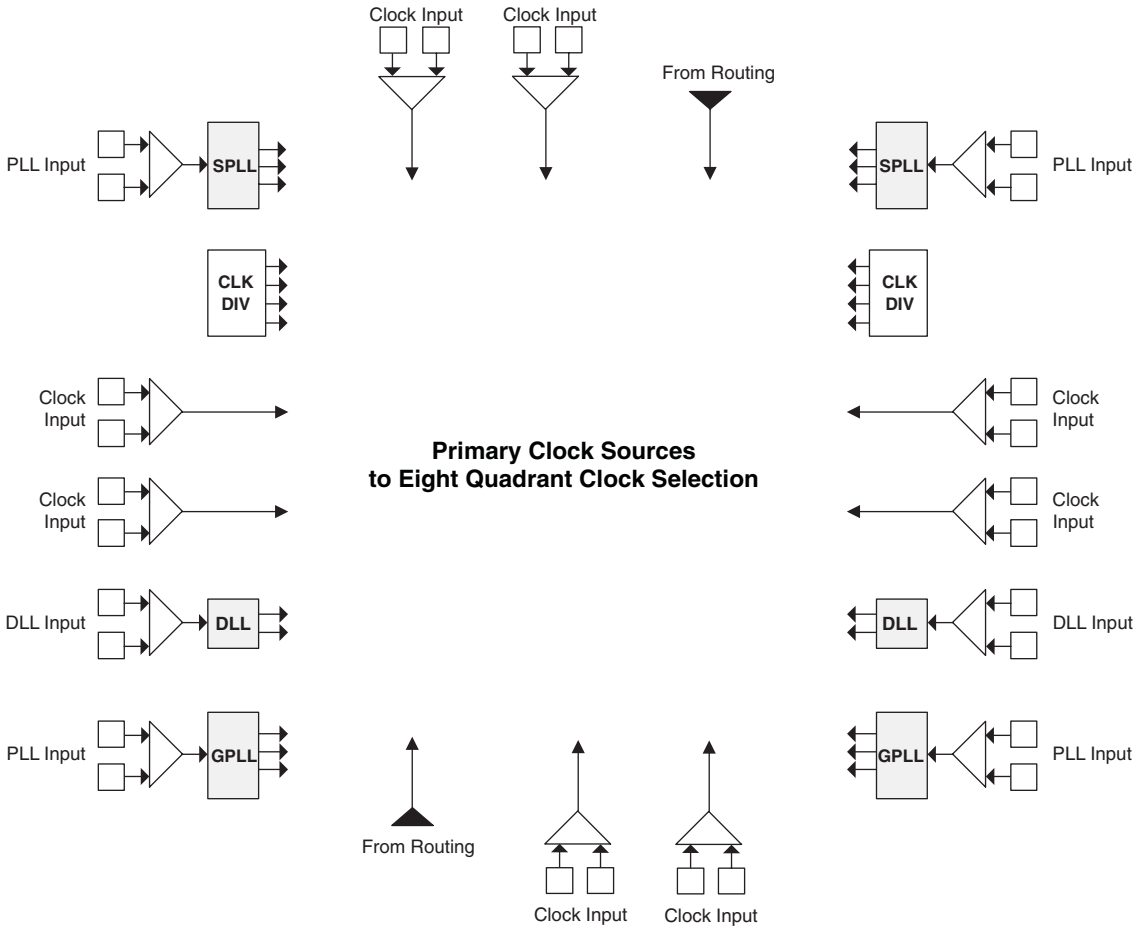
Clock Distribution Network

LatticeECP2 devices have eight quadrant-based primary clocks and eight flexible region-based secondary clocks/control signals. Two high performance edge clocks are available on each edge of the device to support high speed interfaces. These clock inputs are selected from external I/Os, the sysCLOCK PLLs, DLLs or routing. These clock inputs are fed throughout the chip via a clock distribution system.

Primary Clock Sources

LatticeECP2 devices derive clocks from five primary sources: PLL (GPLL and SPLL) outputs, DLL outputs, CLKDIV outputs, dedicated clock inputs and routing. LatticeECP2 devices have two to six sysCLOCK PLLs and two DLLs, located on the left and right sides of the device. There are eight dedicated clock inputs, two on each side of the device. Figure 2-8 shows the primary clock sources.

Figure 2-8. Primary Clock Sources for ECP2-50

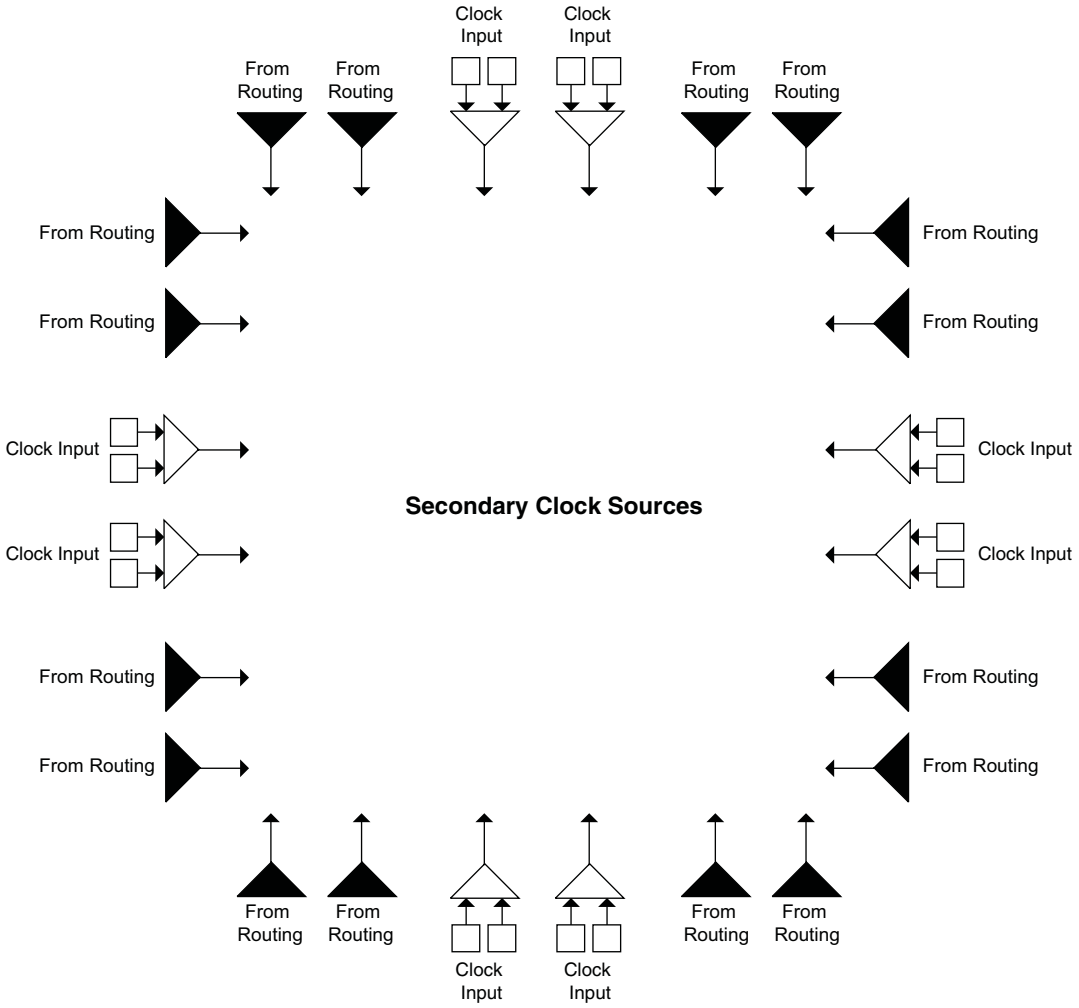


Note: This diagram shows sources for the ECP2-50 device. Smaller devices have fewer SPLLs.

Secondary Clock/Control Sources

LatticeECP2 devices derive secondary clocks (SC0 through EC7) from eight dedicated clock input pads and the rest from routing. Figure 2-9 shows the secondary clock sources.

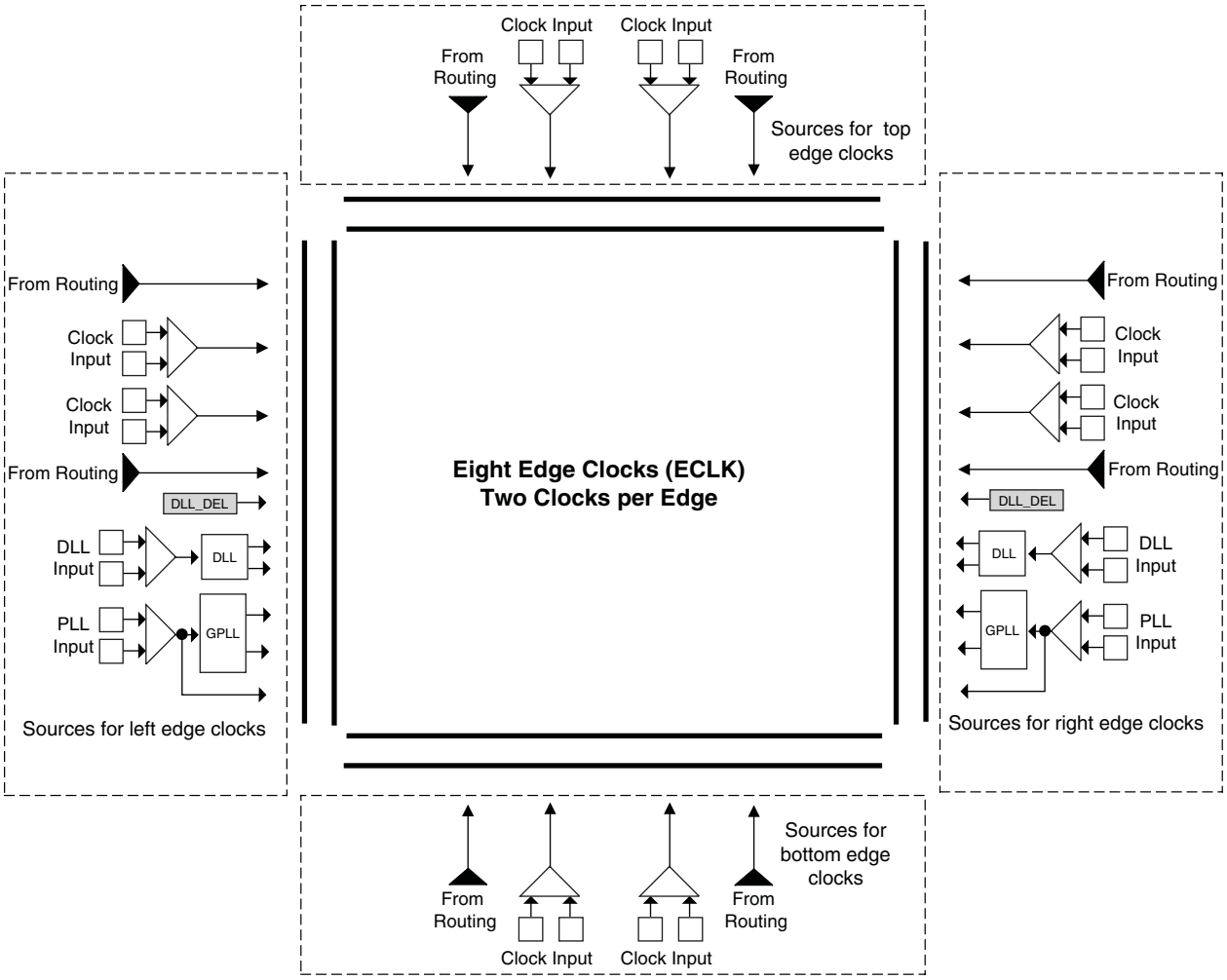
Figure 2-9. Secondary Clock Sources



Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs/DLLs and clock dividers as shown in Figure 2-10.

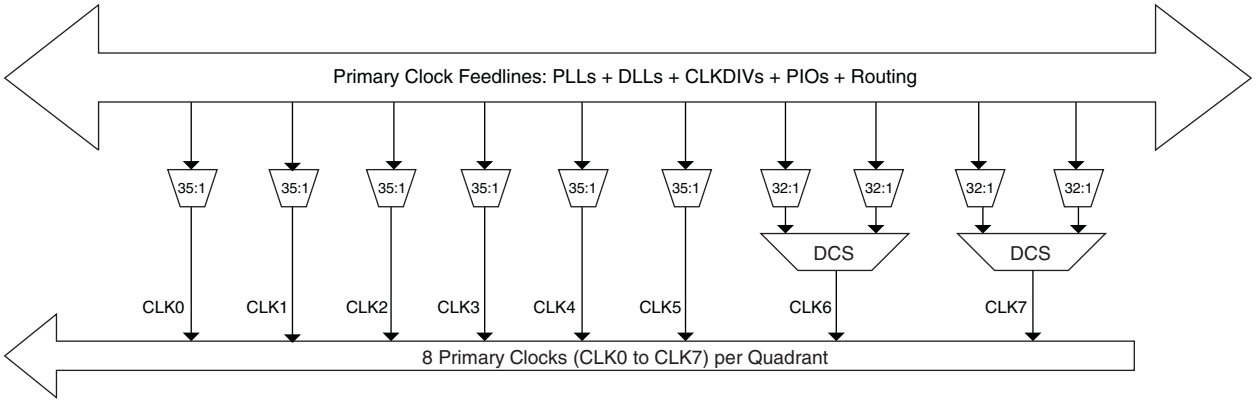
Figure 2-10. Edge Clock Sources



Primary Clock Routing

The clock routing structure in LatticeECP2 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. Figure 2-11 shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally

Figure 2-11. Per Quadrant Primary Clock Selection

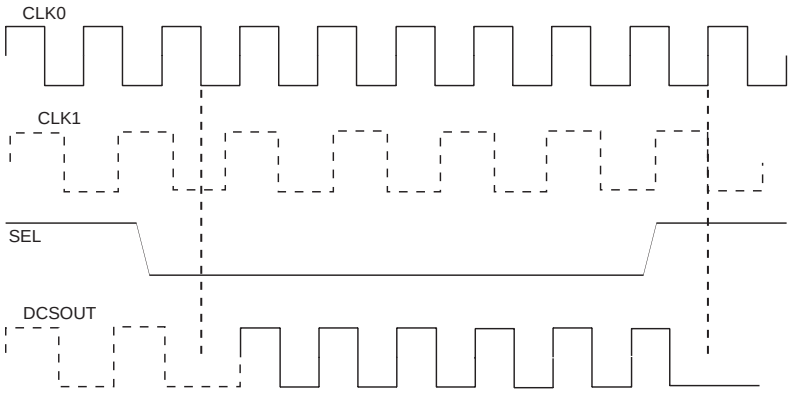


Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved irrespective of when the select signal is toggled. There are two DCS blocks per quadrant; in total, eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see Figure 2-11).

Figure 2-12 shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, please see details of additional technical documentation at the end of this data sheet.

Figure 2-12. DCS Waveforms



Secondary Clock/Control Routing

Secondary clocks in the LatticeECP2 devices are region-based resources. EBR/DSP rows and a special vertical routing channel bound the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP block in the DSP row or the center of the DSP row. Figure 2-13 shows this special vertical routing channel and the eight secondary clock regions for the ECP2-50. LatticeECP2 devices have eight secondary clock resources per region (SC0 to SC7).

The secondary clock muxes are located in the center of the device. Figure 2-13 shows the mux structure of the secondary clock routing. Secondary clocks SC0 to SC3 are used for high fan-out control and SC4 to SC7 are used for clock signals.

Figure 2-13. Secondary Clock Regions ECP2-50

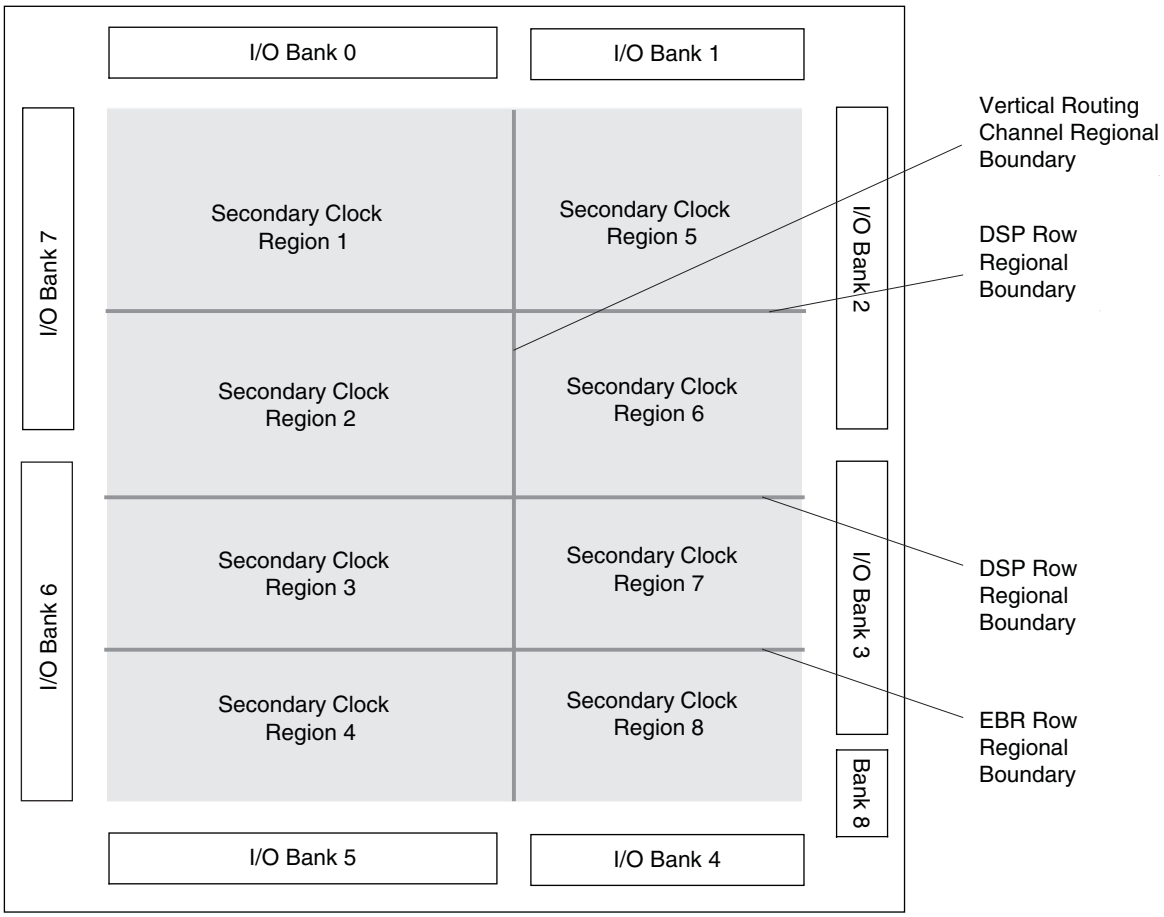
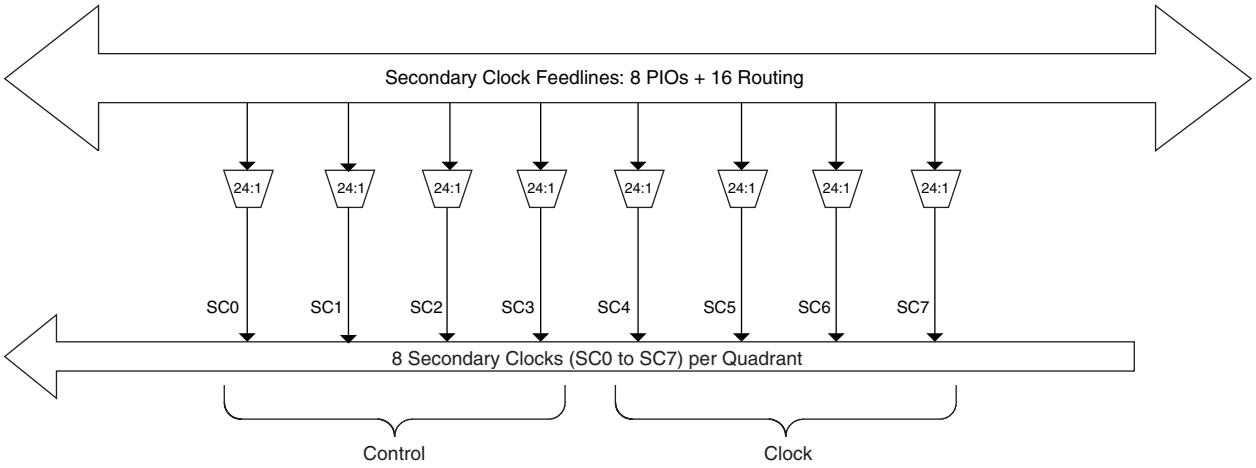


Figure 2-14. Per Region Secondary Clock Selection



Slice Clock Selection

Figure 2-15 shows the clock selections and Figure 2-16 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals via routing can be used as a clock input to the slices. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

Figure 2-15. Slice0 through Slice2 Clock Selection

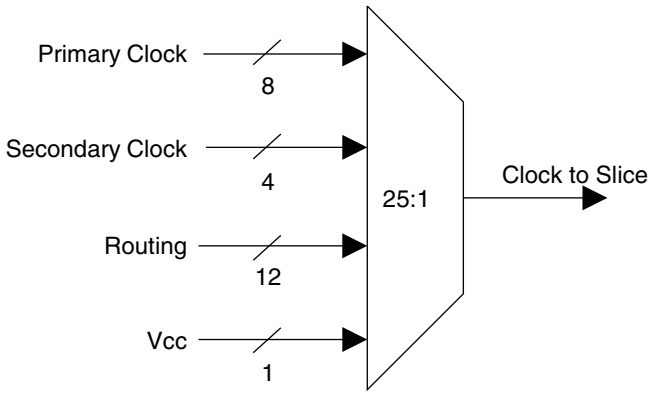
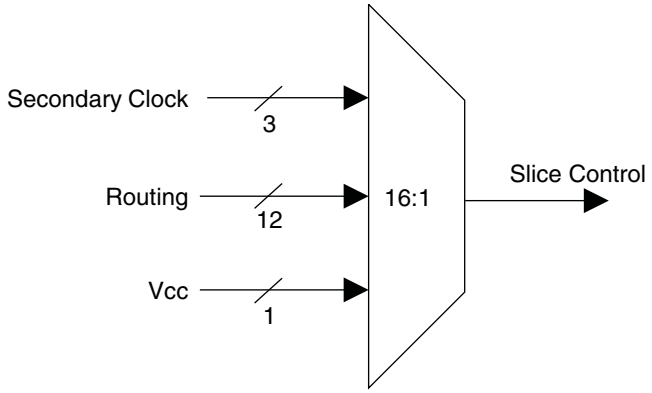


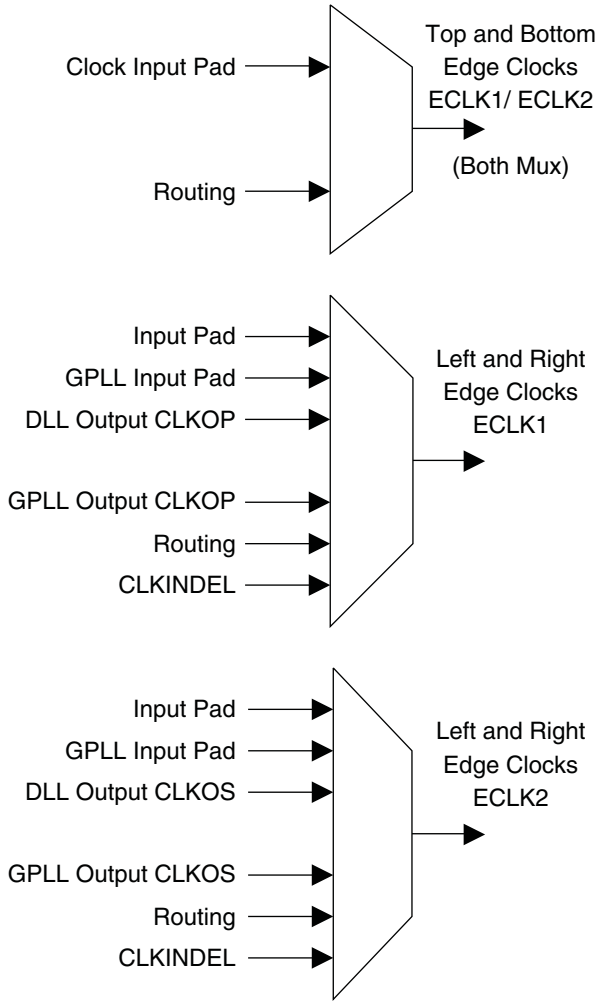
Figure 2-16. Slice0 through Slice2 Control Selection



Edge Clock Routing

LatticeECP2 devices have a number of high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. There are eight edge clocks per device: two edge clocks per edge. Different PLL and DLL outputs are routed to the two muxes on the left and right sides of the device. In addition, the CLKINDEL signal (generated from the DLL_DEL block) is routed to all the edge clock muxes on the left and right sides of the device. Figure 2-17 shows the selection muxes for these clocks.

Figure 2-17. Edge Clock Mux Connections



sysMEM Memory

LatticeECP2 devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of an 18-Kbit RAM with dedicated input and output registers.

sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in Table 2-6. FIFOs can be implemented in sysMEM EBR blocks by implementing support logic with PFUs. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with18-bit and 36-bit data widths.

Table 2-6. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36
True Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18
Pseudo Dual Port	16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36

Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports three forms of write behavior for single port or dual port operation:

1. Normal – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.

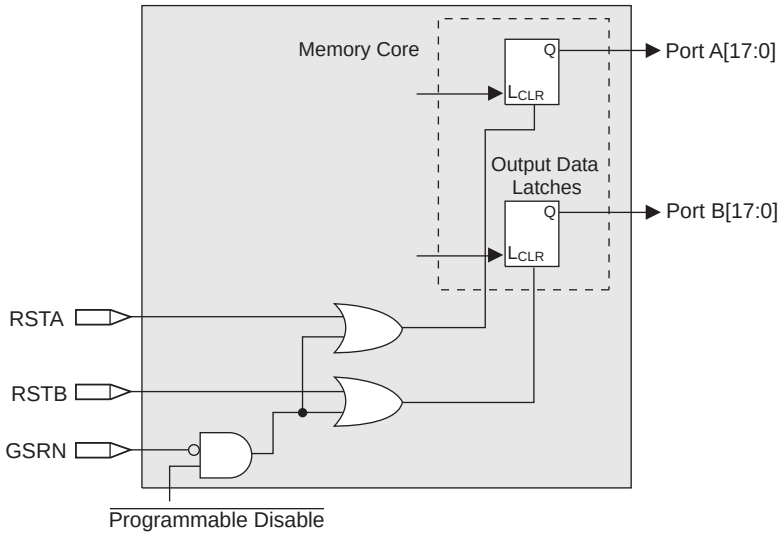
2. Write Through – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

3. Read-Before-Write – When new data is being written, the old content of the address appears at the output. This mode is supported for x9, x18 and x36 data widths.

Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2-18.

Figure 2-18. Memory Core Reset



For further information on the sysMEM EBR block, please see the details of additional technical documentation at the end of this data sheet.

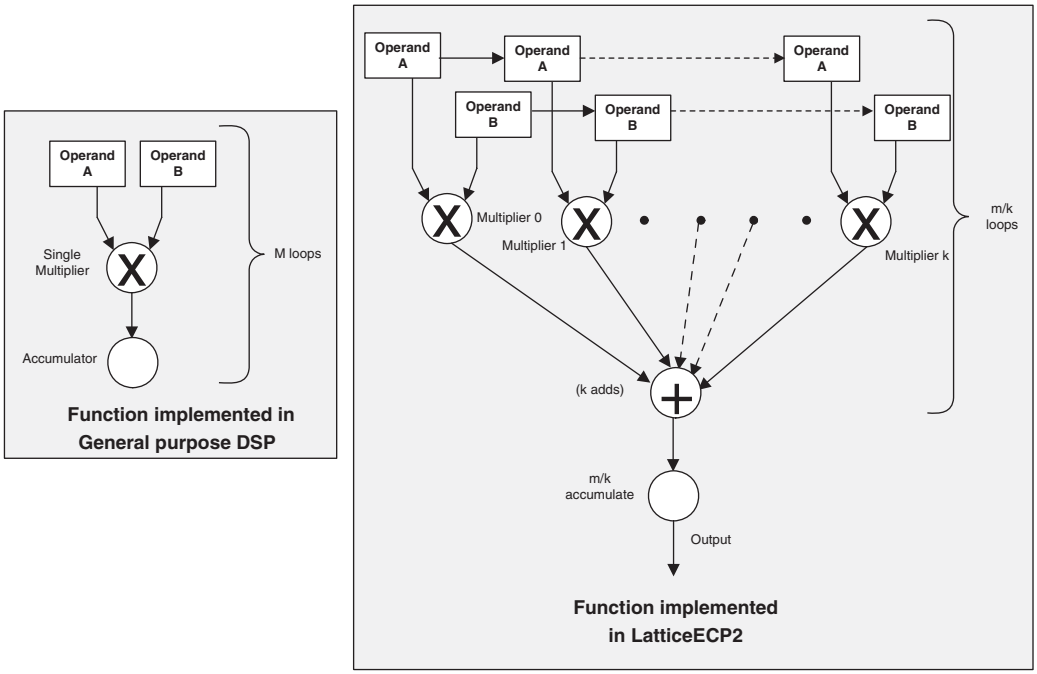
sysDSP™ Block

The LatticeECP2 family provides a sysDSP block making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications are Finite Impulse Response (FIR) filters, Fast Fourier Transforms (FFT) functions, Correlators, Reed-Solomon/Turbo/Convolution encoders and decoders. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

sysDSP Block Approach Compare to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeECP2, on the other hand, has many DSP blocks that support different data-widths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing appropriate level of parallelism. Figure 2-19 compares the fully serial and the mixed parallel and serial implementations.

Figure 2-19. Comparison of General DSP and LatticeECP2 Approaches



sysDSP Block Capabilities

The sysDSP block in the LatticeECP2 family supports four functional elements in three 9, 18 and 36 data path widths. The user selects a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeECP2 family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block. In LatticeECP2 family of devices the DSP elements can be concatenated.

The resources in each sysDSP block can be configured to support the following four elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADD (Multiply, Addition/Subtraction)
- MULTADDSUM (Multiply, Addition/Subtraction, Accumulate)

The number of elements available in each block depends in the width selected from the three available options x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2-7 shows the capabilities of the block.

Table 2-7. Maximum Number of Elements in a Block

Width of Multiply	x9	x18	x36
MULT	8	4	1
MAC	2	2	—
MULTADD	4	2	—
MULTADDSUM	2	1	—

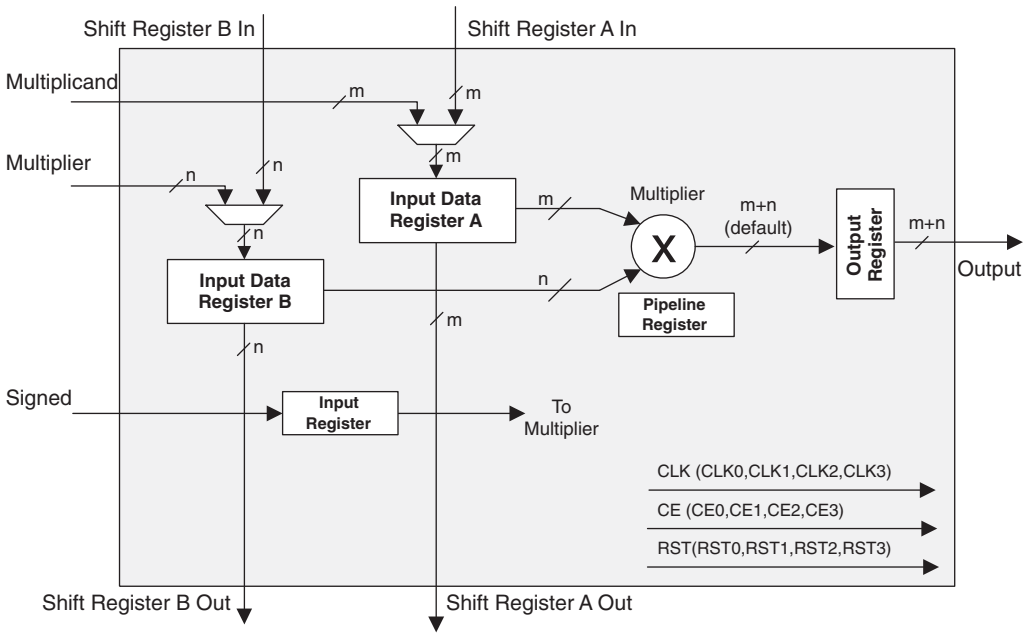
Some options are available in four elements. The input register in all the elements can be directly loaded or can be loaded as shift register from previous operand registers. By selecting ‘dynamic operation’ the following operations are possible:

- In the 'Signed/Unsigned' options the operands can be switched between signed and unsigned on every cycle.
- In the 'Add/Sub' option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. The user can enable the input/output and pipeline registers. Figure 2-20 shows the MULT sysDSP element.

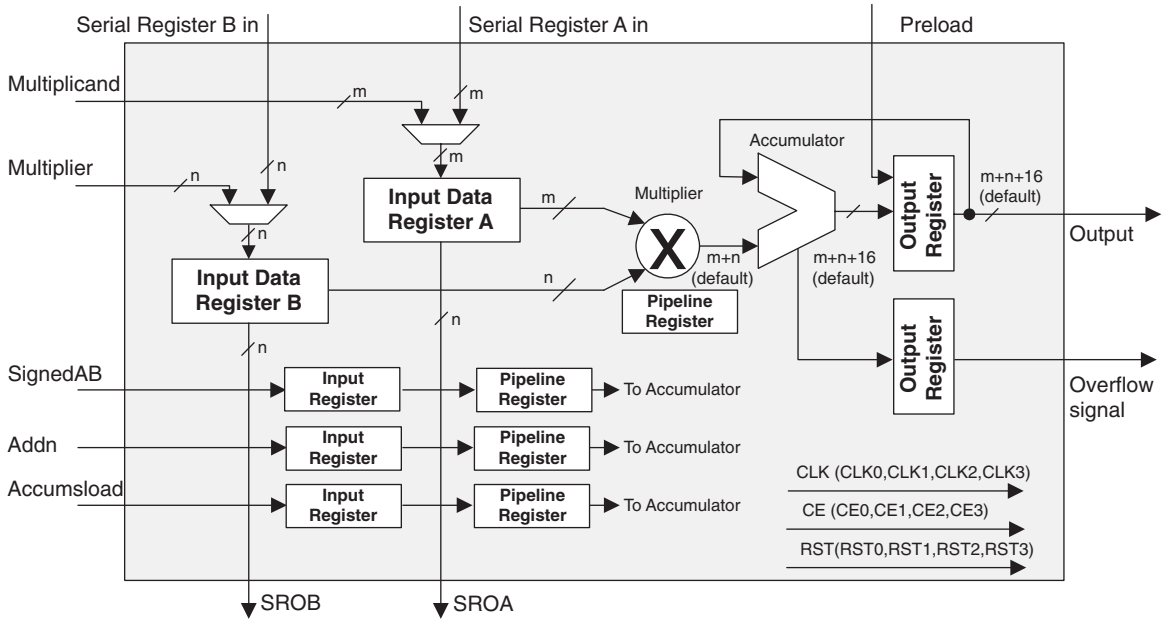
Figure 2-20. MULT sysDSP Element



MAC sysDSP Element

In this case, the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. The user can enable the input and pipeline registers but the output register is always enabled. The output register is used to store the accumulated value. The Accumulators in the DSP blocks in LatticeECP2 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. Figure 2-21 shows the MAC sysDSP element.

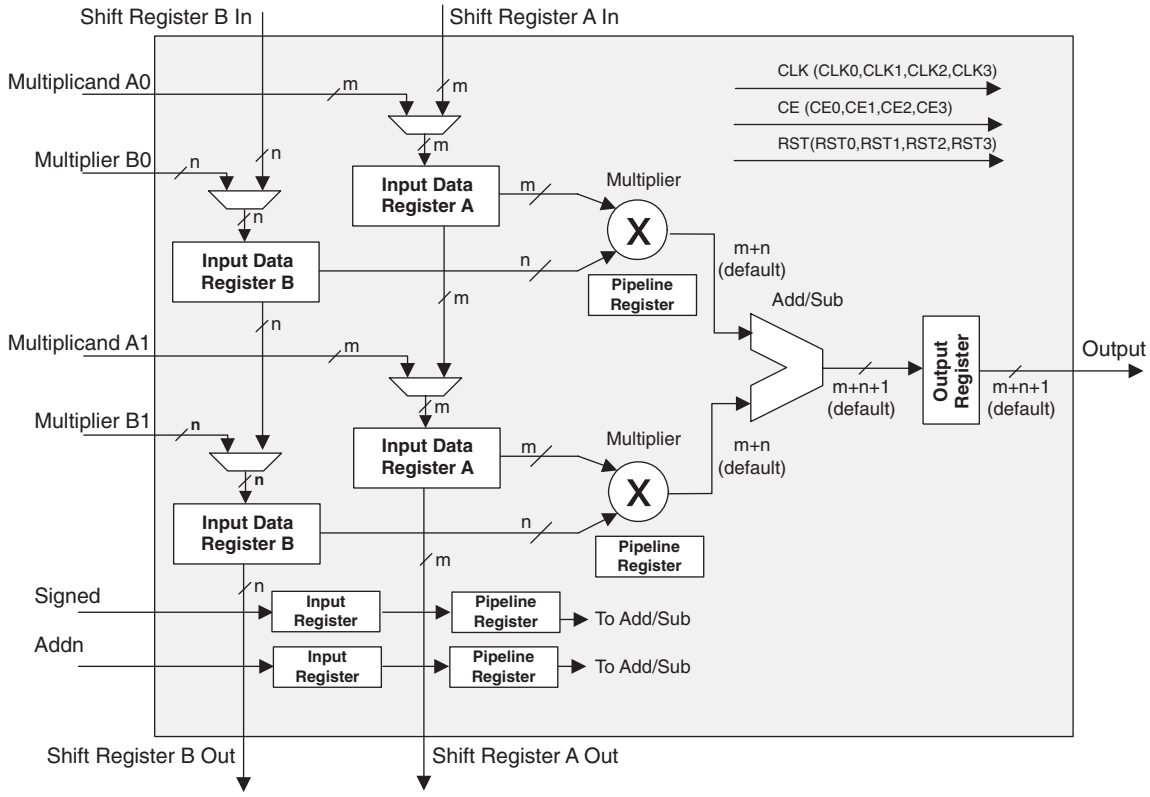
Figure 2-21. MAC sysDSP



MULTADD sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and A2. The user can enable the input, output and pipeline registers. Figure 2-20 shows the MULTADD sysDSP element.

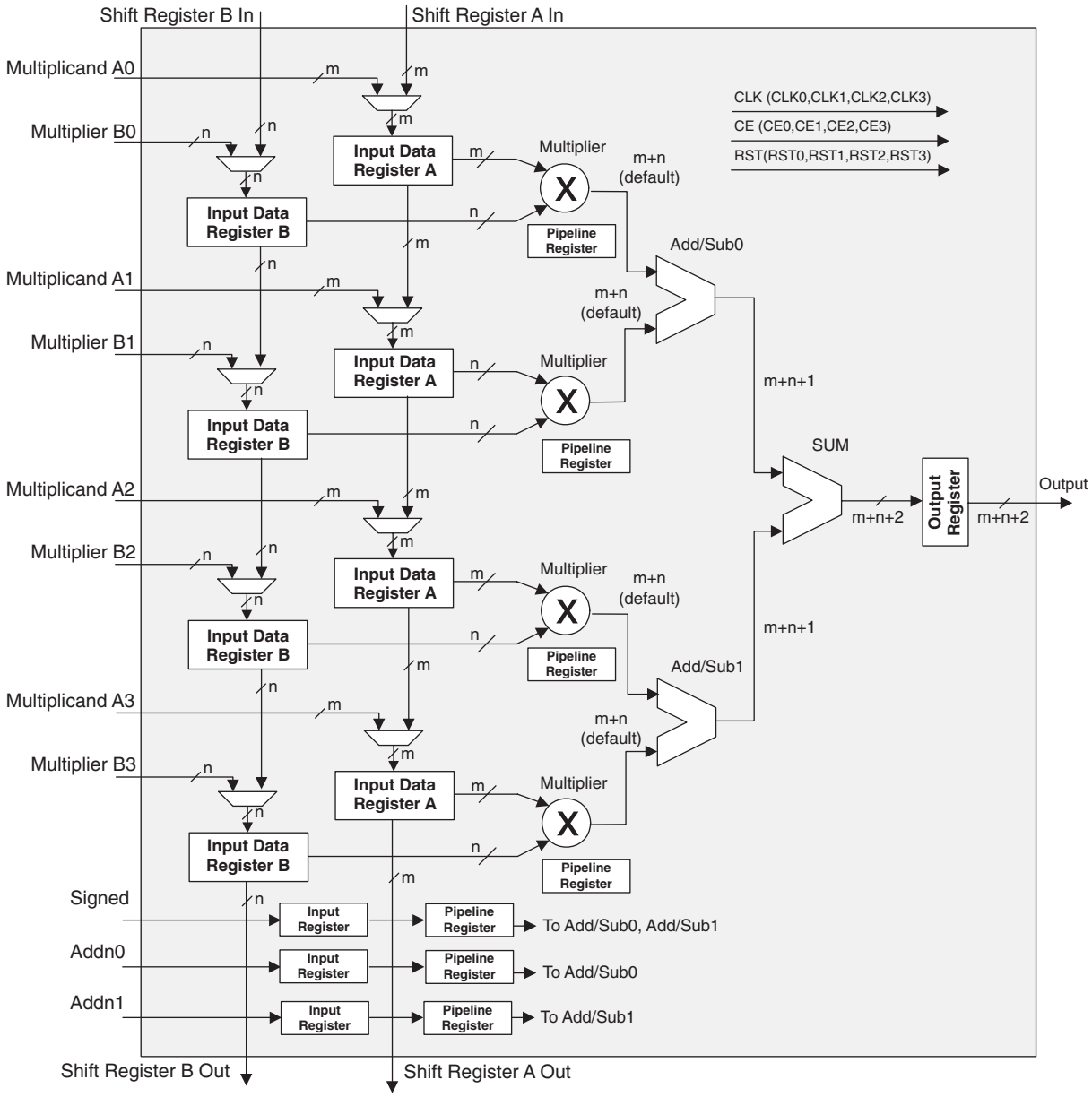
Figure 2-22. MULTADD



MULTADDSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. The user can enable the input, output and pipeline registers. Figure 2-23 shows the MULTADDSUM sysDSP element.

Figure 2-23. MULTADDSUM



Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable and Reset signals from routing are available to every DSP block. Four Clock, Reset and Clock Enable signals are selected for the sysDSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output register. Similarly Clock enable (CE) and

Reset (RST) are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

Signed and Unsigned with Different Widths

The DSP block supports different widths of signed and unsigned multipliers besides x9, x18 and x36 widths. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2-8 provides an example of this.

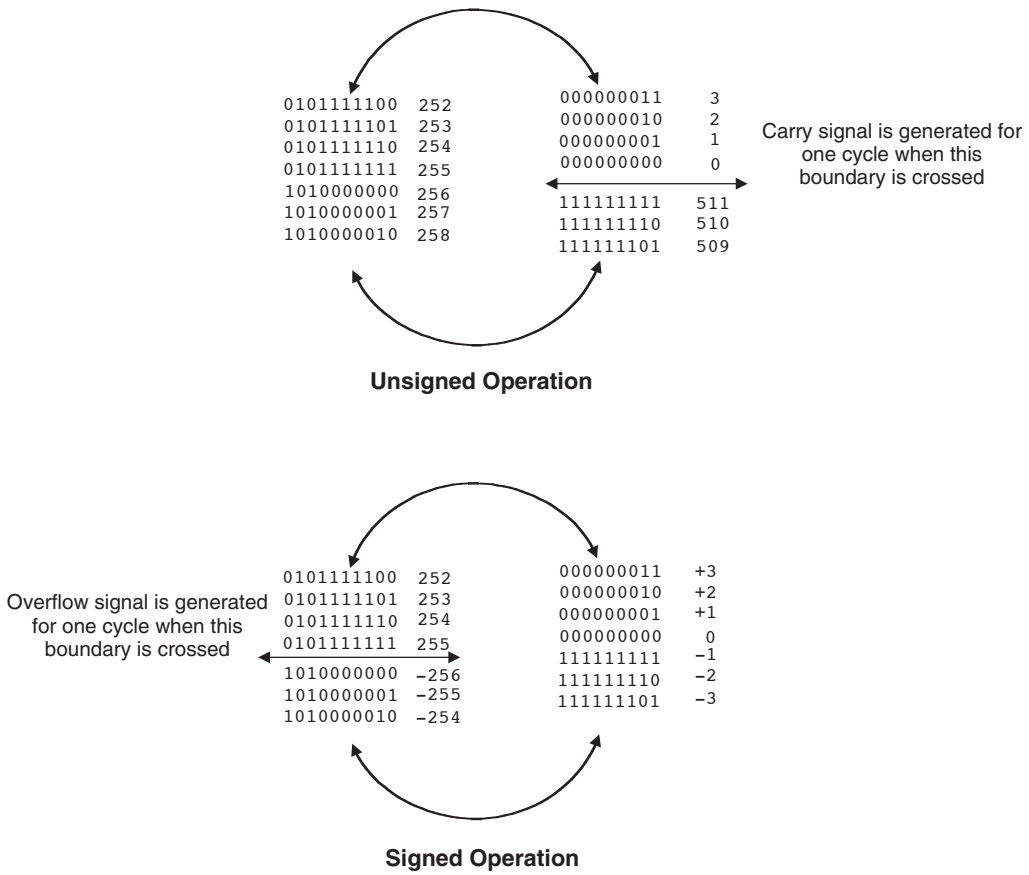
Table 2-8. Sign Extension Example

Number	Unsigned	Unsigned 9-bit	Unsigned 18-bit	Signed	Two's Complement Signed 9 Bits	Two's Complement Signed 18 Bits
+5	0101	000000101	000000000000000101	0101	000000101	000000000000000101
-6	N/A	N/A	N/A	1010	111111010	111111111111111010

OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. When two unsigned numbers are added and the result is a smaller number than the accumulator, "roll-over" is said to have occurred and an overflow signal is indicated. When two positive numbers are added with a negative sum and when two negative numbers are added with a positive sum, then the accumulator "roll-over" is said to have occurred and an overflow signal is indicated. Note that when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions overflow signal for signed and unsigned operands are listed in Figure 2-24.

Figure 2-24. Accumulator Overflow/Underflow



IPexpress™

The user can access the sysDSP block via the ispLEVER IPexpress tool which provides the option to configure each DSP module (or group of modules) or by direct HDL instantiation. In addition, Lattice has partnered with The MathWorks® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with ispLEVER to dramatically shorten the DSP design cycle in Lattice FPGAs.

Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeECP2 DSP include the Bit Correlator, Fast Fourier Transform, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Please contact Lattice to obtain the latest list of available DSP IP cores.

Resources Available in the LatticeECP2 Family

Table 2-9 shows the maximum number of multipliers for each member of the LatticeECP2 family. Table 2-10 shows the maximum available EBR RAM Blocks in each LatticeECP2 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2-9. Maximum Number of DSP Blocks in the LatticeECP2 Family

Device	DSP Block	9x9 Multiplier	18x18 Multiplier	36x36 Multiplier
ECP2-6	3	24	12	3
ECP2-12	6	48	24	6
ECP2-20	7	56	28	7
ECP2-35	8	64	32	8
ECP2-50	18	144	72	18
ECP2-70	22	176	88	22

Table 2-10. Embedded SRAM in the LatticeECP2 Family

Device	EBR SRAM Block	Total EBR SRAM (Kbits)
ECP2-6	3	55
ECP2-12	12	221
ECP2-20	15	277
ECP2-35	18	332
ECP2-50	21	387
ECP2-70	56	1032

LatticeECP2 DSP Performance

Table 2-11 lists the maximum performance in millions of MAC operations per second (MMAC) for each member of the LatticeECP2 family.

Table 2-11. DSP Performance

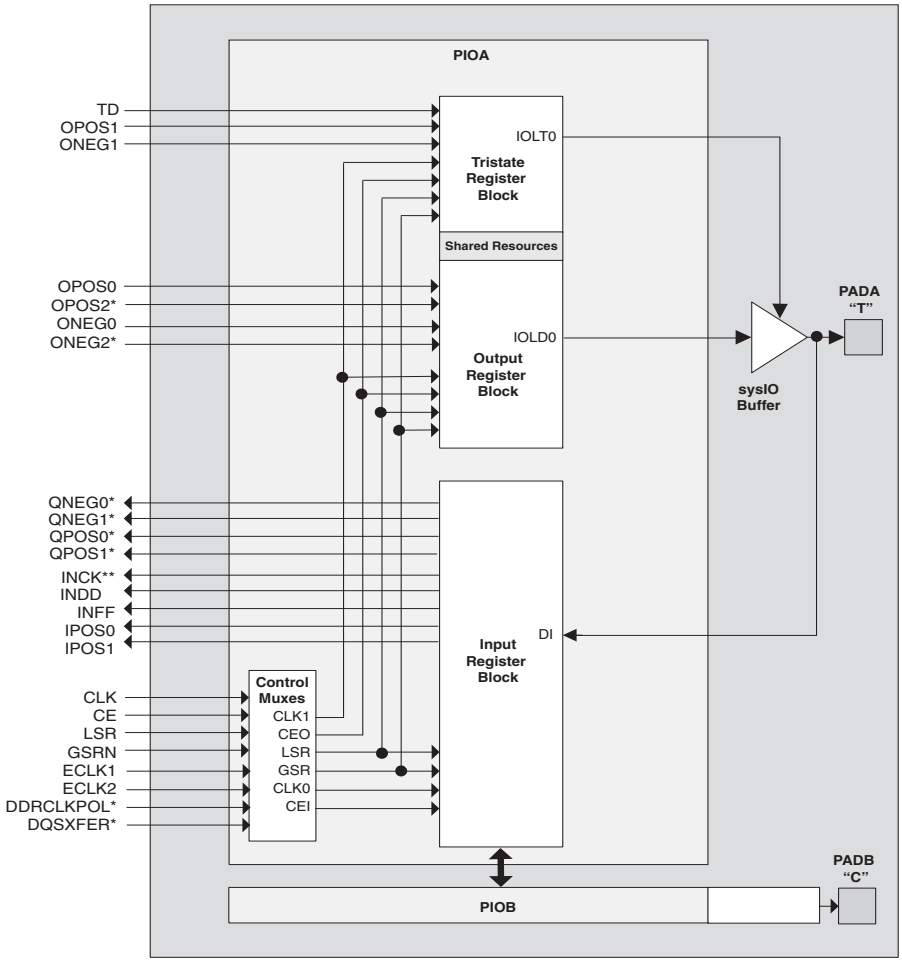
Device	DSP Block	DSP Performance MMAC
ECP2-6	3	TBA
ECP2-12	6	TBA
ECP2-20	7	TBA
ECP2-35	8	TBA
ECP2-50	18	TBA
ECP2-70	22	TBA

For further information on the sysDSP block, please see details of additional technical information at the end of this data sheet.

Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysIO buffers as shown in Figure 2-25. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysIO buffer and receives input from the buffer. Figure 2-12 provides the PIO signal list.

Figure 2-25. PIC Diagram



*Signals are available on left/right/bottom edges only.
** Selected blocks.

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in Figure 2-25. The PAD Labels “T” and “C” distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as inputs.

Table 2-12. PIO Signal List

Name	Type	Description
CE0, CE1	Control from the core	Clock enables for input and output block flip-flops
CLK0, CLK1	Control from the core	System clocks for input and output blocks
ECLK1, ECLK2	Control from the core	Fast edge clocks
LSR	Control from the core	Local Set/Reset
GSRN	Control from routing	Global Set/Reset (active low)
INCK	Input to the core	Input to Primary Clock Network or PLL reference inputs
DQS	Input to PIO	DQS signal from logic (routing) to PIO
INDD	Input to the core	Unregistered data input to core
INFF	Input to the core	Registered input on positive edge of the clock (CLK0)
IPOS0, IPOS1	Input to the core	Double data rate registered inputs to the core
QPOS0[1], QPOS1[1]	Input to the core	Gearbox pipelined inputs to the core
QNEG0[1], QNEG1[1]	Input to the core	Gearbox pipelined inputs to the core
OPOS0, ONEG0, OPOS2, ONEG2	Control from the core	Output signals from the core for SDR and DDR operation
OPOS1 ONEG1	Tristate control from the core	Signals to Tristate Register block for DDR operation
DEL[3:0]	Control from the core	Dynamic input delay control bits
TD	Tristate control from the core	Tristate signal from the core used in SDR operation
DDRCLKPOL	Control from clock polarity bus	Controls the polarity of the clock (CLK0) that feed the DDR input block
DQSXFER	Control from core	Controls signal to the Output block

1. Signals available on left/right/bottom only.
2. Selected I/O.

PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for PIOs in left, right and bottom edges contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. Figure 2-26 shows the diagram of the input register block for left, right and bottom edges. The input register block for the top edge contains one memory element to register the input signal as shown in Figure 2-27. The following description applies to the input register block for PIOs in left, right and bottom edges of the device.

Input signals are fed from the sysIO buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the single data rate (SDR) the data is registered, by one of the registers in the single data rate sync register block, with the system clock. In DDR Mode, two registers are used to sample the data on the positive and negative edges of the DQS signal, creating two data streams, D0 and D1.

These two data streams are synchronized with the system clock before entering the core. Further discussion on this topic is in the DDR Memory section of this data sheet.

By combining input blocks of the complementary PIOs and sharing some registers from output blocks, a gearbox function can be implemented, that takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. Figure 2-26 shows the diagram using this gearbox function. For more information on this topic, please see information regarding additional documentation at the end of this data sheet.

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

Figure 2-26. Input Register Block for Left, Right and Bottom Edges

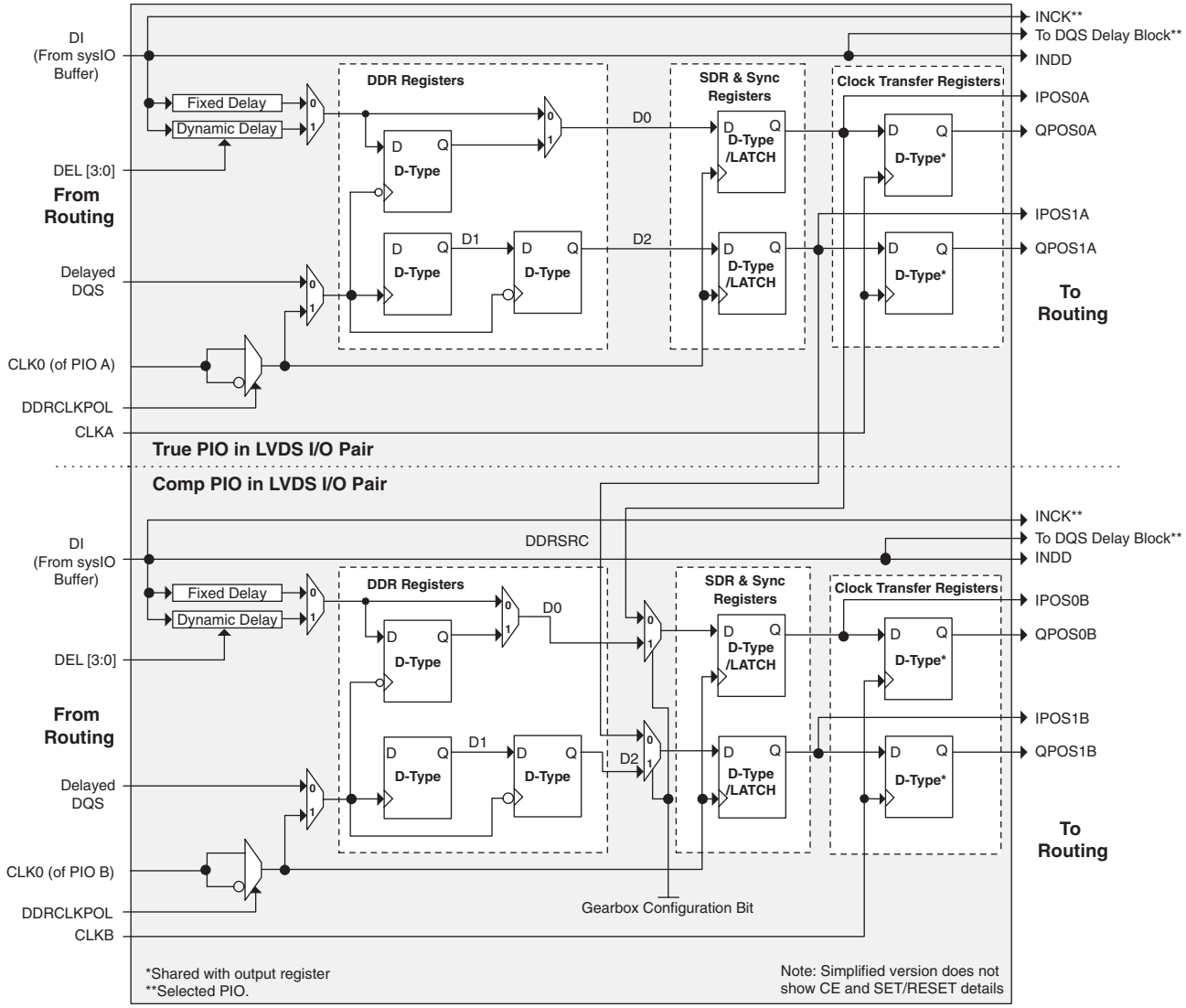
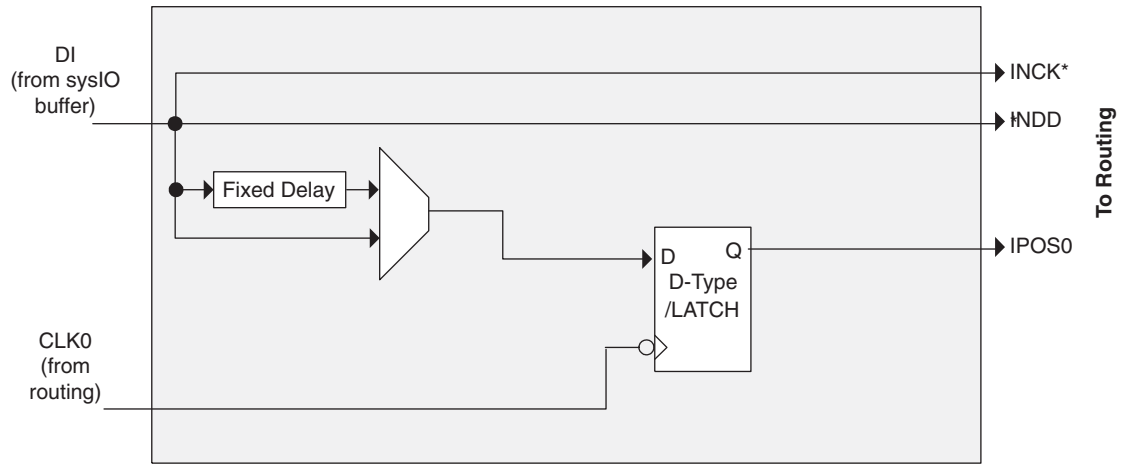


Figure 2-27. Input Register Block Top Edge



Note: Simplified version does not show CE and SET/RESET details.
*On selected blocks.

Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysIO buffers. The blocks on the PIOs on the left, right and bottom contains a register for SDR operation that is combined with an additional latch for DDR operation. Figure 2-28 shows the diagram of the Output Register Block for PIOs on the left, right and the bottom edges. Figure 2-29 shows the diagram of the Output Register Block for PIOs on the top edge of the device.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or latch. In DDR mode, ONEG0 and OPOS0 are fed into registers is fed into registers on the positive edge of the clock. Then at the next clock cycle this registered OPOS0 is latched. A multiplexer running off the same clock selects the correct register for feeding to the output (D0).

By combining output blocks of the complementary PIOs and sharing some registers from input blocks, a gearbox function can be implemented, that takes four data streams ONEG0A, ONEG1A, ONEG1B and ONEG1B. Figure 2-29 shows the diagram using this gearbox function. For more information on this topic, please see information regarding additional documentation at the end of this data sheet.

Figure 2-28. Output and Tristate Block for Left, Right and Bottom Edges

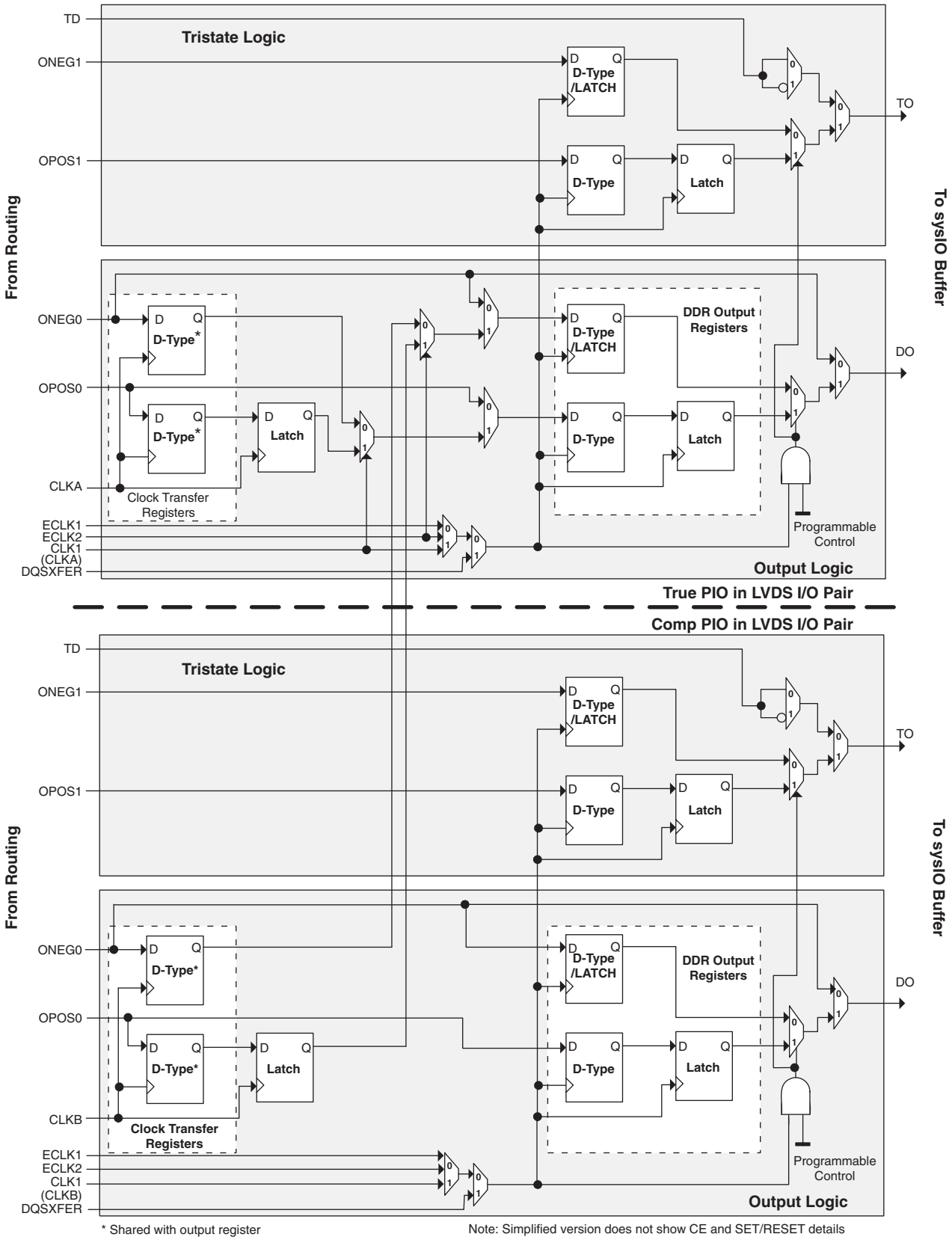
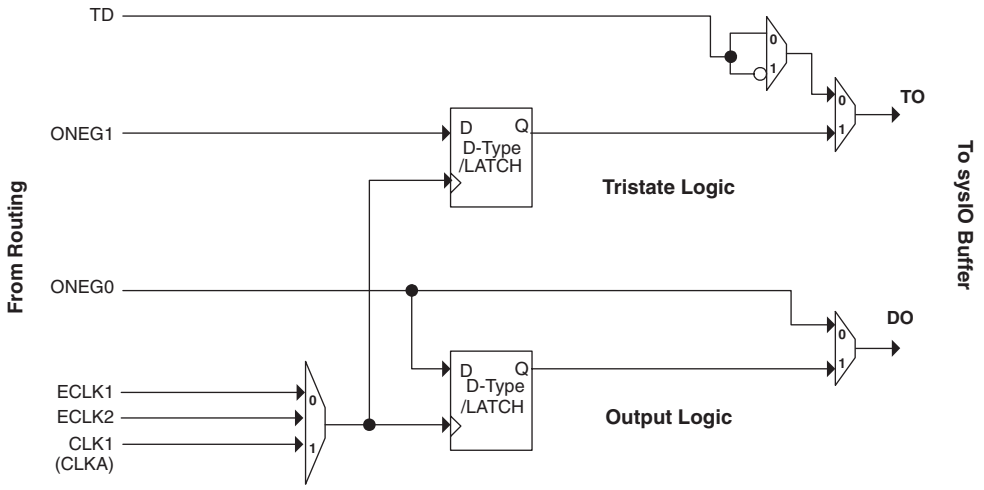


Figure 2-29. Output and Tristate Block, Top Edge



Note: Simplified version does not show CE and SET/RESET details.

Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysIO buffers. The block contains a register for SDR operation and an additional latch for DDR operation. Figure 2-28 shows the diagram of the Tristate Register Block with the Output Block for the left, right and bottom edges and Figure 2-29 shows the diagram of the Tristate Register Block with the Output Block for the top edge.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured a D-type or latch. In DDR mode, ONEG1 and OPOS1 are fed into registers on the positive edge of the clock. Then in the next clock the registered OPOS1 is latched. A multiplexer running off the same clock cycle selects the correct register for feeding to the output (D0).

Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock is selected from one of the clock signals provided from the general purpose routing, one of the edge clocks (ECLK1/ ECLK2) and a DQS signal provided from the programmable DQS pin and provided to the input register block. The clock can optionally be inverted.

DDR Memory Support

Certain PICs have additional circuitry to allow the implementation of high speed source synchronous and DDR memory interfaces. The support varies by edge of the device as detailed below.

Left and Right Edges

PICs on these edges have registered elements that support DDR memory interfaces. One of every 16 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus which spans the set of 16 PIOs. Figure 2-30 shows the assignment of DQS pins in each set of 16 PIOs.

Bottom Edge

PICs on these edges have registered elements that support DDR memory interfaces. One of every 18 PIOs contains a delay element to facilitate the generation of DQS signals. The DQS signal feeds the DQS bus that spans the set of 18 PIOs. Figure 2-31 shows the assignment of DQS pins in each set of 18 PIOs.

Top Edge

The PICs on the top edge are different from PIOs on the left, right and bottom edges. PIOs on this edge do not have registers or DQS signals.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the bottom are designed for memories that support 18 bits of data.

Figure 2-30. DQS Routing for the Left and Right Edges of the Device

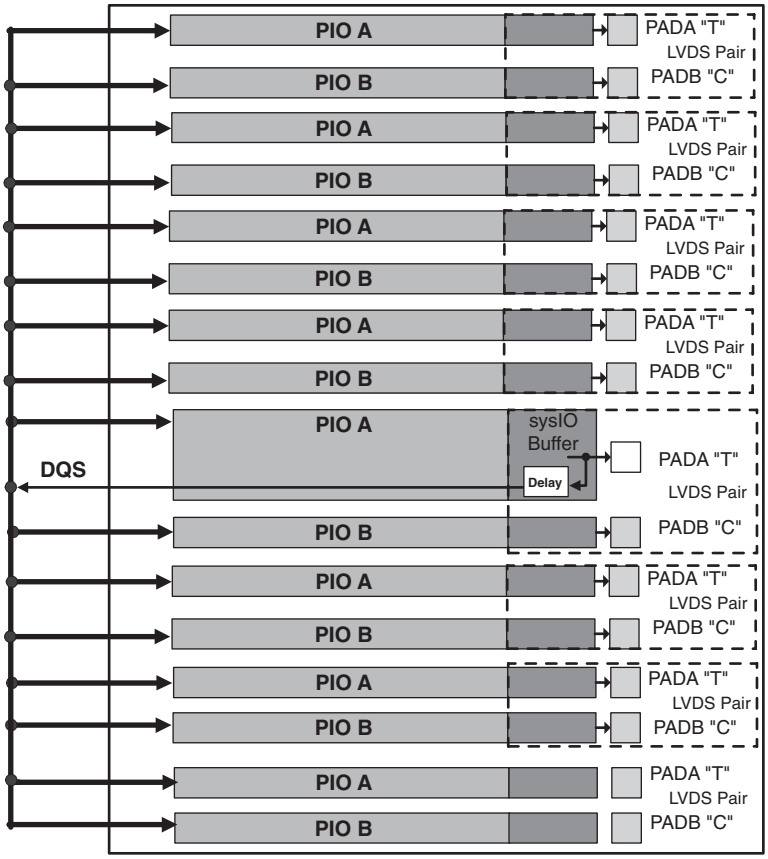
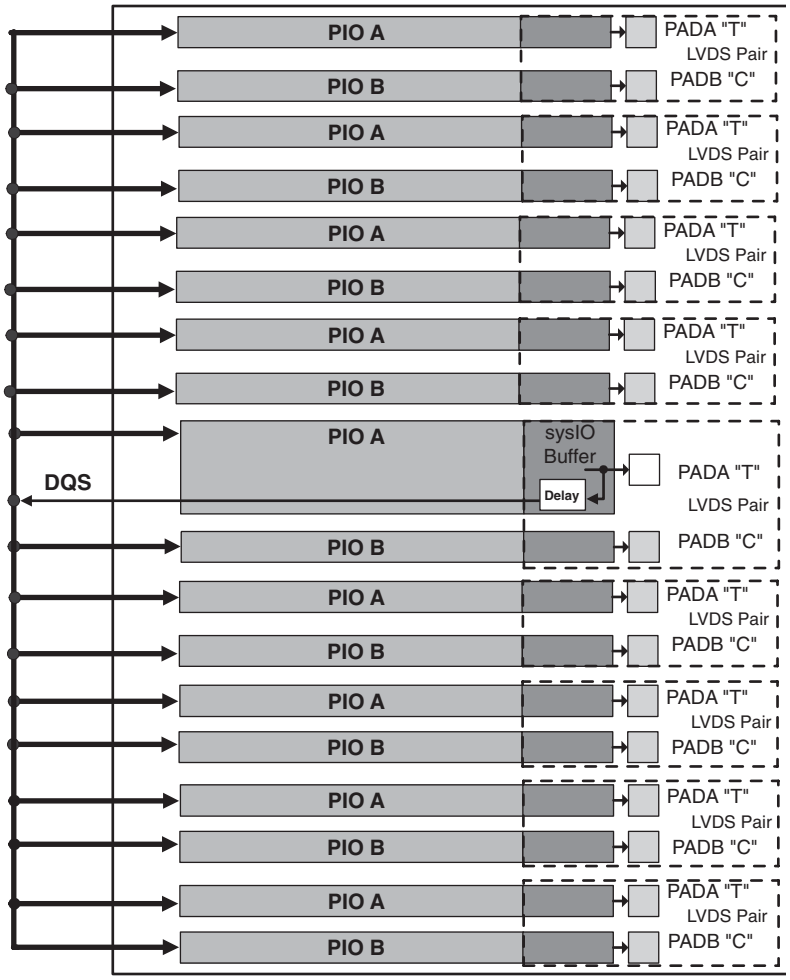


Figure 2-31. DQS Routing for the Bottom Edge of the Device



DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However in DDR memories the clock (referred to as DQS) is not free-running so this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only, as shown in Figure 2-32) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figure 2-32 and Figure 2-33 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of calibration (6-bit bus) signals from two dedicated DLLs (DDR_DLL) on opposite sides of the device. Each DLL compensates DQS delays in its half of the device as shown in Figure 2-32. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

Figure 2-32. DLL Calibration Bus and DQS/DQS Transition Distribution

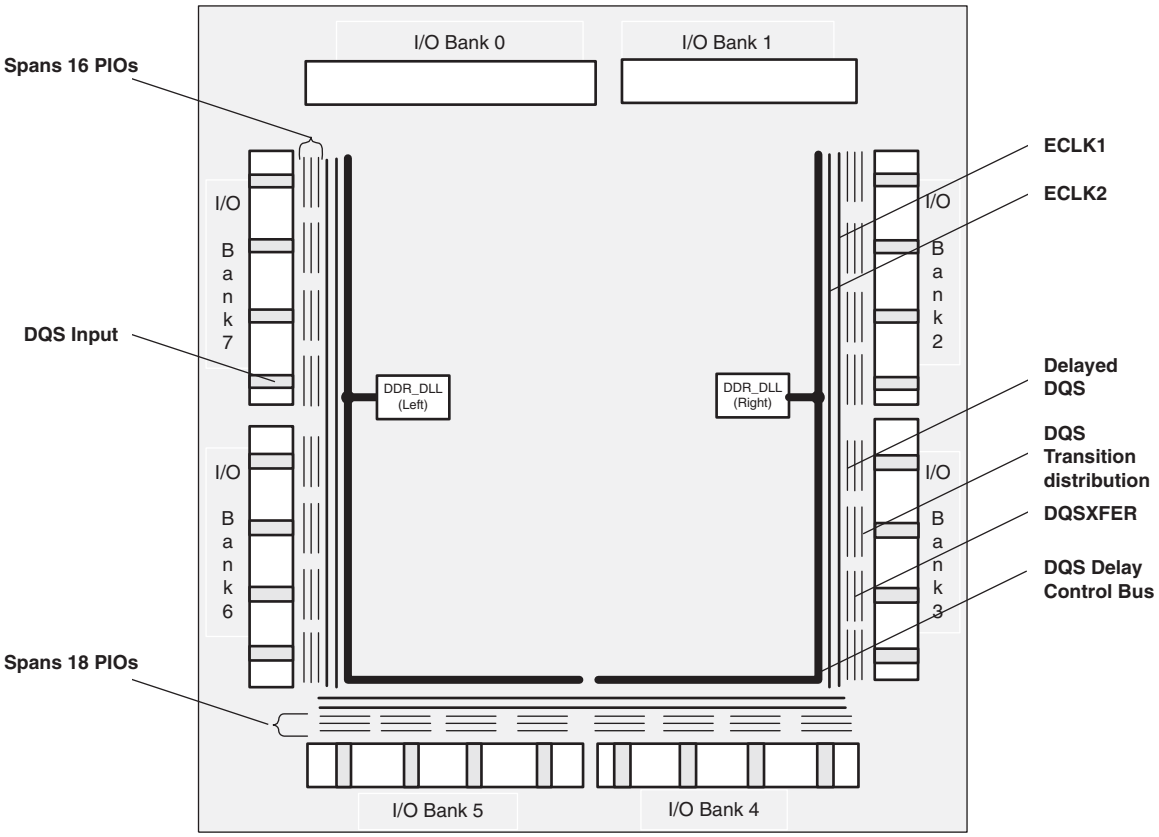
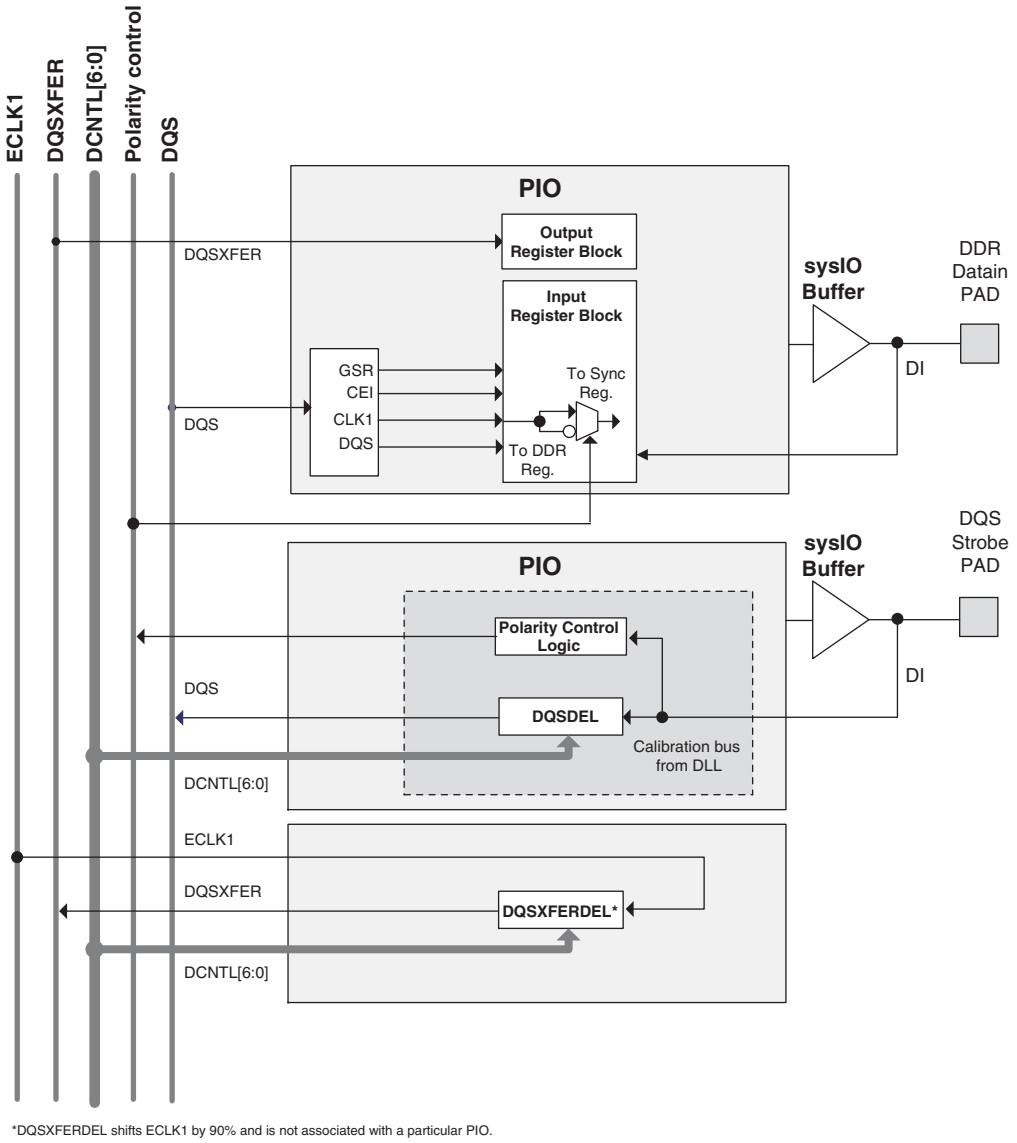


Figure 2-33. DQS Local Bus



*DQSXFERDEL shifts ECLK1 by 90% and is not associated with a particular PIO.

Polarity Control Logic

In a typical DDR Memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown.

The LatticeECP2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block. This requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

DQSXFER

LatticeECP2 devices provide a DQSXFER signal to the output buffer to assist it in data transfer to DDR memories that require DQS strobe be shifted 90º. This shifted DQS strobe is generated by the DQSDEL block. The DQSXFER signal runs the span of the data bus.

sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

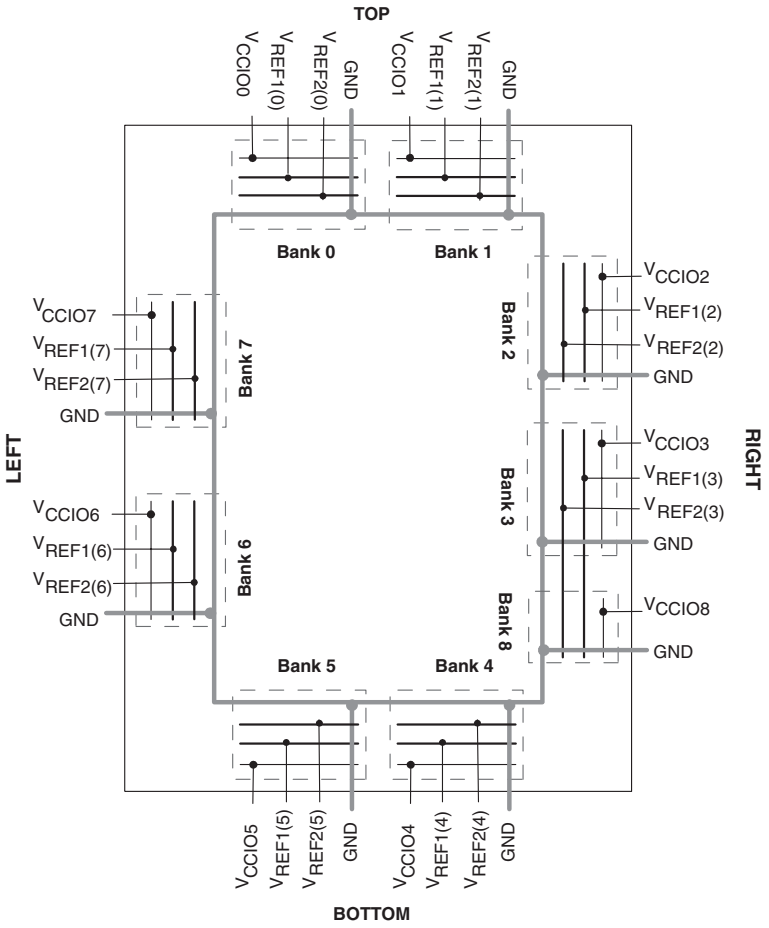
sysIO Buffer Banks

LatticeECP2 devices have nine sysIO buffer banks: eight banks for user I/Os arranged two per side. The ninth sysIO buffer bank (Bank 8) is located adjacent to Bank 3 and has dedicated/shared I/Os for configuration. When a shared pin is not used for configuration it is available as a user I/O. Each bank is capable of supporting multiple I/O standards. Each sysIO bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank, except Bank 8, has voltage references, V_{REF1} and V_{REF2}, that allow it to be completely independent from the others. Bank 8 shares two voltage references, V_{REF1} and V_{REF2}, with Bank 3. Figure 2-34 shows the nine banks and their associated supplies.

In LatticeECP2 devices, single-ended output buffers and ratioed input buffers (LVTTL, LVCMOS and PCI) are powered using V_{CCIO}. LVTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO}.

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2}, that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

Figure 2-34. LatticeECP2 Banks



LatticeECP2 devices contain two types of sysIO buffer pairs.

1. **Top (Bank 0 and Bank 1) sysIO Buffer Pairs (Single-Ended Outputs Only)**
   The sysIO buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

2. **Bottom (Bank 4 and Bank 5) sysIO Buffer Pairs (Single-Ended Outputs Only)**
   The sysIO buffer pairs in the bottom banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

   The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

   Only the I/Os on bottom banks have programmable PCI clamps.

3. **Left and Right (Banks 2, 3, 6 and 7) sysIO Buffer Pairs (50% Differential and 100% Single-Ended Outputs)**
   The sysIO buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input. In these banks the two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential I/O, and the comp (complementary) pad is associated with the negative side of the differential I/O.

   LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

4. **Bank 8 sysIO Buffer Pairs (Single-Ended Outputs, Only on Shared Pins When Not Used by Configuration)**
   The sysIO buffers in Bank 8 consist of single-ended output drivers and single-ended input buffers (both ratioed and referenced). The referenced input buffer can also be configured as a differential input.

   The two pads in the pair are described as "true" and "comp", where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, V_{CCIO8} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information on controlling the output logic state with valid input logic levels during power-up in LatticeECP2 devices, see details of additional technical documentation at the end of this data sheet.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

Supported Standards

The LatticeECP2 sysIO buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTL and other standards. The buffers support the LVTTL, LVCMOS 1.2V, 1.5V, 1.8V, 2.5V and 3.3V standards. In the LVCMOS and LVTTL modes, the buffer has individual configuration options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, MLVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. Tables 2-13 and 2-14 show the I/O standards (together with their supply and reference voltages) supported by LatticeECP2 devices. For further information on utilizing the sysIO buffer to support a variety of standards please see the details of additional technical information at the end of this data sheet.

Table 2-13. Supported Input Standards

Input Standard	V_{REF} (Nom.)	V_{CCIO}[1] (Nom.)
Single Ended Interfaces		
LVTTL	—	—
LVCMOS33	—	—
LVCMOS25	—	—
LVCMOS18	—	1.8
LVCMOS15	—	1.5
LVCMOS12	—	—
PCI 33	—	3.3
HSTL18 Class I, II	0.9	—
HSTL15 Class I	0.75	—
SSTL3 Class I, II	1.5	—
SSTL2 Class I, II	1.25	—
SSTL18 Class I, II	0.9	—
Differential Interfaces		
Differential SSTL18 Class I, II	—	—
Differential SSTL2 Class I, II	—	—
Differential SSTL3 Class I, II	—	—
Differential HSTL15 Class I	—	—
Differential HSTL18 Class I, II	—	—
LVDS, MLVDS, LVPECL, BLVDS, RSDS	—	—

1 When not specified, V_{CCIO} can be set anywhere in the valid operating range.

Table 2-14. Supported Output Standards

Output Standard	Drive	V_{CCIO} (Nom.)
Single-ended Interfaces		
LVTTL	4mA, 8mA, 12mA, 16mA, 20mA	3.3
LVCMOS33	4mA, 8mA, 12mA 16mA, 20mA	3.3
LVCMOS25	4mA, 8mA, 12mA, 16mA, 20mA	2.5
LVCMOS18	4mA, 8mA, 12mA, 16mA	1.8
LVCMOS15	4mA, 8mA	1.5
LVCMOS12	2mA, 6mA	1.2
LVCMOS33, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS25, Open Drain	4mA, 8mA, 12mA 16mA, 20mA	—
LVCMOS18, Open Drain	4mA, 8mA, 12mA 16mA	—
LVCMOS15, Open Drain	4mA, 8mA	—
LVCMOS12, Open Drain	2mA, 6mA	—
PCI33/PCIX†	N/A	3.3
HSTL18 Class I, II	N/A	1.8
HSTL15 Class I	N/A	1.5
SSTL3 Class I, II	N/A	3.3
SSTL2 Class I, II	N/A	2.5
SSTL18 Class I, II	N/A	1.8
Differential Interfaces		
Differential SSTL3, Class I, II	N/A	3.3
Differential SSTL2, Class I, II	N/A	2.5
Differential SSTL18, Class I, II	N/A	1.8
Differential HSTL18, Class I, II	N/A	1.8
Differential HSTL15, Class I	N/A	1.5
LVDS	N/A	2.5
MLVDS[1]	N/A	2.5
BLVDS[1]	N/A	2.5
LVPECL[1]	N/A	3.3
RSDS[1]	N/A	2.5

1. Emulated with external resistors. For more detail, please see information regarding additional technical documentation at the end of this data sheet.

Hot Socketing

LatticeECP2 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Power supplies can be sequenced in any order. During power-up and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LatticeECP2 ideal for many multiple power supply and hot-swap applications.

Configuration and Testing

This section describes the configuration and testing features of the LatticeECP2 family of devices.

IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeECP2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/Os: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CCJ} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards.

For more details on boundary scan test, please see information regarding additional technical documentation at the end of this data sheet.

Device Configuration

All LatticeECP2 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support both byte-wide and serial configuration. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. The sysCONFIG port is a 20-pin interface with six I/Os used as dedicated pins with the remainder used as dual-use pins. See Lattice technical note number TN1108, *LatticeECP2 sysCONFIG Usage Guide* for more information on using the dual-use pins as general purpose I/Os.

There are five ways to configure a LatticeECP2 device:

1. Industry standard SPI serial memories
2. Industry standard byte wide flash with an ispMACH™ 4000, providing control and addressing
3. System microprocessor to drive a sysCONFIG port or JTAG TAP
4. Industry standard FPGA boot PROM memory
5. JTAG

On power-up, the FPGA SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it will remain active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port.

Enhanced Configuration Option

LatticeECP2 devices have enhanced configuration features such as: decryption support, TransFR™ I/O and dual boot image support.

1. **Decryption Support**
   LatticeECP2 devices provide on-chip, non-volatile key storage to support decryption of a 128-bit AES encrypted bitstream, securing designs and deterring design piracy. The decryption block supports nearly all the programming modes.

2. **TransFR (Transparent Field Reconfiguration)**
   TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. See Lattice technical note number TN1087, *Minimizing System Interruption During Configuration Using TransFR Technology,* for details.

3. **Dual Boot Image Support**
   Dual boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeECP2 can be re-booted from this new configuration file. If there is a problem such as corrupt data during down or incorrect version number with this new boot image, the LatticeECP2 device can revert back to the original backup configuration and try again. This all can be done without power cycling the system.

For more information on device configuration, please see details of additional technical documentation at the end of this data sheet.

Software Error Detect (SED) Support

LatticeECP2 devices have dedicated logic to perform CRC checking of the bitstream and can be programmed such that, if an error occurs, the device will reload from a known good boot image or generate an error signal and stop configuring.

For more information on Software Error Detect support, please see details of additional technical documentation at the end of this data sheet.

External Resistor

LatticeECP2 devices require a single external, 10K ohm +/- 1% value between the XRES pin and ground. Device configuration will not be completed if this resistor is missing. There is no boundary scan register on the external resistor pad.

On-Chip Oscillator

Every LatticeECP2 device has an internal CMOS oscillator which is used to derive a Master Clock for configuration. The oscillator and the Master Clock run continuously and are available to user logic after configuration is completed. The default value of the Master Clock is 2.5MHz. Table 2-15 lists all the available Master Clock frequencies. When a different Master Clock is selected during the design process, the following sequence takes place:

1. User selects a different Master Clock frequency
2. During configuration the device starts with the default (2.5MHz) Master Clock frequency
3. The clock configuration settings are contained in the early configuration bitstream
4. The Master Clock frequency changes to the selected frequency once the clock configuration bits are received.

This internal CMOS oscillator is available to the user by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, please see details of additional technical documentation at the end of this data sheet.

Table 2-15. Selectable Master Clock (CCLK) Frequencies During Configuration

CCLK (MHz)	CCLK (MHz)	CCLK (MHz)
2.5[1]	13	45
4.3	15	51
5.4	20	55
6.9	26	60
8.1	30	130
9.2	34	—
10.0	41	—

1. Default frequency.

Density Shifting

The LatticeECP2 family is designed to ensure that different density devices in the same package have the same pin-out. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization will impact the likely success in each case.

LatticeECP2 Family Data Sheet DC and Switching Characteristics

February 2006 Advance Data Sheet

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . . -0.5 to 1.32V

Supply Voltage V_{CCAUX} . . . . . -0.5 to 3.75V

Supply Voltage V_{CCJ} . . . . . -0.5 to 3.75V

Output Supply Voltage V_{CCIO} . . . . . -0.5 to 3.75V

Input or I/O Tristate Voltage Applied[4] . . . . . -0.5 to 3.75V

Storage Temperature (Ambient) . . . . . -65 to 150°C

Junction Temperature (Tj) . . . . . +125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Core Supply Voltage	1.14	1.26	V
V_{CCAUX}	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCIO}[1, 2]	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}[1]	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t_{JCOM}	Junction Commercial Operation	0	85	°C
t_{JIND}	Junction Industrial Operation	-40	100	°C

1. If V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as V_{CC}. If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX}.
2. See recommended voltages by I/O standard in subsequent table.

Hot Socketing Specifications[1, 2, 3, 4]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O Leakage Current	$0 \le V_{IN} \le V_{IH}$ (MAX.)	—	—	+/-1000	µA

1. Insensitive to sequence of V_{CC}, V_{CCAUX} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX} and V_{CCIO}.
2. $0 \le V_{CC} \le V_{CC}$ (MAX), $0 \le V_{CCIO} \le V_{CCIO}$ (MAX) or $0 \le V_{CCAUX} \le V_{CCAUX}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
4. LVCMOS and LVTTL only.
5. Note this table represents DC conditions. For the first 20ns after hot insertion, current specification is 8mA.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Low Leakage	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	10	µA
I_{PU}	I/O Active Pull-up Current	$0 \le V_{IN} \le 0.7\ V_{CCIO}$	-30	—	-210	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\le V_{IN} \le V_{IH}$ (MAX)	30	—	210	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCIO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	210	µA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \le V_{IN} \le V_{IH}$ (MAX)	—	—	-210	µA
V_{BHT}	Bus Hold Trip Points	$0 \le V_{IN} \le V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz.

Supply Current (Standby)[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical[5]	Units
I_{CC}	Core Power Supply Current	ECP2-6		mA
		ECP2-12		mA
		ECP2-20		mA
		ECP2-35		mA
		ECP2-50		mA
		ECP2-70		mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2-6		mA
		ECP2-12		mA
		ECP2-20		mA
		ECP2-35		mA
		ECP2-50		mA
		ECP2-70		mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)			mA
I_{CCSPLL}	SPLL Power Supply Current (per SPLL)			mA
I_{CCIO}	Bank Power Supply Current[6]			mA
I_{CCJ}	V_{CCJ} Power Supply Current			mA

1. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
2. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
3. Frequency 0MHz.
4. Pattern represents a “blank” configuration data file.
5. T_J = 25°C, power supplies at nominal voltage.
6 Per bank.

Initialization Supply Current[1, 2, 3, 4, 5, 6]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typical[5]	Units
I_{CC}	Core Power Supply Current	ECP2-6		mA
		ECP2-12		mA
		ECP2-20		mA
		ECP2-35		mA
		ECP2-50		mA
		ECP2-70		mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2-6		mA
		ECP2-12		mA
		ECP2-20		mA
		ECP2-35		mA
		ECP2-50		mA
		ECP2-70		mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)			mA
I_{CCSPLL}	SPLL Power Supply Current (per SPLL)			mA
I_{CCIO}	Bank Power Supply Current[7]			mA
I_{CCJ}	VCCJ Power Supply Current			mA

1. Until DONE signal is active.
2. For further information on supply current, please see details of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
4. Frequency 0MHz.
5. T_J = 25°C, power supplies at nominal voltage.
6. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.
7. Per bank.

sysIO Recommended Operating Conditions

Standard	V_{CCIO}			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3[2]	3.135	3.3	3.465	—	—	—
LVCMOS 2.5[2]	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2[2]	1.14	1.2	1.26	—	—	—
LVTTL[2]	3.135	3.3	3.465	—	—	—
PCI	3.135	3.3	3.465	—	—	—
SSTL18[2] Class I, II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL2[2] Class I, II	2.375	2.5	2.625	1.15	1.25	1.35
SSTL3[2] Class I, II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL[2] Class I	1.425	1.5	1.575	0.68	0.75	0.9
HSTL[2] 18 Class I, II	1.71	1.8	1.89	0.816	0.9	1.08
LVDS[2]	2.375	2.5	2.625	—	—	—
MLVDS25[1]	2.375	2.5	2.625	—	—	—
LVPECL33[1, 2]	3.135	3.3	3.465	—	—	—
BLVDS25[1, 2]	2.375	2.5	2.625	—	—	—
RSDS[1, 2]	2.375	2.5	2.625	—	—	—
SSTL18D_I[2], II[2]	1.71	1.8	1.89	—	—	—
SSTL25D_ I[2], II[2]	2.375	2.5	2.625	—	—	—
SSTL33D_ I[2], II[2]	3.135	3.3	3.465	—	—	—
HSTL15D_ I[2], II[2]	1.425	1.5	1.575	—	—	—
HSTL18D_ I[2], II[2]	1.71	1.8	1.89	—	—	—

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. Input on this standard does not depend on the value of V_{CCIO}.

sysIO Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}		I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)	Max. (V)	Min. (V)		
LVCMOS 3.3	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCIO} - 0.4	20, 16, 12, 8, 4	-20, -16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.8	-0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	16, 12, 8, 4	-16, -12, -8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.5	-0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	8, 4	-8, -4
					0.2	V_{CCIO} - 0.2	0.1	-0.1
LVCMOS 1.2	-0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	3.6	0.4	V_{CCIO} - 0.4	6, 2	-6, -2
					0.2	V_{CCIO} - 0.2	0.1	-0.1
PCI	-0.3	0.3 V_{CCIO}	0.5 V_{CCIO}	3.6	0.1 V_{CCIO}	0.9 V_{CCIO}	1.5	-0.5
SSTL3 Class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCIO} - 1.1	8	-8
SSTL3 Class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCIO} - 0.9	16	-16
SSTL2 Class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCIO} - 0.62	7.6	-7.6
							12	-12
SSTL2 Class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCIO} - 0.43	15.2	-15.2
							20	-20
SSTL18 Class I	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.4	V_{CCIO} - 0.4	6.7	-6.7
SSTL18 Class II	-0.3	V_{REF} - 0.125	V_{REF} + 0.125	3.6	0.28	V_{CCIO} - 0.28	8	-8
							11	-11
HSTL Class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	4	-4
							8	-8
HSTL18 Class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	8	-8
							12	-12
HSTL18 Class II	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCIO} - 0.4	16	-16

1. The average DC current drawn by I/Os between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8mA, where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank.

sysIO Differential Electrical Characteristics

LVDS

Over Recommended Operating Conditions

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage		0	—	2.4	V
V_{CM}	Input Common Mode Voltage	Half the Sum of the Two Inputs	0.05	—	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	+/-100	—	—	mV
I_{IN}	Input Current	Power On or Power Off	—	—	+/-10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	—	1.38	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100 Ohm	0.9V	1.03	—	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100 Ohm	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		—	—	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100 Ohm	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between H and L		—	—	50	mV
I_{SA},I_{SA}	Output Short Circuit Current	V_{OD} = 0V Driver Outputs Shorted to Ground	—	—	24	mA
I_{SAB}	Output Short Circuit Current	V_{OD} = 0V Driver Outputs Shorted to Each Other	—	—	12	mA

Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details of additional technical information at the end of this data sheet.

LVDS25E

The top and bottom sides of LatticeECP2 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in Figure 3-1 is one possible solution for point-to-point signals.

Figure 3-1. LVDS25E Output Termination Example

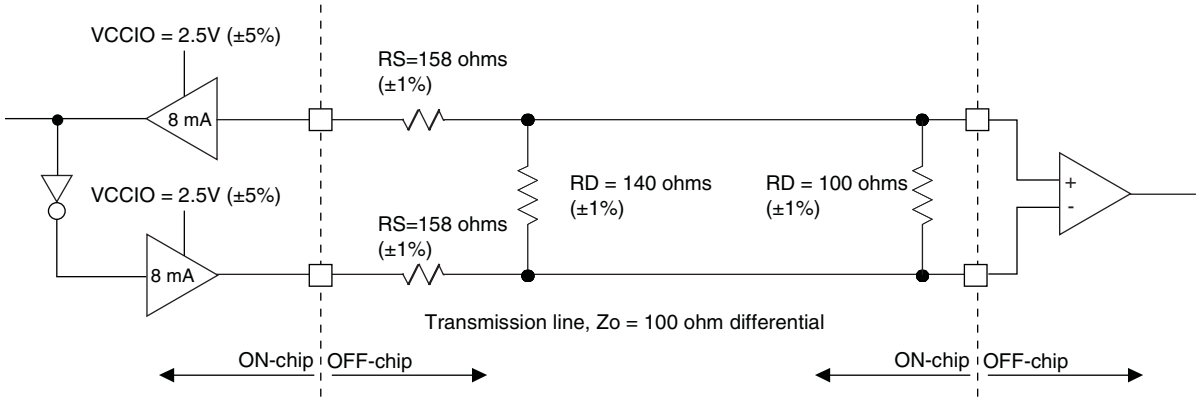


Table 3-1. LVDS25E DC Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/-1%)	158	Ω
R_P	Driver Parallel Resistor (+/-1%)	140	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage (after R_1)	1.43	V
V_{OL}	Output Low Voltage (after R_1)	1.07	V
V_{OD}	Output Differential Voltage (After R_1)	0.35	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	6.03	mA

BLVDS

The LatticeECP2 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3-2 is one possible solution for bi-directional multi-point differential signals.

Figure 3-2. BLVDS Multi-point Output Example

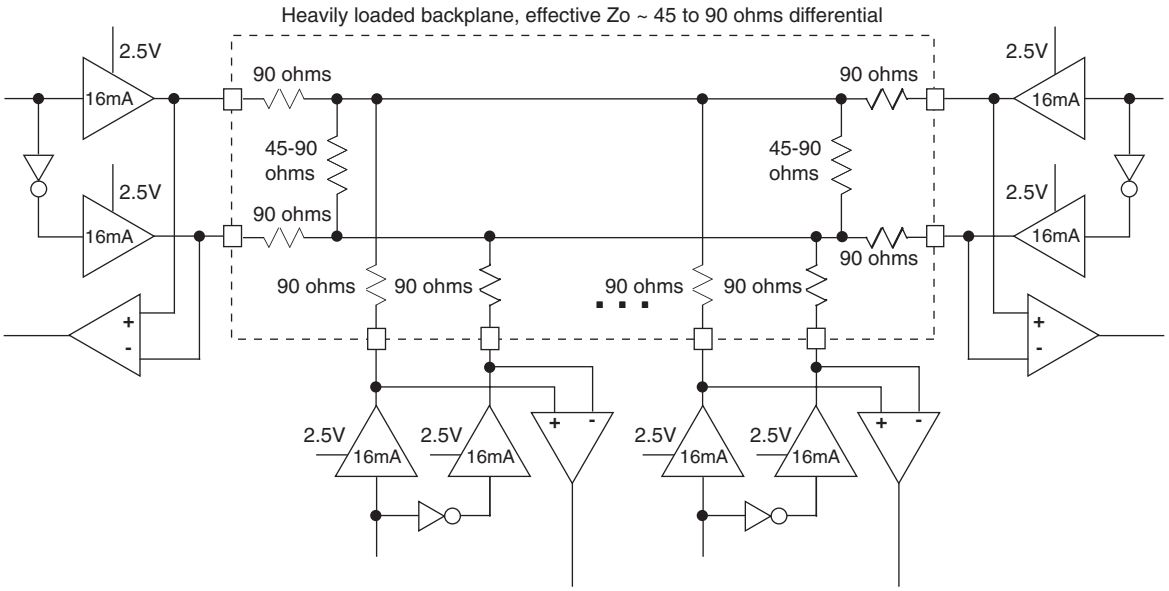


Table 3-2. BLVDS DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical		Units
		Zo = 45Ω	Zo = 45Ω	
V_{CCIO}	Output Driver Supply (+/- 5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/- 1%)	90.00	90.00	Ω
R_{TLEFT}	Driver Parallel Resistor (+/- 1%)	45.00	90.00	Ω
R_{TRIGHT}	Receiver Termination (+/- 1%)	45.00	90.00	Ω
V_{OH}	Output High Voltage (After R1)	1.38	1.48	V
V_{OL}	Output Low Voltage (After R1)	1.12	1.02	V
V_{OD}	Output Differential Voltage (After R1)	0.25	0.46	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	11.24	10.20	mA

1. For input buffer, see LVDS table.

LVPECL

The LatticeECP2 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-3 is one possible solution for point-to-point signals.

Figure 3-3. Differential LVPECL

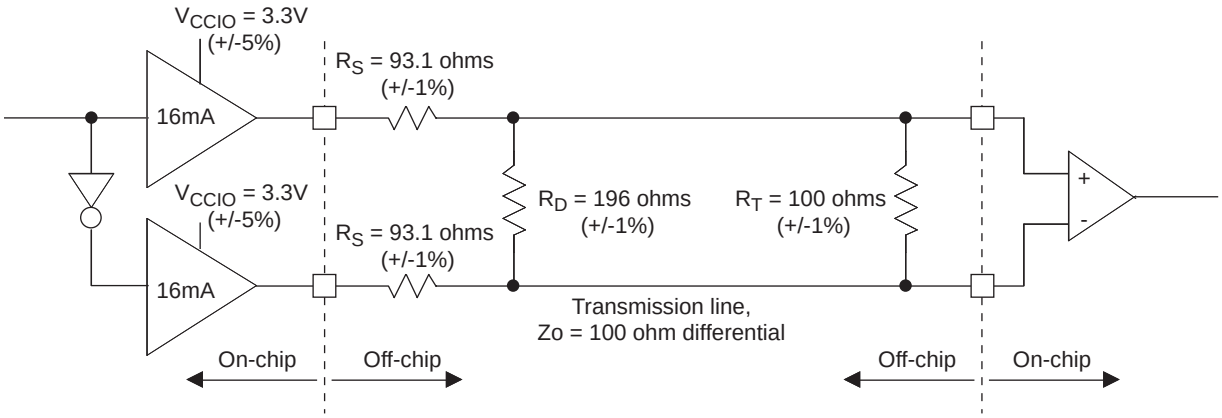


Table 3-3. LVPECL DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	3.30	V
Z_{OUT}	Driver Impedance	10	Ω
R_S	Driver Series Resistor (+/-1%)	93	Ω
R_P	Driver Parallel Resistor (+/-1%)	196	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage (After R_1)	2.05	V
V_{OL}	Output Low Voltage (After R_1)	1.25	V
V_{OD}	Output Differential Voltage (After R_1)	0.80	V
V_{CM}	Output Common Mode Voltage	1.65	V
Z_{BACK}	Back Impedance	100.5	Ω
I_{DC}	DC Output Current	12.11	mA

1. For input buffer, see LVDS table.

RSDS

The LatticeECP2 devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-4 is one possible solution for RSDS standard implementation. Resistor values in Figure 3-4 are industry standard values for 1% resistors.

Figure 3-4. RSDS (Reduced Swing Differential Standard)

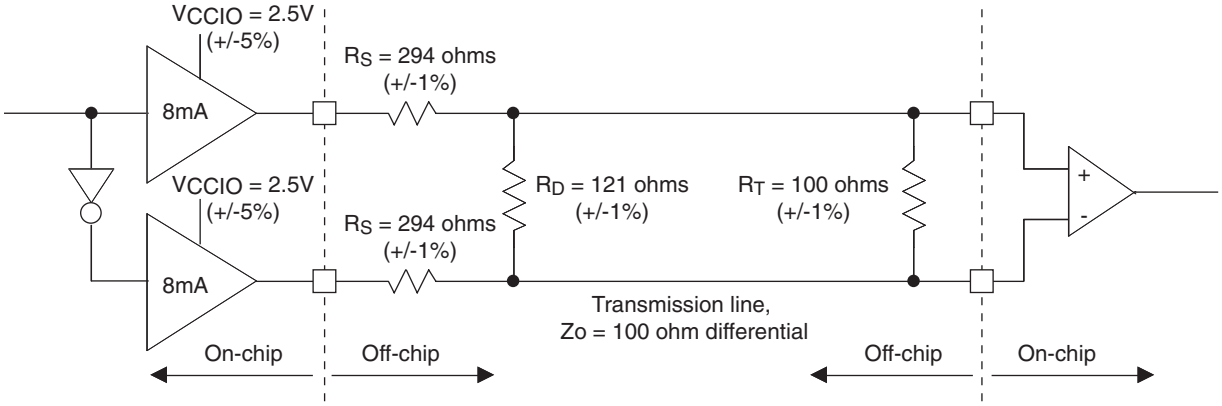


Table 3-4. RSDS DC Conditions[1]

Over Recommended Operating Conditions

Parameter	Description	Typical	Units
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	V
Z_{OUT}	Driver Impedance	20	Ω
R_S	Driver Series Resistor (+/-1%)	294	Ω
R_P	Driver Parallel Resistor (+/-1%)	121	Ω
R_T	Receiver Termination (+/-1%)	100	Ω
V_{OH}	Output High Voltage (After R_1)	1.35	V
V_{OL}	Output Low Voltage (After R_1)	1.15	V
V_{OD}	Output Differential Voltage (After R_1)	0.20	V
V_{CM}	Output Common Mode Voltage	1.25	V
Z_{BACK}	Back Impedance	101.5	Ω
I_{DC}	DC Output Current	3.66	mA

1. For input buffer, see LVDS table.

MLVDS

The LatticeECP2 devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3-5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3-5 are industry standard values for 1% resistors.

Figure 3-5. MLVDS (Reduced Swing Differential Standard)

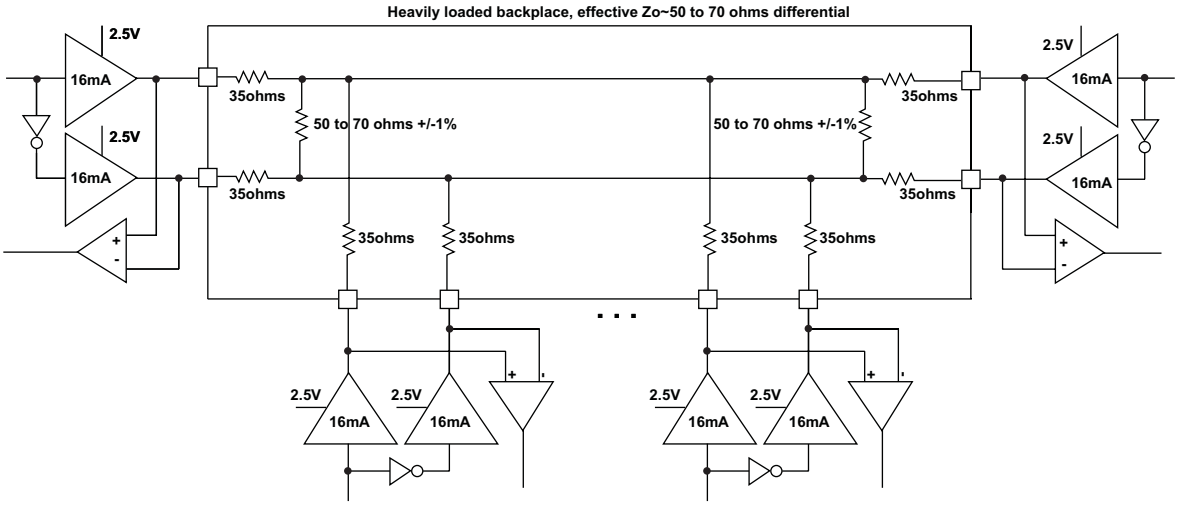


Table 3-5. MLVDS DC Conditions[1]

Parameter	Description	Typical		Units
		Zo=50Ω	Zo=70Ω	
V_{CCIO}	Output Driver Supply (+/-5%)	2.50	2.50	V
Z_{OUT}	Driver Impedance	10.00	10.00	Ω
R_S	Driver Series Resistor (+/-1%)	35.00	35.00	Ω
R_{TLEFT}	Driver Parallel Resistor (+/-1%)	50.00	70.00	Ω
R_{TRIGHT}	Receiver Termination (+/-1%)	50.00	70.00	Ω
V_{OH}	Output High Voltage (After R_1)	1.52	1.60	V
V_{OL}	Output Low Voltage (After R_1)	0.98	0.90	V
V_{OD}	Output Differential Voltage (After R_1)	0.54	0.70	V
V_{CM}	Output Common Mode Voltage	1.25	1.25	V
I_{DC}	DC Output Current	21.74	20.00	mA

1. For input buffer, see LVDS table.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces please see details of additional technical information at the end of this data sheet.

Typical Building Block Function Performance[1]

Pin-to-Pin Performance (LVCMOS25 12mA Drive)

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	6.4	ns
32-bit Decoder	10.0	ns
64-bit Decoder	18.4	ns
4:1 MUX	3.6	ns
8:1 MUX	3.6	ns
16:1 MUX	4.1	ns
32:1 MUX	4.6	ns

Register-to-Register Performance

Function	-7 Timing	Units
Basic Functions		
16-bit Decoder	518	MHz
32-bit Decoder	335	MHz
64-bit Decoder	316	MHz
4:1 MUX	785	MHz
8:1 MUX	618	MHz
16:1 MUX	575	MHz
32:1 MUX	247	MHz
8-bit Adder	458	MHz
16-bit Adder	371	MHz
64-bit Adder	247	MHz
16-bit Counter	469	MHz
32-bit Counter	362	MHz
64-bit Counter	249	MHz
64-bit Accumulator	242	MHz
Embedded Memory Functions		
512x36 Single Port RAM, EBR Output Registers	353	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers)	353	MHz
1024x18 True-Dual Port RAM (Read-Before-Write, EBR Output Registers)	280	MHz
1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers)	260	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (One PFU)	864	MHz
32x2 Pseudo-Dual Port RAM	461	MHz
64x1 Pseudo-Dual Port RAM	349	MHz
DSP Functions		
18x18 Multiplier (All Registers)	479	MHz
9x9 Multiplier (All Registers)	479	MHz

Register-to-Register Performance (Continued)

Function	-7 Timing	Units
36x36 Multiply (All Registers)	422	MHz
18x18 Multiply/Accumulate (Input and Output Registers)	TBA	MHz
18x18 Multiply-Add/Sub-Sum (All Registers)	479	MHz
DSP IP Functions		
16-Tap Fully-Parallel FIR Filter	TBA	MHz
1024-pt, Radix 4, Decimation in Frequency FFT	TBA	MHz
8X8 Matrix Multiplication	TBA	MHz

1. These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with device, design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

Timing v. A0.01

Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the ispLEVER design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The ispLEVER design tool can provide logic timing numbers at a particular temperature and voltage.

LatticeECP2 External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
General I/O Pin Parameters (Using Primary Clock without PLL)[1]									
t_{CO}	Clock to Output - PIO Output Register	LFEC2-50	—	3.49	—	3.79	—	4.10	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LFEC2-50	0.24	—	0.15	—	0.09	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	LFEC2-50	0.02	—	0.11	—	0.23	—	ns
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFEC2-50		—		—		—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFEC2-50		—		—		—	ns
f_{MAX_IO}	Clock Frequency of I/O and PFU Register	LFEC2-50	—		—		—		MHz
General I/O Pin Parameters (Using Primary Clock with PLL)[1]									
t_{COPLL}	Clock to Output - PIO Output Register	LFEC2-50	—		—		—		ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	LFEC2-50		—		—		—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	LFEC2-50		—		—		—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFEC2-50		—		—		—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFEC2-50		—		—		—	ns
DDR[2] and DDR2[3] I/O Pin Parameters									
t_{DVADQ}	Data Valid After DQS (DDR Read)	LFEC2-50	—		—		—		UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	LFEC2-50		—		—		—	UI
t_{DQVBS}	Data Valid Before DQS	LFEC2-50		—		—		—	UI
t_{DQVAS}	Data Valid After DQS	LFEC2-50		—		—		—	UI
f_{MAX_DDR}	DDR Clock Frequency[6]	LFEC2-50	—		—		—		MHz
f_{MAX_DDR2}	DDR Clock Frequency	LFEC2-50	—		—		—		MHz
SPI4.2 I/O Pin Parameters[4]									
$t_{DVACLKSPI}$	Data Valid After CLK	LFEC2-50	—		—		—		ps
$t_{DVECLKSPI}$	Data Hold After CLK	LFEC2-50		—		—		—	ps
t_{DIASPI}	Data Invalid After Clock	LFEC2-50	—		—		—		ps
t_{DIBSPI}	Data Invalid Before Clock	LFEC2-50	—		—		—		ps
SFI4 I/O Pin Parameters[4]									
$t_{DVACLKSFI}$	Data Valid After DQS (DDR Read)	LFEC2-50	—		—		—		ps
$t_{DVECLKSFI}$	Data Hold After DQS (DDR Read)	LFEC2-50		—		—		—	ps
t_{DIASFI}	Data Invalid After Clock	LFEC2-50	—		—		—		ps
t_{DIBSFI}	Data Invalid Before Clock	LFEC2-50	—		—		—		ps
XGMII I/O Pin Parameters[5]									
$t_{SUXGMII}$	Data Setup Before Read Clock	LFEC2-50		—		—		—	ps
t_{HXGMII}	Data Hold After Read Clock	LFEC2-50		—		—		—	ps

LatticeECP2 External Switching Characteristics (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7		-6		-5		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
$t_{DQVBCLKXGMII}$	Data Invalid Before Strobe/Clock	LFEC2-50		—		—		—	ps
$t_{DQVACLKXGMII}$	Data Invalid After Strobe/Clock	LFEC2-50		—		—		—	ps
Primary									
f_{MAX_PRI}	Frequency for Primary Clock Tree	LFEC2-50	—		—		—		MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	LFEC2-50		—		—		—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	LFEC2-50	—		—		—		ps
Secondary Clocks									
f_{MAX_SEC}	Frequency for Secondary Clock Tree	LFEC2-50	—		—		—		MHz
t_{W_SEC}	Clock Pulse Width for Secondary Clock	LFEC2-50		—		—		—	ns
Edge Clocks (ECK1 and ECK2)									
f_{MAX_ECK}	Frequency for Edge Clock	LFEC2-50	—		—		—		MHz
t_{W_ECK}	Clock Pulse Width for ECK	LFEC2-50		—		—		—	ns
t_{SKEW_ECK}	ECK Skew Within an Edge of the Device	LFEC2-50	—		—		—		ps

1. General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
2. DDR timing numbers based on SSTL25.
3. DDR2 timing numbers based on SSTL18.
4. SPI4.2 and SFI4 timing numbers based on LVDS25.
5. XGMII timing numbers based on HSTL class I.
6. Device supports DDR and DDR2 memory data rates down to 95MHz.

Timing v. A0.01

Figure 3-6. SPI4.2 and SFI Transmit Parameters

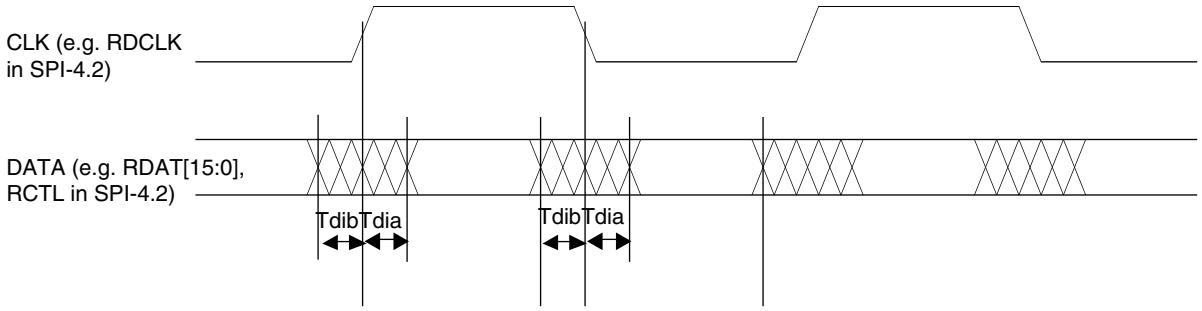


Figure 3-7. DDR1,DDR2, XGMII Transmit Parameters

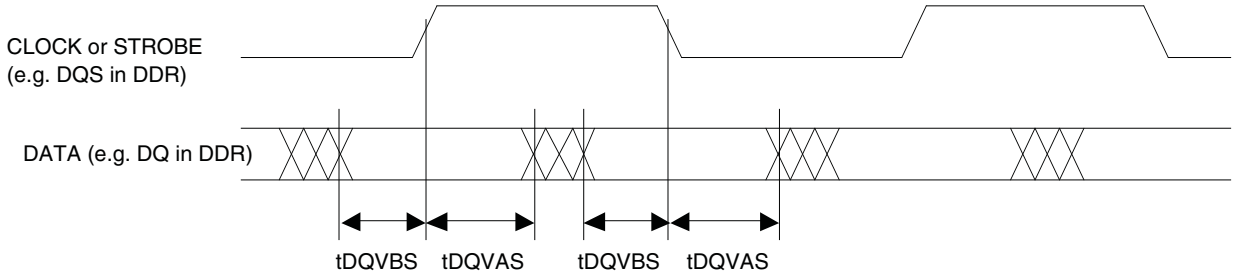


Figure 3-8. XGMII Receiver Parameters

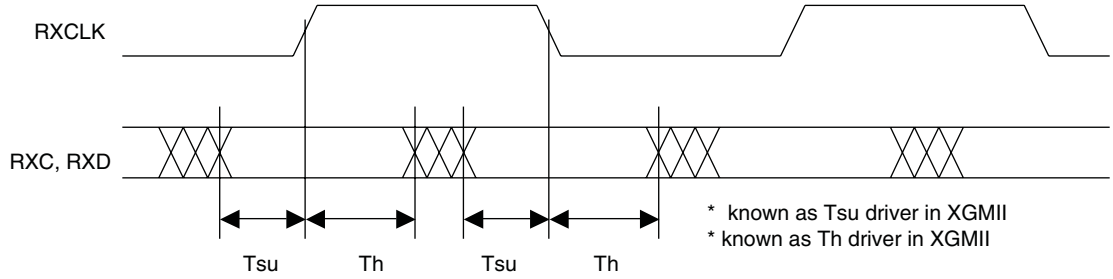
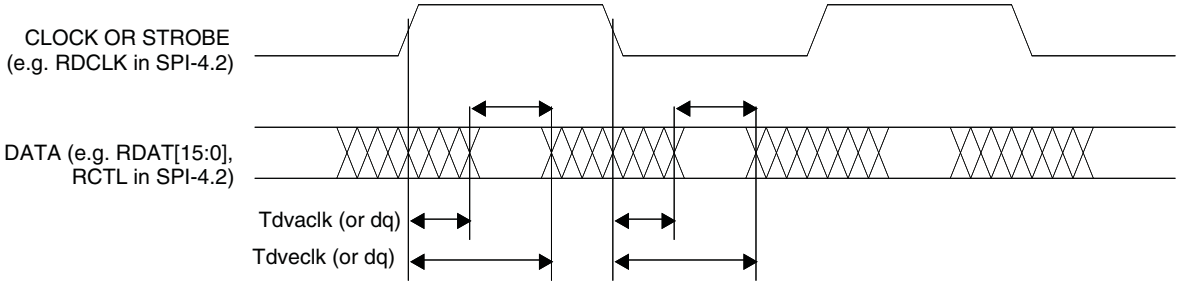


Figure 3-9. DDR1, DDR2, SPI4.2, SFI4 Receiver Parameters



LatticeECP2 Internal Switching Characteristics[1]

Over Recommended Operating Conditions

Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
PFU Logic Mode Timing								
t_{LUT4_PFU}	LUT4 Delay (A to D Inputs to F Output)	—		—		—		ns
t_{LUT6_PFU}	LUT6 Delay (A to D Inputs to OFX Output)	—		—		—		ns
t_{LSR_PFU}	Set/Reset to Output (Asynchronous)	—		—		—		ns
t_{SUM_PFU}	Clock to Mux (M0, M1) Input Setup Time		—		—		—	ns
t_{HM_PFU}	Clock to Mux (M0, M1) Input Hold Time		—		—		—	ns
t_{SUD_PFU}	Clock to D Input Setup Time		—		—		—	ns
t_{HD_PFU}	Clock to D Input Hold Time		—		—		—	ns
t_{CK2Q_PFU}	Clock to Q Delay, (D-type Register Configuration)	—		—		—		ns
PFU Memory Mode Timing								
t_{CORAM_PFU}	Clock to Output Write (F Port)	—		—		—		ns
t_{SUDATA_PFU}	Data Setup Time		—		—		—	ns
t_{HDATA_PFU}	Data Hold Time		—		—		—	ns
t_{SUADDR_PFU}	Address Setup Time		—		—		—	ns
t_{HADDR_PFU}	Address Hold Time		—		—		—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time		—		—		—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time		—		—		—	ns
PIO Input/Output Buffer Timing								
t_{IN_PIO}	Input Buffer Delay (LVCMOS25)	—		—		—		ns
t_{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—		—		—		ns
t_{SUI_PIO}	Input Register Setup Time (Data Before Clock)		—		—		—	ns
t_{HI_PIO}	Input Register Hold Time (Data After Clock)		—		—		—	ns
t_{COO_PIO}	Output Register Clock to Output Delay	—		—		—		ns
t_{SUCE_PIO}	Input Register Clock Enable Setup Time		—		—		—	ns
t_{HCE_PIO}	Input Register Clock Enable Hold Time		—		—		—	ns
t_{SULSR_PIO}	Set/Reset Setup Time		—		—		—	ns
t_{HLSR_PIO}	Set/Reset Hold Time		—		—		—	ns
EBR Timing								
t_{CO_EBR}	Clock (Read) to Output from Address or Data	—		—		—		ns
t_{COO_EBR}	Clock (Write) to Output from EBR Output Register	—		—		—		ns
t_{SUDATA_EBR}	Setup Data to EBR Memory (Write Clk)		—		—		—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory (Write Clk)		—		—		—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memory (Write Clk)		—		—		—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory (Write Clk)		—		—		—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to EBR Memory (Write/Read Clk)		—		—		—	ns
t_{HWREN_EBR}	Hold Write/Read Enable to EBR Memory (Write/Read Clk)		—		—		—	ns

LatticeECP2 Internal Switching Characteristics[1] (Continued)

Over Recommended Operating Conditions

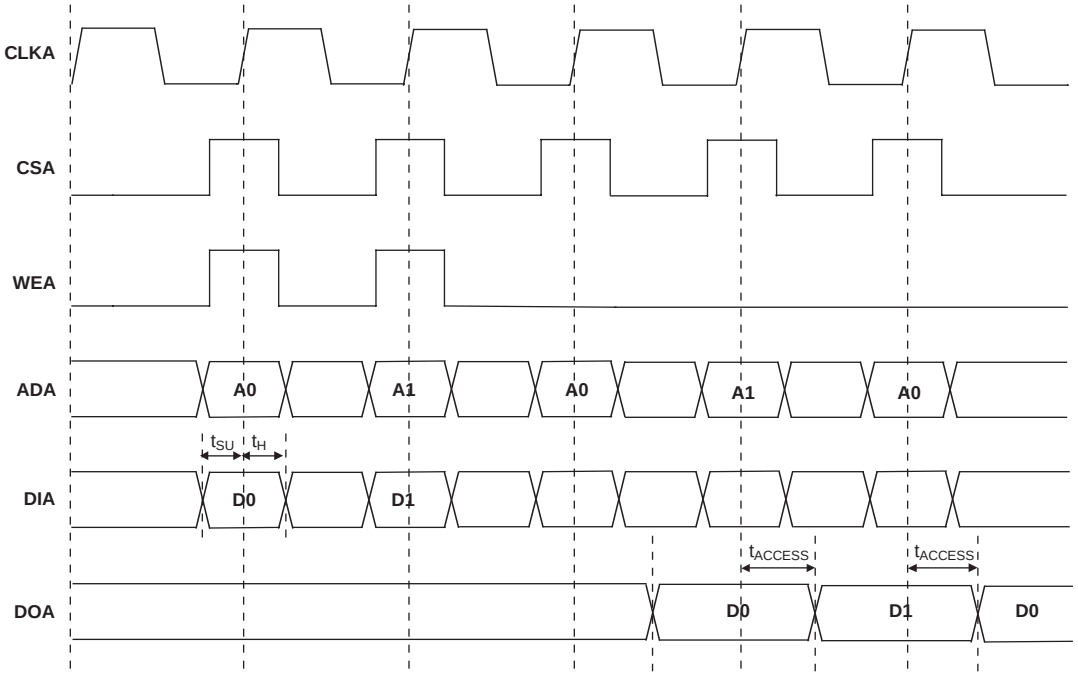
Parameter	Description	-7		-6		-5		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{SUCE_EBR}	Clock Enable Setup Time to EBR Output Register (Read Clk)		—		—		—	ns
t_{HCE_EBR}	Clock Enable Hold Time to EBR Output Register (Read Clk)		—		—		—	ns
t_{RSTO_EBR}	Reset To Output Delay Time from EBR Output Register (Asynchronous)	—		—		—		ns
t_{SUBE_EBR}	Byte Enable Set-Up Time to EBR Output Register		—		—		—	ns
t_{HBE_EBR}	Byte Enable Hold Time to EBR Output Register		—		—		—	ns
Dynamic Delay on Each PIO								
$t_{DEL\_ADJ\_RNG}$	Delay Adjustment Range (in Nine Delay Steps)							ps
GPLL Parameters								
t_{RSTREC_GPLL}		—		—		—		ns
t_{RSTSU_GPLL}			—		—		—	ns
SPLL Parameters								
t_{RSTREC_SPLL}		—		—		—		ns
t_{RSTSU_SPLL}			—		—		—	ns
DSP Block Timing								
t_{SUI_DSP}	Input Register Setup Time		—		—		—	ns
t_{HI_DSP}	Input Register Hold Time		—		—		—	ns
t_{SUP_DSP}	Pipeline Register Setup Time		—		—		—	ns
t_{HP_DSP}	Pipeline Register Hold Time		—		—		—	ns
t_{SUO_DSP}	Output Register Setup Time		—		—		—	ns
t_{HO_DSP}	Output Register Hold Time		—		—		—	ns
t_{COI_DSP}[2]	Input Register Clock to Output Time	—		—		—		ns
t_{COP_DSP}[2]	Pipeline Register Clock to Output Time	—		—		—		ns
t_{COO_DSP}[2]	Output Register Clock to Output Time	—		—		—		ns
$t_{SUADSUB}$	AdSub Input Register Setup Time		—		—		—	ns
t_{HADSUB}	AdSub Input Register Hold Time		—		—		—	ns

1. Internal parameters are characterized but not tested on every device.
2. These parameters include the Adder Subtractor block in the path.

Timing v.

Timing Diagrams

Figure 3-10. Read/Write Mode (Normal)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-11. Read/Write Mode with Input and Output Registers

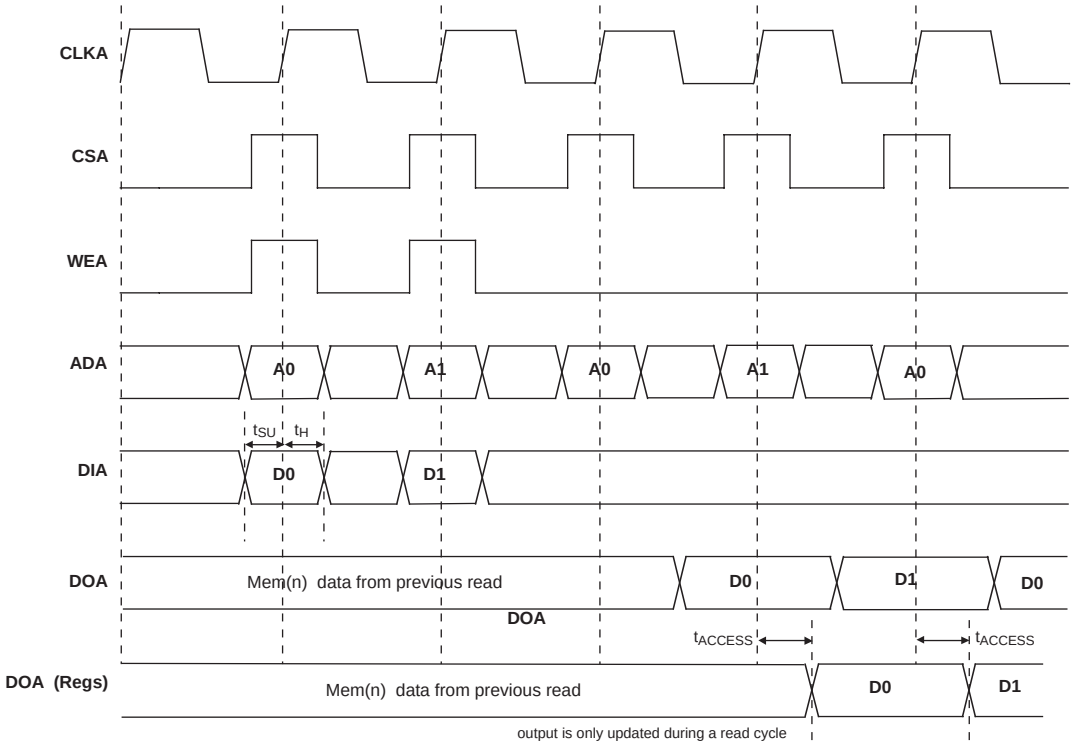
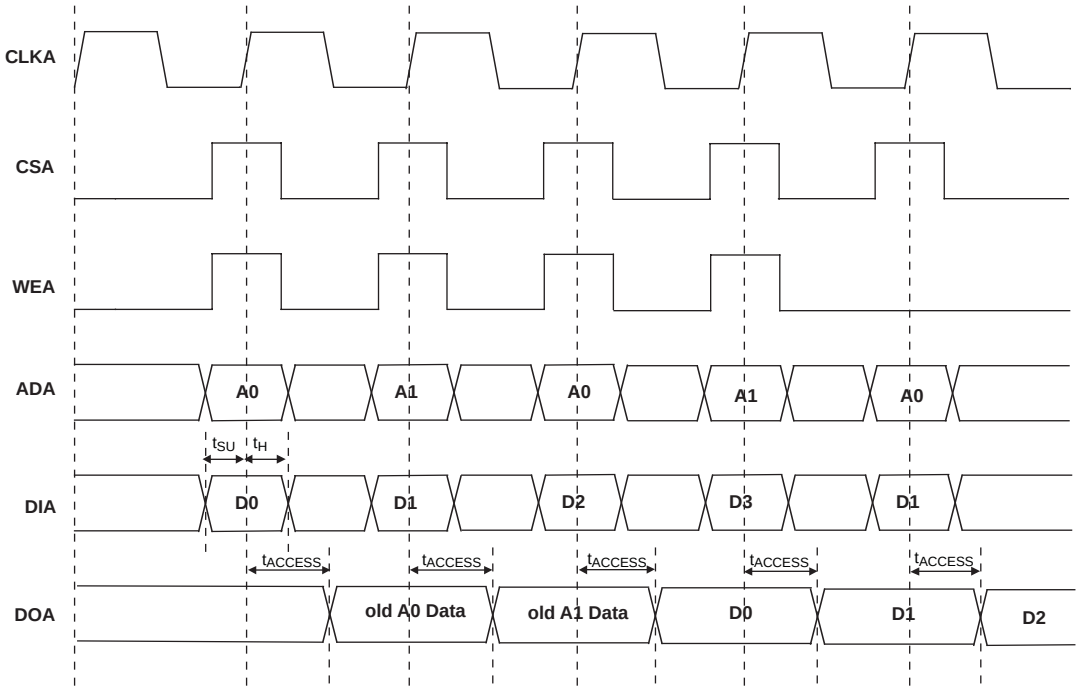
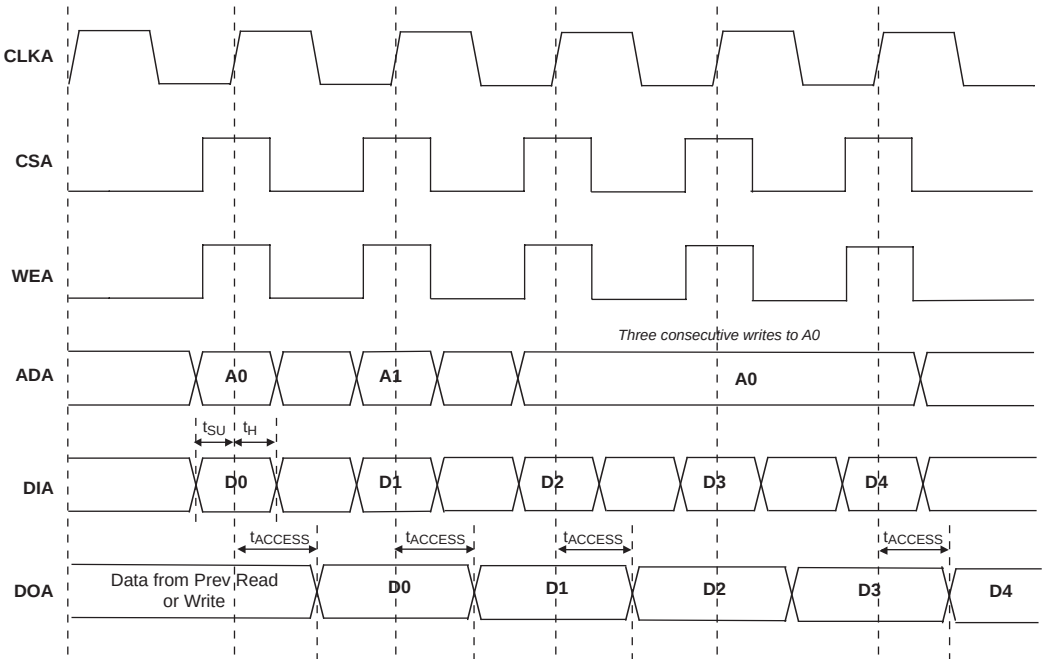


Figure 3-12. Read Before Write (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3-13. Write Through (SP Read/Write on Port A, Input Registers Only)



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

LatticeECP2 Family Timing Adders[1, 2, 3]

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
Input Adjusters					
LVDS25	LVDS				ns
MLVDS	MLVDS				ns
RSDS	RSDS				ns
BLVDS25	BLVDS				ns
LVPECL33	LVPECL				ns
HSTL18_I	HSTL_18 class I				ns
HSTL18_II	HSTL_18 class II				ns
HSTL18D_I	Differential HSTL 18 class I				ns
HSTL18D_II	Differential HSTL 18 class II				ns
HSTL15_I	HSTL_15 class I				ns
HSTL15D_I	Differential HSTL 15 class I				ns
SSTL33_I	SSTL_3 class I				ns
SSTL33_II	SSTL_3 class II				ns
SSTL33D_I	Differential SSTL_3 class I				ns
SSTL33D_II	Differential SSTL_3 class II				ns
SSTL25_I	SSTL_2 class I				ns
SSTL25_II	SSTL_2 class II				ns
SSTL25D_I	Differential SSTL_2 class I				ns
SSTL25D_II	Differential SSTL_2 class II				ns
SSTL18_I	SSTL_18 class I				ns
SSTL18_II	SSTL_18 class II				ns
SSTL18D_I	Differential SSTL_18 class I				ns
SSTL18D_II	Differential SSTL_18 class II				ns
LVTTL33	LVTTL				ns
LVCMOS33	LVCMOS 3.3				ns
LVCMOS25	LVCMOS 2.5				ns
LVCMOS18	LVCMOS 1.8				ns
LVCMOS15	LVCMOS 1.5				ns
LVCMOS12	LVCMOS 1.2				ns
PCI33	3.3V PCI				ns
Output Adjusters					
LVDS25E[4]	LVDS 2.5 E				ns
LVDS25	LVDS 2.5				ns
RSDS[4]	RSDS				ns
MLVDS[4]	MLVDS				ns
BLVDS25[4]	BLVDS 2.5				ns
LVPECL33[4]	LVPECL 3.3				ns
HSTL18_I	HSTL_18 class I				ns
HSTL18_II	HSTL_18 class II				ns
HSTL18D_I	Differential HSTL 18 class I				ns
HSTL18D_II	Differential HSTL 18 class II				ns

LatticeECP2 Family Timing Adders[1, 2, 3] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
HSTL15_I	HSTL_15 class I				ns
HSTL15D_I	Differential HSTL 15 class I				ns
SSTL33_I	SSTL_3 class I				ns
SSTL33_II	SSTL_3 class II				ns
SSTL33D_I	Differential SSTL_3 class I				ns
SSTL33D_II	Differential SSTL_3 class II				ns
SSTL25_I	SSTL_2 class I				ns
SSTL25_II	SSTL_2 class II				ns
SSTL25D_I	Differential SSTL_2 class I				ns
SSTL25D_II	Differential SSTL_2 class II				ns
SSTL18_I	SSTL_1.8 class I				ns
SSTL18_II	SSTL_1.8 class II				ns
SSTL18D_I	Differential SSTL_1.8 class I				ns
SSTL18D_II	Differential SSTL_1.8 class II				ns
LVTTL33_4mA	LVTTL 4mA drive				ns
LVTTL33_8mA	LVTTL 8mA drive				ns
LVTTL33_12mA	LVTTL 12mA drive				ns
LVTTL33_16mA	LVTTL 16mA drive				ns
LVTTL33_20mA	LVTTL 20mA drive				ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, fast slew rate				ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, fast slew rate				ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, fast slew rate				ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, fast slew rate				ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, fast slew rate				ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, fast slew rate				ns
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, fast slew rate				ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, fast slew rate				ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, fast slew rate				ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, fast slew rate				ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, fast slew rate				ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, fast slew rate				ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, fast slew rate				ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, fast slew rate				ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, fast slew rate				ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, fast slew rate				ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, fast slew rate				ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, fast slew rate				ns
LVCMOS33_4mA	LVCMOS 3.3 4mA drive, slow slew rate				ns
LVCMOS33_8mA	LVCMOS 3.3 8mA drive, slow slew rate				ns
LVCMOS33_12mA	LVCMOS 3.3 12mA drive, slow slew rate				ns
LVCMOS33_16mA	LVCMOS 3.3 16mA drive, slow slew rate				ns
LVCMOS33_20mA	LVCMOS 3.3 20mA drive, slow slew rate				ns
LVCMOS25_4mA	LVCMOS 2.5 4mA drive, slow slew rate				ns

LatticeECP2 Family Timing Adders[1, 2, 3] (Continued)

Over Recommended Operating Conditions

Buffer Type	Description	-7	-6	-5	Units
LVCMOS25_8mA	LVCMOS 2.5 8mA drive, slow slew rate				ns
LVCMOS25_12mA	LVCMOS 2.5 12mA drive, slow slew rate				ns
LVCMOS25_16mA	LVCMOS 2.5 16mA drive, slow slew rate				ns
LVCMOS25_20mA	LVCMOS 2.5 20mA drive, slow slew rate				ns
LVCMOS18_4mA	LVCMOS 1.8 4mA drive, slow slew rate				ns
LVCMOS18_8mA	LVCMOS 1.8 8mA drive, slow slew rate				ns
LVCMOS18_12mA	LVCMOS 1.8 12mA drive, slow slew rate				ns
LVCMOS18_16mA	LVCMOS 1.8 16mA drive, slow slew rate				ns
LVCMOS15_4mA	LVCMOS 1.5 4mA drive, slow slew rate				ns
LVCMOS15_8mA	LVCMOS 1.5 8mA drive, slow slew rate				ns
LVCMOS12_2mA	LVCMOS 1.2 2mA drive, slow slew rate				ns
LVCMOS12_6mA	LVCMOS 1.2 6mA drive, slow slew rate				ns
PCI33	3.3V PCI				ns

1. Timing adders are characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in Switching Test Conditions table.
3. All other standards according to the appropriate specification.
4. These timing adders are measured with the recommended resistor values.

Timing v.

sysCLOCK GPLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	Without external capacitor		—	420	MHz
		With external capacitor		—		MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	Without external capacitor		—	420	MHz
		With external capacitor		—		MHz
f_{OUT2}	K-Divider Output Frequency	Without external capacitor		—	840	MHz
		With external capacitor		—		MHz
f_{VCO}	PLL VCO Frequency			—		MHz
f_{PFD}	Phase Detector Input Frequency			—		MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default duty cycle selected [3]				%
t_{PH} [4]	Output Phase Accuracy		—	—		
t_{OPJIT} [1]	Output Clock Period Jitter	f_{OUT} > 100 MHz	—	—		ps
		f_{OUT} < 100 MHz	—	—		UIPP
t_{SK}	Input Clock to Output Clock Skew	N/M = integer	—	—		ps
t_W	Output Clock Pulse Width	At 90% or 10%		—	—	ns
t_{LOCK} [2]	PLL Lock-in Time	Without external capacitor				µs
		With external capacitor	—	—		µs
t_{PA}	Programmable Delay Unit					ps
t_{IPJIT}	Input Clock Period Jitter		—	—		ps
t_{FBKDLY}	External Feedback Delay		—	—		ns
t_{HI}	Input Clock High Time	90% to 90%		—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%		—	—	ns
t_{RST}	Reset Signal Pulse Width (RESETM/ RESETK)					ns
	Reset Signal Pulse Width (CNTRST)	Without capacitor				ns
	Reset Signal Pulse Width (CNTRST)	With capacitor				ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. Relative to CLKOP.

Timing v.

sysCLOCK SPLL Timing

Over Recommended Operating Conditions

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	Without external capacitor		—	420	MHz
		With external capacitor		—		MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	Without external capacitor		—	420	MHz
		With external capacitor		—		MHz
f_{OUT2}	K-Divider Output Frequency (CLKOK)	Without external capacitor		—	840	MHz
		With external capacitor		—		MHz
f_{VCO}	PLL VCO Frequency			—		MHz
f_{PFD}	Phase Detector Input Frequency			—		MHz
AC Characteristics						
t_{DT}	Output Clock Duty Cycle	Default Duty Cycle Selected[3]				%
t_{PH}[4]	Output Phase Accuracy		—	—		
t_{OPJIT}[1]	Output Clock Period Jitter	f_{OUT} > 100 MHz	—	—		ps
		f_{OUT} < 100 MHz	—	—		UIPP
t_{SK}	Input Clock to Output Clock Skew	N/M = Integer	—	—		ps
t_W	Output Clock Pulse Width	At 90% or 10%		—		ns
t_{LOCK}[2]	PLL Lock-in Time	Without external capacitor	—	—		µs
		With external capacitor	—	—		µs
t_{PA}	Programmable Delay Unit		—	—		ps
t_{IPJIT}	Input Clock Period Jitter		—	—		ps
t_{FBKDLY}	External Feedback Delay		—	—		ns
t_{HI}	Input Clock High Time	90% to 90%		—	—	ns
t_{LO}	Input Clock Low Time	10% to 10%		—	—	ns
t_{RST}	Reset Signal Pulse Width (RESETM/ RESETK)					ns
	Reset Signal Pulse Width (CNTRST)	Without external capacitor				ns
	Reset Signal Pulse Width (CNTRST)	With external capacitor				ns

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. Relative to CLKOP.

Timing v.

DLL Timing

Over Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
f_{REF}	Input reference clock frequency (on-chip or off-chip)		—	420	MHz
f_{FB}	Feedback clock frequency (on-chip or off-chip)		—		MHz
f_{CLKOP}[1]	Output clock frequency, CLKOP		—	420	MHz
f_{CLKOS}[2]	Output clock frequency, CLKOS		—		MHz
t_{PJIT}	Output clock period jitter (clean input)		—	420	ps p-p
t_{CYJIT}	Output clock cycle to cycle jitter (clean input)		—		ps p-p
t_{DUTY}	Output clock duty cycle (at 50% levels, 50% duty cycle input clock, 50% duty cycle circuit turned off, time reference delay mode)				%
$t_{DUTYTRD}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, time reference delay mode)				%
$t_{DUTYCIR}$	Output clock duty cycle (at 50% levels, arbitrary duty cycle input clock, 50% duty cycle circuit enabled, clock injection removal mode)				%
t_{SKEW}[3]	Output clock to clock skew between two outputs with the same phase setting	—	—		ps
t_{PHASE}	Phase error measured at device pads using off-chip reference clock and feedback clocks	—	—		ps
t_{PWH}	Input clock minimum pulse width high (at 80% level)		—	—	ps
t_{PWL}	Input clock minimum pulse width low (at 20% level)		—	—	ps
t_R, t_F	Input clock rise and fall time (20% to 80% levels)	—	—		ps
t_{INSTB}	Input clock period jitter		—	—	ps
t_{LOCK}	DLL lock time (input stable until assertion of LOCK)		—	—	cycles
t_{RSWD}	Digital reset minimum pulse width (at 80% level)		—	—	ns
t_{PA}	Delay step size				ps
t_{RANGE1}	Max. delay setting for single delay block (144 taps)				ns
t_{RANGE4}	Max. delay setting for four chained delay blocks				ns

1. CLKOP runs at the same frequency as the input clock.
2. CLKOS minimum frequency is obtained with divide by 4.
3. This is intended to be a “path-matching” design guideline and is not a measurable specification.

LatticeECP2 sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
sysCONFIG Byte Data Flow				
t_{SUCBDI}	Byte D[0:7] Setup Time to CCLK		—	ns
t_{HCBDI}	Byte D[0:7] Hold Time to CCLK		—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—		ns
t_{SUCS}	CSN[0:1] Setup Time to CCLK		—	ns
t_{HCS}	CSN[0:1] Hold Time to CCLK		—	ns
t_{SUWD}	Write Signal Setup Time to CCLK		—	ns
t_{HWD}	Write Signal Hold Time to CCLK		—	ns
t_{DCB}	CCLK to BUSY Delay Time	—		ns
t_{CORD}	CCLK to Out for Read Data	—		ns
sysCONFIG Byte Slave Clocking				
t_{BSCH}	Byte Slave CCLK Minimum High Pulse		—	ns
t_{BSCL}	Byte Slave CCLK Minimum Low Pulse		—	ns
t_{BSCYC}	Byte Slave CCLK Cycle Time		—	ns
sysCONFIG Serial (Bit) Data Flow				
t_{SUSCDI}	DI Setup Time to CCLK Slave Mode		—	ns
t_{HSCDI}	DI Hold Time to CCLK Slave Mode		—	ns
t_{CODO}	CCLK to DOUT in Flowthrough Mode	—		ns
t_{SUMCDI}	DI Setup Time to CCLK Master Mode		—	ns
t_{HMCDI}	DI Hold Time to CCLK Master Mode		—	ns
sysCONFIG Serial Slave Clocking				
t_{SSCH}	Serial Slave CCLK Minimum High Pulse		—	ns
t_{SSCL}	Serial Slave CCLK Minimum Low Pulse		—	ns
sysCONFIG POR, Initialization and Wake-up				
t_{ICFG}	Minimum Vcc to INITN High	—		ms
t_{VMC}	Time from t_{ICFG} to Valid Master CCLK	—		us
t_{PRGMRJ}	PROGRAMN Pin Pulse Rejection	—		ns
t_{PRGM}	PROGRAMN Low Time to Start Configuration		—	ns
t_{DINIT}	PROGRAMN High to INITN High Delay	—		ms
$t_{DPPINIT}$	Delay Time from PROGRAMN Low to INITN Low	—		ns
$t_{DPPDONE}$	Delay Time from PROGRAMN Low to DONE Low	—		ns
t_{IODISS}	User I/O Disable from PROGRAMN Low	—		ns
t_{IOENSS}	User I/O Enabled Time from CCLK Edge During Wake-up Sequence	—		ns
t_{MWC}	Additional Wake Master Clock Signals after DONE Pin High		—	cycles
sysCONFIG SPI Port				
t_{CFGX}	INITN High to CCLK Low	—		µs
t_{CSSPI}	INITN High to CSSPIN Low	—		us
t_{CSCCLK}	CCLK Low before CSSPIN Low		—	ns
t_{SOCDO}	CCLK Low to Output Valid	—		ns
t_{SOE}	CSSPIN[0:1] Active Setup Time		—	ns
t_{CSPID}	CSSPIN[0:1] Low to First CCLK Edge Setup Time			ns

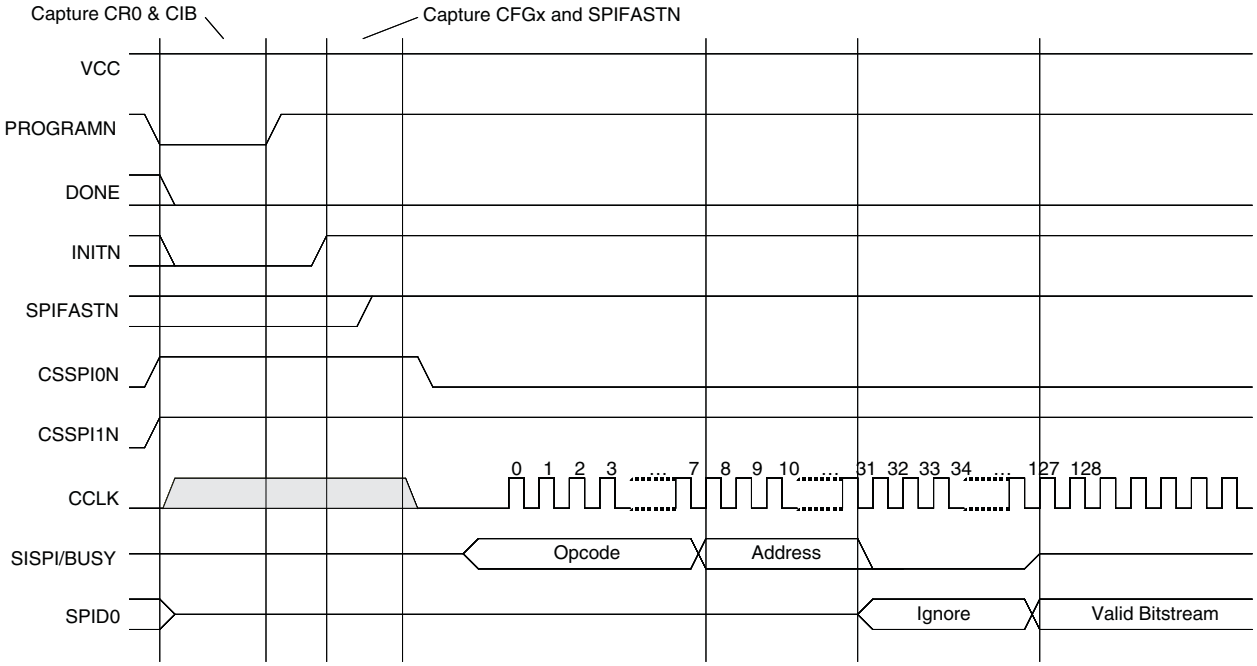
LatticeECP2 sysCONFIG Port Timing Specifications (Continued)

Over Recommended Operating Conditions

Parameter	Description	Min.	Max.	Units
f_{MAXSPI}	Max. CCLK Frequency - SPI Flash Read Opcode (0x03) (SPIFASTN = 1)	—		MHz
	Max. CCLK Frequency - SPI Flash Fast Read Opcode (0x0B) (SPIFASTN = 0)	—		MHz
t_{SUSPI}	SOSPI Data Setup Time Before CCLK		—	ns
t_{HSPI}	SOSPI Data Hold Time After CCLK		—	ns
Master Clock Frequency		Selected value -30%	Selected value +30%	MHz
Duty Cycle				%

Timing v.

Figure 3-14. SPI/SPIm Configuration Waveforms



JTAG Port Timing Specifications

Over Recommended Operating Conditions

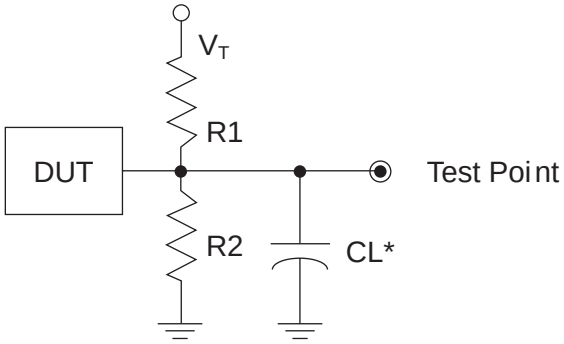
Symbol	Parameter	Min	Max	Units
f_{MAX}	TCK clock frequency	—		MHz
t_{BTCP}	TCK [BSCAN] clock pulse width		—	ns
t_{BTCPH}	TCK [BSCAN] clock pulse width high		—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low		—	ns
t_{BTS}	TCK [BSCAN] setup time		—	ns
t_{BTH}	TCK [BSCAN] hold time		—	ns
t_{BTRF}	TCK [BSCAN] rise/fall time		—	mV/ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—		ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—		ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—		ns
t_{BTCRS}	BSCAN test capture register setup time		—	ns
t_{BTCRH}	BSCAN test capture register hold time		—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—		ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—		ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—		ns

Timing v.

Switching Test Conditions

Figure 3-15 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-6.

Figure 3-15. Output Test Load, LVTTL and LVCMOS Standards



*CL Includes Test Fixture and Probe Capacitance

Table 3-6. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L -> H, H -> L)	∞	∞	0pF	LVCMOS 3.3 = 1.5V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.5 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> H)	∞	1MΩ		$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z -> L)	1MΩ	∞		$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H -> Z)	∞	100		V_{OH} - 0.10	—
LVCMOS 2.5 I/O (L -> Z)	100	∞		V_{OL} + 0.10	V_{CCIO}

Note: Output test conditions for all other interfaces are determined by the respective standards.

Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number*]_[A/B]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/Os for user logic. During configuration the user-programmable I/Os are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.
GSRN	I	Global RESET signal (active low). Any I/O pin can be GSRN.
NC	—	No connect.
GND	—	Ground. Dedicated pins.
V_{CC}	—	Power supply pins for core logic. Dedicated pins.
V_{CCAUX}	—	Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers.
V_{CCIOx}	—	Dedicated power supply pins for I/O bank x.
V_{REF1_x}, V_{REF2_x}	—	Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V_{REF} inputs. When not used, they may be used as I/O pins.
XRES	—	10K ohm +/-1% resistor must be connected between this pad and ground.
PLL, DLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins)		
[LOC][num]_GPLL[T, C]_IN_A	I	General Purpose PLL (GPLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_GPLL[T, C]_FB_A	I	Optional feedback GPLL input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_SPLL[T, C]_IN_A	I	Secondary PLL (SPLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_SPLL[T, C]_FB_A	I	Optional feedback (SPLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_DLL[T, C]_IN_A	I	DLL input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
[LOC][num]_DLL[T, C]_FB_A	I	Optional feedback (DLL) input pads: ULM, LLM, URM, LRM, num = row from center, T = true and C = complement, index A,B,C...at each side.
PCLK[T, C]_[n:0]_[3:0]	I	Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank.
[LOC]DQS[num]	I	DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output.
Test and Programming (Dedicated Pins)		
TMS	I	Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration.

Signal Descriptions (Cont.)

Signal Name	I/O	Description
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled.
TDI	I	Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration.
TDO	O	Output pin. Test Data Out pin used to shift data out of a device using 1149.1.
VCCJ	—	Power supply pin for JTAG Test Access Port.
Configuration Pads (Used during sysCONFIG)		
CFG[2:0]	I	Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, a pull-up is enabled. These are dedicated pins.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. It is a dedicated pin.
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin always has an active pull-up. This is a dedicated pin.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. This is a dedicated pin.
CCLK	I/O	Configuration Clock for configuring an FPGA in sysCONFIG mode.
BUSY/SISPI	I/O	Read control command in SPI3 or SPIX mode.
CSN	I	sysCONFIG chip select (active low). During configuration, a pull-up is enabled.
CS1N	I	sysCONFIG chip select (active low). During configuration, a pull-up is enabled.
WRITEN	I	Write Data on Parallel port (active low).
D[7:0]/SPID[0:7]	I/O	sysCONFIG Port Data I/O.
DOUT/CSON	O	Output for serial configuration data (rising edge of CCLK) when using sysCONFIG port.
DI/CSSPIN	I/O	Input for serial configuration data (clocked with CCLK) when using sysCONFIG port. During configuration, a pull-up is enabled. Output when used in SPI/SPIX modes.

PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

PICs Associated with DQS Strobe	PIO Within PIC	DDR Strobe (DQS) and Data (DQ) Pins
For Left and Right Edges of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
For Bottom Edge of the Device		
P[Edge] [n-4]	A	DQ
	B	DQ
P[Edge] [n-3]	A	DQ
	B	DQ
P[Edge] [n-2]	A	DQ
	B	DQ
P[Edge] [n-1]	A	DQ
	B	DQ
P[Edge] [n]	A	[Edge]DQSn
	B	DQ
P[Edge] [n+1]	A	DQ
	B	DQ
P[Edge] [n+2]	A	DQ
	B	DQ
P[Edge] [n+3]	A	DQ
	B	DQ
P[Edge] [n+4]	A	DQ
	B	DQ

Notes:
1. “n” is a row PIC number.
2. The DDR interface is designed for memories that support one DQS strobe up to 15 bits of data for the left and right edges and up to 17 bits of data for the bottom edge. In some packages, all the potential DDR data (DQ) pins may not be available. PIC numbering definitions are provided in the “Signal Names” column of the Signal Descriptions table.

Pin Information Summary

Pin Type		Package	
		484 fpBGA	672 fpBGA
Single Ended User I/O			—
Differential Pair User I/O			—
Configuration	Dedicated		—
	Muxed		—
TAP			—
Dedicated (total without supplies)			—
V_{CC}			20
V_{CCAUX}			16
V_{CCIO}	Bank0		5
	Bank1		5
	Bank2		5
	Bank3		5
	Bank4		5
	Bank5		5
	Bank6		5
	Bank7		5
	Bank8		2
GND			72
NC			3
Single Ended/ Differential I/O per Bank	Bank0		—
	Bank1		—
	Bank2		—
	Bank3		—
	Bank4		—
	Bank5		—
	Bank6		—
	Bank7		—
V_{CCJ}			—

Power Supply and NC Connections

Signal	484 fpBGA	672 fpBGA
VCC		L12, L13, L14, L15, M11, M12, M15, M16, N11, N16, P11, P16, R11, R12, R15, R16, T12, T13, T14, T15
VCCIO0		D11, D6, G9, J12, K12
VCCIO1		D16, D21, G18, J15, K15
VCCIO2		F23, J20, L23, M17, M18
VCCIO3		AA23, R17, R18, T23, V20
VCCIO4		AC16, AC21, U15, V15, Y18
VCCIO5		AC11, AC6, U12, V12, Y9
VCCIO6		AA4, R10, R9, T4, V7
VCCIO7		F4, J7, L4, M10, M9
VCCIO8		AE25, V18
VCCJ		AB5
VCCAUX		J10, J11, J16, J17, K18, L18, T18, U18, V16, V17, V10, V11, T9, U9, K9, L9
GND		A2, A25, AA18, AA24, AA3, AA9, AD11, AD16, AD21, AD6, AE1, AE26, AF2, AF25, B1, B26, C11, C16, C21, C6, F18, F24, F3, F9, J13, J14, J21, J6, K10, K11, K13, K14, K16, K17, L10, L11, L16, L17, L24, L3, M13, M14, N10, N12, N13, N14, N15, N17, P10, P12, P13, P14, P15, P17, R13, R14, T10, T11, T16, T17, T24, T3, U10, U11, U13, U14, U16, U17, V13, V14, V21, V6
NC		N6, P24, M3

ECP2-50 Logic Signal Connections: 672 fpBGA

Ball Number	Ball Function	Bank	Dual Function	Differential
D2	PL2A	7	VREF2_7	T*
D1	PL2B	7	VREF1_7	C*
GND	GNDIO	7		
F6	PL5A	7		T
F5	PL5B	7		C
VCCIO	VCCIO	7		
E4	PL6A	7		T*
E3	PL6B	7		C*
VCC	VCC	7		
E2	PL7A	7		T
E1	PL7B	7		C
GND	GNDIO	7		
GND	GND	7		
H6	PL8A	7	LDQS8	T*
H5	PL8B	7		C*
F2	PL9A	7		T
VCCIO	VCCIO	7		
F1	PL9B	7		C
H8	PL10A	7		T*
J9	PL10B	7		C*
G4	PL11A	7		T
GND	GNDIO	7		
G3	PL11B	7		C
H7	PL12A	7		T*
VCCAUX	VCCAUX	7		
J8	PL12B	7		C*
G2	PL13A	7		T
G1	PL13B	7		C
H3	PL14A	7		T*
VCCIO	VCCIO	7		
H4	PL14B	7		C*
J5	PL15A	7		T
VCC	VCC	7		
J4	PL15B	7		C
J3	PL16A	7	LDQS16	T*
GND	GNDIO	7		
GND	GND	7		
K4	PL16B	7		C*
H1	PL17A	7		T
H2	PL17B	7		C
VCCIO	VCCIO	7		
K6	PL18A	7		T*
K7	PL18B	7		C*

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
J1	PL19A	7		T
J2	PL19B	7		C
GND	GNDIO	7		
VCCIO	VCCIO	7		
VCC	VCC	7		
K3	PL23A	7		T
K2	PL23B	7		C
GND	GNDIO	7		
GND	GND	7		
K1	PL24A	7	LDQS24	T*
L2	PL24B	7		C*
L1	PL25A	7	LUM0_SPLLT_IN_A	T
VCCIO	VCCIO	7		
M2	PL25B	7	LUM0_SPLLC_IN_A	C
M1	PL26A	7	LUM0_SPLLT_FB_A	T
N2	PL26B	7	LUM0_SPLLC_FB_A	C
GND	GNDIO	7		
M8	LUM0_VCCPLL	7		
GND	GNDAUX	7		
VCCAUX	VCCAUX	7		
VCCIO	VCCIO	7		
VCC	VCC	7		
GND	GNDIO	7		
GND	GND	7		
VCCIO	VCCIO	7		
GND	GNDIO	7		
N1	PL37A	7		*
L8	PL38A	7		T
K8	PL38B	7		C
VCCIO	VCCIO	7		
L6	PL39A	7		T*
K5	PL39B	7		C*
VCC	VCC	7		
L7	PL40A	7		T
L5	PL40B	7		C
GND	GNDIO	7		
GND	GND	7		
P1	PL41A	7	LDQS41	T*
P2	PL41B	7		C*
M6	PL42A	7		T
VCCIO	VCCIO	7		
N8	PL42B	7		C
R1	PL43A	7		T*
R2	PL43B	7		C*

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
M7	PL44A	7	PCLKT7_0	T
GND	GNDIO	7		
N9	PL44B	7	PCLKC7_0	C
GND	GNDAUX	7		
M4	PL46A	6	PCLKT6_0	T*
VCCAUX	VCCAUX	6		
M5	PL46B	6	PCLKC6_0	C*
N7	PL47A	6	VREF2_6	T
P9	PL47B	6	VREF1_6	C
N3	PL48A	6		T*
VCCIO	VCCIO	6		
N4	PL48B	6		C*
N5	PL49A	6		T
VCC	VCC	6		
P7	PL49B	6		C
T1	PL50A	6	LDQS50	T*
GND	GNDIO	6		
GND	GND	6		
T2	PL50B	6		C*
P8	PL51A	6		T
P6	PL51B	6		C
VCCIO	VCCIO	6		
P5	PL52A	6		T*
P4	PL52B	6		C*
U1	PL53A	6		T
V1	PL53B	6		C
GND	GNDIO	6		
P3	PL54A	6		T*
R3	PL54B	6		C*
R4	PL55A	6		T
U2	PL55B	6		C
VCCIO	VCCIO	6		
V2	PL56A	6		T*
W2	PL56B	6		C*
VCC	VCC	6		
T6	PL57A	6		T
R5	PL57B	6		C
GND	GNDIO	6		
GND	GND	6		
R6	PL58A	6	LDQS58	T*
R7	PL58B	6		C*
W1	PL59A	6		T
VCCIO	VCCIO	6		
Y2	PL59B	6		C

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
Y1	PL60A	6	LLM0_GDLLT_IN_A	T*
AA2	PL60B	6	LLM0_GDLLC_IN_A	C*
T5	PL61A	6	LLM0_GDLLT_FB_A	T
GND	GNDIO	6		
T7	PL61B	6	LLM0_GDLLC_FB_D	C
GND	GNDAUX	6		
R8	LLM0_VCCPLL	6		
T8	LLM0_PLLCAP	6		
U3	PL63A	6	LLM0_GPLLT_IN_A	T*
VCCAUX	VCCAUX	6		
U4	PL63B	6	LLM0_GPLLC_IN_A	C*
V3	PL64A	6	LLM0_GPLLT_FB_A	T
U5	PL64B	6	LLM0_GPLLC_FB_A	C
V4	PL65A	6		T*
VCCIO	VCCIO	6		
V5	PL65B	6		C*
Y3	PL66A	6		T
VCC	VCC	6		
Y4	PL66B	6		C
W3	PL67A	6	LDQS67	T*
GND	GNDIO	6		
GND	GND	6		
W4	PL67B	6		C*
AA1	PL68A	6		T
AB1	PL68B	6		C
VCCIO	VCCIO	6		
U8	PL69A	6		T*
U7	PL69B	6		C*
V8	PL70A	6		T
U6	PL70B	6		C
GND	GNDIO	6		
W6	PL71A	6		T*
W5	PL71B	6		C*
AC1	PL72A	6		T
AD1	PL72B	6		C
VCCIO	VCCIO	6		
Y6	PL73A	6		T*
Y5	PL73B	6		C*
VCC	VCC	6		
AE2	PL74A	6		T
AD2	PL74B	6		C
GND	GNDIO	6		
GND	GND	6		
AB3	PL75A	6	LDQS75	T*

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
AB2	PL75B	6		C*
W7	PL76A	6		T
VCCIO	VCCIO	6		
W8	PL76B	6		C
Y7	PL77A	6		T*
Y8	PL77B	6		C*
AC2	PL78A	6		T
GND	GNDIO	6		
AD3	PL78B	6		C
AC3	TCK	9		
AA8	TDI	9		
AB4	TMS	9		
GND	GNDAUX	6		
AA5	TDO	9		
AB5	VCCJ	9		
AE3	PB2A	5	VREF2_5	T
AF3	PB2B	5	VREF1_5	C
VCCAUX	VCCAUX	5		
AC4	PB3A	5		T
AD4	PB3B	5		C
AE4	PB4A	5		T
AF4	PB4B	5		C
VCCIO	VCCIO	5		
V9	PB5A	5		T
W9	PB5B	5		C
GND	GNDIO	5		
AA6	PB6A	5	BDQS6	T
AB6	PB6B	5		C
VCC	VCC	5		
AC5	PB7A	5		T
AD5	PB7B	5		C
AA7	PB8A	5		T
AB7	PB8B	5		C
VCCIO	VCCIO	5		
AE5	PB9A	5		T
AF5	PB9B	5		C
AC7	PB10A	5		T
AD7	PB10B	5		C
GND	GNDIO	5		
GND	GNDAUX	5		
GND	GND	5		
VCCIO	VCCIO	5		
VCC	VCC	5		
GND	GNDIO	5		

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
VCCIO	VCCIO	5		
GND	GNDIO	5		
GND	GND	5		
W10	PB20A	5		T
Y10	PB20B	5		C
VCCAUX	VCCAUX	5		
W11	PB21A	5		T
AA10	PB21B	5		C
AC8	PB22A	5		T
AD8	PB22B	5		C
VCCIO	VCCIO	5		
AB8	PB23A	5		T
AB10	PB23B	5		C
GND	GNDIO	5		
AE6	PB24A	5	BDQS24	T
AF6	PB24B	5		C
VCC	VCC	5		
AA11	PB25A	5		T
AC9	PB25B	5		C
AB9	PB26A	5		T
AD9	PB26B	5		C
VCCIO	VCCIO	5		
Y11	PB27A	5		T
AB11	PB27B	5		C
AE7	PB28A	5		T
AF7	PB28B	5		C
GND	GNDIO	5		
GND	GNDAUX	5		
AC10	PB29A	5		T
GND	GND	5		
AD10	PB29B	5		C
AA12	PB30A	5		T
W12	PB30B	5		C
AB12	PB31A	5		T
VCCIO	VCCIO	5		
Y12	PB31B	5		C
AD12	PB32A	5		T
VCC	VCC	5		
AC12	PB32B	5		C
AC13	PB33A	5	BDQS33	T
GND	GNDIO	5		
AA13	PB33B	5		C
AD13	PB34A	5		T
AC14	PB34B	5		C

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
AE8	PB35A	5		T
VCCIO	VCCIO	5		
AF8	PB35B	5		C
AB15	PB36A	5		T
Y13	PB36B	5		C
AE9	PB37A	5		T
GND	GNDIO	5		
GND	GND	5		
AF9	PB37B	5		C
W13	PB38A	5		T
AA14	PB38B	5		C
VCCAUX	VCCAUX	5		
AE10	PB39A	5		T
AF10	PB39B	5		C
W14	PB40A	5		T
AB13	PB40B	5		C
VCCIO	VCCIO	5		
Y14	PB41A	5		T
AB14	PB41B	5		C
GND	GNDIO	5		
AE11	PB42A	5	BDQS42	T
AF11	PB42B	5		C
VCC	VCC	5		
AD14	PB43A	5		T
AA15	PB43B	5		C
AE12	PB44A	5	PCLKT5_0	T
AF12	PB44B	5	PCLKC5_0	C
VCCIO	VCCIO	5		
GND	GNDIO	5		
GND	GNDAUX	5		
GND	GND	4		
AD15	PB49A	4	PCLKT4_0	T
VCCIO	VCCIO	4		
AC15	PB49B	4	PCLKC4_0	C
AE13	PB50A	4		T
VCC	VCC	4		
AF13	PB50B	4		C
AB17	PB51A	4	BDQS51	T
GND	GNDIO	4		
Y15	PB51B	4		C
AE14	PB52A	4		T
AF14	PB52B	4		C
AA16	PB53A	4		T
VCCIO	VCCIO	4		

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
W15	PB53B	4		C
AC17	PB54A	4		T
AB16	PB54B	4		C
AE15	PB55A	4		T
GND	GNDIO	4		
GND	GND	4		
AF15	PB55B	4		C
AE16	PB56A	4		T
AF16	PB56B	4		C
VCCAUX	VCCAUX	4		
Y16	PB57A	4		T
AB18	PB57B	4		C
AD17	PB58A	4		T
AD18	PB58B	4		C
VCCIO	VCCIO	4		
AC18	PB59A	4		T
AD19	PB59B	4		C
GND	GNDIO	4		
AC19	PB60A	4	BDQS60	T
AE17	PB60B	4		C
VCC	VCC	4		
AB19	PB61A	4		T
AE19	PB61B	4		C
AF17	PB62A	4		T
AE18	PB62B	4		C
VCCIO	VCCIO	4		
W16	PB63A	4		T
AA17	PB63B	4		C
AF18	PB64A	4		T
AF19	PB64B	4		C
GND	GNDIO	4		
GND	GNDAUX	4		
AA19	PB65A	4		T
GND	GND	4		
W17	PB65B	4		C
Y19	PB66A	4		T
Y17	PB66B	4		C
AF20	PB67A	4		T
VCCIO	VCCIO	4		
AE20	PB67B	4		C
AA20	PB68A	4		T
VCC	VCC	4		
W18	PB68B	4		C
AD20	PB69A	4	BDQS69	T

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO	4		
AE21	PB69B	4		C
AF21	PB70A	4		T
AF22	PB70B	4		C
VCCIO	VCCIO	4		
GND	GNDIO	4		
GND	GND	4		
AE22	PB74A	4		T
AD22	PB74B	4		C
VCCAUX	VCCAUX	4		
AF23	PB75A	4		T
AE23	PB75B	4		C
AD23	PB76A	4		T
AC23	PB76B	4		C
VCCIO	VCCIO	4		
AB20	PB77A	4		T
AC20	PB77B	4		C
GND	GNDIO	4		
AB21	PB78A	4	BDQS78	T
AC22	PB78B	4		C
VCC	VCC	4		
W19	PB79A	4		T
AA21	PB79B	4		C
AF24	PB80A	4		T
AE24	PB80B	4		C
VCCIO	VCCIO	4		
Y20	PB81A	4		T
AB22	PB81B	4		C
Y21	PB82A	4	VREF2_4	T
AB23	PB82B	4	VREF1_4	C
GND	GNDIO	4		
GND	GNDAUX	4		
AD24	CFG2	8		
W20	CFG1	8		
AC24	CFG0	8		
GND	GNDAUX	8		
V19	PROGRAMN	8		
AA22	CCLK	8		
AB24	INITN	8		
AD25	DONE	8		
GND	GNDIO	8		
W21	PR77B	8	WRITEN	C
Y22	PR77A	8	CS1N	T
AC25	PR76B	8	CSN	C

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
AB25	PR76A	8	D0	T
VCCIO	VCCIO	8		
AD26	PR75B	8	D1	C
AC26	PR75A	8	D2	T
GND	GND	8		
Y23	PR74B	8	D3	C
GND	GNDIO	8		
W22	PR74A	8	D4	T
AA25	PR73B	8	D5	C
VCC	VCC	8		
AB26	PR73A	8	D6	T
W23	PR72B	8	D7	C
VCCIO	VCCIO	8		
V22	PR72A	8	DI	T
Y24	PR71B	8	DOUT,CSON	C
Y25	PR71A	8	BUSY	T
W24	PR70B	3		C
GND	GNDIO	3		
V23	PR70A	3		T
AA26	PR69B	3		C*
Y26	PR69A	3		T*
U21	PR68B	3		C
VCCIO	VCCIO	3		
U19	PR68A	3		T
W25	PR67B	3		C*
GND	GND	3		
W26	PR67A	3	RDQS67	T*
GND	GNDIO	3		
V24	PR66B	3		C
V25	PR66A	3		T
VCC	VCC	3		
V26	PR65B	3		C*
U26	PR65A	3		T*
VCCIO	VCCIO	3		
U22	PR64B	3	RLM0_GPLLC_FB_A	C
U23	PR64A	3	RLM0_GPLLT_FB_A	T
U24	PR63B	3	RLM0_GPLLC_IN_A	C*
U25	PR63A	3	RLM0_GPLLT_IN_A	T*
VCCAUX	VCCAUX	3		
R20	RLM0_PLLCAP	3		
P18	RLM0_VCCPLL	3		
GND	GNDAUX	3		
T19	PR61B	3	RLM0_GDLLC_FB_A	C
U20	PR61A	3	RLM0_GDLLT_FB_A	T

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO	3		
T25	PR60B	3	RLM0_GDLLC_IN_A	C*
T26	PR60A	3	RLM0_GDLLT_IN_A	T*
T20	PR59B	3		C
T22	PR59A	3		T
VCCIO	VCCIO	3		
R26	PR58B	3		C*
R25	PR58A	3	RDQS58	T*
GND	GND	3		
R22	PR57B	3		C
GND	GNDIO	3		
T21	PR57A	3		T
P26	PR56B	3		C*
VCC	VCC	3		
P25	PR56A	3		T*
R24	PR55B	3		C
VCCIO	VCCIO	3		
R23	PR55A	3		T
P20	PR54B	3		C*
R19	PR54A	3		T*
P21	PR53B	3		C
GND	GNDIO	3		
P19	PR53A	3		T
P23	PR52B	3		C*
P22	PR52A	3		T*
N22	PR51B	3		C
VCCIO	VCCIO	3		
R21	PR51A	3		T
N26	PR50B	3		C*
GND	GND	3		
N25	PR50A	3	RDQS50	T*
GND	GNDIO	3		
N19	PR49B	3		C
N20	PR49A	3		T
VCC	VCC	3		
M26	PR48B	3		C*
M25	PR48A	3		T*
VCCIO	VCCIO	3		
N18	PR47B	3	VREF2_3	C
N21	PR47A	3	VREF1_3	T
L26	PR46B	3	PCLKC3_0	C*
L25	PR46A	3	PCLKT3_0	T*
VCCAUX	VCCAUX	3		
GND	GNDAUX	2		

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
N24	PR44B	2	PCLKC2_0	C
M23	PR44A	2	PCLKT2_0	T
GND	GNDIO	2		
L21	PR43B	2		C*
K22	PR43A	2		T*
M24	PR42B	2		C
N23	PR42A	2		T
VCCIO	VCCIO	2		
K26	PR41B	2		C*
K25	PR41A	2	RDQS41	T*
GND	GND	2		
M20	PR40B	2		C
GND	GNDIO	2		
M19	PR40A	2		T
L22	PR39B	2		C*
VCC	VCC	2		
M22	PR39A	2		T*
K21	PR38B	2		C
VCCIO	VCCIO	2		
M21	PR38A	2		T
K24	PR37B	2		C*
J24	PR37A	2		T*
GND	GNDIO	2		
VCCIO	VCCIO	2		
GND	GND	2		
GND	GNDIO	2		
VCC	VCC	2		
VCCIO	VCCIO	2		
VCCAUX	VCCAUX	2		
GND	GNDAUX	2		
L20	RUM0_VCCPLL	2		
GND	GNDIO	2		
J26	PR26B	2	RUM0_SPLLC_FB_A	C
J25	PR26A	2	RUM0_SPLLT_FB_A	T
J23	PR25B	2	RUM0_SPLLC_IN_A	C
K23	PR25A	2	RUM0_SPLLT_IN_A	T
VCCIO	VCCIO	2		
H26	PR24B	2		C*
H25	PR24A	2	RDQS24	T*
GND	GND	2		
H24	PR23B	2		C
GND	GNDIO	2		
H23	PR23A	2		T
VCC	VCC	2		

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
VCCIO	VCCIO	2		
G26	PR19B	2		C
GND	GNDIO	2		
G25	PR19A	2		T
F26	PR18B	2		C*
F25	PR18A	2		T*
K20	PR17B	2		C
VCCIO	VCCIO	2		
L19	PR17A	2		T
E26	PR16B	2		C*
GND	GND	2		
E25	PR16A	2	RDQS16	T*
GND	GNDIO	2		
J22	PR15B	2		C
H22	PR15A	2		T
VCC	VCC	2		
G24	PR14B	2		C*
G23	PR14A	2		T*
VCCIO	VCCIO	2		
K19	PR13B	2		C
J19	PR13A	2		T
D26	PR12B	2		C*
C26	PR12A	2		T*
VCCAUX	VCCAUX	2		
F22	PR11B	2		C
E24	PR11A	2		T
GND	GNDIO	2		
D25	PR10B	2		C*
C25	PR10A	2		T*
D24	PR9B	2		C
B25	PR9A	2		T
VCCIO	VCCIO	2		
H21	PR8B	2		C*
G22	PR8A	2	RDQS8	T*
GND	GND	2		
B24	PR7B	2		C
GND	GNDIO	2		
C24	PR7A	2		T
D23	PR6B	2		C*
VCC	VCC	2		
C23	PR6A	2		T*
G21	PR5B	2		C
VCCIO	VCCIO	2		
H20	PR5A	2		T

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
GND	GNDIO	2		
E22	PR2B	2	VREF2_2	C*
F21	PR2A	2	VREF1_2	T*
GND	GNDAUX	1		
E23	PT82B	1	VREF2_1	C
GND	GNDIO	1		
D22	PT82A	1	VREF1_1	T
G20	PT81B	1		C
J18	PT81A	1		T
F20	PT80B	1		C
VCCIO	VCCIO	1		
H19	PT80A	1		T
A24	PT79B	1		C
A23	PT79A	1		T
E21	PT78B	1		C
VCC	VCC	1		
F19	PT78A	1		T
C22	PT77B	1		C
GND	GNDIO	1		
E20	PT77A	1		T
B22	PT76B	1		C
VCCIO	VCCIO	1		
B23	PT76A	1		T
C20	PT75B	1		C
D20	PT75A	1		T
A22	PT74B	1		C
VCCAUX	VCCAUX	1		
A21	PT74A	1		T
GND	GND	1		
GND	GNDIO	1		
E19	PT71B	1		C
C19	PT71A	1		T
VCCIO	VCCIO	1		
B21	PT70B	1		C
B20	PT70A	1		T
D19	PT69B	1		C
B19	PT69A	1		T
GND	GNDIO	1		
G17	PT68B	1		C
E18	PT68A	1		T
VCC	VCC	1		
G19	PT67B	1		C
F17	PT67A	1		T
VCCIO	VCCIO	1		

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
A20	PT66B	1		C
A19	PT66A	1		T
E17	PT65B	1		C
D18	PT65A	1		T
GND	GND	1		
GND	GNDAUX	1		
B18	PT64B	1		C
GND	GNDIO	1		
A18	PT64A	1		T
E16	PT63B	1		C
G16	PT63A	1		T
F16	PT62B	1		C
VCCIO	VCCIO	1		
H18	PT62A	1		T
A17	PT61B	1		C
B17	PT61A	1		T
C18	PT60B	1		C
VCC	VCC	1		
B16	PT60A	1		T
C17	PT59B	1		C
GND	GNDIO	1		
D17	PT59A	1		T
E15	PT58B	1		C
VCCIO	VCCIO	1		
G15	PT58A	1		T
A16	PT57B	1		C
B15	PT57A	1		T
D15	PT56B	1		C
VCCAUX	VCCAUX	1		
F15	PT56A	1		T
A14	PT55B	1		C
GND	GND	1		
B14	PT55A	1		T
GND	GNDIO	1		
C15	PT54B	1		C
A15	PT54A	1		T
A13	PT53B	1		C
B13	PT53A	1		T
VCCIO	VCCIO	1		
H17	PT52B	1		C
H15	PT52A	1		T
D13	PT51B	1		C
C14	PT51A	1		T
GND	GNDIO	1		

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
G14	PT50B	1		C
E14	PT50A	1		T
VCC	VCC	1		
A12	PT49B	1		C
B12	PT49A	1		T
VCCIO	VCCIO	1		
F14	PT48B	1	PCLKC1_0	C
D14	PT48A	1	PCLKT1_0	T
GND	GND	1		
H16	XRES	1		
GND	GNDAUX	0		
H14	PT46B	0	PCLKC0_0	C
GND	GNDIO	0		
H13	PT46A	0	PCLKT0_0	T
A11	PT45B	0		C
B11	PT45A	0		T
C13	PT44B	0		C
VCCIO	VCCIO	0		
E13	PT44A	0		T
D12	PT43B	0		C
F13	PT43A	0		T
A10	PT42B	0		C
VCC	VCC	0		
B10	PT42A	0		T
C12	PT41B	0		C
GND	GNDIO	0		
C10	PT41A	0		T
G13	PT40B	0		C
VCCIO	VCCIO	0		
H12	PT40A	0		T
A9	PT39B	0		C
B9	PT39A	0		T
E12	PT38B	0		C
VCCAUX	VCCAUX	0		
G12	PT38A	0		T
A8	PT37B	0		C
GND	GND	0		
B8	PT37A	0		T
GND	GNDIO	0		
E11	PT36B	0		C
C9	PT36A	0		T
A7	PT35B	0		C
B7	PT35A	0		T
VCCIO	VCCIO	0		

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
F12	PT34B	0		C
D10	PT34A	0		T
H11	PT33B	0		C
G11	PT33A	0		T
GND	GNDIO	0		
A6	PT32B	0		C
B6	PT32A	0		T
VCC	VCC	0		
D8	PT31B	0		C
C8	PT31A	0		T
VCCIO	VCCIO	0		
F11	PT30B	0		C
E10	PT30A	0		T
E9	PT29B	0		C
D9	PT29A	0		T
GND	GND	0		
GND	GNDAUX	0		
G10	PT28B	0		C
GND	GNDIO	0		
H10	PT28A	0		T
A5	PT27B	0		C
B5	PT27A	0		T
C7	PT26B	0		C
VCCIO	VCCIO	0		
D7	PT26A	0		T
E8	PT25B	0		C
F10	PT25A	0		T
F8	PT24B	0		C
VCC	VCC	0		
H9	PT24A	0		T
C5	PT23B	0		C
GND	GNDIO	0		
D5	PT23A	0		T
B4	PT22B	0		C
VCCIO	VCCIO	0		
VCCAUX	VCCAUX	0		
GND	GND	0		
GND	GNDIO	0		
VCCIO	VCCIO	0		
GND	GNDIO	0		
VCC	VCC	0		
VCCIO	VCCIO	0		
GND	GND	0		
GND	GNDAUX	0		

ECP2-50 Logic Signal Connections: 672 fpBGA (Cont.)

Ball Number	Ball Function	Bank	Dual Function	Differential
C4	PT10B	0		C
GND	GNDIO	0		
C3	PT10A	0		T
A4	PT9B	0		C
A3	PT9A	0		T
B3	PT8B	0		C
VCCIO	VCCIO	0		
B2	PT8A	0		T
D4	PT7B	0		C
D3	PT7A	0		T
C2	PT6B	0		C
VCC	VCC	0		
C1	PT6A	0		T
G8	PT5B	0		C
GND	GNDIO	0		
G7	PT5A	0		T
E7	PT4B	0		C
VCCIO	VCCIO	0		
F7	PT4A	0		T
E6	PT3B	0		C
E5	PT3A	0		T
G6	PT2B	0	VREF2_0	C
VCCAUX	VCCAUX	0		
G5	PT2A	0	VREF1_0	T

*Supports dedicated LVDS outputs.

LatticeECP2 Family Data Sheet Ordering Information

February 2006 — Advance Data Sheet

Part Number Description

LFE2 – XX E – X XXXXXX X

Device Family
ECP2 (ECP2 FPGA + DSP Blocks)

Logic Capacity
6 = 6K LUTs
12 = 12K LUTs
20 = 20K LUTs
35 = 35K LUTs
50 = 50K LUTs
70 = 70K LUTs

Supply Voltage
E = 1.2V

Grade
C = Commercial
I = Industrial

Package
T144 = 144-pin TQFP
Q208 = 208-pin PQFP
F256 = 256-ball fpBGA
F484 = 484-ball fpBGA
F672 = 672-ball fpBGA
F900 = 900-ball fpBGA

Speed
5 = Slowest
6
7 = Fastest

Ordering Information

Note: LatticeECP2 devices are dual marked. For example, the commercial speed grade LFE2-50E-7F672C is also marked with industrial grade -6I (LFE2-50E-6F672I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial speed grade does not have industrial markings. The markings appear as follows:

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50E-5F484C	339	1.2V	-5	fpBGA	484	COM	50
LFE2-50E-6F484C	339	1.2V	-6	fpBGA	484	COM	50
LFE2-50E-7F484C	339	1.2V	-7	fpBGA	484	COM	50
LFE2-50E-5F672C	500	1.2V	-5	fpBGA	672	COM	50
LFE2-50E-6F672C	500	1.2V	-6	fpBGA	672	COM	50
LFE2-50E-7F672C	500	1.2V	-7	fpBGA	672	COM	50

Industrial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2-50E-5F484I	339	1.2V	-5	fpBGA	484	IND	50
LFE2-50E-6F484I	339	1.2V	-6	fpBGA	484	IND	50
LFE2-50E-5F672I	500	1.2V	-5	fpBGA	672	IND	50
LFE2-50E-6F672I	500	1.2V	-6	fpBGA	672	IND	50

LatticeECP2 Family Data Sheet Supplemental Information

February 2006 **Advance Data Sheet**

For Further Information

A variety of technical notes for the LatticeECP2 family are available on the Lattice web site at www.latticesemi.com.

- LatticeECP2 sysIO Usage Guide (TN1102)
- LatticeECP2 sysCLOCK PLL Design and Usage Guide (TN1103)
- LatticeECP2 Memory Usage Guide (TN1104)
- LatticeECP2 High-Speed I/O Interface (TN1105)
- LatticeECP2 Power Estimation and Management (TN1106)
- LatticeECP2 sysDSP Usage Guide (TN1107)
- LatticeECP2 sysCONFIG Usage Guide (TN1110)

For further information on interface standards refer to the following web sites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com