MAXIM

CMOS 10 and 12 Bit
Multiplying D/A Converters

MX7520/MX7521

General Description

The MX7520 and MX7521 are low cost CMOS multiplying digital-to-analog converters (DACs) with 10 and 12 bit resolution respectively. Both DACs operate from a +5V to +15V supply and dissipate only 20mW.

Thin-film resistors provide typically 0.3% untrimmed gain error and 10ppm/°C gain temperature coefficient. All digital inputs are compatible with both CMOS and TTL logic levels.

Maxim's MX7520 and MX7521 are electrically and pin compatible with Analog Devices' AD7520 and AD7521. The MX7520 is packaged in a 16-lead DIP while the MX7521 is packaged in an 18-lead DIP. Both devices are also available in small outline (SO) packages.

Applications

Machine and Motion Control Systems

Automatic Test Equipment

μP Controlled Calibration Circuitry

Programmable Gain Amplifiers

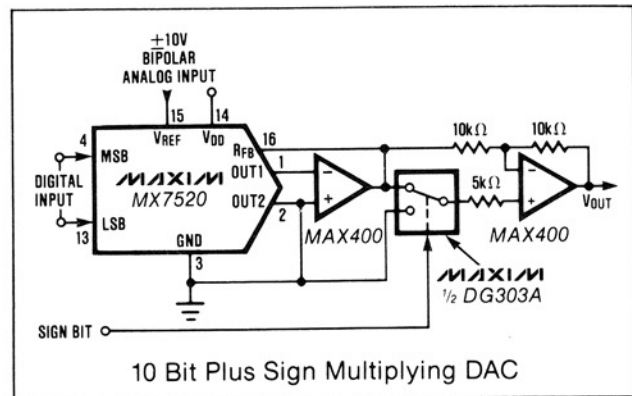Digitally Controlled Filters

Programmable Power Supplies
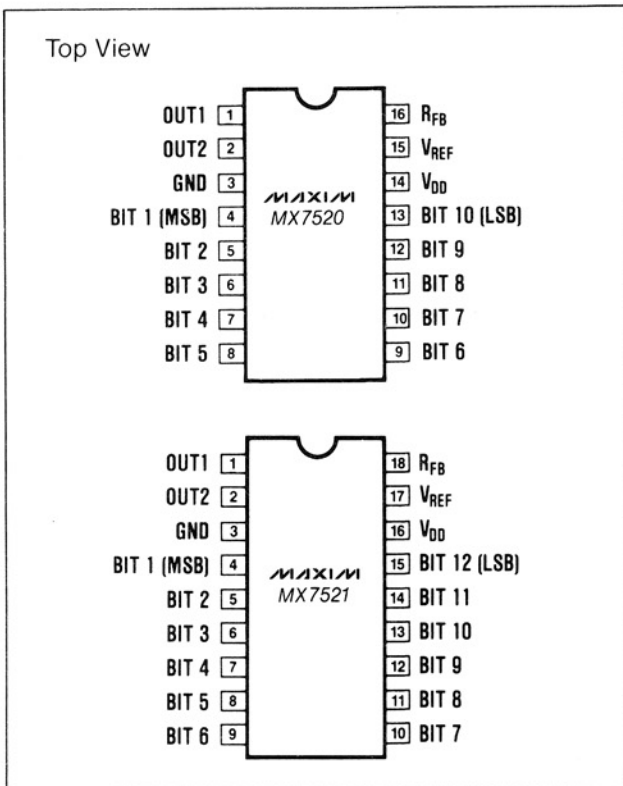
Features

♦ **10 or 12 Bit Resolution**

♦ **8, 9, and 10 Bit End Point Linearity**

♦ **Low Power Consumption — 20mW**

♦ **TTL and CMOS Compatible**

♦ **Pin-For-Pin Second Source**

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
MX7520JN	0°C to +70°C	Plastic DIP	0.2%
MX7520KN	0°C to +70°C	Plastic DIP	0.1%
MX7520LN	0°C to +70°C	Plastic DIP	0.05%
MX7520JCWE	0°C to +70°C	Small Outline	0.2%
MX7520KCWE	0°C to +70°C	Small Outline	0.1%
MX7520LCWE	0°C to +70°C	Small Outline	0.05%
MX7520J/D	0°C to +70°C	Dice	0.2%
MX7520JQ	-25°C to +85°C	CERDIP**	0.2%
MX7520KQ	-25°C to +85°C	CERDIP**	0.1%
MX7520LQ	-25°C to +85°C	CERDIP**	0.05%
MX7520JD	-25°C to +85°C	Ceramic	0.2%
MX7520KD	-25°C to +85°C	Ceramic	0.1%
MX7520LD	-25°C to +85°C	Ceramic	0.05%
MX7520SQ	-55°C to +125°C	CERDIP**	0.2%
MX7520TQ	-55°C to +125°C	CERDIP**	0.1%
MX7520UQ	-55°C to +125°C	CERDIP**	0.05%
MX7520SD	-55°C to +125°C	Ceramic	0.2%
MX7520TD	-55°C to +125°C	Ceramic	0.1%
MX7520UD	-55°C to +125°C	Ceramic	0.05%

* MX7520 — 16 lead package, MX7521 — 18 lead package.
** Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.

Pin Configuration

Typical Operating Circuit

10 Bit Plus Sign Multiplying DAC

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_____ *Maxim Integrated Products* 1

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

CMOS 10 and 12 Bit Multiplying D/A Converters

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .... -0.3V, +17V
V_{REF} to GND .... ±25V
R_{FB} to GND .... ±25V
Digital Input Voltage to GND .... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) .... -0.3V, V_{DD}
Power Dissipation (Derate 6mW/°C above +75°C) 450mW

Operating Temperature
   Commercial (JN/KN/LN/JC/KC/LC) .... 0°C to +70°C
   Industrial (JD/KD/LD/JQ/KQ/LQ) .... –25°C to +85°C
   Military (S/T/U) .... -55°C to +125°C
Storage Temperature .... -65°C to +150°C
Lead Temperature (Soldering 10 secs) .... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A=+25°C, V_{DD} =+ 15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
DC ACCURACY (Note 2)							
Resolution		MX7520			10		Bits
		MX7521			12		
Relative Accuracy (Note 3)		-10V ≤ V_{REF} ≤ +10V, T_A = T_{MIN} to T_{MAX}	0.2% FSR = 8 Bits J/S			±0.2	% FSR
			0.1% FSR = 9 Bits K/T			±0.1	
			0.05% FSR = 10 Bits L/U			±0.05	
Nonlinearity Tempco		-10V ≤ V_{REF} ≤ +10V (Note 4)				2	ppm/°C
Gain Error		-10V ≤ V_{REF} ≤ +10V (Note 5)			0.3		% FSR
Gain Error Tempco		-10V ≤ V_{REF} ≤ +10V (Note 4,5)				10	ppm/°C
Output Leakage Current		OUT1 or OUT2, T_A = T_{MIN} to T_{MAX}			200		nA
Power Supply Rejection	PSRR	(Note 3)			50		ppm/%V_{DD}
V_{REF} Input Resistance	R_{REF}	R_{REF} tempco = –150ppm/°C typ.		5	10	20	kΩ
AC ACCURACY							
Output Current Settling Time (Note 3)		To 0.05% of FSR, all digital inputs high to low and low to high.			500		ns
Feedthrough Error (Note 3,4,6)		All digital inputs low, V_{REF} = 20V_{P-P}, 100kHz sinewave.			10		mV_{P-P}
ANALOG OUTPUTS							
Output Capacitance (Note 3)	C_{OUT}	All digital inputs high,	OUT1		120		pF
			OUT2		37		
		All digital inputs low,	OUT1		37		
			OUT2		120		
Output Noise (Note 3)	e_N	Both outputs, equivalent Johnson noise resistance				10	kΩ
DIGITAL INPUTS (T_A = T_{MIN} to T_{MAX})							
Low State Threshold	V_{INL}					0.8	V
High State Threshold	V_{INH}			2.4			V
Input Current		Low to high state			±1		μA
Input Coding		Unipolar (Table 1), Bipolar (Table 2)		Binary, Offset Binary			
POWER REQUIREMENTS							
Power Supply Range	V_{DD}			+5		+15	V
Power Supply Current	I_{DD}	Digital inputs at GND			5		nA
		Digital inputs high or low				2	mA
Total Power Dissipation		Including V_{REF}			20		mW

Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum voltage if the current is limited to 30mA or less.
Note 2: Full Scale Range is 10V for unipolar mode and ±10V for bipolar mode.
Note 3: See Test Circuits.
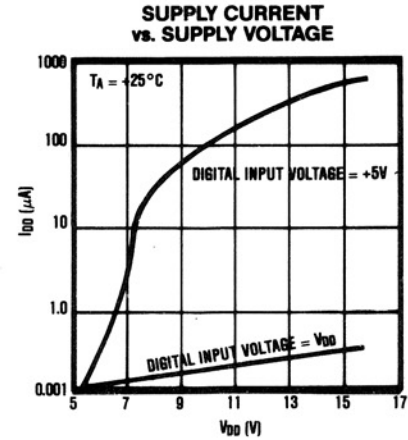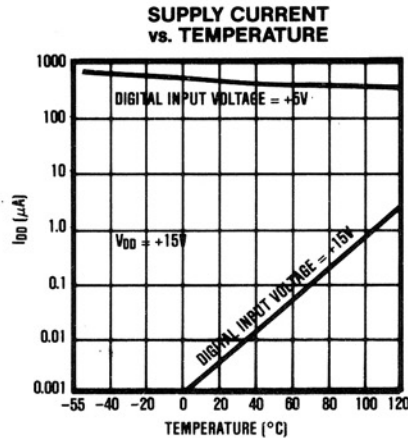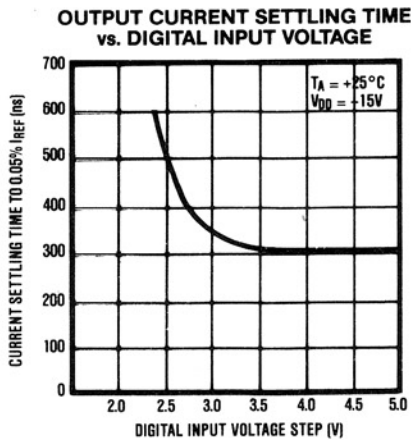**Note 4:** Guaranteed by design but not 100% tested.
Note 5: Using internal feedback resistor, R_{FB}.
Note 6: To minimize feedthrough with the ceramic package, the metal lid must be grounded. If the lid is not grounded, then the feedthrough is 10mV typical and 30mV maximum.

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OUTPUT CURRENT SETTLING TIME vs. DIGITAL INPUT VOLTAGE

SUPPLY CURRENT vs. TEMPERATURE

SUPPLY CURRENT vs. SUPPLY VOLTAGE

Detailed Description

The basic MX7520/21 DAC circuit consists of a laser-trimmed, thin-film R-2R resistor array with CMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. The V_{REF} input accepts a wide range of reference signals including fixed and time-varying voltage or current inputs.

A compensation capacitor, C1, may be needed when the DAC is used with a high speed amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. The correct compensation value depends on the type of op-amp used but typically ranges from 10 to 50pF.
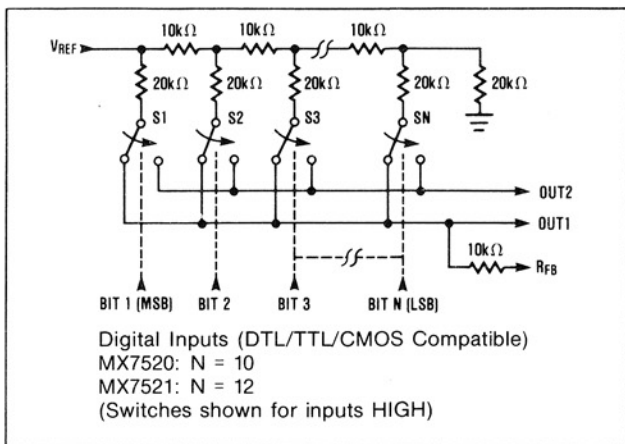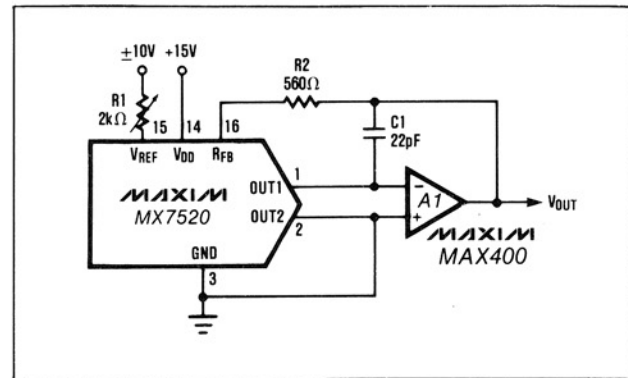

Figure 1. MX7520/MX7521 Functional Diagram

Digital Inputs (DTL/TTL/CMOS Compatible)
MX7520: N = 10
MX7521: N = 12
(Switches shown for inputs HIGH)

Figure 2. Unipolar Binary Operation (2-Quadrant Multiplication)

Application Information
Unipolar Operation

The most common configuration for the MX7520/21 is shown in Figure 2. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. R1 is used for gain adjustment. If no adjustment is desired, R1 and R2 can be omitted. The code table for unipolar operation is given in Table 1. Note that the output polarity is the inverse of the reference input.

Table 1: Code Table (MX7520) — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF} (1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF} (\frac{1}{2} + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1	$-V_{REF} (\frac{1}{2} - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF} (2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

Note: 1 LSB = $2^{-10} V_{REF}$ (MX7520)

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MX7520/MX7521 (vertical text, left margin)

The output op-amp's offset voltage can degrade DAC linearity by causing OUT1 to be terminated at a non-zero voltage. The resulting linearity error is typically $2/3 V_{OS}$. For best performance, a low-offset amplifier such as the MAX400 should be used, or the amplifier offset must be trimmed to typically no more than 1/10 of an LSB's value. The op-amp's input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error as well. I_B should therefore be much less than the DAC's output current for 1 LSB, which is typically $1\mu A$ for the MX7520 and 250nA for the MX7521.
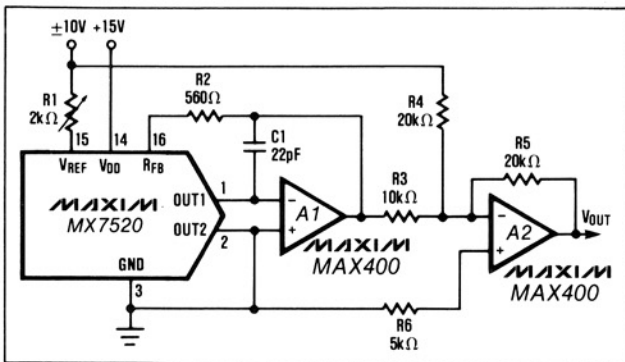

Figure 3. Bipolar Operation (4-Quadrant Multiplication)

Table 2: Code Table (MX7520) — Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}(2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}(1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

Note: 1 LSB = $2^{-9} V_{REF}$ (MX7520)

Bipolar Operation

Bipolar, or four-quadrant, operation is shown in Figure 3. A second amplifier and three matched resistors are required. The output vs. code table is listed in Table 2. In multiplying applications, the MSB determines polarity while the remaining bits control amplitude.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. The op-amp recommendations made in the Unipolar Operation section apply for bipolar operation as well.

Voltage Mode (Single Supply)

The MX7520 is connected as a voltage output DAC in Figure 4. OUT1 is connected to the external reference and OUT2 is grounded. V_{REF}, now the DAC output, is a voltage source with a constant output resistance of R_{ladder} (nominally 10kΩ). In most circuits this output is buffered with an op-amp.
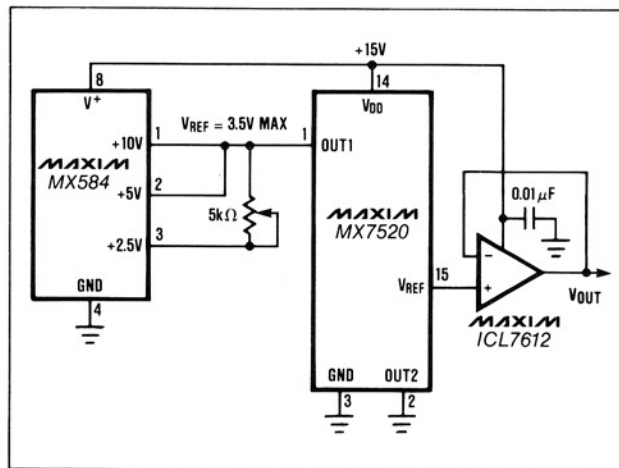

Figure 4. Single Supply Voltage Mode Operation

An advantage of voltage mode operation is single supply operation for the complete circuit, i.e. a negative reference is not required for a positive output. It is important to note that the range of the reference is restricted. The reference input (voltage at OUT1) must always be positive and is limited to no more than 3.5V when V_{DD} is 15V. If the reference voltage is greater than 3.5V, or V_{DD} is reduced, linearity is degraded.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dynamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is mostly dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.
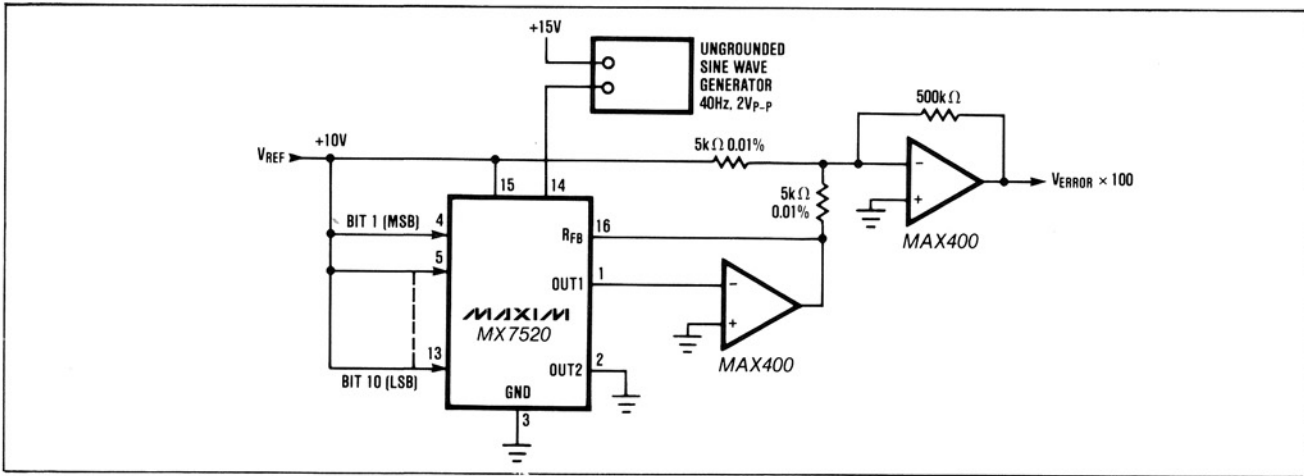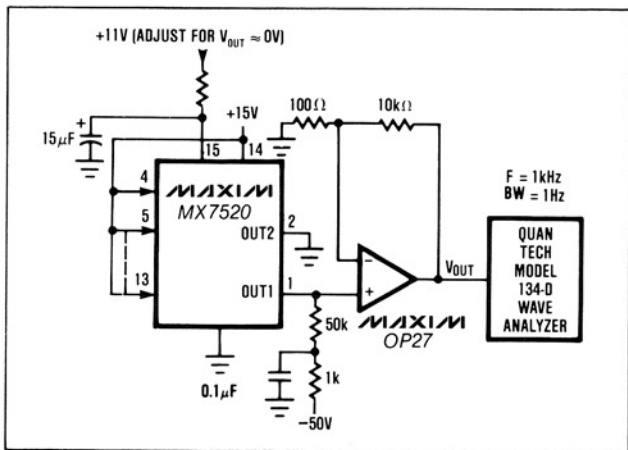
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Figure 5. Power Supply Rejection
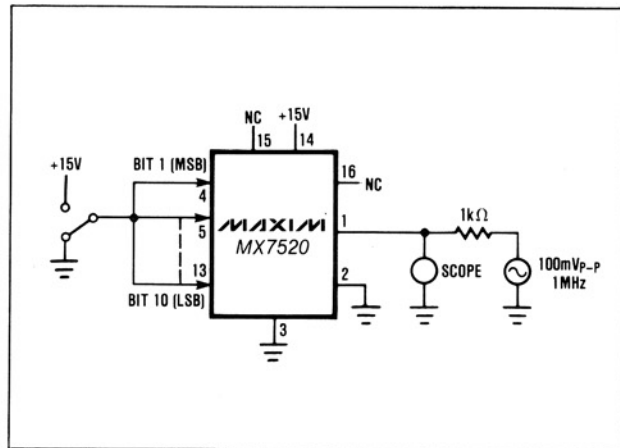

Figure 6. Noise

Figure 7. Output Capacitance
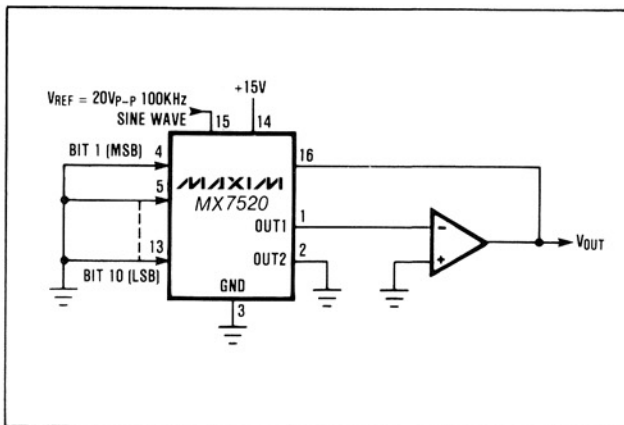
Figure 8. Feedthrough Error
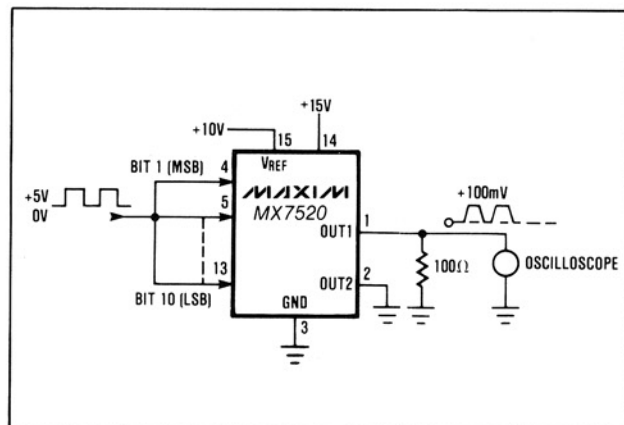
Figure 9. Output Current Settling Time

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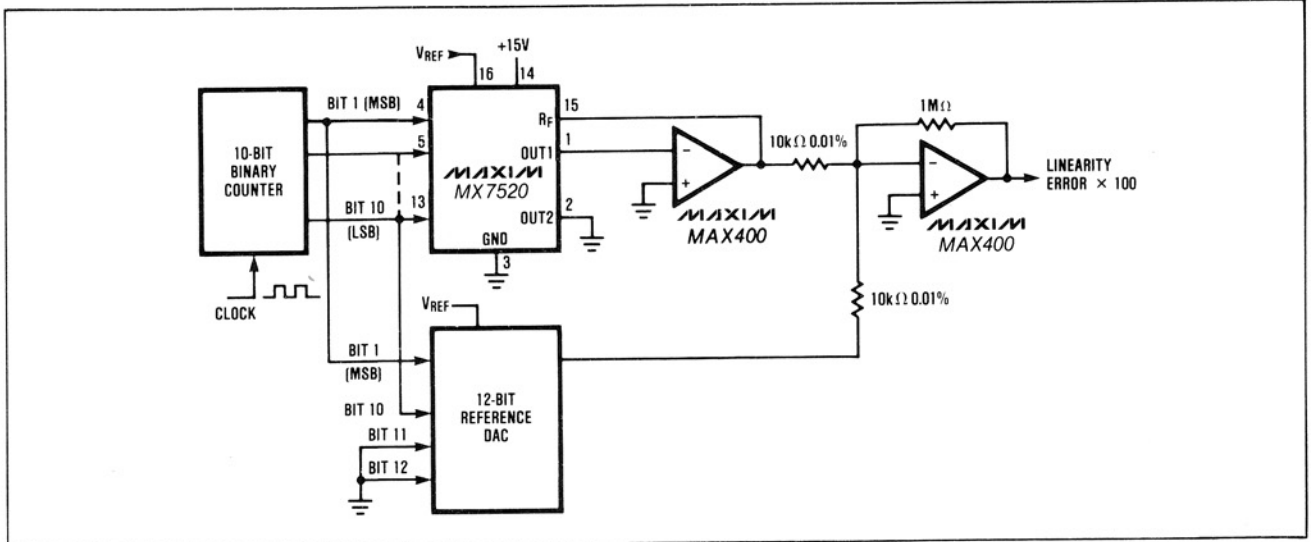
Figure 10. Relative Accuracy

Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
MX7521JN	0°C to +70°C	Plastic DIP	0.2%
MX7521KN	0°C to +70°C	Plastic DIP	0.1%
MX7521LN	0°C to +70°C	Plastic DIP	0.05%
MX7521JCWN	0°C to +70°C	Small Outline	0.2%
MX7521KCWN	0°C to +70°C	Small Outline	0.1%
MX7521LCWN	0°C to +70°C	Small Outline	0.05%
MX7521J/D	0°C to +70°C	Dice	0.2%
MX7521JQ	-25°C to +85°C	CERDIP**	0.2%
MX7521KQ	-25°C to +85°C	CERDIP**	0.1%
MX7521LQ	-25°C to +85°C	CERDIP**	0.05%
MX7521JD	-25°C to +85°C	Ceramic	0.2%
MX7521KD	-25°C to +85°C	Ceramic	0.1%
MX7521LD	-25°C to +85°C	Ceramic	0.05%
MX7521SQ	-55°C to +125°C	CERDIP**	0.2%
MX7521TQ	-55°C to +125°C	CERDIP**	0.1%
MX7521UQ	-55°C to +125°C	CERDIP**	0.05%
MX7521SD	-55°C to +125°C	Ceramic	0.2%
MX7521TD	-55°C to +125°C	Ceramic	0.1%
MX7521UD	-55°C to +125°C	Ceramic	0.05%

* MX7520 — 16 lead package, MX7521 — 18 lead package.
** Maxim reserves the right to ship Ceramic packages in lieu of
CERDIP packages.

Chip Topography

MAXIM

MX7520/MX7521

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

Plastic DIP
PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)

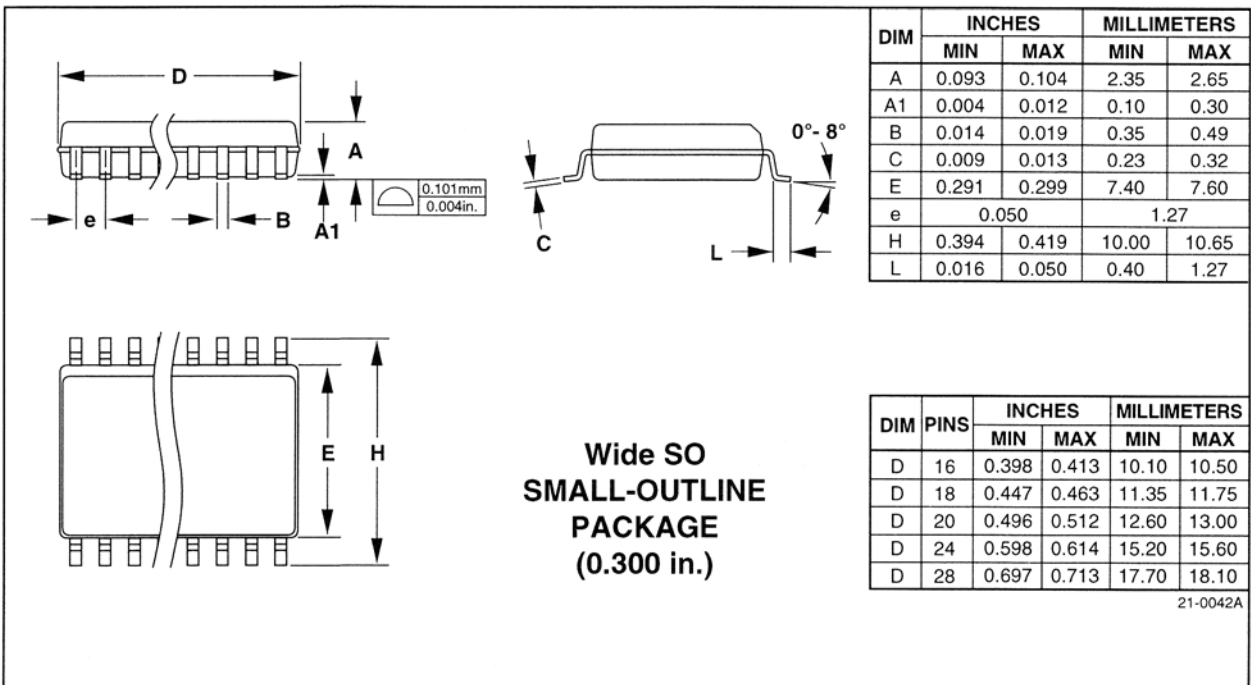| DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	–	2.54	–
eA	0.300	–	7.62	–
eB	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81

PKG.	DIM	PINS	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
P	D	8	0.348	0.390	8.84	9.91
P	D	14	0.735	0.765	18.67	19.43
P	D	16	0.745	0.765	18.92	19.43
P	D	18	0.885	0.915	22.48	23.24
P	D	20	1.015	1.045	25.78	26.54
N	D	24	1.14	1.265	28.96	32.13

21-0043A

Wide SO
SMALL-OUTLINE
PACKAGE
(0.300 in.)

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
E	0.291	0.299	7.40	7.60
e	0.050		1.27	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27

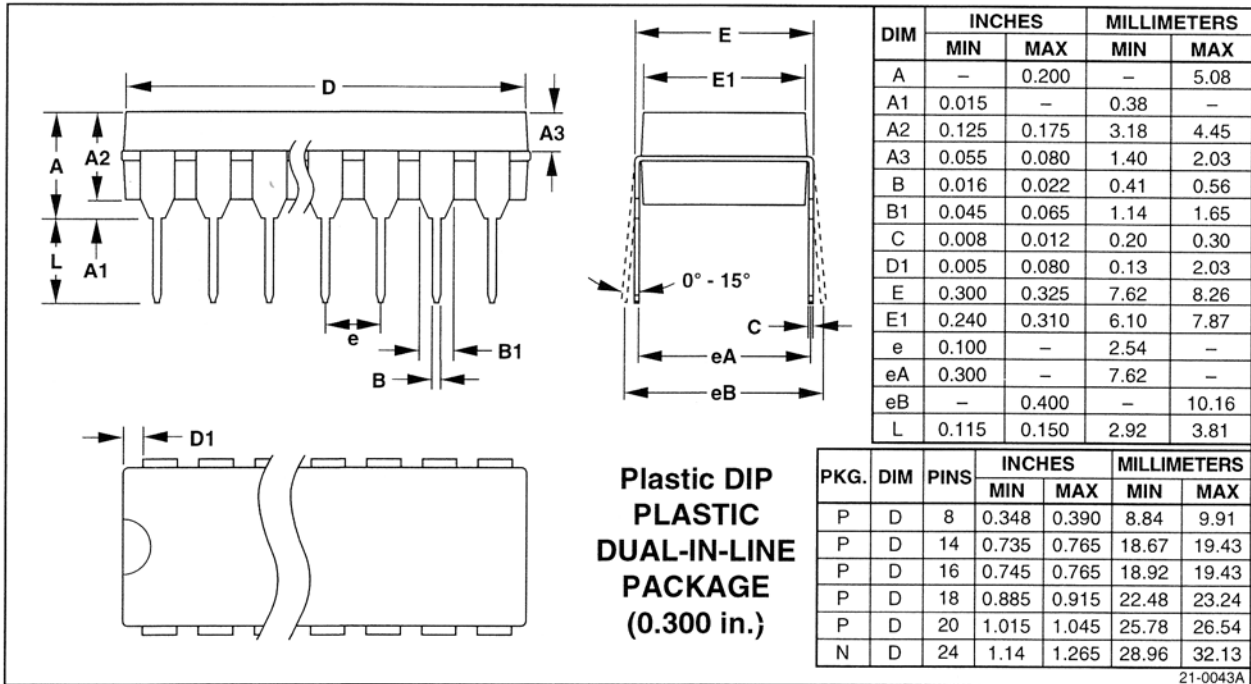| DIM	PINS	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
D	16	0.398	0.413	10.10	10.50
D	18	0.447	0.463	11.35	11.75
D	20	0.496	0.512	12.60	13.00
D	24	0.598	0.614	15.20	15.60
D	28	0.697	0.713	17.70	18.10

21-0042A

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CMOS 10 and 12 Bit
Multiplying D/A Converters

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.070	0.38	1.78
S	–	0.098	–	2.49
S1	0.005	–	0.13	–

DIM	PINS	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
D	8	–	0.405	–	10.29
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51

CERDIP CERAMIC DUAL-IN-LINE PACKAGE (0.300 in.)

21-0045A

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	–	0.225	–	5.72
B	0.014	0.023	0.36	0.58
B2	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
eA	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
Q	0.015	0.070	0.38	1.78
S1	0.005	–	0.13	–

DIM	PINS	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
D	8	–	0.550	–	13.97
D	14	–	0.785	–	19.94
D	16	–	0.840	–	21.34
D	18	–	0.960	–	24.38
D	20	–	1.060	–	26.92
D	24	–	1.280	–	32.51

Ceramic SB CERAMIC SIDEBRAZE PACKAGE (0.300 in.)

21-0047A

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