74ALVCH16501

18-bit universal bus transceiver; 3-state

Rev. 5 — 10 July 2012 Product data sheet

1. General description

The 74ALVCH16501 is an 18-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and $\overline{\text{OEBA}}$), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if CPAB is held at a HIGH or LOW logic level. If LEAB is LOW, the A-bus data is stored in the latch/flip-flop on the LOW-to HIGH transition of CPAB. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses $\overline{\text{OEBA}}$, LEBA and CPBA. The output enables are complimentary (OEAB is active HIGH, and $\overline{\text{OEBA}}$ is active LOW.

To ensure the high-impedance state during power-up or power-down, $\overline{\text{OEBA}}$ should be tied to V_{CC} through a pull-up resistor and OEAB should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standard JESD8-B
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ±24 mA at V_{CC} = 3.0 V
- Universal bus transceiver with D-type latches and D-type flip-flops capable of operating in transparent, latched or clocked mode
- All inputs have bus hold circuitry
- Output drive capability 50 Ω transmission lines at 85 °C
- 3-state non-inverting outputs for bus-oriented applications

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVCH16501DGG	–40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1
74ALVCH16501DL	–40 °C to +85 °C	SSOP56	plastic shrink small outline package; 56 leads; body width 7.5 mm	SOT371-1

4. Functional diagram

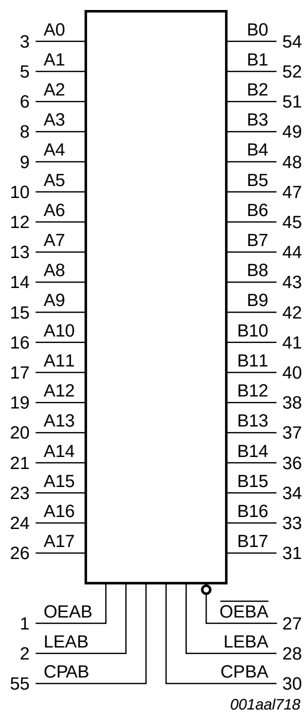


Fig 1. Logic symbol

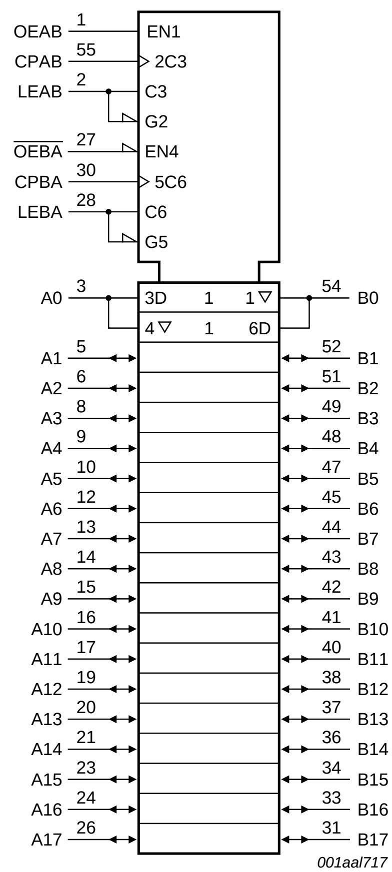


Fig 2. IEC logic symbol

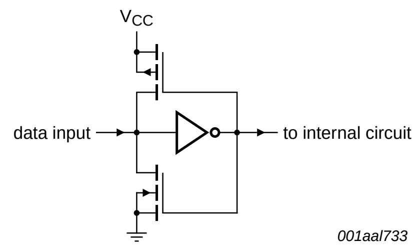


Fig 3. Bus hold circuit

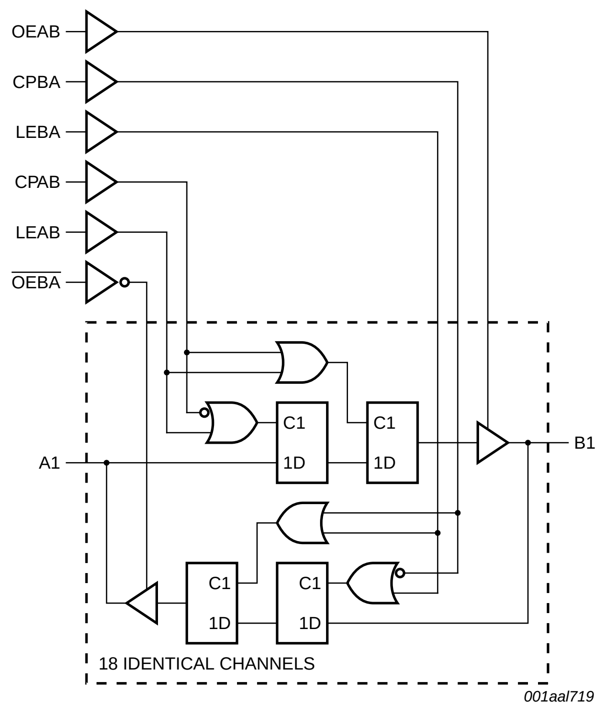


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

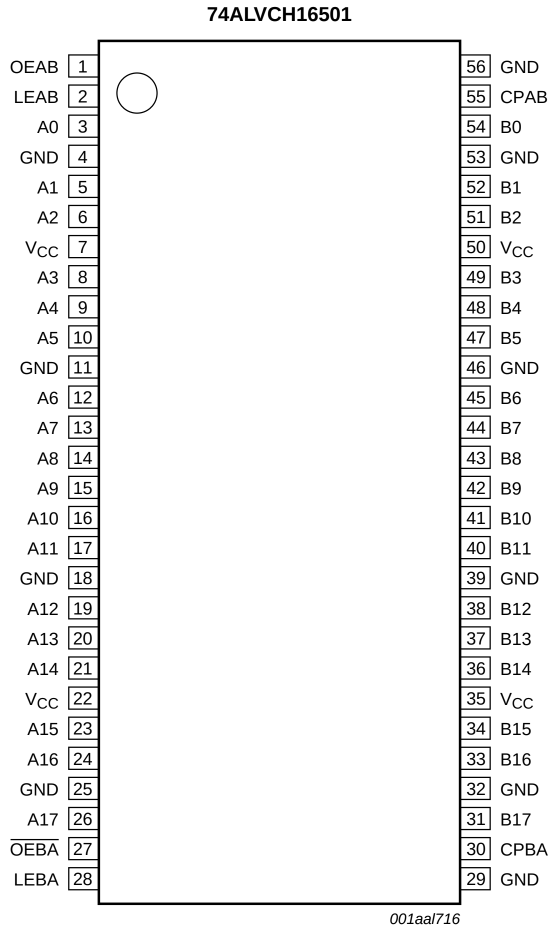


Fig 5. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
OEAB	1	output enable A-to-B input
LEAB	2	latch enable A-to-B input
A0 to A17	3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	data inputs or outputs
GND	4, 11, 18, 25, 29, 32, 39, 46, 53, 56	ground (0 V)
V_{CC}	7, 22, 35, 50	positive supply voltage
$\overline{OEBA}$	27	output enable B-to-A
LEBA	28	latch enable B-to-A

Table 2. Pin description *...continued*

Symbol	Pin	Description
CPBA	30	clock input B-to-A
B0 to B17	54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	data inputs or outputs
CPAB	55	clock input A-to-B

6. Functional description

6.1 Function table

Table 3. Function table[1]

Inputs				Output	Operating mode
$\overline{OEAB}$	LEAB	CPAB	An	Bn	
L	X	X	X	Z	disabled
H	H	X	H	H	transparent
H	H	X	L	L	
H	↓	X	h	H	latch data and display
H	↓	X	l	L	
H	L	↑	h	H	clock data and display
H	L	↑	l	L	
H	L	H or L	X	H	hold data and display
H	L	H or L	X	L	

[1] A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA and CPBA.
H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the enable or clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the enable or clock transition;
X = don't care;
Z = high-impedance OFF-state;
↓ = HIGH-to-LOW clock transition;
↑ = LOW-to-HIGH clock transition.

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	-	mA
V_I	input voltage	control inputs	[1]	–0.5	+4.6	V
		data inputs	[1]	–0.5	V_{CC} + 0.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage		[1]	–0.5	V_{CC} + 0.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA

Table 4. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{GND}	ground current			–100	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C				
		SSOP package	[2]	-	850	mW
		TSSOP package	[3]	-	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 55 °C the value of P_{tot} derates linearly with 11.3 mW/K.

[3] Above 55 °C the value of P_{tot} derates linearly with 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	maximum speed performance				
		C_L = 30 pF	2.3	-	2.7	V
		C_L = 50 pF	3.0	-	3.6	V
		low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.3 V to 3.0 V	0	-	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
T_{amb} = –40 °C to +85 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 V to 2.7 V		1.7	1.2	-	V
		V_{CC} = 2.7 V to 3.6 V		2.0	1.5	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 V to 2.7 V		-	1.2	0.7	V
		V_{CC} = 2.7 V to 3.6 V		-	1.5	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –100 µA; V_{CC} = 2.3 V to 3.6 V		V_{CC} – 0.2	V_{CC}	-	V
		I_O = –6 mA; V_{CC} = 2.3 V		V_{CC} – 0.3	V_{CC} – 0.08	-	V
		I_O = –12 mA; V_{CC} = 2.3 V		V_{CC} – 0.6	V_{CC} – 0.26	-	V
		I_O = –12 mA; V_{CC} = 2.7 V		V_{CC} – 0.5	V_{CC} – 0.14	-	V
		I_O = –12 mA; V_{CC} = 3.0 V		V_{CC} – 0.6	V_{CC} – 0.09	-	V
		I_O = –24 mA; V_{CC} = 3.0 V		V_{CC} – 1.0	V_{CC} – 0.28	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 100 µA; V_{CC} = 2.3 V to 3.6 V		-	GND	0.20	V
		I_O = 6 mA; V_{CC} = 2.3 V		-	0.07	0.40	V
		I_O = 12 mA; V_{CC} = 2.3 V		-	0.15	0.70	V
		I_O = 12 mA; V_{CC} = 2.7 V		-	0.14	0.40	V
		I_O = 24 mA; V_{CC} = 3.0 V		-	0.27	0.55	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 2.3 V to 3.6 V		-	0.1	5	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND; V_{CC} = 2.7 V to 3.6 V		-	0.1	10	µA
I_{CC}	supply current	V_{CC} = 2.3 V to 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A		-	0.2	40	µA
ΔI_{CC}	additional supply current	per data I/O pin; V_{CC} = 2.3 V to 3.6 V; $V_I = V_{CC}$ – 0.6 V; I_O = 0 A		-	150	750	µA
I_{BHL}	bus hold LOW current	V_{CC} = 2.3 V; V_I = 0.7 V	[2]	45	-	-	µA
		V_{CC} = 3.0 V; V_I = 0.8 V	[2]	75	150	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 2.3 V; V_I = 1.7 V	[2]	–45	-	-	µA
		V_{CC} = 3.0 V; V_I = 2.0 V	[2]	–75	–175	-	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 3.6 V	[2]	500	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 3.6 V	[2]	–500	-	-	µA
C_I	input capacitance			-	4.0	-	pF
$C_{I/O}$	input/output capacitance			-	8.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] Valid for data inputs of bus hold parts only.

10. Dynamic characteristics

Table 7. Dynamic characteristics
At recommended operating conditions. Voltages are referenced to GND (ground = 0 V); test circuit Figure 10.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
T_{amb} = −40 °C to +85 °C							
f_{max}	maximum frequency	see Figure 8					
		V_{CC} = 2.3 V to 2.7 V	[2]	150	333	-	MHz
		V_{CC} = 3.0 V to 3.6 V	[3]	150	340	-	MHz
		V_{CC} = 2.7 V		150	333	-	MHz
t_{pd}	propagation delay	An to Bn; Bn to An; see Figure 6	[4]				
		V_{CC} = 2.3 V to 2.7 V	[2]	1.0	2.8	5.1	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	1.0	3.0	4.2	ns
		V_{CC} = 2.7 V		-	3.0	4.6	ns
		LEAB, LEBA to Bn, An; see Figure 8					
		V_{CC} = 2.3 V to 2.7 V	[2]	1.1	3.5	6.1	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	1.3	3.4	4.8	ns
		V_{CC} = 2.7 V		-	3.6	5.3	ns
		CPAB, CPBA to Bn, An; see Figure 8					
		V_{CC} = 2.3 V to 2.7 V	[2]	1.0	3.3	6.1	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	1.4	3.3	4.9	ns
		V_{CC} = 2.7 V		-	3.4	5.6	ns
t_{en}	enable time	$\overline{OEBA}$ to An; see Figure 7	[4]				
		V_{CC} = 2.3 V to 2.7 V	[2]	1.3	2.8	6.3	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	1.1	2.5	5.0	ns
		V_{CC} = 2.7 V		-	3.3	6.0	ns
		OEAB to Bn; see Figure 7					
		V_{CC} = 2.3 V to 2.7 V	[2]	1.0	2.5	5.8	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	1.0	2.4	4.6	ns
		V_{CC} = 2.7 V		-	2.7	5.3	ns
t_{dis}	disable time	$\overline{OEBA}$ to An; see Figure 7	[4]				
		V_{CC} = 2.3 V to 2.7 V	[2]	1.3	2.5	5.3	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	1.3	3.1	4.2	ns
		V_{CC} = 2.7 V		-	3.3	4.6	ns
		OEAB to Bn; see Figure 7					
		V_{CC} = 2.3 V to 2.7 V	[2]	1.5	2.5	6.2	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	1.4	2.9	5.0	ns
		V_{CC} = 2.7 V		-	3.6	5.7	ns

Table 7. Dynamic characteristics *...continued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V); test circuit Figure 10.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_W	pulse width	LEAB, LEBA HIGH; see Figure 8					
		V_{CC} = 2.3 V to 2.7 V	[2]	3.3	0.8	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	3.3	0.9	-	ns
		V_{CC} = 2.7 V		3.3	0.7	-	ns
		CPAB, CPBA HIGH or LOW; see Figure 8					
		V_{CC} = 2.3 V to 2.7 V	[2]	3.3	2.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	3.3	1.1	-	ns
		V_{CC} = 2.7 V		3.3	1.4	-	ns
t_{su}	set-up time	An, Bn to CPAB, CPBA; see Figure 9					
		V_{CC} = 2.3 V to 2.7 V	[2]	1.7	0.1	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	1.3	–0.3	-	ns
		V_{CC} = 2.7 V		1.4	–0.1	-	ns
		An, Bn to LEAB, LEBA; see Figure 9					
		V_{CC} = 2.3 V to 2.7 V	[2]	1.1	0.1	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	1.0	0.3	-	ns
		V_{CC} = 2.7 V		1.0	–0.2	-	ns
t_h	hold time	An, Bn to CPAB, CPBA; see Figure 9					
		V_{CC} = 2.3 V to 2.7 V	[2]	1.7	0.3	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	1.3	0.4	-	ns
		V_{CC} = 2.7 V		1.6	0.3	-	ns
		An, Bn to LEAB, LEBA; see Figure 9					
		V_{CC} = 2.3 V to 2.7 V	[2]	1.6	0.3	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	1.2	0.1	-	ns
		V_{CC} = 2.7 V		1.5	0.1	-	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC}	[5]				
		outputs enabled		-	21	-	pF
		outputs disabled		-	3	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

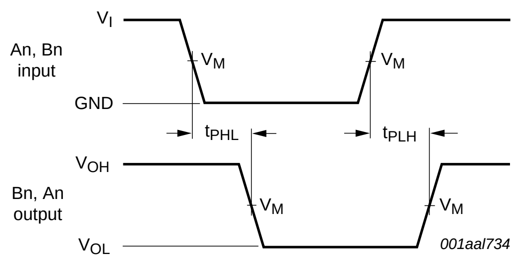
[2] Typical values are measured at V_{CC} = 2.5 V.

[3] Typical values are measured at V_{CC} = 3.3 V.

[4] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts;
N = total load switching outputs;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

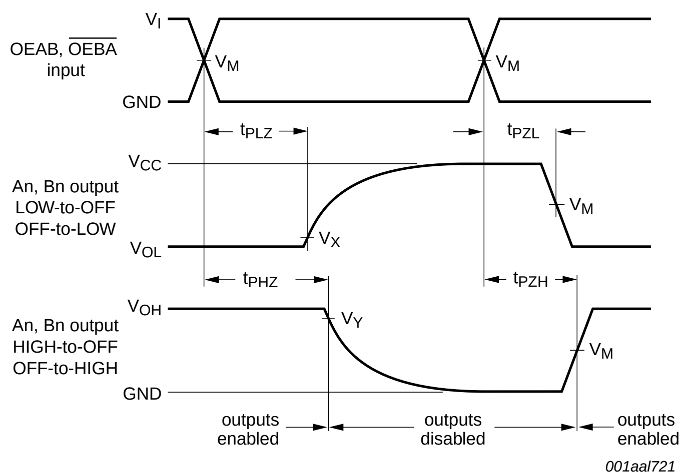
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output levels that occur with the output load.

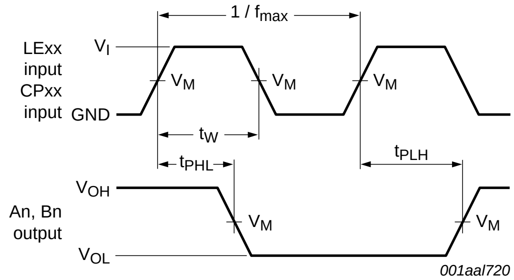
Fig 6. Propagation delay, data input (An, Bn) to data output (Bn, An)



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output levels that occur with the output load.

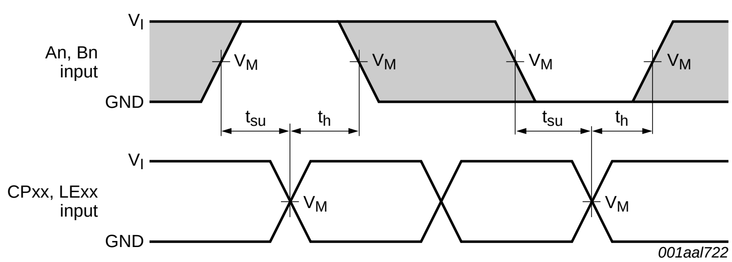
Fig 7. 3-state output enable and disable times



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output levels that occur with the output load.

Fig 8. Propagation delay, latch enable input (LEAB, LEBA) and clock pulse input (CPAB, CPBA) to data output, and pulse width



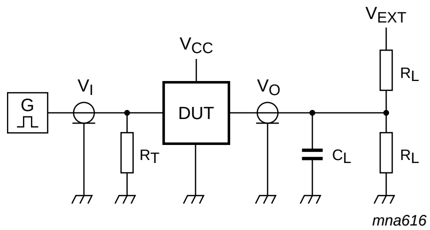
Measurement points are given in Table 8.

Fig 9. Data set-up and hold times (An, Bn inputs to LEAB, LEBA, CPAB and CPBA inputs)

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
2.3 V to 2.7 V and < 2.3 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{OL} + 0.15 V	V_{OH} – 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} – 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} – 0.3 V

12. Test information



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance includes jig and probe capacitance.

R_T = Termination resistance should be equal to Z_o of pulse generator.

V_{EXT} = External voltage for measuring switching times.

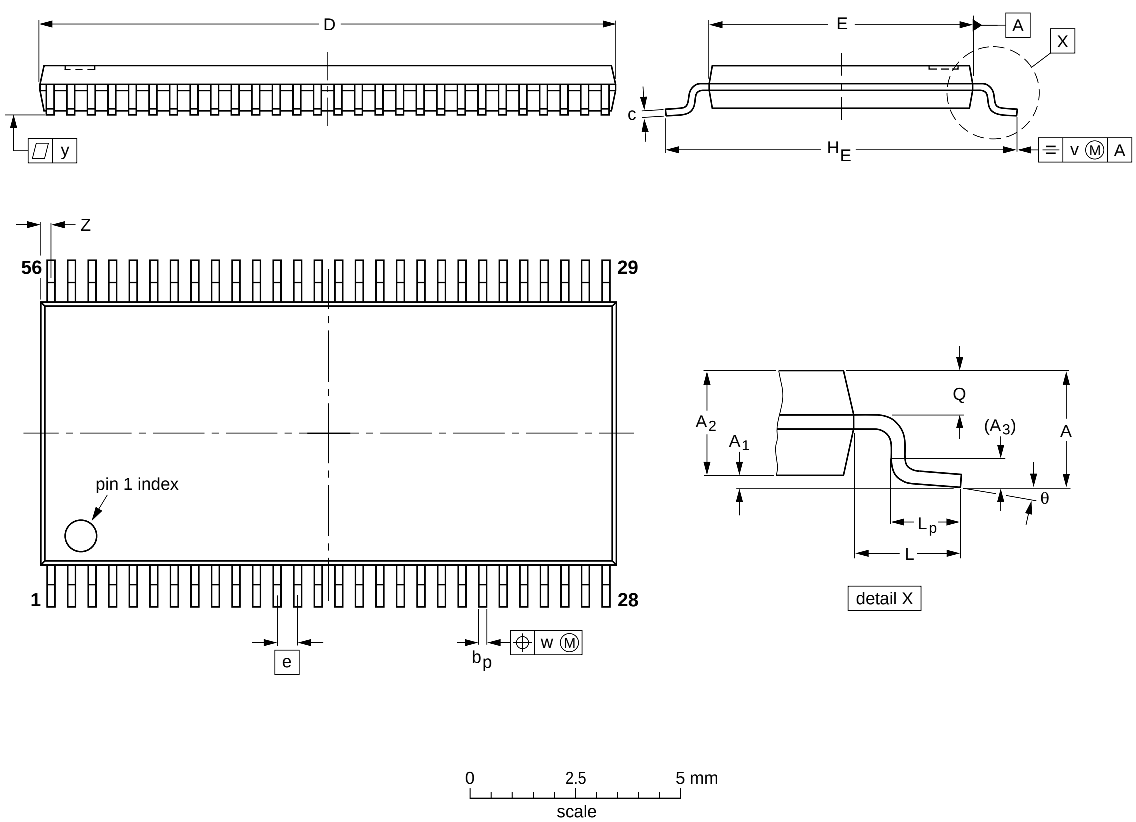
Fig 10. Load circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

13. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

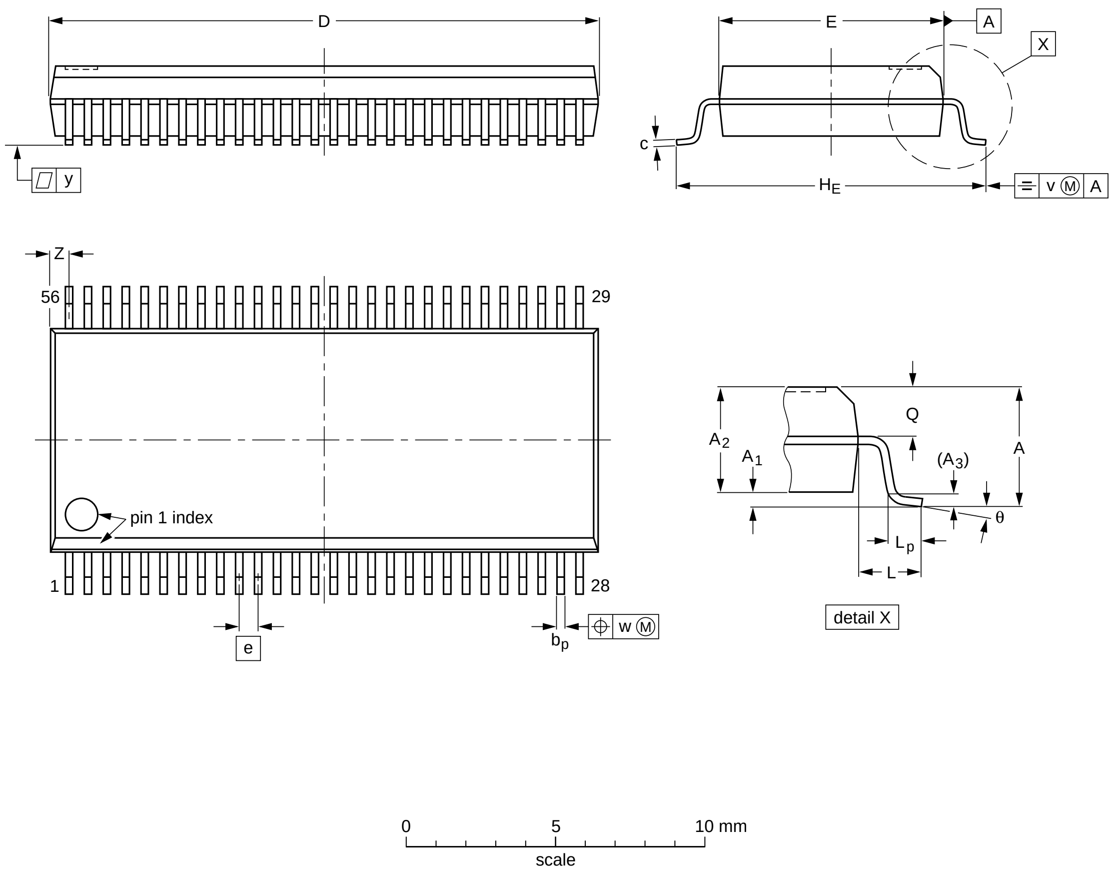
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT364-1 (TSSOP56)

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT371-1		MO-118				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT371-1 (SSOP56)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
74ALVCH16501 v.5	20120710	Product data sheet	-	-	74ALVCH16501 v.4
Modifications:	• Table 8 corrected (errata).				
74ALVCH16501 v.4	20111117	Product data sheet	-	-	74ALVCH16501 v.3
Modifications:	• Legal pages updated.				
74ALVCH16501 v.3	20100402	Product data sheet	-	-	74ALVCH16501 v.2
74ALVCH16501 v.2	19980929	Product specification	-	-	74ALVCH16501 v.1
74ALVCH16501 v.1	19980929	Product specification	-	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

18. Contents

Date of release: 10 July 2012
Document identifier: 74ALVCH16501