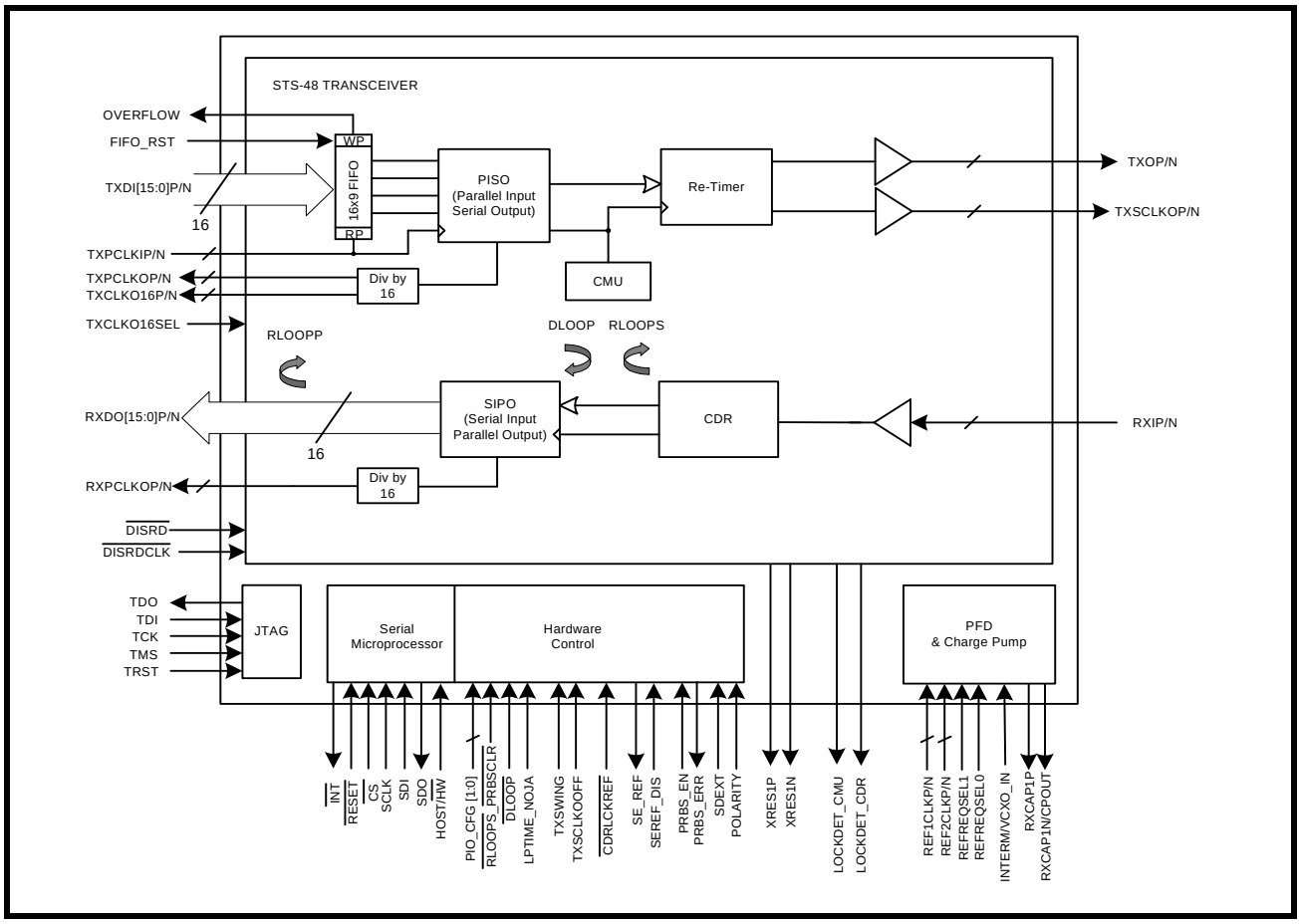
GENERAL DESCRIPTION

The XRT91L82 is a fully integrated SONET/SDH transceiver for OC-48/STM16 applications supporting the use of Forward Error Correction (FEC) capability. The transceiver includes an on-chip Clock Multiplier Unit (CMU), which uses a high frequency Phase-Locked Loop (PLL) to generate the high-speed transmit serial clock from slower external clock references. It also provides Clock and Data Recovery (CDR) functions by synchronizing its on-chip Voltage Controlled Oscillator (VCO) to the incoming serial data stream. The chip provides serial-to-parallel and parallel-to-serial converters and 16-bit Differential LVDS/LVPECL, or Single-Ended LVPECL system interfaces in both receive and transmit directions. The transmit section includes a 16x9 Elastic Buffer (FIFO) to absorb any phase differences between the transmitter clock input and the internally generated transmitter reference clock. In the event of an overflow, an internal FIFO control circuit outputs an OVERFLOW indication. The FIFO under the control of the FIFO_AUTORST register bit can automatically recover from an overflow condition. The operation of the device can be monitored by checking the status of the LOCKDET_CMU and LOCKDET_CDR output signals. An on-chip phase/frequency detector and charge-pump offers the ability to form a de-jittering PLL with an external VCXO that can be used in loop timing mode to clean up the recovered clock in the receive section.

APPLICATIONS

- SONET/SDH-based Transmission Systems
- Add/Drop Multiplexers
- Cross Connect Equipment
- ATM and Multi-Service Switches, Routers and Switch/Routers
- DSLAMS
- SONET/SDH Test Equipment
- DWDM Termination Equipment

FIGURE 1. BLOCK DIAGRAM OF XRT91L82



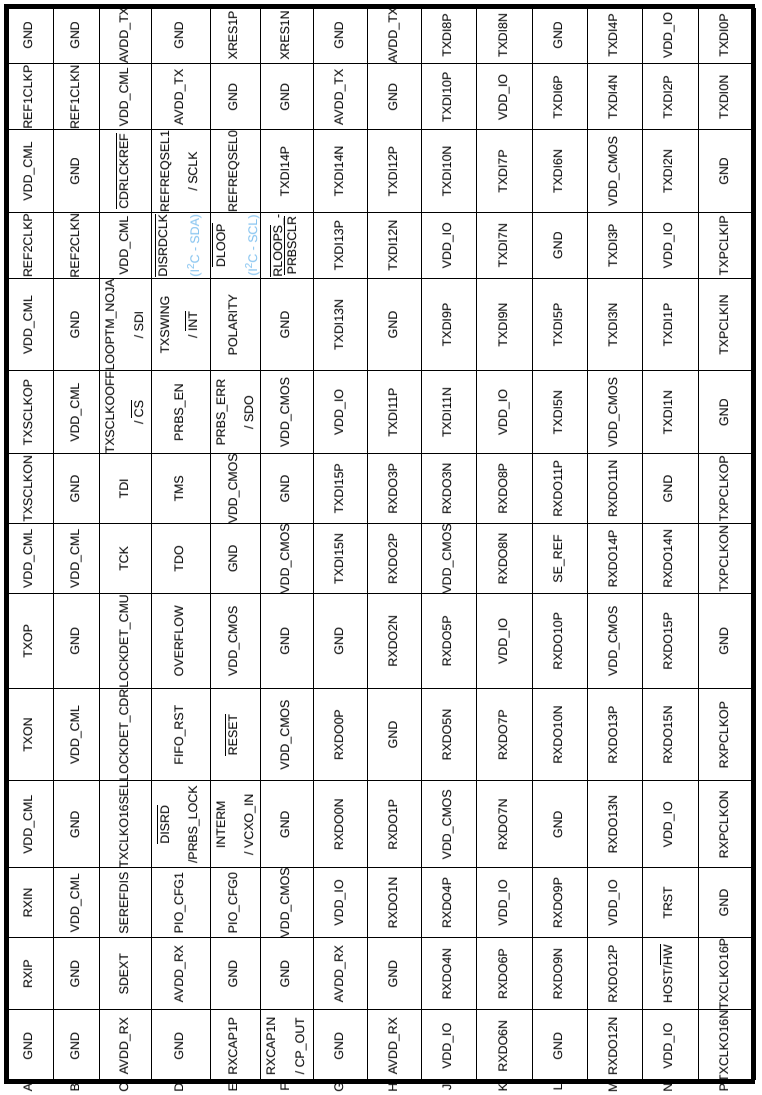
FEATURES

- 2.488 / 2.666 Gbps Transceiver
- Targeted for SONET OC-48/SDH STM-16 Applications
- Selectable full duplex operation between standard rate of 2.488 Gbps or Forward Error Correction rate of 2.666 Gbps
- Single-chip fully integrated solution containing parallel-to-serial converter, clock multiplier unit (CMU), serial-to-parallel converter, and clock data recovery (CDR) functions
- 16-bit Differential LVDS/LVPECL, or Single-Ended LVPECL signaling data paths running at 155.52/166.63 Mbps using internal input termination for reduced passive components on board
- Non-FEC and FEC rate REF1CLKP/N and REF2CLKP/N dual reference input ports
- Supports 155.52/166.63MHz or 77.76/83.31MHz transmit and receive external reference input ports
- Optional VCXO input port support multiple de-jittering modes in Host mode
- On-chip phase detector and charge pump for external VCXO based de-jittering PLL
- Internal FIFO decouples transmit parallel clock input and transmit parallel clock output
- Provides Local, Remote Serial and Remote Parallel Loopback modes as well as Loop Timing mode
- Diagnostics features include various lock detect functions and transmit CMU and receive CDR Lock Detect
- Host mode serial microprocessor interface simplifies monitor and control
- Meets Telcordia, ANSI and ITU-T jitter requirements including T1.105.03 - 2002 SONET Jitter Tolerance specification, GR-253 CORE, GR-253-ILR- SONET Jitter specifications.
- Operates at 1.8V CMOS and CML Power with 3.3V I/O
- 500mW Typical Power Dissipation using LVDS Interface
- Package: 15 x 15 mm 196-pin STBGA
- IEEE 1149.1 Compatable JTAG port

PRODUCT ORDERING INFORMATION

PRODUCT NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT91L82IB	196 STBGA	-40℃ to +85℃

FIGURE 2. 196 BGA PINOUT OF THE XRT91L82 (TOP VIEW)



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PIN DESCRIPTIONS

COMMON CONTROL

NAME	LEVEL	TYPE	PIN	DESCRIPTION
$\overline{\text{RESET}}$	LVTTL, LVCMOS	I	E5	**Master Reset Input** Active low signal. When this pin is pulled "Low" for more than 30ns, the internal registers are set to their default state. See the register description for the default values. This pin is provided with an internal pull-up.
PIO_CFG1 PIO_CFG0	LVTTL, LVCMOS	I	D3 E3	**Parallel I/O Configuration** Selects parallel I/O to be differential LVDS, differential LVPECL, or Single-Ended LVPECL based on table below. This pin is provided with an internal pull-down.
XRES1P XRES1N	-	I	E14 F14	**External LVDS Biasing Resistors** A 402Ω resistor with +/-1% tolerance should be placed across these 2 pins for proper biasing. Although unecessary in LVPECL operation, this resistor is required in LVDS operation. See Figure 8 on page 22.
SE_REF	Analog	O	L7	**Single-Ended LVPECL Biasing Output Reference** **VBB** 100K output bias reference. Maximum load capacitance is 30pF. Maximum sourcing/sinking capability is 750µA and 1000µA respectively.
SEREFDIS	LVTTL, LVCMOS	I	C3	**SE_REF Power down Control** Powers down SE_REF and reduces power consumption. "Low" = SE_REF Enabled "High" = SE_REF Disabled This pin is provided with an internal pull-up.
REF1CLKP REF1CLKN	LVPECL Diff	I	A13 B13	**Reference Clock Input 1** This differential clock input reference is used for the transmit clock multiplier unit (CMU) and clock data recovery (CDR) to provide the necessary high-speed clock reference for this device. Pin REFREQSEL[1:0] determines the value used as the reference. See Pin REFREQSEL[1:0] for more details. Internally terminated and biased.

PIO_CFG [1:0]	VDD_I/O	Input Configuration	Output Configuration
00	3.3V	3.3V Differential LVPECL	3.3V Differential LVPECL
01	3.3V	3.3V Single-Ended LVPECL	3.3V Single-Ended LVPECL
10	3.3V	3.3V Differential LVDS	3.3V Differential LVDS
11	Reserved		

COMMON CONTROL

NAME	LEVEL	TYPE	PIN	DESCRIPTION
REF2CLKP REF2CLKN	LVPECL Diff	I	A11 B11	**Reference Clock Input 2** This differential clock input reference is used for the transmit clock multiplier unit (CMU) and clock data recovery (CDR) to provide the necessary high-speed clock reference for this device. Pin REFREQSEL[1:0] determines the value used as the reference. See Pin REFREQSEL[1:0] for more details. Internally terminated and biased.
REFREQSEL1 / SCLK	LVTTL, LVCMOS	I	D12	**Reference Clock Frequency Select** **Hardware Mode** REFREQSEL1 pin is used to select the frequency of the REF1CLK and/or REF2CLK input to the CMU and CDR. **REFREQSEL [1:0]** / **CMU REFERENCE FREQUENCY** / **CDR REFERENCE FREQUENCY** **00**: 155.52 MHz present on REF1CLK, REF2CLK not used / 155.52 MHz present on REF1CLK, REF2CLK not used **01**: 155.52 MHz present on REF1CLK / 166.63 MHz present on REF2CLK **10**: 166.63 MHz present on REF2CLK / 155.52 MHz present on REF1CLK **11**: 166.63 MHz present on REF2CLK, REF1CLK not used / 166.63 MHz present on REF2CLK, REF1CLK not used ***NOTE:*** *Non-FEC rates require 155.52 MHz clock reference. FEC rates require 166.63 MHz clock reference* This pin is provided with an internal pull-down. **Host Mode** This pin is functions as the microprocessor Serial Clock Input.
REFREQSEL0	LVTTL, LVCMOS	I	E12	**Reference Clock Frequency Select** REFREQSEL0 pin is used to select the frequency of the REF1CLK and/or REF2CLK input to the CMU and CDR. **REFREQSEL [1:0]** / **CMU REFERENCE FREQUENCY** / **CDR REFERENCE FREQUENCY** **00**: 155.52 MHz present on REF1CLK, REF2CLK not used / 155.52 MHz present on REF1CLK, REF2CLK not used **01**: 155.52 MHz present on REF1CLK / 166.63 MHz present on REF2CLK **10**: 166.63 MHz present on REF2CLK / 155.52 MHz present on REF1CLK **11**: 166.63 MHz present on REF2CLK, REF1CLK not used / 166.63 MHz present on REF2CLK, REF1CLK not used ***NOTE:*** *Non-FEC rates require 155.52 MHz clock reference. FEC rates require 166.63 MHz clock reference* This pin is provided with an internal pull-down.

COMMON CONTROL

NAME	LEVEL	TYPE	PIN	DESCRIPTION
PRBS_EN	LVTTL, LVCMOS	I	D9	**2^{23}-1 PRBS TEST Pattern Enable** Generates 2^{23}-1 Pseudo Random Binary Sequence test patterns and analyzes in the receiving block for proper reception. "Low" = Normal Mode "High" = PRBS pattern generator and analyzer Enabled. ***NOTE:*** *A Local Loopback of some type such as Digital Local Loopback or an optical cable loopback is expected to be used in conjunction with PRBS_EN in order for the PRBS analyzer to receive the PRBS pattern.* This pin is provided with an internal pull-down.
PRBS_ERR /SDO	LVCMOS	O	E9	**2^{23}-1 PRBS Pattern Validation Error** **Hardware Mode** Indicates an error condition has occurred/is occuring in the validation of generated PRBS pattern. "Low" = Un-erred transmission and reception of PRBS pattern. "High" = Error Condition occurrence. **Host Mode** This pin is functions as the microprocessor Serial Data Output.
$\overline{\text{RLOOPS\_}}$ - $\overline{\text{PRBSCLR}}$	LVTTL, LVCMOS	I	F11	**Serial Remote Loopback** **Normal Mode** The serial remote loopback mode interconnects the receive serial data input to the transmit serial data output. If serial remote loopback is enabled, the 16-bit parallel transmit data input is ignored while the 16-bit parallel receive data output and parallel receive clock output is maintained. "Low" = Serial Remote Loopback Mode Enabled "High" = Disabled **PRBSTest Mode** When PRBS_EN is asserted, this bit is used to clear or reset PRBS_ERR error condition. Serial Remote Loopback is not available in PRBS Test Mode. "Low" = Clears PRBS_ERR condition "High" = Normal Mode This pin is provided with an internal pull-up.

COMMON CONTROL

NAME	LEVEL	TYPE	PIN	DESCRIPTION
$\overline{\text{DLOOP}}$	LVTTL, LVCMOS	I	E11	**Digital Local Loopback** The digital local loopback mode interconnects the 16-bit parallel transmit data and parallel transmit clock input to the 16-bit parallel receive data and parallel receive clock output respectively while maintaining the transmit serial data output. If digital local loopback is enabled, the receive serial data input is ignored. "Low" = Digital Local Loopback Mode Enabled "High" = Disabled This pin is provided with an internal pull-up.
LOOPTM_NOJA / SDI	LVTTL, LVCMOS	I	C10	**Loop Timing Mode With No Jitter Attenuation** **Hardware Mode** When the loop timing mode is activated, the external local reference clock input to the CMU is replaced with the 1/16th of the high-speed recovered receive clock coming from the CDR. "Low" = Disabled "High" = Loop timing Activated This pin is provided with an internal pull-down. **Host Mode** This pin is functions as the microprocessor Serial Data Input.

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
TXDI0P TXDI0N TXDI1P TXDI1N TXDI2P TXDI2N TXDI3P TXDI3N TXDI4P TXDI4N TXDI5P TXDI5N TXDI6P TXDI6N TXDI7P TXDI7N TXDI8P TXDI8N TXDI9P TXDI9N TXDI10P TXDI10N TXDI11P TXDI11N TXDI12P TXDI12N TXDI13P TXDI13N TXDI14P TXDI14N TXDI15P TXDI15N	LVDS, LVPECL Diff and SE	I	P14 P13 N10 N9 N13 N12 M11 M10 M14 M13 L10 L9 L13 L12 K12 K11 J14 K14 J10 K10 J13 J12 H9 J9 H12 H11 G11 G10 F12 G12 G8 G7	**Transmit Parallel Data Input** The 155.52 Mbps 16-bit parallel transmit data input should be applied to the transmit parallel bus simultaneously to be sampled at the rising edge of the TXPCLKIP/N input. The 16-bit parallel interface is multiplexed into the transmit serial output interface, MSB first (TXDI15P/N). TXDI[15:0]P/N 100 Ω internal termination is controlled by INTERM pin or register bit. Inputs are internally biased to VDD_IO - 1V for AC coupled applications. For LVPECL Single-Ended applications, either a 100K VBB bias reference must be provided or the SE_REF pin can also be used to bias and connected all the negative polarity "N" pins. ***NOTE:*** *The XRT91L82 can accept 166.63 Mbps 16-bit parallel transmit data input for Forward Error Correction (FEC) Applications.*
TXOP TXON	CMLDIFF	O	A6 A5	**Transmit Serial Data Output** The transmit serial data output stream is generated by multiplexing the 16-bit parallel transmit data input into a 2.488 Gbps serial data output stream. In Forward Error Correction, the transmit serial data output stream is 2.666 Gbps.
TXSWING / $\overline{\text{INT}}$	LVTTL, LVCMOS	I/O	D10	**Transmit Serial CML Output Swing Mode** **Hardware Mode** Selects the generated transmit serial CML Output swing to the optical module. "Low" = Low Swing CML Mode "High" = High Swing CML Mode This pin is provided with an internal pull-up. **Host Mode** This pin is functions as the microprocessor Interrupt Output. ***NOTE:*** *This pin becomes an open drain output in Host Mode and requires an external pull-up resistor.*

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
TXSCLKOP TXSCLKON	CMLDIFF	O	A9 A8	**2.488/2.666 GHz Transmit Serial Clock Output** A high-speed 2.488/2.666 GHz Transmit serial clock output that can be used to retime TXOP/N.
TXSCLKOOFF / $\overline{CS}$	LVTTL, LVCMOS	I	C9	**2.488/2.666 GHz Hi-speed Serial Clock Output Tristate** **Hardware Mode** Tristates TXSCLKOP/N output and reduces power consumption. "Low" = TXSCLKOP/N output Enabled "High" = Tristates TXSCLKOP/N output This pin is provided with an internal pull-up. **Host Mode** This pin is functions as the microprocessor Chip Select Input.
INTERM / VCXO_IN	LVTTL, LVCMOS / SE- LVCMOS	I	E4	**Transmit Parallel Bus Input Internal Termination** **Hardware Mode** Provides 100Ω line-to-line internal termination to TXDI[15:0]P/N and TXPCLKIP/N. "Low" = Disabled "High" = TXDI[15:0]P/N and TXPCLKIP/N internally terminated. This pin is provided with an internal pull-down. **Host Mode - Voltage Controled 77.76/83.31 MHz or 155.52/166.63 MHz External Oscillator Input** This 77.76/83.31 MHz or 155.52/166.63 MHz Single-Ended LVCMOS clock input is used for the transmit PLL jitter attenuation. ALTFREQSEL register bit determines the value used as the reference. Software register bit VCXOSEL allows the selection of the De-Jitter VCXO Mode. See ALTFREQSEL and VCXO_SEL software register bit description for more details.
TXPCLKIP TXPCLKIN	LVDS, LVPECL Diff and SE	I	P11 P10	**Transmit Parallel Clock Input** 155.52 MHz clock input used to sample the 16-bit parallel transmit data input TXDI[15:0]P/N. TXPCLKIP/N 100 Ω internal termination is controlled by INTERM pin or register bit. TXPCLKIP/N inputs are internally biased to VDD_IO - 1V for AC coupled application. ***NOTE:*** *The XRT91L82 can accept a 166.63 MHz transmit clock input for Forward Error Correction (FEC) Applications.*
TXPCLKOP TXPCLKON	LVDS, LVPECL Diff and SE	O	P8 P7	**Transmit Parallel Clock Output** This 155.52 MHz clock can be used for the downstream device to generate the TXDI[15:0]P/N data and TXPCLKIP/N clock input. This enables the downstream device and the STS-48 transceiver to be in synchronization. ***NOTE:*** *The XRT91L82 can output a 166.63 MHz transmit clock output for Forward Error Correction (FEC).*

TRANSMITTER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
TXCLKO16P TXCLKO16N	LVDS, LVPECL Diff and SE	O	P2 P1	**Auxiliary Clock Output (155.52/19.44 MHz)** 155.52 or 19.44 MHz auxiliary clock derived from CMU output. This clock can also be used for the downstream device as a reference for generating the TXDI[15:0]P/N data and TXPCLKIP/N clock input. This enables the downstream device and the STS-48 transceiver to be in synchronization. The frequency output of this pin is controlled by TXCLKO16SEL. ***NOTE:*** *This pin can output a 166.63/20.83 MHz transmit clock output for Forward Error Correction (FEC).*
TXCLKO16SEL	LVTTL, LVCMOS	I	C4	**Auxiliary Clock Output Select** This pin is used to select the auxiliary clock output. "Low" = TXCLKO16P/N outputs 155.52/ 166.63 MHz "High" = TXCLKO16P/N outputs 19.44/ 20.83 MHz This pin is provided with an internal pull-down.
LOCKDET_CMU	LVCMOS	O	C6	**CMU Lock Detect** This pin is used to monitor the lock condition of the clock multiplier unit. "Low" = CMU Out of Lock "High" = CMU Locked
OVERFLOW	LVCMOS	O	D6	**Transmit FIFO Overflow** This pin is used to monitor the transmit FIFO status. "Low" = Normal Status "High" = Overflow Condition
FIFO_RST	LVTTL, LVCMOS	I	D5	**FIFO Control Reset** FIFO_RST should be held "High" for a minimum of 2 TXPCLKOP/N cycles after powering up and during manual FIFO reset. After the FIFO_RST pin is returned "Low," it will take 8 to 10 TXPCLKOP/N cycles for the FIFO to flush out. Upon an interrupt indication that the FIFO has an overflow condition, this pin is used to reset or flush out the FIFO. "Low" = Normal Operation "High" = Manual FIFO Reset This pin is provided with an internal pull-down. ***NOTES:*** **1.** ***In Hardware Mode****, to automatically reset the FIFO, tie the OVERFLOW output pin to the FIFO_RST input pin or if desired, an asynchronous FIFO reset pin and the OVERFLOW output pin can be logically 'OR'ed and the output tied to the FIFO_RST input pin.* **2.** ***In Host Mode****, this pin is disabled and not used. FIFO_RST is asserted through Microprocessor Control Register 0x03H Bit-D0. A FIFO_AUTORST bit is also available on Microprocessor Control Register 0x03H Bit-D1.*

RECEIVER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
RXDO0P RXDO0N RXDO1P RXDO1N RXDO2P RXDO2N RXDO3P RXDO3N RXDO4P RXDO4N RXDO5P RXDO5N RXDO6P RXDO6N RXDO7P RXDO7N RXDO8P RXDO8N RXDO9P RXDO9N RXDO10P RXDO10N RXDO11P RXDO11N RXDO12P RXDO12N RXDO13P RXDO13N RXDO14P RXDO14N RXDO15P RXDO15N	LVDS, LVPECL Diff and SE	O	G5 G4 H4 H3 H7 H6 H8 J8 J3 J2 J6 J5 K2 K1 K5 K4 K8 K7 L3 L2 L6 L5 L8 M8 M2 M1 M5 M4 M7 N7 N6 N5	**Receive Parallel Data Output** 155.52 Mbps 16-bit parallel receive data output is updated simultaneously on the falling edge of the RXPCLKOP/N output. The 16-bit parallel interface is de-multiplexed from the receive serial data input, MSB first (RXDO15P/N). For LVPECL Single-Ended applications, all the negative polarity "N" pins should not be connected. ***NOTE:*** *The XRT91L82 can output 166.63 Mbps 16-bit parallel receive data output for Forward Error Correction (FEC) Applications.*
RXIP RXIN	CMLDIFF	I	A2 A3	**Receive Serial Data Input** The receive serial data stream of 2.488 Gbps is applied to these input pins. In Forward Error Correction, the receive serial data stream is 2.666 Gbps. This pin is internally biased and terminated.
RXPCLKOP RXPCLKON	LVDS, LVPECL Diff and SE	O	P5 P4	**Receive Parallel Clock Output** 155.52 MHz parallel clock output used to update the 16-bit parallel receive data output RXDO[15:0]P/N at the falling edge of this clock. ***NOTE:*** *The XRT91L82 can output a 166.63 MHz receive clock output for Forward Error Correction (FEC).*

RECEIVER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
$\overline{\text{CDRLCKREF}}$	LVTTL, LVCMOS	I	C12	**CDR's Recovered High-speed Serial Clock Reference** Controls CDR's operation. "Low" = Forced to lock to CDR PLL reference training clock "High" = Normal Operation (Locked to incoming serial data) This pin is provided with an internal pull-up.
$\overline{\text{DISRD}}$ /PRBS_LOCK	LVTTL, LVCMOS	I/O	D4	**Receive Parallel Data Output Disable** **Hardware Mode** If this pin is set to "0", the 16-bit parallel receive data output will asynchronously mute. "Low" = Forces RXDO[15:0]P/N to a logic state of "0" "High" = Normal Mode This pin is provided with an internal pull-up. **Host Mode 2^{23}-1 PRBS Pattern Lock Output Indicator** This pin indicates the current state condition of the PRBS pattern analyzer when the PRBS pattern generator is enabled. "Low" = PRBS pattern analyzer currently Out of Lock "High" = PRBS pattern analyzer currently Locked
$\overline{\text{DISRDCLK}}$	LVTTL, LVCMOS	I	D11	**Receive Parallel Clock Output Disable** This pin is used to asynchronously control the activity of the parallel receive clock output. "Low" = Forces RXPCLKOP/N to a logic state of "0" "High" = Normal Mode This pin is provided with an internal pull-up.
LOCKDET_CDR	LVCMOS	O	C5	**CDR Lock Detect** This pin is used to monitor the lock condition of the clock and data recovery unit. "Low" = CDR Out of Lock "High" = CDR Locked
SDEXT	LVTTL, LVCMOS	I	C2	**Signal Detect Input from Optical Module** When inactive, it will automatically mute received data output bus RXDO[15:0]P/N upon Loss of Signal Detection (LOSD) condition. "Active" = Normal Operation (SDEXT detects signal presence) "Inactive" =Mutes upon LOSD (SDEXT detects signal absence) This pin is provided with an internal pull-up.
POLARITY	LVTTL, LVCMOS	I	E10	**Polarity for SDEXT Input** Controls the Signal Detect polarity convention of SDEXT. "Low" = SDEXT is active "Low" "High" = SDEXT is active "High" This pin is provided with an internal pull-up.

RECEIVER SECTION

NAME	LEVEL	TYPE	PIN	DESCRIPTION
RXCAP1P	Analog	I	E1	**External Receive Loop Filter** **Hardware Mode** This pin is required for the external loop filter capacitor and resistors. See Figure 5 on page 19. **Host Mode - No Connect** This pin is not connected in Host Mode.
RXCAP1N / CP_OUT	Analog	I/O	F1	**External Receive Loop Filter** **Hardware Mode** This pin is required for the external loop filter capacitor and resistors. See Figure 5 on page 19. **Host Mode - Charge Pump Output (for external VCXO)** The nominal output of the charge pump current is 250µA.

POWER AND GROUND

NAME	TYPE	PIN	DESCRIPTION
AVDD_RX	PWR	C1, D2, G2, H1	**Analog 1.8V Receiver Power Supply** AVDD_RX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD_RX power supply pins should have bypass capacitors to the nearest ground.
AVDD_TX	PWR	C14, D13, G13, H14	**Analog 1.8V Transmitter Power Supply** AVDD_TX should be isolated from the digital power supplies. For best results, use a ferrite bead along with an internal power plane separation. The AVDD_TX power supply pins should have bypass capacitors to the nearest ground.
VDD_CML	PWR	A4, A7, A10, A12, B3, B5, B7, B9, C11, C13	**CML 1.8V Power Supply** These pins require a 1.8V potential.
VDD_CMOS	PWR	E6, E8, F3, F5, F7, F9, J4, J7, M6, M9, M12	**Digital 1.8V Power Supply** VDD_CMOS should be isolated from the analog power supplies. For best results, use a ferrite bead along with an internal power plane separation. The VDD_CMOS power supply pins should have bypass capacitors to the nearest ground.
VDD_IO	PWR	G3, G9, J1, J11, K3, K6, K9, K13, M3, N1, N4, N11, N14	**3.3V LVPECL/ 3.3V LVDS Input /Output Bus Power Supply and 3.3V Digital I/O Power Supply** These pins require a 3.3V potential in LVPECL or LVDS operation. These pins also power the 3.3V Digital I/O Power Supply.
GND	GND	A1, A14, B1, B2, B4, B6, B8, B10, B12, B14, D1, D14, E2, E7, E13, F2, F4, F6, F8, F10, F13, G1, G6, G14, H2, H5, H10, H13, L1, L4, L11, L14, N8, P3, P6, P9, P12	**Ground for 3.3V / 1.8V Digital Power Supplies** It is recommended that all ground pins of this device be tied together.

NOTE: *For VDD_{IO}=3.3V, all input control pins are LVCMOS and LVTTL compatible. All output control pins are LVCMOS compatible only.*

SERIAL MICROPROCESSOR INTERFACE

NAME	LEVEL	TYPE	PIN	DESCRIPTION
HOST/$\overline{HW}$	LVTTL, LVCMOS	I	N2	**Host or Hardware Mode Select Input** The XRT91L82 offers two modes of operation for interfacing to the device. The Host mode uses a serial microprocessor interface for programming individual registers. The Hardware mode is controlled by the state of the hardware pins set by the user. When left unconnected, by default, the device is configured in the Hardware mode. "Low" = Hardware Mode "High" = Host Mode This pin is provided with an internal pull-down.
TXSCLKOOFF / $\overline{CS}$	LVTTL, LVCMOS	I	C9	**Chip Select Input (Host Mode Only)** Active "Low" signal. This signal enables the serial microprocessor interface by pulling chip select "Low". The serial microprocessor is disabled when the chip select signal returns "High". ***NOTES:*** **1.** *The serial microprocessor interface does **not** support burst mode. Chip Select must be de-asserted after each operation cycle.* **2.** *Chip Select is only active in Host Mode.* This pin is provided with an internal pull-up.
REFREQSEL1 / SCLK	LVTTL, LVCMOS	I	D12	**Serial Clock Input (Host Mode Only)** Once $\overline{CS}$ is pulled "Low", the serial microprocessor interface requires 16 clock cycles for a complete Read or Write operation. Serial Clock Input is only active in Host Mode. This pin is provided with an internal pull-down.
LOOPTM_NOJA / SDI	LVTTL, LVCMOS	I	C10	**Serial Data Input (Host Mode Only)** When $\overline{CS}$ is pulled "Low", the serial data input is sampled on the rising edge of SCLK. Serial Data Input is only active in Host Mode. This pin is provided with an internal pull-down.
PRBS_ERR / SDO	LVCMOS	O	E9	**Serial Data Output (Host Mode Only)** If a Read function is initiated, the serial data output is updated on the falling edge of SCLK8 through SCLK15, with the LSB (D0) updated first. This enables the data to be sampled on the rising edge of SCLK9 through SCLK16. Serial Data Output is only active in Host Mode.
TXSWING / $\overline{INT}$	LVCMOS	O	D10	**Interrupt Output (Host Mode Only)** Active "Low" signal. This signal is asserted "Low" when a change in alarm status occurs. Once the status registers have been read, the interrupt pin will return "High". Interrupt Output is only active in Host Mode. ***NOTE:*** *This pin is an open drain output and requires an external pull-up resistor.*

JTAG

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TCK	C7	I	**Test clock:** Boundary Scan Clock Input. This pin is provided with an internal pull-down.
TMS	D8	I	**Test Mode Select:** Boundary Scan Mode Select Input. JTAG is disabled by default. ***Note**: This input pin should be pulled "Low" for JTAG operation* This pin is provided with an internal pull-up.
TDI	C8	I	**Test Data In:** Boundary Scan Test Data Input This pin is provided with an internal pull-up.
TDO	D7	O	**Test Data Out:** Boundary Scan Test Data Output
TRST	N3	I	**JTAG Test Reset Input** ***Note**: This input pin should be pulled "Low" to reset JTAG* This pin is provided with an internal pull-up.

NO CONNECTS

NAME	LEVEL	TYPE	PIN	DESCRIPTION
None	N/A	N/A	None	**No Connect** This pin can be left floating or tied to ground.

1.0 FUNCTIONAL DESCRIPTION

The XRT91L82 Transceiver is designed to operate with a SONET Framer/ASIC device and provide a high-speed serial interface to optical networks. The Transceiver converts 16-bit parallel data at 155.52/166.63 MHz to a serial CML bit stream at 2.488/2.666 Gbps and vice-versa. It implements a clock multiplier unit (CMU), SONET/SDH serialization/de-serialization (SerDes), and receive clock and data recovery (CDR) unit. The Transceiver is divided into Transmit and Receive sections and is used to provide the front end component of SONET equipment, which includes primarily serial transmit and receive functions.

1.1 Hardware Mode vs. Host Mode

Functionality of the STS-48/STM-16 Transceiver can be configured by using either Host mode or Hardware mode. Hardware mode is selected by pulling HOST/$\overline{HW}$ "Low" or leaving this pin unconnected. The transceiver functionality is then controlled by the hardware pins described in the Hardware Pin Descriptions. However, if Host mode is selected by pulling HOST/$\overline{HW}$ "High", the functionality is controlled by programming internal R/W registers using the Serial Microprocessor interface. Whether using Host or Hardware mode, the functionality remains the same. Therefore, the following sections describe the functionality rather than how each function is controlled. The Hardware Pin Descriptions and the Register Bit Descriptions concentrate on configuring the device.

1.2 Clock Input Reference

The XRT91L82 can accept both 155.52 MHz non-FEC or 166.63 MHz FEC clock input at REF1CLKP/N and/or REF2CLKP/N as its internal timing reference for generating higher speed clocks. The reference clock can be provided with one of two frequencies chosen by REFREQSEL[1:0]. The reference frequency options for the XRT91L82 are listed in Table 1.

TABLE 1: REFERENCE FREQUENCY OPTIONS (NORMAL MODE/ FEC RATE)

REFREQSEL [1:0]	CMU REFERENCE CLOCK FREQUENCY	CDR REFERENCE CLOCK FREQUENCY	REF1CLK CLOCK FREQUENCY	REF2CLK CLOCK FREQUENCY	TRANSMIT DATA RATE	RECEIVE DATA RATE
00	REF1CLK	REF1CLK	155.52 MHz non-FEC	not used	2.488 Gbps non-FEC	2.488 Gbps non-FEC
01	REF1CLK	REF2CLK	155.52 MHz non-FEC	166.63 MHz FEC	2.488 Gbps non-FEC	2.666 Gbps FEC
10	REF2CLK	REF1CLK	155.52 MHz non-FEC	166.63 MHz FEC	2.666 Gbps FEC	2.488 Gbps non-FEC
11	REF2CLK	REF2CLK	not used	166.63 MHz FEC	2.666 Gbps FEC	2.666 Gbps FEC

1.3 Alternate Clock Input Reference (Host Mode Only)

In Host mode, the XRT91L82 has the option to accept a lower reference frequency of 77.76 MHz non-FEC or 83.31 MHz FEC clock input at REF1CLKP/N and/or REF2CLKP/N. To use this feature, register bit ALTFREQSEL must be set "Low" on bit- D5 of "Configuration Control Register (0x07h)". The alternate reference frequency options are listed below in Table 2.

TABLE 2: ALTERNATE REFERENCE FREQUENCY OPTIONS (NORMAL MODE/ FEC RATE)

REFREQSEL [1:0]	CMU REFERENCE CLOCK FREQUENCY	CDR REFERENCE CLOCK FREQUENCY	REF1CLK CLOCK FREQUENCY	REF2CLK CLOCK FREQUENCY	TRANSMIT DATA RATE	RECEIVE DATA RATE
00	REF1CLK	REF1CLK	77.76 MHz non-FEC	not used	2.488 Gbps non-FEC	2.488 Gbps non-FEC
01	REF1CLK	REF2CLK	77.76 MHz non-FEC	83.31 MHz FEC	2.488 Gbps non-FEC	2.666 Gbps FEC
10	REF2CLK	REF1CLK	77.76 MHz non-FEC	83.31 MHz FEC	2.666 Gbps FEC	2.488 Gbps non-FEC
11	REF2CLK	REF2CLK	not used	83.31 MHz FEC	2.666 Gbps FEC	2.666 Gbps FEC

1.4 Data Latency

Due to different operating modes and data logic paths through the device, there is an associated latency from data ingress to data egress. Table 3 specifies the data latency for a typical path.

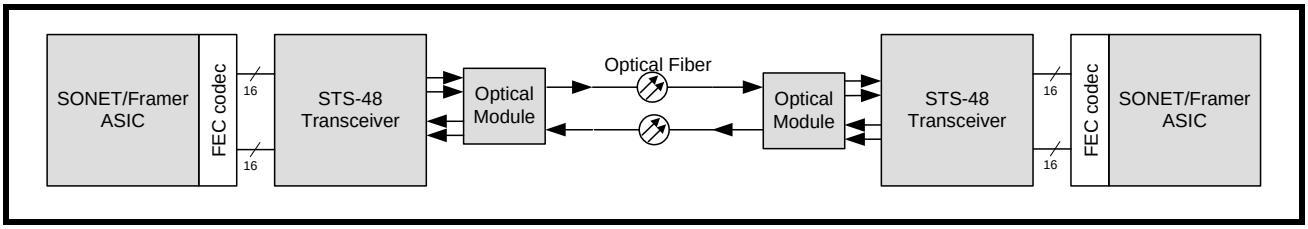
TABLE 3: DATA INGRESS TO DATA EGRESS LATENCY

MODE OF OPERATION	DATA PATH	CLOCK REFERENCE	MAXIMUM REFNCLK CLOCK CYCLES
Thru-mode	Data on TXDI[15:0]P/N to data on TXOP/N	REF1CLKP/N or REF2CLKP/N Clock	18 to 20

1.5 Forward Error Correction (FEC)

Forward Error Correction is used to control errors along a one-way path of communication. FEC sends extra information along with data which can be used by a receiver to check and correct the data without requesting re-transmission of the original information. It does so by introducing a known structure into a data sequence prior to transmission. The most common methods are to replace a 14-bit data packet with a 15-bit codeword structure, or to replace a 17-bit data packet with an 18-bit codeword structure. The XRT91L82 supports FEC by accepting a clock input reference frequency of 83.31 or 166.63 MHz. Both reference frequencies allows the transmit 16-bit parallel data input to be applied to the STS-48 transceiver at 166.63 Mbps which is converted to a 2.666 Gbps serial output stream to an optical module. A simplified block diagram of FEC is shown in Figure 3.

FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF FORWARD ERROR CORRECTION



1.6 PRBS Pattern Generator and Analyzer

The XRT91L82 contains an on-chip Pseudo Random Binary Sequence (PRBS) generator and detector for diagnostic purpose. With the PRBS_EN asserted, the transmitter will send out PRBS pattern of 2^{23}-1 in STS-48/48c or STM-16 rate. At the same time, the receiver PRBS detector is also enabled. Whenever the PRBS detector is not in sync, the PRBS_ERR bit will be set to “1”. To clear the erred condition, PRBSCLR must be toggled "Low." If the correct PRBS pattern is detected by the receiver, then PRBS_ERR pin will go “Low” to indicate PRBS synchronization has been achieved, otherwise PRBS_ERR will remain "1." PRBSCLR shares pin F11 with RLOOPS. Serial Remote Line Loopback (RLOOPS) is disabled when PRBS_EN is enabled.

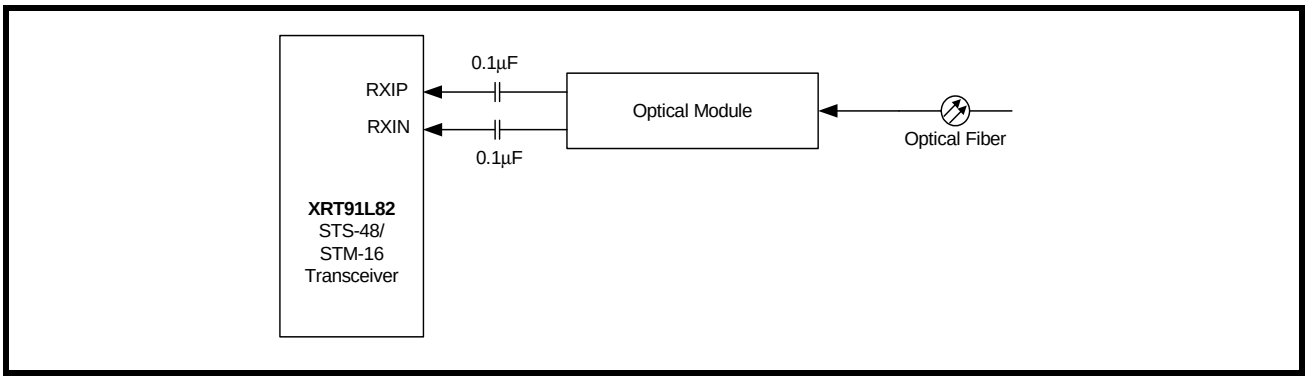
2.0 RECEIVE SECTION

The receive section of XRT91L82 includes the differential inputs RXIP/N, followed by the clock and data recovery unit (CDR) and receive serial-to-parallel converter. The receiver accepts the high-speed Non-Return to Zero (NRZ) serial data at 2.488/2.666 Gbps through the differential input interfaces RXIP/N. The clock and data recovery unit recovers the high-speed receive clock from the incoming scrambled NRZ data stream. The recovered serial data is converted into 16-bit-wide 155.52/166.63 Mbps parallel data and presented to the RXDO[15:0]P/N parallel interface. This parallel interface can be configured for Differential LVPECL/LVDS, or Single-Ended LVPECL operation. A divide-by-16 version of the high-speed recovered clock, RXPCLKOP/N is used to synchronize the transfer of the 16-bit RXDO[15:0]P/N data with the receive portion of the upstream device. Upon initialization or loss of signal or loss of lock the 155.52 MHz or 166.63 MHz external local reference clock is used to start-up the clock recovery phase-locked loop for proper operation. In Host Mode, a special loopback feature can be configured when parallel remote loopback ($\overline{\text{RLOOPP}}$) is used in conjunction with de-jittered loop-time mode that allows the re-transmitted data to comply with ITU and Bellcore jitter generation specifications.

2.1 Receive Serial Input

The receive serial CML inputs are applied to RXIP/N. The receive serial inputs can be AC or DC coupled to an optical module or an electrical interface. A simplified AC coupled block diagram is shown in Figure 4.

FIGURE 4. RECEIVE SERIAL INPUT INTERFACE BLOCK



NOTE: *Some optical modules integrate AC coupled capacitors within the module. If so, the external AC coupled capacitors are not necessary and can be excluded.*

The 2.488/2.666 Gbps high-speed differential CML RXIP/N input swing characteristics is shown in Table 4. Figure 17, “CML Differential Voltage Swing,” on page 29 shows the CML differential voltage swing.

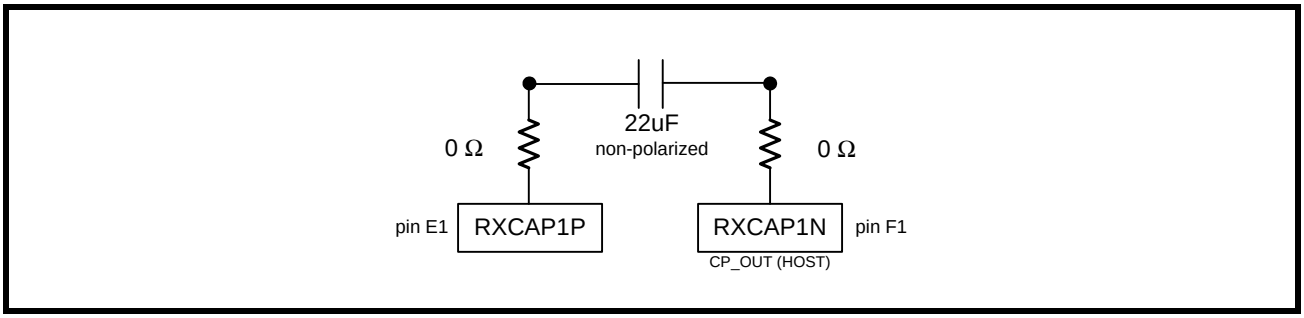
TABLE 4: DIFFERENTIAL CML INPUT SWING PARAMETERS

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
ΔV_{INDIFF}	Differential Input Voltage Swing	100		2000	mV
ΔV_{INSE}	Single-Ended Input Voltage Swing	50		1000	mV
ΔV_{INBIAS}	Input Bias Range (AC Coupled)	VDD_CML - 0.4		VDD_CML - 0.2	V
R_{DIFF}	Differential Input Resistance	80	100	120	Ω

2.2 External Receive Loop Filter Capacitors

These external loop filter 0Ω resistors and 22µF non-polarized capacitor provide the necessary components to achieve the required receiver jitter performance. They must be well isolated to prohibit noise entering the CDR block. Figure 5 shows the pin connections and external loop filter components. The external loop filter is not needed while in host mode and RXCAP1N becomes the charge pump output for the external VCXO.

FIGURE 5. EXTERNAL LOOP FILTER



2.3 Receive Clock and Data Recovery

The clock and data recovery unit accepts the high-speed NRZ serial data from the differential CML receiver and generates a clock that is the same frequency as the incoming data. The clock recovery utilizes REF1CLKP/N and/or REF2CLKP/N to train and monitor its clock recovery PLL. Initially upon startup, the PLL locks to the local reference clock within ±500 ppm. Once this is achieved, the PLL then attempts to lock onto the incoming receive data stream. Whenever the recovered clock frequency deviates from the local reference clock frequency by more than approximately ±500 ppm, the clock recovery PLL will switch and lock back onto the local reference clock. When this condition occurs the PLL will declare Loss of Lock and the LOCKDET_CDR signal will be pulled "Low." Whenever a Loss of Lock/Loss of Signal Detection (LOSD) event occurs, the CDR will continue to supply a receive clock (based on the local reference clock) to the upstream framer device. A Loss of Lock condition will also be declared when the external SDEXT becomes inactive. When the SDEXT is de-asserted by the optical module or when $\overline{\text{DISRD}}$ is asynchronously asserted "Low," receive parallel data output will be forced to a logic zero state for the entire duration that a LOSD condition is detected or for as long as $\overline{\text{DISRD}}$ is asserted "Low." This acts as a receive data mute upon LOSD function to prevent random noise from being misinterpreted as valid incoming data. When the SDEXT becomes active and the recovered clock is determined to be within ±500 ppm accuracy with respect to the local reference source, the clock recovery PLL will switch and lock back onto the incoming receive data stream and the lock detect output (LOCKDET_CDR) will go active. Table 5 specifies the Clock and Data Recovery Unit performance characteristics.

TABLE 5: CLOCK AND DATA RECOVERY UNIT PERFORMANCE

NAME	PARAMETER	MIN	TYP	MAX	UNITS
REF_{DUTY}	Reference clock duty cycle	45		55	%
REF_{TOL}	Reference clock frequency tolerance[1]	-20		+20	ppm
$OCLK_{JIT}$	Clock output jitter generation with 155.52 MHz reference clock		5	7	mUI_{rms}
$OCLK_{JIT}$	Clock output jitter generation with 166.63 MHz reference clock		5	7	mUI_{rms}
TOL_{JIT}	Input jitter tolerance with 1 MHz < f < 20 MHz PRBS pattern	0.4		0.7	UI
$OCLK_{FREQ}$	Frequency output	2.488		2.667	GHz
$OCLK_{DUTY}$	Clock output duty cycle	45		55	%

Jitter specification is defined using a 12kHz to 20MHz appropriate SONET/SDH filter.

[1]Required to meet SONET output frequency stability requirements.

2.4 External Signal Detection

XRT91L82 supports external Signal Detection (SDEXT). The external Signal Detect function is supported by the SDEXT input. This input is coming from the optical module through an output usually called “SD” or “FLAG” which indicates the lack or presence of optical power. Depending on the manufacturer of these devices, the polarity of this signal can be either active "Low" or active "High." The SDEXT and POLARITY inputs are Exclusive OR’ed to generate the internal Loss of Signal Detect (LOSD) declaration and Mute upon LOSD control signal. Whenever an external SD is absent, the XRT91L82 will automatically force the receive parallel data output to a logic state "0" for the entire duration that a LOSD condition is declared as well as update the status registers whenever the host mode serial microprocessor interface feature is active. This acts as a receive data mute upon LOSD function to prevent random noise from being misinterpreted as valid incoming data. Table 6 specifies SDEXT declaration polarity settings.

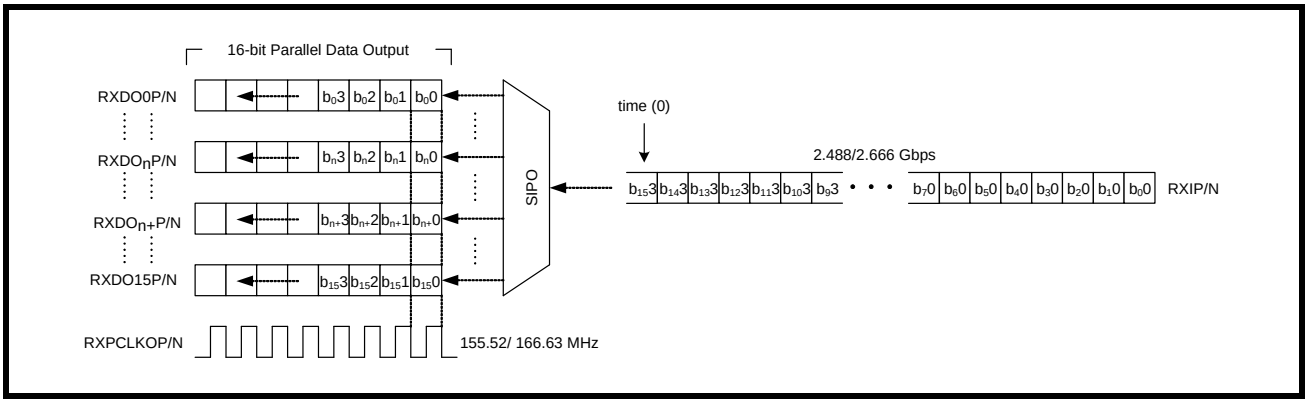
TABLE 6: LOSD DECLARATION POLARITY SETTING

SDEXT	POLARITY	INTERNAL SIGNAL DETECT	RECEIVE PARALLEL DATA OUTPUT RXDO[15:0]P/N	CLOCK AND DATA RECOVERY PLL REFERENCE LOCK
0	**0**	Active Low. Optical signal presence indicated by SDEXT logic 0 input from optical module. **LOSD not declared.**	Not Muted	Hi-Spd Received Data
0	**1**	Active High. Optical signal presence indicated by SDEXT logic 1 input from optical module. **LOSD declared.**	Muted	Local Reference Clock
1	**0**	Active Low. Optical signal presence indicated by SDEXT logic 0 input from optical module. **LOSD declared.**	Muted	Local Reference Clock
1	**1**	Active High. Optical signal presence indicated by SDEXT logic 1 input from optical module. **LOSD not declared.**	Not Muted	Hi-Spd Received Data

2.5 Receive Serial Input to Parallel Output (SIPO)

The SIPO is used to convert the 2.488/2.666 Gbps serial data input to 155.52/166.63 Mbps parallel data output which can interface to a SONET Framer/ASIC. The SIPO bit de-interleaves the serial data input into a 16-bit parallel output to RXDO[15:0]P/N. A simplified block diagram is shown in Figure 6.

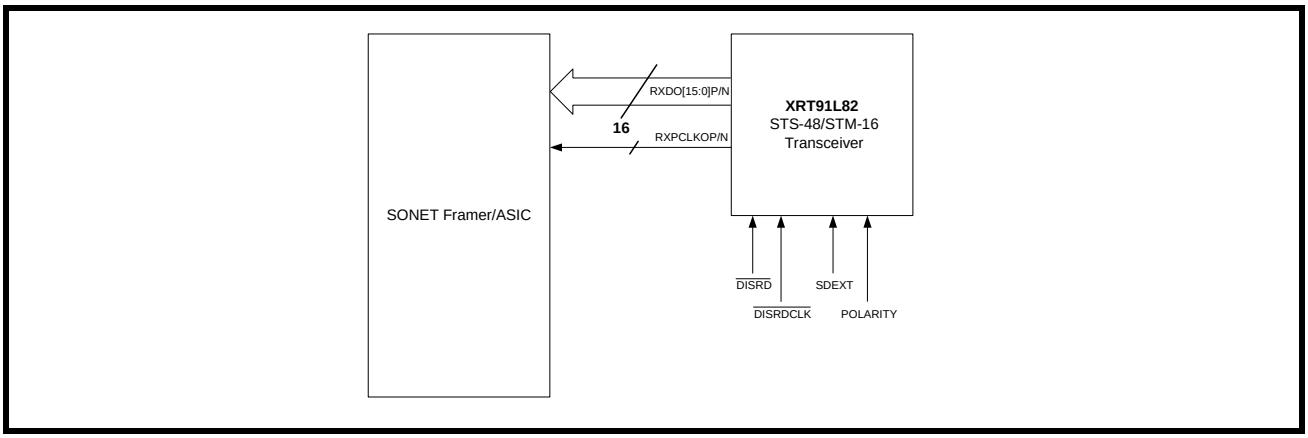
FIGURE 6. SIMPLIFIED BLOCK DIAGRAM OF SIPO



2.6 Receive Parallel Output Interface

The 16-bit LVDS, Differential LVPECL or Single-Ended LVPECL 155.52/166.63 Mbps parallel data output of the receive path is used to interface to a SONET Framer/ASIC synchronized to the recovered clock. A simplified block diagram is shown in Figure 7.

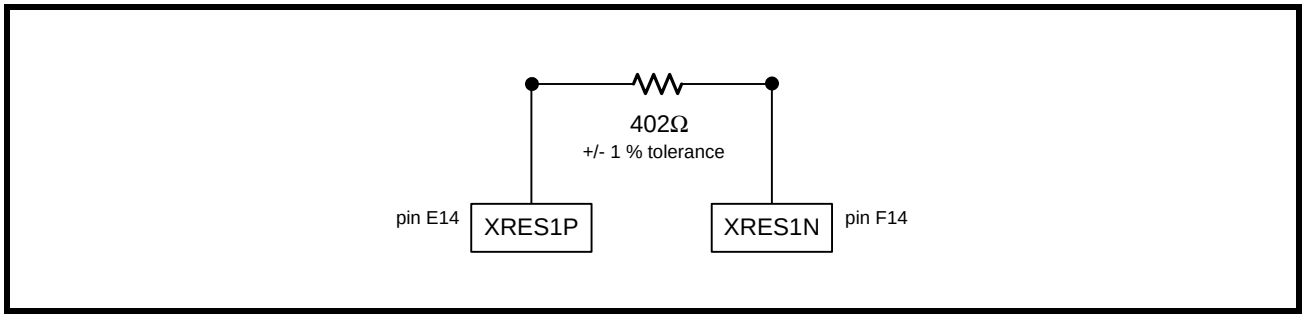
FIGURE 7. RECEIVE PARALLEL OUTPUT INTERFACE BLOCK



2.7 Receive Parallel Interface LVDS Operation

When operating the 16-bit Differential bus in LVDS mode, a 402Ω external resistor is needed across XRES1P and XRES1N to properly bias the RXDO[15:0]P/N and RXPCLKOP/N pins. Figure 8 shows the proper biasing resistor installed.

FIGURE 8. LVDS EXTERNAL BIASING RESISTORS



2.8 Parallel Receive Data Output Disable/Mute Upon LOSD

The parallel receiver data outputs are automatically pulled "Low" during a LOSD condition to prevent data chattering. However, the user must select the proper SDEXT polarity for the optical module used. In addition, by pulling $\overline{\text{DISRD}}$ "Low", the receiver data outputs will be muted asynchronously or forced to a logic state of "0" regardless of the data input stream.

2.9 Parallel Receive Clock Output Disable

Like $\overline{\text{DISRD}}$, $\overline{\text{DISRDCLK}}$ is used to mute the parallel receiver clock output RXPCLKOP/N regardless of the data input stream. By pulling $\overline{\text{DISRDCLK}}$ "Low", the receiver clock output will be asynchronously muted whenever desired.

2.10 Receive Parallel Data Output Timing

The receive parallel data output from the STS-48/STM-16 receiver will adhere to the setup and hold times shown in Figure 9 and Table 7.

FIGURE 9. RECEIVE PARALLEL OUTPUT TIMING

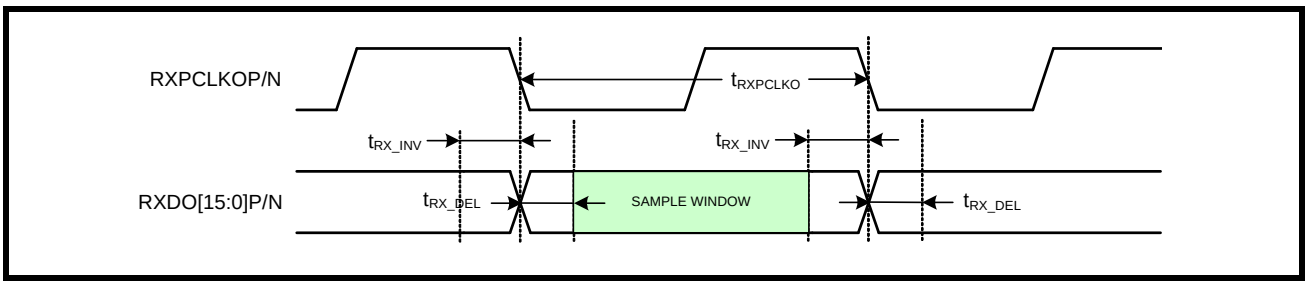


TABLE 7: RECEIVE PARALLEL DATA AND CLOCK OUTPUT TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
$t_{RXPCLKO}$	Receive parallel clock output period (155.52 MHz non-FEC rate)		6.43		ns
$t_{RXPCLKO}$	Receive parallel clock output period (166.63 MHz FEC rate)		6.00		ns
t_{RX_INV}	RXPCLKOP/N "Low" to data invalid window			1000	ps
t_{RX_DEL}	RXPCLKOP/N "Low" to data delay			900	ps
RX_{DUTY}	RXPCLKOP/N Duty Cycle	45		55	%

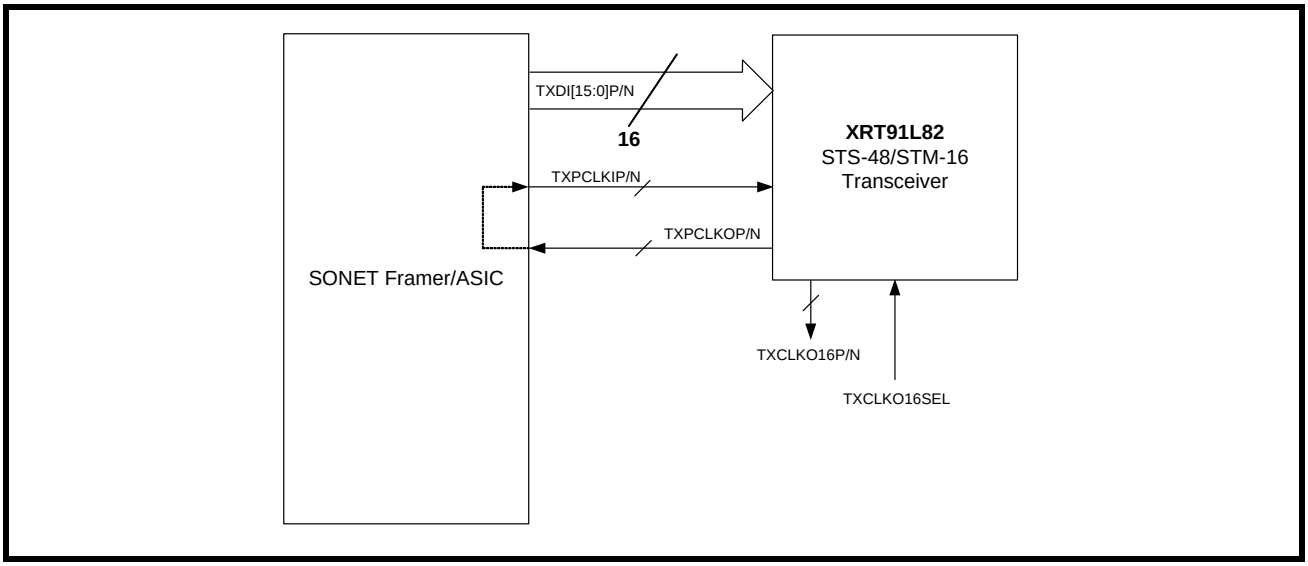
3.0 TRANSMIT SECTION

The transmit section of the XRT91L82 accepts 16-bit parallel data and converts it to serial CML data output intented to interface to an optical module. It consists of a 16-bit parallel Differential LVPECL/LVDS, or Single-Ended LVPECL interface, a 16x9 FIFO, Parallel-to-Serial Converter, a clock multiplier unit (CMU), a Current Mode Logic (CML) differential line driver, and Loop Timing modes. The CML serial data output rate is 2.488/ 2.666 Gbps for STS-48 applications. The high frequency serial clock is synthesized by a PLL, which uses a low frequency clock as its input reference. In order to synchronize the data transfer process, the synthesized 2.488/2.666 GHz serial clock output is divided by sixteen and the 155.52/166.63 MHz clock is presented to the upstream device to be used as its timing source.

3.1 Transmit Parallel Interface

The parallel data from an upstream device is presented to the XRT91L82 through a 16-bit Differential LVPECL/ LVDS/Single-Ended LVPECL parallel bus interface TXDI[15:0]P/N. The data is latched into a parallel input register on the rising edge of TXPCLKIP/N. If the SONET Framer/ASIC is synchronized to the same timing source as the XRT91L82, the transmit data and clock input can directly interface to the STS-48/STM-16 transceiver. However, if the SONET Framer/ASIC is synchronized to a separate crystal, the XRT91L82 has two clock output references that can be used to synchronize the SONET Framer/ASIC. TXPCLKOP/N is a 155.52/166.63 MHz Differential LVPECL/LVDS or Single-Ended LVPECL clock output source that is derived from the CMU synthesized clock. TXCLKO16P/N is a 155.52/166.63 MHz or 19.44/20.83 MHz Differential LVPECL/LVDS or Single-Ended LVPECL auxiliary clock output source that is also derived from the CMU sythensized clock. Either of these two clock output sources can be used to synchronize the SONET Framer/ ASIC to the XRT91L82. A simplified block diagram of the parallel interface is shown in Figure 10.

FIGURE 10. TRANSMIT PARALLEL INPUT INTERFACE BLOCK



3.2 Transmit Parallel Data Input Timing

When applying parallel data input to the transmitter, the setup and hold times should be followed as shown in Figure 11 and Table 8. Table 9 shows the parameters for TXPCLKOP/N clock output.

FIGURE 11. TRANSMIT PARALLEL INPUT TIMING

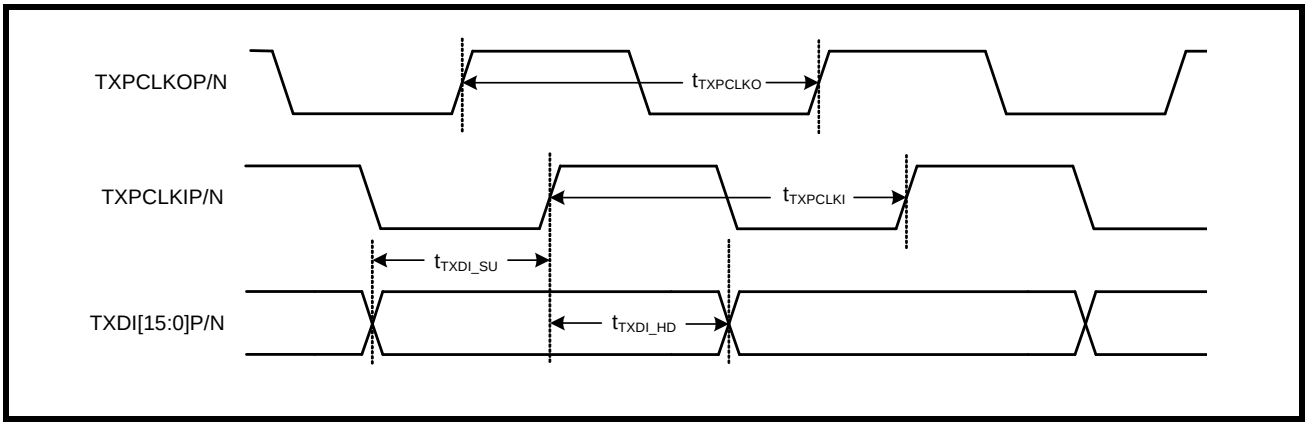


TABLE 8: TRANSMIT PARALLEL DATA AND CLOCK INPUT TIMING SPECIFICATION

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
$t_{TXPCLKI}$	Transmit parallel clock input period (155.52 MHz non-FEC rate)		6.43		ns
$t_{TXPCLKI}$	Transmit parallel clock input period (166.63 MHz FEC rate)		6.00		ns
t_{TXDI_SU}	TXPCLKIP/N "High" to data setup time	1000			ps
t_{TXDI_HD}	TXPCLKIP/N "High" to data hold time	500			ps
TX_{DUTY}	TXPCLKIP/N Duty Cycle	40		60	%

TABLE 9: TRANSMIT PARALLEL CLOCK OUTPUT TIMING SPECIFICATION

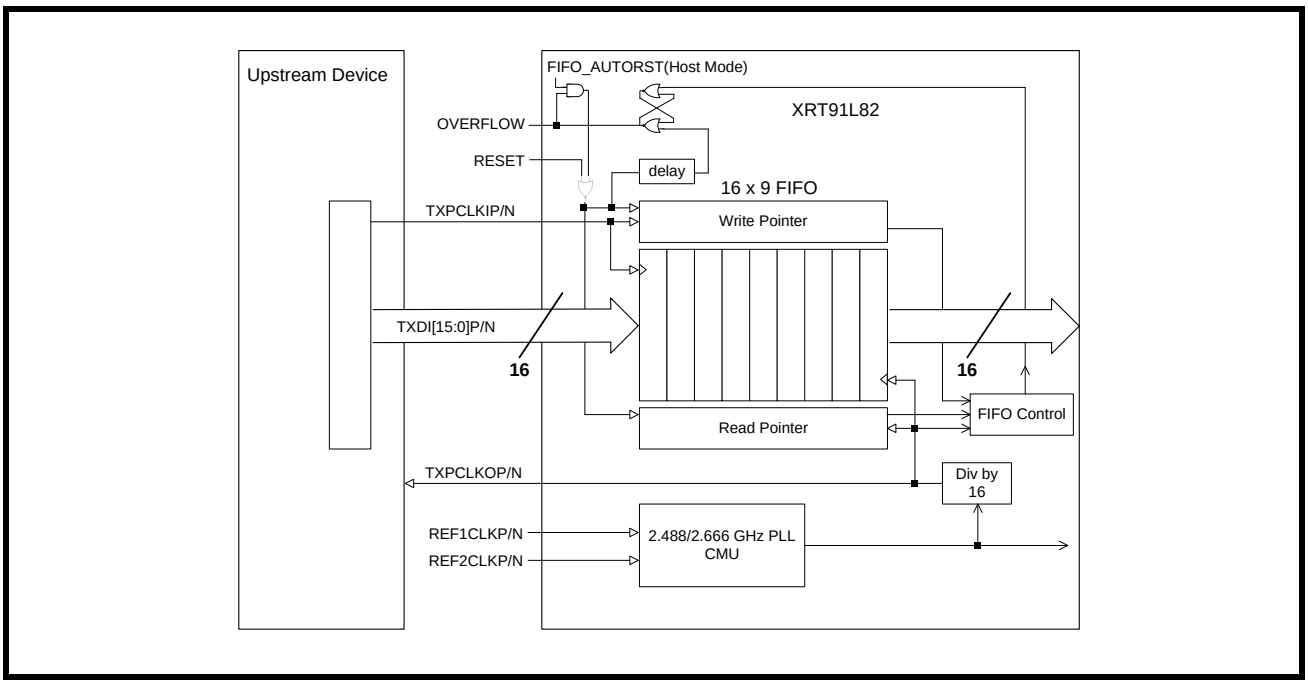
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
$t_{TXPCLKO}$	Transmit parallel clock output period (155.52 MHz non-FEC rate)		6.43		ns
$t_{TXPCLKO}$	Transmit parallel clock output period (166.63 MHz FEC rate)		6.00		ns
TX_{DUTY}	TXPCLKOP/N Duty Cycle	45		55	%

3.3 Transmit FIFO

The Parallel Interface also includes a 16x9 FIFO that can be used to eliminate difficult timing issues between the input transmit clock and the clock derived from the CMU. The use of the FIFO permits the system to tolerate an arbitrary amount of delay and jitter between TXPCLKOP/N and TXPCLKIP/N. The FIFO can be initialized when FIFO_RST is asserted and held "High" for 2 cycles of the TXPCLKOP/N clock. When the FIFO_RST is de-asserted, it will take 8 to 10 TXPCLKOP/N cycles for the FIFO to flush out. Once the FIFO is centered, the delay between TXPCLKOP/N and TXPCLKIP/N can decrease or increase up to two periods of the low-speed clock. Should the delay exceed this amount, the read and write pointers will point to the same word in the FIFO resulting in a loss of transmitted data (FIFO overflow). In the event of a FIFO overflow, the FIFO control logic will initiate an OVERFLOW signal that can be used by an external controller to issue a FIFO RESET signal.

In Host Mode, the transceiver under the control of the FIFO_AUTORST register bit can automatically recover from an overflow condition. When the FIFO_AUTORST register bit is set to a "High" level, once an overflow condition is detected, the chip will set the OVERFLOW pin to a high level and will automatically reset and center the FIFO. Figure 12 provides a detailed overview of the transmit FIFO in a system interface.

FIGURE 12. TRANSMIT FIFO AND SYSTEM INTERFACE



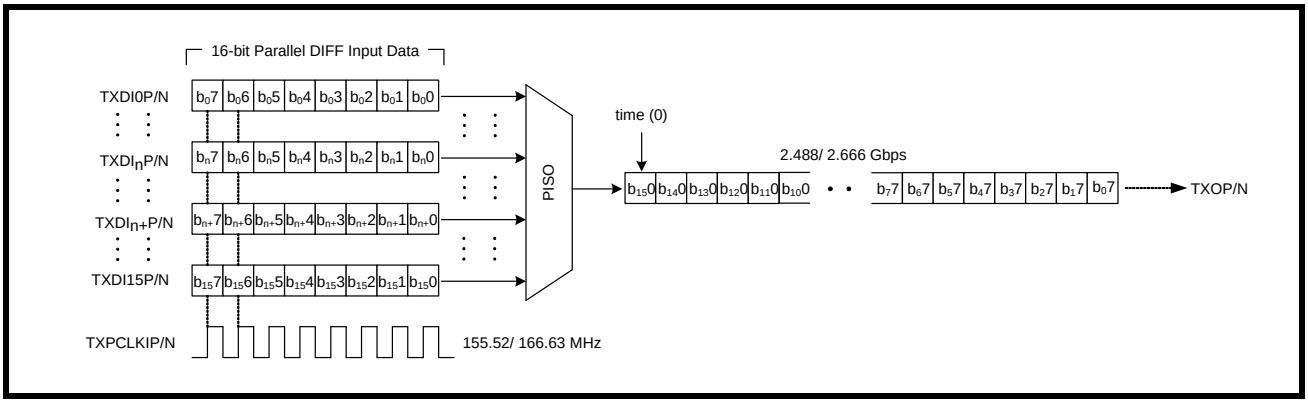
3.4 FIFO Calibration Upon Power Up

It is required that the FIFO_RST pin be pulled "High" for 2 TXPCLKOP/N cycles to flush out the FIFO after the device is powered on. If the FIFO experiences an Overflow condition, FIFO_RST can be used to manually reset the FIFO. In Host Mode, the STS-48 transceiver has an automatic FIFO reset register bit that will allow the FIFO to automatically reset upon an Overflow condition. FIFO_AUTORST register bit should be pulled "High" to enable the automatic FIFO reset function.

3.5 Transmit Parallel Input to Serial Output (PISO)

The PISO is used to convert 155.52/166.63 Mbps parallel data input to 2.488/2.666 Gbps serial data output which can interface to an optical module. The PISO bit interleaves parallel data input into a serial bit stream taking the first bit from TXDI15P/N, then the first bit from TXDI14P/N, and so on as shown in Figure 13.

FIGURE 13. SIMPLIFIED BLOCK DIAGRAM OF PISO



3.6 Clock Multiplier Unit (CMU) and Re-Timer

The high-speed serial clock synthesized by the CMU is divided by 16 and is then presented to the upstream device as TXPCLKOP/N clock. The upstream device should use TXPCLKOP/N as its timing source. The upstream device then generates the TXPCLKIP/N clock that is phase aligned with the transmit data and provides it to the parallel interface of the transmitter. The data must meet setup and hold times with respect to TXPCLKIP/N. The XRT91L82 will latch TXDI[15:0]P/N on the rising edge of TXPCLKIP/N. The clock synthesizer uses a PLL to lock to the differential input reference clock REF1CLKP/N and REF2CLKP/N. REF1CLKP/N and/or REF2CLKP/N input can accept a clock from a Differential LVPECL crystal oscillator that has a frequency accuracy better than 20ppm in order for the TXSCLKOP/N frequency to have the accuracy required for SONET systems. It will then use this reference clock to generate the 2.488/2.666 GHz STS-48/STM-16 serial clock output TXSCLKOP/N and in addition feed this high-speed synthesized clock to the PISO. The Retimer will then align the transmit serial data from the PISO with this 2.488/2.666 GHz synthesized clock to generate the output TXOP/N. Table 10 specifies the Clock Multiplier Unit performance characteristics.

In Host Mode, the clock synthesizer can also be driven by an optional external VCXO for loop timed or local reference de-jitter applications. VCXO_IN can be connected to the output of a VCXO that can be configured to clean up the recovered received clock coming from CP_OUT in loop timing mode before being applied to the input of the transmit CMU as a reference clock. In addition, the internal phase/frequency detector and charge pump, combined with an external VCXO can alternately be used as a jitter attenuator to de-jitter a noisy system reference clock such as REF1CLKP/N or REF2CLKP/N prior to it being used to time the CMU. The following Section 3.7, “Loop Timing and Clock Control,” on page 26 illustrate the use of this method.

TABLE 10: CLOCK MULTIPLIER UNIT PERFORMANCE

NAME	PARAMETER	MIN	TYP	MAX	UNITS
REF_{DUTY}	Reference clock duty cycle	45		55	%
REF_{TOL}	Reference clock frequency tolerance[1]	-20		+20	ppm
REF_{STS48}	Reference clock jitter limits from 12 KHz to 20 MHz			-61	dB_C
$OCLK_{JIT}$	Clock output jitter generation with 155.52 MHz reference clock		3.2	5.0	mUI_{rms}
$OCLK_{JIT}$	Clock output jitter generation with 166.63 MHz reference clock		3.2	5.0	mUI_{rms}
$OCLK_{FREQ}$	Frequency output	2.488		2.667	GHz
$OCLK_{DUTY}$	Clock output duty cycle	45		55	%

Jitter specification is defined using a 12kHz to 20MHz appropriate SONET/SDH filter.

[1]Required to meet SONET output frequency stability requirements.

3.7 Loop Timing and Clock Control

Two types of loop timing are possible in the XRT91L82.

In the Hardware mode, the loop timing (without an external VCXO) is controlled by the LOOPTM_NOJA pin. This mode is selected by asserting the LOOPTM_NOJA signal to a "High" level. When the loop timing mode is activated, the external local reference clock to the input of the CMU is replaced with the 1/16th of the high-speed recovered receive clock coming from the CDR. Under this condition both the transmit and receive sections are synchronized to the recovered receive clock. The normal looptime mode directly locks the CMU to the recovered receive clock with no external de-jittering.

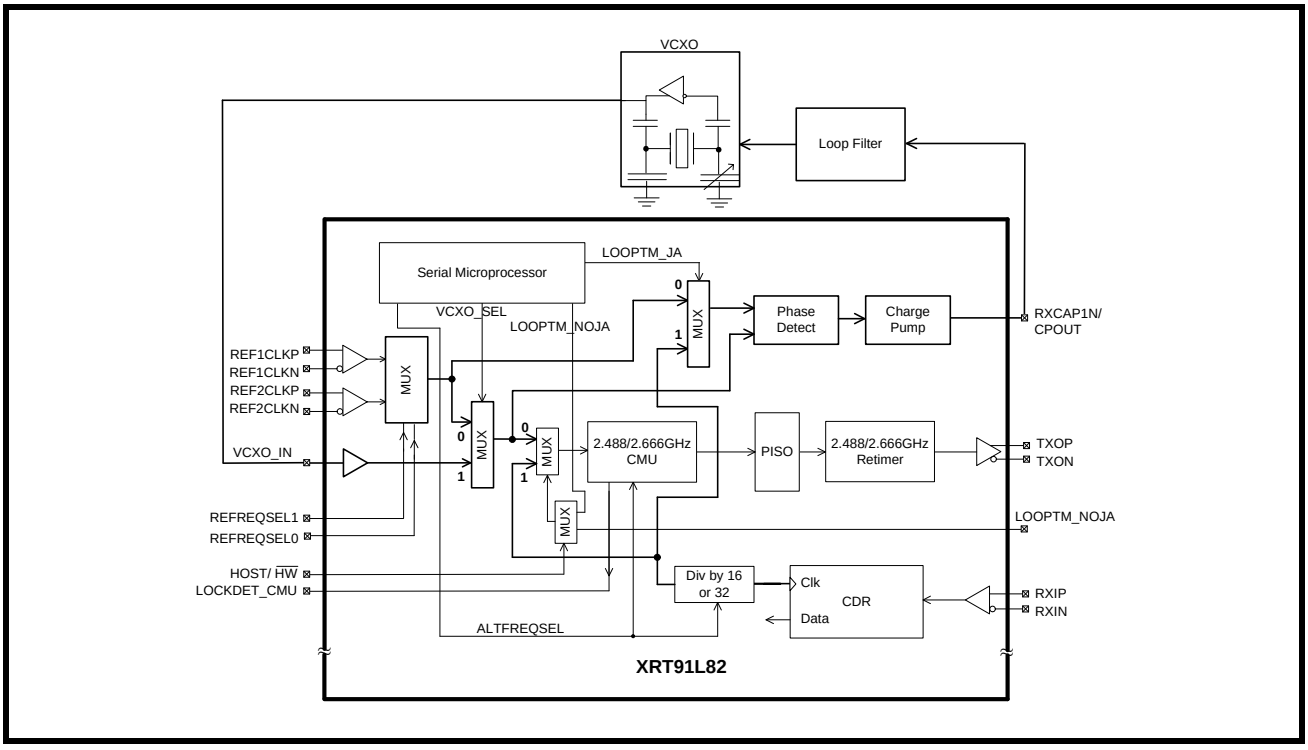
In Host Mode, loop timing performance can be further improved using an external VCXO-based PLL to clean up the jitter of the recovered receive clock. In this case the VCXO_SEL register bit should be set "High." By doing so, the CMU receives its reference clock signal from an external VCXO connected to the VCXO_IN input. The LOOPTM_JA register bit must also be set "High" in order to select the recovered receive clock as the reference source for the de-jitter PLL. In this state, the VCXO will be phase locked to the recovered receive clock through a narrowband loop filter. The use of the on-chip phase/frequency detector with charge pump and an external VCXO to remove the transmit jitter due to jitter in the recovered clock is shown in Figure 14.

The on-chip phase/frequency detector can also be used to remove the jitter from a noisy reference signal that is applied to the REF1CLKP/N or REF2CLKP/N inputs. In this case the LOOPTM_NOJA register bit should be set "Low," the VCXO_SEL set "High," and the LOOPTM_JA register bit set "Low." In this configuration, the REF1CLKP/N or REF2CLKP/N CMU reference signal is used as the reference to the de-jitter PLL and the de-jittered output of the phase locked VCXO is used as the timing reference to the CMU. Table 11 provides configuration for selecting the loop timing and reference de-jitter modes.

TABLE 11: LOOP TIMING AND REFERENCE DE-JITTER CONFIGURATIONS

VCXO_SEL (REGISTER BIT)	LOOPTM_JA (REGISTER BIT)	LOOPTM_NOJA (PIN/REGISTER BIT)	CONFIGURATION	ACTION
0	0	0	HARDWARE AND HOST MODE	Normal mode
0	0	1	HARDWARE AND HOST MODE	Loop timing without de-jitter VCXO
1	0	0	HOST MODE ONLY	REF1CLKP/N or REF2CLKP/N reference de-jitter VCXO
1	1	0	HOST MODE ONLY	Loop timing with de-jitter VCXO

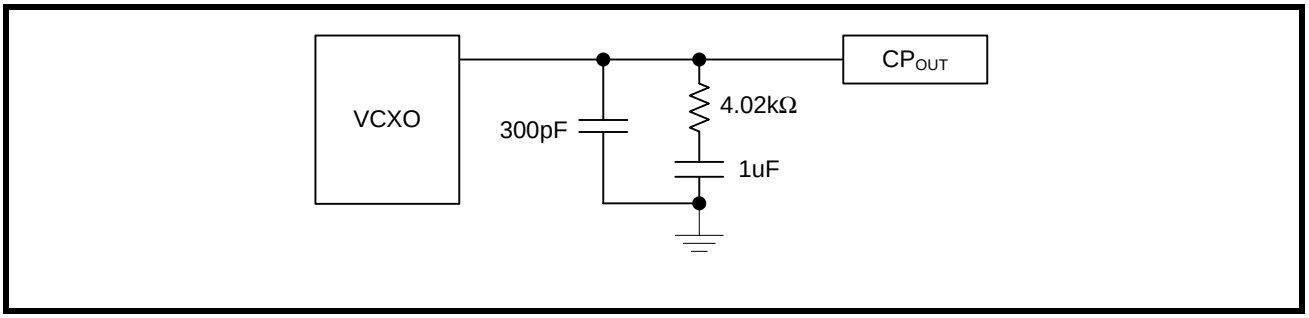
FIGURE 14. LOOP TIMING MODE USING AN EXTERNAL CLEANUP VCXO (HOST MODE ONLY)



3.8 External Loop Filter (Host Mode Only)

During Host Mode operation, RXCAP1N becomes the charge pump output CP_OUT. As shown in Figure 14, the internal charge pump is used to drive an external loop filter and external VCXO. The charge pump current is fixed at 250uA. Figure 15 is a simplified block diagram of the external loop filter and recommended values.

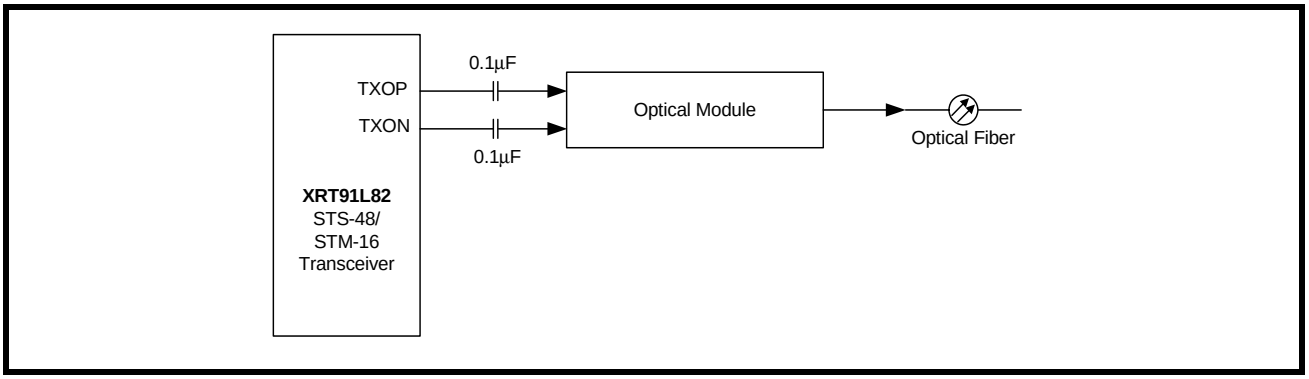
FIGURE 15. SIMPLIFIED DIAGRAM OF THE EXTERNAL LOOP FILTER



3.9 Transmit Serial Output Control

The 2.488/2.666 Gbps transmit serial output is avaliable on TXOP/N pins. The transmit serial output can be AC or DC coupled to an optical module or electrical interface. A simplified AC coupling block diagram is shown in Figure 16.

FIGURE 16. TRANSMIT SERIAL OUTPUT INTERFACE BLOCK



NOTE: *Some optical modules integrate AC coupled capacitors within the module. If so, the external AC coupled capacitors are not necessary and can be excluded.*

The 2.488/2.666 Gbps high-speed differential CML output TXOP/N swing mode can be controlled through an pin called TXSWING. Setting this pin "Low" enables Low Swing Mode and lowers power consumption. Setting this pin "High" configures the transmit serial output for High Swing Mode. Figure 17 shows the CML differential voltage swing.

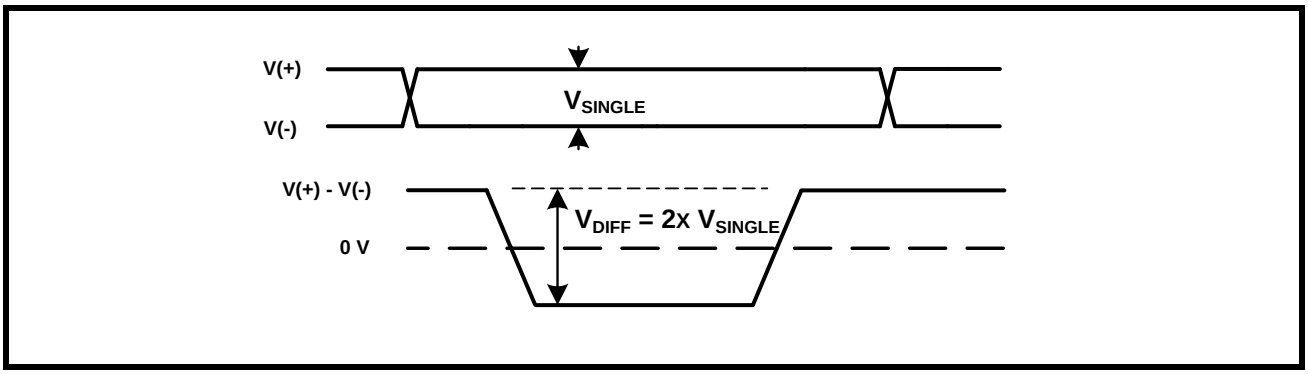
TABLE 12: DIFFERENTIAL CML OUTPUT SWING PARAMETERS

SIGNAL TYPE	PARAMETER	MIN (mV)	MAX (mV)	CML SERIAL VOLTAGE OUTPUT	TXSWING SETTING (100Ω LINE TO LINE)
Clock	$\Delta V_{OUTDIFF}$	700	1400	Differential Voltage Swing	High Swing Mode
Clock	ΔV_{OUTSE}	350	700	Single-Ended Voltage Swing	High Swing Mode
Data	$\Delta V_{OUTDIFF}$	800	1400	Differential Voltage Swing	High Swing Mode
Data	ΔV_{OUTSE}	400	700	Single-Ended Voltage Swing	High Swing Mode

TABLE 12: DIFFERENTIAL CML OUTPUT SWING PARAMETERS

SIGNAL TYPE	PARAMETER	MIN (mV)	MAX (mV)	CML SERIAL VOLTAGE OUTPUT	TXSWING SETTING (100Ω LINE TO LINE)
Clock	$\Delta V_{OUTDIFF}$	400	700	Differential Voltage Swing	Low Swing Mode
Clock	ΔV_{OUTSE}	200	350	Single-Ended Voltage Swing	Low Swing Mode
Data	$\Delta V_{OUTDIFF}$	400	850	Differential Voltage Swing	Low Swing Mode
Data	ΔV_{OUTSE}	200	425	Single-Ended Voltage Swing	Low Swing Mode

FIGURE 17. CML DIFFERENTIAL VOLTAGE SWING

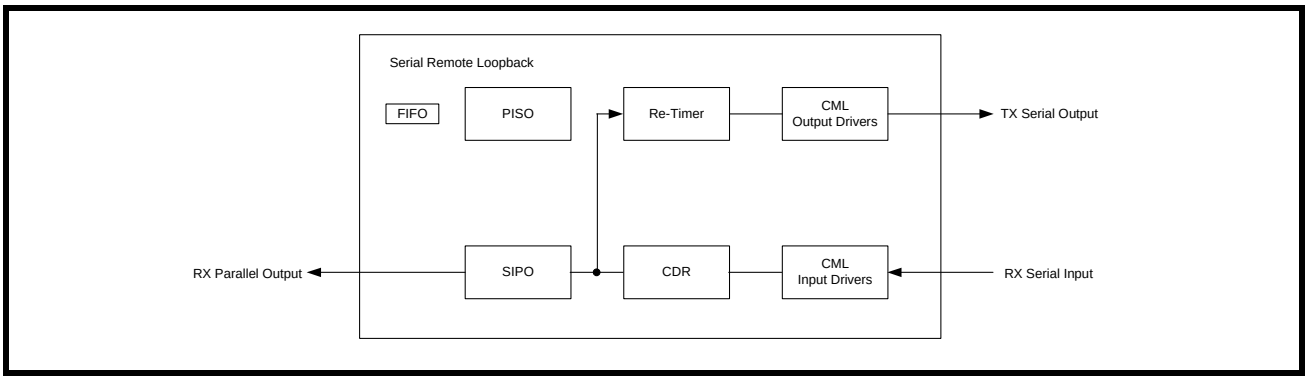


4.0 DIAGNOSTIC FEATURES

4.1 Serial Remote Loopback

RLOOPS_PRBSCLR is a dual function pin that serves as both serial remote loopback enable and PRBS error clear function. The serial remote loopback function is activated by setting RLOOPS_PRBSCLR "Low". When serial remote loopback is activated, the high-speed serial receive data from RXIP/N is presented at the high-speed transmit output TXOP/N, and the high-speed recovered clock is selected and presented to the high-speed transmit clock output TXSCLKOP/N. During serial remote loopback, the high-speed receive data (RXIP/N) is also converted to parallel data and presented at the low-speed receive parallel interface RXDO[15:0]P/N. The recovered receive clock is also divided by 16 and presented at the low-speed clock output RXPCLKOP/N to synchronize the transfer of the 16-bit received parallel data. In PRBS Test Mode, serial remote loopback is not available when the PRBS generator and analyzer is enabled. This pin serve as the PRBS error clear (PRBSCLR) function to reset the PRBS_ERR error output indicator. A simplified block diagram of serial remote loopback is shown in Figure 18.

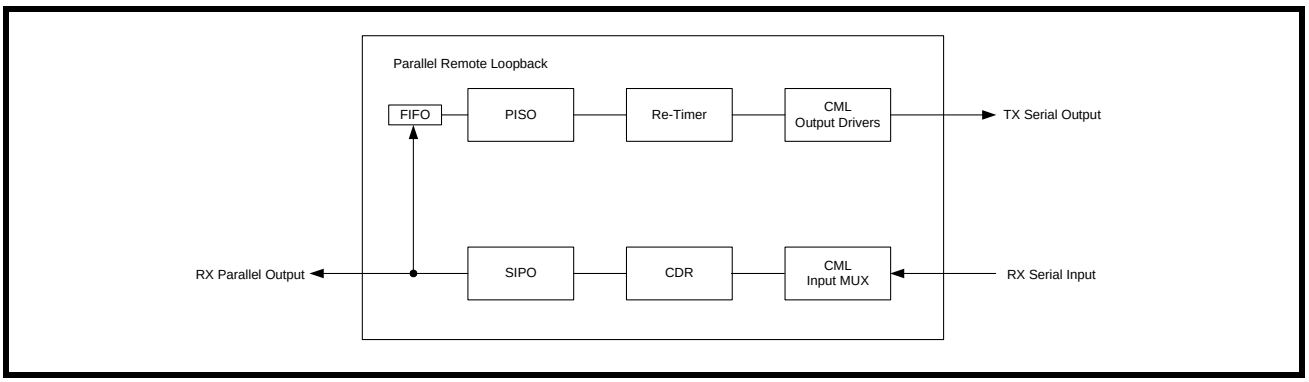
FIGURE 18. SERIAL REMOTE LOOPBACK



4.2 Parallel Remote Loopback (Host Mode Only)

RLOOPP controls a more comprehensive version of remote loopback that can also be used in conjunction with the de-jitter PLL that is phase locked to the recovered receive clock. In this mode, the received signal is processed by the CDR, and is sent through the serial to parallel converter. At this point, the 16-bit parallel data and clock are looped back to the transmit FIFO. Concurrently, if receive clock jitter attenuation is also employed, the received clock is divided down in frequency and presented to the input of the integrated phase/frequency detector and is compared to the frequency of a VCXO that is connected to the VCXO_IN input. With the LOOPTM_JA configured to use the recovered receive clock as the reference and VCXO_SEL asserted, the VCXO is phase locked to the recovered receive clock. The de-jittered clock is then used to retime the transmitter, resulting in the re-transmission of the de-jittered received data out of TXOP/N. A FIFO reset using FIFO_RST should follow immediately after enabling/disabling parallel remote loopback. A simplified block diagram of parallel remote loopback is shown in Figure 19.

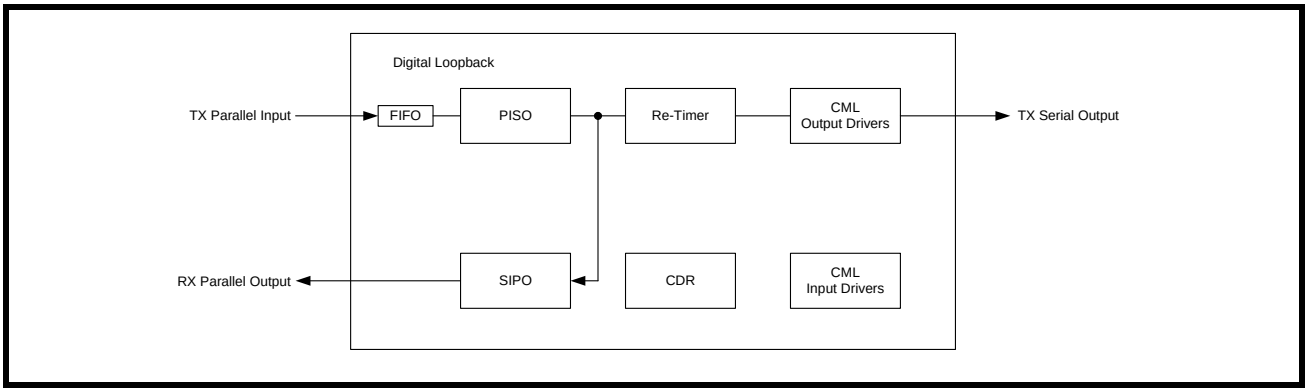
FIGURE 19. PARALLEL REMOTE LOOPBACK



4.3 Digital Local Loopback

The digital local loopback is activated when the $\overline{\text{DLOOP}}$ signal is set "Low." When digital local loopback is activated, the high-speed data from the output of the parallel to serial converter is looped back and presented to the high-speed input of the receiver serial to parallel converter. The CMU output is also looped back to the receive section and is used to synchronize the transfer of the data through the receiver. In Digital loopback mode the transmit data from the transmit parallel interface TXDI[15:0]P/N is serialized and presented to the high-speed transmit output TXOP/N along with the high-speed transmit clock which is generated from the clock multiplier unit and presented to the TXSCLKOP/N pins. A simplified block diagram of digital loopback is shown in Figure 20.

FIGURE 20. DIGITAL LOOPBACK



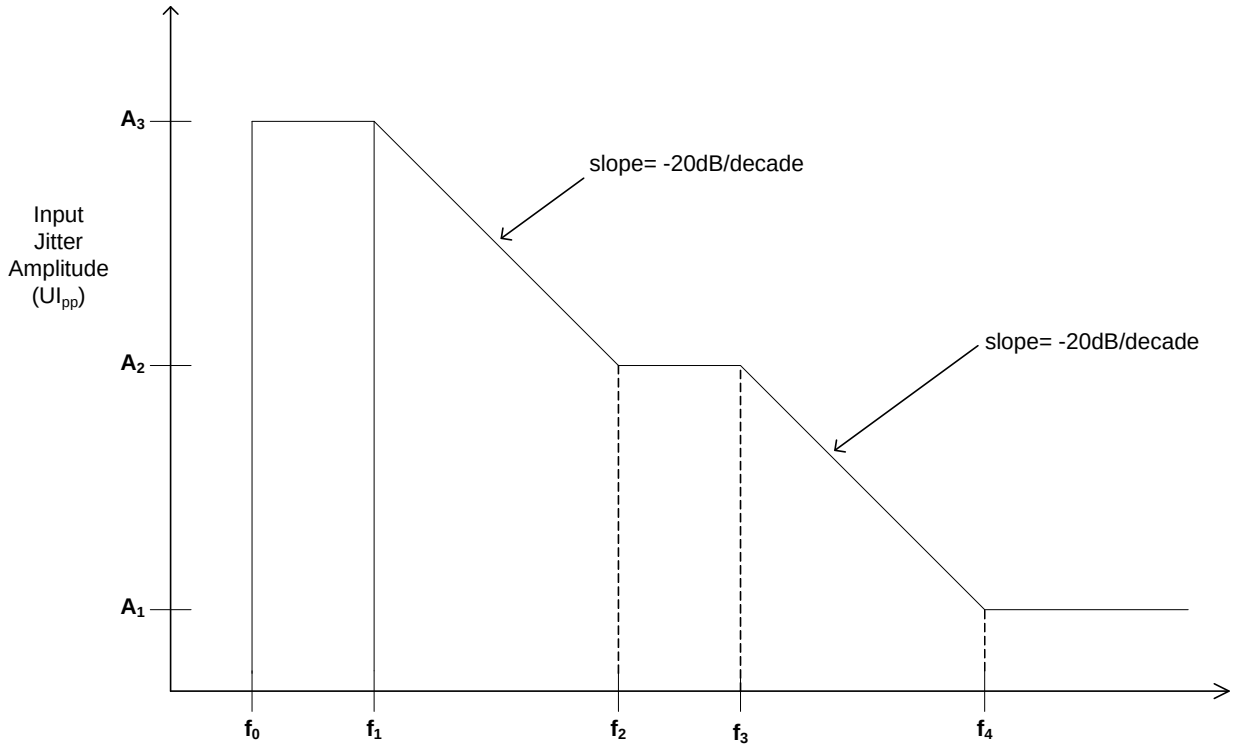
4.4 SONET Jitter Requirements

SONET equipment jitter requirements are specified for the following three types of jitter. The definitions of each of these types of jitter are given below. SONET equipment jitter requirements are specified for the following three types of jitter.

4.4.1 Jitter Tolerance:

Jitter tolerance is defined as the peak-to-peak amplitude of sinusoidal jitter applied on the input OC-N equipment interface that causes an equivalent 1dB optical power penalty. OC-1/STS-1, OC-3/STS-3, OC-12/ STS-12 and OC-48/STS-48 category II SONET interfaces should tolerate, the input jitter applied according to the mask of Figure 21, with the corresponding parameters specified in the figure.

FIGURE 21. JITTER TOLERANCE MASK



OC-N/STS-N LEVEL	F0 (HZ)	F1 (HZ)	F2 (HZ)	F3 (HZ)	F4 (HZ)	A1 (UIPP)	A2 (UIPP)	A3 (UIPP)
1	10	30	300	2K	20K	0.15	1.5	15
3	10	30	300	6.5K	65K	0.15	1.5	15
12	10	30	300	25K	250K	0.15	1.5	15
48	10	600	6000	100K	1000K	0.15	1.5	15

FIGURE 22. XRT91L82 MEASURED JITTER TOLERANCE IN LOOP TIMING MODE AT 2.488 GBPS STS-48/STM-16

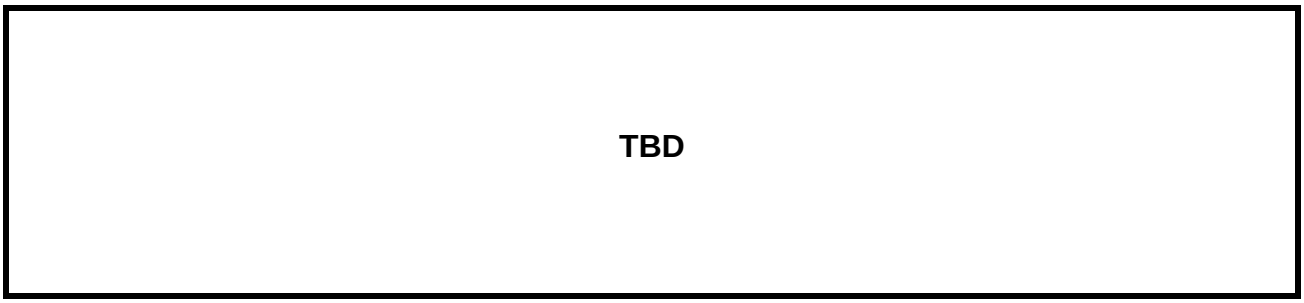
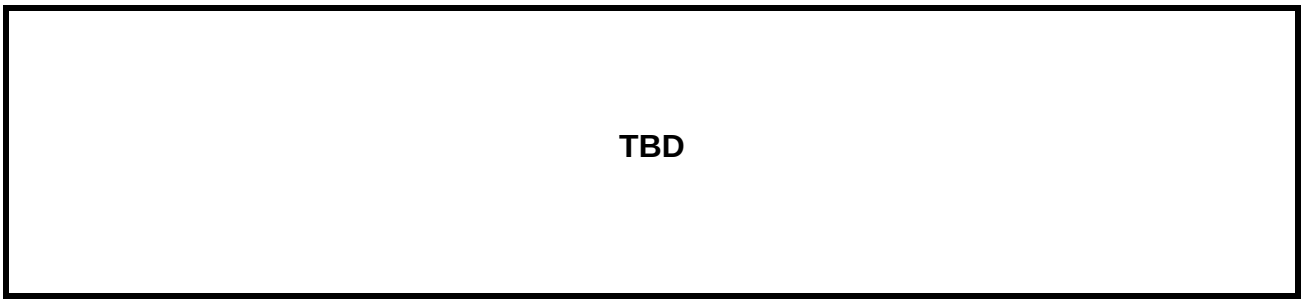


FIGURE 23. XRT91L82 MEASURED JITTER TOLERANCE IN LOOP TIMING MODE AT 2.666 GBPS FEC MODE



4.4.2 Jitter Transfer

Jitter transfer is defined as the ratio of the jitter on the output of STS-N to the jitter applied on the input of STS-N versus frequency. Jitter transfer is important in applications where the system is utilized in the loop-timed mode, where the recovered clock is used as the source of the transmit clock.

FIGURE 24. XRT91L82 MEASURED JITTER TRANSFER IN LOOP TIMING MODE AT 2.488 GBPS STS-48/STM-16

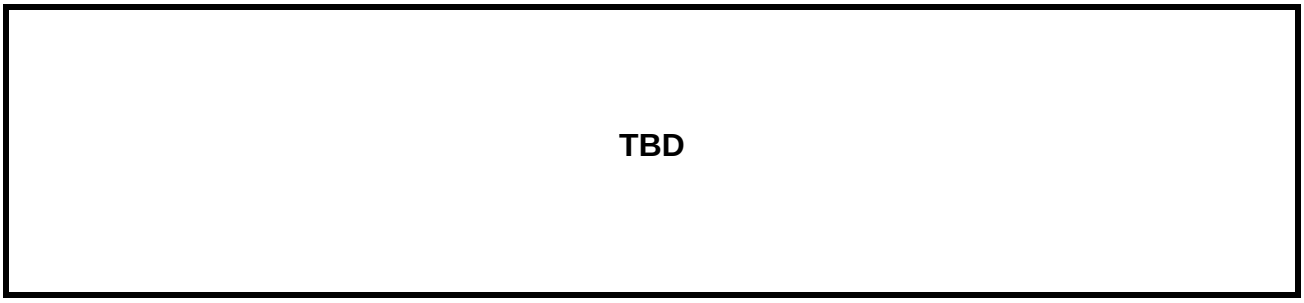
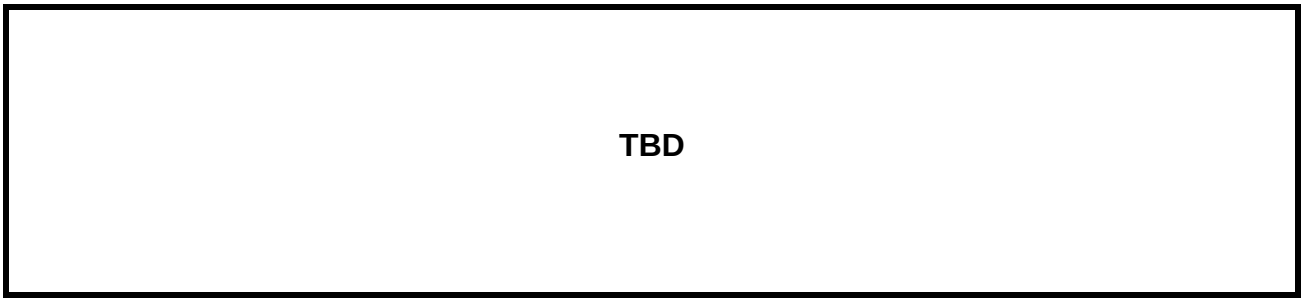


FIGURE 25. XRT91L82 MEASURED JITTER TRANSFER IN LOOP TIMING MODE AT 2.666 GBPS FEC MODE



4.4.3 Jitter Generation

Jitter generation is defined as the amount of jitter at the STS-N output in the absence of applied input jitter. The Bellcore and ITU requirement for this type jitter is 0.01UI rms measured with a specific band-pass filter.

For more information on these specifications refer to Bellcore TR-NWT-000253 sections 5.6.2-5 and GR-253-CORE section 5.6.

FIGURE 26. XRT91L82 MEASURED ELECTRICAL PHASE NOISE TRANSMIT JITTER GENERATION AT 2.488 GBPS

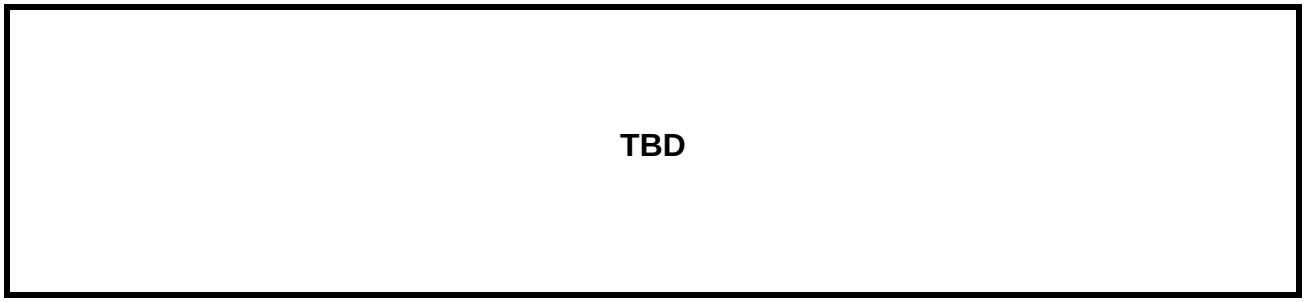
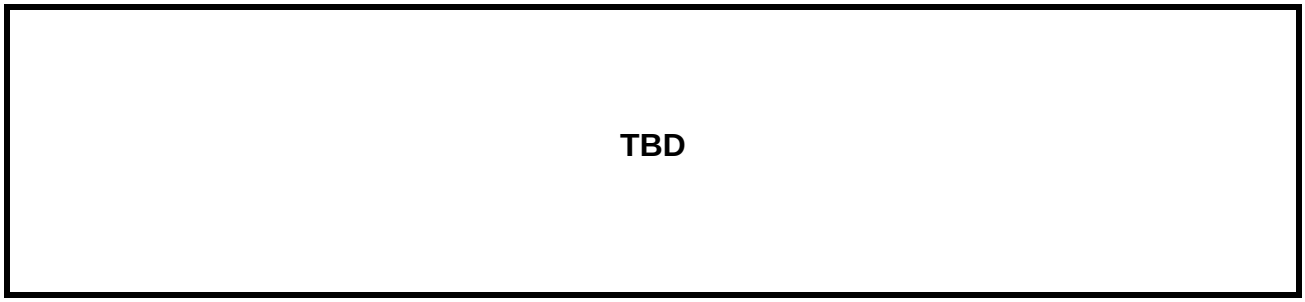


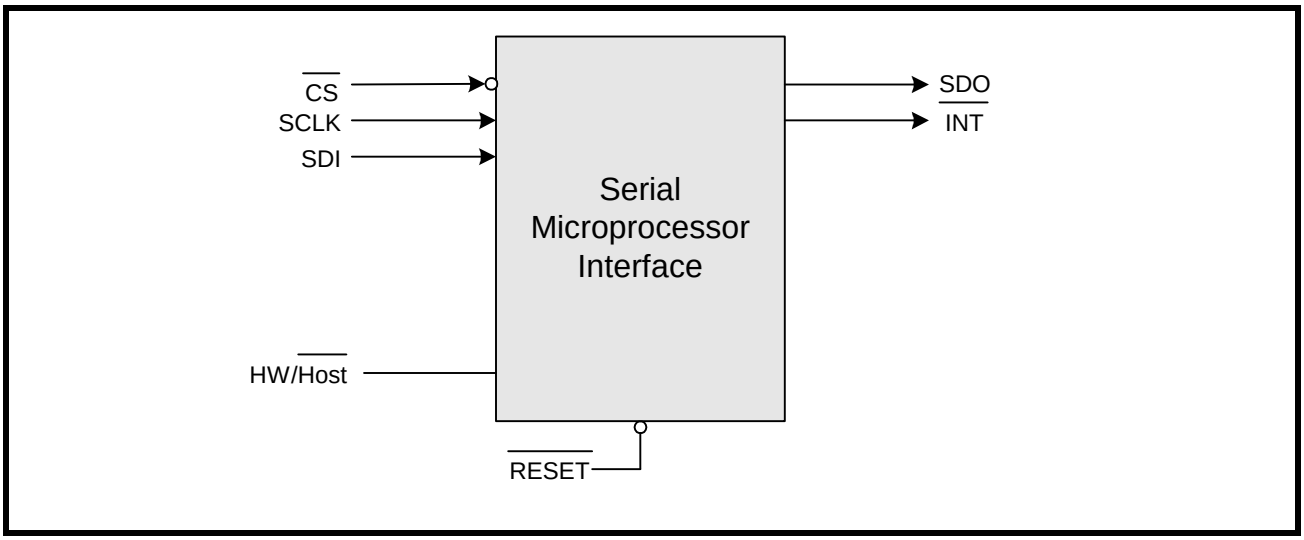
FIGURE 27. XRT91L82 MEASURED ELECTRICAL PHASE NOISE TRANSMIT JITTER GENERATION AT 2.666 GBPS



5.0 SERIAL MICROPROCESSOR INTERFACE BLOCK

The serial microprocessor uses a standard 3-pin serial port with $\overline{CS}$, SCLK, and SDI for programming the transceiver. Optional pins such as SDO, $\overline{INT}$, and $\overline{RESET}$ allow the ability to read back contents of the registers, monitor the transceiver via an interrupt pin, and reset the transceiver to its default configuration by pulling reset "Low" for more than 30ns. A simplified block diagram of the Serial Microprocessor is shown in Figure 28.

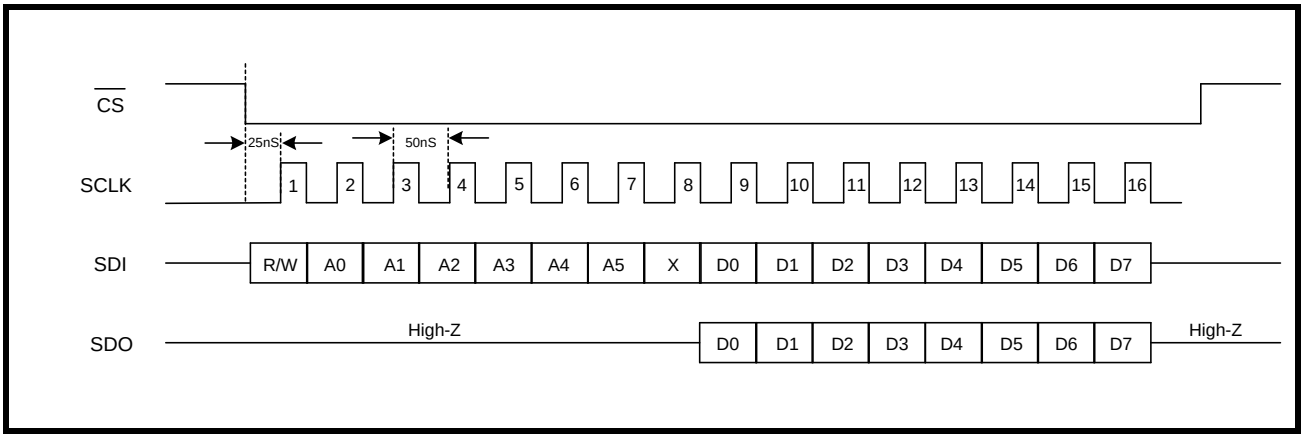
FIGURE 28. SIMPLIFIED BLOCK DIAGRAM OF THE SERIAL MICROPROCESSOR INTERFACE



5.1 SERIAL TIMING INFORMATION

The serial port requires 16 bits of data applied to the SDI (Serial Data Input) pin. The Serial Microprocessor samples SDI on the rising edge of SCLK (Serial Clock Input). The data is not latched into the device until all 16 bits of serial data have been sampled. A timing diagram of the Serial Microprocessor is shown in Figure 29.

FIGURE 29. TIMING DIAGRAM FOR THE SERIAL MICROPROCESSOR INTERFACE



NOTE: *The serial microprocessor interface does **NOT** support "burst write" or "burst read" operations. Chip Select (active "Low") **must be de-asserted** at the end of every single write or single read operation.*

5.2 16-BIT SERIAL DATA INPUT DESCRITPTION

The serial data input is sampled on the rising edge of SCLK. In readback mode, the serial data output is updated on the falling edge of SCLK. The serial data must be applied to the transceiver LSB first. The 16 bits of serial data are described below.

5.2.1 R/W (SCLK1)

The first serial bit applied to the transceiver informs the microprocessor that a Read or Write operation is desired. If the R/W bit is set to “0”, the microprocessor is configured for a Write operation. If the R/W bit is set to “1”, the microprocessor is configured for a Read operation.

5.2.2 A[5:0] (SCLK2 - SCLK7)

The next 6 SCLK cycles are used to provide the address to which a Read or Write operation will occur. A0 (LSB) must be sent to the transceiver first followed by A1 and so forth until all 6 address bits have been sampled by SCLK.

5.2.3 X (Dummy Bit SCLK8)

The dummy bit sampled by SCLK8 is used to allow sufficient time for the serial data output pin to update data if the readback mode is selected by setting R/W = “1”. Therefore, the state of this bit is ignored and can hold either “0” or “1” during both Read and Write operations.

5.2.4 D[7:0] (SCLK9 - SCLK16)

The next 8 SCLK cycles are used to provide the data to be written into the internal register chosen by the address bits. D0 (LSB) must be sent to the transceiver first followed by D1 and so forth until all 8 data bits have been sampled by SCLK. Once 16 SCLK cycles have been complete, the transceiver holds the data until $\overline{CS}$ is pulled “High” whereby, the serial microprocessor latches the data into the selected internal register.

5.3 8-BIT SERIAL DATA OUTPUT DESCRIPTION

The serial data output is updated on the falling edge of SCLK9 - SCLK16 if R/W is set to “1”. D0 (LSB) is provided on SCLK9 to the SDO pin first followed by D1 and so forth until all 8 data bits have been updated. The SDO pin allows the user to read the contents stored in individual registers by providing the desired address on the SDI pin during the Read cycle.

6.0 REGISTER MAP AND BIT DESCRIPTIONS

TABLE 13: MICROPROCESSOR REGISTER MAP

REG	ADDR	TYPE	D7	D6	D5	D4	D3	D2	D1	D0
Control Registers (0x00h - 0x3Fh)										
0	0x00	R/W	Reserved	PRBSLIE	PRBSEIE	VCXOIE	LOSIE	CDRIE	CMUIE	FIFOIE
1	0x01	RUR	Reserved	PRBSLIS	PRBSEIS	VCXOIS	LOSIS	CDRIS	CMUIS	FIFOIS
2	0x02	RO	Reserved	PRBS_LOCK	PRBS_ERR	VCXOD	LOSD	CDRD	CMUD	FIFOD
3	0x03	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FIFO_AUTO-RST	FIFO_RST
4	0x04	R/W	Reserved	Reserved	Reserved	Reserved	$\overline{\text{DISRD}}$	$\overline{\text{DISRDCLK}}$	TXSCLKOFF	$\overline{\text{CDRLCKREF}}$
5	0x05	R/W	Reserved	Reserved	PRBS_INV	PRBS_EN	Reserved	$\overline{\text{DLOOP}}$	$\overline{\text{RLOOPS}}$	$\overline{\text{RLOOPP}}$
6	0x06	R/W	VCXOLKEN	LOOPBW	Reserved	Reserved	Reserved	VCXO_SEL	LOOPTM_JA	LOOPTM_ NOJA
7	0x07	R/W	REFREQSEL 1	REFREQSEL 0	ALTFREQSEL	TXCLK016 SEL	INTERM	SEREFDIS	TXSWING	POLARITY
8	0x08		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
9	0x09		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
10	0x0A		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11	0x0B		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x0C - 0x3B		R/W	**Reserved**							
60	0x3C	RO	**Device ID MSB (See Bit Description)**							
61	0x3D	RO	**Device ID LSB (See Bit Description)**							
63	0x3F	RO	**Revision ID (See Bit Description)**							

TABLE 14: MICROPROCESSOR REGISTER 0X00H BIT DESCRIPTION

INTERRUPT ENABLE CONTROL REGISTER (0X00H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	PRBSLIE	**2^{23}-1 PRBS Pattern Lock Interrupt Enable** "0" = Masks the PRBS Pattern Lock interrupt generation "1" = Enables Interrupt generation ***NOTE:*** *PRBS_EN must be enabled for this bit to have functional meaning.*	R/W	0
D5	PRBSEIE	**2^{23}-1 PRBS Pattern Error Interrupt Enable** "0" = Masks the PRBS error interrupt generation "1" = Enables Interrupt generation ***NOTE:*** *PRBS_EN must be enabled for this bit to have functional meaning.*	R/W	0
D4	VCXOIE	**Voltage Controlled External Oscillator Lock Interrupt Enable** "0" = Masks the VCXO Lock interrupt generation "1" = Enables Interrupt generation ***NOTE:*** *VCXOLKEN must be enabled for this bit to have functional meaning.*	R/W	0
D3	LOSIE	**Loss of Signal Interrupt Enable** "0" = Masks the LOS interrupt generation "1" = Enables Interrupt generation	R/W	0
D2	CDRIE	**Clock and Data Recovery Lock Interrupt Enable** "0" = Masks the CDR Lock interrupt generation "1" = Enables Interrupt generation	R/W	0
D1	CMUIE	**Clock Multiplier Unit Lock Interrupt Enable** "0" = Masks the CMU Lock interrupt generation "1" = Enables Interrupt generation	R/W	0
D0	FIFOIE	**FIFO Overflow Interrupt Enable** "0" = Masks the FIFO Overflow interrupt generation "1" = Enables Interrupt generation	R/W	0

TABLE 15: MICROPROCESSOR REGISTER 0X01H BIT DESCRIPTION

INTERRUPT STATUS CONTROL REGISTER (0X01H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	PRBSLIS	**2^{23}-1 PRBS Pattern Lock Interrupt Status** An external interrupt will not occur unless the PRBSLIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in PRBS Lock Status Occurred ***NOTE:*** *PRBS_EN must be enabled for this bit to have functional meaning.*	RUR	0
D5	PRBSEIS	**2^{23}-1 PRBS Pattern Error Detect Interrupt Status** Indicates an error condition **has occurred** in the validation of generated PRBS pattern. "0" = Un-erred transmission and reception of PRBS pattern. "1" = PRBS pattern validation error has Occured ***NOTE:*** *PRBS_EN must be enabled for this bit to have functional meaning.*	RUR	0
D4	VCXOIS	**Voltage Controlled External Oscillator Lock Interrupt Status** An external interrupt will not occur unless the VCXOIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in VCXO Lock Status Occurred ***NOTE:*** *VCXOLKEN must be enabled for this bit to have functional meaning.*	RUR	0
D3	LOSIS	**Loss of Signal Interrupt Status** An external interrupt will not occur unless the RLOSIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in LOS Status Occurred	RUR	0
D2	CDRIS	**Clock and Data Recovery Lock Interrupt Status** An external interrupt will not occur unless the CDRIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in CDR Lock Status Occurred	RUR	0
D1	CMUIS	**Clock Multiplier Unit Lock Interrupt Status** An external interrupt will not occur unless the CMUIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in CMU Lock Status Occurred	RUR	0
D0	FIFOIS	**FIFO Overflow Interrupt Status** An external interrupt will not occur unless the FIFOIE is set to "1" in the channel register 0x00h. "0" = No Change "1" = Change in FIFO Overflow Status Occurred	RUR	0

TABLE 16: MICROPROCESSOR REGISTER 0X02H BIT DESCRIPTION

STATUS CONTROL REGISTER (0X02H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	PRBS_LOCK	**2^{23}-1 PRBS Pattern Lock Detection** Indicates that current state condition of the PRBS pattern analyzer when the PRBS pattern generator is enabled. "0" = PRBS pattern analyzer currently Out of Lock "1" = PRBS pattern analyzer currently Locked	RO	0
D5	PRBS_ERR	**2^{23}-1 PRBS Pattern Error Detection** Indicates an error condition **is occuring** in the validation of generated PRBS pattern. "0" = Un-erred transmission and reception of PRBS pattern. "1" = PRBS pattern validation error condition is present. ***NOTE:*** *PRBS_EN must be enabled for this bit to have functional meaning.*	RO	0
D4	VCXOD	**Voltage Controlled External Oscillator Lock Detection** The VCXOD is used to indicate whether the internal clock reference is locked to an external VCO. "0" = VCXO currently not Locked "1" = VCXO Locked ***NOTE:*** *VCXOLKEN must be enabled for this bit to have functional meaning.*	RO	0
D3	LOSD	**Loss of Signal Detection** The LOSD indicates the Loss of Signal Detect activity. "0" = No Alarm "1" = A LOSD condition is present	RO	0
D2	CDRD	**Clock and Data Recovery Lock Detection** The CDRD is used to indicate that the CDR is locked. "0" = CDR Out of Lock "1" = CDR Locked	RO	0
D1	CMUD	**Clock Multiplier Unit Lock Detection** The CMUD is used to indicate that the CMU is locked. "0" = CMU Out of Lock "1" = CMU Locked	RO	0
D0	FIFOD	**FIFO Overflow Detection** The FIFOD indicates that the FIFO is experiencing an overflow condition. "0" = No Alarm "1" = A FIFO Overflow condition is present	RO	0

TABLE 17: MICROPROCESSOR REGISTER 0X03H BIT DESCRIPTION

FIFO CONTROL REGISTER (0X03H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	Reserved	This Register Bit is Not Used	X	X
D5	Reserved	This Register Bit is Not Used	X	X
D4	Reserved	This Register Bit is Not Used	X	X
D3	Reserved	This Register Bit is Not Used	X	X
D2	Reserved	This Register Bit is Not Used	X	X
D1	FIFO_ AUTORST	**Automatic FIFO Overflow Reset** If this bit is set to "1", the STS-48 transceiver will automatically flush the FIFO upon an overflow condition. Upon power-up, the FIFO should be manually reset by setting FIFO_RST to "1" for a minimum of 2 TXPCLKOP/N cycles. "0" = Manual FIFO reset required for Overflow Conditions "1" = Automatically resets FIFO upon Overflow Detection	R/W	0
D0	FIFO_RST	**Manual FIFO Reset** FIFORST should be set to "1" for a minimum of 2 TXPCLKOP/N cycles during power-up and manual FIFO reset in order to flush out the FIFO. After the FIFORST bit is returned "Low," it will take 8 to 10 TXPCLKOP/N cycles for the FIFO to flush out. Upon an interrupt indication that the FIFO has an overflow condition, this bit is used to reset or flush out the FIFO. "0" = Normal Operation "1" = Manual FIFO Reset ***NOTE:*** *To automatically reset the FIFO, see the FIFO_AUTORST bit.*	R/W	0

TABLE 18: MICROPROCESSOR REGISTER 0X04H BIT DESCRIPTION

OUTPUT CONTROL REGISTER (0X04H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	Reserved	This Register Bit is Not Used	X	X
D5	Reserved	This Register Bit is Not Used	X	X
D4	Reserved	This Register Bit is Not Used	X	X
D3	$\overline{\text{DISRD}}$	**Receive Parallel Data Output Disable** If this bit is set to "0", the 16-bit parallel receive data output will asynchronously mute. "0" = Forces RXDO[15:0]P/N to a logic state "0" "1" = Normal Mode	R/W	1
D2	$\overline{\text{DISRDCLK}}$	**Receive Parallel Clock Output Disable** This bit is used to asynchronously control the activity of the parallel receive clock output. "0" = Forces RXPCLKOP/N to a logic state of "0" "1" = Normal Mode	R/W	1
D1	TXSCLKOOFF	**Transmit Serial Clock Output Tristate** This bit is used to control the activity of the 2.488/2.666 GHz differential serial clock output. Tristating TXSCLKOP/N output reduces power consumption. "0" = TXSCLKOP/N output Enabled "1" = TXSCLKOP/N output Tristated	R/W	1
D0	$\overline{\text{CDRLCKREF}}$	**CDR's Recovered High-speed Serial Clock Reference** Controls CDR's operation. "0" = Forced to lock to CDR PLL reference training clock "1" = Normal Operation (Locked to incoming serial data)	R/W	1

TABLE 19: MICROPROCESSOR REGISTER 0X05H BIT DESCRIPTION

DIAGNOSTIC CONTROL REGISTER (0X05H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Reserved	This Register Bit is Not Used	X	X
D6	Reserved	This Register Bit is Not Used	X	X
D5	PRBS_INV	**2^{23}-1 PRBS Pattern Invert** This bit will invert each of the Pseudo Random Binary Sequence pattern bit from "0" to "1" and from "1" to "0." "0" = Normal Operation "1" = PRBS bit patterns inverted.	R/W	0
D4	PRBS_EN	**2^{23}-1 PRBS TEST Pattern Enable** Generates 2^{23}-1 Pseudo Random Binary Sequence test patterns and analyzes in the receiving block for correct sequence pattern. "0" = Normal Mode "1" = PRBS pattern generator and analyzer Enabled. ***NOTE:*** *A Local Loopback of some type such as Digital Local Loopback or an optical cable loopback is expected to be used in conjunction with PRBS_EN in order for the PRBS analyzer to receive the PRBS pattern.*	R/W	0
D3	Reserved	This Register Bit is Not Used	X	X
D2	$\overline{\text{DLOOP}}$	**Digital Local Loopback** Digital local loopback allows the transmit input pins to be looped back to the receive output pins for local diagnostics. The transmit serial data output is valid during the digital loopback. "0" = Enable Digital Local Loopback "1" = Disabled ***NOTE:*** *$\overline{\text{RLOOPS}}$ and $\overline{\text{RLOOPP}}$ should be **disabled** when $\overline{\text{DLOOP}}$ is enabled.*	R/W	1

DIAGNOSTIC CONTROL REGISTER (0X05H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D1	$\overline{\text{RLOOPS}}$	**Serial Remote Loopback** Serial remote loopback allows the receive serial input pins to be looped back to the transmit serial output pins for remote diagnostics. The receive data output is valid during a serial remote loopback. "0" = Enable Remote Serial Loopback "1" = Disabled ***NOTE:*** *$\overline{\text{DLOOP}}$ and $\overline{\text{RLOOPP}}$ should be **disabled** when $\overline{\text{RLOOPS}}$ is enabled.*	R/W	1
D0	$\overline{\text{RLOOPP}}$	**Parallel Remote Loopback** Parallel remote loopback has the same affect as the serial remote loopback, except that the data input is allowed to pass through the SIPO before it's looped back to the transmit path, wherein it passes through the transmit FIFO, through the PISO, and back out the transmit serial output. The receive data output is valid during a parallel remote loopback. "0" = Enable Remote Parallel Loopback "1" = Disabled ***NOTE:*** *$\overline{\text{DLOOP}}$ and $\overline{\text{RLOOPS}}$ should be **disabled** when $\overline{\text{RLOOPP}}$ is enabled. The internal FIFO should also be flushed using FIFO_RST when parallel remote loopback is enabled/disabled.*	R/W	1

TABLE 20: MICROPROCESSOR REGISTER 0X06H BIT DESCRIPTION

TIMING CONTROL REGISTER (0X06H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	VCXOLKEN	**De-Jitter PLL Lock Detect Enable** This bit enables the VCXO_IN input lock detect circuit to be active. "0" = VCXO Lock Detect Disabled "1" = VCXO Lock Detect Enabled	R/W	0
D6	LOOPBW	**CMU Loop Band Width Select** This bit is used to select the bandwidth of the clock multiplier unit of the transmit path to a narrow or wide band. Use Wide Band for clean reference signals and Narrow Band for noisy references. "0" = Wide Band (4x) "1" = Narrow Band (1x)	R/W	0
D5	Reserved	This Register Bit is Not Used	X	X
D4	Reserved	This Register Bit is Not Used	X	X
D3	Reserved	This Register Bit is Not Used	X	X
D2	VCXO_SEL	**VCXO De-Jitter Select** This bit selects either the normal REF1CLKP/N and REF2CLKP/N or the de-jitter VCXO_IN as a reference clock to the CMU. "0" = Normal REF1CLKP/N and/or REF2CLKP/N Mode "1" = De-Jitter VCXO Mode	R/W	0
D1	LOOPTM_JA	**Loop Timing With Jitter Attenuation** The LOOPTM_JA bit must be set to "1" in order to select the recovered receive clock as the reference source for the de-jitter PLL. "0" = Disabled "1" = Loop timing with de-jitter PLL Activated	R/W	0
D0	LOOPTM_ NOJA	**Loop Timing With No Jitter Attenuation** When the loop timing mode is activated, the external local reference clock input to the CMU is replaced with the 1/16th or 1/32nd (ALTFREQSEL option available in Host Mode) of the high-speed recovered receive clock coming from the CDR. "0" = Disabled "1" = Loop timing Activated	R/W	0

TABLE 21: MICROPROCESSOR REGISTER 0X07H BIT DESCRIPTION

<table>
<tr><th colspan="5">CONFIGURATION CONTROL REGISTER (0X07H)</th></tr>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th><th>Register Type</th><th>Default Value (HW reset)</th></tr>
<tr><td>D7</td><td>REFREQSEL1</td><td>Input Reference Frequency Select
This bit is used to select the clock input reference.

<table>
<tr><th>REFREQSEL [1:0]</th><th>CMU REFERENCE FREQUENCY</th><th>CDR REFERENCE FREQUENCY</th></tr>
<tr><td>00</td><td>155.52 MHz present on REF1CLK
REF2CLK not used</td><td>155.52 MHz present on REF1CLK
REF2CLK not used</td></tr>
<tr><td>01</td><td>155.52 MHz present on REF1CLK</td><td>166.63 MHz present on REF2CLK</td></tr>
<tr><td>10</td><td>166.63 MHz present on REF2CLK</td><td>155.52 MHz present on REF1CLK</td></tr>
<tr><td>11</td><td>166.63 MHz present on REF2CLK
REF1CLK not used</td><td>166.63 MHz present on REF2CLK
REF1CLK not used</td></tr>
</table>
Note: Non-FEC transmission and/or reception modes require 155.52 MHz clock reference. FEC transmission and/or reception mode requires 166.63 MHz clock reference.</td><td>R/W</td><td>0</td></tr>
<tr><td>D6</td><td>REFREQSEL0</td><td>Input Reference Frequency Select
This bit is used to select the clock input reference.

<table>
<tr><th>REFREQSEL [1:0]</th><th>CMU REFERENCE FREQUENCY</th><th>CDR REFERENCE FREQUENCY</th></tr>
<tr><td>00</td><td>155.52 MHz present on REF1CLK
REF2CLK not used</td><td>155.52 MHz present on REF1CLK
REF2CLK not used</td></tr>
<tr><td>01</td><td>155.52 MHz present on REF1CLK</td><td>166.63 MHz present on REF2CLK</td></tr>
<tr><td>10</td><td>166.63 MHz present on REF2CLK</td><td>155.52 MHz present on REF1CLK</td></tr>
<tr><td>11</td><td>166.63 MHz present on REF2CLK
REF1CLK not used</td><td>166.63 MHz present on REF2CLK
REF1CLK not used</td></tr>
</table>
Note: Non-FEC transmission and/or reception modes require 155.52 MHz clock reference. FEC transmission and/or reception mode requires 166.63 MHz clock reference.</td><td>R/W</td><td>0</td></tr>
</table>

CONFIGURATION CONTROL REGISTER (0X07H)

BIT	NAME	FUNCTION	Register Type	Default Value (HW reset)
D5	ALTFREQSEL	**Alternate Low Reference Frequency Select (77.76/83.31 MHz)** This pin is used to select and support lower frequency settings on REF1CLKP/N and REF2CLKP/N reference clock inputs. When using a VCXO, this pin should also be set accordingly to the VCXO frequency output. "0" = 77.76/83.31 MHz reference frequency support "1" = 155.52/166.63 MHz reference frequency support If **ALTFREQSEL** = "**0**" **REFREQSEL [1:0]** / **CMU REFERENCE FREQUENCY** / **CDR REFERENCE FREQUENCY** **00**: 77.76 MHz present on REF1CLK, REF2CLK not used / 77.76 MHz present on REF1CLK, REF2CLK not used **01**: 77.76 MHz present on REF1CLK / 83.31 MHz present on REF2CLK **10**: 83.31 MHz present on REF2CLK / 77.76 MHz present on REF1CLK **11**: 83.31 MHz present on REF2CLK, REF1CLK not used / 83.31 MHz present on REF2CLK, REF1CLK not used Note: Non-FEC transmission and/or reception modes require 77.76 MHz clock reference. FEC transmission and/or reception mode requires 83.31 MHz clock reference. If **ALTFREQSEL** = "**1**" **REFREQSEL [1:0]** / **CMU REFERENCE FREQUENCY** / **CDR REFERENCE FREQUENCY** **00**: 155.52 MHz present on REF1CLK, REF2CLK not used / 155.52 MHz present on REF1CLK, REF2CLK not used **01**: 155.52 MHz present on REF1CLK / 166.63 MHz present on REF2CLK **10**: 166.63 MHz present on REF2CLK / 155.52 MHz present on REF1CLK **11**: 166.63 MHz present on REF2CLK, REF1CLK not used / 166.63 MHz present on REF2CLK, REF1CLK not used Note: Non-FEC transmission and/or reception modes require 155.52 MHz clock reference. FEC transmission and/or reception mode requires 166.63 MHz clock reference.	R/W	1
D4	TXCLKO16SEL	**Auxiliary Clock Output Select** This bit is used to select the auxiliary clock frequency output. "0" = TXCLKO16P/N outputs 155.52/166.63 MHz "1" = TXCLKO16P/N outputs 19.44/20.83 MHz	R/W	0

CONFIGURATION CONTROL REGISTER (0X07H)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D3	INTERM	**Transmit Parallel Bus Input Internal Termination** Provides 100Ω line-to-line internal termination to TXDI[15:0]P/N and TXPCLKIP/N. "Low" = Disabled "High" = TXDI[15:0]P/N and TXPCLKIP/N internally terminated.	R/W	0
D2	SEREFDIS	**SE_REF Power down Control** Powers down SE_REF and reduces power consumption. "0" = SE_REF Enabled "1" = SE_REF Disabled	R/W	1
D1	TXSWING	**Serial CML Optical Transceiver Swing Select** This bit is used to select the output swing of the high-speed CML interface to the optical transceiver. "0" = Low Swing Mode CML Output Selected "1" = High Swing Mode CML Output Selected See Table 12 in “Section 3.9, Transmit Serial Output Control” on page 28.	R/W	1
D0	POLARITY	**Polarity for SDEXT Input** Controls the Signal Detect polarity convention of SDEXT. "0" = SDEXT is active "Low" "1" = SDEXT is active "High"	R/W	1

TABLE 22: MICROPROCESSOR REGISTER 0X3CH BIT DESCRIPTION

DEVICE "ID" REGISTER (0X3CH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7 D6 D5 D4 D3 D2 D1 D0	Device "ID" MSB	The device "ID" of the XRT91L82 LIU is 0x8003h. Along with the revision "ID", the device "ID" is used to enable software to identify the silicon adding flexibility for system control and debug.	RO	1 0 0 0 0 0 0 0

TABLE 23: MICROPROCESSOR REGISTER 0X3DH BIT DESCRIPTION

DEVICE "ID" REGISTER (0X3DH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Device "ID" LSB	The device "ID" of the XRT91L82 LIU is 0x8003h. Along with the revision "ID", the device "ID" is used to enable software to identify the silicon adding flexibility for system control and debug.	RO	0
D6				0
D5				0
D4				0
D3				0
D2				0
D1				1
D0				1

TABLE 24: MICROPROCESSOR REGISTER 0X3FH BIT DESCRIPTION

REVISION "ID" REGISTER (0X3FH)				
BIT	**NAME**	**FUNCTION**	Register Type	Default Value (HW reset)
D7	Revision "ID"	The revision "ID" of the XRT91L82 LIU is used to enable software to identify which revision of silicon is currently being tested. The revision "ID" for the first revision of silicon (Revision A) will be 0x01h.	RO	This byte shows the revision of the device.
D6				
D5				
D4				
D3				
D2				
D1				
D0				

7.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Thermal Resistance of STBGA Package....Θ_{jA} = 25°C/W		Operating Temperature Range.....-40°C t o 85°C
Thermal Resistance of STBGA Package....Θ_{jC} = 10°C/W		Case Temperature under bias.....-55°C to 125°C
ESD Protection (HBM).....>2000V		Storage Temperature .....-65°C to 150°C

ABSOLUTE MAXIMUM POWER AND INPUT LOGIC SIGNALS

SYMBOL	TYPE	PARAMETER	MIN	TYP	MAX	UNITS
$VDD_{1.8}$		1.8V Digital and Analog Power Supplies	-0.5		3.6	V
$VDD_{\_IO}$		3.3V LVPECL/LVDS Input Power Supply	-0.5		6.0	V
	LVPECL	DC logic signal input voltage	-0.5		$VDD_{\_IO}$ +0.5	V
	LVDS	DC logic signal input voltage	-0.5		$VDD_{\_IO}$ +0.5	V
	LVTTL/ LVCMOS	DC logic signal input voltage	-0.5		5.5	V
	LVCMOS	DC logic signal output voltage	-0.5		$VDD_{\_IO}$ +0.5	V
	LVPECL	Input current	-100		100	mA
	LVTTL/ LVCMOS	Input current	-100		100	mA

NOTE: *Stresses listed under Absolute Maximum Power and I/O ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods will severely affect device reliability.*

POWER AND CURRENT DC ELECTRICAL CHARACTERISTICS

SYMBOL	TYPE	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
$VDD_{1.8}$		CML and CMOS Power Supply Voltage	1.710	1.8	1.890	V	
$AVDD_{TX}$		Transmit Power Supply Voltage (AVDD_TX)	1.710	1.8	1.890	V	
$AVDD_{RX}$		Receiver Power Supply Voltage (AVDD_RX)	1.710	1.8	1.890	V	
$VDD_{\_IO}$		LVPECL or LVDS Input and Digital I/O Power Supply Voltage	3.135	3.3	3.465	V	
		1.8V Power Supply Noise Rejection Ratio			50	mV_{P-P}	6 KHz - 2 MHz
		3.3V Power Supply Noise Rejection Ratio			50	mV_{P-P}	6 KHz - 2 MHz
$I_{DD\_1.8}$		1.8V Total Power Supply Current		TBD		mA	
I_{DD_IO}		3.3V Total Power Supply Current		TBD		mA	

POWER AND CURRENT DC ELECTRICAL CHARACTERISTICS

SYMBOL	TYPE	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
P_{LVDS}		Total Power Dissipation		500	700	mW	LVDS
P_{LVPECL}		Total Power Dissipation		1400	1700	mW	LVPECL

LVPECL LOGIC SIGNAL DC ELECTRICAL CHARACTERISTICS

Test Condition: T_A = 25°C, $VDD_{1.8}$ = 1.8V ± 5%, $VDD_{\_IO}$ = 3.3V ± 5%, $VDD_{\_IO}$= 3.3V ± 5% unless otherwise specified

SYMBOL	TYPE	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{OH}	LVPECL	Output High Voltage	$VDD_{\_IO}$ -1.15		$VDD_{\_IO}$ -0.735	V	
V_{OL}	LVPECL	Output Low Voltage	$VDD_{\_IO}$ -1.95		$VDD_{\_IO}$ -1.495	V	
V_{ODIFF}	LVPECL	Output Differential Voltage Swing	1		2	V	
$V_{OSINGLE}$	LVPECL	Output Single-Ended Voltage Swing	0.5		1	V	Single-Ended
V_{IH}	LVPECL	Input High Voltage	$VDD_{\_IO}$ - 1.2		$VDD_{\_IO}$ - 0.7	V	Differential and Single-Ended
V_{IL}	LVPECL	Input Low Voltage	$VDD_{\_IO}$ - 2.0		$VDD_{\_IO}$ - 1.40	V	Differential and Single-Ended
V_{IDIFF}	LVPECL	Input Differential Voltage	0.4		2.4	V	Differential Mode. See Figure 17
$V_{ISINGLE}$	LVPECL	Input Single-Ended Voltage Swing	0.2		1.2	V	Differential Mode. See Figure 17
V_{ISE}	LVPECL	Input Single-Ended Voltage Swing	0.4 (+/- 0.2V w.r.t. VBB100K)			V	Single-Ended Mode See Figure 17

LVDS LOGIC SIGNAL DC ELECTRICAL CHARACTERISTICS

Test Condition: T_A = 25°C, $VDD_{1.8}$ = 1.8V ± 5%, $VDD_{\_IO}$ = 3.3V ± 5% unless otherwise specified

SYMBOL	TYPE	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{OH}	LVDS	Output High Voltage			1680	mV	100 Ω line - line
V_{OL}	LVDS	Output Low Voltage	810			mV	100 Ω line - line
V_{ODIFF}	LVDS	Output Differential Voltage Swing	450		1320	mV	100 Ω line - line
$V_{OSINGLE}$	LVDS	Output Single-Ended Voltage Swing	225		660	mV	100 Ω line - line
V_{IH}	LVDS	Input High Voltage			2400	mV	

Test Condition: T_A = 25°C, $VDD_{1.8}$ = 1.8V ± 5%, VDD_{IO} = 3.3V ± 5% unless otherwise specified							
SYMBOL	**TYPE**	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
V_{IL}	LVDS	Input Low Voltage	800			mV	
V_{IDIFF}	LVDS	Input Differential Voltage Swing	200		1300	mV	
$V_{ISINGLE}$	LVDS	Input Single-Ended Voltage Swing	100		650	mV	

LVTTL/LVCMOS SIGNAL DC ELECTRICAL CHARACTERISTICS

Test Condition: T_A = 25°C, $VDD_{1.8}$ = 1.8V ± 5%, VDD_{IO} = 3.3V ± 5% unless otherwise specified							
SYMBOL	**TYPE**	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
V_{OH}	LVCMOS	Output High Voltage	2.93		VDD_{IO}	V	I_{OH} = -1.0mA
V_{OL}	LVCMOS	Output Low Voltage	0		0.2	V	I_{OH} = 1.0mA
V_{IH}	LVTTL/ LVCMOS	Input High Voltage	2.2		3.3	V	
V_{IL}	LVTTL/ LVCMOS	Input Low Voltage	-0.5		0.7	V	
I_{IH}	LVTTL/ LVCMOS	Input High Current		50	500	µA	2.2V<V_{IN}<3.3V V_{IN}=2.4V typical
I_{IL}	LVTTL/ LVCMOS	Input Low Current			-500	µA	-0.5V<V_{IN}<0.7V
I_{LEAK}	LVTTL/ LVCMOS	Input Leakage Current	-10		10	µA	V_{IN} = VDD_{IO} or V_{IN} = 0
I_{LEAK_PU}	LVTTL/ LVCMOS	Input Leakage Current with Pull-Up Resistor	61.3		216	µA	V_{IN} = 0
I_{LEAK_PD}	LVTTL/ LVCMOS	Input Leakage Current with Pull-Down Resistor	61.3		216	µA	V_{IN} = VDD_{IO}

NOTE: *All input control pins are LVCMOS and LVTTL compatible. All output control pins are LVCMOS compatible only.*

SEREF OUTPUT CHARACTERISTICS

SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
V_{BB}	100 K Reference Bias Voltage	VDD_{IO} - 1.45		VDD_{IO} - 1.17	V	
NOTE: *The SEREF output is designed to have maximum 30pF load capacitance, 750µA sourcing and 1 mA sinking capability.*						

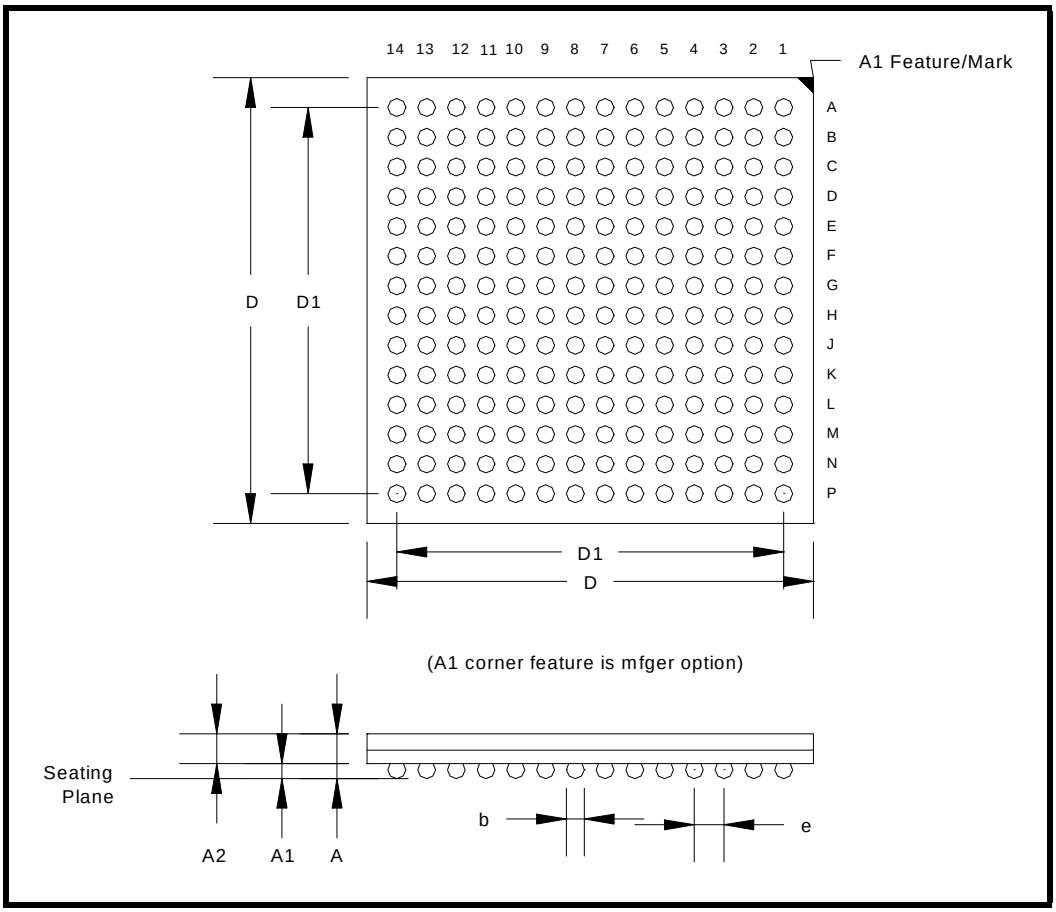
ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT91L82IB	196 Shrink Thin Ball Grid Array (15.0 mm x 15.0 mm, STBGA)	-40°C to +85°C

196 SHRINK THIN BALL GRID ARRAY

(15.0 MM X 15.0 MM, STBGA)

REV. 1.00



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.053	0.067	1.35	1.70
A1	0.010	0.022	0.25	0.55
A2	0.033	0.052	0.85	1.31
D	0.585	0.596	14.85	15.15
D1	0.512 BSC		13.00 BSC	
b	0.018	0.022	0.45	0.55
e	0.039 BSC		1.00 BSC	

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.0	November 2004	Preliminary XRT91L82 datasheet.
P1.0.1	December 2004	Fixed pin-out discrepancies.
P1.0.2	January 2005	1.Added $\overline{CS}$ de-assertion note on section 5.1. 2.Updated all registers and fixed register 0x02, 0x04, 0x05 microprocessor bit descriptions and modified several functional bit description for active low assertion and default settings. 3.Updated pin descriptions, corrected 'falling edge' typo error in section 3.6 to 'rising edge'. 4.Enhanced receive and transmit interface block diagrams and table formats in pin and microprocessor descriptions. 5.Corrected errors in Table 1 Reference Frequency Options. Removed 2.5V I/O support. 6.Remove 'RXSEL' reference on the RXIP/N pin description. 7.Minor edit in receive section 2.

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.3	March 2005	1.Moved microprocessor SDI pin from D10 to pin C10 and SCLK from D4 to pin D12. 2.Moved CP_OUT from pin F14 pin to pin F1 for Host Mode operation only. 3.Moved VCXO_IN from pin E14 to pin E4. 4.Removed IN_TERM in pin E4 to reflect enhanced internal bus termination support. 5.Added RXCAP1P and RXCAP1N/CP_OUT on pins E1 and F1 for external loop filter capacitors. 5.Added XRES1P and XRES1N LVDS biasing external resistors on pins E14 and F14. 6.Renamed RESETB, TXSCLKODIS, FIFO_RST/SCLK, REFREQSEL1, SEREF_EN, RLOOPS/PRBS_CLEAR, DLOOP, TX_SWING, TEST_MODE, PRBS_NOLOCK, RXCLKP/N, RXLCKREF, DISRD, DISRDCLK, LOSEXT pins to RESET, TXSCLKOOFF, FIFO_RST, REFREQSEL1/SCLK, SEREF_DIS, RLOOPS_PRBSCLR, DLOOP, TXSWING, PRBS_EN, PRBS_ERR, RXPCLKOP/N, RXLCKREF, DISRD, DISRDCLK, SDEXT respectively to reflect active low assertion and more precise functionality. 7.Renamed and updated bit description of VDD_3.3 to VDD_IO for 3.3V LVPECL /1.8V LVDS I/O references. 8.Updated STBGA pinout to include above mentioned changes. 9.Retouched 91L82 Block Diagram. 10.Corrected RXDO[15:0]P/N description error from 'updated on rising edge' to 'updated on falling edge' of RXPCLKOP/N. 11.Corrected PRBS_EN, FIFO_RST, TXSCLKOOFF description errors . 12.Removed unsupported note for transparent mode FIFO operation in section 3.3 and enhanced and corrected FIFO reset operation description. 13.Corrected Figure 14, "Loop Timing Mode Using an External Cleanup VCXO (Host Mode Only) 14.Added CMU and CDR performace tables. 15.Added CML input swing characteristics. 16.Added external loop filter and LVDS biasing resistor diagrams. 17.Added Data Latency in section 1.0. 18.Updated transmit and receive timing diagrams and timing table specifications. 19.Removed all references to limiting amplifier. 20.Significantly enhanced Signal Detection/LOS section description. 21.Change MHz to Mbps to reflect Parallel data I/O and Serial I/O more accurately. Corrected and enhanced PISO and SIPO diagrams. 22.Added JTAG input pin pull-up and pull-down descriptions. 23.Moved FIFO figure from sect 3.6 to section 3.3. 24.Enlarged CML output swing figure. 25.Added directional arrows for RXIP/N and TXOP/N. 26.Added place holders for jitter performance charts. 27.Reformatted AC/DC electrical characteristics tables. 28.Rearrange Pin List format and formatted Table Header shading. 29.Added cross-reference for register bits and corrected mispellings and retouched bit descriptions. 30.Updated Microprocessor Register Bits and Descriptions to reflect changes. 31.Changed OC-48 to STS-48 name.

REVISION HISTORY

REVISION #	DATE	DESCRIPTION
P1.0.4	March 2005	1.Renamed $\overline{\text{RXLCKREF}}$ to $\overline{\text{CDRLCKREF}}$ and corrected pin and microprocessor bit description. 2.Reinstated INTERM pin on E4 to support Single-Ended LVPEL in Hardware Mode and added INTERM/VCXO_IN pin description. 3.Renamed AVDD1.8_RX, AVDD1.8_TX, VDD1.8 power and VSS ground pin connections to AVDD_RX, AVDD_TX, VDD_CMOS and GND respectively. 4.Split VDD_IO to VDD_IO and VDD_O and added pin description definition requiring 1.8V potential for VDD_O in LVDS operation. 5.Added ALTFREQSEL to support lower 77.76/83.31 MHz reference clocks, INTERM, and SEREFDIS in Host Mode. 6.Corrected LOOPTM_NOJA pin and microprocessor descripton. 7.Redesigned microprocessor registers. 8.Enhanced Section 7.0 Electrical Charateristics. 9.Enhanced Figure 1, “Block Diagram of XRT91L82. 10.Updated Figure 2, “196 BGA Pinout of THE XRT91L82 (Top View). 11.Corrected typos in pin description section and Figure 5, “External Loop Filter. 12.Enhanced Section 3.6 "Clock Multiplier Unit (CMU) and Re-Timer. 13.Updated Figure 14, “Loop Timing Mode Using an External Cleanup VCXO (Host Mode Only).
P1.0.5	April 2005	1.Changed VDD_O to VDD_IO and removed 1.8V potential requirement for LVDS operation. 2.Added internal termination and biasing notes in pin descriptions. 3.Moved microprocessor $\overline{\text{INT}}$ pin from C5 to pin D10 and SDO from C6 to pin E9. 4.Corrected REFREQSEL1/SCLK pin from D5 to D12. 5.In Host Mode, Added PRBS_LOCK on pin D4. Added PRBS Lock Interrupt Enable, Status, and Detection register bits. Added PRBS inversion capability. 6.Moved PRBS Enable register bit from D3 to D4 in register 0x05h. 7.Changed ALTFREQSEL and TXSWING register bit default values to "1." 8.Corrected Transmit Parallel Interface LVDS Operation section and moved to receive section 2.7. 9.Updated Figure 14 Loop Timing Mode Using an External Cleanup VCXO. 10.Revised and Updated Electrical Characteristics section 7.0

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