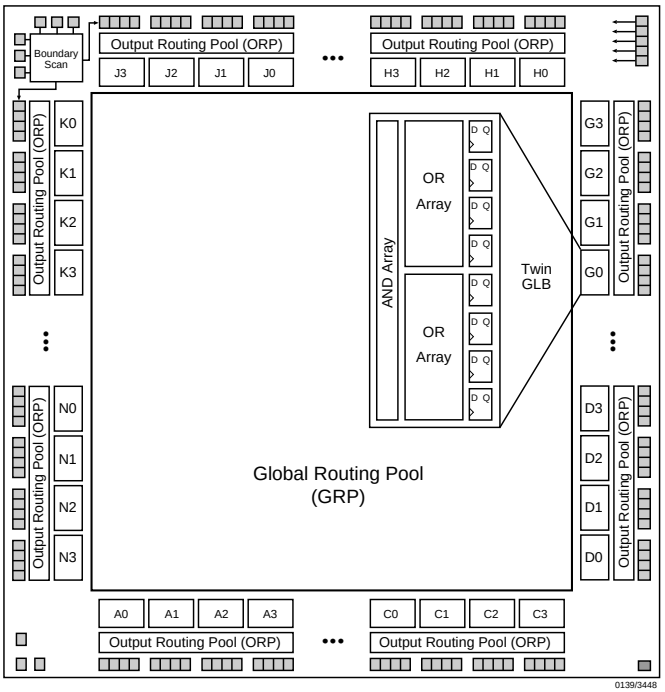
ispLSI® 3448

In-System Programmable High Density PLD

Features

- **HIGH-DENSITY PROGRAMMABLE LOGIC**
  - **— 224 I/O**
  - **— 20000 PLD Gates**
  - **— 672 Registers**
  - **— High Speed Global Interconnect**
  - **— Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.**
  - **— Small Logic Block Size for Random Logic**
- **HIGH-PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— fmax = 90 MHz Maximum Operating Frequency**
  - **— tpd = 12 ns Propagation Delay**
  - **— TTL Compatible Inputs and Outputs**
  - **— Electrically Erasable and Reprogrammable**
  - **— Non-Volatile**
  - **— 100% Tested at Time of Manufacture**
  - **— Unused Product Term Shutdown Saves Power**
- **ispLSI FEATURES:**
  - **— 5V In-System Programmable (ISP™) Using Lattice ISP or Boundary Scan Test (IEEE 1149.1) Protocol**
  - **— Increased Manufacturing Yields, Reduced Time-to-Market, and Improved Product Quality**
  - **— Reprogram Soldered Devices for Faster Debugging**
- **100% IEEE 1149.1 BOUNDARY SCAN COMPATIBLE**
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - **— Complete Programmable Device Can Combine Glue Logic and Structured Designs**
  - **— Enhanced Pin Locking Capability**
  - **— Five Dedicated Clock Inputs**
  - **— Synchronous and Asynchronous Clocks**
  - **— Programmable Output Slew Rate Control to Minimize Switching Noise**
  - **— Flexible I/O Placement**
  - **— Optimized Global Routing Pool Provides Global Interconnectivity**
- **ispDesignEXPERT™ – LOGIC COMPILER AND COMPLETE ISP DEVICE DESIGN SYSTEMS FROM HDL SYNTHESIS THROUGH IN-SYSTEM PROGRAMMING**
  - **— Superior Quality of Results**
  - **— Tightly Integrated with Leading CAE Vendor Tools**
  - **— Productivity Enhancing Timing Analyzer, Explore Tools, Timing Simulator and ispANALYZER™**
  - **— PC and UNIX Platforms**

Functional Block Diagram



Description

The ispLSI 3448 is a High-Density Programmable Logic Device containing 672 Registers, 224 Universal I/Os, five Dedicated Clock Inputs, 14 Output Routing Pools (ORP) and a Global Routing Pool (GRP) which allows complete inter-connectivity between all of these elements. The ispLSI 3448 features 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 3448 offers non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on the ispLSI 3448 device is the Twin Generic Logic Block (Twin GLB) labelled A0, A1...N3. There are a total of 56 of these Twin GLBs in the ispLSI 3448 device. Each Twin GLB has 24 inputs, a programmable AND array and two OR/Exclusive-OR Arrays, and eight outputs which can be configured to be either combinatorial or registered. All Twin GLB inputs come from the GRP.

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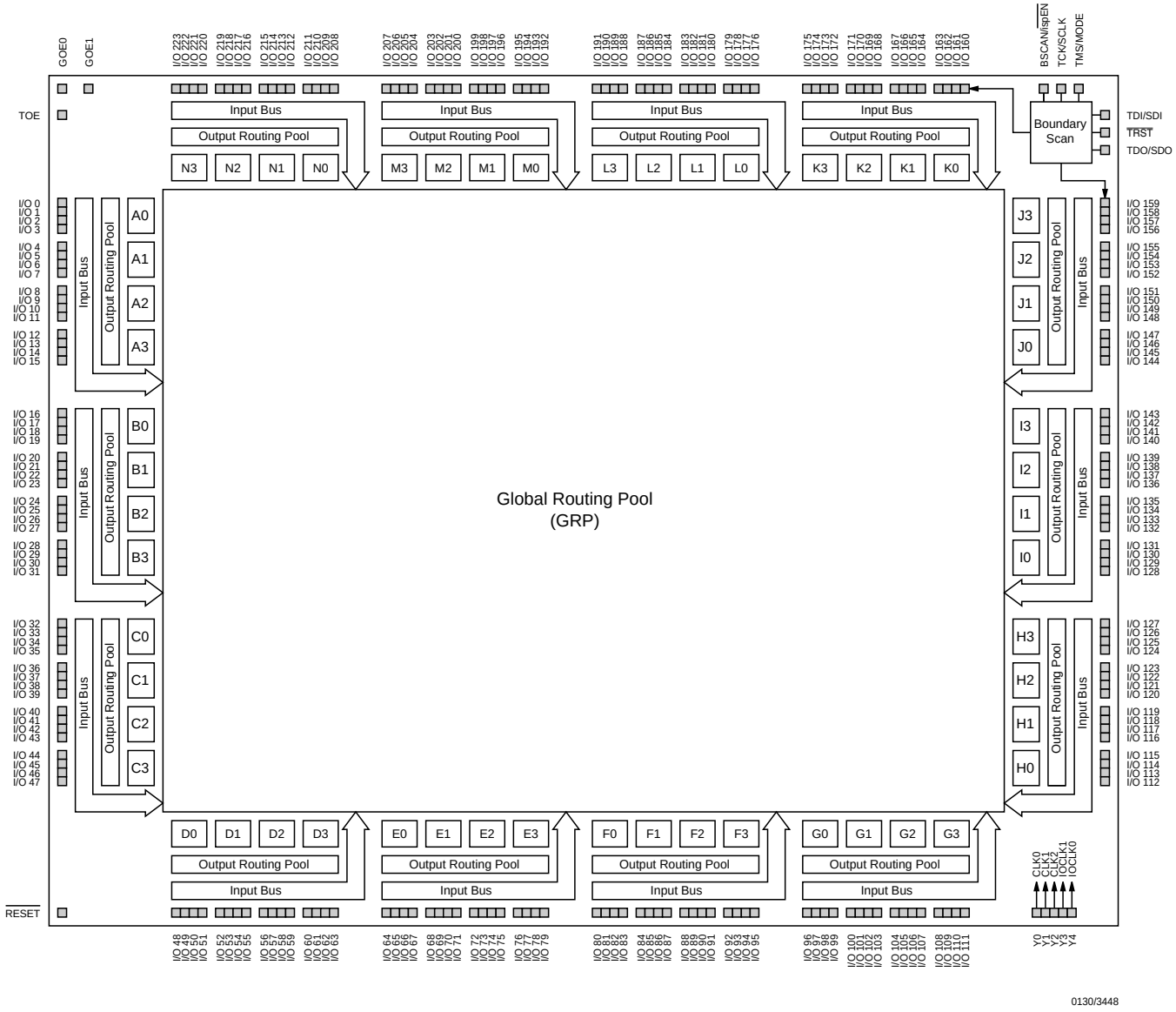
Functional Block Diagram

Figure 1. ispLSI 3448 Functional Block Diagram



Description (continued)

All local logic block outputs are brought back into the GRP so they can be connected to the inputs of any other logic block on the device. The device also has 224 I/O cells, each of which is directly connected to an I/O ball. Each I/O cell can be individually programmed to be a combinatorial input, a registered input, a latched input, an output or a bidirectional I/O with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

The 224 I/O cells are grouped into 14 sets of 16 bits. Each of these I/O groups is associated with a logic Megablock through the use of the ORP. Each Megablock is able to provide one Product Term Output Enable (PTOE) signal which is globally distributed to all I/O cells. That PTOE signal can be generated within any GLB in the Megablock. Each I/O cell can select one of 16 available OEs (two Global OEs and 14 PTOEs).

Four Twin GLBs, 16 I/O cells and one ORP are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of the four Twin GLBs are connected to a set of 16 I/O cells by the ORP. The ispLSI 3448 device contains 14 of these Megablocks.

The GRP has as its inputs the outputs from all of the Twin GLBs and all of the inputs from the bidirectional I/O cells. All of these signals are made available to the inputs of the Twin GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.

Clocks in the ispLSI 3448 device are provided through five dedicated signals. Three clocks are provided for the Twin GLBs and the remaining two clocks are provided for the I/O cells.

The table below lists key attributes of the device along with the number of resources available.

An additional feature of the ispLSI 3448 is the Boundary Scan capability, which is composed of cells connected between the on-chip system logic and the device's inputs and outputs. All I/O have associated boundary scan registers, with 3-state I/O using three boundary scan registers and inputs using one.

The ispLSI 3448 supports all IEEE 1149.1 mandatory instructions, which include BYPASS, EXTEST and SAMPLE.

Key Attributes of the ispLSI 3448

Attribute	Quantity
Twin GLBs	56
Registers	672
I/O	224
Global Clocks	5
Global OE	2
Test OE	1

Table 1-0003/3448

Absolute Maximum Ratings [1]

Supply Voltage V_{CC} ..... -0.5 to +7.0V

Input Voltage Applied ..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature ..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 140°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC} +1	V

Table 2-0005/3448

Capacitance (T_A=25°C,f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O Capacitance	10	pf	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V
C_2	Clock Capacitance	11	pf	V_{CC} = 5.0V, V_Y = 2.0V

Table 2-0006/3320

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
ispLSI Erase/Reprogram Cycles	10000	–	Cycles

Table 2-0008/3320

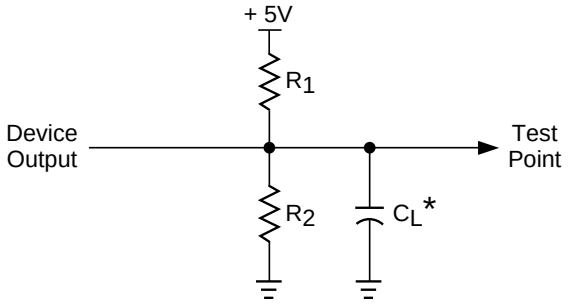
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3 ns 10% to 90%
Input Timing Reference Levels	1.5V
Ouput Timing Reference Levels	1.5V
Output Load	See Figure 2

Table 2-0003/3448

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A

Output Load conditions (See Figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} +0.5V	470Ω	390Ω	5pF

Table 2 - 0004A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)	–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	–	–	10	µA
I_{IL-isp}	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}	–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V	–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V, f_{CLOCK} = 1 MHz	–	470	–	mA

Table 2-0007/3448

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Guaranteed but not 100% tested.
2. Measured using 28 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

External Switching Characteristics[1, 2, 3]

Over Recommended Operating Conditions

PARAMETER	TEST COND.[5]	#[2]	DESCRIPTION[1]	-90		-70		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	12.0	–	15.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	15.0	–	18.0	ns
f_{max}	A	3	Clock Frequency with Internal Feedback [3]	90.0	–	70.0	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	62.5	–	50.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Maximum Toggle [4]	100	–	83.0	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	7.0	–	9.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	7.5	–	9.0	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	8.5	–	11.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	8.0	–	10.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	14.0	–	15.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	9.0	–	12.0	–	ns
t_{ptoeen}	B	14	Input to Output Enable	–	25.0	–	30.0	ns
$t_{ptoedis}$	C	15	Input to Output Disable	–	25.0	–	30.0	ns
t_{goeen}	B	16	Global OE Output Enable	–	10.0	–	12.0	ns
t_{goedis}	C	17	Global OE Output Disable	–	10.0	–	12.0	ns
t_{toeen}	B	18	Test OE Output Enable	–	13.0	–	15.0	ns
t_{toedis}	C	19	Test OE Output Disable	–	13.0	–	15.0	ns
t_{wh}	–	20	Ext. Synchronous Clock Pulse Duration, High	5.0	–	6.0	–	ns
t_{wl}	–	21	Ext. Synchronous Clock Pulse Duration, Low	5.0	–	6.0	–	ns
t_{su3}	–	22	I/O Reg Setup Time before Ext. Synchronous Clock (Y3, Y4)	4.5	–	5.0	–	ns
t_{h3}	–	23	I/O Reg Hold Time after Ext. Sync Clock (Y3, Y4)	0.0	–	0.0	–	ns

Table 2-0030/3320

1. Unless noted otherwise, all parameters use 20 PTXOR path and ORP.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. f_{max} (Toggle) may be less than $1/(t_{wh} + t_{wl})$. This is to allow for a clock duty cycle of other than 50%.
5. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-90		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{iobp}	24	I/O Register Bypass	–	2.3	–	3.2	ns
t_{iolat}	25	I/O Latch Delay	–	14.0	–	18.2	ns
t_{iosu}	26	I/O Register Setup Time before Clock	7.5	–	9.0	–	ns
t_{ioh}	27	I/O Register Hold Time after Clock	-3.0	–	-4.0	–	ns
t_{ioco}	28	I/O Register Clock to Out Delay	–	8.3	–	10.2	ns
t_{ior}	29	I/O Register Reset to Out Delay	–	8.3	–	10.2	ns
GRP							
t_{grp}	30	GRP Delay	–	3.2	–	3.5	ns
$t_{feedback}$	31	Feedback Delay	–	1.0	–	1.6	ns
GLB							
t_{4ptbp}	32	4 Product Term Bypass Path Delay (Comb.)	–	4.0	–	5.3	ns
t_{4ptbr}	33	4 Product Term Bypass Path Delay (Reg.)	–	3.5	–	3.8	ns
t_{1ptxor}	34	1 Product Term/XOR Path Delay	–	5.0	–	5.8	ns
$t_{20ptxor}$	35	20 Product Term/XOR Path Delay	–	5.0	–	5.8	ns
t_{xoradj}	36	XOR Adjacent Path Delay[3]	–	6.2	–	7.3	ns
t_{gbp}	37	GLB Register Bypass Delay	–	0.5	–	0.5	ns
t_{gsu}	38	GLB Register Setup Time before Clock	1.5	–	2.5	–	ns
t_{gh}	39	GLB Register Hold Time after Clock	5.4	–	6.3	–	ns
t_{gco}	40	GLB Register Clock to Output Delay	–	0.5	–	1.0	ns
t_{gro}	41	GLB Register Reset to Output Delay	–	1.0	–	1.0	ns
t_{ptre}	42	GLB Product Term Reset to Register Delay	–	8.9	–	10.5	ns
t_{ptoe}	43	GLB Product Term Output Enable to I/O Cell Delay	–	15.0	–	18.3	ns
t_{ptck}	44	GLB Product Term Clock Delay	3.7	3.7	4.5	4.5	ns
ORP							
t_{orp}	45	ORP Delay	–	1.5	–	2.0	ns
t_{orpbp}	46	ORP Bypass Delay	–	0.0	–	0.0	ns

Table 2-0036/3448

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Internal Timing Parameters[1]

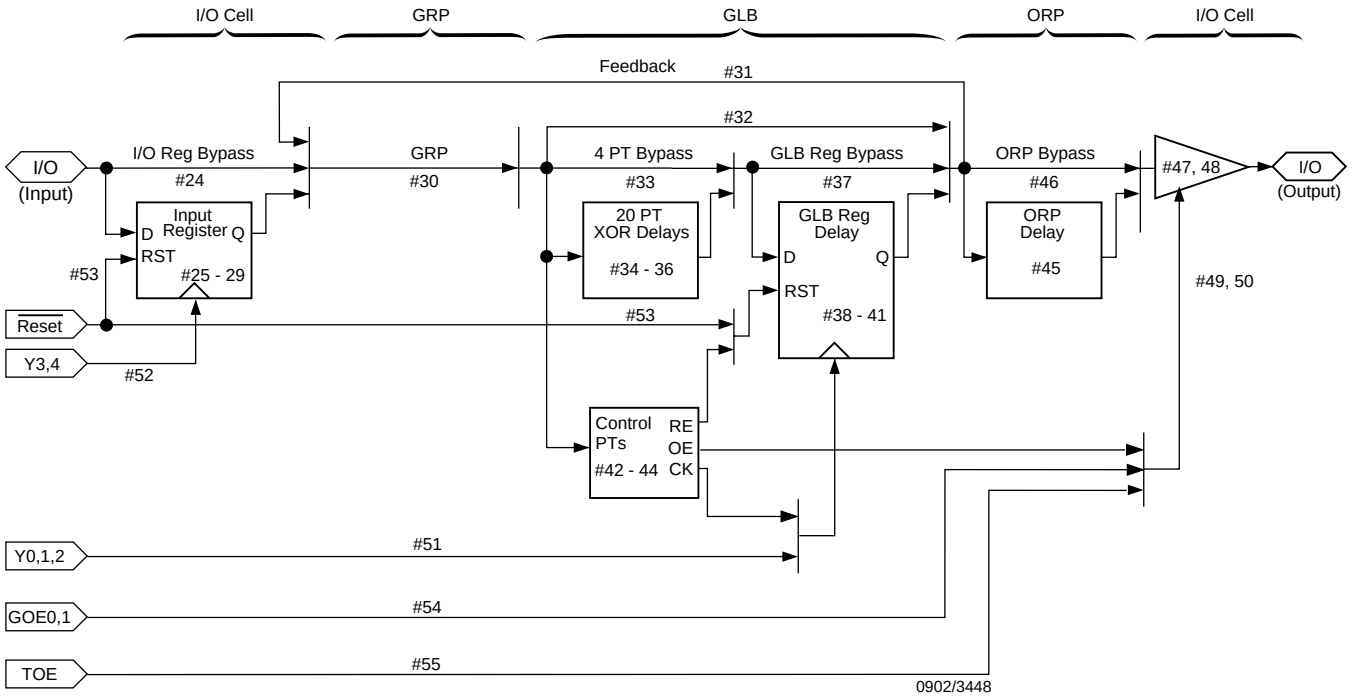
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-90		-70		UNITS
			MIN.	MAX.	MIN.	MAX.	
Outputs							
t_{ob}	47	Output Buffer Delay	–	2.5	–	3.0	ns
t_{obs}	48	Output Buffer Delay, Slew Limited Adder	–	13.0	–	13.0	ns
t_{oen}	49	I/O Cell OE to Output Enabled	–	4.5	–	5.0	ns
t_{odis}	50	I/O Cell OE to Output Disabled	–	4.5	–	5.0	ns
Clocks							
$t_{gy0/1/2}$	51	Clock Delay, Y0 or Y1 or Y2 to Global GLB Clock Line	3.5	3.5	4.0	4.0	ns
$t_{ioy3/4}$	52	Clock Delay, Y3 or Y4 to I/O Cell Global Clock Line	3.0	3.0	4.0	4.0	ns
Global Reset							
t_{gr}	53	Global Reset to GLB and I/O Registers	–	9.0	–	9.0	ns
t_{goe}	54	Global OE Pad Buffer	–	5.5	–	7.0	ns
t_{toe}	55	Test OE Pad Buffer	–	8.5	–	10.0	ns

Table 2-0037/3448

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.

ispLSI 3448 Timing Model



Derivations of tsu, th and tco from the Product Term Clock[1]

tsu	=	Logic + Reg su - Clock (min)
	=	(**t**iobp + **t**grp + **t**20ptxor) + (**t**gsu) - (**t**iobp + **t**grp + **t**ptck(min))
	=	(#24+ #30+ #35) + (#38) - (#24+ #30+ #44)
2.8 ns	=	(2.3 + 3.2 + 5.0) + (1.5) - (2.3 + 3.2 + 3.7)
th	=	Clock (max) + Reg h - Logic
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gh) - (**t**iobp + **t**grp + **t**20ptxor)
	=	(#24+ #30+ #44) + (#39) - (#24+ #30+ #35)
4.1 ns	=	(2.3 + 3.2 + 3.7) + (5.4) - (2.3 + 3.2 + 5.0)
tco	=	Clock (max) + Reg co + Output
	=	(**t**iobp + **t**grp + **t**ptck(max)) + (**t**gco) + (**t**orp + **t**ob)
	=	(#24 + #30 + #44) + (#40) + (#45 + #47)
13.7 ns	=	(2.3 + 3.2 + 3.7) + (0.5) + (1.5 + 2.5)

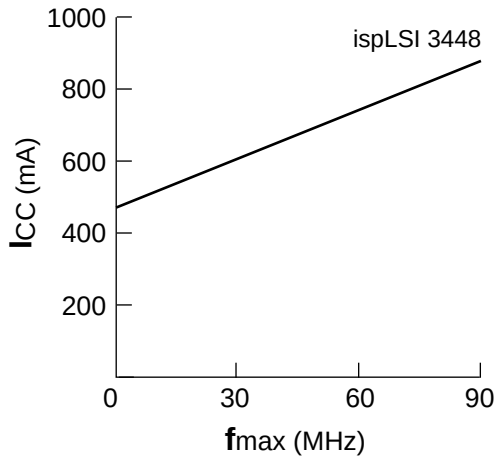
Table 2-0042/3448

Note: Calculations are based on timing specs for the ispLSI 3448-90L.

Power Consumption

Power consumption in the ispLSI 3448 device depends on two primary factors: the speed at which the device is operating and the number of product terms used. Figure 3 shows the relationship between power and operating speed.

Figure 3. Typical Device Power Consumption vs fmax



Notes: Configuration of 28 16-bit Counters
Typical Current at 5V, 25° C

I_{CC} can be estimated for the ispLSI 3448 using the following equation:

I_{CC} = 60 + (# of PTs * 0.46) + (# of nets * Max. freq * 0.01) where:
# of PTs = Number of Product Terms used in design
# of nets = Number of Signals used in device
Max. freq = Highest Clock Frequency to the device

The I_{CC} estimate is based on typical conditions (V_{CC} = 5.0V, room temperature) and an assumption of two GLB loads on average exists. These values are for estimates only. Since the value of I_{CC} is sensitive to operating conditions and the program in the device, the actual I_{CC} should be verified.

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Signal Description

Signal Name	Description
I/O	Input/Output – These are the general purpose I/O used by the logic array.
GOE0, GOE1	Global Output Enable inputs.
TOE	Test Output Enable pin – This pin tristates all I/O pins when a logic low is driven.
$\overline{\text{RESET}}$	Active Low (0) Reset which resets all of the GLB and I/O registers in the device.
Y0, Y1, Y2	Dedicated Clock inputs connect to one of the clock inputs of all the GLBs on the device.
Y3, Y4	Dedicated Clock inputs connect to one of the clock inputs of all the I/O cells on the device.
BSCAN/$\overline{\text{ispEN}}$	Input – Dedicated in-system programming enable input. When this is high, the BSCAN TAP controller signals TMS, TDI, TDO and TCK are enabled. When this is brought low, the ISP State Machine control signals MODE, SDI, SDO and SLCK are enabled. High-to-low transition will put the device in the programming mode and put all I/O in the high-Z state.
TDI/SDI	Input – This signal performs two functions. It is the Test Data input signal when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as an input to load programming data into the device. SDI is also used as one of the two control signals for the ISP State Machine.
TCK/SCLK	Input – This signal performs two functions. It is the Test Clock input signal when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it functions as a clock signal for the Serial Shift Register.
TMS/MODE	Input – This signal performs two functions. It is the Test Mode Select input signal when $\overline{\text{ispEN}}$ is logic high. When $\overline{\text{ispEN}}$ is logic low, it controls the operation of the ISP State Machine.
$\overline{\text{TRST}}$	Input – Test Reset, active low to reset the Boundary Scan State Machine.
TDO/SDO	Output – This signal performs two functions. When $\overline{\text{ispEN}}$ is logic low, it reads the ISP data. When $\overline{\text{ispEN}}$ is high, it functions as Test Data Out.
GND	Ground (GND)
VCC	Vcc
NC[1]	No Connect.

Signal Locations

Signal	432-Ball BGA
GOE0, GOE1	R2, W1
TOE	H3
$\overline{\text{RESET}}$	AA31
Y0, Y1, Y2, Y3, Y4	U30, N31, L1, AB3, AF1
BSCAN/$\overline{\text{ispEN}}$	AD29
TDI/SDI	K29
TCK/SCLK	AG29
TMS/MODE	F31
$\overline{\text{TRST}}$	E3
TDO/SDO	AH3
GND	A1, A2, A16, A30, A31, B1, B5, B9, B13, B19, B23, B27, B31, E2, E30, J2, J30, N2, N30, T1, T31, W2, W30, AC2, AC30, AG2, AG30, AK1, AK5, AK9, AK13, AK19, AK23, AK27, AK31, AL1, AL2, AL16, AL30, AL31
VCC	A3, A10, A22, A29, B14, B18, C1, C31, K1, K31, P2, P30, V2, V30, AB1, AB31, AJ1, AJ31, AK14, AK18, AL3, AL10, AL22, AL29
NC[1]	B2, B3, B30, C3, C7, C11, C14, C18, C21, C25, C29, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27, D28, E4, E28, F4, F28, G3, G4, G28, G29, H4, H28, J4, J28, K4, K28, L3, L4, L28, L29, M4, M28, N4, N28, P3, P4, P28, P29, R4, R28, T4, T28, U4, U28, V3, V4, V28, V29, W4, W28, Y4, Y28, AA3, AA4, AA28, AA29, AB4, AB28, AC4, AC28, AD4, AD28, AE3, AE4, AE28, AE29, AF4, AF28, AG4, AG28, AH4, AH5, AH6, AH7, AH8, AH9, AH10, AH11, AH12, AH13, AH14, AH15, AH16, AH17, AH18, AH19, AH20, AH21, AH22, AH23, AH24, AH25, AH26, AH27, AH28, AJ3, AJ7, AJ11, AJ14, AJ18, AJ21, AJ25, AJ29, AK2, AK30

1. NCs are not to be connected to any active signals, VCC or GND.

I/O Locations

Signal	BGA	Signal	BGA	Signal	BGA	Signal	BGA	Signal	BGA	Signal	BGA
I/O 0	T30	I/O 38	AK24	I/O 76	AK7	I/O 114	R1	I/O 152	A9	I/O 190	C26
I/O 1	U29	I/O 39	AL24	I/O 77	AL6	I/O 115	P1	I/O 153	C10	I/O 191	A27
I/O 2	U31	I/O 40	AJ23	I/O 78	AK6	I/O 116	N1	I/O 154	B10	I/O 192	A28
I/O 3	V31	I/O 41	AL23	I/O 79	AJ6	I/O 117	N3	I/O 155	B11	I/O 193	C27
I/O 4	W31	I/O 42	AJ22	I/O 80	AL5	I/O 118	M1	I/O 156	A11	I/O 194	B28
I/O 5	W29	I/O 43	AK22	I/O 81	AL4	I/O 119	M2	I/O 157	C12	I/O 195	B29
I/O 6	Y31	I/O 44	AK21	I/O 82	AJ5	I/O 120	M3	I/O 158	B12	I/O 196	C28
I/O 7	Y30	I/O 45	AL21	I/O 83	AK4	I/O 121	L2	I/O 159	A12	I/O 197	D29
I/O 8	Y29	I/O 46	AJ20	I/O 84	AK3	I/O 122	K2	I/O 160	C13	I/O 198	C30
I/O 9	AA30	I/O 47	AK20	I/O 85	AJ4	I/O 123	K3	I/O 161	A13	I/O 199	D30
I/O 10	AB30	I/O 48	AL20	I/O 86	AJ2	I/O 124	J1	I/O 162	A14	I/O 200	E29
I/O 11	AB29	I/O 49	AJ19	I/O 87	AH2	I/O 125	J3	I/O 163	C15	I/O 201	D31
I/O 12	AC31	I/O 50	AL19	I/O 88	AG3	I/O 126	H1	I/O 164	B15	I/O 202	E31
I/O 13	AC29	I/O 51	AL18	I/O 89	AH1	I/O 127	H2	I/O 165	A15	I/O 203	F29
I/O 14	AD31	I/O 52	AJ17	I/O 90	AG1	I/O 128	G1	I/O 166	C16	I/O 204	F30
I/O 15	AD30	I/O 53	AK17	I/O 91	AF3	I/O 129	G2	I/O 167	B16	I/O 205	G30
I/O 16	AE31	I/O 54	AL17	I/O 92	AF2	I/O 130	F1	I/O 168	C17	I/O 206	G31
I/O 17	AE30	I/O 55	AJ16	I/O 93	AE2	I/O 131	F2	I/O 169	B17	I/O 207	H29
I/O 18	AF31	I/O 56	AK16	I/O 94	AE1	I/O 132	F3	I/O 170	A17	I/O 208	H30
I/O 19	AF30	I/O 57	AJ15	I/O 95	AD3	I/O 133	E1	I/O 171	A18	I/O 209	H31
I/O 20	AF29	I/O 58	AK15	I/O 96	AD2	I/O 134	D1	I/O 172	A19	I/O 210	J29
I/O 21	AG31	I/O 59	AL15	I/O 97	AD1	I/O 135	D2	I/O 173	C19	I/O 211	J31
I/O 22	AH31	I/O 60	AL14	I/O 98	AC3	I/O 136	C2	I/O 174	A20	I/O 212	K30
I/O 23	AH30	I/O 61	AL13	I/O 99	AC1	I/O 137	D3	I/O 175	B20	I/O 213	L30
I/O 24	AJ30	I/O 62	AJ13	I/O 100	AB2	I/O 138	C4	I/O 176	C20	I/O 214	L31
I/O 25	AH29	I/O 63	AL12	I/O 101	AA2	I/O 139	B4	I/O 177	A21	I/O 215	M29
I/O 26	AJ28	I/O 64	AK12	I/O 102	AA1	I/O 140	C5	I/O 178	B21	I/O 216	M30
I/O 27	AK29	I/O 65	AJ12	I/O 103	Y3	I/O 141	A4	I/O 179	B22	I/O 217	M31
I/O 28	AK28	I/O 66	AL11	I/O 104	Y2	I/O 142	A5	I/O 180	C22	I/O 218	N29
I/O 29	AJ27	I/O 67	AK11	I/O 105	Y1	I/O 143	C6	I/O 181	A23	I/O 219	P31
I/O 30	AL28	I/O 68	AK10	I/O 106	W3	I/O 144	B6	I/O 182	C23	I/O 220	R29
I/O 31	AL27	I/O 69	AJ10	I/O 107	V1	I/O 145	A6	I/O 183	A24	I/O 221	R30
I/O 32	AJ26	I/O 70	AL9	I/O 108	U3	I/O 146	B7	I/O 184	B24	I/O 222	R31
I/O 33	AK26	I/O 71	AJ9	I/O 109	U2	I/O 147	A7	I/O 185	C24	I/O 223	T29
I/O 34	AL26	I/O 72	AL8	I/O 110	U1	I/O 148	C8	I/O 186	A25		
I/O 35	AK25	I/O 73	AK8	I/O 111	T3	I/O 149	B8	I/O 187	B25		
I/O 36	AL25	I/O 74	AJ8	I/O 112	T2	I/O 150	A8	I/O 188	A26		
I/O 37	AJ24	I/O 75	AL7	I/O 113	R3	I/O 151	C9	I/O 189	B26		

Signal Configuration

ispLSI 3448 432-Ball BGA Signal Diagram

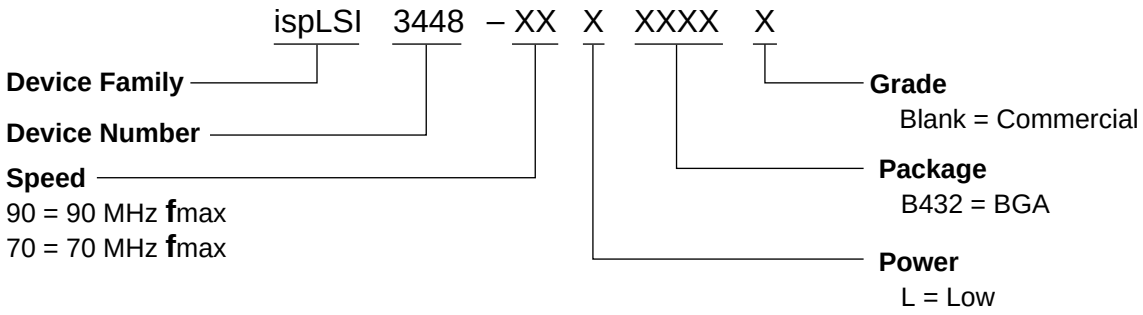
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	GND	VCC	I/O 192	I/O 191	I/O 188	I/O 186	I/O 183	I/O 181	VCC	I/O 177	I/O 174	I/O 172	I/O 171	I/O 170	GND	I/O 165	I/O 162	I/O 161	I/O 159	I/O 156	VCC	I/O 152	I/O 150	I/O 147	I/O 145	I/O 142	I/O 141	VCC	GND	GND	A
B	GND	NC[1]	I/O 195	I/O 194	GND	I/O 189	I/O 187	I/O 184	GND	I/O 179	I/O 178	I/O 175	GND	VCC	I/O 169	I/O 167	I/O 164	VCC	GND	I/O 158	I/O 155	I/O 154	GND	I/O 149	I/O 146	I/O 144	GND	I/O 139	NC[1]	NC[1]	GND	B
C	VCC	I/O 198	NC[1]	I/O 196	I/O 193	I/O 190	NC[1]	I/O 185	I/O 182	I/O 180	NC[1]	I/O 176	I/O 173	NC[1]	I/O 168	I/O 166	I/O 163	NC[1]	I/O 160	I/O 157	NC[1]	I/O 153	I/O 151	I/O 148	NC[1]	I/O 143	I/O 140	I/O 138	NC[1]	I/O 136	VCC	C
D	I/O 201	I/O 199	I/O 197	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	I/O 137	I/O 135	I/O 134	D
E	I/O 202	GND	I/O 200	NC[1]																								NC[1]	TRST	GND	I/O 133	E
F	MODE/ TMS	I/O 204	I/O 203	NC[1]																								NC[1]	I/O 132	I/O 131	I/O 130	F
G	I/O 206	I/O 205	NC[1]	NC[1]																								NC[1]	NC[1]	I/O 129	I/O 128	G
H	I/O 209	I/O 208	I/O 207	NC[1]																								NC[1]	TOE	I/O 127	I/O 126	H
J	I/O 211	GND	I/O 210	NC[1]																								NC[1]	I/O 125	GND	I/O 124	J
K	VCC	I/O 212	TDI/ SDI	NC[1]																								NC[1]	I/O 123	I/O 122	VCC	K
L	I/O 214	I/O 213	NC[1]	NC[1]																								NC[1]	NC[1]	I/O 121	Y2	L
M	I/O 217	I/O 216	I/O 215	NC[1]																								NC[1]	I/O 120	I/O 119	I/O 118	M
N	Y1	GND	I/O 218	NC[1]																								NC[1]	I/O 117	GND	I/O 116	N
P	I/O 219	VCC	NC[1]	NC[1]																								NC[1]	NC[1]	VCC	I/O 115	P
R	I/O 222	I/O 221	I/O 220	NC[1]																								NC[1]	I/O 113	GOE 0	I/O 114	R
T	GND	I/O 0	I/O 223	NC[1]																								NC[1]	I/O 111	I/O 112	GND	T
U	I/O 2	Y0	I/O 1	NC[1]																								NC[1]	I/O 108	I/O 109	I/O 110	U
V	I/O 3	VCC	NC[1]	NC[1]																								NC[1]	NC[1]	VCC	I/O 107	V
W	I/O 4	GND	I/O 5	NC[1]																								NC[1]	I/O 106	GND	GOE 1	W
Y	I/O 6	I/O 7	I/O 8	NC[1]																								NC[1]	I/O 103	I/O 104	I/O 105	Y
AA	RESET	I/O 9	NC[1]	NC[1]																								NC[1]	NC[1]	I/O 101	I/O 102	AA
AB	VCC	I/O 10	I/O 11	NC[1]																								NC[1]	Y3	I/O 100	VCC	AB
AC	I/O 12	GND	I/O 13	NC[1]																								NC[1]	I/O 98	GND	I/O 99	AC
AD	I/O 14	I/O 15	ispEN/ BSCAN	NC[1]																								NC[1]	I/O 95	I/O 96	I/O 97	AD
AE	I/O 16	I/O 17	NC[1]	NC[1]																								NC[1]	NC[1]	I/O 93	I/O 94	AE
AF	I/O 18	I/O 19	I/O 20	NC[1]																								NC[1]	I/O 91	I/O 92	Y4	AF
AG	I/O 21	GND	TCK/ SCLK	NC[1]																								NC[1]	I/O 88	GND	I/O 90	AG
AH	I/O 22	I/O 23	I/O 25	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	NC[1]	TDO/ SDO	I/O 87	I/O 89	AH
AJ	VCC	I/O 24	NC[1]	I/O 26	I/O 29	I/O 32	NC[1]	I/O 37	I/O 40	I/O 42	NC[1]	I/O 46	I/O 49	NC[1]	I/O 52	I/O 55	I/O 57	NC[1]	I/O 62	I/O 65	NC[1]	I/O 69	I/O 71	I/O 74	NC[1]	I/O 79	I/O 82	I/O 85	NC[1]	I/O 86	VCC	AJ
AK	GND	NC[1]	I/O 27	I/O 28	GND	I/O 33	I/O 35	I/O 38	GND	I/O 43	I/O 44	I/O 47	GND	VCC	I/O 53	I/O 56	I/O 58	VCC	GND	I/O 64	I/O 67	I/O 68	GND	I/O 73	I/O 76	I/O 78	GND	I/O 83	I/O 84	NC[1]	GND	AK
AL	GND	GND	VCC	I/O 30	I/O 31	I/O 34	I/O 36	I/O 39	I/O 41	VCC	I/O 45	I/O 48	I/O 50	I/O 51	I/O 54	GND	I/O 59	I/O 60	I/O 61	I/O 63	I/O 66	VCC	I/O 70	I/O 72	I/O 75	I/O 77	I/O 80	I/O 81	VCC	GND	GND	AL
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

ispLSI 3448
Bottom View

1. NCs are not to be connected to any active signals, VCC or GND.

Note: Ball A1 indicator dot on top side of package.

Part Number Description



0212/3448

Ordering Information

COMMERCIAL

FAMILY	fmax (MHz)	tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	90	12	ispLSI 3448-90LB432	432-Ball BGA
	70	15	ispLSI 3448-70LB432	432-Ball BGA

Table 2-0041/3448