

PERFORMANCE PLASTIC PACKAGE ULTRA MINIATURE PURE SILICON™ CLOCK OSCILLATORS

ASDMP



2.5 x 2.0 x 0.85 mm

ASDMP Series

Moisture Sensitivity Level – MSL 1



RoHS
Compliant

FEATURES:

- Ultra Miniature Pure Silicon™ Clock Oscillator
- High Performance MEMS Technology by Discera
- Low Power Consumption for high speed communication
- Exceptional Stability Over Temp. at -40 to +85°C, ±15ppm
- Extended Automotive Grade Temp. stability at -55 to +125°C, ±25ppm
- Available in 50kG Shock Resistance Configuration upon request
- MIL-STD-883 shock and vibration compliant
- Durable QFN Plastic Compact Packaging
- Standby or Disable Tri-state function
- Low jitter (Period jitter RMS and Phase jitter RMS)
- High power supply noise reduction, -50dBc

APPLICATIONS:

- Storage Area Networks (SATA, SAS, Fiber Channel)
- Passive Optical Networks (EPON, 10G-EPON, GPON, 10G-PON)
- Ethernet (1G, 10GBASE-T/KR/LR/SR, FCoE)
- HD/SD/SDI Video & Surveillance
- PCI Express
- Display port

STANDARD SPECIFICATIONS:

Common Key Electrical Specifications – CMOS, LVPECL, LVDS, and HCSL

Parameters	Minimum	Typical	Maximum	Units	Notes	
Frequency Range	CMOS	10.000	-----	170.000	MHz	Commercial, Industrial Temp range
	CMOS	10.000	-----	100.000		Automotive -55 ~ +125°C
	LVPECL	10.000	-----	460.000		Commercial, Industrial Temp range
	LVDS	10.000	-----	460.000		Commercial, Industrial Temp range
	HCSL	10.000	-----	460.000		Commercial, Industrial Temp range
Operating Temperature	-20	-----	+70	°C	See options	
Storage Temperature	-55	-----	+150	°C		
Overall Frequency Stability	-50	-----	+50	ppm	See options	
Supply Voltage (V _{dd})	+2.25	-----	+3.6	V		
Startup Time	-----	-----	5	ms		
Enable Time	-----	-----	20	ns	STD (Tri-state)	
	-----	-----	5	ms	PD option (Power Down)	
Disable Time	-----	-----	5	ns		
Stand-by Current	-----	20	22	mA	STD (Tri-state)	
Disable Current	-----	-----	0.095		PD option (Power Down)	
Tri-state Function (Standby/Disable)	"1" (VIH ≥ 0.75*V _{dd}) or Open: Oscillation "0" (VIL < 0.25*V _{dd}) : Hi Z			V	40kΩ pull-up resistor embedded	
Aging	-5.0	-----	+5.0	ppm	First year	

Key Electrical Specifications – CMOS

Parameters	Minimum	Typical	Maximum	Units	Notes
Supply Current (I _{dd})	-----	31	35	mA	CL=15pF, 125MHz
Output Logic Level	V _{OH}	0.9*V _{dd}	-----	V	I _F =±6mA
	V _{OL}	-----	0.1*V _{dd}	V	
Rise Time	-----	1.1	2.0	ns	CL=15pF 20%/80%*VDD
Fall Time	-----	1.3	2.0	ns	
Duty Cycle	45	-----	55	%	
Integrated Phase Jitter (J _{PH})	-----	0.30	2	ps	200kHz ~ 20MHz@125MHz
	-----	0.38	2		100kHz ~ 20MHz@125MHz
	-----	1.70	2		12kHz ~ 20MHz@125MHz
Period Jitter RMS (J _{PER})	-----	3.0	-----	ps	

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Key Electrical Specifications – LVPECL

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current (I_{dd})		-----	56.5	58	mA	RL=50Ω
Output Logic Level	V_{OH}	$V_{dd}-1.08$	-----	-----	V	RL=50Ω
	V_{OL}	-----	-----	$V_{dd}-1.55$	V	
Peak to Peak Output Swing (V_{pp})		-----	800	-----	mV	Single ended
Rise Time	T_r	-----	250	-----	ps	RL=50Ω , CL=0pF 20%/80%*VDD
Fall Time	T_f	-----	250	-----		
Duty Cycle		48	-----	52	%	Differential
Integrated Phase Jitter (J_{PH})		-----	0.25	2	ps	200kHz ~ 20MHz @156.25MHz
		-----	0.38	2		100kHz ~ 20MHz @156.25MHz
		-----	1.70	2		12kHz ~ 20MHz @156.25MHz
Period Jitter RMS (J_{PER})		-----	2.5	-----	ps	

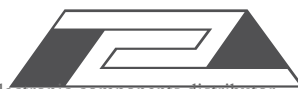
Key Electrical Specifications – LVDS

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current (I_{dd})		-----	29	32	mA	RL=100Ω
Output Offset Voltage (V_{OS})		1.125	-----	1.4	V	RL=100Ω differential
Delta Offset Voltage (ΔV_{OS})		-----	-----	50	mV	
Peak to Peak Output Swing (V_{pp})		-----	350	-----	mV	Single ended
Rise Time	T_r	-----	200	-----	ps	RL=50Ω , CL=2pF 20%/80%*VDD
Fall Time	T_f	-----	200	-----		
Duty Cycle		48	-----	52	%	Differential
Integrated Phase Jitter (J_{PH})		-----	0.28	2	ps	200kHz ~ 20MHz @156.25MHz
		-----	0.40	2		100kHz ~ 20MHz @156.25MHz
		-----	1.70	2		12kHz ~ 20MHz @156.25MHz
Period Jitter RMS (J_{PER})		-----	2.5	-----	ps	

Key Electrical Specifications – HCSL

Parameters		Minimum	Typical	Maximum	Units	Notes
Supply Current (I_{dd})		-----	40	42	mA	RL=50Ω
Output Logic Level	V_{OH}	0.725	-----	-----	V	RL=50Ω
	V_{OL}	-----	-----	0.1	V	
Peak to Peak Output Swing (V_{pp})		-----	750	-----	mV	Single ended
Rise Time	T_r	200	-----	400	ps	RL=50Ω , CL=2pF 20%/80%*VDD
Fall Time	T_f	200	-----	400		
Duty Cycle		48	-----	52	%	Differential
Integrated Phase Jitter (J_{PH})		-----	0.25	2	ps	200kHz ~ 20MHz @156.25MHz
		-----	0.37	2		100kHz ~ 20MHz @156.25MHz
		-----	1.70	2		12kHz ~ 20MHz @156.25MHz
Period Jitter RMS (J_{PER})		-----	2.5	-----	ps	

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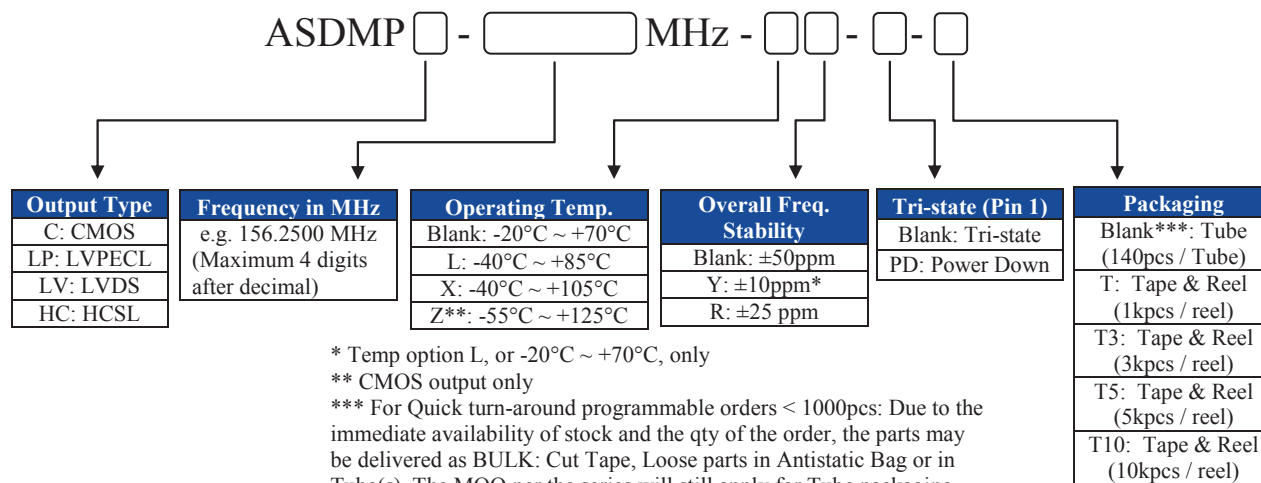


Absolute Maximum Ratings

Item	Minimum	Maximum	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	V _{dd} +0.3	V	
Junction Temp.	-----	+150	°C	
Storage Temp.	-55	+150	°C	
Soldering Temp.	-----	+260	°C	40sec max
ESD			V	
HBM		4,000		
MM		400		
CDM		1,500		

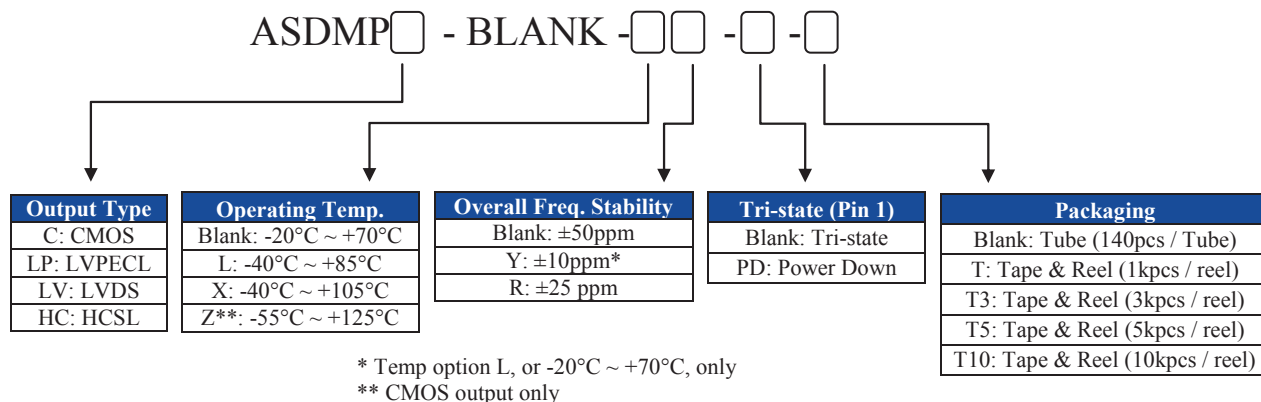
PART IDENTIFICATIONS:

Programmed Orders (Quantity > 1,000pcs)

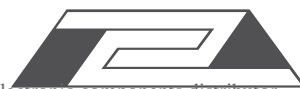


4.0.2 Un-Programmed Orders

Blank un-programmed oscillators and our low cost portable programmer are available for quick turn engineering requirements. Please call ABRACON or visit MEMSpeed Pro II site <http://www.abracon.com/memspeedpro/MEMSpeedProFlyerII.pdf> for more information.



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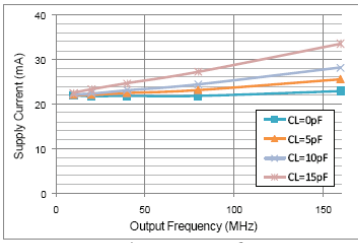
2.5 x 2.0 x 0.85 mm



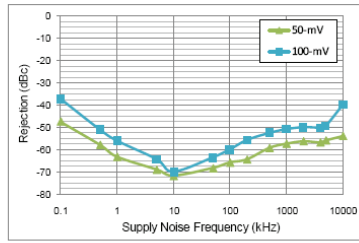
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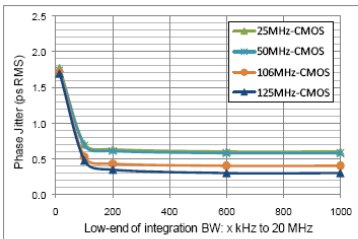
CMOS OUTPUT:



Supply current over freq

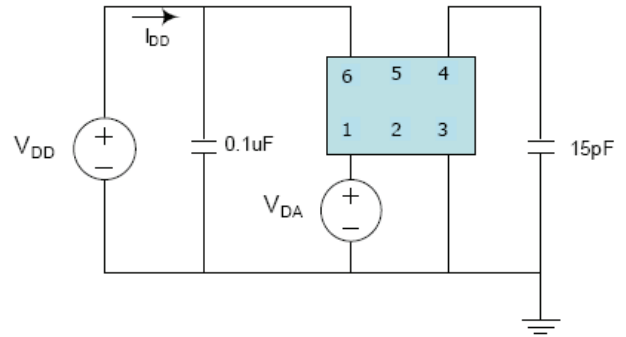


Power supply rejection ratio

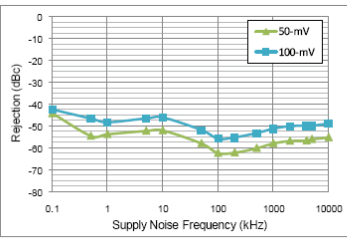


Phase jitter (integrated phase noise)

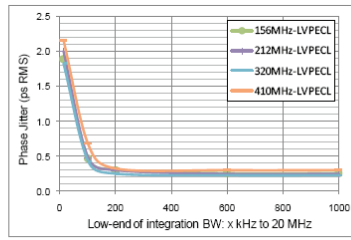
TEST CIRCUIT:



LVPECL OUTPUT:

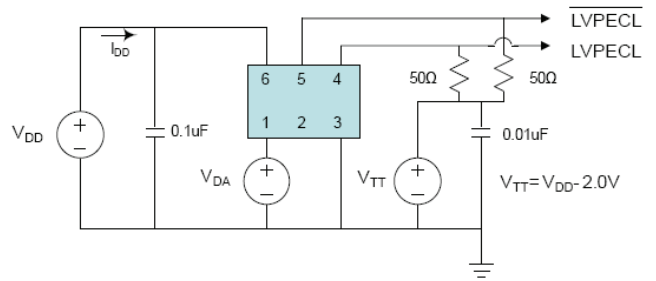


Power supply rejection ratio

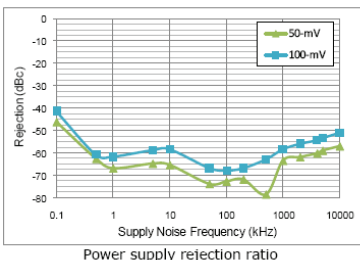


Phase jitter (integrated phase noise)

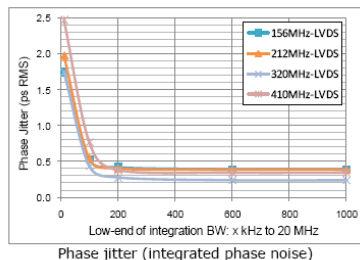
TEST CIRCUIT:



LVDS OUTPUT:

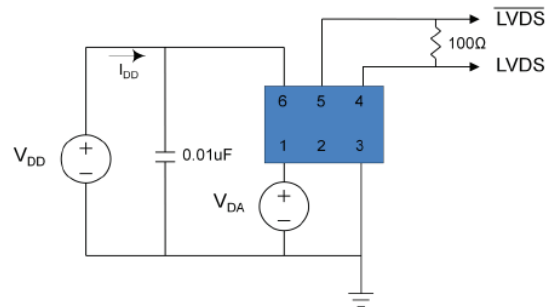


Power supply rejection ratio

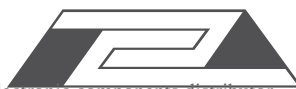


Phase jitter (integrated phase noise)

TEST CIRCUIT:



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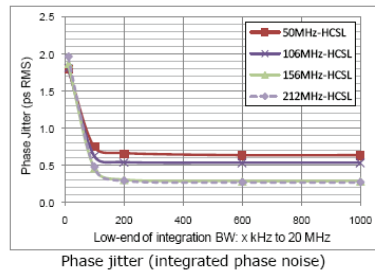
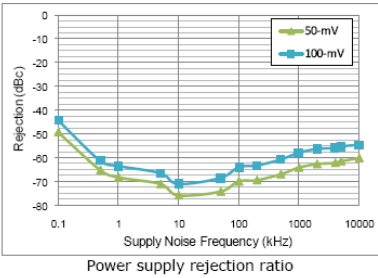


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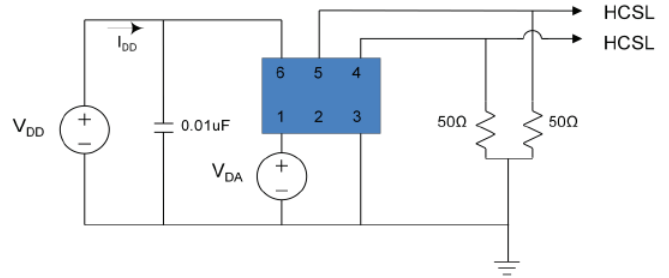
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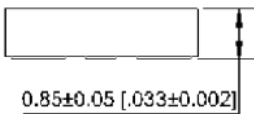
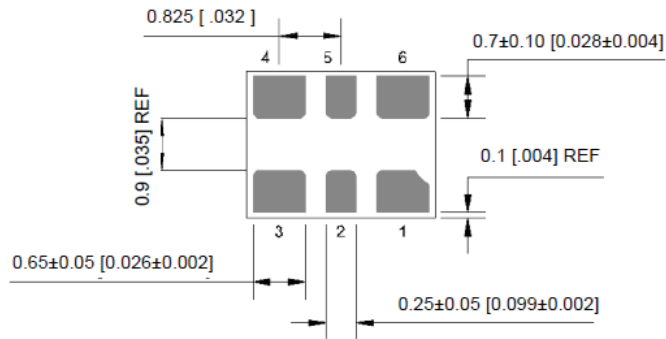
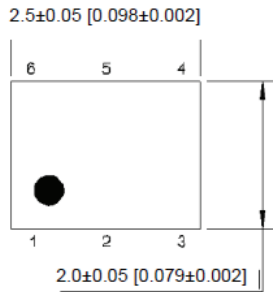
HCSL OUTPUT:



TEST CIRCUIT:



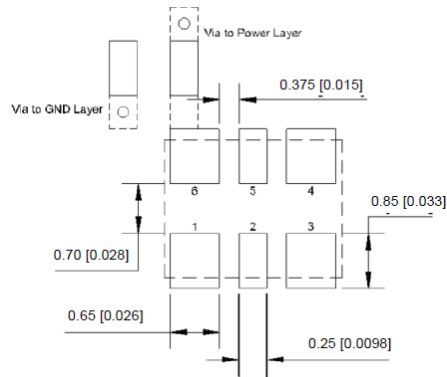
OUTLINE DRAWING:



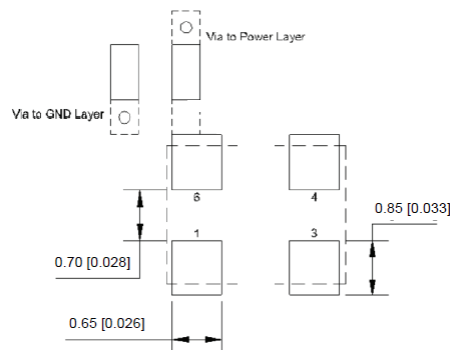
Pin #	Function
1	Tri-state
2	NC
3	GND
4	Output
5	NC (CMOS) Output (LVPECL, LVDS, HCSL)
6	Vdd

Note: Recommend using an approximately 0.01µF bypass capacitor between PIN 6 and 3.

Dimensions: mm (inches)

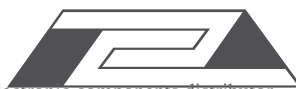


Recommended Land Pattern for LVPECL, LVDS, HCSL



Recommended Land Pattern for CMOS

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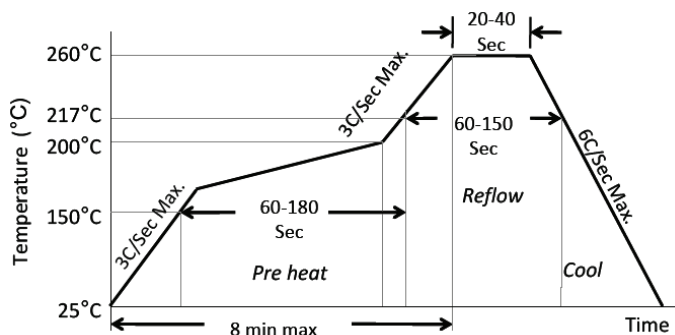


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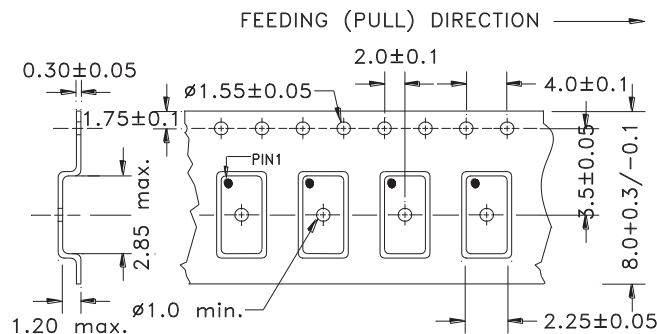
REFLOW PROFILE:



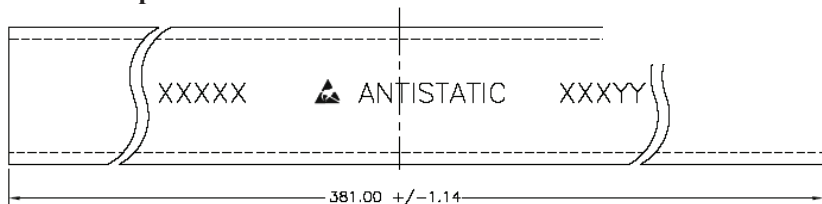
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

TAPE & REEL:

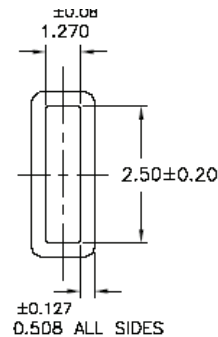
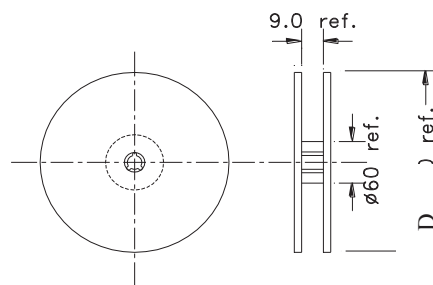
T= 1,000pcs/reel (D=180mm)
T3= 3,000pcs/reel (D=180mm)
T5= 5,000pcs/reel (D=330mm)
T10= 10,000pcs/reel (D=330mm)



Tube: 140 pcs/tube



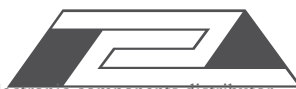
Unit orientation in tube:



Dimensions: mm

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