

# QUAD FREQUENCY VOLTAGE-CONTROLLED CRYSTAL OSCILLATOR (VCXO) 10 MHz TO 1.4 GHz

## Features

- Available with any-rate output frequencies from 10–945 MHz and selected frequencies to 1.4 GHz
- Four selectable output frequencies
- 3rd generation DSPLL<sup>®</sup> with superior jitter performance
- 3x better frequency stability than SAW-based oscillators
- Internal fixed crystal frequency ensures high reliability and low aging
- Available CMOS, LVPECL, LVDS, and CML outputs
- 3.3, 2.5, and 1.8 V supply options
- Industry-standard 5 x 7 mm package and pinout
- Pb-free/RoHS-compliant

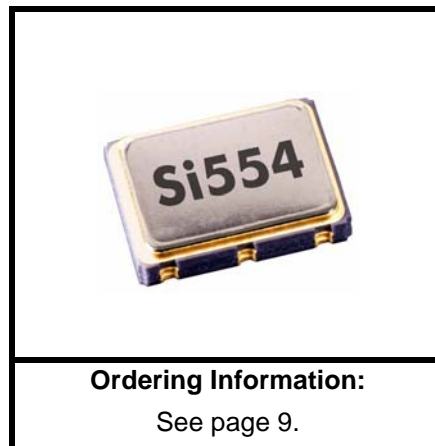
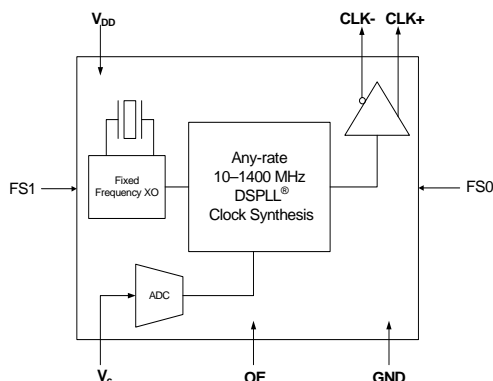
## Applications

- SONET/SDH
- xDSL
- 10 GbE LAN / WAN
- Low jitter clock generation
- Optical modules
- Clock and data recovery

## Description

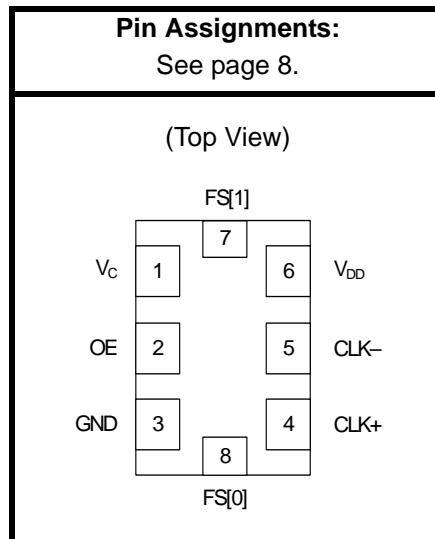
The Si554 quad-frequency VCXO utilizes Silicon Laboratories' advanced DSPLL<sup>®</sup> circuitry to provide a very low jitter clock for all output frequencies. The Si554 is available with any-rate output frequency from 10 to 945 MHz and selected frequencies to 1400 MHz. Unlike traditional VCXOs, where a different crystal is required for each output frequency, the Si554 uses one fixed crystal frequency to provide a wide range of output frequencies. This IC-based approach allows the crystal resonator to provide exceptional frequency stability and reliability. In addition, DSPLL clock synthesis provides superior supply noise rejection, simplifying the task of generating low jitter clocks in noisy environments typically found in communication systems. The Si554 IC-based VCXO is factory-configurable for a wide variety of user specifications including frequency, supply voltage, output format, tuning slope, and temperature stability. Specific configurations are factory-programmed at time of shipment, thereby eliminating the long lead times associated with custom oscillators.

## Functional Block Diagram



## Ordering Information:

See page 9.



## 1. Electrical Specifications

**Table 1. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Supply Voltage <sup>1</sup>	$V_{DD}$	3.3 V option	2.97	3.3	3.63	V
		2.5 V option	2.25	2.5	2.75	V
		1.8 V option	1.71	1.8	1.89	V
Supply Current	$I_{DD}$	Output enabled LVPECL	—	120	130	mA
		CML	—	108	117	
		LVDS	—	99	108	
		CMOS	—	90	98	
		Tristate mode	—	60	75	mA
Output Enable (OE) and Frequency Select FS[1:0] <sup>2</sup>		$V_{IH}$	$0.75 \times V_{DD}$	—	—	V
		$V_{IL}$	—	—	0.5	V
Operating Temperature Range	$T_A$		−40	—	85	°C

**Notes:**

- Selectable parameter specified by part number. See Section 3. "Ordering Information" on page 9 for further details.
- OE and FS[1:0] pins include a 17 k $\Omega$  resistor to VDD.

**Table 2.  $V_C$  Control Voltage Input**

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Control Voltage Tuning Slope <sup>1,2,3</sup>	$K_V$	10 to 90% of $V_{DD}$	—	33	—	ppm/V
				45		
				90		
				135		
				180		
				356		
Control Voltage Linearity <sup>4</sup>	$L_{VC}$	BSL	−5	±1	+5	%
		Incremental	−10	±5	+10	%
Modulation Bandwidth	BW		9.3	10.0	10.7	kHz
$V_C$ Input Impedance	$Z_{VC}$		500	—	—	k $\Omega$
Nominal Control Voltage	$V_{CNOM}$	@ $f_O$	—	$V_{DD}/2$	—	V
Control Voltage Tuning Range	$V_C$		0		$V_{DD}$	V

**Notes:**

- Positive slope; selectable option by part number. See Section 3. "Ordering Information" on page 9.
- For best jitter and phase noise performance, always choose the smallest  $K_V$  that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope ( $K_V$ ), Stability, and Absolute Pull Range (APR)" for more information.
- $K_V$  variation is ±10% of typical values.
- BSL determined from deviation from best straight line fit with  $V_C$  ranging from 10 to 90% of  $V_{DD}$ . Incremental slope determined with  $V_C$  ranging from 10 to 90% of  $V_{DD}$ .

Table 3. CLK± Output Frequency Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Nominal Frequency <sup>1,2,3</sup>	$f_O$	LVDS/CML/LVPECL	10	—	945	MHz
		CMOS	10	—	160	MHz
Temperature Stability <sup>1,4</sup>		$T_A = -40$ to $+85$ °C	-20	—	+20	ppm
			-50	—	+50	
			-100	—	+100	
Absolute Pull Range <sup>1,4</sup>	APR		±12	—	±375	ppm
Aging		Frequency drift over first year.	—	—	±3	ppm
		Frequency drift over 15 year life.	—	—	±10	
Power up Time <sup>5</sup>	$t_{OSC}$		—	—	10	ms
Settling Time After FS[1:0] Change	$t_{FRQ}$	Both FS[1] and FS[0] changing simultaneously	—	—	20	ms

**Notes:**

- See Section 3. "Ordering Information" on page 9 for further details.
- Specified at time of order by part number. Also available in frequencies from 970 to 1134 MHz and 1213 to 1417 MHz.
- Nominal output frequency set by  $V_{CNOM} = V_{DD}/2$ .
- Selectable parameter specified by part number.
- Time from power up or tristate mode to  $f_O$  (to within ±1 ppm of  $f_O$ ).

Table 4. CLK± Output Levels and Symmetry

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
LVPECL Output Option <sup>1</sup>	$V_O$	mid-level	$V_{DD} - 1.42$	—	$V_{DD} - 1.25$	V
	$V_{OD}$	swing (diff)	1.1	—	1.9	$V_{PP}$
	$V_{SE}$	swing (single-ended)	0.55	—	0.95	$V_{PP}$
LVDS Output Option <sup>2</sup>	$V_O$	mid-level	1.125	1.20	1.275	V
	$V_{OD}$	swing (diff)	0.5	0.7	0.9	$V_{PP}$
CML Output Option <sup>2</sup>	$V_O$	2.5/3.3 V option mid-level	—	$V_{DD} - 1.30$	—	V
		1.8 V option mid-level	—	$V_{DD} - 0.36$	—	V
	$V_{OD}$	2.5/3.3 V option swing (diff)	1.10	1.50	1.90	$V_{PP}$
		1.8 V option swing (diff)	0.35	0.425	0.50	$V_{PP}$
CMOS Output Option <sup>3</sup>	$V_{OH}$	$I_{OH} = 32$ mA	$0.8 \times V_{DD}$	—	$V_{DD}$	V
	$V_{OL}$	$I_{OL} = 32$ mA	—	—	0.4	
Rise/Fall time (20/80%)	$t_R, t_F$	LVPECL/LVDS/CML	—	—	350	ps
		CMOS with $C_L = 15$ pF	—	1	—	ns
Symmetry (duty cycle)	SYM	LVPECL: $V_{DD} - 1.3$ V (diff) LVDS: 1.25 V (diff) CMOS: $V_{DD}/2$	45	—	55	%

**Notes:**

- 50 Ω to  $V_{DD} - 2.0$  V.
- $R_{term} = 100$  Ω (differential).
- $C_L = 15$  pF

Table 5. CLK± Output Phase Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS) <sup>1,2,3</sup> for $F_{OUT} \geq 500$ MHz	$\phi_J$	Kv = 33 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.26 0.26	— —	ps
		Kv = 45 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.27 0.26	— —	ps
		Kv = 90 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.32 0.26	— —	ps
		Kv = 135 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.40 0.27	— —	ps
		Kv = 180 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.49 0.28	— —	ps
		Kv = 356 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 80 MHz (OC-192)	— —	0.87 0.33	— —	ps

**Notes:**

1. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest  $K_V$  that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope ( $K_V$ ), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCXO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.
4. Max jitter for LVPECL output with  $V_C=1.65V$ ,  $V_{DD}=3.3V$ , 155.52 MHz.
5. Max offset frequencies: 80 MHz for  $F_{OUT} \geq 250$  MHz, 20 MHz for  $50 \text{ MHz} \leq F_{OUT} < 250$  MHz, 2 MHz for  $10 \text{ MHz} \leq F_{OUT} < 50$  MHz.

Table 5. CLK± Output Phase Jitter (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units	
Phase Jitter (RMS) <sup>1,2,3,4,5</sup> for F <sub>OUT</sub> of 125 to 500 MHz	$\phi_J$	Kv = 33 ppm/V					
		12 kHz to 20 MHz (OC-48)	—	0.37	—	ps	
		50 kHz to 80 MHz (OC-192)	—	0.33	—		
		Kv = 45 ppm/V					
		12 kHz to 20 MHz (OC-48)	—	0.37	0.4	ps	
		50 kHz to 80 MHz (OC-192)	—	0.33	—		
		Kv = 90 ppm/V					
		12 kHz to 20 MHz (OC-48)	—	0.43	—	ps	
		50 kHz to 80 MHz (OC-192)	—	0.34	—		
		Kv = 135 ppm/V					
		12 kHz to 20 MHz (OC-48)	—	0.50	—	ps	
		50 kHz to 80 MHz (OC-192)	—	0.34	—		
Kv = 180 ppm/V							
12 kHz to 20 MHz (OC-48)	—	0.59	—	ps			
50 kHz to 80 MHz (OC-192)	—	0.35	—				
Kv = 356 ppm/V							
12 kHz to 20 MHz (OC-48)	—	1.00	—	ps			
50 kHz to 80 MHz (OC-192)	—	0.39	—				

**Notes:**

1. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest K<sub>V</sub> that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K<sub>V</sub>), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCXO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.
4. Max jitter for LVPECL output with V<sub>C</sub>=1.65V, V<sub>DD</sub>=3.3V, 155.52 MHz.
5. Max offset frequencies: 80 MHz for F<sub>OUT</sub> ≥ 250 MHz, 20 MHz for 50 MHz ≤ F<sub>OUT</sub> < 250 MHz, 2 MHz for 10 MHz ≤ F<sub>OUT</sub> < 50 MHz.

Table 5. CLK± Output Phase Jitter (Continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Phase Jitter (RMS) <sup>1,2,5</sup> for F <sub>OUT</sub> 10 to 160 MHz CMOS Output Only	$\phi_J$	Kv = 33 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 20 MHz	— —	0.63 0.62	— —	ps
		Kv = 45 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 20 MHz	— —	0.63 0.62	— —	ps
		Kv = 90 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 20 MHz	— —	0.67 0.66	— —	ps
		Kv = 135 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 20 MHz	— —	0.74 0.72	— —	ps
		Kv = 180 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 20 MHz	— —	0.83 0.8	— —	ps
		Kv = 356 ppm/V 12 kHz to 20 MHz (OC-48) 50 kHz to 20 MHz	— —	1.26 1.2	— —	ps

**Notes:**

1. Refer to AN255, AN256, and AN266 for further information.
2. For best jitter and phase noise performance, always choose the smallest K<sub>V</sub> that meets the application's minimum APR requirements. See "AN266: VCXO Tuning Slope (K<sub>V</sub>), Stability, and Absolute Pull Range (APR)" for more information.
3. See "AN255: Replacing 622 MHz VCXO devices with the Si550 VCXO" for comparison highlighting power supply rejection (PSR) advantage of Si55x versus SAW-based solutions.
4. Max jitter for LVPECL output with V<sub>C</sub>=1.65V, V<sub>DD</sub>=3.3V, 155.52 MHz.
5. Max offset frequencies: 80 MHz for F<sub>OUT</sub> ≥ 250 MHz, 20 MHz for 50 MHz ≤ F<sub>OUT</sub> < 250 MHz, 2 MHz for 10 MHz ≤ F<sub>OUT</sub> < 50 MHz.

Table 6. CLK± Output Period Jitter

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Period Jitter*	J <sub>PER</sub>	RMS	—	2	—	ps
		Peak-to-Peak	—	14	—	ps

\*Note: Any output mode, including CMOS, LVPECL, LVDS, CML. N = 1000 cycles. Refer to AN279 for further information.

**Table 7. CLK± Output Phase Noise (Typical)**

Offset Frequency	74.25 MHz 90 ppm/V LVPECL	491.52 MHz 45 ppm/V LVPECL	622.08 MHz 135 ppm/V LVPECL	Units
100 Hz	-87	-75	-65	dBc/Hz
1 kHz	-114	-100	-90	
10 kHz	-132	-116	-109	
100 kHz	-142	-124	-121	
1 MHz	-148	-135	-134	
10 MHz	-150	-146	-146	
100 MHz	n/a	-147	-147	

**Table 8. Environmental Compliance**

The Si554 meets the following qualification test requirements.

Parameter	Conditions/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002.3 B
Mechanical Vibration	MIL-STD-883F, Method 2007.3 A
Solderability	MIL-STD-883F, Method 203.8
Gross & Fine Leak	MIL-STD-883F, Method 1014.7
Resistance to Solvents	MIL-STD-883F, Method 2016
Moisture Sensitivity Level	J-STD-020, MSL 1
Contact Pads	J-STD-020, MSL 1

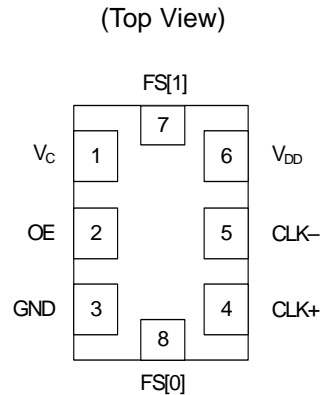
**Table 9. Absolute Maximum Ratings<sup>1</sup>**

Parameter	Symbol	Rating	Units
Maximum Operating Temperature	T <sub>AMAX</sub>	85	°C
Supply Voltage, 1.8 V Option	V <sub>DD</sub>	-0.5 to +1.9	V
Supply Voltage, 2.5/3.3 V Option	V <sub>DD</sub>	-0.5 to +3.8	V
Input Voltage (any input pin)	V <sub>I</sub>	-0.5 to V <sub>DD</sub> + 0.3	V
Storage Temperature	T <sub>S</sub>	-55 to +125	°C
ESD Sensitivity (HBM, per JESD22-A114)	ESD	2000	V
Soldering Temperature (Pb-free profile) <sup>2</sup>	T <sub>PEAK</sub>	260	°C
Soldering Temperature Time @ T <sub>PEAK</sub> (Pb-free profile) <sup>2</sup>	t <sub>P</sub>	20–40	seconds

**Notes:**

- Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation or specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.
- The device is compliant with JEDEC J-STD-020C. Refer to Si5xx Packaging FAQ available for download from [www.silabs.com/VCXO](http://www.silabs.com/VCXO) for further information, including soldering profiles.

## 2. Pin Descriptions



**Table 10. Si554 Pin Descriptions**

Pin	Name	Type	Function
1	$V_C$	Analog Input	Control Voltage
2	OE*	Input	Output Enable (Polarity = High): 0 = clock output disabled (outputs tri-stated) 1 = clock output enabled
3	GND	Ground	Electrical and Case Ground
4	CLK+	Output	Oscillator Output
5	CLK- (N/A for CMOS)	Output	Complementary Output (N/C for CMOS)
6	$V_{DD}$	Power	Power Supply Voltage
7	FS[1]*	Input	Frequency Select MSB
8	FS[0]*	Input	Frequency Select LSB

**\*Note:** FS[1:0] and OE include a 17 k $\Omega$  pullup resistor to  $V_{DD}$ . Output Enable polarity selectable at time of order. See Section 3. "Ordering Information" on page 9 for details on frequency select and OE polarity ordering options.



### 3. Ordering Information

The Si554 supports a variety of options including frequency, temperature stability, tuning slope, output format, and  $V_{DD}$ . Specific device configurations are programmed into the Si554 at time of shipment. Configurations are specified using the Part Number Configuration chart shown below. Silicon Labs provides a web browser-based part number configuration utility to simplify this process. Refer to [www.silabs.com/VCXOPartNumber](http://www.silabs.com/VCXOPartNumber) to access this tool and for further ordering instructions. The Si554 VCXO series is supplied in an industry-standard, RoHS-compliant, lead-free, 8-pad, 5 x 7 mm package. Tape and reel packaging is an ordering option.

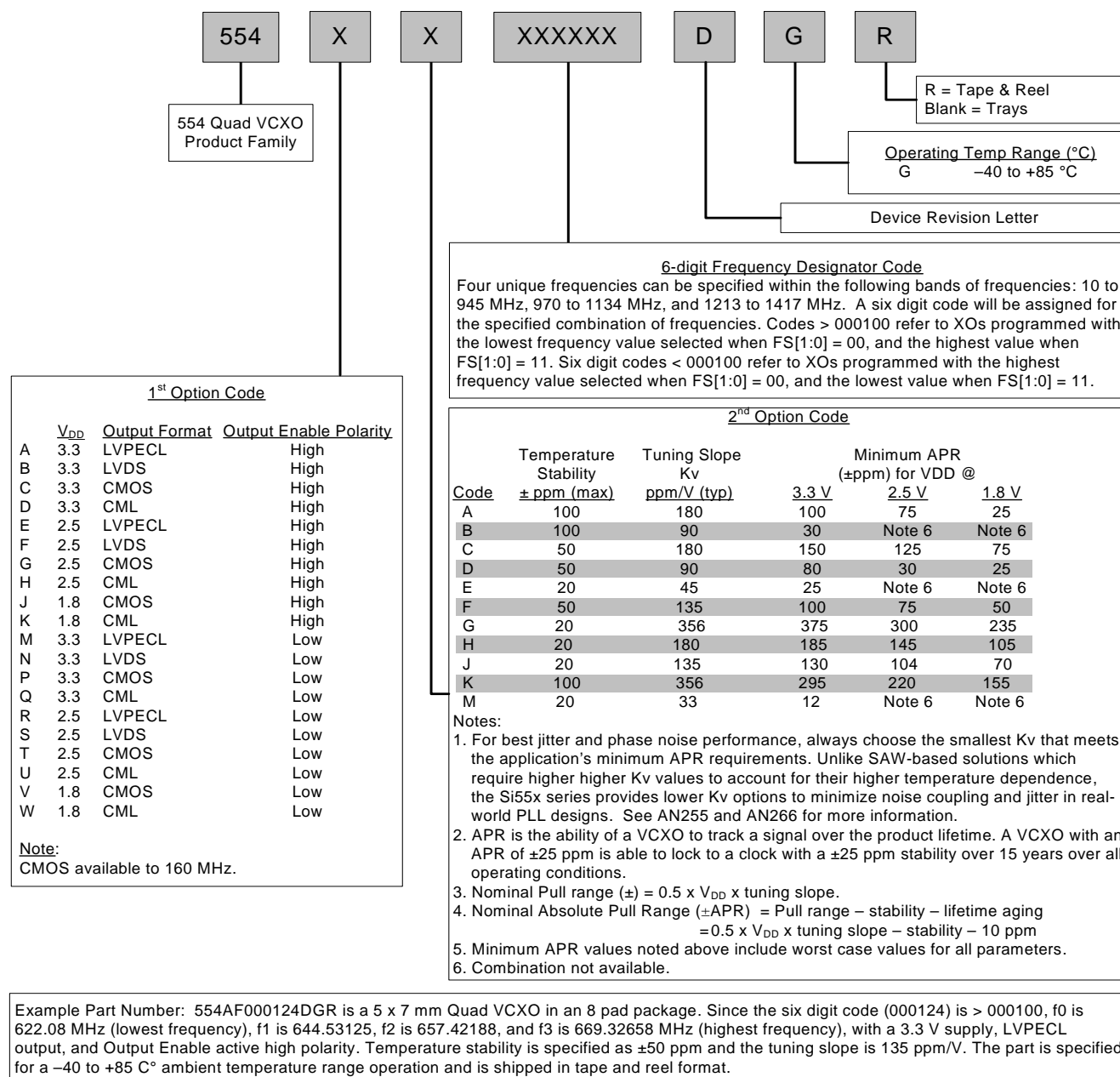


Figure 1. Part Number Convention

## 4. Package Outline and Suggested Pad Layout

Figure 2 illustrates the package details for the Si554. Table 11 lists the values for the dimensions shown in the illustration.

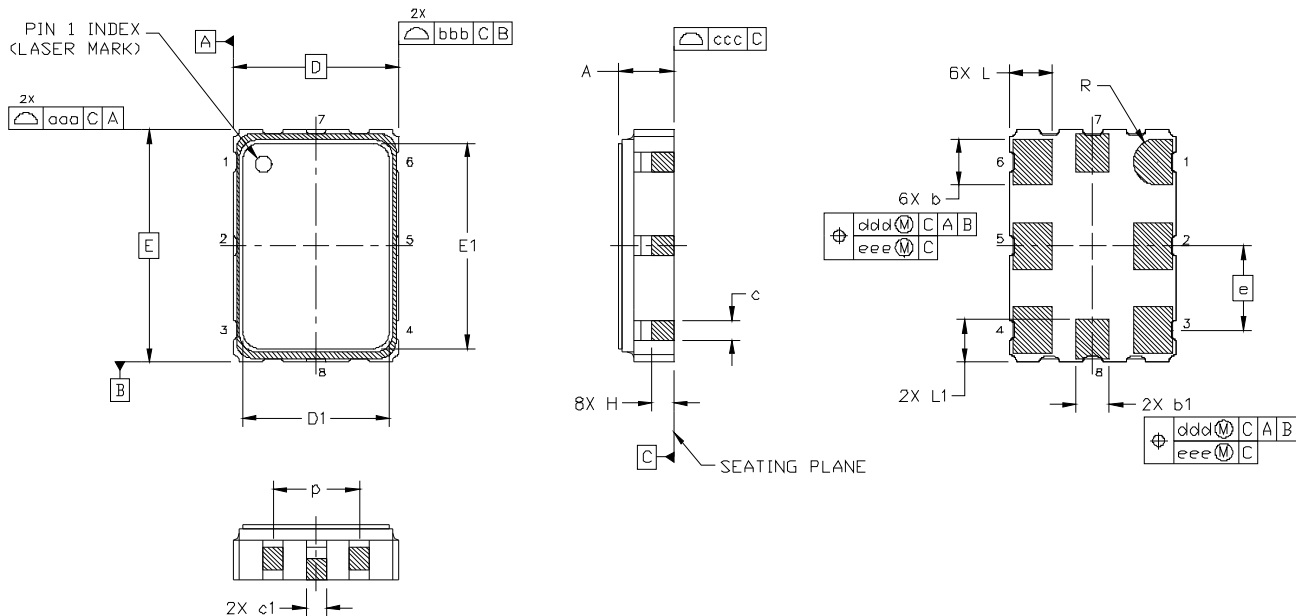


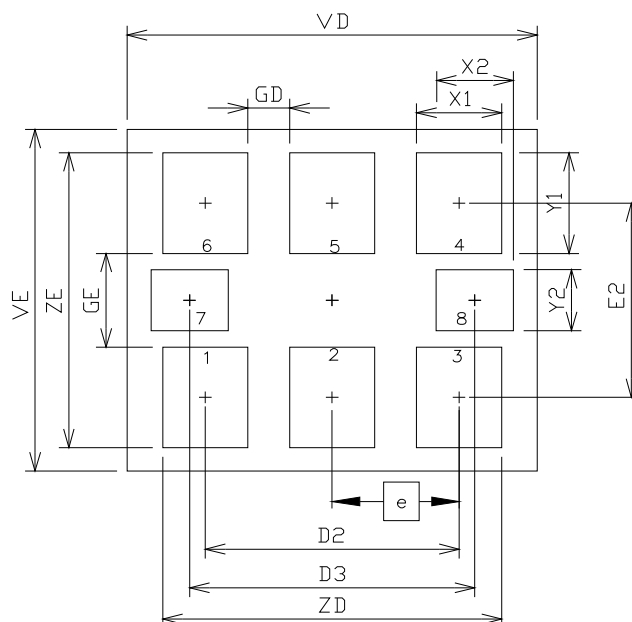
Figure 2. Si554 Outline Diagram

Table 11. Package Diagram Dimensions (mm)

Dimension	Min	Nom	Max
A	1.50	1.65	1.80
b	1.30	1.40	1.50
b1	0.90	1.00	1.10
c	0.50	0.60	0.70
c1	0.30	—	0.60
D	5.00 BSC		
D1	4.30	4.40	4.50
e	2.54 BSC		
E	7.00 BSC		
E1	6.10	6.20	6.30
H	0.55	0.65	0.75
L	1.17	1.27	1.37
L1	1.07	1.17	1.27
p	1.80	—	2.60
R	0.70 REF		
aaa	—	—	0.15
bbb	—	—	0.15
ccc	—	—	0.10
ddd	—	—	0.10
eee	—	—	0.05
<b>Note:</b>			
1. All dimensions shown are in millimeters (mm) unless otherwise noted.			
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.			

## 5. 8-Pin PCB Land Pattern

Figure 3 illustrates the 8-pin PCB land pattern for the Si554. Table 12 lists the values for the dimensions shown in the illustration.



**Figure 3. Si554 PCB Land Pattern**

**Table 12. PCB Land Pattern Dimensions (mm)**

Dimension	Min	Max
D2	5.08 REF	
D3	5.705 REF	
e	2.54 BSC	
E2	4.20 REF	
GD	0.84	—
GE	2.00	—
VD	8.20 REF	
VE	7.30 REF	
X1	1.70 TYP	
X2	1.545 TYP	
Y1	2.15 REF	
Y2	1.3 REF	
ZD	—	6.78
ZE	—	6.30

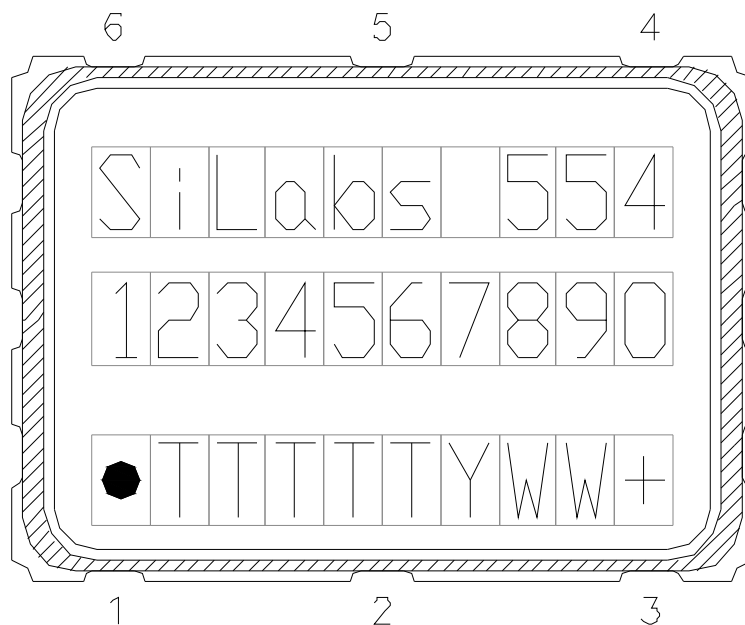
**Note:**

1. Dimensioning and tolerancing per the ANSI Y14.5M-1994 specification.
2. Land pattern design follows IPC-7351 guidelines.
3. All dimensions shown are at maximum material condition (MMC).
4. Controlling dimension is in millimeters (mm).

# Si554

## 6. Top Marking

### 6.1. Si554 Top Marking



### 6.2. Top Marking Explanation

Line	Position	Description
1	1–10	“SiLabs”+ Part Family Number, 554 (First 3 characters in part number)
2	1–10	Si554: Option1+Option2+Freq(7)+Temp Si554 w/ 8-digit resolution: Option1+Option2+ConfigNum(6)+Temp
3	<b>Trace Code</b>	
	Position 1	Pin 1 orientation mark (dot)
	Position 2	Product Revision (D)
	Position 3–6	Tiny Trace Code (4 alphanumeric characters per assembly release instructions)
	Position 7	Year (least significant year digit), to be assigned by assembly site (ex: 2007 = 7)
	Position 8–9	Calendar Work Week number (1–53), to be assigned by assembly site
	Position 10	“+” to indicate Pb-Free and RoHS-compliant

## DOCUMENT CHANGE LIST

### Revision 0.6 to Revision 1.0

- Updated Table 4 on page 3.
  - Updated 2.5 V/3.3 V and 1.8 V CML output level specifications.
- Updated Table 5 on page 4.
  - Removed the words “Differential Modes: LVPECL/LVDS/CML” in the footnote referring to AN256.
  - Added footnotes clarifying max offset frequency test conditions.
  - Added CMOS phase jitter specs.
- Updated Table 9 on page 7.
  - Separated 1.8 V, 2.5 V/3.3 V supply voltage specifications.
  - Updated ESD HBM sensitivity rating.
- Updated and clarified Table 8 on page 7
  - Added “Moisture Sensitivity Level” and “Contact Pads” rows.
- Updated 6. “Top Marking” on page 12 to reflect specific marking information (previously, figure was generic).
- Updated 4. “Package Outline and Suggested Pad Layout” on page 10.
  - Added crystal impedance pin in Figure 2 on page 10 and Table 11 on page 10.
- Reordered spec tables and back matter to conform to data sheet quality conventions.

## CONTACT INFORMATION

### Silicon Laboratories Inc.

400 West Cesar Chavez  
Austin, TX 78701  
Tel: 1+(512) 416-8500  
Fax: 1+(512) 416-9669  
Toll Free: 1+(877) 444-3032

Please visit the Silicon Labs Technical Support web page:  
<https://www.silabs.com/support/pages/contacttechnicalsupport.aspx>  
and register to submit a technical support request.

The information in this document is believed to be accurate in all respects at the time of publication but is subject to change without notice. Silicon Laboratories assumes no responsibility for errors and omissions, and disclaims responsibility for any consequences resulting from the use of information included herein. Additionally, Silicon Laboratories assumes no responsibility for the functioning of undescribed features or parameters. Silicon Laboratories reserves the right to make changes without further notice. Silicon Laboratories makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Silicon Laboratories assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. Silicon Laboratories products are not designed, intended, or authorized for use in applications intended to support or sustain life, or for any other application in which the failure of the Silicon Laboratories product could create a situation where personal injury or death may occur. Should Buyer purchase or use Silicon Laboratories products for any such unintended or unauthorized application, Buyer shall indemnify and hold Silicon Laboratories harmless against all claims and damages.

Silicon Laboratories, Silicon Labs, and DSPLL are trademarks of Silicon Laboratories Inc.  
Other products or brandnames mentioned herein are trademarks or registered trademarks of their respective holders.