

General Description

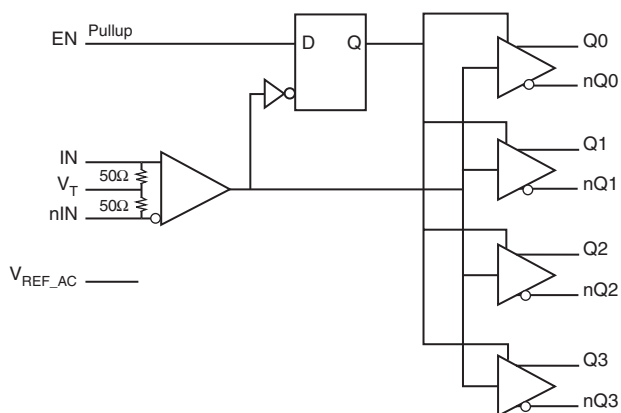


The ICS8S89831I is a high speed 1-to-4 Differential-to-LVPECL/ECL Fanout Buffer. The ICS8S89831I is optimized for high speed and very low output skew, making it suitable for use in demanding applications such as SONET, 1 Gigabit and 10 Gigabit Ethernet, and Fibre Channel. The internally terminated differential input and VREF_AC pin allow other differential signal families such as LVDS, LVHSTL and CML to be easily interfaced to the input with minimal use of external components. The device also has an output enable pin which may be useful for system test and debug purposes. The ICS8S89831I is packaged in a small 3mm x 3mm 16-pin VFQFN package which makes it ideal for use in space-constrained applications.

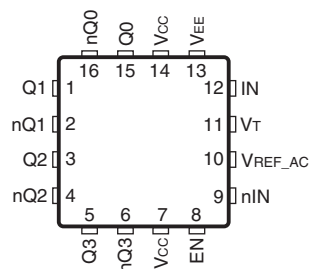
Features

- Four LVPECL/ECL outputs
- IN, nIN input can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- 50Ω internal input termination to V_T
- Output frequency: >2.1GHz
- Output skew: 30ps (maximum)
- Part-to-part skew: 185ps (maximum)
- Additive phase jitter, RMS: 0.31ps (typical)
- Propagation Delay: 570ps (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 2.5V±5%, 3.3V±5%, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.3V±5%, -2.5V±5%
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS8S89831I

16-Lead VFQFN

3mm x 3mm x 0.925mm package body

K Package

Top View

Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|--------|---------------|--------|--------|---|
| 1, 2 | Q1, nQ1 | Output | | Differential output pair. LVPECL/ECL interface levels. |
| 3, 4 | Q2, nQ2 | Output | | Differential output pair. LVPECL/ECL interface levels. |
| 5, 6 | Q3, nQ3 | Output | | Differential output pair. LVPECL/ECL interface levels. |
| 7, 14 | V_{CC} | Power | | Power supply pins. |
| 8 | EN | Input | Pullup | Synchronizing clock enable. When LOW, Qx outputs will go LOW and nQx outputs will go HIGH on the next LOW transition at IN input. Input threshold is $V_{CC}/2$. Includes a 37k Ω pull-up resistor. Default state is HIGH when left floating. The internal latch is clocked on the falling edge of the input signal IN. LVTTTL / LVCMOS interface levels. |
| 9 | nIN | Input | | Inverting differential LVPECL clock input. RT = 50 Ω termination to V_T . |
| 10 | V_{REF_AC} | Output | | Reference voltage for AC-coupled applications. |
| 11 | V_T | Input | | Termination input. $I_{REF_AC} (max.) < \pm 2mA$. |
| 12 | IN | Input | | Non-inverting LVPECL differential clock input. RT = 50 Ω termination to V_T . |
| 13 | V_{EE} | Power | | Negative supply pin. |
| 15, 16 | Q0, nQ0 | Output | | Differential output pair. LVPECL/ECL interface levels. |

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|-----------------------|-----------------|---------|---------|---------|------------|
| R_{PULLUP} | Input Pullup Resistor | | | 37 | | k Ω |

Function Tables

Table 3A. Control Input Function Table

| Input | Outputs | |
|-------|---------------|----------------|
| EN | Q0:Q3 | nQ0:nQ3 |
| 0 | Disabled; LOW | Disabled; HIGH |
| 1 | Enabled | Enabled |

NOTE: After EN switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in *Figure 1*.

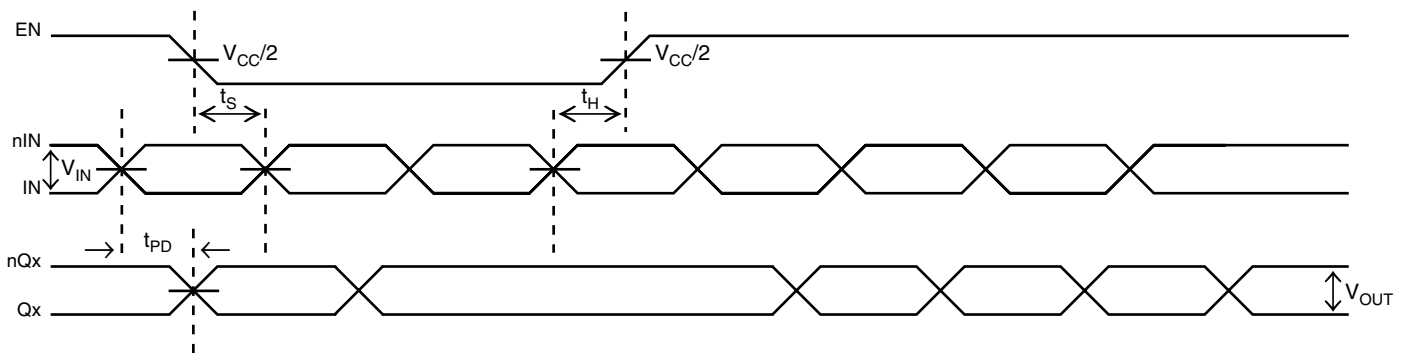


Figure 1. EN Timing Diagram

Table 3B. Truth Table

| Inputs | | | Outputs | |
|--------|-----|----|------------|------------|
| IN | nIN | EN | Q0:Q3 | nQ0:nQ3 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| X | X | 0 | 0 (NOTE 1) | 1 (NOTE 1) |

NOTE 1: On the next negative transition of the input signal (IN).

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|--|------------------------------------|
| Supply Voltage, V_{CC} | 4.6V (LVPECL mode, $V_{EE} = 0V$) |
| Negative Supply Voltage, V_{EE} | -4.6V (ECL mode, $V_{CC} = 0V$) |
| Inputs, V_I (LVPECL mode) | -0.5V to $V_{CC} + 0.5V$ |
| Inputs, V_I (ECL mode) | 0.5V to $V_{EE} - 0.5V$ |
| Outputs, I_O Continuous Current Surge Current | 50mA 100mA |
| Input Current, I_N , nIN | $\pm 50mA$ |
| V_T Current, I_{VT} | $\pm 100mA$ |
| V_{REF_AC} Input Sink/Source Current, I_{REF_AC} | $\pm 2mA$ |
| Operating Temperature Range, T_A | -40°C to +85°C |
| Package Thermal Impedance, θ_{JA} , (Junction-to-Ambient) | 74.7°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|-----------------|---------|---------|---------|-------|
| V_{CC} | Positive Supply Voltage | | 2.375 | 3.3 | 3.465 | V |
| I_{EE} | Power Supply Current | | | | 45 | mA |

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|--------------------------------|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2.2 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | 0 | | 0.8 | V |
| I_{IH} | Input High Current | $V_{CC} = V_{IN} = 3.465V$ | | | 10 | μA |
| I_{IL} | Input Low Current | $V_{CC} = 3.465V, V_{IN} = 0V$ | -150 | | | μA |

Table 4C. Differential DC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------|---|---------------------|-----------------|-----------------|-----------------|----------|
| R_{IN} | Differential Input Resistance (IN, nIN) | IN to VT, nIN to VT | 40 | 50 | 60 | Ω |
| V_{IH} | Input High Voltage (IN, nIN) | | 1.2 | | V_{CC} | V |
| V_{IL} | Input Low Voltage (IN, nIN) | | 0 | | $V_{IH} - 0.15$ | V |
| V_{IN} | Input Voltage Swing | | 0.15 | | 1.2 | V |
| V_{DIFF_IN} | Differential Input Voltage Swing | | 0.3 | | | V |
| I_{IN} | Input Current; NOTE 1 (IN, nIN) | | | | 35 | mA |
| V_{REF_AC} | Bias Voltage | | $V_{CC} - 1.45$ | $V_{CC} - 1.37$ | $V_{CC} - 1.32$ | V |

NOTE 1: Guaranteed by design.

Table 4D. LVPECL DC Characteristics, $V_{CC} = 2.5V \pm 5\%$, $3.3V \pm 5\%$, $T_A = -40^\circ\text{C}$ to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|-----------------------------------|-----------------|------------------|---------|------------------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | $V_{CC} - 1.175$ | | $V_{CC} - 0.85$ | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | $V_{CC} - 2.0$ | | $V_{CC} - 1.575$ | V |
| V_{OUT} | Output Voltage Swing | | 0.6 | | 1.0 | V |
| V_{DIFF_OUT} | Differential Output Voltage Swing | | 1.2 | | 2.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CC} - 2V$.

AC Electrical Characteristics

Table 5. AC Characteristics, $V_{CC} = 0V$; $V_{EE} = -3.3V \pm 5\%$, $-2.5V \pm 5\%$ or $V_{CC} = 2.5V \pm 5\%$, $3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|--------------|--|--------------|--|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | | Output Swing $\geq 450mV$ | 2.1 | | | GHz |
| t_{PD} | Propagation Delay; (Differential); NOTE 1 | | Input Swing: 150mV | 300 | | 570 | ps |
| | | | Input Swing: 800mV | 255 | | 510 | ps |
| $t_{sk(o)}$ | Output Skew; NOTE 2, 4 | | | | | 30 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 3, 4 | | | | | 185 | ps |
| f_{jit} | Buffer Additive Jitter; RMS; refer to Additive Phase Jitter Section | | 155.52MHz, Integration Range: 12kHz – 20MHz | | 0.31 | | ps |
| t_S | Clock Enable Setup Time | EN to IN/nIN | | 300 | | | ps |
| t_H | Clock Enable Hold Time | EN to IN/nIN | | 300 | | | ps |
| t_R / t_F | Output Rise/Fall Time | | 20% to 80% | 100 | | 250 | ps |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters characterized at $\leq 1GHz$ unless otherwise noted.

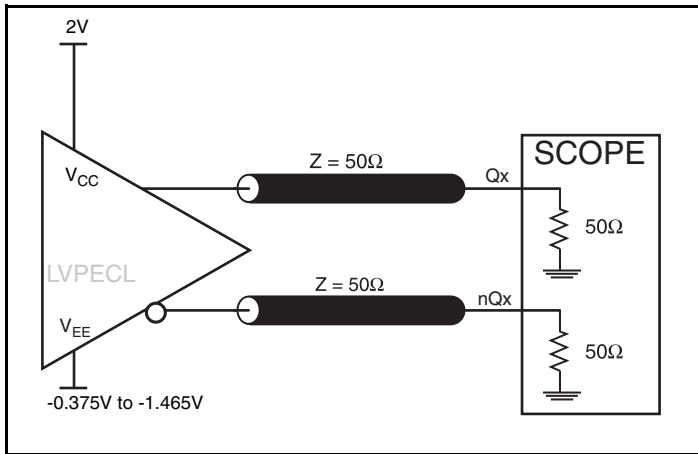
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

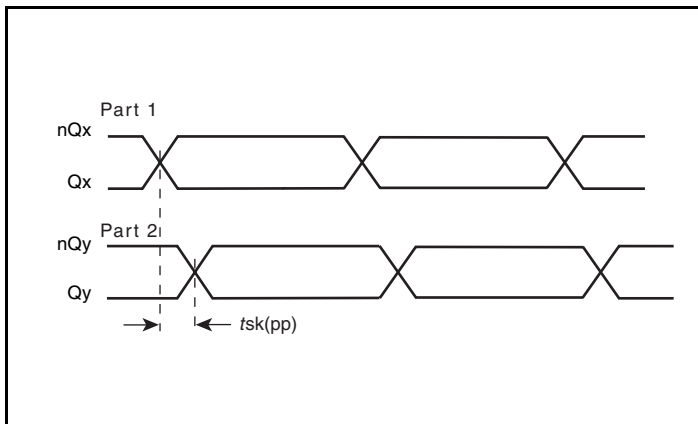
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

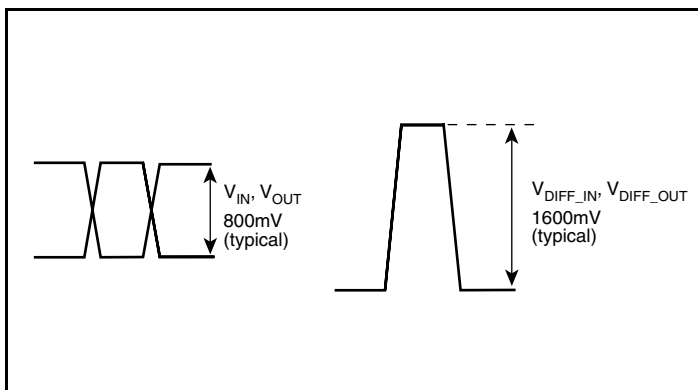
Parameter Measurement Information



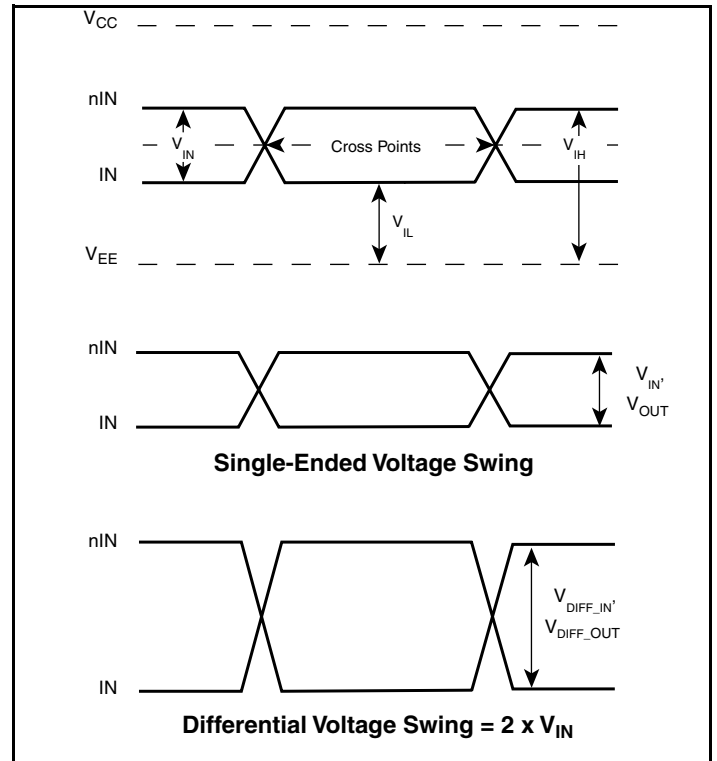
Output Load AC Test Circuit



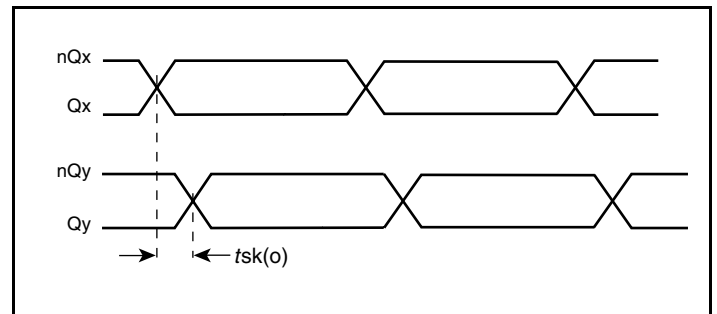
Part-to-Part Skew



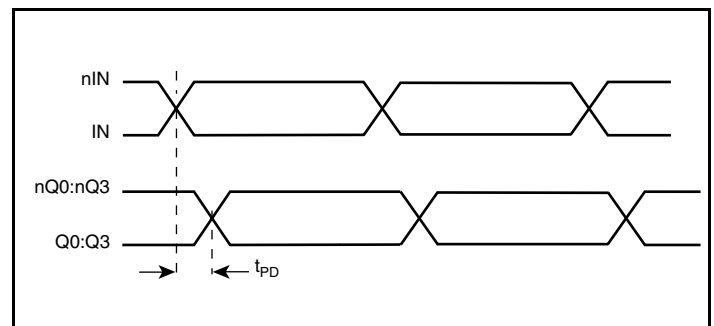
Single-ended & Differential Input Voltage Swing



Differential Input Level

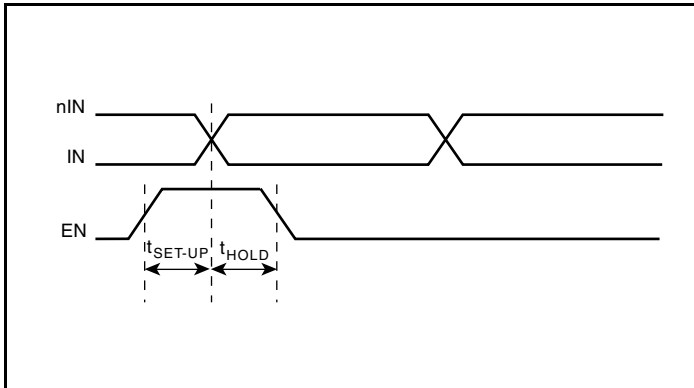


Output Skew

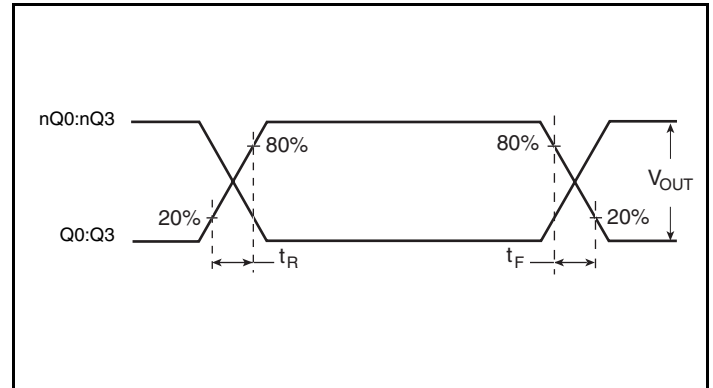


Propagation Delay

Parameter Measurement Information, continued



Setup & Hold Time



Output Rise/Fall Time

Application Information

Recommendations for Unused Output Pins

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

3.3V Differential Input with Built-In 50Ω Termination Interface

The IN/nIN with built-in 50Ω terminations accept LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 2A to 2D* show interface examples for the IN/nIN input with built-in 50Ω terminations driven by the most common driver types. The input interfaces

suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

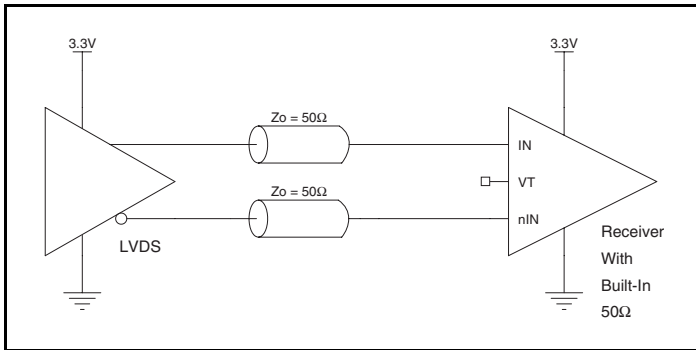


Figure 2A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

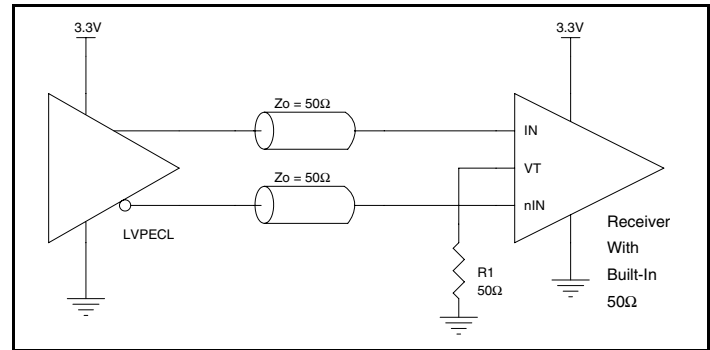


Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

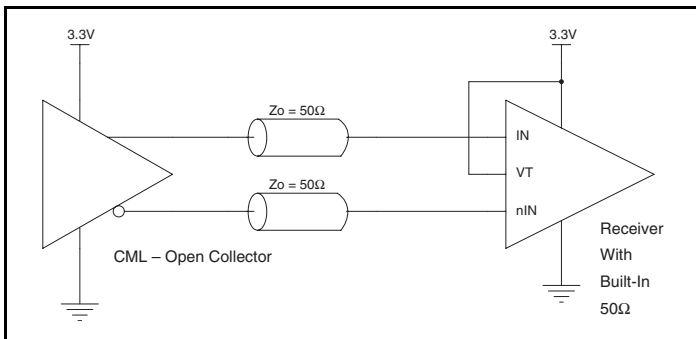


Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Open Collector

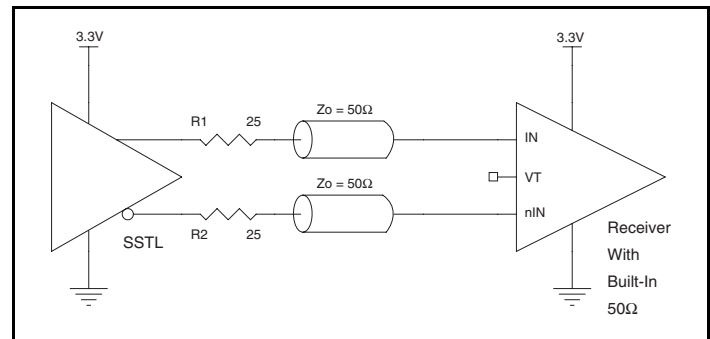


Figure 2D. IN/nIN Input with Built-In 50Ω Driven by an SSTL Driver

2.5V LVPECL Input with Built-In 50Ω Termination Interface

The IN/nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML, SSTL and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 3A to 3D* show interface examples for the IN/nIN with built-in 50Ω termination input driven by

the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

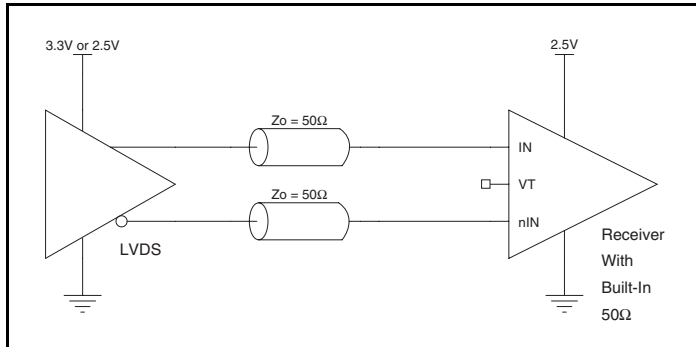


Figure 3A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

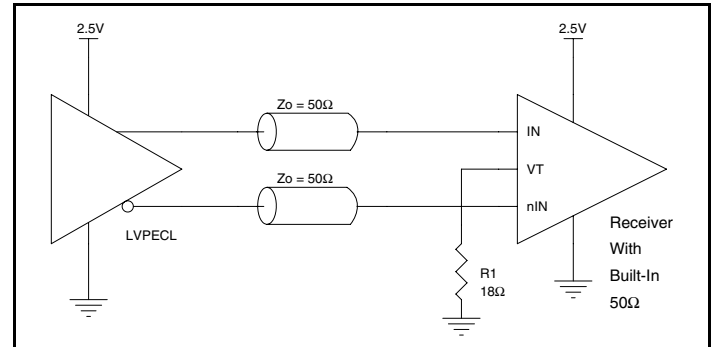


Figure 3B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

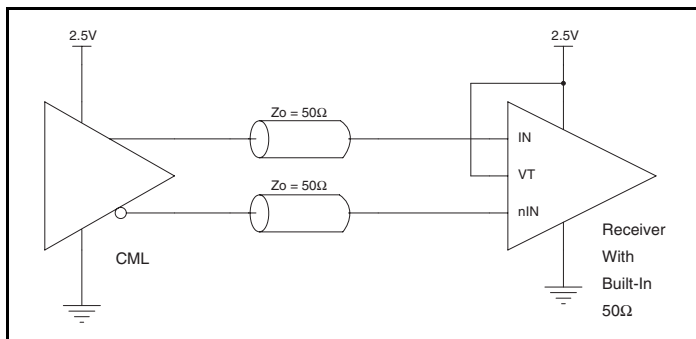


Figure 3C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Open Collector

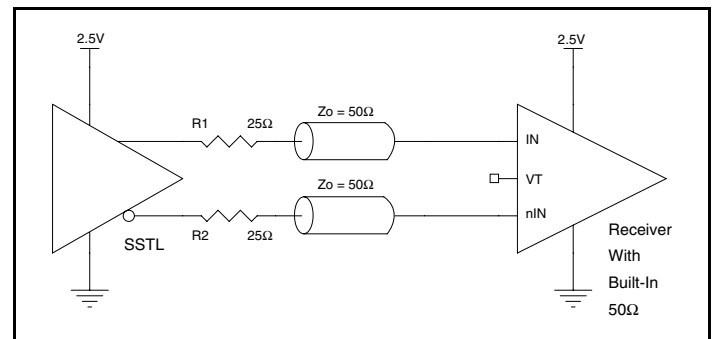


Figure 3D. IN/nIN Input with Built-In 50Ω Driven by an SSTL Driver

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

Figures 4A and 4B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

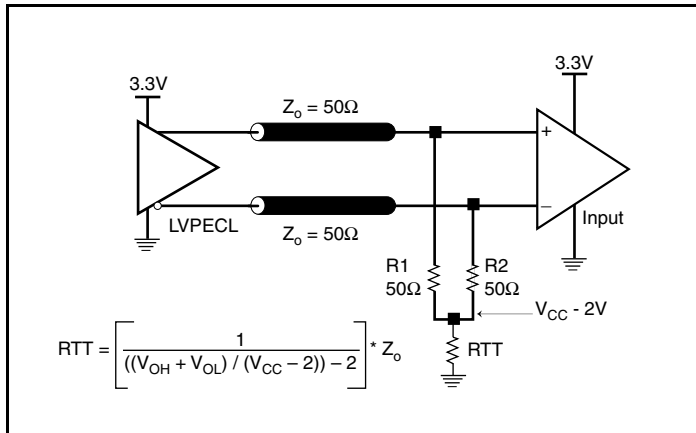


Figure 4A. 3.3V LVPECL Output Termination

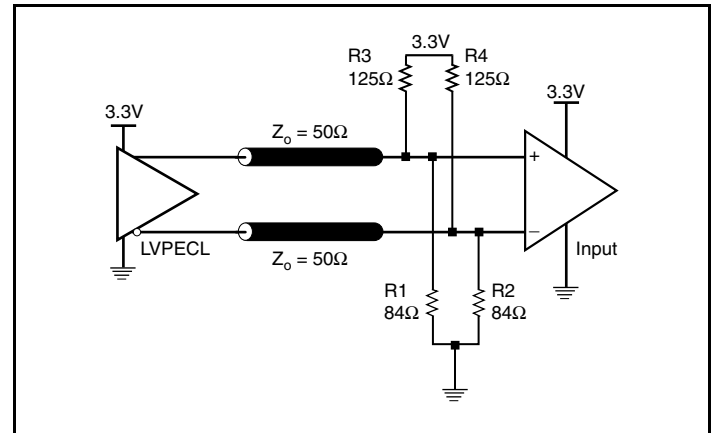


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{CC} - 2V$. For $V_{CC} = 2.5V$, the $V_{CC} - 2V$ is very close to ground

level. The $R3$ in Figure 5B can be eliminated and the termination is shown in Figure 5C.

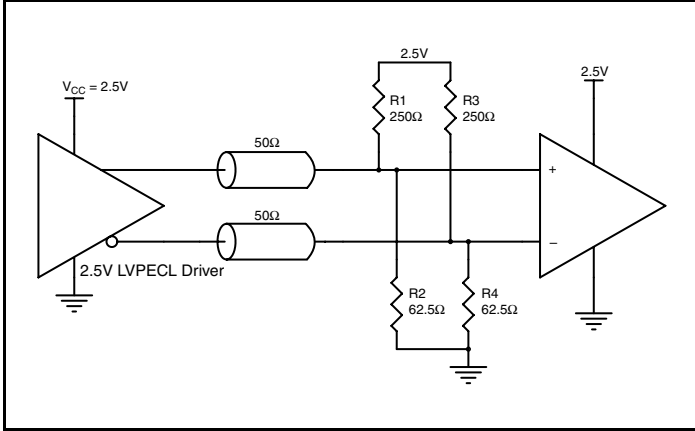


Figure 5A. 2.5V LVPECL Driver Termination Example

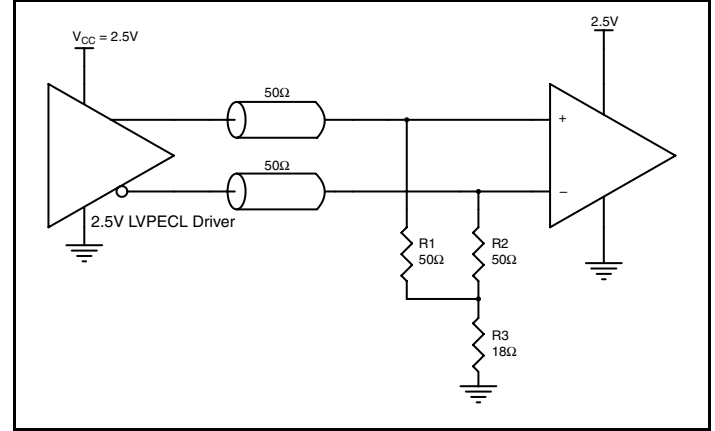


Figure 5B. 2.5V LVPECL Driver Termination Example

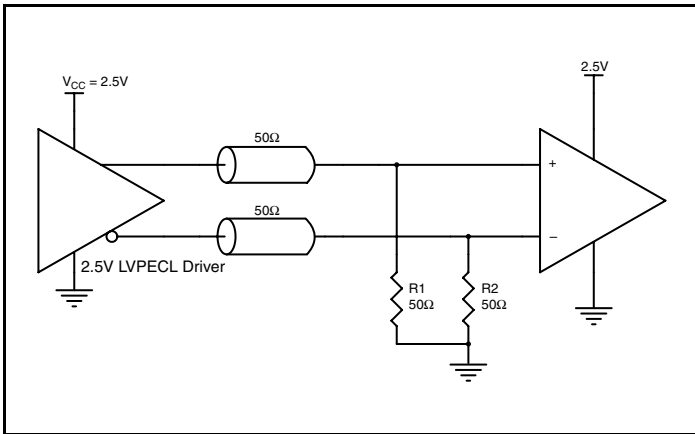


Figure 5C. 2.5V LVPECL Driver Termination Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

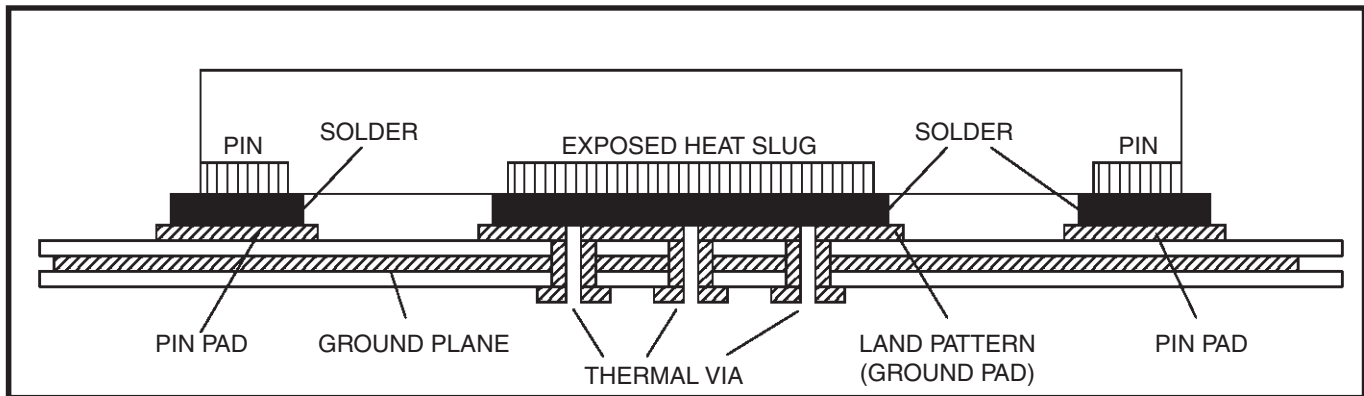


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Example

Figure 7 shows a schematic example of the ICS8S89831I. This schematic provides examples of input and output handling. The ICS8S89831I input has built-in 50Ω termination resistors. The input can directly accept various types of differential signal without AC couple. For AC couple termination, the ICS8S89831I also provides the VREF_AC pin for proper offset level after the AC couple. This example shows the ICS8S89831I input driven by a 2.5V LVPECL

driver with AC couple. The ICS8S89831I outputs are LVPECL driver. In this example, we assume the traces are long transmission line and the receiver is high input impedance without built-in matched load. An example of 3.3V LVPECL termination is shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

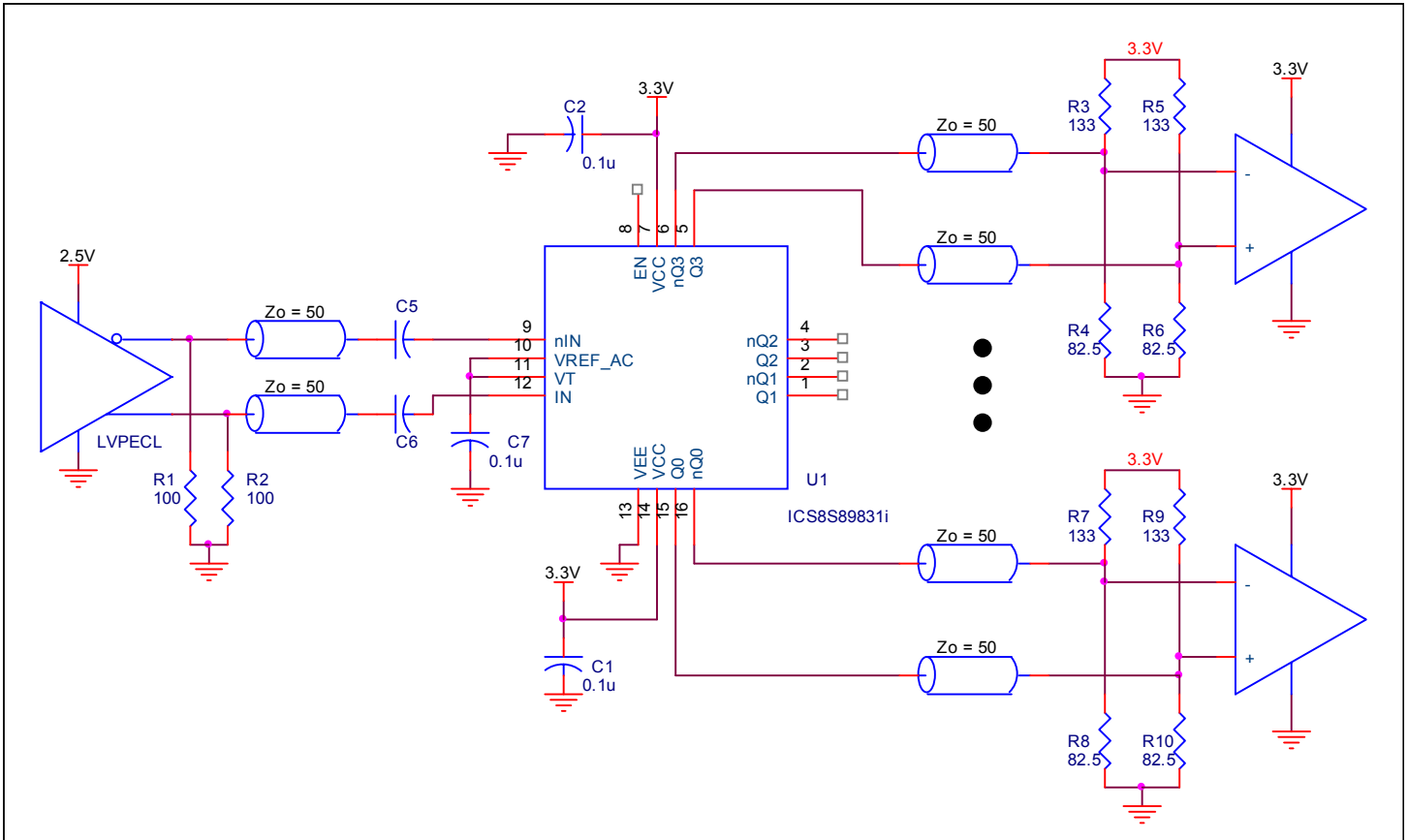


Figure 7. ICS8S89831I Application Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8S89831I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8S89831I is the sum of the core power plus the power dissipation in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipation in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 45mA = 155.925mW$
- Power (outputs)_{MAX} = **32.94mW/Loaded Output pair**
If all outputs are loaded, the total power is $4 * 32.94mW = 131.76mW$
- Power Dissipation for internal termination R_T
Power $(R_T)_{MAX} = (V_{IN_MAX})^2 / R_{T_MIN} = (1.2V)^2 / 80\Omega = 18mW$

Total Power_{MAX} (3.3V, with all outputs switching) = $155.925mW + 131.76mW + 18mW = 305.685mW$

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$85^\circ C + 0.306W * 74.7^\circ C/W = 107.9^\circ C$. This is well below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFN, Forced Convection

| Meters per Second | θ_{JA} by Velocity | | |
|---|---------------------------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 74.7°C/W | 65.3°C/W | 58.5°C/W |

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

The LVPECL output driver circuit and termination are shown in *Figure 8*.

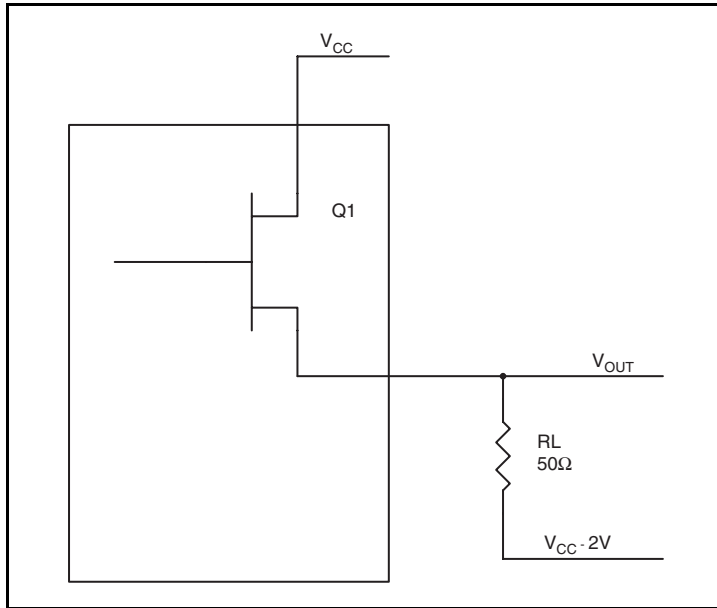


Figure 8. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.85V$
($V_{CC_MAX} - V_{OH_MAX}$) = **0.85V**
- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.575V$
($V_{CC_MAX} - V_{OL_MAX}$) = **1.575V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.85V)/50\Omega] * 0.85V = \mathbf{19.55mW}$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.575V)/50\Omega] * 1.575V = \mathbf{13.39mW}$$

Total Power Dissipation per output pair = $Pd_H + Pd_L = \mathbf{32.94mW}$

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

| θ_{JA} by Velocity | | | |
|---|----------|----------|----------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 74.7°C/W | 65.3°C/W | 58.5°C/W |

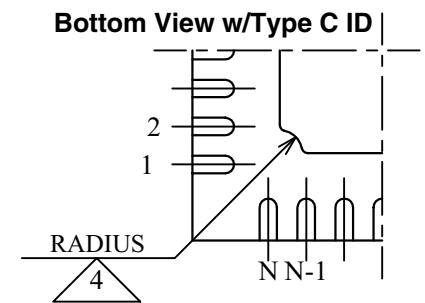
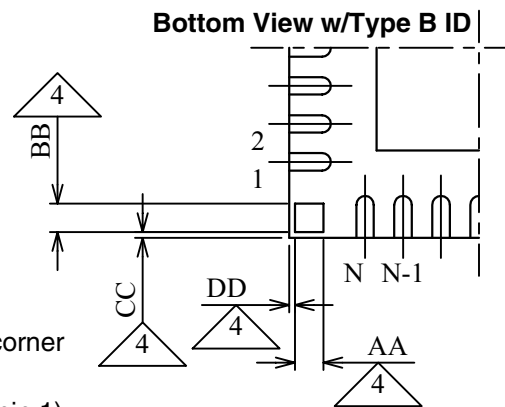
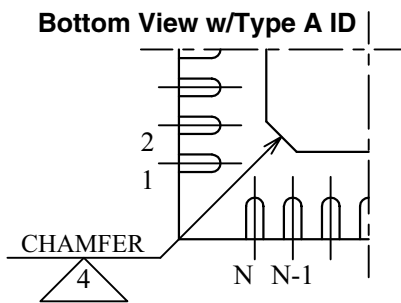
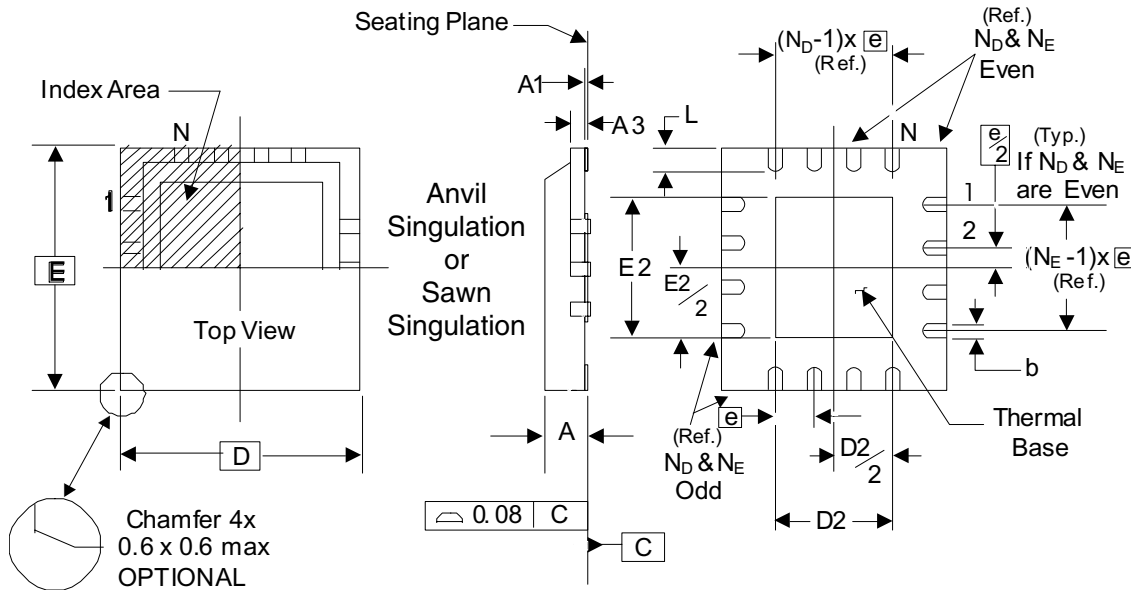
Transistor Count

The transistor count for ICS8S89831I is: 328

This device is pin and function compatible and a suggested replacement for ICS889831.

Package Outline and Package Dimensions

Package Outline - K Suffix for 16 Lead VFQFN



There are 3 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type B: Dummy pad between pin 1 and N.
3. Type C: Mouse bite on the paddle (near pin 1)

Table 8. Package Dimensions

| JEDEC Variation: VEED-2/-4 All Dimensions in Millimeters | | |
|---|------------|---------|
| Symbol | Minimum | Maximum |
| N | 16 | |
| A | 0.80 | 1.00 |
| A1 | 0 | 0.05 |
| A3 | 0.25 Ref. | |
| b | 0.18 | 0.30 |
| $N_D \& N_E$ | 4 | |
| D & E | 3.00 Basic | |
| D2 & E2 | 1.00 | 1.80 |
| e | 0.50 Basic | |
| L | 0.30 | 0.50 |

Reference Document: JEDEC Publication 95, MO-220

Ordering Information

Table 9. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|---------|---------------------------|--------------------|---------------|
| 8S89831AKILF | 831A | "Lead-Free" 16 Lead VFQFN | Tube | -40°C to 85°C |
| 8S89831AKILFT | 831A | "Lead-Free" 16 Lead VFQFN | 2500 Tape & Reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|-----|-------|------|--|---------|
| A | | 11 | Deleted <i>Differential Input with Built-in 50Ω Termination Unused Input Handling</i> application section. This section does not apply when there is only one input. | 4/22/10 |
| | | 15 | Power Considerations - in Power Dissipation section, corrected Power (RT) calculation. Calculation = 18mW from 98mW. Total Power and Junction Temperature calculations have also been updated. | |
| | | | | |



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