Low Skew, 1-to-8, Differential-to-LVDS Clock

General Description

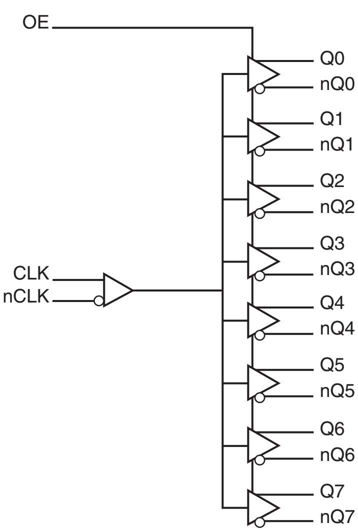
The ICS85408 is a low skew, high performance 1-to-8 Differential-to-LVDS Clock Distribution Chip and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS85408 CLK, nCLK pair can accept most differential input levels and translates them to 3.3V LVDS output levels. Utilizing Low Voltage Differential Signaling (LVDS), the ICS85408 provides a low power, low noise, low skew, point-to-point solution for distributing LVDS clock signals.

Guaranteed output and part-to-part skew specifications make the ICS85408 ideal for those applications demanding well defined performance and repeatability.

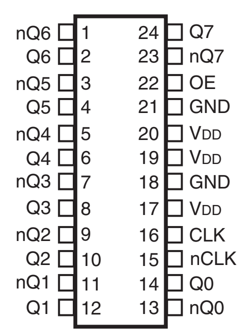
Features

- Eight differential LVDS output pairs
- CLK/nCLK can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Maximum output frequency: 700MHz
- Translates any differential input signal (LVPECL, LVHSTL, SSTL, HCSL) to LVDS levels without external bias networks
- Translates any single-ended input signal to LVDS with resistor bias on nCLK input
- Output skew: 50ps (maximum)
- Part-to-part skew: 550ps (maximum)
- Propagation delay: 2.4ns (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS85408

24-Lead TSSOP
4.4mm x 7.8mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	nQ6, Q6	Output		Differential output pair. LVDS interface levels.
3, 4	nQ5, Q5	Output		Differential output pair. LVDS interface levels.
5, 6	nQ4, Q4	Output		Differential output pair. LVDS interface levels.
7, 8	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
9, 10	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
11, 12	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
13, 14	nQ0, Q0	Output		Differential output pair. LVDS interface levels.
15	nCLK	Input	Pullup	Inverting differential clock input.
16	CLK	Input	Pulldown	Non-inverting differential clock input.
17, 19, 20	V_{DD}	Power		Positive supply pins.
18, 21	GND	Power		Power supply ground.
22	OE	Input	Pullup	Output enable. Controls the enabling and disabling of outputs Qx, nQx. When HIGH, the outputs are enabled. When LOW, the outputs are in High-Impedance. LVCMOS / LVTTL interface levels.
23, 24	nQ7, Q7	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance (per output)			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Output Enable Function Table

Inputs	Outputs
OE	**Q[0:7], nQ[0:7]**
0	High-Impedance
1	Active (default)

Table 3B. Clock Input Function Table

Inputs		Outputs		Input to Output Mode	Polarity
CLK	**nCLK**	**Q[0:7]**	**nQ[0:7]**		
0	1	LOW	HIGH	Differential to Differential	Non-Inverting
1	0	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, *Wiring the Differential Input to Accept Single-Ended Levels.*

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O (LVDS) Continuos Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. LVDS Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				90	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nCLK	$V_{DD} = V_{IN}$ = 3.465V			5	
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	$R_L = 100\Omega$	250	400	600	mV
ΔV_{OD}	V_{OD} Magnitude Change	$R_L = 100\Omega$			50	mV
V_{OS}	Offset Voltage	$R_L = 100\Omega$	1.125	1.4	1.6	V
ΔV_{OS}	V_{OS} Magnitude Change	$R_L = 100\Omega$			50	mV
I_{OZ}	High Impedance Leakage		-10		+10	µA
I_{OFF}	Power Off Leakage		-1		+1	µA
I_{OSD}	Differential Output Short Circuit Current				-5.5	mA
I_{OS}/I_{OSB}	Output Short Circuit Current				-12	mA

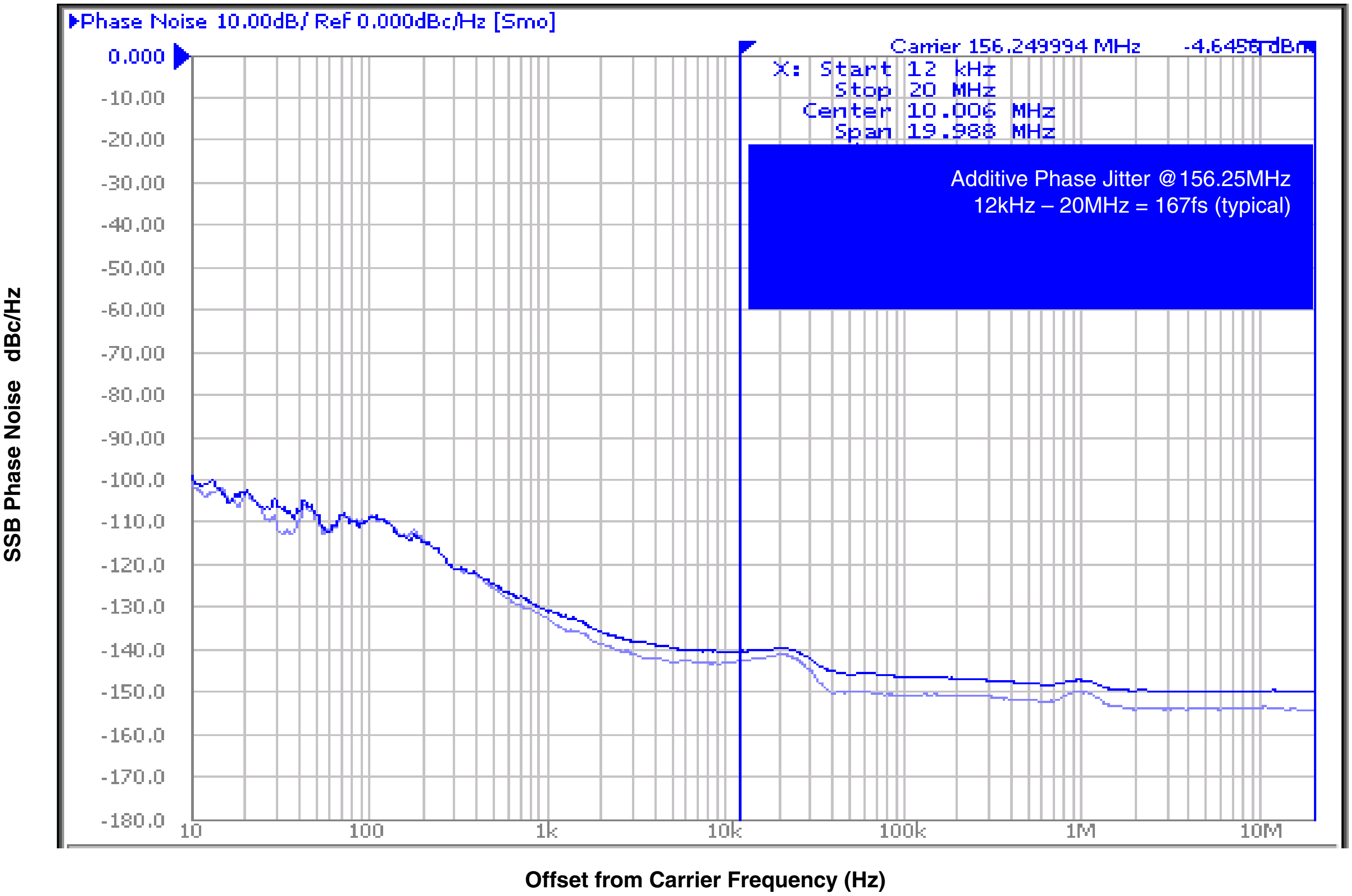
Table 5. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				700	MHz
t_{PD}	Propagation Delay; NOTE 1		1.6		2.4	ns
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	156.25MHz, Integration Range: (12kHz – 20MHz)		167		fs
tsk(o)	Output Skew; NOTE 2, 4				50	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 4				550	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		600	ps
odc	Output Duty Cycle		45		55	%
t_{PZL}, t_{PZH}	Output Enable Time; NOTE 5				5	ns
t_{PLZ}, t_{PHZ}	Output Disable Time; NOTE 5				5	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at $f \le$ 622MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crossing point of the input to the differential output crossing point.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

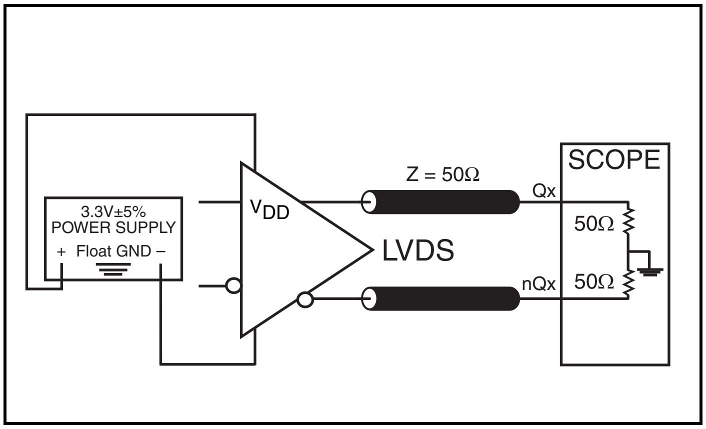
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

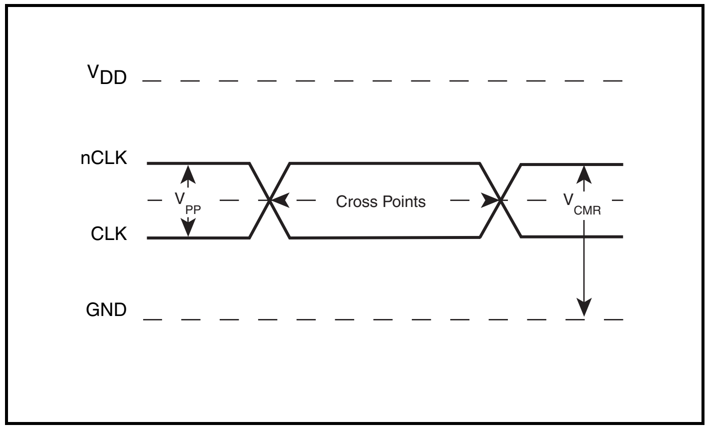


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

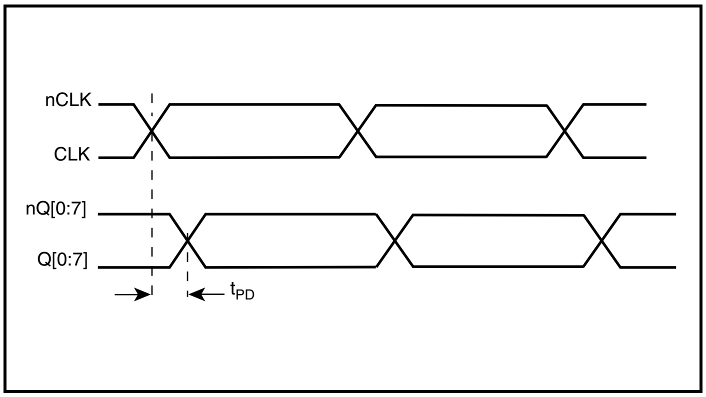
Parameter Measurement Information



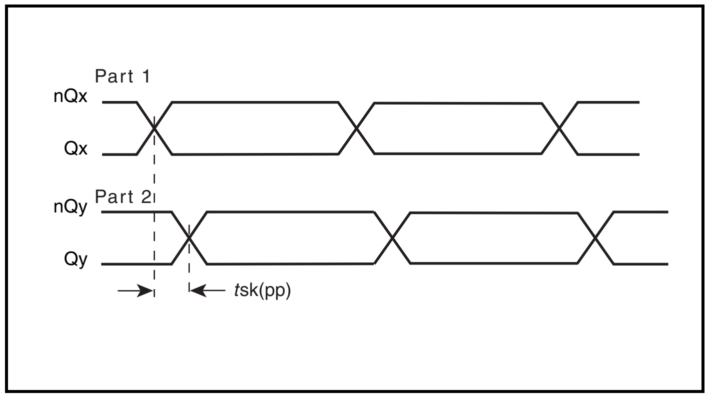
3.3V LVDS Output Load AC Test Circuit



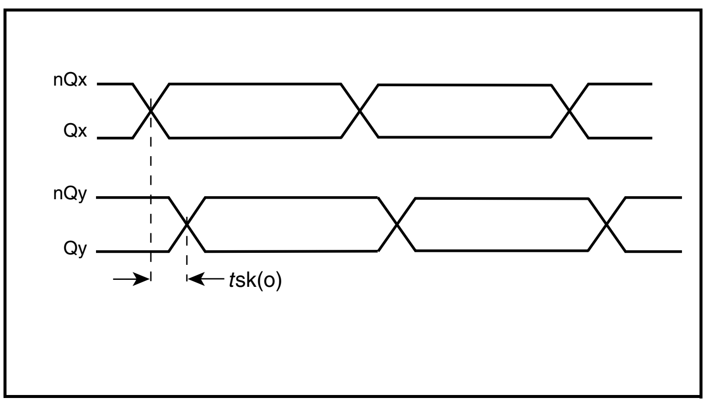
Differential Input Level



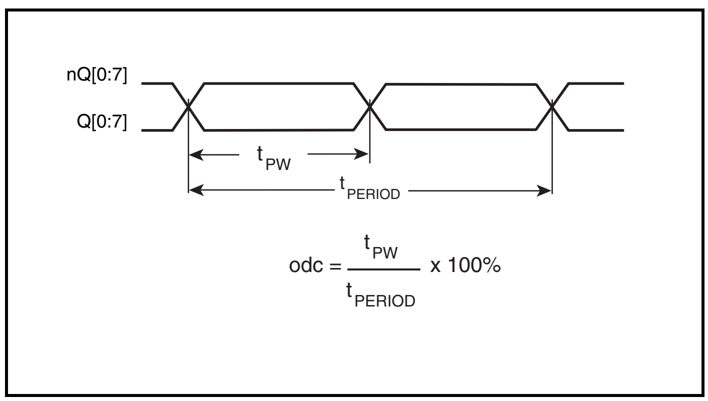
Propagation Delay



Part-to-Part Skew

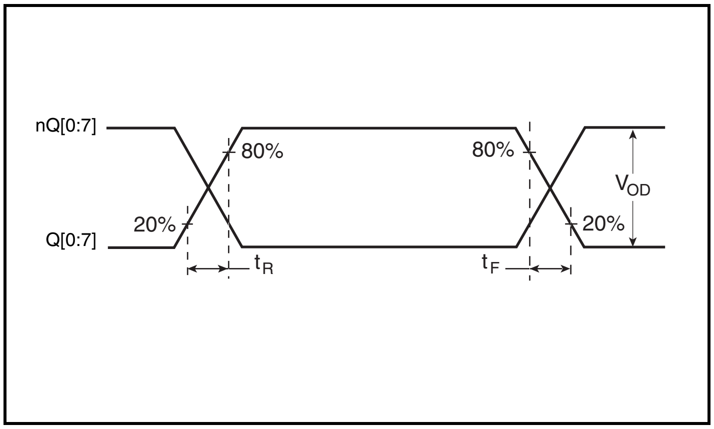


Output Skew

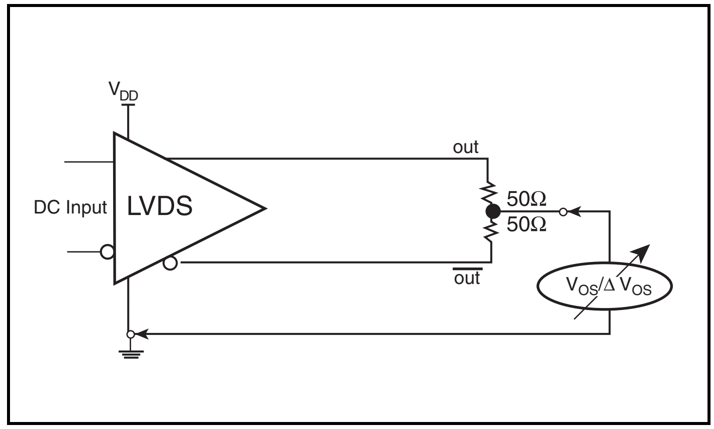


Output Duty Cycle/Pulse Width/Period

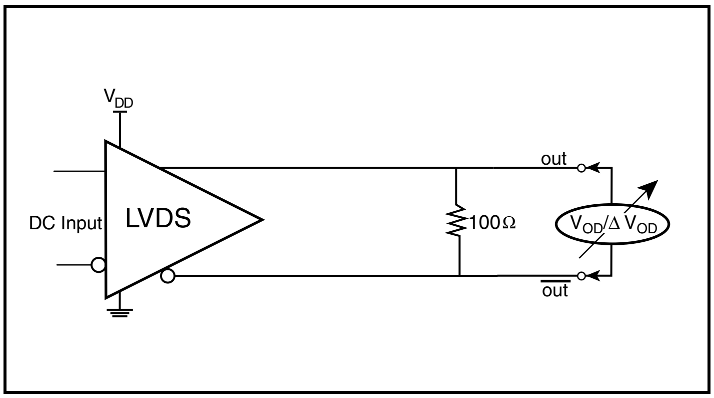
Parameter Measurement Information, continued



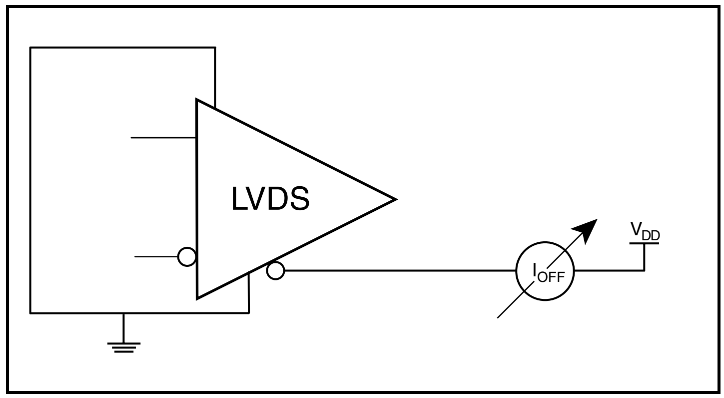
Output Rise/Fall Time



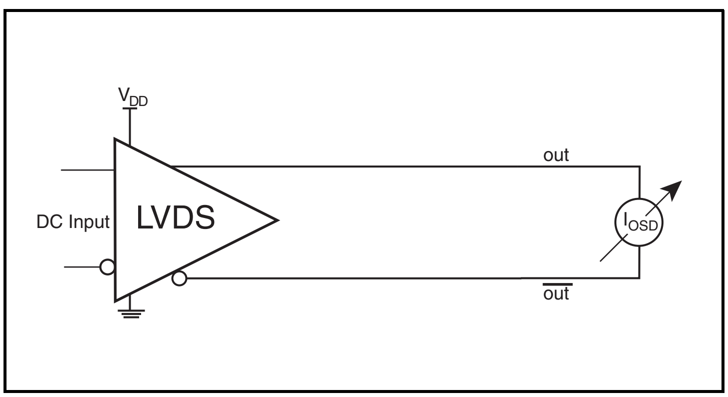
Offset Voltage Setup



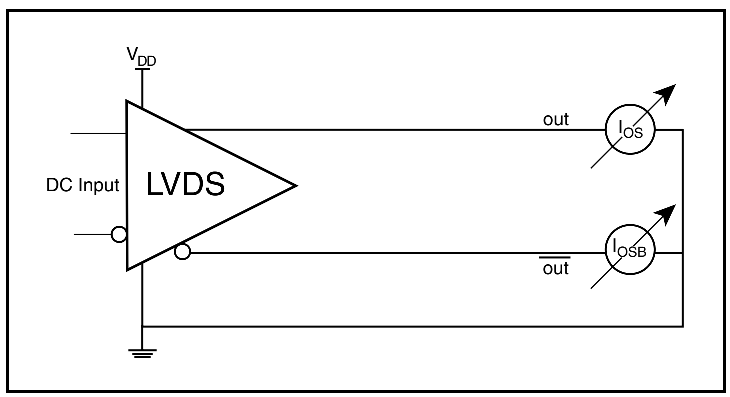
Differential Output Voltage Setup



Power Off Leakage Setup



Differential Output Short Circuit Setup



Output Short Circuit Current Setup

Application Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how the differential input can be wired to accept single-ended levels. The reference voltage V_REF = $V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

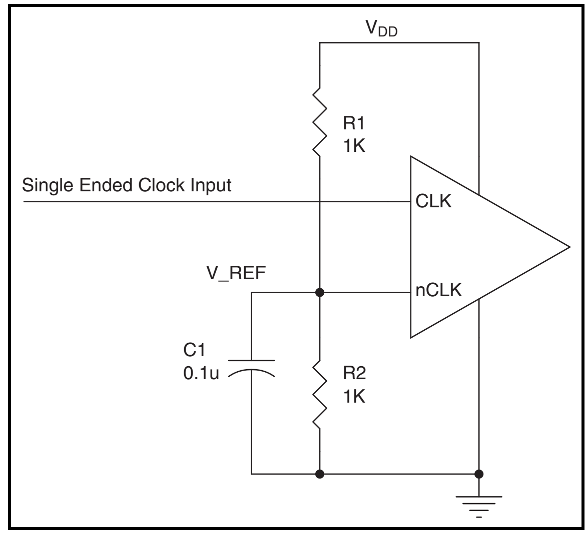


Figure 1. Single-Ended Signal Driving Differential Input

Recommendations for Unused Output Pins

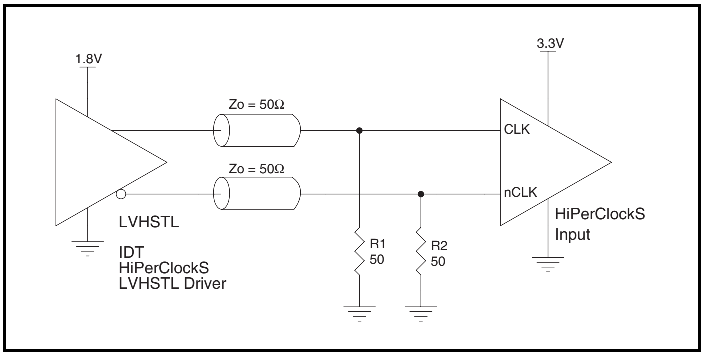
Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



2A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

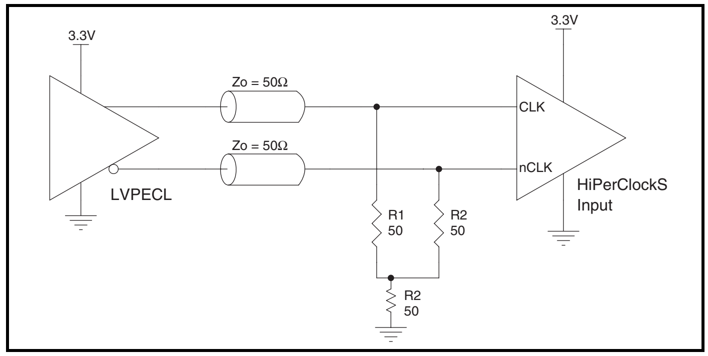


Figure 2B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

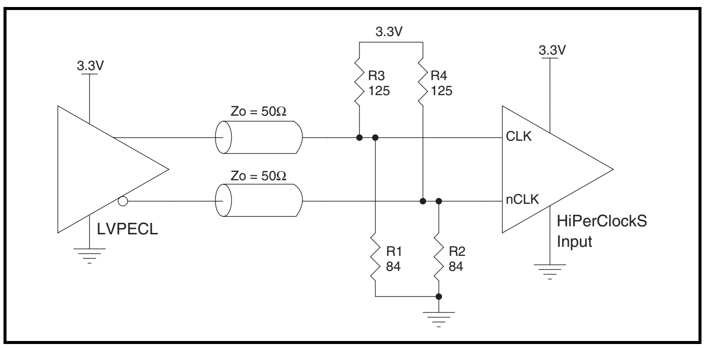


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

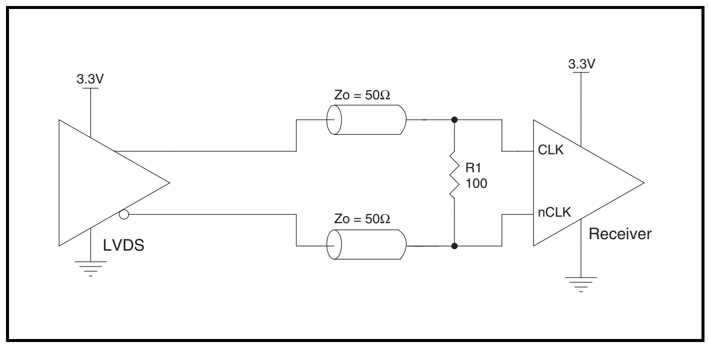


Figure 2D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

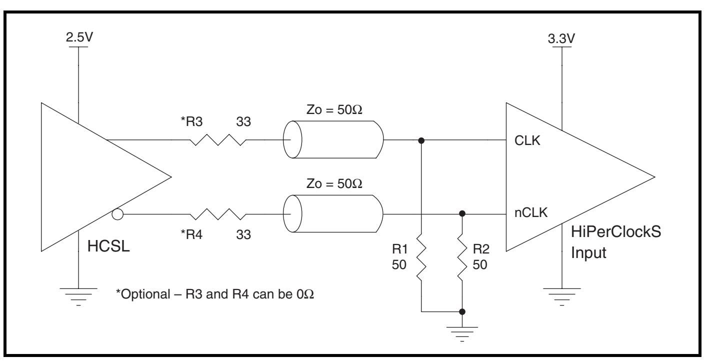


Figure 2E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

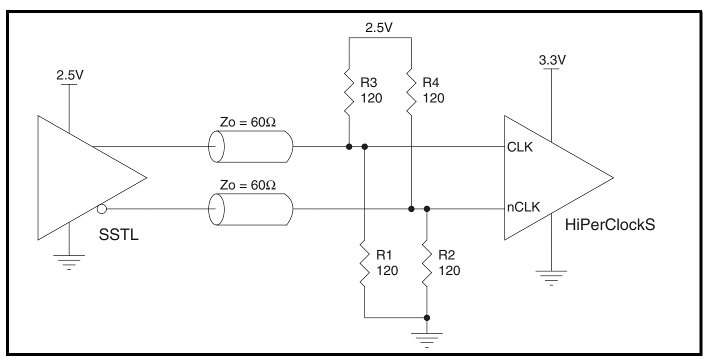


Figure 2F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

3.3V LVDS Driver Termination

A general LVDS interface is shown in *Figure 3.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

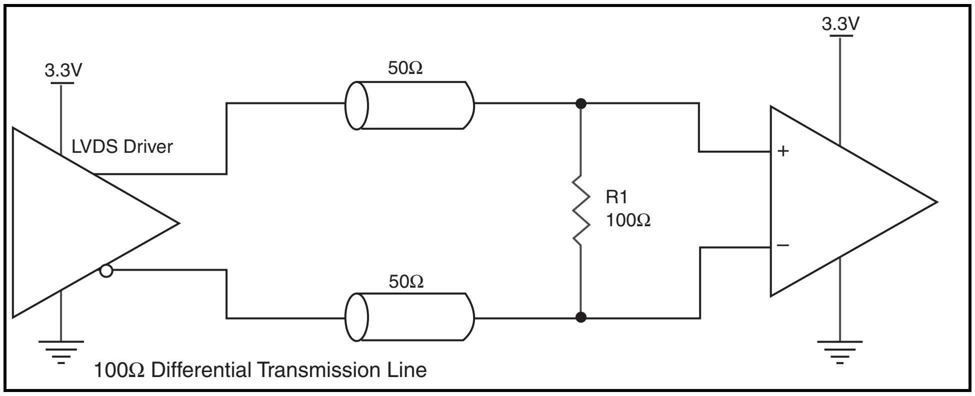


Figure 3. Typical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS85408.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS85408 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 90mA = **311.85mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 70°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.312W * 70°C/W = 91.8°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 24 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65.0°C/W	62°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65.0°C/W	62°C/W

Transistor Count

The transistor count for ICS85408 is: 1821

Pin compatible with SN65LVDS104

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

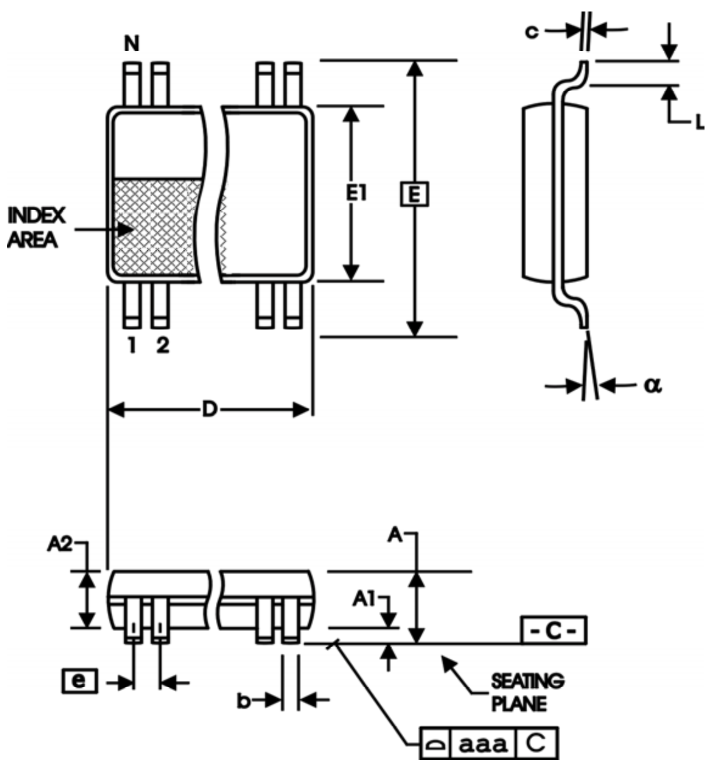


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
85408BG	ICS85408BG	24 Lead TSSOP	Tube	0°C to 70°C
85408BGT	ICS85408BG	24 Lead TSSOP	1000 Tape & Reel	0°C to 70°C
85408BGLF	ICS85408BGLF	“Lead-Free” 24 Lead TSSOP	Tube	0°C to 70°C
85408BGLFT	ICS85408BGLF	“Lead-Free” 24 Lead TSSOP	1000 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T6 T8	9 11	Reliability Table - revised air flow from Linear Feet per Minute to Meters per Second. Ordering Information Table - corrected typo in Part/Order Number from ICS8540BG to ICS85408BG.	5/6/04
A		1	Pin Assignment - corrected package information from 300-MIL to 173-MIL.	8/25/04
A	 T8	1 11	Features Section - added *Lead-Free* bullet. Corrected Block Diagram. Ordering Information Table - added *Lead-Free* information.	4/25/05
A	T8	11	Ordering Information Table - added *Lead-Free* part number.	12/6/07
B	T5	5 6 12	AC Characteristics Table - added Additive Phase Jitter spec. Added Additive Phase Jitter Plot. Added *Power Considerations* section. Converted datasheet format.	6/24/09

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