



LOW VOLTAGE PLL CLOCK DRIVER

IDT5V9351

FEATURES:

- Fully integrated PLL
- Output frequency up to 200MHz
- 2.5V and 3.3V Compatible
- Compatible with PowerPC™, Intel, and high performance RISC microprocessors
- Output frequency configurable
- Cycle-to-cycle jitter max. 22ps RMS
- Compatible with MPC9351
- Available in TQFP package

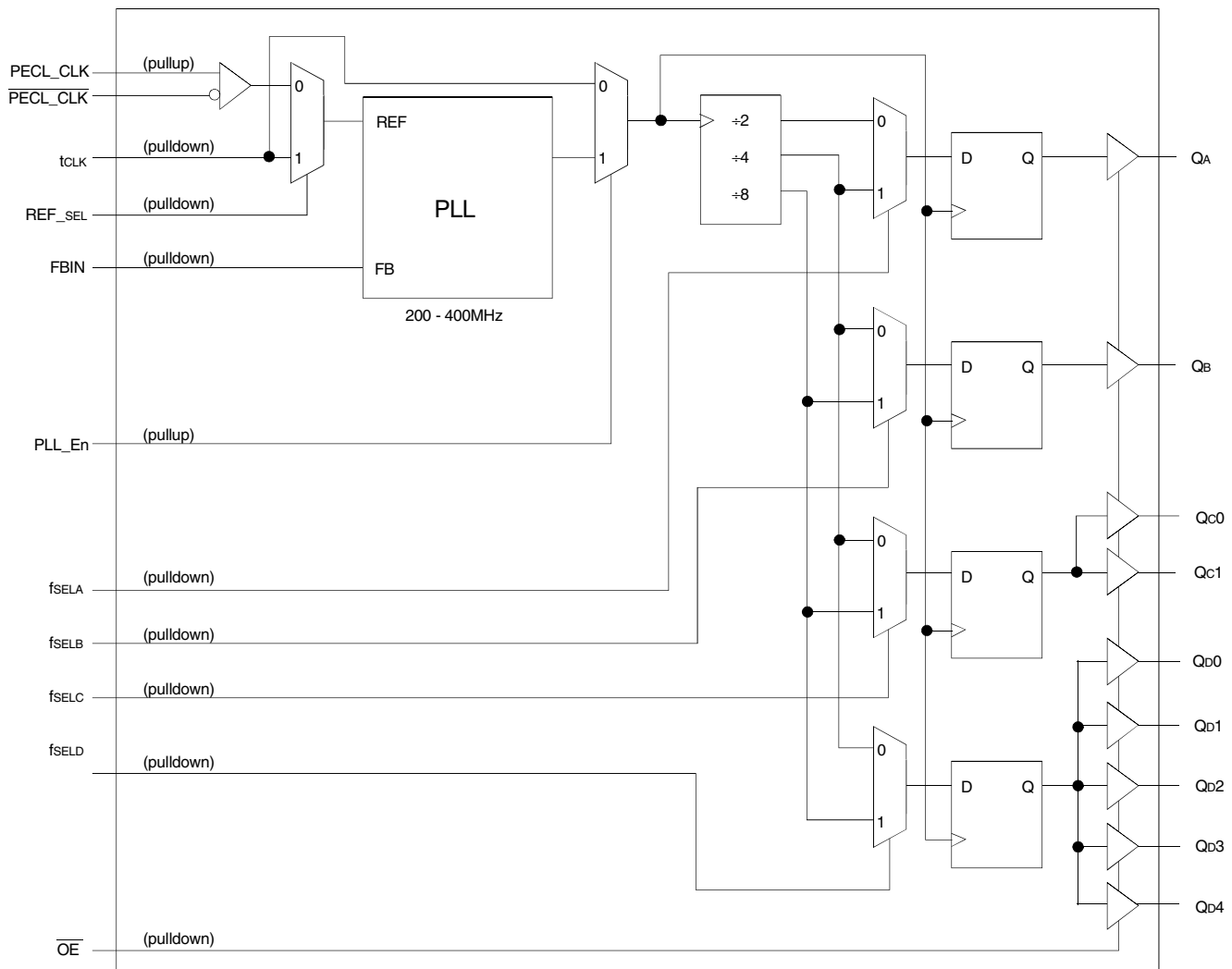
DESCRIPTION:

The IDT5V9351 is a high performance, zero delay, low skew, phase-lock loop (PLL) clock driver. It has four banks of configurable outputs. The IDT5V9351 uses a differential PECL reference input and an external feedback input. These features allow the IDT5V9351 to be used as a zero delay, low skew fan-out buffer. REF_SEL allows selection between PECL input or TCLK, a CMOS clock driver input.

If PLL_EN is set to low and REF_SEL to high, it will bypass the PLL. By doing so, the IDT5V9351 will be in clock buffer mode. Any clock applied to TCLK will be divided down to four output banks.

When PLL_EN is set high, PLL is enabled. Any clock applied to TCLK will be clocked in both phase and frequency to FBIN. PECL clock is activated by setting REF_SEL to low.

FUNCTIONAL BLOCK DIAGRAM

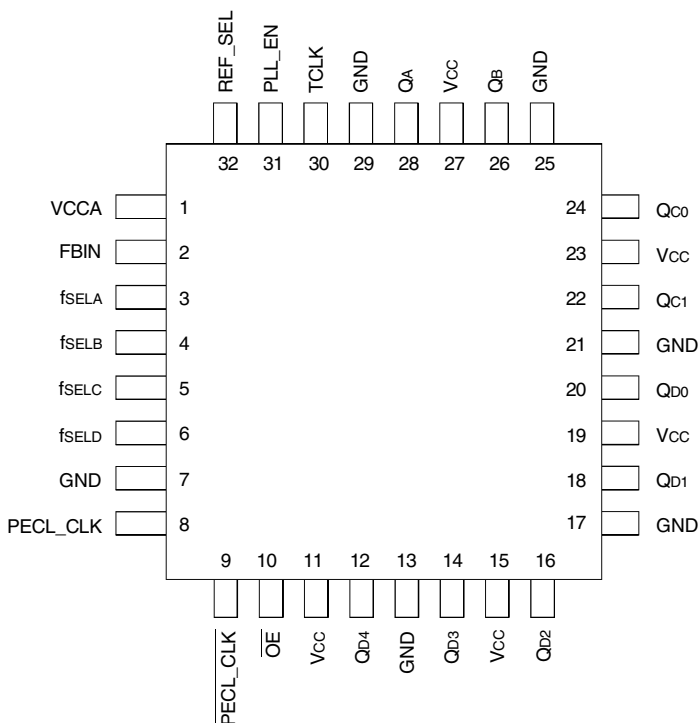


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INDUSTRIAL TEMPERATURE RANGE

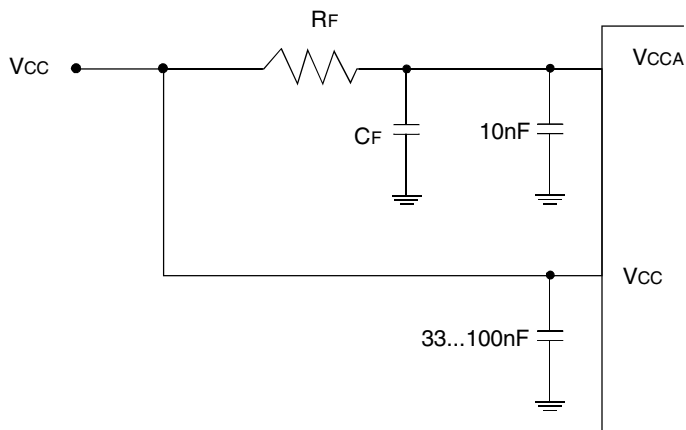
MARCH 2003

PIN CONFIGURATION



TQFP
TOP VIEW

LOGIC DIAGRAM^(1,2)



NOTES:

- IDT5V9351 requires an external RC filter for the analog power supply pin VCCA.
- For $V_{CC} = 2.5V$, $R_F = 9-10\Omega$, $C_F = 22\mu F$.
For $V_{CC} = 3.3V$, $R_F = 5-15\Omega$, $C_F = 22\mu F$.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max.	Unit
V _{CC}	Supply Voltage	-0.3 to +4.6	V
V _I	Input Voltage	-0.3 to V _{CC} +0.3	V
V _O	DC Output Voltage	-0.3 to V _{CC} +0.3	V
I _{IN}	Input Current	±20	mA
I _O	DC Output Current	±50	mA
T _{STG}	Storage Temperature	-55 to +150	°C

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit
C _{IN}	Input Capacitance	—	4	—	pF
C _{PD}	Power Dissipation Capacitance	—	10	—	pF

GENERAL SPECIFICATIONS

Symbol	Description	Min.	Typ.	Max.	Unit
V _{TT}	Output Termination Voltage		V _{CC} /2		V
HBM	ESD (Human Body Model)	2000			V
LU	Latch-Up Immunity	200			mA

PIN DESCRIPTION

Terminal		Type	Description
Name	No.		
PECL-CLK PECL-CLK	8, 9	I	Differential clock reference, LOW voltage positive ECL input
TCLK	30	I	Single-ended reference clock signal or test clock
FBIN	2	I	Feedback signal input
REF_SEL	32	I	Reference clock input
fSEL(D:A)	3, 4, 5, 6	I	Frequency control pin
\overline{OE}	10	I	Output enable/disable
QA	28	O	Bank A clock output
QB	26	O	Bank B clock output
QC(1:0)	22, 24	O	Bank C clock output
QD(4:0)	12, 14, 16, 18, 20	O	Bank D clock output
VCCA	1	PWR	Positive power supply for PLL
VCC	11, 15, 19, 23, 27	PWR	Positive power supply for I/O and core
GND	7, 13, 17, 21, 25, 29	Ground	Negative power supply
PLL_EN	31	I	PLL enable input. When set HIGH, PLL is enabled. When set LOW, PLL is disabled.

FUNCTIONALITY

Control	Default	0	1
REF_SEL	0	Selects PECL_CLK as reference clock	Selects TCLK as reference clock
PLL_EN	1	Test mode with PLL Disabled	PLL Enabled
OE	0	Outputs enabled	Outputs disabled
FSELA	0	$Q_A = V_{CO} \div 2$	$Q_A = V_{CO} \div 4$
FSELB	0	$Q_B = V_{CO} \div 4$	$Q_B = V_{CO} \div 8$
FSELC	0	$Q_C = V_{CO} \div 4$	$Q_C = V_{CO} \div 8$
FSELD	0	$Q_D = V_{CO} \div 4$	$Q_D = V_{CO} \div 8$

NOTE:

1. Output frequency relationship with respect to input reference frequency CLK. QC1 is connected to FBIN.

FUNCTION TABLE⁽¹⁾

INPUTS				OUTPUTS			
fSELA	fSELB	fSELC	fSELD	QA	QB	QC	QD
0	0	0	0	2 * CLK	CLK	CLK	CLK
0	0	0	1	2 * CLK	CLK	CLK	CLK ÷ 2
0	0	1	0	4 * CLK	2 * CLK	CLK	2 * CLK
0	0	1	1	4 * CLK	2 * CLK	CLK	CLK
0	1	0	0	2 * CLK	CLK ÷ 2	CLK	CLK
0	1	0	1	2 * CLK	CLK ÷ 2	CLK	CLK ÷ 2
0	1	1	0	4 * CLK	CLK	CLK	2 * CLK
0	1	1	1	4 * CLK	CLK	CLK	CLK
1	0	0	0	CLK	CLK	CLK	CLK
1	0	0	1	CLK	CLK	CLK	CLK ÷ 2
1	0	1	0	2 * CLK	2 * CLK	CLK	2 * CLK
1	0	1	1	2 * CLK	2 * CLK	CLK	CLK
1	1	0	0	CLK	CLK ÷ 2	CLK	CLK
1	1	0	1	CLK	CLK ÷ 2	CLK	CLK ÷ 2
1	1	1	0	2 * CLK	CLK	CLK	2 * CLK
1	1	1	1	2 * CLK	CLK	CLK	CLK

NOTE:

1. Output frequency relationship with respect to input reference frequency CLK. QC1 is connected to FBIN.

DC ELECTRICAL CHARACTERISTICS

TA = -40°C to +85°C, VCC = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
V _{IH}	Input HIGH Voltage	LVC MOS Inputs	2	—	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage	LVC MOS Inputs	—	—	0.8	V
V _{PP}	Peak-to-Peak Input Voltage	PECL_CLK	250	—	—	mV
V _{CMR}	Common Mode ⁽¹⁾	PECL_CLK	1	—	V _{CC} - 0.6	V
V _{OH}	Output HIGH Voltage ⁽²⁾	I _{OH} = -24mA	2.4	—	—	V
V _{OL}	Output LOW Voltage ⁽²⁾	I _{OL} = 24mA	—	—	0.55	V
		I _{OL} = 12mA	—	—	0.3	
Z _{OUT}	Output Impedance		—	14 - 17	—	Ω
I _{IN}	Input Leakage Current		—	—	±150	μA
I _{CC}	Maximum Quiescent Supply Current	All V _{CC} Pins	—	—	1	mA
I _{CCPLL}	Maximum PLL Supply Current	V _{CCA} Only	—	3	5	mA

NOTES:

- V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
- The IDT5V9351 outputs can drive series or parallel terminated 50Ω (or 50Ω to V_{CC}/2) transmission lines on the incident edge.

PLL INPUT REFERENCE CHARACTERISTICS

V_{CC} = 3.3V ± 5%, T_A = -40°C to +85°C

Symbol	Parameter	Min.	Max	Unit	
t _R , t _F	TCLK Input Rise/Fall Levels, 0.8V to 2V	—	1	ns	
f _{REF}	Reference Input Frequency ⁽¹⁾	÷ 2 feedback	100	200	MHz
		÷ 4 feedback	50	100	
		÷ 8 feedback	25	50	
	Static Test Mode	0	300		
f _{REFDC}	Reference Input Duty Cycle	25	75	%	

NOTE:

1. Maximum and minimum input reference is limited by the VCO lock range and the feedback divider for the TCLK or PECL_CLK inputs.

AC ELECTRICAL CHARACTERISTICS ⁽¹⁾

T_A = -40°C to +85°C, V_{CC} = 3.3V ± 5%

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit	
t _R , t _F	Output Rise/Fall Time	0.55V to 2.4V	0.1	—	1	ns	
V _{PP}	Peak-to-Peak Input Voltage	LVPECL	500	—	1000	mV	
V _{CMR}	Common Mode Range ⁽²⁾	LVPECL	1.2	—	V _{CC} - 0.9	V	
t _{DW}	Output Duty Cycle	100-200 MHz	45	50	55	%	
		50-100 MHz	47.5	50	52.5		
		25-50 MHz	48.75	50	51.75		
t _{sk(o)}	Output to Output Skew		—	—	150	ps	
f _{VCO}	PLL VCO Lock Range		200	—	400	MHz	
f _{MAX}	Maximum Output Frequency	÷ 2 output	100	—	200	MHz	
		÷ 4 output	50	—	100		
		÷ 8 output	25	—	50		
t _{PD}	Propagation Delay (Static Phase Offset)	TCLK to FBIN	-50	—	150	ps	
		PECL_CLK to FBIN	25	—	325		
t _{PLZ} , t _{PHZ}	Output Disable Time		—	—	10	ns	
t _{PZL} , t _{PZH}	Output Enable Time		—	—	10	ns	
Bw	PLL Closed Loop Bandwidth	÷ 2 feedback	-3db point of PLL transfer characteristic	—	9 - 20	—	MHz
		÷ 4 feedback		—	3 - 9.5	—	
		÷ 8 feedback		—	1.2 - 2.1	—	
t _J	Cycle-to-Cycle Jitter ÷ 4 feedback (Single Output Frequency Configuration)	RMS Value	—	10	22	ps	
t _{JT (PER)}	Period Jitter ÷ 4 feedback (Single Output Frequency Configuration)	RMS Value	—	8	15	ps	
t _{JT (φ)}	I/O Phase Jitter	RMS Value	—	4 - 17	—	ps	
t _{LOCK}	Maximum PLL Lock Time		—	—	1	ms	

NOTES:

- AC Characteristics apply for parallel output termination of 50Ω to V_{TT}.
- V_{CMR(AC)} is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within V_{PP(AC)} specifications.

DC ELECTRICAL CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 2.5\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	Min.	Typ.	Max	Unit
V_{IH}	Input HIGH Voltage	LVC MOS Inputs	1.7	—	$V_{CC} + 0.3$	V
V_{IL}	Input LOW Voltage	LVC MOS Inputs	—	—	0.7	V
V_{PP}	Peak-to-Peak Input Voltage	PECL_CLK	250	—	—	mV
V_{CMR}	Common Mode ⁽¹⁾	PECL_CLK	1	—	$V_{CC} - 0.6$	V
V_{OH}	Output HIGH Voltage ⁽²⁾	$I_{OH} = -15\text{mA}$	1.8	—	—	V
V_{OL}	Output LOW Voltage ⁽²⁾	$I_{OL} = 15\text{mA}$	—	—	0.6	V
I_{IN}	Input Current		—	—	± 150	μA
C_{IN}	Input Capacitance		—	4	—	pF
Z_{OUT}	Output Impedance		—	17 - 20	—	Ω
C_{PD}	Power Dissipation Capacitance		—	10	—	pF
I_{CC}	Maximum Quiescent Supply Current	All V_{CC} Pins	—	—	1	mA
I_{CCPLL}	Maximum PLL Supply Current	V_{CC} Only	—	3	5	mA

NOTES:

- V_{CMR} is the difference from the most positive side of the differential input signal. Normal operation is obtained when the HIGH input is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
- The IDT5V9351 outputs can drive series or parallel terminated 50Ω (or 50Ω to $V_{CC}/2$) transmission lines on the incident edge.

PLL INPUT REFERENCE CHARACTERISTICS

$V_{CC} = 2.5\text{V} \pm 5\%$, $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Min.	Max	Unit
t_r, t_f	TCLK Input Rise/Fall Levels, 0.7V to 1.7V	—	1	ns
f_{REF}	Reference Input Frequency ⁽¹⁾	$\div 2$ feedback	100	200
		$\div 4$ feedback	50	100
		$\div 8$ feedback	25	50
f_{REFDC}	Reference Input Duty Cycle	25	75	%

NOTE:

- Maximum and minimum input reference is limited by the VCO lock range and the feedback divider for the TCLK or PECL_CLK inputs.

AC ELECTRICAL CHARACTERISTICS ⁽¹⁾

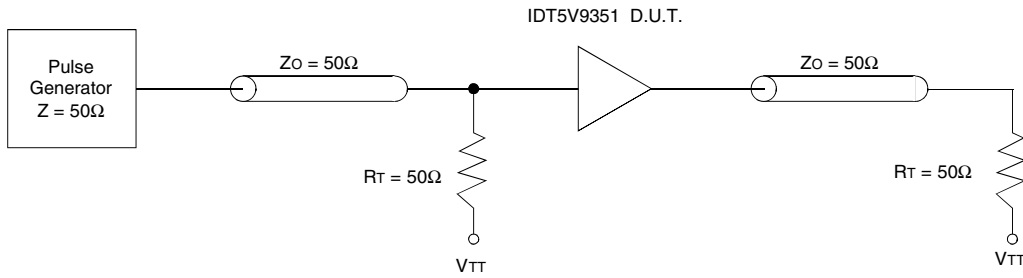
T_A = -40°C to +85°C, V_{CC} = 2.5V ± 5%

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit	
t _R , t _F	Output Rise/Fall Time	0.6V to 1.8V	0.1	—	1	ns	
V _{PP}	Peak-to-Peak Input Voltage	LVPECL	500	—	1000	mV	
V _{CMR}	Common Mode Range ⁽²⁾	LVPECL	1.2	—	V _{CC} - 0.6	V	
t _{DW}	Output Duty Cycle	100-200 MHz	45	50	55	%	
		50-100 MHz	47.5	50	52.5		
		25-50 MHz	48.75	50	51.75		
t _{SK(O)}	Output to Output Skew		—	—	150	ps	
f _{VCO}	PLL VCO Lock Range		200	—	400	MHz	
f _{MAX}	Maximum Output Frequency	÷ 2 output	100	—	200	MHz	
		÷ 4 output	50	—	100		
		÷ 8 output	25	—	50		
t _{PD}	Input to FBIN Delay	TCLK to FBIN	-100	—	100	ps	
		PECL_CLK to FBIN	0	—	300		
t _{PLZ} , t _{PHZ}	Output Disable Time		—	—	12	ns	
t _{PZL} , t _{PZH}	Output Enable Time		—	—	12	ns	
BW	PLL Closed Loop Bandwidth	÷ 2 feedback	-3db point of PLL to transfer characteristic	—	4 - 15	—	MHz
		÷ 4 feedback		—	2 - 7	—	
		÷ 8 feedback		—	0.7 - 2	—	
t _J	Cycle-to-Cycle Jitter ÷ 4 feedback (Single Output Frequency Configuration)	RMS Value	—	10	22	ps	
t _{JIT (PER)}	Period Jitter ÷ 4 feedback (Single Output Frequency Configuration)	RMS Value	—	8	15	ps	
t _{JIT (Φ)}	I/O Phase Jitter	RMS Value	—	6 - 25	—	ps	
t _{LOCK}	Maximum PLL Lock Time		—	—	1	ms	

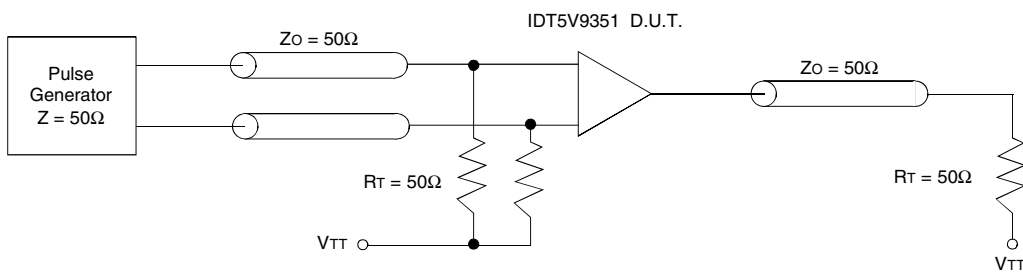
NOTES:

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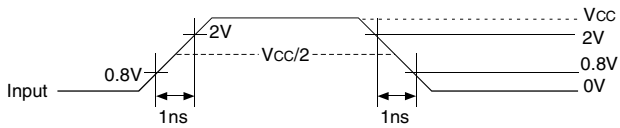
TEST CIRCUITS AND WAVEFORMS



TCLK AC Test Reference for $V_{CC} = 2.5V$ and $V_{CC} = 3.3V$



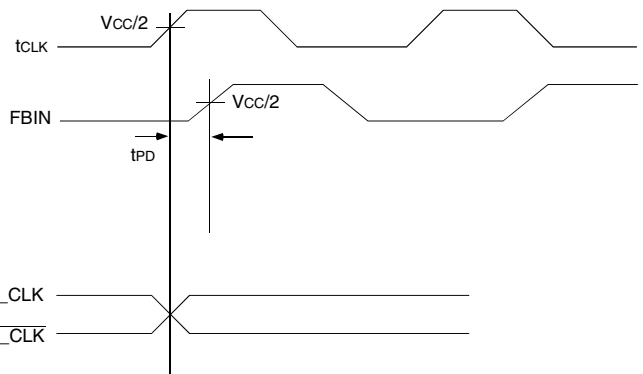
PECL_CLK AC Test Reference



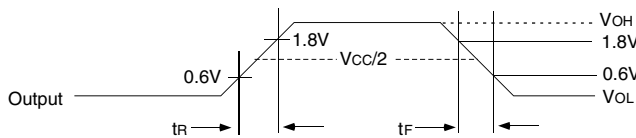
Input Characteristics for 3.3V



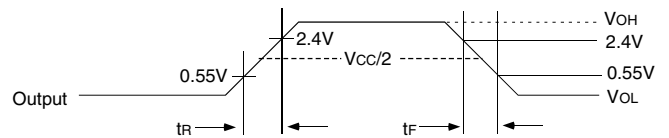
Input Characteristics for 2.5V



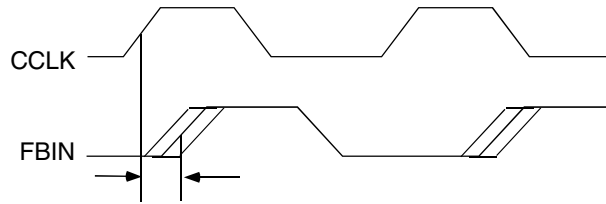
Prop Delay



Output Test Conditions for $V_{CC} = 2.5V \pm 5\%$

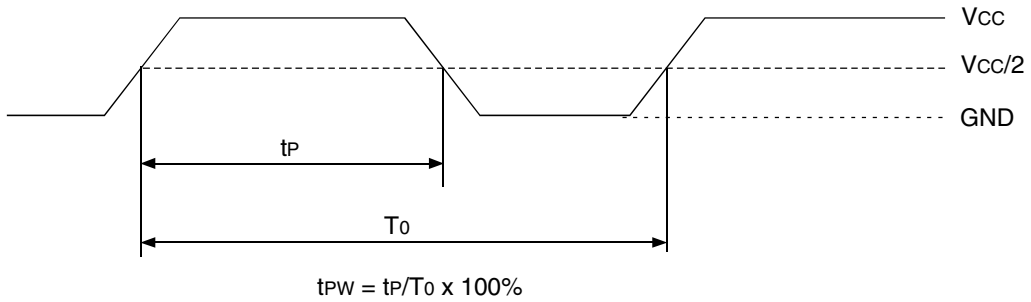


Output Test Conditions for $V_{CC} = 3.3V \pm 5\%$

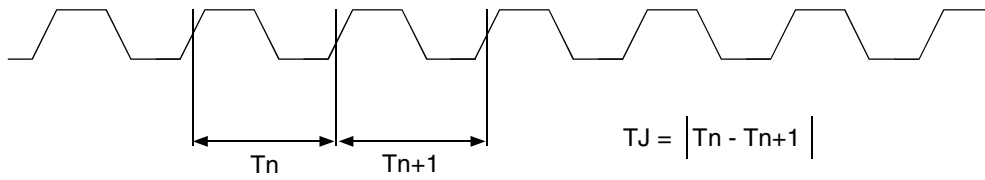


$$T_{J(0)} = |T_0 - T_1 \text{ MEAN}|$$

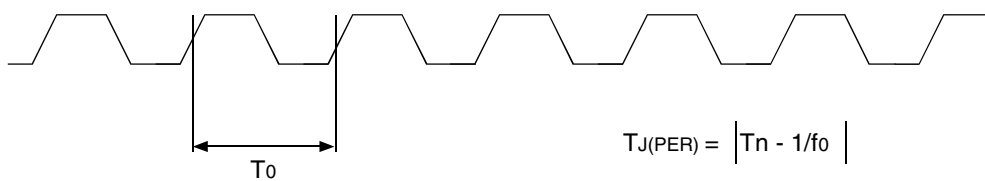
I/O Jitter



Output Duty Cycle

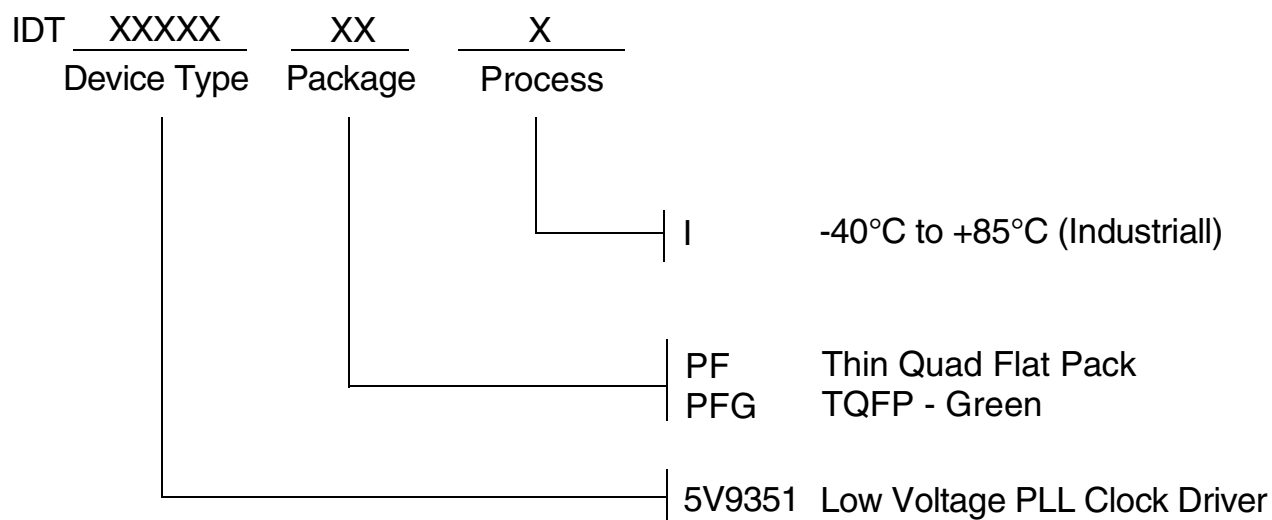


Cycle-to-Cycle Jitter



Period Jitter

ORDERING INFORMATION



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