N-Channel Enhancement-Mode Vertical DMOS FETs

Features

- Low threshold (2.0V max.)
- High input impedance
- Low input capacitance
- Fast switching speeds
- Low on-resistance
- Free from secondary breakdown
- Low input and output leakage

Applications

- Logic level interfaces - ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic drives
- Analog switches
- General purpose line drivers
- Telecom switches

General Description

This low threshold enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

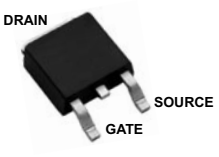
Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

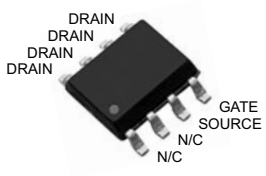
Device	Package Options				BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (max) (Ω)	$V_{GS(th)}$ (max) (V)	$I_{D(ON)}$ (min) (A)
	TO-252 (D-PAK)	8-Lead SOIC	TO-92	Die*				
TN2640	TN2640K4-G	TN2640LG-G	TN2640N3-G	TN2640ND	400	5.0	2.0	2.0

-G indicates package is RoHS compliant ('Green')
** MIL visual screening available*

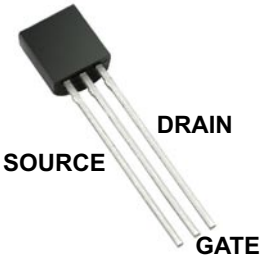
Pin Configurations



TO-252 (D-PAK) (K4)



8-Lead SOIC (LG)



TO-92 (N3)

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	+300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* *Distance of 1.6mm from case for 10 seconds.*

Product Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____= "Green" Packaging

Package may or may not include the following marks: Si or

TO-252 (D-PAK) (K4)

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8-Lead SOIC (LG)

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Package may or may not include the following marks: Si or

TO-92 (N3)

Thermal Characteristics

Package	I_D (continuous)† (mA)	I_D (pulsed) (A)	Power Dissipation @T_A = 25°C (W)	θ_{jc} (°C/W)	θ_{ja} (°C/W)	I_{DR}† (mA)	I_{DRM} (A)
TO-252 (D-PAK)	500	3.0	2.5‡	6.25	50	500	3.0
8-Lead SOIC	260	2.0	1.3‡	24	96‡	260	2.0
TO-92	220	2.0	0.74	125	170	220	2.0

Notes:

† I_D (continuous) is limited by max rated T_j.

‡ Mounted on FR4 board, 25mm x 25mm x 1.57mm

Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	400	-	-	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate threshold voltage	0.8	-	2.0	V	V_{GS} = V_{DS}, I_D = 2.0mA
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-2.5	-4.0	mV/°C	V_{GS} = V_{DS}, I_D = 2.0mA
I_{GSS}	Gate body leakage	-		100	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero gate voltage drain current	-	-	10	µA	V_{GS} = 0V, V_{DS} = Max rating
		-	-	1.0	mA	V_{DS} = 0.8 Max Rating, V_{GS} = 0V, T_A = 125°C
$I_{D(ON)}$	On-state drain current	1.5	3.5	-	A	V_{GS} = 5.0V, V_{DS} = 25V
		2.0	4.0	-		V_{GS} = 10V, V_{DS} = 25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	3.2	5.0	Ω	V_{GS} = 4.5V, I_D = 500mA
		-	3.0	5.0		V_{GS} = 10V, I_D = 500mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	0.75	%/°C	V_{GS} = 10V, I_D = 500mA
G_{FS}	Forward transconductance	200	330	-	mmho	V_{DS} = 25V, I_D = 100mA
C_{ISS}	Input capacitance	-	210	225	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	30	50		
C_{RSS}	Reverse transfer capacitance	-	8.0	15		

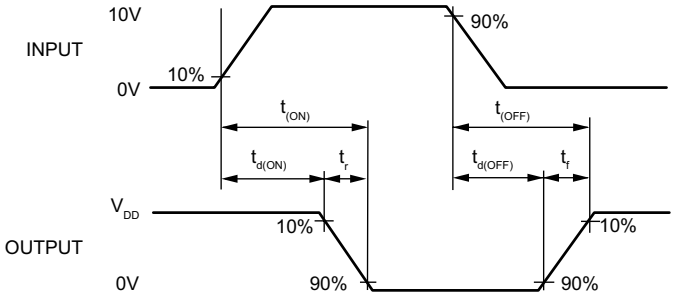
Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

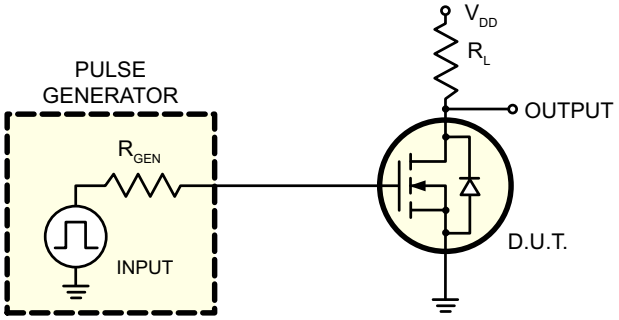
Sym	Parameter	Min	Typ	Max	Units	Conditions
$t_{d(ON)}$	Turn-on delay time	-	4.0	15	ns	V_{DD} = 25V, I_D = 2.0A, R_{GEN} = 25Ω
t_r	Rise time	-	15	20		
$t_{d(OFF)}$	Turn-off delay time	-	20	25		
t_f	Fall time	-	22	27		
V_{SD}	Diode forward voltage drop	-	-	0.9	V	V_{GS} = 0V, I_{SD} = 200mA
t_{rr}	Reverse recovery time	-	300	-	ns	V_{GS} = 0V, I_{SD} = 1.0A

Notes:

1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

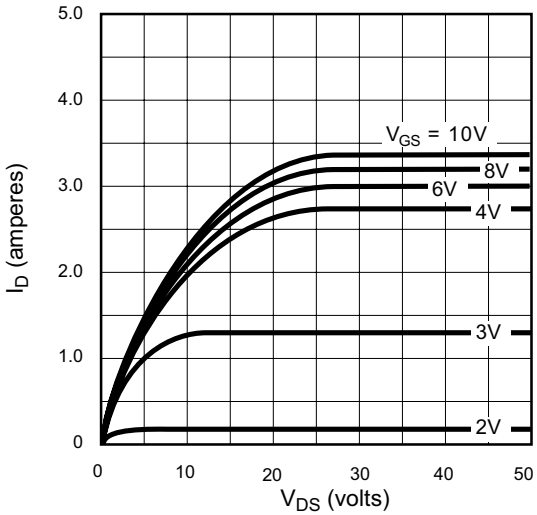
N- Channel Switching Waveforms and Test Circuit



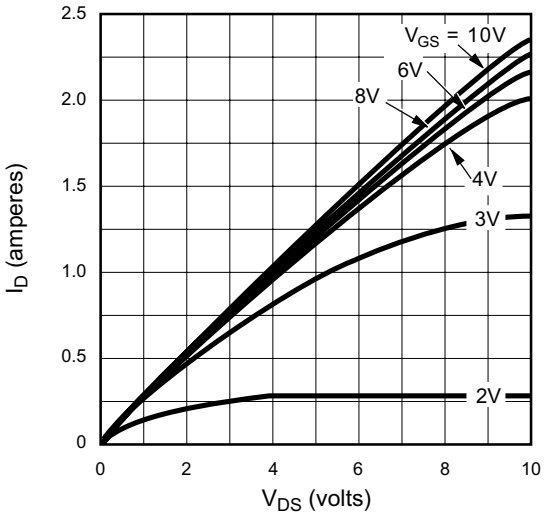


Typical Performance Curves

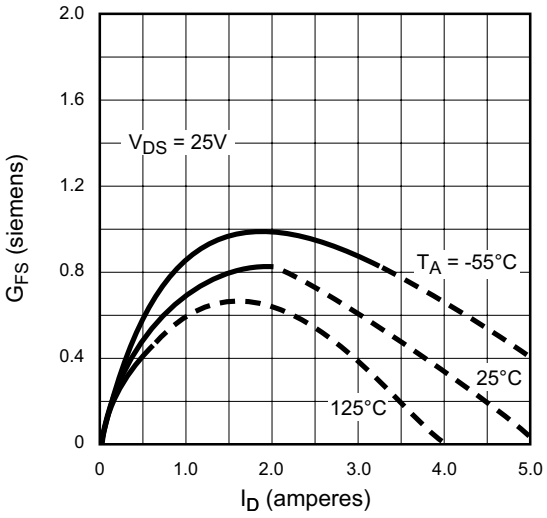
Output Characteristics



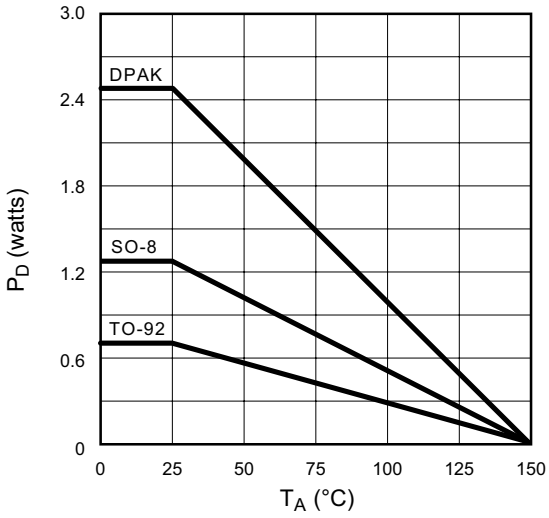
Saturation Characteristics



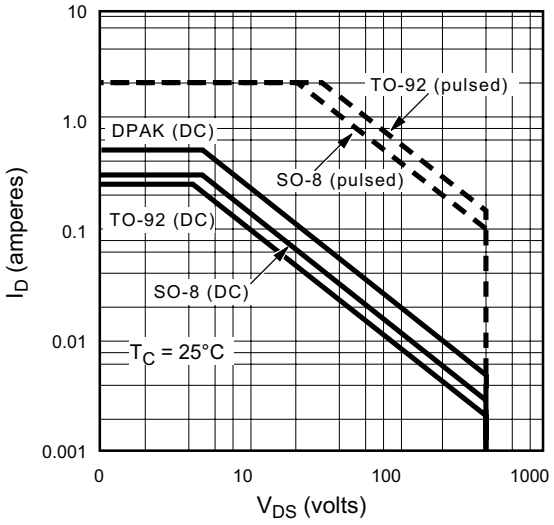
Transconductance vs. Drain Current



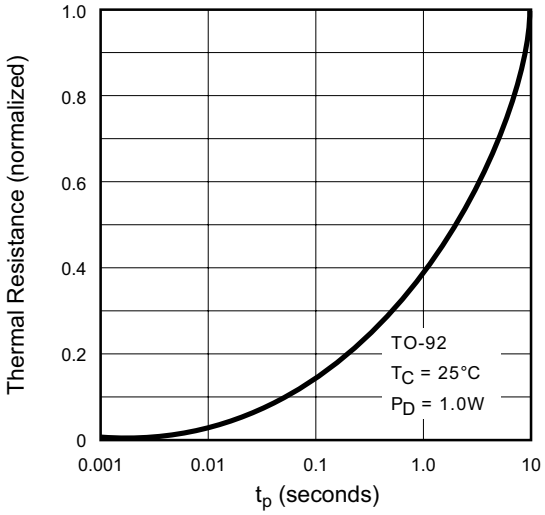
Power Dissipation vs. Temperature



Maximum Rated Safe Operating Area

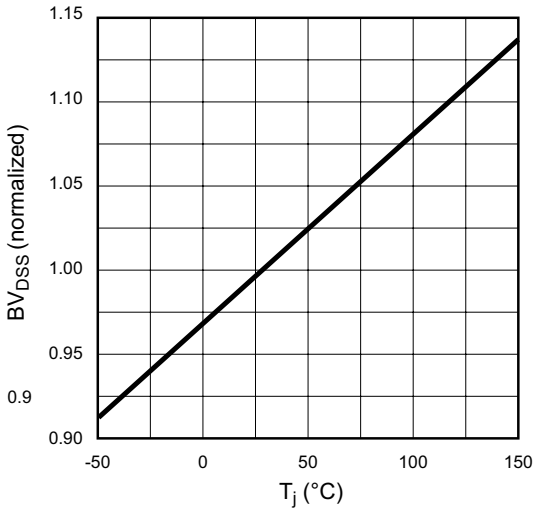


Thermal Response Characteristics

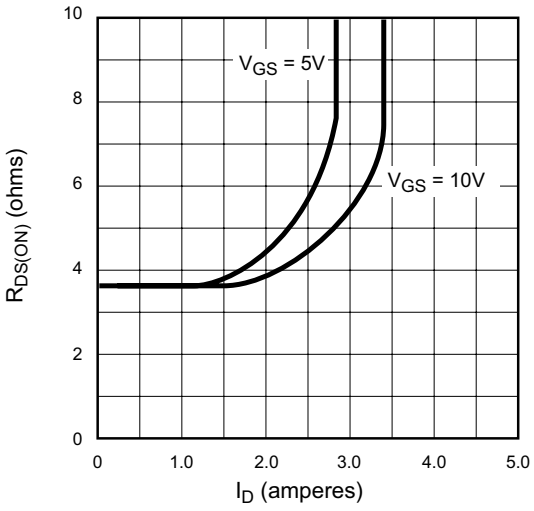


Typical Performance Curves (cont.)

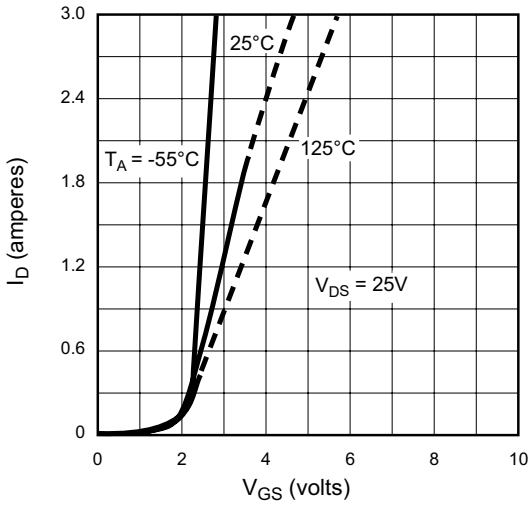
BV$_{DSS}$ Variation with Temperature



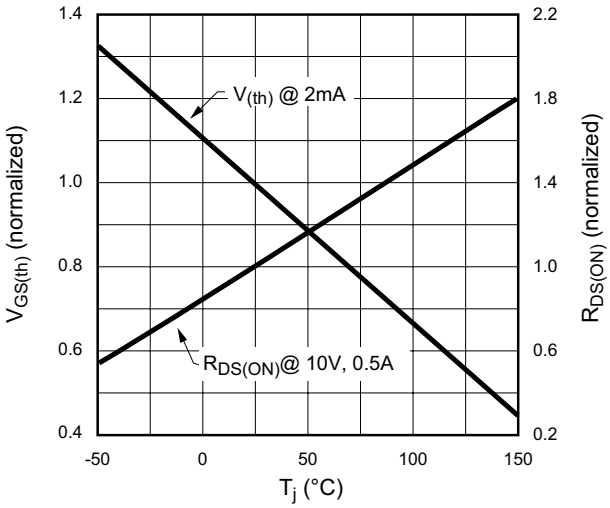
On-Resistance vs. Drain Current



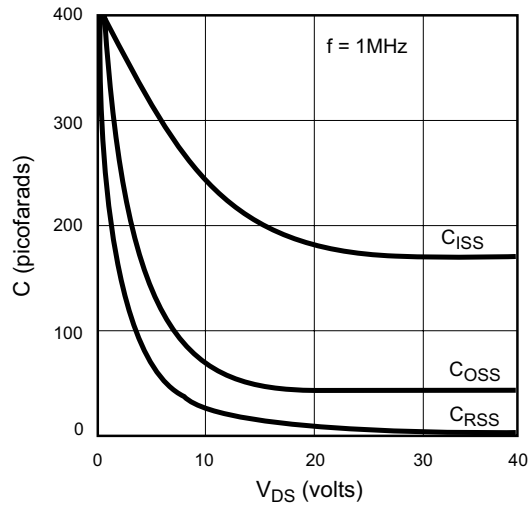
Transfer Characteristics



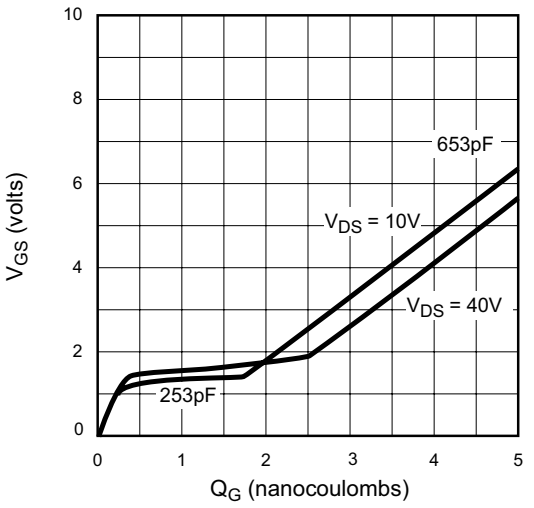
V_{TH} and R_{DS} Variation with Temperature



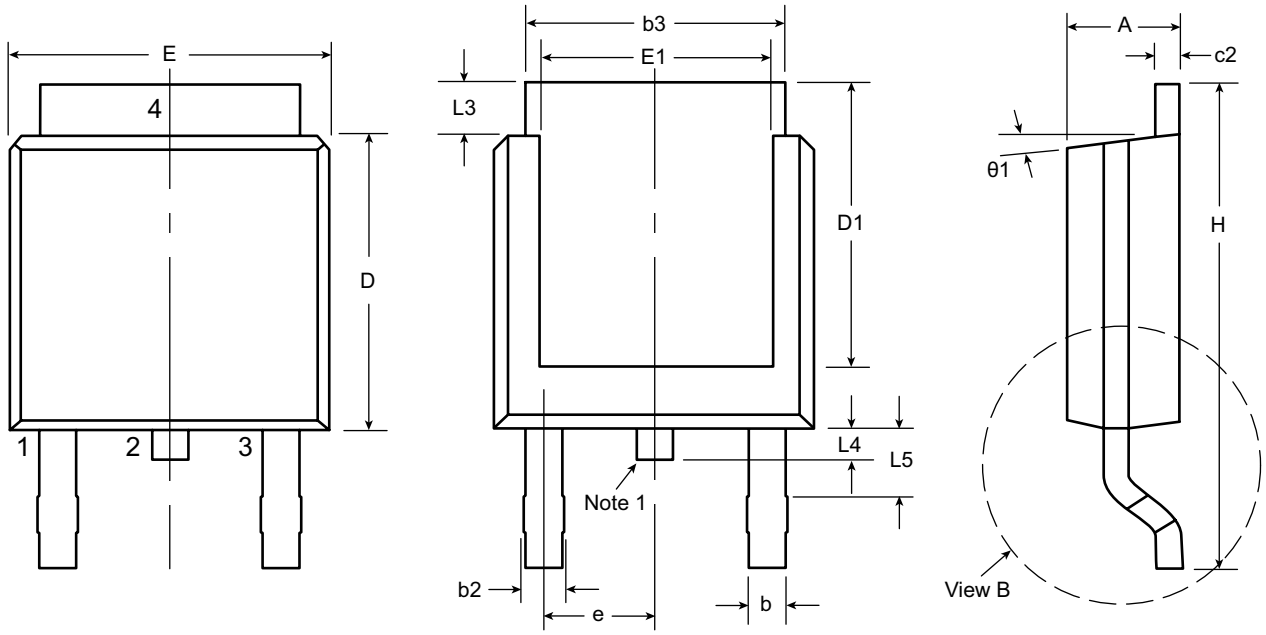
Capacitance vs. Drain-to-Source Voltage



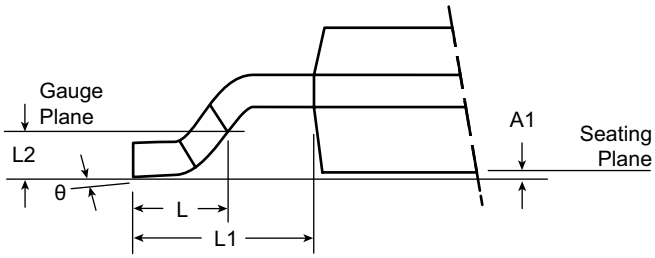
Gate Drive Dynamic Characteristics



3-Lead TO-252 D-PAK Package Outline (K4)



Front View **Rear View** **Side View**



View B

Note:

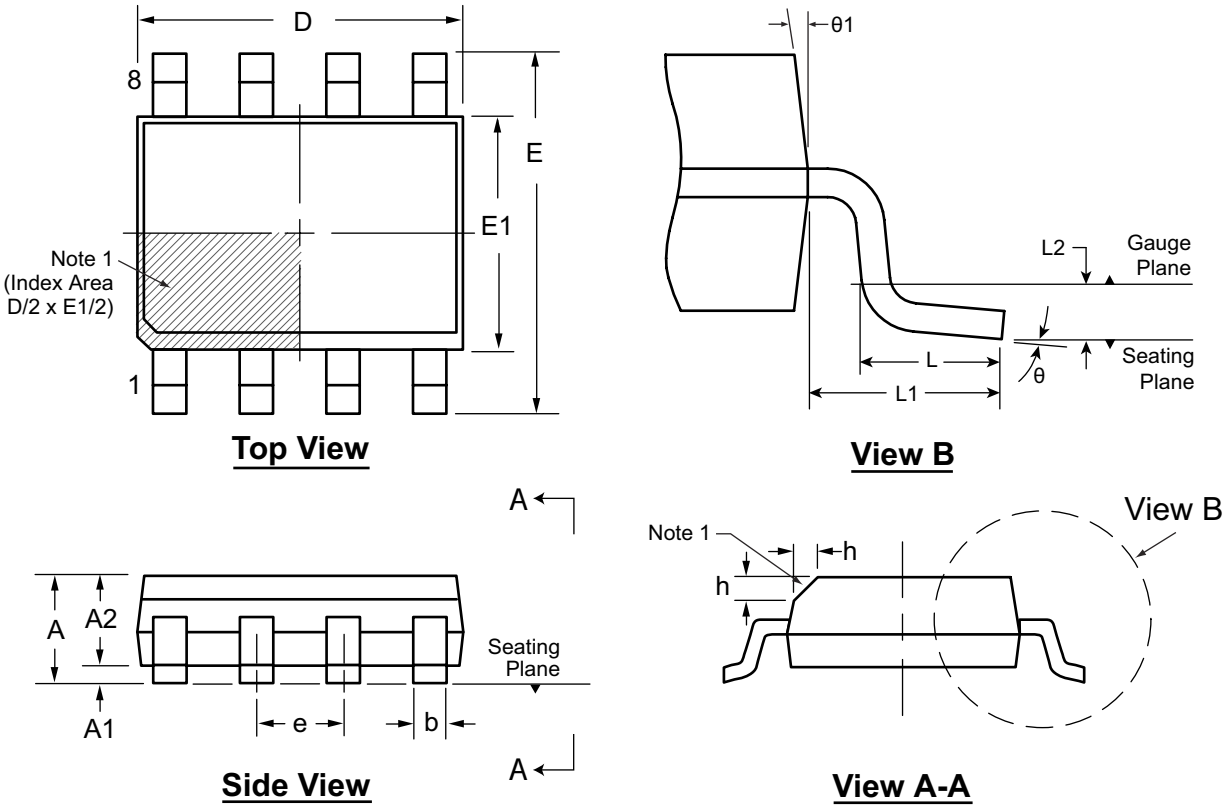
1. *Although 4 terminal locations are shown, only 3 are functional. Lead number 2 was removed.*

Symbol		A	A1	b	b2	b3	c2	D	D1	E	E1	e	H	L	L1	L2	L3	L4	L5	θ	θ1
Dimen-sion (inches)	MIN	.086	.000*	.025	.030	.195	.018	.235	.205	.250	.170	.090 BSC	.370	.055	.108 REF	.020 BSC	.035	.025*	.045	0^0	0^0
	NOM	-	-	-	-	-	-	.240	-	-	-		-	.060			-	-	-	-	-
	MAX	.094	.005	.035	.045	.215	.035	.245	.217*	.265	.182*		.410	.070			.050	.040	.060	10^0	15^0

JEDEC Registration TO-252, Variation AA, Issue E, June 2004.
** This dimension is not specified in the JEDEC drawing.*
Drawings not to scale.
Supertex Doc. #: *DSPD-3TO252K4, Version E041309.*

8-Lead SOIC (Narrow Body) Package Outline (LG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



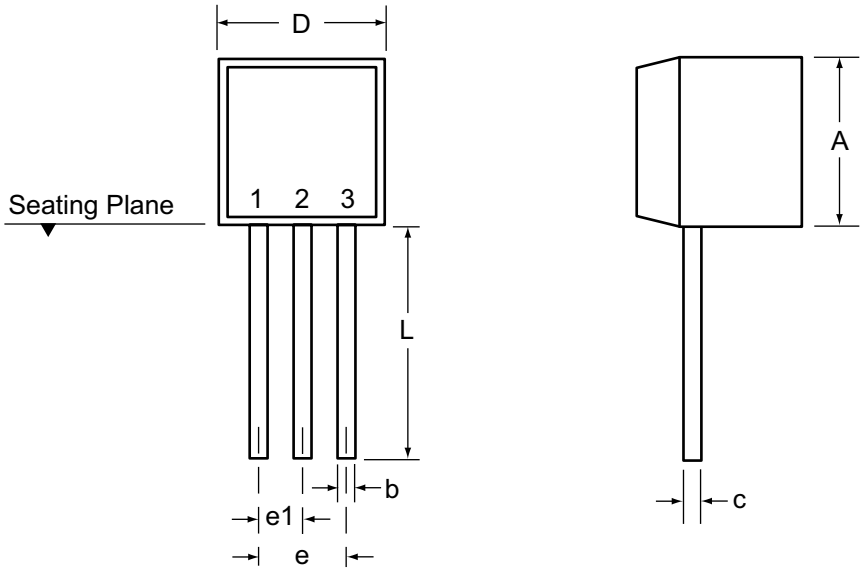
Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

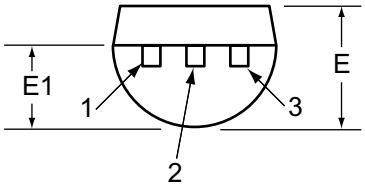
Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-8SOLGTG, Version I041309.*

3-Lead TO-92 Package Outline (N3)



Front View **Side View**



Bottom View

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
***Supertex Doc.#:** DSPD-3TO92N3, Version E041009.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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