

LM2940QML

LM2940QML 1A Low Dropout Regulator



Literature Number: SNVS389A

LM2940QML

1A Low Dropout Regulator

General Description

The LM2940 positive voltage regulator features the ability to source 1A of output current with a dropout voltage of typically 0.5V and a maximum of 1V over the entire temperature range. Furthermore, a quiescent current reduction circuit has been included which reduces the ground current when the differential between the input voltage and the output voltage exceeds approximately 3V. The quiescent current with 1A of output current and an input-output differential of 5V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode ($V_{IN} - V_{OUT} \leq 3V$).

Designed also for vehicular applications, the LM2940 and all regulated circuitry are protected from reverse battery installations or 2-battery jumps. During line transients, such as load dump when the input voltage can momentarily exceed the specified maximum operating voltage, the regulator will au-

tomatically shut down to protect both the internal circuits and the load. The LM2940 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Features

- Available with radiation guarantee
— ELDRS Free 100 krad(Si)
- Dropout voltage typically 0.5V @ $I_O = 1A$
- Output current in excess of 1A
- Output voltage trimmed before assembly
- Reverse battery protection
- Internal short circuit current limit
- Mirror image insertion protection

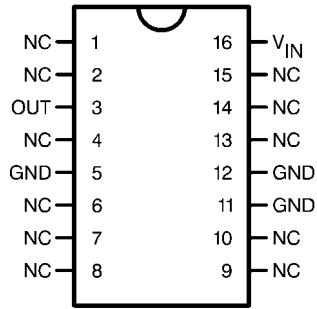
Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
LM2940WG-5.0/883	5962-8958701XA	WG16A	16LD Ceramic SOIC
LM2940WG5.0RLQV ELDRS FREE (Note 7)	5962R8958702VXA 100 krad(Si)	WG16A	16LD Ceramic SOIC
LM2940GW-5.0/883	5962-8958703XA	WG16A	16LD Ceramic SOIC
LM2940GW5.0RLQV ELDRS FREE (Note 7)	5962R8958704VXA 100 krad(Si)	WG16A	16LD Ceramic SOIC
LM2940-5.0 MDE ELDRS FREE (Note 7)	5962R8958702V9A 100 krad(Si)	(Note 1)	BARE DIE

Note 1: FOR ADDITIONAL DIE INFORMATION, PLEASE VISIT THE HI REL WEB SITE AT: www.national.com/analog/space/level_die

Connection Diagrams

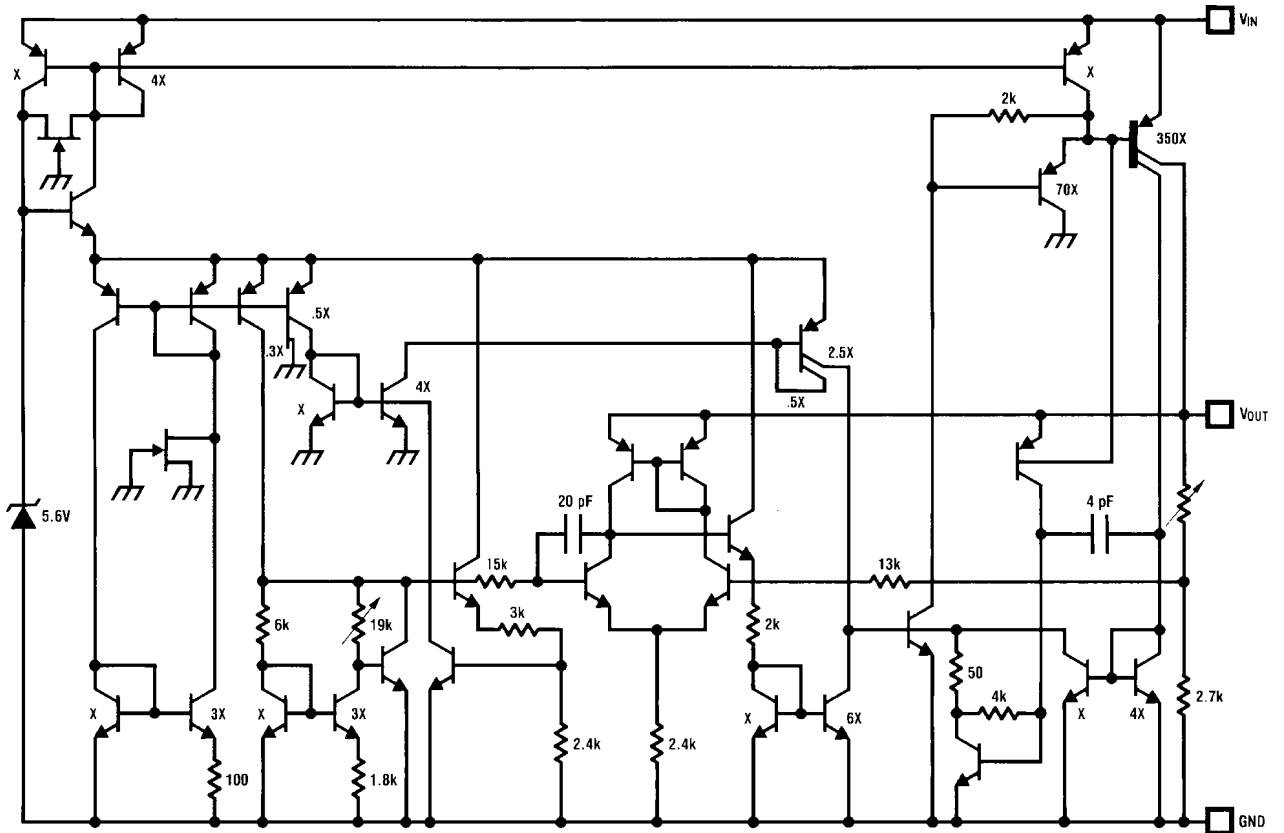
16-Lead Ceramic Surface-Mount Package (WG)



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Top View
See NS Package Number WG16A

Equivalent Schematic Diagram



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Absolute Maximum Ratings *(Note 2)*

Input Voltage (Survival Voltage $\leq 100\text{mS}$)	60V
Internal Power Dissipation with no heat sink ($T_A = +25^\circ\text{C}$) <i>(Note 3)</i>	1W
Maximum Junction Temperature	150°C
Storage Temperature Range	$-65^\circ\text{C} \leq T_A \leq +150^\circ\text{C}$
Lead Temperature (Soldering 10 seconds)	300°C
Thermal Resistance	
θ_{JA}	
16LD Ceramic SOIC (Still Air) 'WG'	122°C/W
16LD Ceramic SOIC (Still Air) 'GW'	136°C/W
16LD Ceramic SOIC (500LF/Min Air flow) 'WG'	77°C/W
16LD Ceramic SOIC (500LF/Min Air flow) 'GW'	87°C/W
θ_{JC}	
16LD Ceramic SOIC 'WG' <i>(Note 4)</i>	5°C/W
16LD Ceramic SOIC 'GW'	13°C/W
Package Weight 'WG'	360 mg
Package Weight 'GW'	410 mg
ESD Susceptibility <i>(Note 5)</i>	4KV

Recommended Operating Conditions *(Note 2)*

Input Voltage	26V
Temperature Range	$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp °C
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

LM2940-5.0 Electrical Characteristics SMD: 5962R8958701

DC Parameters

The following conditions apply, unless otherwise specified.

DC: $V_I = 10V$, $I_O = 1A$, $C_O = 22\mu F$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_O	Output Voltage	$V_{IN} = 10V$, $I_{OUT} = 5mA$		4.85	5.15	V	1
				4.75	5.25	V	2, 3
		$V_{IN} = 6V$, $I_{OUT} = 5mA$		4.85	5.15	V	1
				4.75	5.25	V	2, 3
		$V_{IN} = 7V$, $I_{OUT} = 5mA$		4.85	5.15	V	1
				4.75	5.25	V	2, 3
		$V_{IN} = 26V$, $I_{OUT} = 5mA$		4.85	5.15	V	1
				4.75	5.25	V	2, 3
		$V_{IN} = 10V$, $I_{OUT} = 1A$		4.85	5.15	V	1
				4.75	5.25	V	2, 3
$V_{IN} = 6V$, $I_{OUT} = 1A$		4.85	5.15	V	1		
		4.75	5.25	V	2, 3		
$V_{IN} = 6V$, $I_{OUT} = 50mA$		4.85	5.15	V	1		
		4.75	5.25	V	2, 3		
$V_{IN} = 10V$, $I_{OUT} = 50mA$		4.85	5.15	V	1		
		4.75	5.25	V	2, 3		
	Reverse Polarity Input Voltage DC	$R_O = 100\Omega$	(Note 6)	-15		V	1, 2, 3
I_Q	Quiescent Current	$V_{IN} = 10V$, $I_{OUT} = 5mA$		0.0	15	mA	1
				0.0	20	mA	2, 3
		$V_{IN} = 7V$, $I_{OUT} = 5mA$		0.0	15	mA	1
				0.0	20	mA	2, 3
		$V_{IN} = 26V$, $I_{OUT} = 5mA$		0.0	15	mA	1
				0.0	20	mA	2, 3
$V_{IN} = 10V$, $I_{OUT} = 1A$		0.0	50	mA	1		
		0.0	100	mA	2, 3		
V_{RLine}	Line Regulation	$7V \leq V_{IN} \leq 26V$, $I_{OUT} = 5mA$		-40	40	mV	1
				-50	50	mV	2, 3
V_{RLoad}	Load Regulation	$V_{IN} = 10V$, $50mA \leq I_{OUT} \leq 1A$		-50	50	mV	1
				-100	100	mV	2, 3
V_{DO}	Dropout Voltage	$I_{OUT} = 1A$		0.0	0.7	V	1
				0.0	1.0	V	2, 3
		$I_{OUT} = 100mA$		0.0	200	mV	1
				0.0	300	mV	2, 3
I_{SC}	Short Circuit Current	$V_{IN} = 10V$		1.5		A	1
				1.3		A	2, 3

AC Parameters SMD: 5962R8958701

The following conditions apply, unless otherwise specified.

AC: $V_I = 10V$, $I_O = 1A$, $C_O = 22\mu F$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
	Max Line Transient	$V_O \leq 6V$, $R_O = 100\Omega$, $t = 20mS$	(Note 6)	40		V	1, 2, 3
	Reverse Polarity Input Voltage Transient	$t = 20mS$, $R_O = 100\Omega$	(Note 6)	-45		V	1, 2, 3
RR	Ripple Rejection	$V_{IN} = 10V$, $1V_{RMS}$, $f = 1KHz$, $I_{OUT} = 5mA$	(Note 6)	60		dB	4
			(Note 6)	50		dB	5, 6
N_O	Output Noise Voltage	$V_{IN} = 10V$, $I_{OUT} = 5mA$, 10Hz - 100KHz	(Note 6)	0.0	700	μV_{RMS}	1, 2, 3
Z_O	Output Impedance	$V_{IN} = 10V$, $f_O = 120Hz$ $I_{OUT} = 100mA$ DC and 20mA AC	(Note 6)		1.0	Ω	1, 2, 3

LM2940-5.0 Electrical Characteristics SMD: 5962R8958702

DC Parameters

The following conditions apply, unless otherwise specified.

DC: $V_I = 10V$, $I_O = 1A$, $C_O = 22\mu F$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_O	Output Voltage	$V_{IN} = 10V$, $I_{OUT} = 5mA$		4.85	5.15	V	1
				4.75	5.25	V	2, 3
		$V_{IN} = 6V$, $I_{OUT} = 5mA$		4.85	5.15	V	1
				4.75	5.25	V	2, 3
		$V_{IN} = 7V$, $I_{OUT} = 5mA$		4.85	5.15	V	1
				4.75	5.25	V	2, 3
		$V_{IN} = 26V$, $I_{OUT} = 5mA$		4.85	5.15	V	1
				4.75	5.25	V	2, 3
		$V_{IN} = 10V$, $I_{OUT} = 1A$		4.85	5.15	V	1
				4.75	5.25	V	2, 3
$V_{IN} = 6V$, $I_{OUT} = 1A$		4.85	5.15	V	1		
		4.75	5.25	V	2, 3		
$V_{IN} = 6V$, $I_{OUT} = 50mA$		4.85	5.15	V	1		
		4.75	5.25	V	2, 3		
$V_{IN} = 10V$, $I_{OUT} = 50mA$		4.85	5.15	V	1		
		4.75	5.25	V	2, 3		
	Reverse Polarity Input Voltage DC	$R_O = 100\Omega$	(Note 6)	-15		V	1, 2, 3
I_Q	Quiescent Current	$V_{IN} = 10V$, $I_{OUT} = 5mA$		0.0	15	mA	1
				0.0	20	mA	2, 3
		$V_{IN} = 7V$, $I_{OUT} = 5mA$		0.0	15	mA	1
				0.0	20	mA	2, 3
		$V_{IN} = 26V$, $I_{OUT} = 5mA$		0.0	15	mA	1
				0.0	20	mA	2, 3
$V_{IN} = 10V$, $I_{OUT} = 1A$		0.0	50	mA	1		
		0.0	100	mA	2, 3		
V_{RLine}	Line Regulation	$7V \leq V_{IN} \leq 26V$, $I_{OUT} = 5mA$		-40	40	mV	1
				-50	50	mV	2, 3
V_{RLoad}	Load Regulation	$V_{IN} = 10V$, $50mA \leq I_{OUT} \leq 1A$		-50	50	mV	1
				-100	100	mV	2, 3
V_{DO}	Dropout Voltage	$I_{OUT} = 1A$		0.0	0.7	V	1
				0.0	1.0	V	2, 3
		$I_{OUT} = 100mA$		0.0	200	mV	1
				0.0	300	mV	2, 3
I_{SC}	Short Circuit Current	$V_{IN} = 10V$		1.5		A	1
				1.3		A	2, 3

AC Parameters SMD: 5962R8958702

The following conditions apply, unless otherwise specified.

AC: $V_I = 10V$, $I_O = 1A$, $C_O = 22\mu F$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
	Max Line Transient	$V_O \leq 6V$, $R_O = 100\Omega$, $t = 20mS$	(Note 6)	40		V	1, 2, 3
	Reverse Polarity Input Voltage Transient	$t = 20mS$, $R_O = 100\Omega$	(Note 6)	-45		V	1, 2, 3
RR	Ripple Rejection	$V_{IN} = 10V$, $1V_{RMS}$, $f = 1KHz$, $I_{OUT} = 5mA$	(Note 6)	60		dB	4
			(Note 6)	50		dB	5, 6
N_O	Output Noise Voltage	$V_{IN} = 10V$, $I_{OUT} = 5mA$, 10Hz - 100KHz	(Note 6)	0.0	700	μV_{RMS}	1, 2, 3
Z_O	Output Impedance	$V_{IN} = 10V$, $f_O = 120Hz$ $I_{OUT} = 100mA$ DC and 20mA AC	(Note 6)		1.0	Ω	1, 2, 3

DC Drift Parameters

The following conditions apply, unless otherwise specified.

DC: $V_I = 10V$, $I_O = 1A$, $C_O = 22\mu F$, "Delta calculations performed on QMLV devices at group B, subgroup 5 only"

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_O	Output Voltage	$V_{IN} = 10V$, $I_{OUT} = 5mA$		-30	30	mV	1
		$V_{IN} = 6V$, $I_{OUT} = 5mA$		-30	30	mV	1
		$V_{IN} = 7V$, $I_{OUT} = 5mA$		-30	30	mV	1
		$V_{IN} = 26V$, $I_{OUT} = 5mA$		-30	30	mV	1
		$V_{IN} = 10V$, $I_{OUT} = 1A$		-30	30	mV	1
		$V_{IN} = 6V$, $I_{OUT} = 1A$		-30	30	mV	1
		$V_{IN} = 6V$, $I_{OUT} = 50mA$		-30	30	mV	1
		$V_{IN} = 10V$, $I_{OUT} = 50mA$		-30	30	mV	1
V_{RLOAD}	Load Regulation	$V_{IN} = 10V$, $50mA \leq I_{OUT} \leq 1A$		-20	20	mV	1

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A) / \theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. With heat sinking, the maximum power is 5 Watts, but then this will depend upon the temperature of the heat sink, the efficiency of the heat sink, and the efficiency of the heat flow between the package body and the heat sink. We can not predict these values.

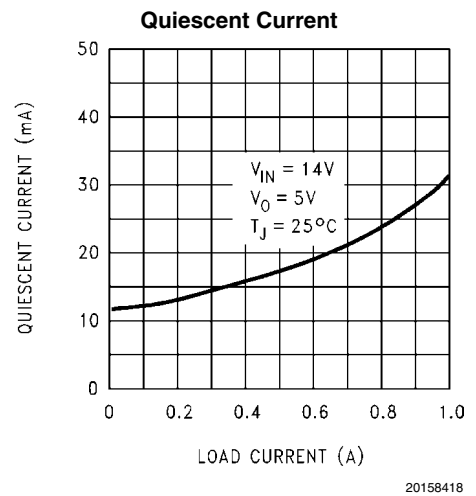
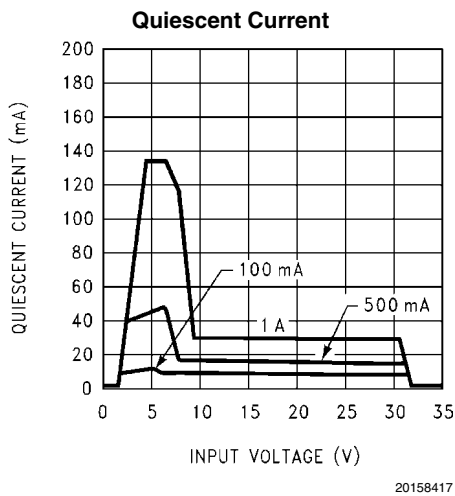
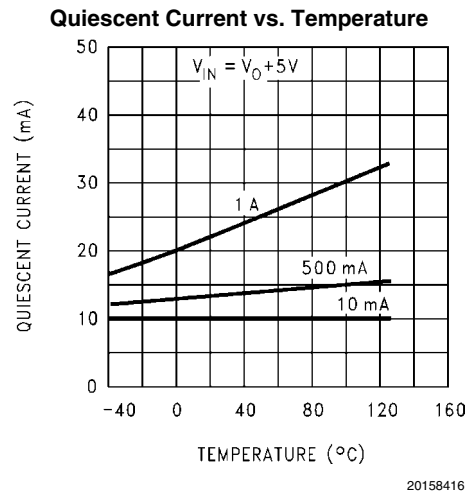
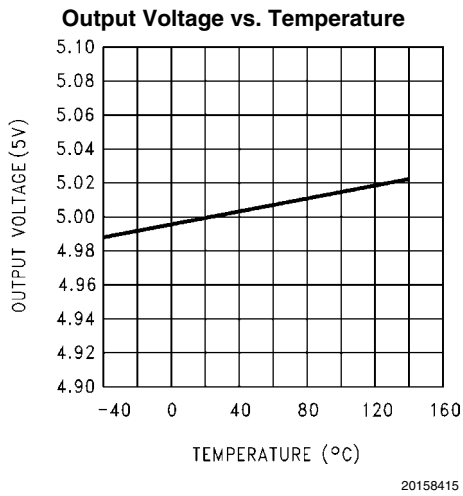
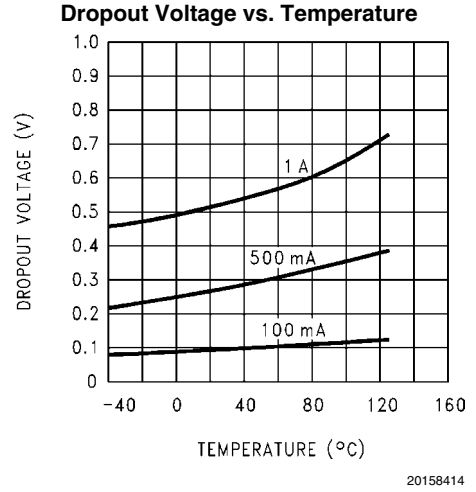
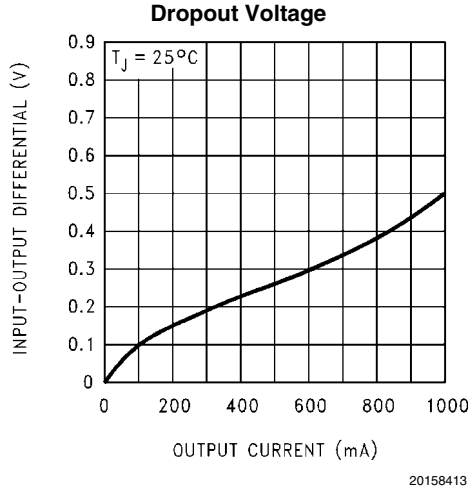
Note 4: The package material for these devices allows much improved heat transfer over our standard ceramic packages. In order to take full advantage of this improved heat transfer, heat sinking must be provided between the package base (directly beneath the die), and either metal traces on, or thermal vias through, the printed circuit board. Without this additional heat sinking, device power dissipation must be calculated using θ_{JA} , rather than θ_{JC} , thermal resistance. It must not be assumed that the device leads will provide substantial heat transfer out of the package, since the thermal resistance of the lead frame material is very poor, relative to the material of the package base. The stated θ_{JC} thermal resistance is for the package material only, and does not account for the additional thermal resistance between the package base and the printed circuit board. The user must determine the value of the additional thermal resistance and must combine this with the stated value for the package, to calculate the total allowed power dissipation for the device.

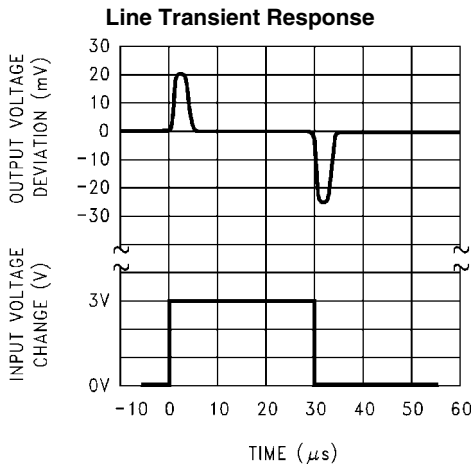
Note 5: Human body model, 1.5 k Ω in series with 100 pF.

Note 6: Functional test only.

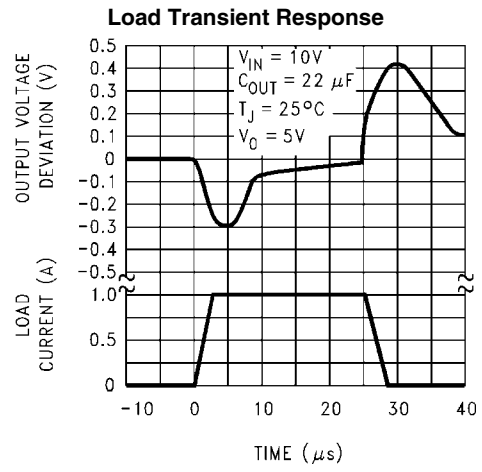
Note 7: These parts are tested on a wafer by wafer basis at high and low dose rates according to MIL-STD-883 Test Method 1019 Conditions A and D with no enhanced low dose rate sensitivity (ELDRS). Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics.

Typical Performance Characteristics

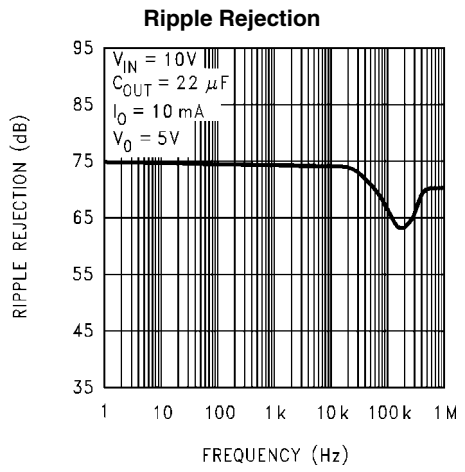




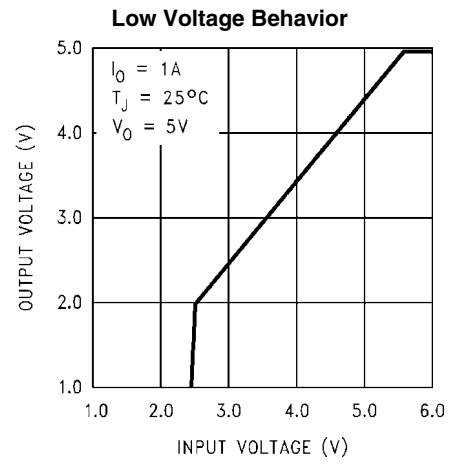
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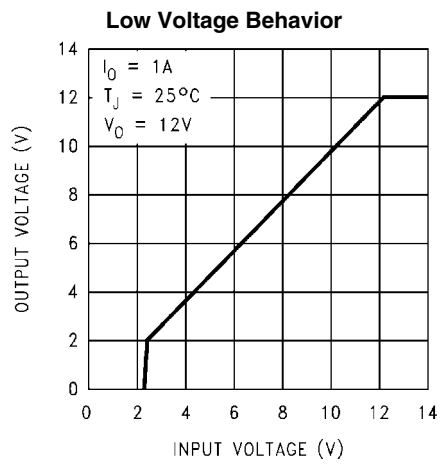
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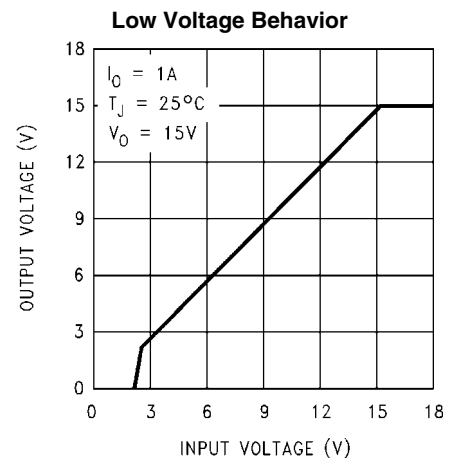
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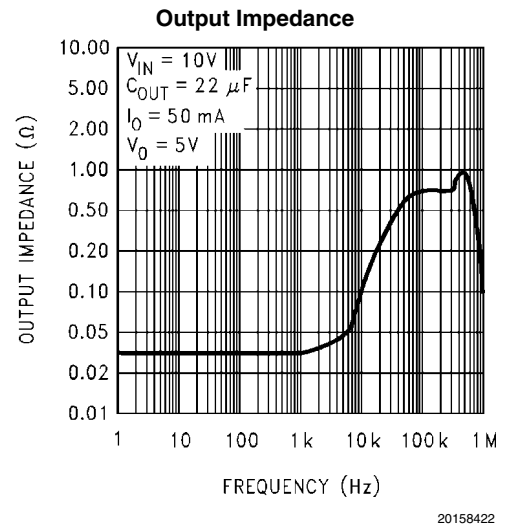
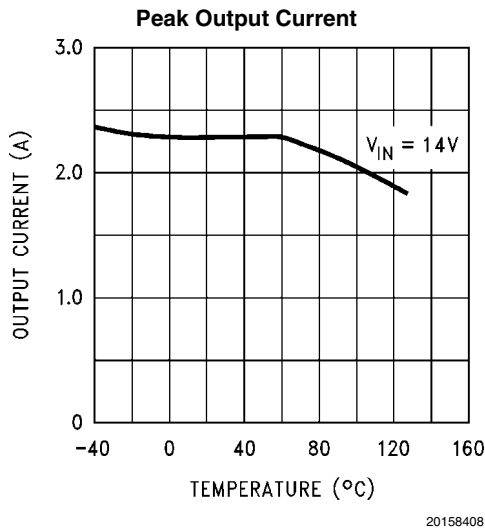
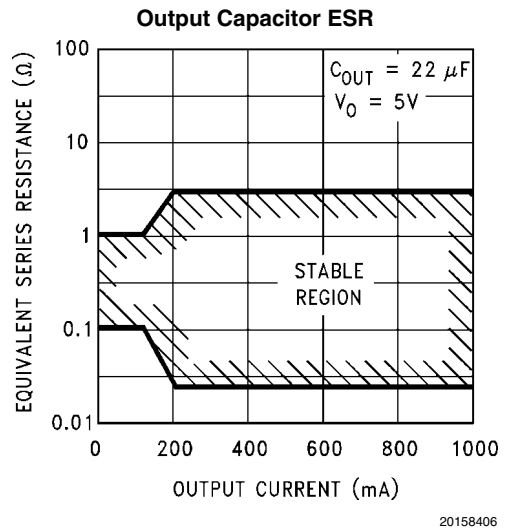
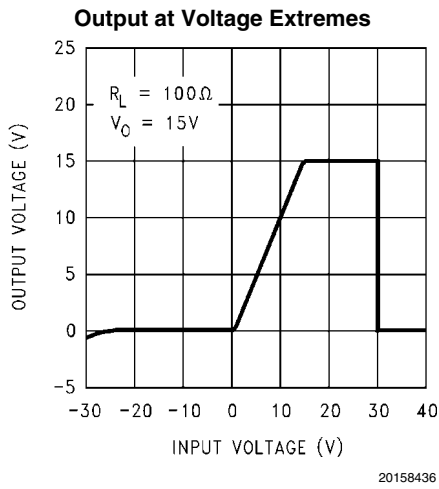
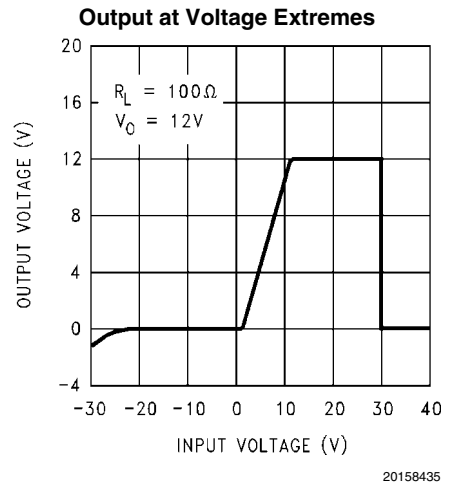
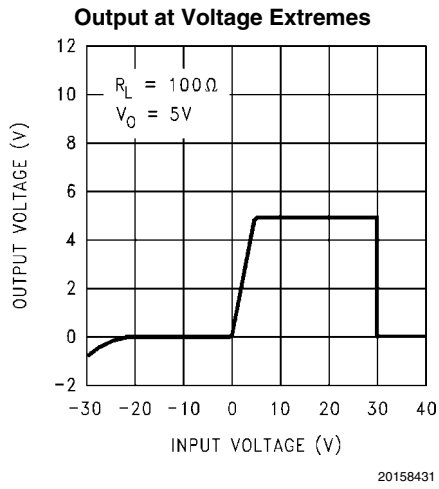
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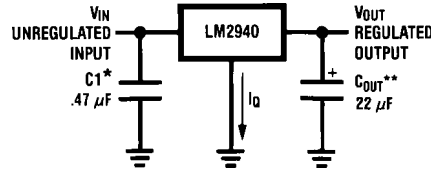
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Typical Application



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*Required if regulator is located far from power supply filter.

**C_{OUT} must be at least 22 µF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator and the ESR is critical; see curve.

Application Hints

EXTERNAL CAPACITORS

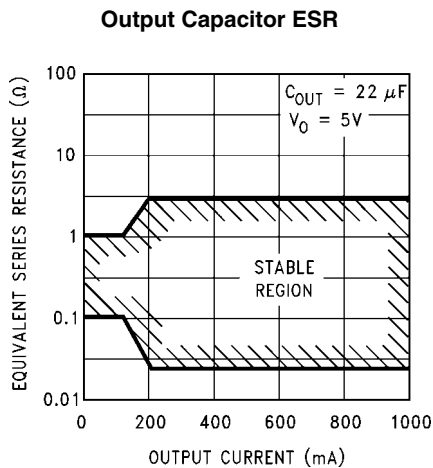
The output capacitor is critical to maintaining regulator stability, and must meet the required conditions for both ESR (Equivalent Series Resistance) and minimum amount of capacitance.

MINIMUM CAPACITANCE:

The minimum output capacitance required to maintain stability is 22 µF (this value may be increased without limit). Larger values of output capacitance will give improved transient response.

ESR LIMITS:

The ESR of the output capacitor will cause loop instability if it is too high or too low. The acceptable range of ESR plotted versus load current is shown in the graph below. **It is essential that the output capacitor meet these requirements, or oscillations can result.**



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FIGURE 1. ESR Limits

It is important to note that for most capacitors, ESR is specified only at room temperature. However, the designer must ensure that the ESR will stay inside the limits shown over the entire operating temperature range for the design.

For aluminum electrolytic capacitors, ESR will increase by about 30X as the temperature is reduced from 25°C to -40°C. This type of capacitor is not well-suited for low temperature operation.

Solid tantalum capacitors have a more stable ESR over temperature, but are more expensive than aluminum electrolytic.

ics. A cost-effective approach sometimes used is to parallel an aluminum electrolytic with a solid Tantalum, with the total capacitance split about 75/25% with the Aluminum being the larger value.

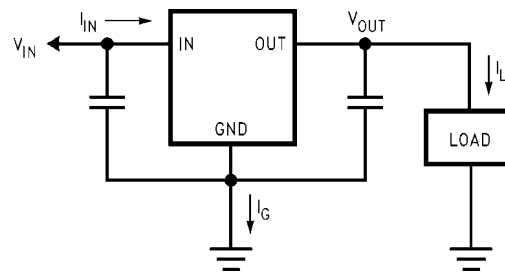
If two capacitors are paralleled, the effective ESR is the parallel of the two individual values. The “flatter” ESR of the Tantalum will keep the effective ESR from rising as quickly at low temperatures.

HEATSINKING

A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under Absolute Maximum Ratings.

To determine if a heatsink is required, the power dissipated by the regulator, P_D, must be calculated.

The figure below shows the voltages and currents which are present in the circuit, as well as the formula for calculating the power dissipated in the regulator:



20158437

$$I_{IN} = I_L + I_G$$

$$P_D = (V_{IN} - V_{OUT}) I_L + (V_{IN}) I_G$$

FIGURE 2. Power Dissipation Diagram

The next parameter which must be calculated is the maximum allowable temperature rise, T_R (max). This is calculated by using the formula:

$$T_R (\text{max}) = T_J (\text{max}) - T_A (\text{max})$$

where: T_J (max) is the maximum allowable junction temperature.

T_A (max) is the maximum ambient temperature which will be encountered in the application.

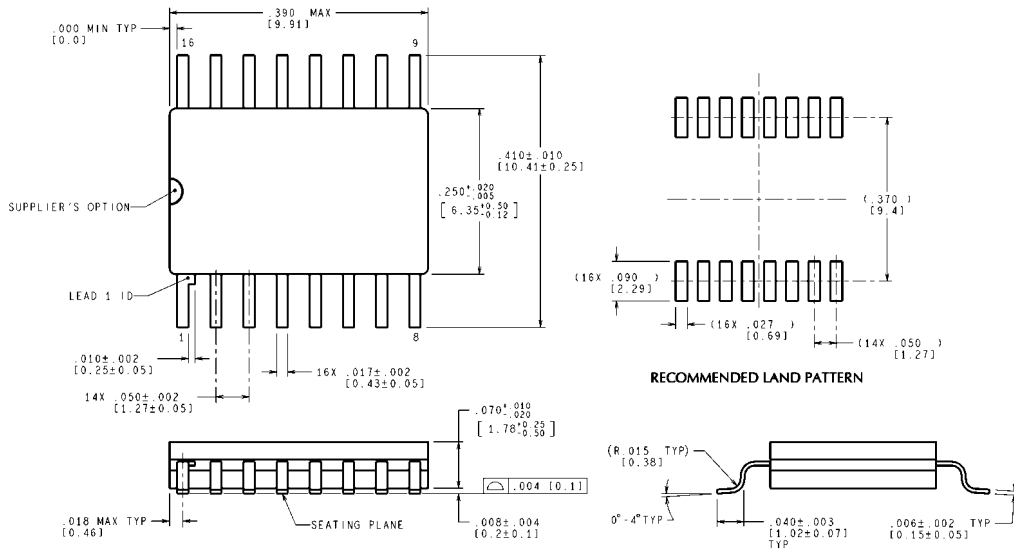
Using the calculated values for T_R(max) and P_D, the maximum allowable value for the junction-to-ambient thermal resistance, θ_(JA), can now be found:

$$\theta_{(JA)} = T_R (\text{max})/P_D$$

Revision History

Released	Revision	Section	Changes
05/10/2010	A	New Release, Corporate format	1 MDS data sheets converted into one Corp. data sheet format added reference to New ELDRS device. Change AC subgroups from 4, 5, 6, 7, 8A, 8B to 1, 2, 3 for parameters Max Line Transient, Reverse Polarity Input Voltage Transient, Output Noise Voltage, Output Impedance. To bring it into agreement with the SMD. MNL2940-5.0-X Rev 1A1 will be archived.
12-Oct-2010	B	Ordering Information, Absolute Max Ratings	Ordering Information — Added LM2940GW5.0/883, LM2940GW5.0RLQV. Absolute Max Ratings — Added Theta JA and Theta JC along with Package Weight for 'GW' devices. LM2940QML Rev A will be archived.

Physical Dimensions inches (millimeters) unless otherwise noted



MIL-PRF-38535
CONFIGURATION CONTROL

CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY

WG16A (Rev E)

16 Lead Surface Mount Package (WG)
See NS Package Number WG16A

Notes

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