SUCCESS BY DESIGN

SP37E760
PRELIMINARY

3.3V I/O Controller for Embedded Applications

FEATURES

- 3.3 Volt Operation
- Intelligent Auto Power Management
- 16 Bit Address Qualification (Optional)
- Serial Ports
  - Two High Speed NS16C550 Compatible UARTs with Send/Receive 16 Byte FIFOs
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
- ISA Host Interface
- General Purpose Address Decoder
  - 16-Byte Block Decode
- Multi-Mode Parallel Port with ChiProtect
  - Standard Mode
  - IBM PC/XT, PC/AT, and PS/2 Compatible

  Bi-directional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible
  - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - Enhanced Capabilities Port (ECP) Compatible (IEEE 1284 Compliant)
  - Incorporates ChiProtect Circuitry for Protection Against Damage Due to Printer Power-On
  - 192 Base I/O Address, 7 IRQ and 3 DMA Options
- 100 Pin QFP and TQFP Packages

GENERAL DESCRIPTION

The SMSC SP37E760 is a 3.3v PC 97-compliant I/O Controller. The SP37E760 utilizes SMSC's proven SuperCell technology and is optimized for embedded applications. The SP37E760 incorporates a 16-byte data FIFO, two 16C550 compatible UARTs and one Multi-Mode parallel port with ChiProtect circuitry plus EPP and ECP support. Both on-chip UARTs are compatible with the NS16C550.

The parallel port is compatible with IBM PC/AT architectures. The parallel port ChiProtect circuitry prevents damage caused by an attached powered printer when the SP37E760 is not powered.

The SP37E760 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes. The SP37E760 also features Software Configurable Logic (SCL) for ease of use. SCL allows programmable system configuration of key functions such as the parallel port, and UARTs.

ORDERING INFORMATION

Order Numbers:

SP37E760-MC for 100 Pin QFP Package

SP37E760-MD for 100 Pin TQFP Package

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Hauppauge, NY 11788
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1 PIN CONFIGURATIONS

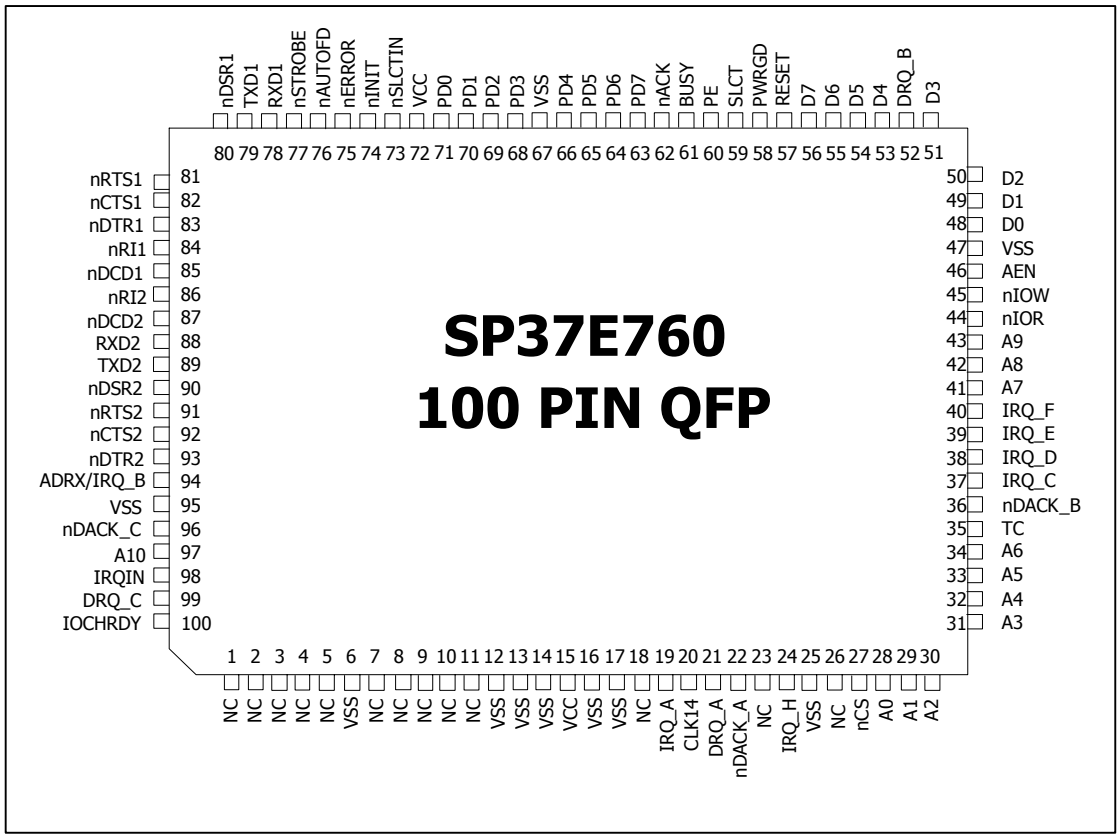


FIGURE 1 - SP37E760 QFP PIN CONFIGURATION

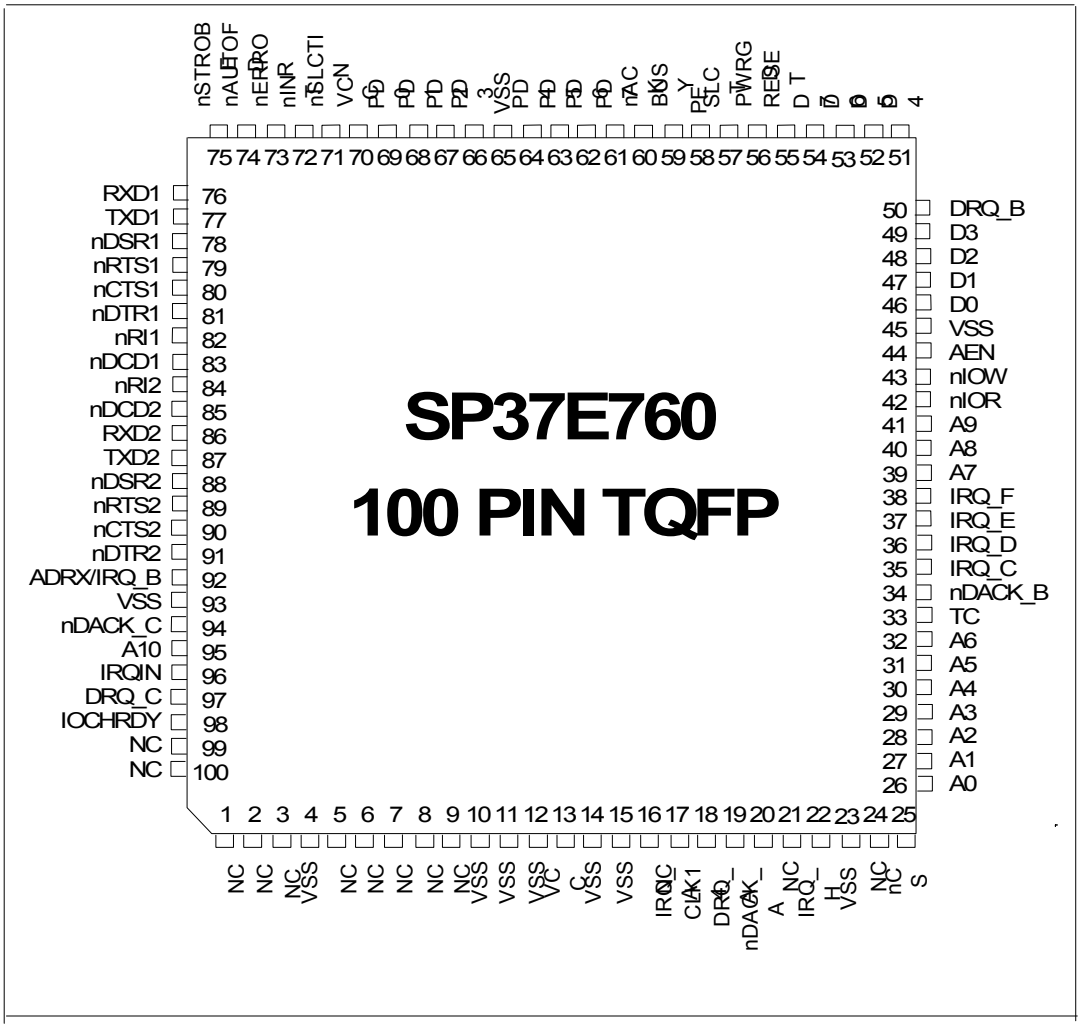


FIGURE 2 - SP37E760 TQFP PIN CONFIGURATION

2 PIN DESCRIPTION

2.1 Buffer Type Per Pin

Table 1 - DESCRIPTION OF PIN FUNCTIONS

PIN #		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
TQFP	QFP				
HOST PROCESSOR INTERFACE					
46-49 51-54	48-51 53-56	Data Bus 0-7	D0-D7	IO12	The data bus connection used by the host microprocessor to transmit data to and from the chip. These pins are in a high-impedance state when not in the output mode.
42	44	nI/O Read	nIOR	IS	This active low signal is issued by the host microprocessor to indicate an I/O read operation.
43	45	nI/O Write	nIOW	IS	This active low signal is issued by the host microprocessor to indicate an I/O write operation.
44	46	Address Enable	AEN	IS	Active high Address Enable indicates DMA operations on the host data bus. Used internally to qualify appropriate address decodes.
26-32 39-41, 95	28-34 41-43, 97	Address Bus	A0-A10	I	These host address bits determine the I/O address to be accessed during nIOR and nIOW cycles. These bits are latched internally by the leading edge of nIOR and nIOW. All internal address decodes use the full A0 to A10 address bits.
19,50, 97	21,52, 99	DMA Request A, B, C	DRQ_A DRQ_B DRQ_C	O12	These active high outputs are the DMA request for byte transfers of data between the host and the chip. These signals are cleared on the last byte of the data transfer by the nDACK signal going low (or by nIOR going low if nDACK was already low as in demand mode).
20,34, 94	22,36, 96	nDMA Acknowl-edge A, B, C	nDACK_A nDACK_B nDACK_C	IS	These are active low inputs acknowledging the request for a DMA transfer of data between the host and the chip. These inputs enable the DMA read or write internally.
33	35	Terminal Count	TC	IS	This signal indicates that DMA data transfer is complete. TC is only accepted when nDACK_x is low. In AT and PS/2 model 30 modes, TC is active high and in PS/2 mode, TC is active low.
17, 35-38, 22	19, 37-40, 24	Interrupt Request A, C, D, E, F, and H	IRQ_A IRQ_C IRQ_D IRQ_E IRQ_F IRQ_H	O12/OD12	Interrupt requests from a logical device or IRQIN are output on one of the IRQA-H signals. Refer to the configuration registers section for additional information. If EPP or ECP Mode is enabled this output is pulsed low and released to allow sharing of interrupts.
25	27	Chip Select Input	nCS	I	This active low input serves as an external decoder for address lines above A10.
55	57	Reset	RESET	IS	This active high signal resets the chip and must be valid for 500ns minimum. The effect on the internal registers is described in the appropriate section. The configuration registers are not affected by this reset.
98	100	I/O Channel Ready (Note[3])	IOCHRDY	OD12	This pin is pulled low to extend the read/write command. IOCHRDY can be used by the Parallel Port in EPP mode.
SERIAL PORTS INTERFACE					
86	88	Receive Data 2	RXD2	IS	Receiver serial data input for port 2.

PIN #		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
TQFP	QFP				
87	89	Transmit Data 2 (Note[4])	TXD2	O12PD	Transmit serial data output for port 2.
76	78	Receive Data 1	RXD1	I	Receiver serial data input for port 1.
77	79	Transmit Data 1	TXD1	O12	Transmit serial data output for port 1.
79,89	81,91	nRequest to Send (System Option)	nRTS1 nRTS2 (SYSOPT)	O6	Active low Request to Send outputs for the Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of the Modem Control Register (MCR). The hardware reset will reset the nRTS signal to inactive mode (high). nRTS is forced inactive during loop mode operation. At the trailing edge of hardware reset the nRTS2 inputs is latched to determine the configuration base address: 0 = INDEX Base I/O Address 3F0 Hex; 1 = INDEX Base I/O Address 370 Hex.
81,91	83,93	nData Terminal Ready	nDTR1 nDTR2	O6	Active low Data Terminal Ready outputs for the serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the nDTR signal to inactive mode (high). nDTR is forced inactive during loop mode operation.
80,90	82,92	nClear to Send	nCTS1 nCTS2	I	Active low Clear to Send inputs for the serial port. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of nCTS signal by reading bit 4 of Modem Status Register (MSR). A nCTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when nCTS changes state. The nCTS signal has no effect on the transmitter. Note: Bit 4 of MSR is the complement of nCTS.
78,88	80,90	nData Set Ready	nDSR1 nDSR2	I	Active low Data Set Ready inputs for the serial port. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of nDSR signal by reading bit 5 of Modem Status Register (MSR). A nDSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nDSR changes state. Note: Bit 5 of MSR is the complement of nDSR.
83,85	85,87	nData Carrier Detect	nDCD1 nDCD2	I	Active low Data Carrier Detect inputs for the serial port. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of nDCD signal by reading bit 7 of Modem Status Register (MSR). A nDCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nDCD changes state. Note: Bit 7 of MSR is the complement of nDCD.

PIN #		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
TQFP	QFP				
82,84	84,86	nRing Indicator	nRI1 nRI2	I (Note[1])	Active low Ring Indicator inputs for the serial port. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of nRI signal by reading bit 6 of Modem Status Register (MSR). A nRI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nRI changes state. Note: Bit 6 of MSR is the complement of nRI.
PARALLEL PORT INTERFACE (NOTE 2)					
71	73	nPrinter Select Input (Note[2])	nSLCTIN	(OD14/OP14)/OD12	This active low output selects the printer. This is the complement of bit 3 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
72	74	nInitiate Output (Note[2])	nINIT	(OD14/OP14)/OD12	This output is bit 2 of the printer control register. This is used to initiate the printer when low. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
74	76	nAutofeed Output (Note[2])	nAUTOFD	(OD14/OP14)/OD12	This output goes low to cause the printer to automatically feed one line after each line is printed. The nAUTOFD output is the complement of bit 1 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
75	77	nStrobe Output (Note[2])	nSTROBE	(OD14/OP14)/OD12	An active low pulse on this output is used to strobe the printer data into the printer. The nSTROBE output is the complement of bit 0 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
59	61	Busy	BUSY	I/OD12	This is a status output from the printer, a high indicating that the printer is not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
60	62	nAcknowl-edge	nACK	I/OD12	A low active output from the printer indicating that it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the nACK input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
58	60	Paper End	PE	I/OD12	Another status output from the printer, a high indicating that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.

PIN #		NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
TQFP	QFP				
57	59	Printer Selected Status	SLCT	I/OD12	This high active output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
73	75	nError	nERROR	I/OD12	A low on this input from the printer indicates that there is a error condition at the printer. Bit 3 of the Printer Status register reads the nERR input. Refer to Parallel Port description for use of this pin in ECP and EPP mode.
69-66, 64	71-68, 66	Port Data 0-Port Data 4	PD0-4	IOP14/IS	Port Data 0-4
63	65	Port Data 5	PD5	IOP14	Port Data 5
62	64	Port Data 6	PD6	IOP14/ OD12	Port Data 6
61	63	Port Data 7	PD7	IOP14	Port Data 7
MISC					
18	20	14.318 MHz Input Clock	CLK14	ICLK	The external connection to a single source 14.318 MHz clock.
92	94	Address X/ Interrupt Request B	nADRX IRQ_B	O12/ OD12	Active low address decode out: used to decode a 1, 8, or 16 byte address block. (An external pull-up is required). Refer to Configuration registers CR03, CR08 and CR09 for more information. The interrupt request from a logical device or IRQIN may be output on IRQ_B. Refer to the configuration registers for more information. If EPP or ECP Mode is enabled, this output is pulsed low and released to allow sharing of interrupts.
56	58	Power Good	PWRGD	I/O4	This active high input indicates that the power (VCC) is valid. For device operation PWRGD must be active. When PWRGD is inactive, all inputs are disconnected and put into a low power mode; all outputs are put into high impedance. The contents af all registers are preserved as long as VCC is valid. The output driver current drain when PWRGD is inactive mode drops to I_{STBY} - standby current.
96	98	External Interrupt Input	IRQIN	IS	This pin is used to steer an interrupt signal from an external device onto one of eight IRQ outputs IRQA-H.
POWER INTERFACE					
13,70	15,72	Power	VCC		Positive Supply Voltage.
4, 10, 11, 12, 14, 15, 23, 45, 65, 93	6, 12, 13, 14, 16, 17, 25, 47, 67, 95	Ground	VSS		Ground Supply.
1, 2, 3, 5, 6, 7, 8, 9, 16, 21, 24, 99, 100	1, 2, 3, 4, 5, 7, 8, 9, 10, 11, 18, 23, 26,	Non Connect	NC		Non-Connected Pins

Note 1: nRI and the UART interrupts are active when PWRGD is active and the UARTS are either fully powered or in AUTOPOWER DOWN mode.
Note 2: Active (push-pull) output drivers are required on these pins in the enhanced parallel port modes.
Note 3: An external pull-up must be provided for IOCHRDY.
Note 4: The pull-down on this pin is always active including when the output driver is tristated and regardless of the state of PWRGD.

2.2 Buffer Type Summary

Table 2 below describes the buffer types shown in Table 1. All values are specified at V_{cc} = +3.3v, ±10%

Table 2 - SP37E760 3.3V Buffer Type Summary

BUFFER TYPE	DESCRIPTION
IO12	Input/Output. 12mA sink; 6mA source
O12	Output. 12mA sink; 6mA source
O12PD	Output. 12mA sink; 6mA source with 30µa pull-down
OD12	Open Drain. 12mA sink
O6	Output. 6mA sink; 3mA source
OD14	Open Drain. 14mA sink
OP14	Output. 14mA sink; 14mA source. Backdrive Protected
IOP14	Input/Output. 14mA sink; 14mA source. Backdrive Protected
O4	Output. 4mA sink; 2mA source
ICLK	Input to Crystal Oscillator Circuit (TTL levels)
I	Input TTL Compatible
IS	Input with Schmitt Trigger

2.3 Output Drivers

Active output drivers in the SP37E760 will always achieve the minimum specified DC Electrical Characteristics shown in Table 54. Note: If there is a pull-up on an external node driven by an active output driver the SP37E760 will sink current from the pull-up through the low impedance source.

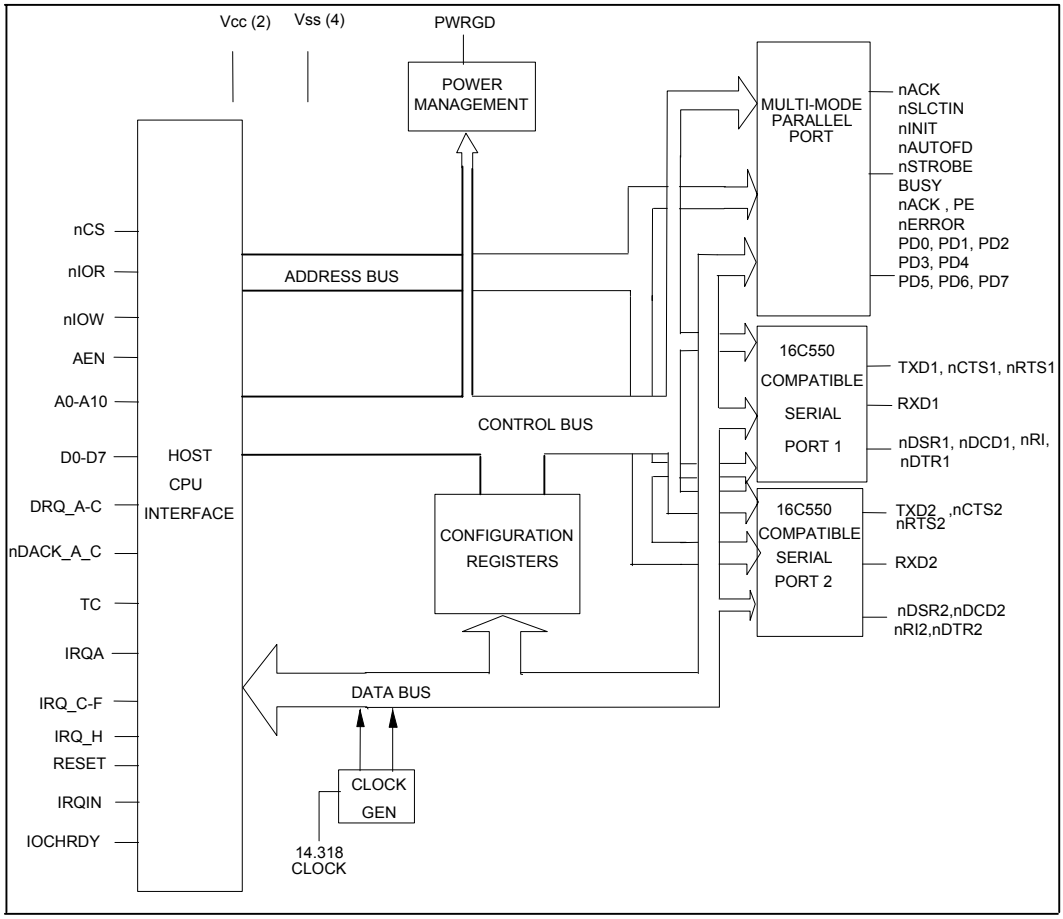


FIGURE 3 - SP37E760 BLOCK DIAGRAM

3 FUNCTIONAL DESCRIPTION

Super I/O Registers

Table 3 shows the addresses of the various device blocks of the Super I/O immediately after power up. The base addresses must be set in the configuration registers before accessing these devices. The base addresses of the Serial and Parallel Ports can be moved via the configuration registers.

3.1 Host Processor Interface

The host processor communicates with the SP37E760 using the Super I/O registers. Register access is accomplished through programmed I/O or DMA transfers. All registers are 8 bits wide. All host interface output buffers are capable of sinking a minimum of 12 mA.

Table 3 - SP37E760 Block Addresses

ADDRESS	BLOCK NAME	NOTES
3F0, 3F1 or 370, 371	Configuration	Write only; Note 1
Base +[0:7]	Serial Port Com 1	Disabled at power up; Note 2
Base1 +[0:7] Base2 +[0:7]	Serial Port Com 2	Disabled at power up; Note 2
Base +[0:3] all modes Base +[4:7] for EPP Base +[400:403] for ECP	Parallel Port	Disabled at power up; Note 2

Note 1: Configuration registers can only be modified in the configuration state, refer to section CONFIGURATION on page 45 for more information. All logical blocks in the SP37E760 can operate normally in the Configuration State.

Note 2: The base addresses must be set in the configuration registers before accessing the logical device blocks.

4 SERIAL PORT (UART)

The SP37E760 incorporates two full function UARTs. They are compatible with the NS16450, the 16450 ACE registers and the NS16550A. The UARTs perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 115.2K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTs each contain a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. The UARTs are also capable of supporting the MIDI data rate. Refer to the SP37E760 Configuration Registers for information on disabling, powering down and changing the base address of the UARTs. The interrupt from a UART is enabled by programming OUT2 of that UART to a logic "1". When OUT2 is a logic "0" the UART Interrupt is disabled.

4.1 Register Description

Addressing of the accessible registers of the Serial Port is shown below (Table 4). The base addresses of the serial ports are defined by the configuration registers (see section CONFIGURATION on page 45). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The SP37E760 contains two serial ports, each of which contain a register set as described below.

Table 4 - Addressing the Serial Port

DLAB[1]	A2	A1	A0	REGISTER NAME
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write)

Note[1]: DLAB is Bit 7 of the Line Control Register

4.1.1 RECEIVE BUFFER REGISTER (RB)

The Receive Buffer register (Address Offset = 0H, DLAB = 0, READ ONLY) holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit character which is transferred to the Receive Buffer register. The shift register is not accessible.

4.1.2 TRANSMIT BUFFER REGISTER (TB)

The Transmit Buffer register (Address Offset = 0H, DLAB = 0, WRITE ONLY) contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data character to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

4.1.3 INTERRUPT ENABLE REGISTER (IER)

The lower four bits of the Interrupt Enable register (Address Offset = 1H, DLAB = 0, READ/WRITE) control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, by setting the appropriate bits of this register to a high selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the SP37E760. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

4.1.3.1 ERDAI, Bit 0

The ERDAI bit enables the Received Data Available Interrupt (and time-out interrupts in the FIFO mode) when set to logic “1”.

4.1.3.2 ETHREI, Bit 1

The ETHREI bit enables the Transmitter Holding Register Empty Interrupt when set to logic “1”.

4.1.3.3 ELSI, Bit 2

The ELSI bit enables the Received Line Status Interrupt when set to logic “1”. The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

4.1.3.4 EMSI, Bit 3

The EMSI bit enables the MODEM Status Interrupt when set to logic “1”. An MSI is caused when one of the Modem Status Register bits changes state.

4.1.3.5 Reserved, Bits 4 - 7

Bits 4 to 7 are *RESERVED*. Reserved bits cannot be written and return 0 when read.

4.1.4 INTERRUPT IDENTIFICATION REGISTER (IIR)

By accessing the Interrupt Identification register (Address Offset = 2H, DLAB = X, READ), the host CPU can determine the highest priority interrupt and its source. Four levels of interrupt priority exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to the Interrupt Control Table, Table 5). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed.

4.1.4.1 Interrupt Pending, Bit 0

The Interrupt Pending bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic “0”, an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic “1”, no interrupt is pending.

4.1.4.2 Interrupt ID, Bits 1 - 2

The Interrupt ID bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table (Table 5).

4.1.4.3 Time-Out, Bit 3

In non-FIFO mode, the Time-Out bit is a logic “0”. In FIFO mode the Time-Out bit is set along with bit 2 when a time-out interrupt is pending.

4.1.4.4 Reserved, Bits 4 - 5

Bits 4 to 5 are *RESERVED*. Reserved bits cannot be written and return 0 when read.

4.1.4.5 FIFOs Enabled, Bits 6 - 7

The FIFOs Enabled bits are set when the FIFO CONTROL Register bit 0 equals 1.

Table 5 - Interrupt Control

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1	1	0	0	Second	Character Time-out Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Character times and there is at least 1 character in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

4.1.5 FIFO CONTROL REGISTER (FCR)

The FIFO Control register (Address Offset = 2H, DLAB = X, WRITE) appears at the same location as the IIR. This register is used to enable and clear the FIFOs and set the RCVR FIFO trigger level. Note: DMA is not supported.

4.1.5.1 FIFO Enable, Bit 0

Setting the FIFO Enable bit to a logic “1” enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic “0” disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

4.1.5.2 RCVR FIFO Reset, Bit 1

Setting the RCVR FIFO Reset bit to a logic “1” clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

4.1.5.3 XMIT FIFO Reset, Bit 2

Setting the XMIT FIFO Reset bit to a logic “1” clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

4.1.5.4 DMA Mode Select, Bit 3

Writing to the DMA Mode Select bit has no effect on the operation of the UART. The RXRDY and TXRDY pins are not available on this chip.

4.1.5.5 Reserved, Bits 4 - 5

Bits 4 to 5 are *RESERVED*. Reserved bits cannot be written and return 0 when read.

4.1.5.6 RCVR Trigger, Bits 6 - 7

The RCVR Trigger bits are used to set the trigger level for the RCVR FIFO interrupt (Table 6).

Table 6 - RCVR Trigger Encoding

RCVR TRIGGER		RCVR FIFO Trigger Level (BYTES)
Bit 7	**Bit 6**	
0	**0**	**1**
0	**1**	**4**
1	**0**	**8**
1	**1**	**14**

4.1.6 LINE CONTROL REGISTER (LCR)

The Line Control register (Address Offset = 3H, DLAB = 0, READ/WRITE) contains the formatting information for the serial line.

4.1.6.1 Word Length Select, Bits 0 - 1

The Word Length Select bits specify the number of bits in each transmitted or received serial character. Note: the *Start*, *Stop* and *Parity* bits are not included in the word length. The encoding of the Word Length bits is shown in Table 7.

Table 7 - Word Length Encoding

WORD LENGTH SELECT		WORD LENGTH (Bits)
Bit 1	**Bit 0**	
0	0	5
0	1	6
1	0	7
1	1	8

4.1.6.2 Stop Bits, Bit 2

The Stop Bits bit specifies the number of stop bits in each transmitted or received serial character. Table 8 describes the Stop Bits encoding.

Table 8 - STOP Bit Encoding

STOP BITS (Bit 2)	WORD LENGTH	NUMBER OF STOP BITS
0	-	1
0	5 Bits	1.5
1	6 Bits	2
1	7 Bits	2
1	8 Bits	2

Note: The receiver ignores stop bits beyond the first, regardless of the number of stop bits used in transmitting.

4.1.6.3 Parity Enable, Bit 3

When the Parity Enable bit is a logic “1” a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed.

4.1.6.4 Even Parity Select, Bit 4

When the Even Parity Select (EPS) bit is a logic “0” and the Parity Enable is a logic “1”, an odd number of logic “1”’s is transmitted or checked in the data word and the parity bit. When the Parity Enable is a logic “1” and the EPS bit is a logic “1” an even number of bits is transmitted and checked.

4.1.6.5 Stick Parity, Bit 5

When the Stick Parity bit is a logic “1” and the Parity Enable is a logic “1”, the parity bit is transmitted and then detected by the receiver in the opposite state indicated by the EPS bit.

4.1.6.6 Set Break, Bit 6

When the Set Break Control bit is a logic “1”, the transmit data output (TXD) is forced to the Spacing or logic “0” state and remains there until reset by a low level bit 6, regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

4.1.6.7 DLAB, Bit 7

The Divisor Latch Access Bit must be set high (logic “1”) to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic “0”) to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

4.1.7 MODEM CONTROL REGISTER (MCR)

The Modem Control register (Address Offset = 4H, DLAB = X, READ/WRITE) manages the interface for the MODEM, data set, or device emulating a MODEM.

4.1.7.1 Data Terminal Ready, Bit 0

The Data Terminal Ready bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic “1”, the nDTR output is forced to a logic “0”. When bit 0 is a logic “0”, the nDTR output is forced to a logic “1”.

Request To Send, Bit 1

The Request To Send bit controls the Request To Send (nRTS) output. . When bit 1 is set to a logic “1”, the nRTS output is forced to a logic “0”. When bit 1 is a logic “0”, the nRTS output is forced to a logic “1”.

4.1.7.2 OUT1, Bit 2

The OUT1 bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

4.1.7.3 OUT2, Bit 3

The OUT2 bit is used to enable the UART interrupt. When OUT2 is a logic “0”, the serial port interrupt output is forced to a high impedance state; i.e, disabled. When OUT2 is a logic “1”, the serial port interrupt outputs are enabled.

4.1.7.4 Loop, Bit 4

The Loop bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic “1”, the following occurs:

1. The TXD is set to the Marking State (logic “1”).
2. The receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is “looped back” into the Receiver Shift Register input.
4. All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.
5. The four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (nDSR, nCTS, RI and DCD) respectively.
6. The Modem Control output pins are forced inactive.
7. Data that is transmitted is immediately received.

The Loopback feature allows the processor to verify the transmit and receive data paths of the Serial Port. The receiver and the transmitter interrupts are fully operational in loopback mode. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs.

The interrupts are still controlled by the Interrupt Enable Register.

4.1.7.5 Reserved, Bits 5 - 7

Bits 5 to 7 are *RESERVED*. Reserved bits cannot be written and return 0 when read.

4.1.8 LINE STATUS REGISTER (LSR)

Address Offset = 5H, DLAB = X, READ/WRITE

4.1.8.1 Data Ready, Bit 0

Data Ready (DR) is set to a logic "1" whenever a complete received data character has been transferred into the Receiver Buffer Register or the FIFO. DR is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

4.1.8.2 Overrun Error, Bit 1

The Overrun Error (OE) bit indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrun error will occur only when the FIFO is full and the next character has been completely received in the shift register: the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition and reset whenever the Line Status Register is read.

4.1.8.3 Parity Error, Bit 2

The Parity Error (PE) bit indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

4.1.8.4 Framing Error, Bit 3

The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

4.1.8.5 Break Interrupt, Bit 4

The Break Interrupt (BI) bit is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received requires the serial data (RXD) to be logic "1" for at least ½ bit time.

Note: LSR Bits 1 through 4 produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

4.1.8.6 Transmitter Holding Register Empty, Bit 5

The Transmitter Holding Register Empty (THRE) bit indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is read-only.

4.1.8.7 Transmitter Empty, Bit 6

The Transmitter Empty (TEMT) bit is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is read-only. In the FIFO mode this bit is set whenever the THR and TSR are both empty.

4.1.8.8 RCVR FIFO Error, Bit 7

The RCVR FIFO Error bit is permanently set to logic "0" in the 450 mode. In the FIFO mode this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

4.1.9 MODEM STATUS REGISTER (MSR)

The Modem Status register (Address Offset = 6H, DLAB = X, READ/WRITE) provides the current state of the control lines from the MODEM or peripheral device. In addition to this current state information, four bits of the MODEM Status Register provide state change information. These four bits are set to logic "1" whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

4.1.9.1 Delta Clear To Send, Bit 0

The Delta Clear To Send (DCTS) bit indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

4.1.9.2 Delta Data Set Ready, Bit 1

The Delta Data Set Ready (DDSR) bit indicates that the nDSR input has changed state since the last time the MSR was read.

4.1.9.3 Trailing Edge Of Ring Indicator, Bit 2

The Trailing Edge of Ring Indicator (TERI) bit indicates that the nRI input has changed from logic "0" to logic "1".

4.1.9.4 Delta Data Carrier Detect, Bit 3

The Delta Data Carrier Detect (DDCD) bit indicates that the nDCD input to the chip has changed state.

Note: Whenever bits 0, 1, 2, or 3 are set to a logic "1", a MODEM Status Interrupt is generated.

4.1.9.5 Clear To Send, Bit 4

The Clear To Send bit is the complement of the Clear To Send input (nCTS). If the Loop bit of the MCR is set to logic "1", this bit is equivalent to nRTS in the MCR.

4.1.9.6 Data Set Ready, Bit 5

The Data Set Ready bit is the complement of the Data Set Ready input (nDSR). If the Loop bit of the MCR is set to logic "1", this bit is equivalent to DTR in the MCR.

4.1.9.7 Ring Indicator, Bit 6

The Ring Indicator bit is the complement of the Ring Indicator input (nRI). If the Loop bit of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

4.1.9.8 Data Carrier Detect, Bit 7

The Data Carrier Detect bit is the complement of the Data Carrier Detect input (nDCD). If the Loop bit of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

4.1.10 SCRATCHPAD REGISTER (SCR)

The Scratchpad register (Address Offset =7H, DLAB =X, READ/WRITE) has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

4.1.11 PROGRAMMABLE BAUD RATE GENERATOR DIVISOR LATCHES

The internal Baud Rate Generator (BRG) using the Programmable Baud Rate Generator Divisor Latches DDL and DDM (Address Offset = 0 and 1, DLAB = 1, READ/WRITE) is capable of taking any clock input (DC to 3 MHz) and

dividing it by any divisor from 1 to 65535. The Baud Rate Generator output is 16x the baud rate. Two 8-bit latches store the divisor in 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the DDL and DDM registers the BRG clock is divided by 3. If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the clock is divided by 2 with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is a 1.8462 MHz clock.

Table 9 shows the baud rates possible with a 1.8462 MHz clock.

Table 9 - Baud Rates Using 1.8462 MHz Clock

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL*	CROC: BIT 7 OR 6
50	2307	0.03	X
75	1538	0.03	X
110	1049	0.005	X
134.5	858	0.01	X
150	769	0.03	X
300	384	0.16	X
600	192	0.16	X
1200	96	0.16	X
1800	64	0.16	X
2000	58	0.5	X
2400	48	0.16	X
3600	32	0.16	X
4800	24	0.16	X
7200	16	0.16	X
9600	12	0.16	X
19200	6	0.16	X
38400	3	0.16	X
57600	2	1.6	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

4.1.12 THE AFFECTS OF RESET ON THE UART REGISTERS

The RESET Function (Table 10) details the affects of RESET on each of the Serial Port registers.

Table 10 - RESET Function

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.	RESET	Bit 0 is high; Bits 1 - 7 low
FIFO Control	RESET	All bits low
Line Control Reg.	RESET	All bits low
MODEM Control Reg.	RESET	All bits low
Line Status Reg.	RESET	All bits low except 5 - 6 high
MODEM Status Reg.	RESET	Bits 0 - 3 low; Bits 4 - 7 input
TXD1, TXD2	RESET	High
INTRPT (RCVR errs)	RESET/Read LSR	Low
INTRPT (RCVR Data Ready)	RESET/Read RBR	Low
INTRPT (THRE)	RESET/ReadIIR/Write THR	Low

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
OUT2B	RESET	High
RTSB	RESET	High
DTRB	RESET	High
OUT1B	RESET	High
RCVR FIFO	RESET/FCR1*FCR0/_FCR0	All bits low
XMIT FIFO	RESET/FCR1*FCR0/_FCR0	All bits low

4.2 FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = “1”, IER bit 0 = “1”), RCVR interrupts occur as follows:

1. The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.
2. The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.
3. The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.
4. The data ready bit (LSR bit 0)is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO time-out interrupts occur as follows:

1. A FIFO time-out interrupt occurs if all the following conditions exist:
   - at least one character is in the FIFO
   - The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay.)
   - The most recent CPU read of the FIFO was longer than 4 continuous character times ago.

2. This will cause a maximum character received to interrupt issued delay of 160 msec at 300 BAUD with a 12 bit character.
3. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baud rate).
4. When a time-out interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.
5. When a time-out interrupt has not occurred the time-out timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = “1”, IER bit 1 = “1”), XMIT interrupts occur as follows:

1. The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.
2. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmit FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character time-out and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

4.3 FIFO Polled Mode Operation

With FCR bit 0 = “1” resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user’s program will check RCVR and XMITTER status via the LSR. LSR definitions for the FIFO Polled Mode are as follows:

1. Bit 0=1 as long as there is one byte in the RCVR FIFO.
2. Bits 1 to 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2=0.
3. Bit 5 indicates when the XMIT FIFO is empty.
4. Bit 6 indicates that both the XMIT FIFO and shift register are empty.
5. Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or time-out condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Table 11 - Individual UART Channel Register Summary

REGISTER ADDRESS*	REGISTER NAME	REGISTER SYMBOL	BIT 0	BIT 1
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 0 (Note 1)	Data Bit 1
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 0	Data Bit 1
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	”0” if Interrupt Pending	Interrupt ID Bit
ADDR = 2	FIFO Control Register (Write Only)	FCR	FIFO Enable	RCVR FIFO Reset
ADDR = 3	Line Control Register	LCR	Word Length Select Bit 0 (WLS0)	Word Length Select Bit 1 (WLS1)
ADDR = 4	MODEM Control Register	MCR	Data Terminal Ready (DTR)	Request to Send (RTS)
ADDR = 5	Line Status Register	LSR	Data Ready (DR)	Overrun Error (OE)
ADDR = 6	MODEM Status Register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)
ADDR = 7	Scratch Register (Note 4)	SCR	Bit 0	Bit 1
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 0	Bit 1
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 8	Bit 9

*DLAB is Bit 7 of the Line Control Register (ADDR = 3).
Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
Note 2: When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Table 12 - Individual UART Channel Register Summary Continued

BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Enable Receiver Line Status Interrupt (ELSI)	Enable MODEM Status Interrupt (EMSI)	0	0	0	0

BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Interrupt ID Bit	Interrupt ID Bit (Note 5)	0	0	FIFOs Enabled (Note 5)	FIFOs Enabled (Note 5)
XMIT FIFO Reset	DMA Mode Select (Note 6)	Reserved	Reserved	RCVR Trigger LSB	RCVR Trigger MSB
Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
OUT1 (Note 3)	OUT2 (Note 3)	Loop	0	0	0
Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) (Note 2)	Error in RCVR FIFO (Note 5)
Trailing Edge Ring Indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note 3: This bit no longer has a pin associated with it.
Note 4: When operating in the XT mode, this register is not available.
Note 5: These bits are always zero in the non-FIFO mode.
Note 6: Writing a one to this bit has no effect. DMA modes are not supported in this chip.

4.4 Notes On Serial Port FIFO Mode Operation

4.4.1 GENERAL

The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

4.4.2 TX AND RX FIFO OPERATION

The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. **The UART will prevent loads to the Tx FIFO if it currently holds 16 characters.** Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. **Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt.**

This one character Tx interrupt delay will remain active until at least two bytes have been loaded into the FIFO, concurrently. When the Tx FIFO empties after this condition, the Tx interrupt will be activated without a one character delay.

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun

Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. **To prevent the software from having to check for this situation the chip incorporates a time-out interrupt.**

The time-out interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The time-out interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (256K baud).

5 PARALLEL PORT

The SP37E760 incorporates an IBM XT/AT compatible parallel port. The SP37E760 supports the optional PS/2 type bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) parallel port modes. Refer to the SP37E760 Configuration Registers and the following hardware configuration description for information on disabling, powering down, changing the base address, and selecting the mode of operation of the parallel port.

The SP37E760 also incorporates SMSC's ChiProtect circuitry, which prevents possible damage to the parallel port due to printer power-up.

The functionality of the Parallel Port is achieved through the use of eight addressable ports, with their associated registers and control gating. The control and data port are read/write by the CPU, the status port is read/write in the EPP mode. The address map and bit encoding of the Parallel Port registers is shown in Table 13; the Parallel Port Connector is shown in Table 14.

Table 13 - Parallel Port Registers

	BASE ADDRESS OFFSET	D0	D1	D2	D3	D4	D5	D6	D7
DATA PORT[1]	00H	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
STATUS PORT[1]	01H	TMOUT	0	0	nERR	SLCT	PE	nACK	nBUSY
CONTROL PORT[1]	02H	STROBE	AUTOFD	nINIT	SLC	IRQE	PCD	0	0
EPP ADDR PORT[2,3]	03H	PD0	PD1	PD2	PD3	PD4	PD5	PD6	AD7
EPP DATA PORT 0[2,3]	04H	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
EPP DATA PORT 1[2,3]	05H	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
EPP DATA PORT 2[2,3]	06H	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
EPP DATA PORT 3[2,3]	07H	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7

Note[1] These registers are available in all modes.
Note[2] These registers are only available in EPP mode.
Note[3] For EPP mode, IOCHRDY must be connected to the ISA bus.

Table 14 - Parallel Port Connector

HOST CONNECTOR	PIN #		STANDARD	EPP	ECP
	TQFP	QFP			
1	75	77	nSTROBE	nWrite	nStrobe
2-9	69-66,64-61	71-68, 66-63	PD<0:7>	PData<0:7>	PData<0:7>
10	60	62	nACK	Intr	nAck
11	59	61	BUSY	nWait	Busy, PeriphAck(3)
12	58	60	PE	(NU)	PError, nAckReverse(3)
13	57	59	SLCT	(NU)	Select
14	74	76	nAUOTFD	nDatastb	nAutoFd, HostAck(3)
15	73	75	nERROR	(NU)	nFault(1) nPeriphRequest(3)
16	72	74	nINIT	(NU)	nInit(1) nReverseRqst(3)
17	71	73	nSLCTIN	nAddrstrb	nSelectIn(1,3)

(1) = Compatible Mode
(3) = High Speed Mode

Note: For the cable interconnection required for ECP support and the Slave Connector pin numbers, refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.09, Jan. 7, 1993. This document is available from Microsoft.

5.1 IBM XT/AT COMPATIBLE, BI-DIRECTIONAL AND EPP MODES

5.1.1 DATA PORT

ADDRESS OFFSET = 00H

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus with the rising edge of the nIOW input. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation in SPP mode, PD0 - PD7 ports are buffered (not latched) and output to the host CPU.

5.1.2 STATUS PORT

ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. The contents of this register are latched for the duration of an nIOR read cycle. The bits of the Status Port are defined as follows:

5.1.2.1 BIT 0 TMOUT - TIME OUT

This bit is valid in EPP mode only and indicates that a 10 usec time out has occurred on the EPP bus. A logic "0" means that no time out error has occurred; a logic "1" means that a time out error has been detected. This bit is cleared by a RESET. Writing a one to this bit clears the time out status bit. On a write, this bit is self clearing and does not require a write of a zero. Writing a zero to this bit has no effect.

BITS 1, 2 - are not implemented as register bits, during a read of the Printer Status Register these bits are a low level.

BIT 3 nERR - nERROR

The level on the nERROR input is read by the CPU as bit 3 of the Printer Status Register. A logic "0" means an error has been detected; a logic "1" means no error has been detected.

5.1.2.1.1 BIT 4 SLCT - PRINTER SELECTED STATUS

The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic "1" means the printer is on line; a logic "0" means it is not selected.

5.1.2.1.2 BIT 5 PE - PAPER END

The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic "1" indicates a paper end; a logic "0" indicates the presence of paper.

5.1.2.2 BIT 6 nACK - nACKNOWLEDGE

The level on the nACK input is read by the CPU as bit 6 of the Printer Status Register. A logic 0 means that the printer has received a character and can now accept another. A logic "1" means that it is still processing the last character or has not received the data.

5.1.2.3 BIT 7 nBUSY - nBUSY

The complement of the level on the nBUSY input is read by the CPU as bit 7 of the Printer Status Register. A logic 0 in this bit means that the printer is busy and cannot accept a new character. A logic "1" means that it is ready to accept the next character.

5.1.3 CONTROL PORT

ADDRESS OFFSET = 02H

The Control Port is located at an offset of '02H' from the base address. The Control Register is initialized by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

5.1.3.1 BIT 0 STROBE - STROBE

This bit is inverted and output onto the nSTROBE output.

5.1.3.2 BIT 1 AUTOFD - AUTOFEED

This bit is inverted and output onto the nAUTOFD output. A logic "1" causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

5.1.3.3 BIT 2 nINIT - nINITIATE OUTPUT

This bit is output onto the nINIT output without inversion.

5.1.3.4 BIT 3 SLCTIN - PRINTER SELECT INPUT

This bit is inverted and output onto the nSLCTIN output. A logic "1" on this bit selects the printer; a logic "0" means the printer is not selected.

5.1.3.5 BIT 4 IRQE - INTERRUPT REQUEST ENABLE

The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going nACK input. When the IRQE bit is programmed low the IRQ is disabled.

5.1.3.6 BIT 5 PCD - PARALLEL CONTROL DIRECTION

Parallel Control Direction is valid in extended mode only (CR#1<3>=0). In printer mode, the direction is always out regardless of the state of this bit. In bi-directional mode, a logic "0" means that the printer port is in output mode (write); a logic "1" means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

5.1.4 EPP ADDRESS PORT

ADDRESS OFFSET = 03H

The EPP Address Port is located at an offset of '03H' from the base address. The address register is cleared at initialization by RESET. During a WRITE operation, the contents of DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports, the leading edge of nIOW causes an EPP ADDRESS WRITE cycle to be performed, the trailing edge of IOW latches the data for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read, the leading edge of IOR causes an EPP ADDRESS READ cycle to be performed and the data output to the host CPU, the deassertion of ADDRSTB latches the PData for the duration of the IOR cycle. This register is only available in EPP mode.

5.1.5 EPP DATA PORT 0

ADDRESS OFFSET = 04H

The EPP Data Port 0 is located at an offset of '04H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the contents of DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports, the leading edge of nIOW causes an EPP DATA WRITE cycle to be performed, the trailing edge of IOW latches the data for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read, the leading edge of IOR causes an EPP READ cycle to be performed and the data output to the host CPU, the deassertion of DATASTB latches the PData for the duration of the IOR cycle. This register is only available in EPP mode.

5.1.6 EPP DATA PORT 1

ADDRESS OFFSET = 05H

The EPP Data Port 1 is located at an offset of '05H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

5.1.7 EPP DATA PORT 2

ADDRESS OFFSET = 06H

The EPP Data Port 2 is located at an offset of '06H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

5.1.8 EPP DATA PORT 3

ADDRESS OFFSET = 07H

The EPP Data Port 3 is located at an offset of '07H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

5.2 EPP 1.9 OPERATION

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10μsec have elapsed from the start of the EPP cycle (nIOR or nIOW asserted) to nWAIT being deasserted (after command). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

During an EPP cycle, if STROBE is active, it overrides the EPP write signal forcing the PDx bus to always be in a write mode and the nWRITE signal to always be asserted.

5.2.1 SOFTWARE CONSTRAINTS

Before an EPP cycle is executed, the software must ensure that the control register bit PCD is a logic "0" (i.e. a 04H or 05H should be written to the Control port). If the user leaves PCD as a logic "1", and attempts to perform an EPP write, the chip is unable to perform the write (because PCD is a logic "1") and will appear to perform an EPP read on the parallel bus, no error is indicated.

5.2.2 EPP 1.9 WRITE

The timing for a write operation (address or data) is shown in timing diagram EPP 1.9 Write Data or Address cycle. IOCHRDY is driven active low at the start of each EPP write and is released when it has been determined that the write cycle can complete. The write cycle can complete under the following circumstances:

1. If the EPP bus is not ready (nWAIT is active low) when nDATASTB or nADDRSTB goes active then the write can complete when nWAIT goes inactive high.
2. If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of nDATASTB, nWRITE or nADDRSTB. The write can complete once nWAIT is determined inactive.

Write Sequence of operation

1. The host selects an EPP register, places data on the SData bus and drives nIOW active.
2. The chip drives IOCHRDY inactive (low).
3. If WAIT is not asserted, the chip must wait until WAIT is asserted.
4. The chip places address or data on PData bus, clears PDIR, and asserts nWRITE.
5. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
6. Peripheral deasserts nWAIT, indicating that any setup requirements have been satisfied and the chip may begin the termination phase of the cycle.
7. A) The chip deasserts nDATASTB or nADDRSTRB, this marks the beginning of the termination phase. If it has not already done so, the peripheral should latch the information byte now.
   B) The chip latches the data from the SData bus for the PData bus and asserts (releases) IOCHRDY allowing the host to complete the write cycle.
8. Peripheral asserts nWAIT, indicating to the host that any hold time requirements have been satisfied and acknowledging the termination of the cycle.
9. Chip may modify nWRITE and nPDATA in preparation for the next cycle.

5.2.3 EPP 1.9 READ

The timing for a read operation (data) is shown in timing diagram EPP Read Data cycle. IOCHRDY is driven active low at the start of each EPP read and is released when it has been determined that the read cycle can complete. The read cycle can complete under the following circumstances:

1. If the EPP bus is not ready (nWAIT is active low) when nDATASTB goes active then the read can complete when nWAIT goes inactive high.
2. If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of WRITE or before nDATASTB goes active. The read can complete once nWAIT is determined inactive.

Read Sequence of Operation

1. The host selects an EPP register and drives nIOR active.
2. The chip drives IOCHRDY inactive (low).
3. If WAIT is not asserted, the chip must wait until WAIT is asserted.
4. The chip tri-states the PData bus and deasserts nWRITE.
5. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
6. Peripheral drives PData bus valid.
7. Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
8. A) The chip latches the data from the PData bus for the SData bus, deasserts DATASTB or nADDRSTRB, this marks the beginning of the termination phase.
   B) The chip drives the valid data onto the SData bus and asserts (releases) IOCHRDY allowing the host to complete the read cycle.
9. Peripheral tri-states the PData bus and asserts nWAIT, indicating to the host that the PData bus is tri-stated.
10. Chip may modify nWRITE, PDIR and nPDATA in preparation for the next cycle.

5.3 EPP 1.7 OPERATION

When the EPP 1.7 mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle (nIOR or nIOW asserted) to the end of the cycle nIOR or nIOW deasserted). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

5.3.1 SOFTWARE CONSTRAINTS

Before an EPP cycle is executed, the software must ensure that the control register bits D0, D1 and D3 are set to zero. Also, bit D5 (PCD) is a logic “0” for an EPP write or a logic “1” for and EPP read.

5.3.2 EPP 1.7 WRITE

The timing for a write operation (address or data) is shown in timing diagram EPP 1.7 Write Data or Address cycle. IOCHRDY is driven active low when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The write cycle can complete when nWAIT is inactive high.

Write Sequence of Operation

1. The host sets PDIR bit in the control register to a logic “0”. This asserts nWRITE.
2. The host selects an EPP register, places data on the SData bus and drives nIOW active.
3. The chip places address or data on PData bus.
4. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
5. If nWAIT is asserted, IOCHRDY is deasserted until the peripheral deasserts nWAIT or a time-out occurs.
6. When the host deasserts nI0W the chip deasserts nDATASTB or nADDRSTRB and latches the data from the SData bus for the PData bus.

7. Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

5.3.3 EPP 1.7 READ

The timing for a read operation (data) is shown in timing diagram EPP 1.7 Read Data cycle. IOCHRDY is driven active low when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The read cycle can complete when nWAIT is inactive high.

Read Sequence of Operation

1. The host sets PDIR bit in the control register to a logic "1". This deasserts nWRITE and tri-states the PData bus.
2. The host selects an EPP register and drives nIOR active.
3. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
4. If nWAIT is asserted, IOCHRDY is deasserted until the peripheral deasserts nWAIT or a time-out occurs.
5. The Peripheral drives PData bus valid.
6. The Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
7. When the host deasserts nI0R the chip deasserts nDATASTB or nADDRSTRB.
8. Peripheral tri-states the PData bus.
9. Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

Table 15 - EPP Pin Descriptions

EPP SIGNAL	EPP NAME	TYPE	DESCRIPTION
nWRITE	nWrite	O	This signal is active low. It denotes a write operation.
PD<0:7>	Address/Data	I/O	Bi-directional EPP byte wide address and data bus.
INTR	Interrupt	I	This signal is active high and positive edge triggered. (Pass through with no inversion, Same as SPP).
WAIT	nWait	I	This signal is active low. It is driven inactive as a positive acknowledgment from the device that the transfer of data is completed. It is driven active as an indication that the device is ready for the next transfer.
DATASTB	nData Strobe	O	This signal is active low. It is used to denote data read or write operation.
RESET	nReset	O	This signal is active low. When driven active, the EPP device is reset to its initial operational mode.
ADDRSTB	nAddress Strobe	O	This signal is active low. It is used to denote address read or write operation.
PE	Paper End	I	Same as SPP mode.
SLCT	Printer Selected Status	I	Same as SPP mode.
NERR	Error	I	Same as SPP mode.
PDIR	Parallel Port Direction	O	This output shows the direction of the data transfer on the parallel port bus. A low means an output/write condition and a high means an input/read condition. This signal is normally a low (output/write) unless PCD of the control register is set or if an EPP read cycle is in progress.

Note 1: SPP and EPP can use 1 common register.

Note 2: nWrite is the only EPP output that can be over-ridden by SPP control port during an EPP cycle. For correct EPP read cycles, PCD is required to be a low.

5.4 EXTENDED CAPABILITIES PARALLEL PORT

ECP provides a number of advantages, some of which are listed below. The individual features are explained in greater detail in the remainder of this section.

- High performance half-duplex forward and reverse channel
- Interlocked handshake, for fast reliable transfer
- Optional single byte RLE compression for improved throughput (64:1)
- Channel addressing for low-cost peripherals
- Maintains link and data layer separation
- Permits the use of active output drivers
- Permits the use of adaptive signal timing
- Peer-to-peer capability

5.4.1 VOCABULARY

The following terms are used in this document:

assert When a signal asserts it transitions to a "true" state, when a signal deasserts it transitions to a "false" state.

forward Host to Peripheral communication.

reverse Peripheral to Host communication.

Pword A port word; equal in size to the width of the ISA interface. For this implementation, PWord is always 8 bits.

1 A high level

0 A low level

These terms may be considered synonymous:

- PeriphClk, nAck
- HostAck, nAutoFd
- PeriphAck, Busy
- nPeriphRequest, nFault
- nReverseRequest, nInit
- nAckReverse, PError
- Xflag, Select
- ECPMode, nSelectIn
- HostClk, nStrobe

Reference Document:
IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev 1.09, Jan 7, 1993. This document is available from Microsoft. The bit map of the Extended Parallel Port registers is shown in Table 16.

Table 16 - ECP Registers

	D7	D6	D5	D4	D3	D2	D1	D0
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
ecpAFifo[2]	Addr/RLE	Address or RLE field						
dsr[1]	nBusy	nAck	PError	Select	nFault	0	0	0
dcr[1]	0	0	Direction	ackIntEn	SelectIn	nInit	autofd	strobe
cFifo[2]	Parallel Port Data FIFO							
ecpDFifo[2]	ECP Data FIFO							
tFifo[2]	Test FIFO							
cnfgA	0	0	0	1	0	0	0	0
cnfgB	compress	intrValue	0	0	0	0	0	0
ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty

Note[1] These registers are available in all modes.

Note[2] All FIFOs use one common 16 byte FIFO.

5.4.2 ISA IMPLEMENTATION STANDARD

This specification describes the standard ISA interface to the Extended Capabilities Port (ECP). All ISA devices supporting ECP must meet the requirements contained in this section or the port will not be supported by Microsoft. For a description of the ECP Protocol, please refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.09, Jan.7, 1993. This document is available from Microsoft.

5.4.3 DESCRIPTION

The port is software and hardware compatible with existing parallel ports so that it may be used as a standard LPT port if ECP is not required. The port is designed to be simple and requires a small number of gates to implement. It does not do any "protocol" negotiation, rather it provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward and reverse directions.

Small FIFOs are employed in both forward and reverse directions to smooth data flow and improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes deep. The port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The port also supports run length encoded (RLE) decompression (required) in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. Hardware support for compression is optional.

Table 17 - ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
nStrobe	O	During write operations nStrobe registers data or address into the slave on the asserting edge (handshakes with Busy).
Pdata 7:0	I/O	Contains address or data or RLE data.
Nack	I	Indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
PeriphAck (Busy)	I	This signal deasserts to indicate that the peripheral can accept data. This signal handshakes with nStrobe in the forward direction. In the reverse direction this signal indicates whether the data lines contain ECP command information or data. The peripheral uses this signal to flow control in the forward direction. It is an "interlocked" handshake with nStrobe. PeriphAck also provides command information in the reverse direction.
Perror (nAckReverse)	I	Used to acknowledge a change in the direction the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. It is an "interlocked" handshake with nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select	I	Indicates printer on line.
NAutoFd (HostAck)	O	Requests a byte of data from the peripheral when asserted, handshaking with nAck in the reverse direction. In the forward direction this signal indicates whether the data lines contain ECP address or data. The host drives this signal to flow control in the reverse direction. It is an "interlocked" handshake with nAck. HostAck also provides command information in the forward phase.
NFault (nPeriphRequest)	I	Generates an error interrupt when asserted. This signal provides a mechanism for peer-to-peer communication. This signal is valid only in the forward direction. During ECP Mode the peripheral is permitted (but not required) to drive this pin low to request a reverse transfer. The request is merely a "hint" to the host; the host has ultimate control over the transfer direction. This signal would be typically used to generate an interrupt to the host CPU.
NInit	O	Sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. The peripheral is only allowed to drive the bi-directional data bus while in ECP Mode and HostAck is low and nSelectIn is high.
NSelectIn	O	Always deasserted in ECP mode.

5.4.4 REGISTER DEFINITIONS

The register definitions are based on the standard IBM addresses for LPT. All of the standard printer ports are supported. The additional registers attach to an upper bit decode of the standard LPT port definition to avoid conflict with standard ISA devices. The port is equivalent to a generic parallel port interface and may be operated in that mode. The port registers vary depending on the mode field in the ecr (Table 19). Table 18 lists these dependencies. Operation of the devices in modes other that those specified is undefined.

Table 18 - ECP Register Definitions

NAME	ADDRESS (Note 1)	ECP MODES	FUNCTION
data	+000h R/W	000-001	Data Register
ecpAFifo	+000h R/W	011	ECP FIFO (Address)
dsr	+001h R/W	All	Status Register
dcr	+002h R/W	All	Control Register
cFifo	+400h R/W	010	Parallel Port Data FIFO
ecpDFifo	+400h R/W	011	ECP FIFO (DATA)
tFifo	+400h R/W	110	Test FIFO
cnfgA	+400h R	111	Configuration Register A
cnfgB	+401h R/W	111	Configuration Register B
ecr	+402h R/W	All	Extended Control Register

Note 1: These addresses are added to the parallel port base address as selected by configuration register or jumpers.
Note 2: All addresses are qualified with AEN. Refer to the AEN pin definition.

Table 19 - Mode Descriptions

MODE	DESCRIPTION (Refer to ECR Register Description)
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the configuration registers)
101	(Reserved)
110	Test mode
111	Configuration mode

5.4.4.1 DATA and ecpAFifo PORT

ADDRESS OFFSET = 00H
Modes 000 and 001 (Data Port)

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus on the rising edge of the nIOW input. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation, PD0 - PD7 ports are read and output to the host CPU.

Mode 011 (ECP FIFO - Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is only defined for the forward direction (direction is 0). Refer to the ECP Parallel Port Forward Timing Diagram, located in the Timing Diagrams section of this data sheet .

5.4.4.2 DEVICE STATUS REGISTER (dsr)

ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. Bits 0 - 2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status Port are defined as follows:

5.4.4.2.1 BIT 3 nFault

The level on the nFault input is read by the CPU as bit 3 of the Device Status Register.

5.4.4.2.2 BIT 4 Select

The level on the Select input is read by the CPU as bit 4 of the Device Status Register.

5.4.4.2.3 BIT 5 PError

The level on the PError input is read by the CPU as bit 5 of the Device Status Register. Printer Status Register.

5.4.4.2.4 BIT 6 nAck

The level on the nAck input is read by the CPU as bit 6 of the Device Status Register.

5.4.4.2.5 BIT 7 nBusy

The complement of the level on the BUSY input is read by the CPU as bit 7 of the Device Status Register.

5.4.4.3 DEVICE CONTROL REGISTER (dcr)

ADDRESS OFFSET = 02H

The Control Register is located at an offset of '02H' from the base address. The Control Register is initialized to zero by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

5.4.4.3.1 BIT 0 STROBE - STROBE

This bit is inverted and output onto the nSTROBE output.

5.4.4.3.2 BIT 1 AUTOFD - AUTOFEED

This bit is inverted and output onto the nAUTOFD output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

5.4.4.3.3 BIT 2 nINIT - nINITIATE OUTPUT

This bit is output onto the nINIT output without inversion.

5.4.4.3.4 BIT 3 SELECTIN

This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

5.4.4.3.5 BIT 4 ackIntEn - INTERRUPT REQUEST ENABLE

The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU due to a low to high transition on the nACK input. Refer to the description of the interrupt under Operation, Interrupts.

5.4.4.3.6 BIT 5 DIRECTION

If mode=000 or mode=010, this bit has no effect and the direction is always out regardless of the state of this bit. In all other modes, Direction is valid and a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

5.4.4.3.7 Bits 6 and 7

during a read are a low level, and cannot be written.

5.4.4.4 cFifo (Parallel Port Data FIFO)

ADDRESS OFFSET = 400h
Mode = 010

Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

5.4.4.5 ecpDFifo (ECP Data FIFO)

ADDRESS OFFSET = 400H
Mode = 011

Bytes written or DMAed from the system to this FIFO, when the direction bit is 0, are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

Data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO when the direction bit is 1. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

5.4.4.6 tFifo (Test FIFO Mode)

ADDRESS OFFSET = 400H
Mode = 110

Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction.

Data in the tFIFO will not be transmitted to the to the parallel port lines using a hardware protocol handshake. However, data in the tFIFO may be displayed on the parallel port data lines.

The tFIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full tFIFO, the new data is not accepted into the tFIFO. If an attempt is made to read data from an empty tFIFO, the last data byte is re-read again. The full and empty bits must always keep track of the correct FIFO state. The tFIFO will transfer data at the maximum ISA rate so that software may generate performance metrics.

The FIFO size and interrupt threshold can be determined by writing bytes to the FIFO and checking the full and serviceIntr bits.

The writeIntrThreshold can be determined by starting with a full tFIFO, setting the direction bit to 0 and emptying it a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

The readIntrThreshold can be determined by setting the direction bit to 1 and filling the empty tFIFO a byte at a time until **serviceIntr** is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

Data bytes are always read from the head of tFIFO regardless of the value of the direction bit. For example if 44h, 33h, 22h is written to the FIFO, then reading the tFIFO will return 44h, 33h, 22h in the same order as was written.

5.4.4.7 cnfgA (Configuration Register A)

ADDRESS OFFSET = 400H
Mode = 111

This register is a read only register. When read, 10H is returned. This indicates to the system that this is an 8-bit implementation. (PWord = 1 byte)

5.4.4.8 cnfgB (Configuration Register B)

ADDRESS OFFSET = 401H
Mode = 111

5.4.4.8.1 BIT 7 compress

This bit is read only. During a read it is a low level. This means that this chip does not support hardware RLE compression. It does support hardware de-compression!

5.4.4.8.2 BIT 6 intrValue

Returns the value on the ISA iRq line to determine possible conflicts.

5.4.4.8.3 BITS 5:0 Reserved

During a read are a low level. These bits cannot be written.

5.4.4.9 ecr (Extended Control Register)

ADDRESS OFFSET = 402H
Mode = all

This register controls the extended ECP parallel port functions (Table 20).

5.4.4.9.1 BITS 7,6,5

These bits are Read/Write and select the Mode.

BIT 4 nErrIntrEn

Read/Write (Valid only in ECP Mode)
1: Disables the interrupt generated on the asserting edge of nFault.
0: Enables an interrupt pulse on the high to low edge of nFault. Note that an interrupt will be generated if nFault is asserted (interrupting) and this bit is written from a "1" to a "0". This prevents interrupts from being lost in the time between the read of the ecr and the write of the ecr.

5.4.4.9.2 BIT 3 dmaEn

Read/Write
1: Enables DMA (DMA starts when serviceIntr is "0").
0: Disables DMA unconditionally.

5.4.4.9.3 BIT 2 serviceIntr

Read/Write
1: Disables DMA and all of the service interrupts.
0: Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred serviceIntr bit shall be set to a "1" by hardware, it must be reset to "0" to re-enable the interrupts. Writing this bit to a "1" will not cause an interrupt.
case dmaEn=1:
During DMA (this bit is set to a "1" when terminal count is reached).
case dmaEn=0 direction=0:
This bit shall be set to "1" whenever there are writeIntrThreshold or more bytes free in the FIFO.
case dmaEn=0 direction=1:
This bit shall be set to "1" whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.

5.4.4.9.4 BIT 1 full

Read only
1: The FIFO cannot accept another byte or the FIFO is completely full.
0: The FIFO has at least 1 free byte.

5.4.4.9.5 BIT 0 empty

Read only
1: The FIFO is completely empty.
0: The FIFO contains at least 1 byte of data.

Table 20 - Extended Control Register

R/W	MODE
000:	Standard Parallel Port mode . In this mode the FIFO is reset and common collector drivers are used on the control lines (nStrobe, nAutoFd, nInit and nSelectIn). Setting the direction bit will not tri-state the output drivers in this mode.
001:	PS/2 Parallel Port mode. Same as above except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. All drivers have active pull-ups (push-pull).
010:	Parallel Port FIFO mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when direction is 0. All drivers have active pull-ups (push-pull).

R/W	MODE
011:	ECP Parallel Port Mode. In the forward direction (direction is 0) bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. In the reverse direction (direction is 1) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo. All drivers have active pull-ups (push-pull).
100:	Selects EPP Mode: In this mode, EPP is selected if the EPP supported option is selected in configuration register CR4. All drivers have active pull-ups (push-pull).
101:	Reserved
110:	Test Mode. In this mode the FIFO may be written and read, but the data will not be transmitted on the parallel port. All drivers have active pull-ups (push-pull).
111:	Configuration Mode. In this mode the confgA, confgB registers are accessible at 0x400 and 0x401. All drivers have active pull-ups (push-pull).

5.4.5 OPERATION

5.4.5.1 Mode Switching/Software Control

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (modes 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer.

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

Once in an extended forward mode the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In this case all control signals will be deasserted before the mode switch. In an ECP reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001. Since the automatic hardware ECP reverse handshake only cares about the state of the FIFO it may have acquired extra data which will be discarded. It may in fact be in the middle of a transfer when the mode is changed back to 000 or 001. In this case the port will deassert nAutoFd independent of the state of the transfer. The design shall not cause glitches on the handshake signals if the software meets the constraints above.

5.4.5.2 ECP Operation

Prior to ECP operation the Host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol. This is a somewhat complex negotiation carried out under program control in mode 000. After negotiation, it is necessary to initialize some of the port bits. The following are required:

- Set Direction = 0, enabling the drivers.
- Set strobe = 0, causing the nStrobe signal to default to the deasserted state.
- Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.
- Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo respectively.

Note that all FIFO data transfers are byte wide and byte aligned. Address/RLE transfers are byte-wide and only allowed in the forward direction.

The host may switch directions by first switching to mode = 001, negotiating for the forward or reverse channel, setting direction to 1 or 0, then setting mode = 011. When direction is 1 the hardware shall handshake for each ECP read data byte and attempt to fill the FIFO. Bytes may then be read from the ecpDFifo as long as it is not empty .

ECP transfers may also be accomplished (albeit slowly) by handshaking individual bytes under program control in mode = 001, or 000.

5.4.5.3 Termination from ECP Mode

Termination from ECP Mode is similar to the termination from Nibble/Byte Modes. The host is permitted to terminate from ECP Mode only in specific well-defined states. The termination can only be executed while the bus is in the forward direction. To terminate while the channel is in the reverse direction, it must first be transitioned into the forward direction.

5.4.5.4 Command/Data

ECP Mode supports two advanced features to improve the effectiveness of the protocol for some applications. The features are implemented by allowing the transfer of normal 8 bit data or 8-bit commands (Table 21).

When in the forward direction, normal data is transferred when HostAck is high and an 8 bit command is transferred when HostAck is low.
The most significant bit of the command indicates whether it is a run-length count (for compression) or a channel address.

When in the reverse direction, normal data is transferred when PeriphAck is high and an 8 bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero. Reverse channel addresses are seldom used and may not be supported in hardware.

Table 21 - Forward Channel Commands (HostAck Low) Reverse Channel Commands (PeripAck Low) Data Compression

D7	D[6:0]
0	Run-Length Count (0-127) (mode 0011 0X00 only)
1	Channel Address (0-127)

The SP37E760 supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Run length encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.
Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. A run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

5.4.5.5 Pin Definition

The drivers for nStrobe, nAutoFd, nInit and nSelectIn are open-collector in mode 000 and are push-pull in all other modes.

5.4.5.6 ISA Connections

The interface can never stall causing the host to hang. The width of data transfers is strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide, byte aligned and end on a byte boundary. (The PWord value can be obtained by reading Configuration Register A, cnfgA, described in the next section). Single byte wide transfers are always possible with standard or PS/2 mode using program control of the control signals.

5.4.5.7 Interrupts

The interrupts are enabled by **serviceIntr** in the **ecr** register.
serviceIntr = 1 Disables the DMA and all of the service interrupts.
serviceIntr = 0Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupt is generated immediately when this bit is changed from a 1 to a 0. This can occur during Programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold.

The interrupt generated is ISA friendly in that it must pulse the interrupt line low, allowing for interrupt sharing. After a brief pulse low following the interrupt event, the interrupt line is tri-stated so that other interrupts may assert.
An interrupt is generated when:
1. For DMA transfers: When **serviceIntr** is 0, dmaEn is 1 and the DMA TC is received.
2. For Programmed I/O:

a. When **serviceIntr** is “0”, dmaEn is “0”, direction is “0” and there are writeIntrThreshold or more free bytes in the FIFO. Also, an interrupt is generated when **serviceIntr** is cleared to “0” whenever there are writeIntrThreshold or more free bytes in the FIFO.

b.(1)When **serviceIntr** is 0, dmaEn is 0, direction is “1” and there are readIntrThreshold or more bytes in the FIFO. Also, an interrupt is generated when **serviceIntr** is cleared to “0” whenever there are readIntrThreshold or more bytes in the FIFO.

3. When nErrIntrEn is “0” and nFault transitions from high to low or when nErrIntrEn is set from “1” to “0” and nFault is asserted.
4. When ackIntEn is “1” and the nAck signal transitions from a low to a high.

5.4.5.8 FIFO Operation

The FIFO threshold is set in the chip configuration registers. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. (FIFO test mode will be addressed separately.) After a reset, the FIFO is disabled. Each data byte is transferred by a Programmed I/O cycle or PDRQ depending on the selection of DMA or Programmed I/O mode.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.
A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host must be very responsive to the service request. This is the desired case for use with a “fast” system.

A high value of threshold (i.e. 12) is used with a “sluggish” system by affording a long latency period after a service request, but results in more frequent service requests.

5.4.5.9 DMA TRANSFERS

Notes:
PDRQ - Currently selected Parallel Port DRQ channel
nPDACK - Currently selected Parallel Port DACK channel
PINTR - Currently selected Parallel Port IRQ channel

5.4.5.9.1 Typical DMA Mode Transfers

DMA transfers are always to or from the ecpDFifo, tFifo or CFifo. DMA utilizes the standard PC DMA services. To use the DMA transfers, the host first sets up the direction and state as in the programmed I/O case. Then it programs the DMA controller in the host with the desired count and memory address. Lastly it sets dmaEn to “1” and **serviceIntr** to “0”. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, disabling DMA. In order to prevent possible blocking of refresh requests dReq shall not be asserted for more than 32 DMA cycles in a row. The FIFO is enabled directly by asserting nPDACK and addresses need not be valid. PINTR is generated when a TC is received. PDRQ must not be asserted for more than 32 DMA cycles in a row. After the 32nd cycle, PDRQ must be kept unasserted until nPDACK is deasserted for a minimum of 350nsec. (Note: The only way to properly terminate DMA transfers is with a TC).

DMA may be disabled in the middle of a transfer by first disabling the host DMA controller. Then setting serviceIntr to 1, followed by setting dmaEn to 0, and waiting for the FIFO to become empty or full.

Restarting the DMA is accomplished by enabling DMA in the host, setting dmaEn to 1, followed by setting serviceIntr to 0.

5.4.5.9.2 DMA Mode - Transfers from the FIFO to the Host

(Note: In the reverse mode, the peripheral may not continue to fill the FIFO if it runs out of data to transfer, even if the chip continues to request more data from the peripheral).

The ECP activates the PDRQ pin whenever there is data in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The ECP will deactivate the PDRQ pin when the FIFO becomes empty or when the TC becomes true (qualified by nPDACK), indicating that no more data is required. PDRQ goes inactive after nPDACK goes active for the last byte of a data transfer (or on the active edge of nIOR, on the last byte, if no edge is present on nPDACK). If PDRQ goes inactive due to the FIFO going empty, then PDRQ is active again as

soon as there is one byte in the FIFO. If PDRQ goes inactive due to the TC, then PDRQ is active again when there is one byte in the FIFO, and **serviceIntr** has been re-enabled. (Note: A data underrun may occur if PDRQ is not removed in time to prevent an unwanted cycle).

5.4.5.10 Programmed I/O Mode or Non-DMA Mode

The ECP or parallel port FIFOs may also be operated using interrupt driven programmed I/O. Software can determine the writeIntrThreshold, readIntrThreshold, and FIFO depth by accessing the FIFO in Test Mode.

Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. To use the programmed I/O transfers, the host first sets up the direction and state, sets dmaEn to 0 and **serviceIntr** to 0.

The ECP requests programmed I/O transfers from the host by activating the PINTR pin. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

Note: A threshold of 16 is equivalent to a threshold of 15. These two cases are treated the same.

5.4.5.11 Programmed I/O - Transfers from the FIFO to the Host

In the reverse direction an interrupt occurs when serviceIntr is 0 and readIntrThreshold bytes are available in the FIFO. If at this time the FIFO is full it can be emptied completely in a single burst, otherwise readIntrThreshold bytes may be read from the FIFO in a single burst.

readIntrThreshold =(16-<threshold>) data bytes in FIFO

An interrupt is generated when **serviceIntr** is 0 and the number of bytes in the FIFO is greater than or equal to (16-<threshold>). (If the threshold = 12, then the interrupt is set whenever there are 4-16 bytes in the FIFO.) The PINT pin can be used for interrupt-driven systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. If at this time the FIFO is full, it can be completely emptied in a single burst, otherwise a minimum of (16-<threshold>) bytes may be read from the FIFO in a single burst.

5.4.5.12 Programmed I/O - Transfers from the Host to the FIFO

In the forward direction an interrupt occurs when serviceIntr is 0 and there are writeIntrThreshold or more bytes free in the FIFO. At this time if the FIFO is empty it can be filled with a single burst before the empty bit needs to be re-read. Otherwise it may be filled with writeIntrThreshold bytes.

writeIntrThreshold = (16-<threshold>) free bytes in FIFO

An interrupt is generated when **serviceIntr** is 0 and the number of bytes in the FIFO is less than or equal to <threshold>. (If the threshold = 12, then the interrupt is set whenever there are 12 or less bytes of data in the FIFO.) The PINT pin can be used for interrupt-driven systems. The host must respond to the request by writing data to the FIFO. If at this time the FIFO is empty, it can be completely filled in a single burst, otherwise a minimum of (16-<threshold>) bytes may be written to the FIFO in a single burst. This process is repeated until the last byte is transferred into the FIFO.

6 AUTO POWER MANAGEMENT

Power management is provided for the following SP37E760 logical devices: UART1, UART2 and the Parallel Port. For each logical device two types of power management are provided; direct powerdown and auto powerdown.

Direct powerdown is controlled by the powerdown bits in the configuration registers. One bit is provided for each logical device. Auto powerdown can be enabled for each logical device by setting the Auto Powerdown Enable bits in the configuration registers. In addition, a chip-level hardware powerdown function has been provided through the PWRGD pin. Refer to Table 1 and to other descriptions of the PWRGD function, for example section CONFIGURATION, for more information.

6.1 Pin Behavior

The SP37E760 is specifically designed for portable PC systems where power conservation is a primary concern. Consequently, the behavior of the device pins during powerdown are very important.

6.1.1 SYSTEM INTERFACE PINS

Table 22 gives the state of the system interface pins in the powerdown state. Pins unaffected by the powerdown are labeled “Unchanged”. Input pins are “Disabled” to prevent them from causing currents internal to the SP37E760 when they have indeterminate input values.

Table 22 - State of System Pins in Auto Powerdown

SYSTEM PINS	STATE IN AUTO POWERDOWN
Input Pins	
IOR	Unchanged
IOW	Unchanged
A[0:9]	Unchanged
D[0:7]	Unchanged
RESET	Unchanged
IDENT	Unchanged
DACK	Unchanged
TC	Unchanged
Output Pins	
FINTR	Unchanged (low)
DB[0:7]	Unchanged
FDRQ	Unchanged (low)

6.2 UART Power Management

Direct UART power management is controlled by the UART1 and UART2 Power Down bits in Configuration Register 2. Refer to section CR02 on page 49 for more information.

UART Auto Power Management is enabled by the UART 1 and UART 2 Enable bits in Configuration Register 7 (see section CR07 on page 51). When set, these bits enable the following auto power management features:

1. The transmitter enters auto powerdown when the transmit buffer and transmit shift register are empty.
2. The receiver enters powerdown when the following conditions are all met:
   - Receive FIFO is empty
   - The receiver is waiting for a start bit.

Note: While in the powerdown state, the Ring Indicator interrupts are still valid and are activated when the RI inputs change.

The UART transmitters exit the powerdown state on a write to the XMIT buffer. The UART receivers exit the auto powerdown state when RXDx changes state.

6.3 Parallel Port

Direct parallel port power management is controlled by the Parallel Port Power bit in Configuration Register 1. Refer to section CR01 on page 48 for more information.

Parallel port Auto Power Management is enabled by the Parallel Port Enable bit in Configuration Register 7 (see section CR07 on page 51). When set, this bit allows the ECP or EPP logical parallel port blocks to be placed into the powerdown state as follows:

The EPP logic is in powerdown under any of the following conditions:

1. EPP is not enabled in the configuration registers.
2. EPP is not selected through ecr while in ECP mode.

The ECP logic is in powerdown under any of the following conditions:

1. ECP is not enabled in the configuration registers.
2. SPP, PS/2 Parallel port or EPP mode is selected through ecr while in ECP mode.

The parallel port logic can change powerdown modes when the ECP mode is changed through the ecr register or when the parallel port mode is changed through the configuration registers.

7 CONFIGURATION

The configuration of the SP37E760 is programmed through hardware selectable Configuration Access Ports that appear when the chip is placed into the configuration state. The SP37E760 logical device blocks, if enabled, will operate normally in the configuration state.

7.1 Configuration Access Ports

The Configuration Access Ports are the CONFIG PORT, the INDEX PORT, and the DATA PORT (Table 23). The base address of these registers is controlled by the nRTS2/SYSOPT pin (see Table 1). To determine the configuration base address, the state of the nRTS2/SYSOPT pin is latched by the falling edge of a hardware reset. If the latched state is a 0, the base address of the Configuration Access Ports is located at address 3F0H; if the latched state is a 1, the base address is located at address 370H.

Table 23 - Configuration Access Ports

PORT NAME	SYSOPT = 0	SYSOPT = 1	TYPE
CONFIG PORT	0x3F0	0x370	WRITE
INDEX PORT	0x3F0	0x370	READ/WRITE[1,2]
DATA PORT	INDEX PORT + 1		READ/WRITE[1]

Note[1]: The INDEX and DATA ports are active only when the SP37E760 is in the configuration state.
Note[2]: The INDEX PORT is only readable in the configuration state.

7.2 Configuration State

The configuration registers are used to select programmable chip options. The SP37E760 operates in two possible states: the run state and the configuration state. After power up by default the chip is in the run state. To program the configuration registers, the configuration state must be explicitly enabled. Programming the configuration registers typically follows this sequence:

1. Enter the Configuration State,
2. Program the Configuration Register(s),
3. Exit the Configuration State.

7.2.1 ENTERING THE CONFIGURATION STATE

To enter the configuration state write the Configuration Access Key to the CONFIG PORT. The Configuration Access Key is one byte of 55H data. The SP37E760 will automatically activate the Configuration Access Ports following this procedure.

7.2.2 CONFIGURATION REGISTER PROGRAMMING

The SP37E760 contains configuration registers CR00-CR2F. After the SP37E760 enters the configuration state, configuration registers can be programmed by first writing the register index number (00 - 2FH) to the Configuration Select Register (CSR) through the INDEX PORT and then writing or reading the configuration register contents through the DATA PORT. Configuration register access remains enabled until the configuration state is explicitly exited.

7.2.3 EXITING THE CONFIGURATION STATE

To exit the configuration state, write one byte of AAH data to the CONFIG PORT. The SP37E760 will automatically deactivate the Configuration Access Ports following this procedure, at which point configuration register access cannot occur until the configuration state is explicitly re-enabled.

7.2.4 PROGRAMMING EXAMPLE

The following is a configuration register programming example written in Intel 8086 assembly language.

```
;------------------------------.
; ENTER CONFIGURATION STATE   |
;------------------------------‘
MOV     DX,3F0H
MOV     AX,055H
OUT     DX,AL
;------------------------------.
; CONFIGURE REGISTERS CR0-CRx |
;------------------------------‘
MOV     DX,3F0H
MOV     AL,00H
OUT     DX,AL          ;Point to CR0
MOV     DX,3F1H
MOV     AL,3FH
OUT     DX,AL          ;Update CR0
;
MOV     DX,3F0H
MOV     AL,01H
OUT     DX,AL          ;Point to CR1
MOV     DX,3F1H
MOV     AL,9FH
OUT     DX,AL          ;Update CR1
;
; Repeat for all CRx registers
;
;------------------------------.
; EXIT CONFIGURATION STATE    |
;------------------------------‘
MOV     DX,3F0H
MOV     AX,AAH
OUT     DX,AL
```

7.2.5 CONFIGURATION SELECT REGISTER (CSR)

The Configuration Select Register can only be accessed when the SP37E760 is in the configuration state. The CSR is located at the INDEX PORT address and must be initialized with configuration register index before the register can be accessed using the DATA PORT.

7.3 Configuration Registers Description

The configuration registers are set to their default values at power up (Table 24) and are not affected by RESET, except where noted in the register descriptions that follow.

Table 24 - Configuration Registers

DEFAULT	INDEX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
28H	CR00	Valid	Reserved			Reserved	Reserved	Reserved	
9CH	CR01	Lock CRx	Reserved			PP MODE	PP PWR	Reserved	
88H	CR02	UART2 PWR	Reserved			UART1 PWR	Reserved		
70H	CR03	ADRX/ IRQ_B	Reserved				ADRX IRQ_B	Reserved	PWRGD
00H	CR04	Reserved	EPP Type	MIDI 2	MIDI 1	Reserved		PP Ext. Modes	
00H	CR05	Reserved							

DEFAULT	INDEX	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
FFH	CR06	Reserved							
00H	CR07	Auto Power Management				Reserved		Reserved	
00H	CR08	ADRA7	ARDA6	ADRA5	ADRA4	0	0	0	0
00H	CR09	ADRx Config Cntrl		Reserved			ADRA10	ADRA9	ADRA8
00H	CR0A	Reserved	Reserved	Reserved		ECP FIFO Threshold			
00H	CR0B	Reserved							
02H	CR0C	UART 2 Speed	UART 1 Speed	UART 2 Mode			UART 2 Duplex	UART 2 XMIT Polarity	UART 2 RCV Polarity
28H	CR0D	Device ID							
Revision	CR0E	Device Revision							
00H	CR0F	Test 7	Test 6	Test 5	Test 4	Test 3	Test 2	Test 1	Test 0
00H	CR10	Test 15	Test 14	Test 13	Test 12	Test 11	Test 10	Test 9	Test 8
80H	CR11	Test 23	Test 22	Test 21	Test 20	Test 19	Test 18	Test 17	Test 16
00H	CR12 - CR13	Reserved							
-	CR14	Reserved							
-	CR15	UART1 FIFO Control Shadow							
-	CR16	UART2 FIFO Control Shadow							
03H	CR17	Reserved							
00H	CR18 - CR1D	Reserved							
80H	CR1E	Reserved							
00H	CR1F	Reserved							
3CH	CR20	Reserved						0	0
00H	CR21-CR22	Reserved							
00H	CR23	Parallel Port - ADR[9:2]							
00H	CR24	Serial Port 1 - ADR[9:3]							0
00H	CR25	Serial Port 2 - ADR[9:3]							0
00H	CR26	Reserved				Parallel Port DRQ			
00H	CR27	Reserved				Parallel Port IRQ			
00H	CR28	Serial 1 IRQ				Serial 2 IRQ			
00H	CR29	Reserved			Reserved	IRQIN IRQ			
00H	CR2A	Reserved							
00H	CR2B	SCE Base I/O ADDR[10:3]							
00H	CR2C	Reserved				Serial Port 2 DMA Channel Select			
03H	CR2D	Reserved							
00H	CR2E	Software Select A							
00H	CR2F	Software Select B							

7.3.1 CR00

CR00 can only be accessed in the configuration state and after the CSR has been initialized to 00H. The default value of this register after power up is 28H (Table 25).

Table 25 - CR00

BIT NO.	BIT NAME	DESCRIPTION
0:2	Reserved	Read Only. A read returns 0
3	Reserved	Read Only.
4,5,6	Reserved	Read only. A read returns bit 5 as a 1 and bits 4 and 6 as a 0.
7	Valid	A high level on this software controlled bit can be used to indicate that a valid configuration cycle has occurred. The control software must take care to set this bit at the appropriate times. Set to zero after power up. This bit has no effect on any other hardware in the chip.

7.3.2 CR01

CR01 can only be accessed in the configuration state and after the CSR has been initialized to 01H. The default value of this register after power up is 9CH (Table 26).

Table 26 - CR01

BIT NO.	BIT NAME	DESCRIPTION
0,1	Reserved	Read Only. A read returns “0”.
2	Parallel Port Power[1]	A high level on this bit, supplies power to the Parallel Port (Default). A low level on this bit puts the Parallel Port in low power mode.
3	Parallel Port Mode	Parallel Port Mode. A high level on this bit, sets the Parallel Port for Printer Mode (Default). A low level on this bit enables the Extended Parallel port modes. Refer to Bits 0 and 1 of CR4
4	Reserved	Read Only. A read returns “1”.
5,6	Reserved	Read Only. A read returns “0”.
7	Lock CRx	A high level on this bit enables the reading and writing of CR00 - CR2F (Default). A low level on this bit disables the reading and writing of CR00 - CR2F. Note: once the Lock Crx bit is set to “0”, this bit can only be set to “1” by a hard reset or power-up reset.

Note[1]: Power Down bits disable the respective logical device and associated pins, however the power down bit does not disable the selected address range for the logical device. To disable the host address registers the logical device’s base address must be set below 100h. Devices that are powered down but still reside at a valid I/O base address will participate in Plug-and-Play range checking.

7.3.3 CR02

CR02 can only be accessed in the configuration state and after the CSR has been initialized to 02H. The default value of this register after power up is 88H (Table 27).

Table 27 - CR02

BIT NO.	BIT NAME	DESCRIPTION
0:2	Reserved	Read Only. A read returns "0".
3	UART1 Power Down[1]	A high level on this bit, allows normal operation of the Primary Serial Port (Default). A low level on this bit places the Primary Serial Port into Power Down Mode.
4:6	Reserved	Read Only. A read returns "0".
7	UART2 Power Down[1]	A high level on this bit, allows normal operation of the Secondary Serial Port, including the SCE block (Default). A low level on this bit places the Secondary Serial Port including the SCE block into Power Down Mode.

Note[1]: Power Down bits disable the respective logical device and associated pins, however the power down bit does not disable the selected address range for the logical device. To disable the host address registers the logical device's base address must be set below 100h. Devices that are powered down but still reside at a valid I/O base address will participate in Plug-and-Play range checking.

7.3.4 CR03

CR03 can only be accessed in the configuration state and after the CSR has been initialized to 03H. The default value after power up is 70H (Table 28).

Table 28 - CR03

BIT NO.	BIT NAME	DESCRIPTION
0	PWRGD	Bit 0 — Pin Function 0 — PWRGD (default) 1 — Reserved
1	Reserved	Reserved- Read as Zero
3	Reserved	Reserved - Read as zero
4	Reserved	Reserved - Read as one
5	Reserved	Reserved - Read as one
6	Reserved	Reserved - Read as one
7,2	ADRx/ IRQ_B	Bit - 7 / Bit - 2 — Pin 92 0 / 0 — Default 0 / 1 — Reserved 1 / 0 — ADRX 1 / 1 — IRQ_B

Note[1]: See Note[2] in section CR05 on page 50.

7.3.5 CR04

CR04 can only be accessed in the configuration state and after the CSR has been initialized to 04H. The default value after power up is 00H (Table 29).

Table 29 - CR04: Parallel and Serial Extended Setup Register

BIT NO.	BIT NAME	DESCRIPTION		
1,0	Parallel Port Extended Modes	Bit 1	Bit 0	If CR1 bit 3 is a low level then:
		0	0	Standard and Bi-directional Modes (SPP) (default)
		0	1	EPP Mode and SPP
		1	0	ECP Mode[2]
		1	1	ECP Mode & EPP Mode[1,2]
2,3	Reserved	. Reserved – Read as 0		
4	MIDI 1[3]	Serial Clock Select Port 1: A low level on this bit, disables MIDI support, clock = divide by 13 (default). A high level on this bit enables MIDI support, clock = divide by 12.		
5	MIDI 2[3]	Serial Clock Select Port 2: A low level on this bit, disables MIDI support, clock = divide by 13 (default). A high level on this bit enables MIDI support, clock = divide by 12.		
6	EPP Type	0 = EPP 1.9 (default) 1 = EPP 1.7		
7	Reserved	Reserved - Read as 0.		

Note[1]: In this mode, EPP can be selected through the ecr register of ECP as mode 100.
Note[2]: In these modes, 2 drives can be supported directly, 3 or 4 drives must use external 4 drive support. SPP can be selected through the ecr register of ECP as mode 000.
Note[3]: MIDI Support: The Musical Instrumental Digital Interface (MIDI) operates at 31.25Kbaud (+/-1%) which can be derived from 125KHz. (24 MHz/12=2 MHz, 2 MHz/16=125 KHz).

7.3.6 CR05

(Reserved). The default value after power up is 00H .

7.3.7 CR06

(Reserved). The default value of this register after power up is FFH.

7.3.8 CR07

CR07 can only be accessed in the configuration state and after the CSR has been initialized to 07H. The default value of this register after power up is 00H (Table 30). CR07 controls auto power management.

Table 30 - CR07: Auto Power Management and Boot Drive Select

BIT NO.	BIT NAME	DESCRIPTION
0,1	Reserved	Read as 0.
2	Reserved	Read as 0.
3	Reserved	Read as 0.
4	Parallel Port Enable	This bit controls the AUTOPOWER DOWN feature of the Parallel Port. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by POR or a hardware reset.
5	UART 2 Enable	This bit controls the AUTOPOWER DOWN feature of the UART2. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by POR or a hardware reset.
6	UART 1 Enable	This bit controls the AUTOPOWER DOWN feature of the UART1. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by POR or a hardware reset.
7	Reserved	Read as 0.

7.3.9 CR08

CR08 can only be accessed in the configuration state and after the CSR has been initialized to 08H. The default value of this register after power up is 00H (Table 31). CR08 contains the lower 4 bits (ADRA7:4) for the ADRx address decoder. Bits D0 - D3 are Reserved. Reserved bits cannot be written and return 0 when read.

Table 31 - CR08: ADRx Lower Address Decode

D7	D6	D5	D4	D3	D2	D1	D0
ADRA7	ADRA6	ADRA5	ADRA4	Reserved			

7.3.10 CR09

CR09 can only be accessed in the configuration state and after the CSR has been initialized to 09H. The default value of this register after power up is 00H (Table 32). CR09 contains the upper 3 bits (ADRA10:8) of the ADRx address decoder and the ADRx Configuration Control Bits D[7:6]. The ADRx Configuration Control Bits configure the ADRx Address Decoder (Table 33).

Table 32 - CR09: ADRx Upper Address Decoder and Configuration

D7	D6	D5	D4	D3	D2	D1	D0
ADRx CONFIGURATION CONTROL		Reserved			ADRA10	ADRA9	ADRA8

Table 33 - ADRx Configuration Bits

ADRx CONFIGURATION CONTROL		DESCRIPTION
D7	D6	
0	0	ADRx disabled
0	1	1 Byte decode A[3:0]=0000b
1	0	8 Byte block decode A[3:0]=0XXXb
1	1	16 byte block decode A[3:0]=XXXXb

Note: Upper Address Decode requirements: nCS = '0' is required to qualify the ADRx output.

7.3.11 CR0A

CR0A can only be accessed in the configuration state and after the CSR has been initialized to 0AH. The default value of this register after power up is 00H (Table 34). CR0A defines the FIFO threshold for the ECP mode parallel port. Bits D[7:4] are Reserved. Reserved Bits cannot be written and return 0 when read.

Table 34 - CR0A

D7	D6	D5	D4	D3	D2	D1	D0
RESERVED		RESERVED		ECP FIFO THRESHOLD			
				THR3	THR2	THR1	THR0

7.3.12 CR0B

CR0B can only be accessed in the configuration state and after the CSR has been initialized to 0BH. The default value of this register after power up is 00H.

7.3.13 CR0C

CR0C can only be accessed in the configuration state and after the CSR has been initialized to 0CH. The default value of this register after power up is 02H (Table 35). CR0C controls the operating mode of the UART. This register is reset to the default state by a POR or a hardware reset.

Table 35 - CR0C

BIT NO.	BIT NAME	DESCRIPTION
0	UART 2 RCV Polarity	0 = RX input active high (default). 1 = RX input active low.
1	UART 2 XMIT Polarity	0 = TX output active high. 1 = TX output active low (default).
2	UART 2 Duplex	This bit is used to define the FULL/HALF DUPLEX operation of UART 2. 1 = Half duplex 0 = Full duplex (default)
3, 4, 5	UART 2 MODE	UART 2 Mode 5 4 3 0 0 0 Standard (default) Other Values Reserved
6	UART 1 Speed	This bit enables the high speed mode of UART 1. 1 = High speed enabled 0 = Standard (default)

BIT NO.	BIT NAME	DESCRIPTION
7	UART Speed	This bit enables the high speed mode of UART 2. 1 = High speed enabled 0 = Standard (default)

7.3.14 CR0D

CR0D can only be accessed in the configuration state and after the CSR has been initialized to 0DH. This register is read only. CR0D contains the SP37E760 Device ID. The default value of this register after power up is 28H.

7.3.15 CR0E

CR0E can only be accessed in the configuration state and after the CSR has been initialized to 0EH. This register is read only. CR0E contains the current SP37E760 Chip Revision Level.

7.3.16 CR0F

CR0F can only be accessed in the configuration state and after the CSR has been initialized to 0FH. The default value of this register after power up is 00H (Table 36). CR0F is a test control register and all bits must be treated as Reserved. Note: all test modes are reserved for SMSC use. Activating test mode registers may produce undesired results.

Table 36 - CR0F

BIT NO.	BIT NAME	DESCRIPTION
0	Test 0	RESERVED FOR SMSC USE
1	Test 1	
2	Test 2	
3	Test 3	
4	Test 4	
5	Test 5	
6	Test 6	
7	Test 7	

7.3.17 CR10

CR10 can only be accessed in the configuration state and after the CSR has been initialized to 10H. The default value of this register after power up is 00H (Table 37) CR10 is a test control register and all bits must be treated as Reserved. NOTE: all test modes are reserved for SMSC use. Activating test mode registers may produce undesired results.

Table 37 - CR10

BIT NO.	BIT NAME	DESCRIPTION
0	Test 8	RESERVED FOR SMSC USE
1	Test 9	
2	Test 10	
3	Test 11	
4	Test 12	
5	Test 13	
6	Test 14	
7	Test 15	

7.3.18 CR11

CR11 can only be accessed in the configuration state and after the CSR has been initialized to 11H. The default value of this register after power up is 80H (Table 38). CR11 is a test control register and all bits must be treated as

Reserved. Note: all test modes are reserved for SMSC use. Activating test mode registers may produce undesired results.

Table 38 - CR11

BIT NO.	BIT NAME	DESCRIPTION
0	Test 16	RESERVED FOR SMSC USE
1	Test 17	
2	Test 18	
3	Test 19	
4	Test 20	
5	Test 21	
6	Test 22	
7	Test 23	

7.3.19 CR12 - CR13

CR12 - CR13 are reserved and Read Only. The default value of these registers after power up is 00H.

7.3.20 CR14

(Reserved).

7.3.21 CR15

CR15 can only be accessed in the configuration state and after the CSR has been initialized to 15H. CR15 shadows the bits in the write-only UART1 run-time FCR register (Table 39).

Table 39 - CR15: UART1 FCR Shadow Register

		D7	D6	D5	D4	D3	D2	D1	D0	Default
CR 15	R	RCVR TRIGGER MSB	RCVR TRIGGE R LSB	Reserved		DMA MODE SELECT	XMIT FIFO RESE T	RCVR FIFO RESE T	FIFO ENABL E	N/A

7.3.22 CR16

CR161 can only be accessed in the configuration state and after the CSR has been initialized to 16H. CR16 shadows the bits in the write-only UART2 run-time FCR register (Table 40).

Table 40 - CR16: UART2 FCR Shadow Register

		D7	D6	D5	D4	D3	D2	D1	D0	Default
CR16	R	RCVR TRIGGE R MSB	RCVR TRIGGER LSB	Reserved		DMA MODE SELECT	XMIT FIFO RESET	RCVR FIFO RESET	FIFO ENABLE	N/A

7.3.23 CR17

(Reserved). The default value of this register after power up is 003H.

7.3.24 CR18 - CR1D

CR18 - CR1D registers are Reserved and Read Only . The default value of these registers after power up is 00H.

7.3.25 CR1E

(Reserved). The default value of this register after power up is 80H.

7.3.26 CR1F

(Reserved). The default value of this register after power up is 00H.

7.3.27 CR20

(Reserved). The default value of this register after power up is 3CH.

7.3.28 CR21 - CR22

Registers CR21 - CR22 are Reserved. Reserved bits cannot be written and return 0 when read.

7.3.29 CR23

CR23 can only be accessed in the configuration state and after the CSR has been initialized to 23H. The default value of this register after power up is 00H (Table 41). CR23 is used to select the base address of the parallel port. If EPP is not enabled, the parallel port can be set to 192 locations on 4-byte boundaries from 100H - 3FCH; if EPP is enabled, the parallel port can be set to 96 locations on 8-byte boundaries from 100H - 3F8H (Table 42). To disable the parallel port, set ADR9 and ADR8 to zero.

Parallel Port Address Decoding: nCS = '0' and A10 = '0' are required to access the Parallel Port when in Compatible, Bi-directional, or EPP modes. A10 is active when in ECP mode.

Table 41 - CR23: Parallel Port Base Address Register

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2

Table 42 - Parallel Port Addressing Options

EPP ENABLED	ADDRESSING (LOW BITS) DECODE
No	A[1:0] = XXb
Yes	A[2:0] = XXXb

7.3.30 CR24

CR24 can only be accessed in the configuration state and after the CSR has been initialized to 24H. The default value of this register after power up is 00H (Table 43). CR24 is used to select the base address of Serial Port 1 (UART1). The serial port can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 1, set ADR9 and ADR8 to zero. Set CR24.0 to 0 when writing the UART1 Base Address.

Serial Port 1 Address Decoding: nCS = '0' and A10 = '0' are required to access UART1 registers. A[2:0] are decoded as XXXb.

Table 43 - CR24: UART1 Base Address Register

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	0

7.3.31 CR25

CR25 can only be accessed in the configuration state and after the CSR has been initialized to 25H. The default value of this register after power up is 00H (Table 44). CR25 is used to select the base address of Serial Port 2 (UART2). Serial Port 2 can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 2, set ADR9 and ADR8 to zero. Set CR25.0 to 0 when writing the UART2 Base Address.

Serial Port 2 Address Decoding: nCS = '0' and A10 = '0' are required to access UART2 registers. A[2:0] are decoded as XXXb.

Table 44 - CR25: UART2 Base Address Register

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3	0

7.3.32 CR26

CR26 can only be accessed in the Configuration State and after the CSR has been initialized to 26H. The default value of this register after power up is 00H (Table 45). CR26 is used to select the DMA for the Parallel Port (bits 0 - 3). Any unselected DMA Request output (DRQ) is in tristate.

Table 45 - CR26: PP DMA Selection Register

D3-D0	DMA SELECTED
0000	None
0001	DMA_A
0010	DMA_B
0011	DMA_C

7.3.33 CR27

CR27 can only be accessed in the configuration state and after the CSR has been initialized to 27H. The default value of this register after power up is 00H (Table 46). CR27 is used to select the Parallel Port (bits 3 - 0). Any unselected IRQ output (registers CR27 - CR29) is in tristate.

Table 46 - CR27: PP IRQ Selection Register

D3-D0	IRQ SELECTED
0000	None
0001	IRQ_A
0010	IRQ_B
0011	IRQ_C
0100	IRQ_D
0101	IRQ_E
0110	IRQ_F
0111	Reserved
1000	IRQ_H

7.3.34 CR28

CR28 can only be accessed in the configuration state and after the CSR has been initialized to 28H. The default value of this register after power up is 00H. CR28 is used to select the IRQ for Serial Port 1 (bits 7 - 4) and for Serial Port 2 (bits 3 - 0). Refer to the IRQ encoding for CR27 (Table 46). Any unselected IRQ output (registers CR27 - CR29) is in tristate.

To properly share an IRQ between UART1 and UART2:

1. Configure UART1 to use the desired IRQ pin.
2. Set UART2 to 0FH i.e., set CR28.[3:0] = 1111b. This selects the share IRQ mechanism. Refer to Table 47, below.

Table 47 - UART Interrupt Operation

UART1		UART2			IRQ PINS	
UART1 OUT2 bit	UART1 IRQ Output State	UART2 OUT2 bit	UART2 IRQ Output State	Share IRQ	UART1 Pin State	UART2 Pin State
0	Z	0	Z	No	Z	Z
1	asserted	0	Z	No	1	Z
1	de-asserted	0	Z	No	0	Z
0	Z	1	asserted	No	Z	1
0	Z	1	de-asserted	No	Z	0
1	asserted	1	asserted	No	1	1

UART1		UART2			IRQ PINS	
UART1 OUT2 bit	UART1 IRQ Output State	UART2 OUT2 bit	UART2 IRQ Output State	Share IRQ	UART1 Pin State	UART2 Pin State
1	asserted	1	de-asserted	No	1	0
1	de-asserted	1	asserted	No	0	1
1	de-asserted	1	de-asserted	No	0	0
0	Z	0	Z	Yes	Z	Z
1	asserted	0	Z	Yes	1	Z
1	de-asserted	0	Z	Yes	0	Z
0	Z	1	asserted	Yes	1	Z
0	Z	1	de-asserted	Yes	0	Z
1	asserted	1	asserted	Yes	1	Z
1	asserted	1	de-asserted	Yes	1	Z
1	de-asserted	1	asserted	Yes	1	Z
1	de-asserted	1	de-asserted	Yes	0	Z
It is the responsibility of the software to ensure that two IRQ's are not set to the same IRQ number. Potential damage to chip may result. **Note:** Z = Don't Care.						

7.3.35 CR29

CR29 can only be accessed in the configuration state and after the CSR has been initialized to 29H. The default value of this register after power up is 00H (Table 48). CR29 is used to select the IRQ mapping (bits 0 - 3) for the IRQIN pin. Refer to IRQ encoding for CR27 (Table 46). Any unselected IRQ output (registers CR27 - CR29) is in tristate.

Table 48 - CR29

BIT NO.	NAME	DESCRIPTION
0-3	IRQIN	Selects the IRQ for IRQIN
4-7	*RESERVED*	Not Writeable, Reads Return "0"

7.3.36 CR2A

Register CR2A is reserved. The default value of this register after power up is 00H.

7.3.37 CR2B

CR2B can only be accessed in the configuration state and after the CSR has been initialized to 2BH. The default value of this register after power up is 00H (Table 49). CR2B is used to set the SCE base address ADR[10:3]. The SCE base address can be set to 224 locations on 8-byte boundaries from 100H - 7F8H. To disable the SCE, set ADR10, ADR9 and ADR8 to zero.

SCE Address Decoding: nCS = '0' required to access SCE registers. A[2:0] are decoded as XXXb.

Table 49 - CR2B: SCE Base Address Register

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
ADR10	ADR9	ADR8	ADR7	ADR6	ADR5	ADR4	ADR3

7.3.38 CR2C

CR2C can only be accessed in the configuration state and after the CSR has been initialized to 2CH. The default value of this register after power up is 00H (Table 50). Bits D[3:0] of this register are used to select the DMA for the SCE. Bits D[7:4] are Reserved. Reserved bits cannot be written and return 0 when read. Any unselected DMA Request output (DRQ) is in tristate.

Table 50 - CR2C: SCE DMA Select Register

D3-D0	DMA SELECTED
0000	None
0001	DMA_A
0010	DMA_B
0011	DMA_C

7.3.39 CR2D

CR2D can only be accessed in the configuration state and after the CSR has been initialized to 2DH. The default value of this register after power up is 03H.

Table 51 - CR2D

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR2D	R/W	Reserved								0x03

7.3.40 CR2E

CR2E can only be accessed in the configuration state and after the CSR has been initialized to 2EH. The default value of this register after power up is 00H (Table 52).

Table 52 - CR2E

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR2E	R/W	Software Select A								0x00

7.3.41 CR2F

CR2F can only be accessed in the configuration state and after the CSR has been initialized to 2FH. The default value of this register after power up is 00H (Table 53).

Table 53 - CR2F

		D7	D6	D5	D4	D3	D2	D1	D0	DEFAULT
CR2F	R/W	Software Select B								0x00

8 OPERATIONAL DESCRIPTION

8.1 MAXIMUM GUARANTEED RATINGS

Operating Temperature Range ..... 0^oC to $+70^oC$
Storage Temperature Range ..... -55^o to $+150^oC$
Lead Temperature Range (soldering, 10 seconds) ..... $+325^oC$
Positive Voltage on any pin, with respect to Ground ..... +5.5V
Negative Voltage on any pin, with respect to Ground ..... -0.3V
Maximum V_{CC} ..... +5V

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

8.2 DC ELECTRICAL CHARACTERISTICS

(T_A = 0°C - 70°C, V_{cc} = +3.3 V ± 10%)

Table 54 – DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	
I_{CLK} Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	2.2			V	
Input Leakage (All I and IS buffers except PWRGD)						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{cc}
Input Current PWRGD	I_{OH}		75	150	µA	V_{IN} = 0

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IO12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
O12PD Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
O6 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -3mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
OD14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
OP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
IOP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O4 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 4mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -2mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{cc} (Note 1)
Supply Current Active	I_{CC}		15	20	mA	All outputs open.
Supply Current Standby	I_{CSBY}			100	µA	Note 3
ChiProtect (SLCT, PE, BUSY, nACK, nERROR)	I_{IL}			±10	µA	Chip in circuit: V_{CC} = 0V V_{IN} = 5.5V Max.
Backdrive Protect (nSLCTIN, nINIT, nAUTOFD, nSTROBE, PD[7:0])	I_{IL}			±10	µA	Chip in circuit: V_{CC} = 0V V_{IN} = 5.5V Max.

Note 1: Output leakage is measured with the current pins in high impedance as defined by the PWRGD pin.
Note 2: Output leakage is measured with the low driving output off, either for a high level output or a high impedance state defined by PWRGD.
Note 3: Defined by the device configuration with the PWRGD input low.

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{CC} = 3.3V

Table 55 - Clock Pin Loading

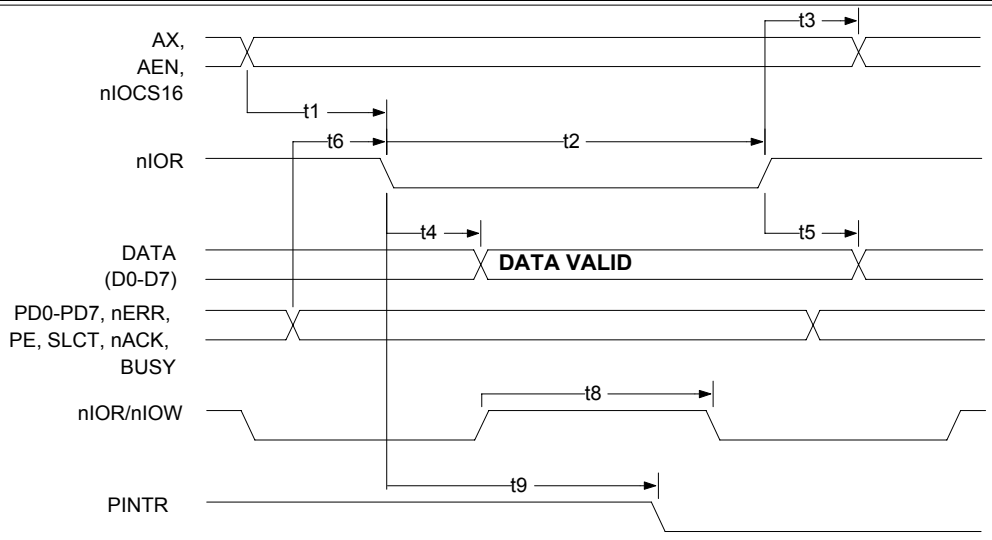
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Table 56 - Capacitive Loading per Output Pin

SIGNAL NAME	TOTAL CAPACITANCE (pF)
SD[0:7]	240
IOCHRDY	240
IRQs	120
DRQs	120
TXD	100
nRTS	100
nDTR	100
PD[7:0]	240
nSLCTIN	240
nINIT	240

9 AC TIMING

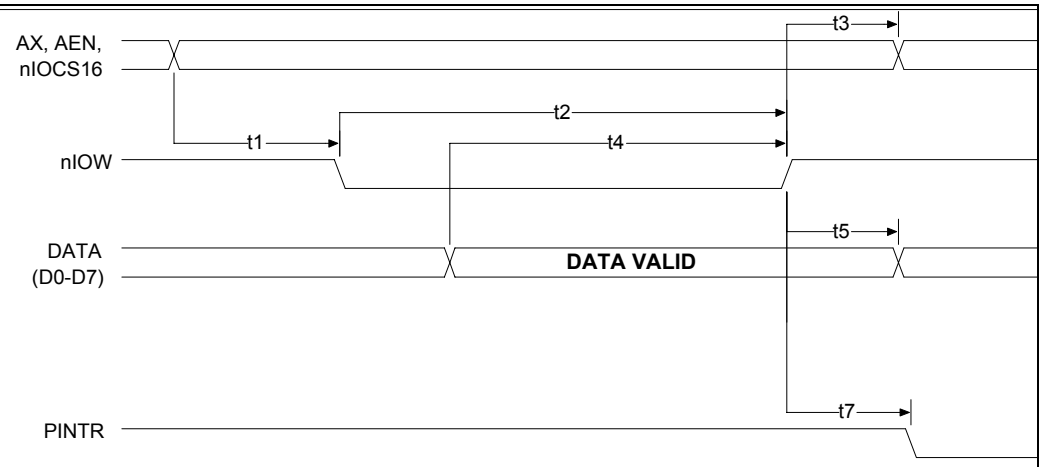
9.1 Host Timing



PINTR is the interrupt assigned to the Parallel Port

	Parameter	min	typ	max	units
t1	A0-A9, AEN, nIOCS16 Set Up to nIOR Low	40			ns
t2	nIOR Width	150			ns
t3	A0-A9, AEN, nIOCS16 Hold from nIOR High	10			ns
t4	Data Access Time from nIOR Low			100	ns
t5	Data to Float Delay from nIOR High	10		60	ns
t6	Parallel Port Setup		20		ns
t8	nIOR or nIOW Inactive for Transfers to and from ECP FIFO	150			ns
t9	nIOR Active to PINTR Inactive			260	ns

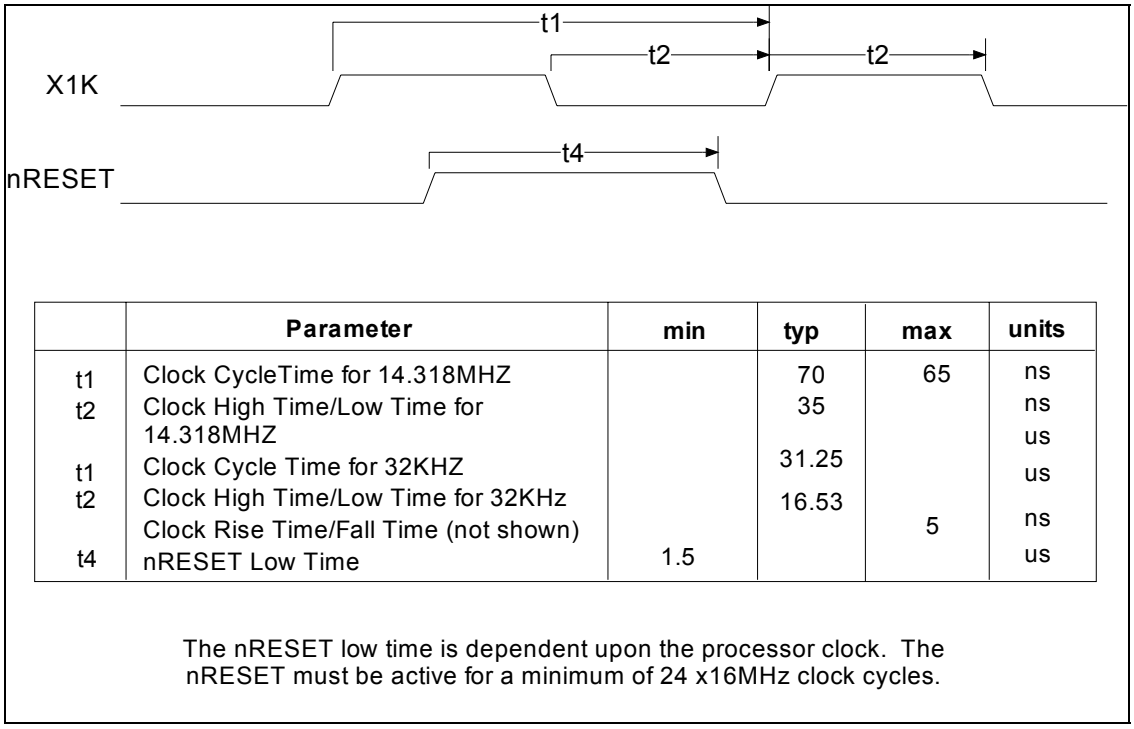
FIGURE 4 - MICROPROCESSOR READ TIMING



PINTR is the interrupt assigned to the Parallel Port

	Parameter	min	typ	max	units
t1	A0-A9, AEN, nIOCS16 Set Up to nIOW Low	40			ns
t2	nIOW Width	150			ns
t3	A0-A9, AEN, nIOCS16 Hold from nIOW High	10			ns
t4	Data Set Up Time to nIOW High	40			ns
t5	Data Hold Time from nIOW High	10			ns
t7	nIOW Inactive to PINTR Inactive			260	ns

FIGURE 5 - MICROPROCESSOR WRITE TIMING

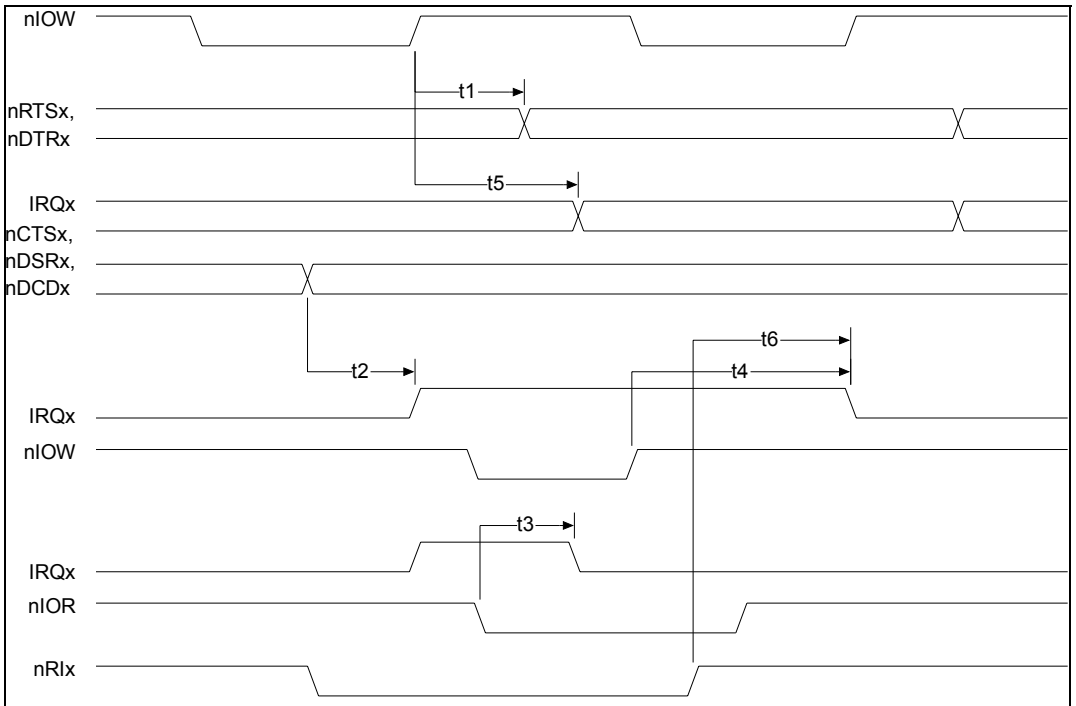


	Parameter	min	typ	max	units
t1	Clock CycleTime for 14.318MHZ		70	65	ns
t2	Clock High Time/Low Time for 14.318MHZ		35		ns
t1	Clock Cycle Time for 32KHZ		31.25		us
t2	Clock High Time/Low Time for 32KHz		16.53		us
	Clock Rise Time/Fall Time (not shown)			5	ns
t4	nRESET Low Time	1.5			us

The nRESET low time is dependent upon the processor clock. The nRESET must be active for a minimum of 24 x16MHz clock cycles.

FIGURE 6 - CLOCK TIMING

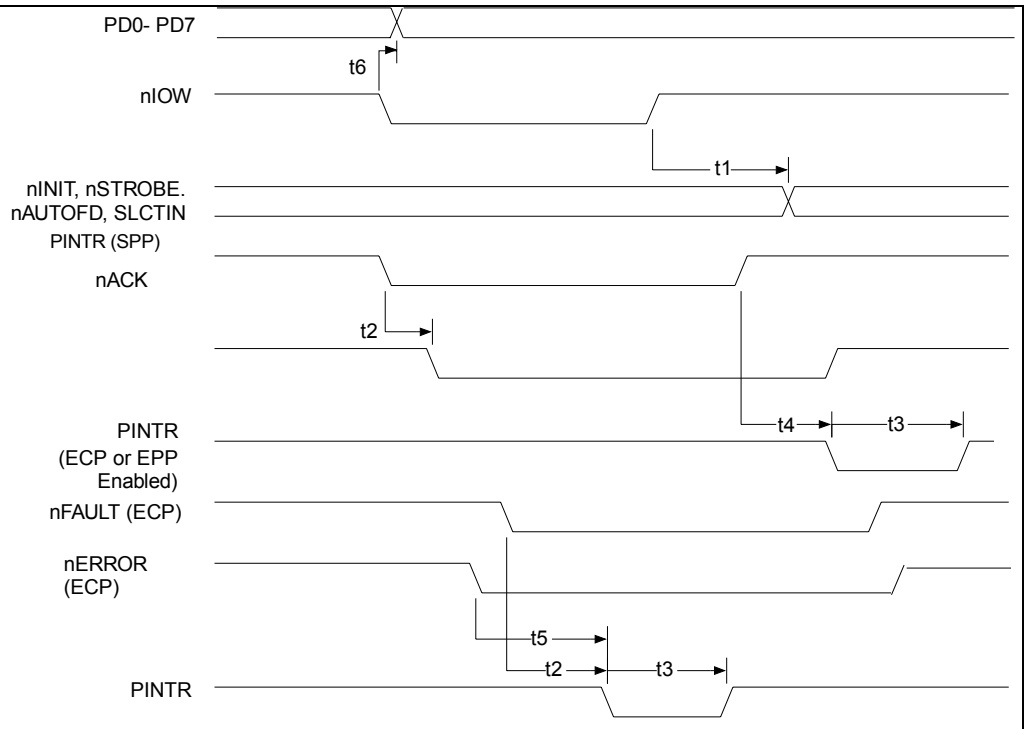
9.2 Serial Port Timing



	Parameter	min	typ	max	units
t1	nRTSx, nDTRx Delay from nIOW			200	ns
t2	IRQx Active Delay from nCTSx, nDSRx, nDCDx			100	ns
t3	IRQx Inactive Delay from nIOR (Leading Edge)			120	ns
t4	IRQx Inactive Delay from nIOW (Trailing Edge)			125	ns
t5	IRQx Inactive Delay from nIOW	10		100	ns
t6	IRQx Active Delay from nRIx			100	ns

FIGURE 7 - SERIAL PORT TIMING

9.3 Parallel Port Timing

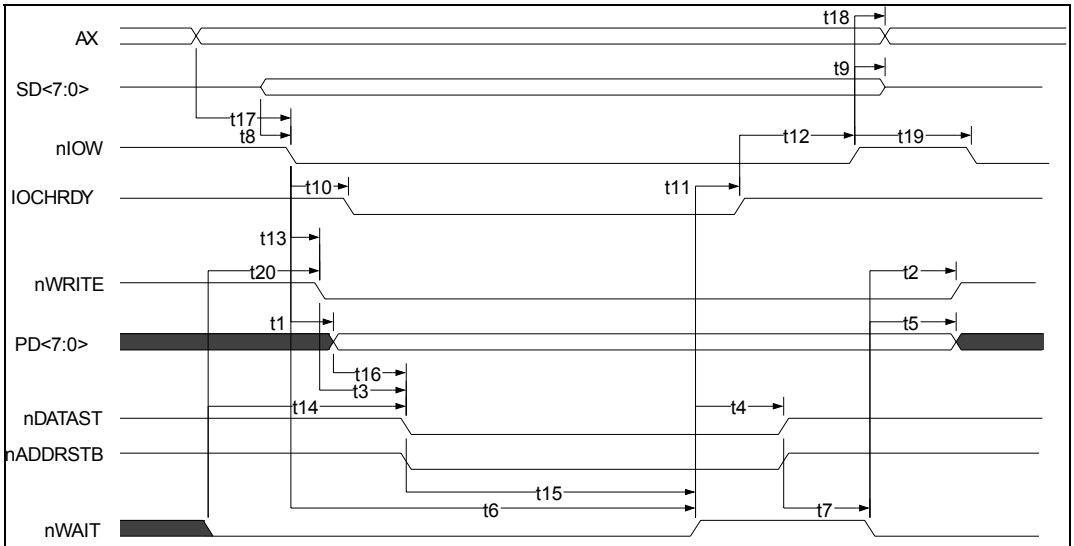


	Parameter	min	typ	max	units
t1	nINIT, nSTROBE, nAUTOFD Delay from nIOW Inactive			100	ns
t2	PINTR Delay from nACK, nFAULT			60	ns
t3	PINTR Active Low in ECP and EPP Modes	200		300	ns
t4	PINTR Delay from nACK			105	ns
t5	nERROR Active to PINTR Active			105	ns
t6	PD0-PD7 Delay from nIOW Active			100	ns

PINTR is the interrupt assigned to the Parallel Port

FIGURE 8 - PARALLEL PORT TIMING

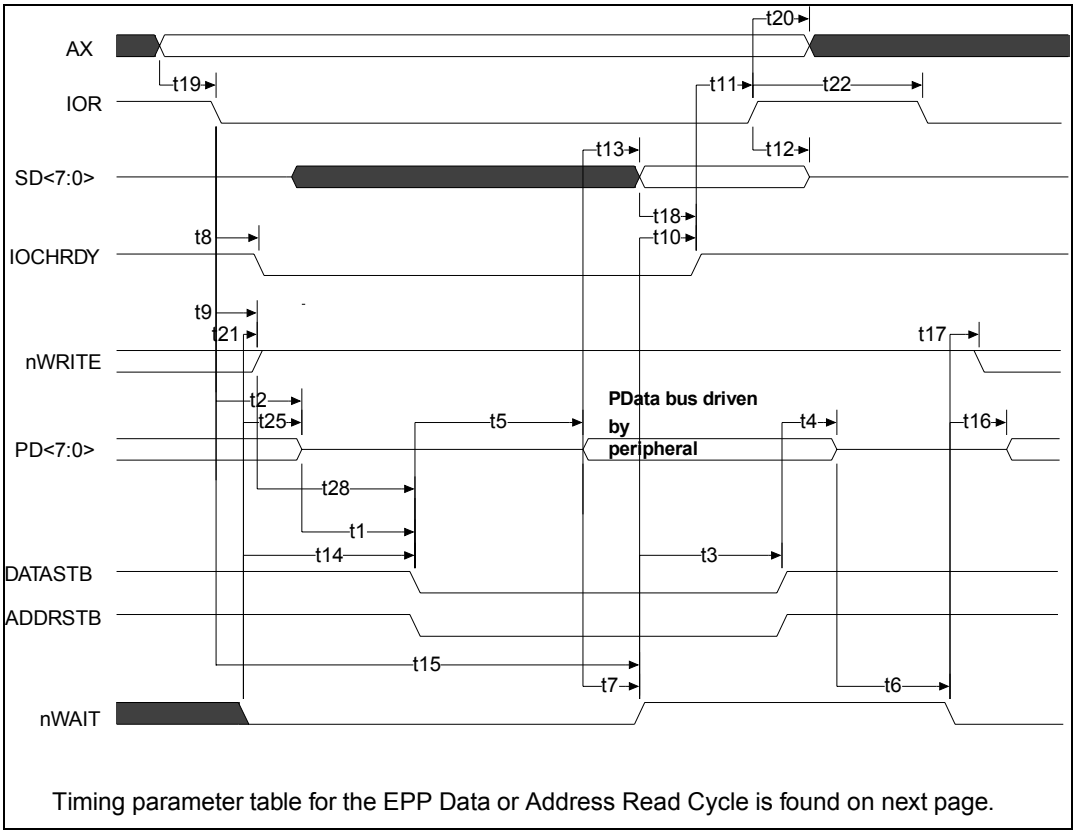
9.3.1 PARALLEL PORT EPP TIMING



	Parameter	min	max	units	Notes
t1	nIOW Asserted to PDATA Valid	0	50	ns	
t2	nWAIT Asserted to nWRITE Change	60	185	ns	1
t3	nWRITE to Command Asserted	5	35	ns	
t4	nWAIT Deasserted to Command Deasserted	60	190	ns	1
t5	nWAIT Asserted to PDATA Invalid	0		ns	1
t6	Time Out	10	12	µs	
t7	Command Deasserted to nWAIT Asserted	0		ns	
t8	SDATA Valid to IOW Asserted	10		ns	
t9	nIOW Deasserted to DATA Invalid	0		ns	
t10	nIOW Asserted to IOCHRDY Asserted	0	24	ns	
t11	WAIT Deasserted to nIOCHRDY Deasserted	60	160	ns	1
t12	IOCHRDY Deasserted to nIOW Deasserted	10		ns	
t13	nIOW Asserted to nWRITE Asserted	0	70	ns	
t14	nWAIT Asserted to Command Asserted	60	210	ns	1
t15	Command Asserted to nWAIT Deasserted	0	10	µs	
t16	PDATA Valid to Command Asserted	10		ns	
t17	Ax Valid to nIOW Asserted	40		ns	
t18	nIOW Deasserted to Ax Invalid	10		ns	
t19	nIOW Deasserted to nIOW or nIOR Asserted	40		ns	
t20	nWAIT Asserted to nWRITE Asserted	60	185	ns	1

NOTE: WAIT must be filtered to compensate for ringing on the parallel bus cable. WAIT is considered to have settled after it does not transition for a minimum of 50 nsec.

FIGURE 9 - EPP 1.9 DATA OR ADDRESS WRITE CYCLE



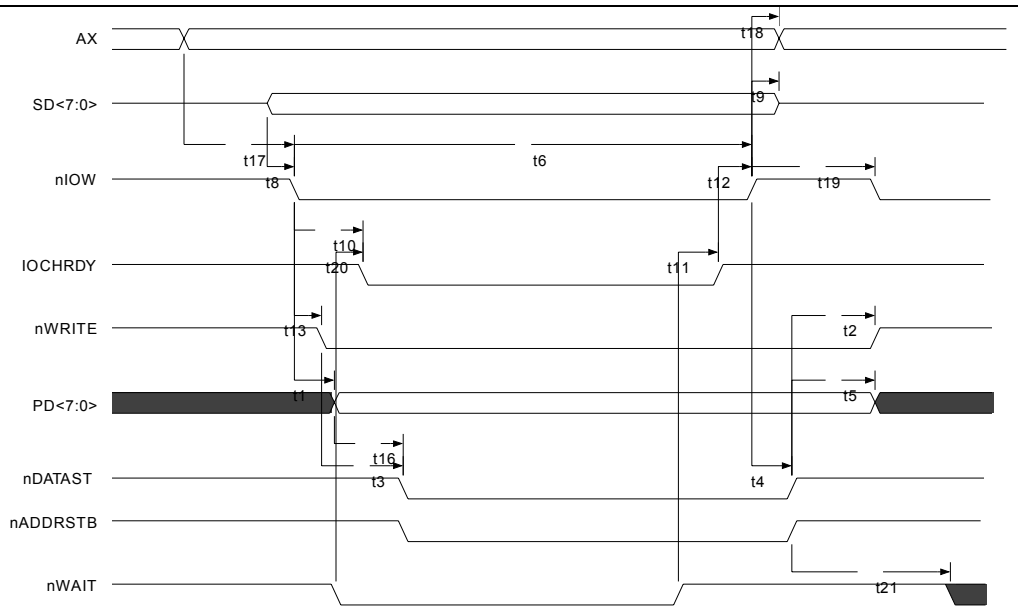
Timing parameter table for the EPP Data or Address Read Cycle is found on next page.

FIGURE 10 - EPP 1.9 DATA OR ADDRESS READ CYCLE

	Parameter	min	max	units	Notes
t1	PDATA Hi-Z to Command Asserted	0	30	ns	
t2	nIOR Asserted to PDATA Hi-Z	0	50	ns	
t3	nWAIT Deasserted to Command Deasserted	60	180	ns	1
t4	Command Deasserted to PDATA Hi-Z	0		ns	
t5	Command Asserted to PDATA Valid	0		ns	
t6	PDATA Hi-Z to nWAIT Deasserted	0		µs	
t7	PDATA Valid to nWAIT Deasserted	0		ns	
t8	nIOR Assertd to IOCHRDY Asserted	0	24	ns	
t9	nWRITE Deasserted to nIOR Asserted	0		ns	2
t10	nWAIT Deasserted to IOCHRDY Deasserted	60	160	ns	1
t11	IOCHRDY Deasserted to nIOR Deasserted	0		ns	
t12	nIOR Deasserted to SDATA Hi-Z (Hold Time)	0	40	ns	
t13	PDATA Valid to SDATA Valid	0	75	ns	
t14	nWAIT Asserted to Command Asserted	0	195	ns	
t15	Time Out	10	12	µs	
t16	nWAIT Deasserted to PDATA Driven	60	190	ns	1
t17	nWAIT Deasserted to nWRITE Modified	60	190	ns	1,2
t18	SDATA Valid to IOCHRDY Deasserted	0	85	ns	3
t19	Ax Valid to nIOR Asserted	40		ns	
t20	nIOR Deasserted to Ax Invalid	10	10	ns	
t21	nWAIT Asserted to nWRITE Deasserted	0	185	ns	
t22	nIOR Deasserted to nIOW or nIOR Asserted	40		ns	
t25		60	180	ns	1
t28	nWAIT Asserted to PDATA Hi-Z WRITE Deasserted to Command	1		ns	

NOTES:
1. n WAIT is considered to have settled after it does not transition for a minimum of 50 ns.
2. When not executing a write cycle, EPP nWRITE is inactive high.
3. 85 is true only if t7 = 0.

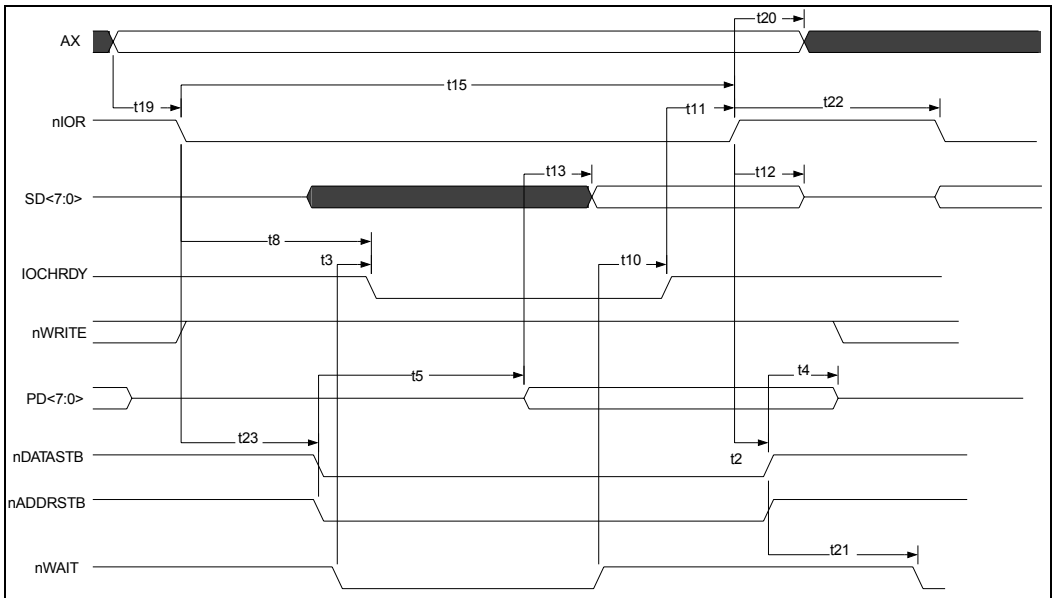
FIGURE 11 - EPP 1.9 DATA OR ADDRESS READ CYCLE TIMING PARAMETERS



	Parameter	min	max	units	Notes
t1	nIOW Asserted to PDATA Valid	0	50	ns	
t2	Command Dessserted to nWRITE Change	0	40	ns	
t3	nWRITE to Command	5	35	ns	
t4	nIOW Deasserted to Command Deasserted		50	ns	2
t5	Command Deasserted to PDATA Invalid	50		ns	
t6	Time Out	10	12	µs	
t8	SDATA Valid to nIOW Asserted	10		ns	
t9	nIOW Deasserted to DATA Invalid	0		ns	
t10	nIOW Asserted to IOCHRDY Asserted	0	24	ns	
t11	nWAIT Deasserted to IOCHRDY Deasserted		40	ns	
t12	IOCHRDY Deasserted to nIOW Deasserted	10		ns	
t13	nIOW Asserted to nWRITE Asserted	0	50	ns	
t16	PDATA Valid to Command Asserted	10	35	ns	
t17	Ax Valid to nIOW Asserted	40		ns	
t18	nIOW Deasserted to Ax Invalid	10		µs	
t19	nIOW Deasserted to nIOW or nIOR Asserted	100		ns	
t20	nWAIT Asserted to IOCHRDY Deasserted		45	ns	
t21	Command Deasserted to nWAIT Deasserted	0		ns	

NOTES:
1. WRITE is controlled by clearing the PDIR bit to "0" in the control register before performing an EPP Write.
2. This number is only valid if WAIT is active when nIOW goes active.

FIGURE 12 - EPP 1.7 DATA OR ADDRESS WRITE CYCLE



	Parameter	min	max	units	Notes
t2	nIOR Deasserted to Command Deasserted		50	ns	
t3	nWAIT Asserted to IOCHRDY Deasserted	0	40	ns	
t4	Command Deasserted to PDATA Hi-Z	0		ns	
t5	Command Asserted to PDATA Valid	0		ns	
t8	nIOR Asserted to IOCHRDY Asserted		24	ns	
t10	nWAIT Deasserted to nIOCHRDY Deasserted		50	ns	
t11	nIOCHRDY Deasserted to nIOR Deasserted	0		ns	
t12	nIOR Deasserted to SDATA High-Z (Hold Time)	0	40	ns	
t13	PData Valid to SDATA Valid		40	ns	
t15	Time Out	10	12	µs	
t19	Ax Valid to nIOR Asserted	40		ns	
t20	nIOR Deasserted to Ax Invalid	10		ns	
t21	Command Deasserted to nWAIT Deasserted	0		ns	
t22	nIOR Deasserted to nIOW or nIOR Asserted	40		ns	
t23	nIOR Asserted to Command Asserted		55	ns	

NOTE:

1. nWRITE is controlled by setting the PDIR bit to "1" in the control register before performing an EPP Read.

FIGURE 13 - EPP 1.7 DATA OR ADDRESS READ CYCLE

9.3.2 PARALLEL PORT ECP TIMING

9.3.2.1 Parallel Port FIFO (Mode 101)

The standard parallel port is run at or near the peak 500 Kbps allowed in the forward direction using DMA. The state machine does not examine nAck and begins the next transfer based on Busy. Refer to FIGURE 14.

9.3.2.2 ECP Parallel Port Timing

The timing is designed to allow operation at approximately 2.0Mbytes/sec over a 15ft cable. If a shorter cable is used then the bandwidth will increase.

9.3.2.3 Forward-Idle

When the host has no data to send it keeps HostClk (nStrobe) high and the peripheral will leave PeriphClk (Busy) low.

9.3.2.4 Forward Data Transfer Phase

The interface transfers data and commands from the host to the peripheral using an interlocked PeriphAck and HostClk. The peripheral may indicate its desire to send data to the host by asserting nPeriph Request.

The Forward Data Transfer Phase may be entered from the Forward-Idle Phase. While in the Forward Phase the peripheral may asynchronously assert the nPeriph Request (nFault) to request that the channel be reversed. When the peripheral is not busy it sets PeriphAck (Busy) low. The host then sets HostClk (nStrobe) low when it is prepared to send data. The data must be stable for the specified setup time prior to the falling edge of HostClk. The peripheral then sets PeriphAck (Busy) high to acknowledge the handshake. The host then sets HostClk (nStrobe) high. The peripheral then accepts the data and sets PeriphAck (Busy) low, completing the transfer. This sequence is shown in FIGURE 15.

The timing is designed to provide 3 cable round-trip times for data setup if Data is driven simultaneously with HostClk (nStrobe).

9.3.2.5 Reverse-Idle Phase

The peripheral has no data to send and keeps PeriphClk high. The host is idle and keeps HostAck low.

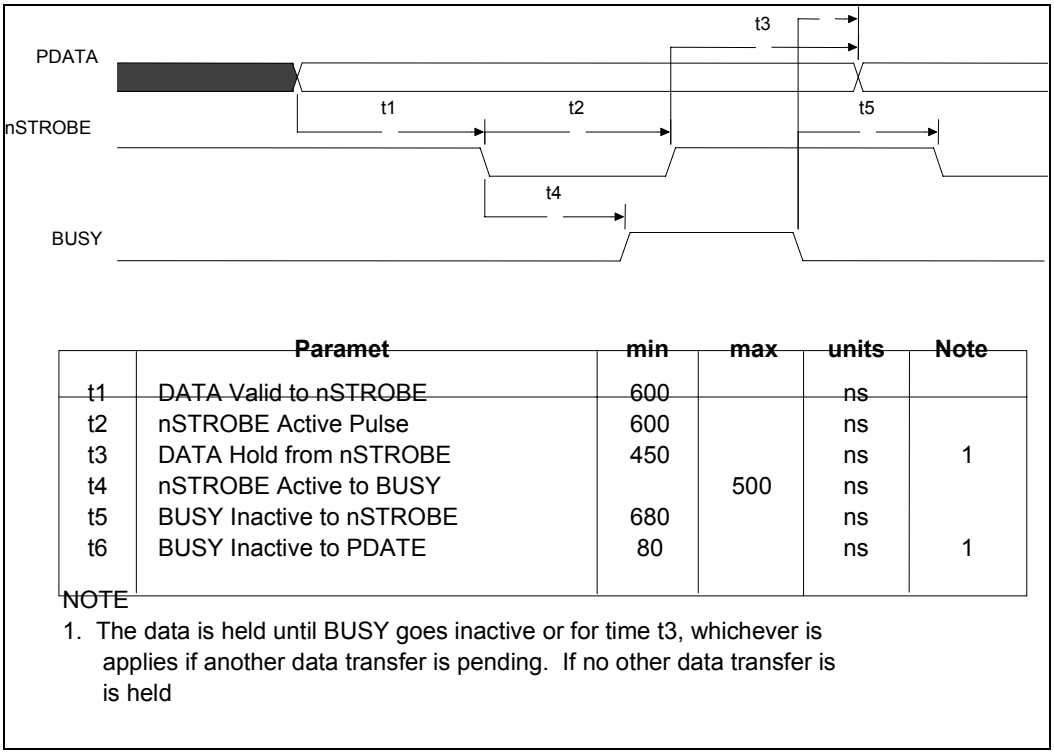
9.3.2.6 Reverse Data Transfer Phase

The interface transfers data and commands from the peripheral to the host using an interlocked HostAck and PeriphClk.

The Reverse Data Transfer Phase may be entered from the Reverse-Idle Phase. After the previous byte has beed accepted the host sets HostAck (nAutoFd) low. The peripheral then sets PeriphClk (nAck) low when it has data to send. The data must be stable for the specified setup time prior to the falling edge of PeriphClk. When the host is ready it to accept a byte it sets. HostAck (nAutoFd) high to acknowledge the handshake. The peripheral then sets PeriphClk (nAck) high. After the host has accepted the data it sets HostAck (nAutoFd) low, completing the transfer. This sequence is shown in FIGURE 16.

9.3.2.7 Output Drivers

To facilitate higher performance data transfer, the use of balanced CMOS active drivers for critical signals (Data, HostAck, HostClk, PeriphAck, PeriphClk) are used ECP Mode. Because the use of active drivers can present compatibility problems in Compatible Mode (the control signals, by tradition, are specified as open-collector), the drivers are dynamically changed from open-collector to totem-pole. The timing for the dynamic driverchange is specified in the IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.14, July. 14, 1993, available from Microsoft. The dynamic driver change must be implemented properly to prevent glitching the outputs.

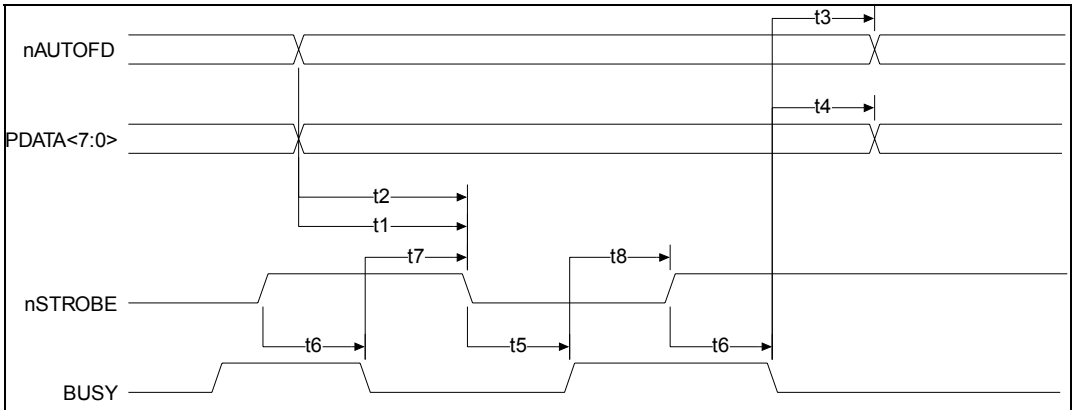


	Paramet	min	max	units	Note
t1	DATA Valid to nSTROBE	600		ns	
t2	nSTROBE Active Pulse	600		ns	
t3	DATA Hold from nSTROBE	450		ns	1
t4	nSTROBE Active to BUSY		500	ns	
t5	BUSY Inactive to nSTROBE	680		ns	
t6	BUSY Inactive to PDATE	80		ns	1

NOTE

1. The data is held until BUSY goes inactive or for time t3, whichever is applies if another data transfer is pending. If no other data transfer is is held

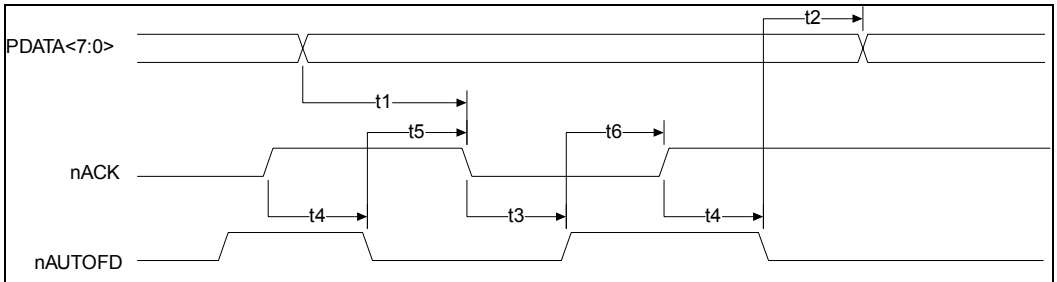
FIGURE 14 - PARALLEL PORT FIFO TIMING



	Parameter	min	max	units	Notes
t1	nAUTOFD Valid to nSTROBE Asserted	0	60	ns	
t2	PDATA Valid to nSTROBE Asserted	0	60	ns	
t3	BUSY Deasserted to nAUTOFD Changed	80	180	ns	1,2
t4	nBUSY Deasserted to PDATA Changed	80	180	ns	1,2
t5	nSTROBE Asserted to BUSY Asserted	0		ns	
t6	nSTROBE Deasserted to Busy Deasserted	0		ns	
t7	nBUSY Deasserted to nSTROBE Asserted	80	200	ns	1,2
t8	nBUSY Asserted to nSTROBE Deasserted	80	180	ns	2

NOTES:
1. Maximum value only applies if there is data in the FIFO waiting to be written out.
2. BUSY is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

FIGURE 15 - ECP PARALLEL PORT FORWARD TIMING

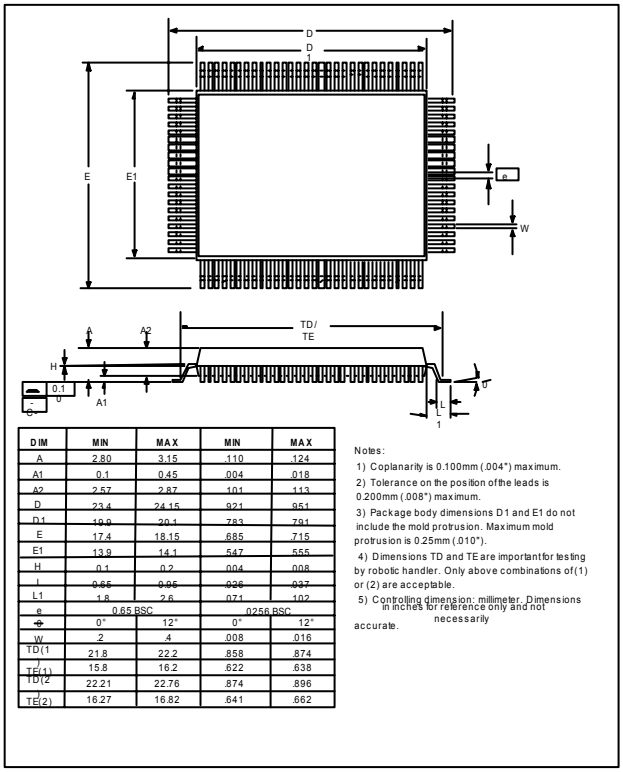


	Parameter	min	max	units	Notes
t1	PDATA Valid to nACK Asserted	0		ns	
t2	nAUTOFD Deasserted to PDATA Changed	0		ns	
t3	nACK Asserted to nAUTOFD Deasserted	80	200	ns	1,2
t4	nACK Deasserted to nAUTOFD Asserted	80	200	ns	2
t5	nAUTOFD Asserted to nACK Asserted	0		ns	
t6	nAUTOFD Deasserted to nACK Deasserted	0		ns	

NOTES:
1. Maximum value only applies if there is room in the FIFO and a terminal count has not been received. ECP can stall by keeping nAUTOFD low.
2. nACK is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

FIGURE 16 - ECP PARALLEL PORT REVERSE TIMING

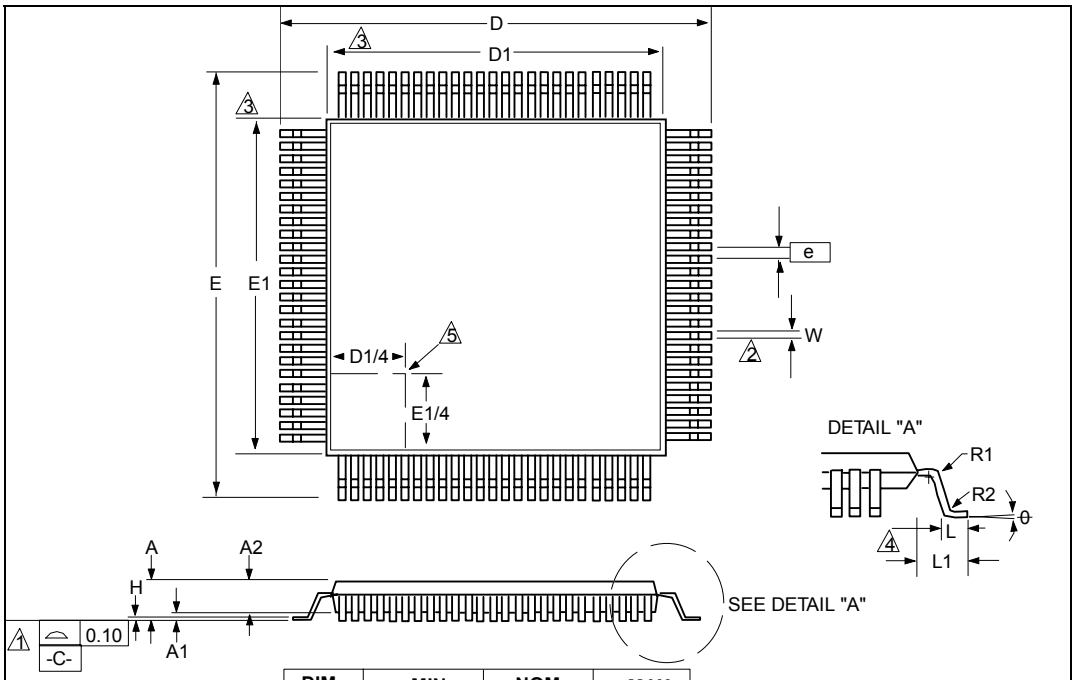
10 PACKAGE OUTLINES



DIM	MIN	MAX	MIN	MAX
A	2.80	3.15	.110	.124
A1	0.1	0.45	.004	.018
A2	2.57	2.87	.101	.113
D	23.4	24.15	.921	.951
D1	19.9	20.1	.783	.791
E	17.4	18.15	.685	.715
E1	13.9	14.1	.547	.555
H	0.1	0.2	.004	.008
L	0.65	0.95	.026	.037
L1	1.8	2.6	.071	.102
e	0.65 BSC		.0256 BSC	
θ	0°	12°	0°	12°
W	.2	.4	.008	.016
TD(1)	21.8	22.2	.858	.874
TE(1)	15.8	16.2	.622	.638
TD(2)	22.21	22.76	.874	.896
TE(2)	16.27	16.82	.641	.662

Notes:
1) Coplanarity is 0.100mm (.004") maximum.
2) Tolerance on the position of the leads is 0.200mm (.008") maximum.
3) Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25mm (.010").
4) Dimensions TD and TE are important for testing by robotic handler. Only above combinations of (1) or (2) are acceptable.
5) Controlling dimension: millimeter. Dimensions in inches for reference only and not necessarily accurate.

FIGURE 17 – 100 PIN QFP



DIM	MIN	NOM	MAX
A			1.6
A1	0.05		
A2	1.35	1.40	1.45
D	15.75	16.00	16.25
D1	13.90	14.00	14.10
E	15.75	16.00	16.25
E1	13.90	14.00	14.10
H			0.20
L	0.45	0.60	0.75
L1		1.00	
e		0.50 BSC	
θ	0°		8°
W		0.25	
R1		0.20	
R2		0.20	

Notes:
1. Coplanarity is 0.100mm maximum.
2. Tolerance on the position of the leads is 0.13mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25mm per side.
4. Dimension for foot length L are measured at the gauge plane 0.25mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.
6. Controlling dimension: millimeter

FIGURE 18 – 100 PIN TQFP

11 SP37E760 REVISIONS

PAGE(S)	SECTION/FIGURE/ENTRY	CORRECTION	DATE REVISED
1	Title	3.3V Super I/O Controller for Embedded Applications changed to: 3.3V I/O Controller for Embedded Applications	04/13/01