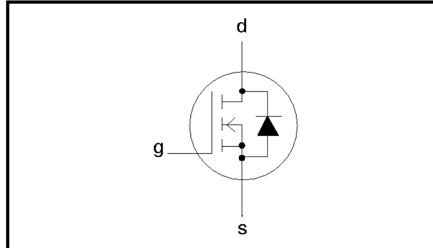
N-channel TrenchMOS™ transistor PSMN009-100W

FEATURES

- **'Trench'** technology
- Very low on-state resistance
- Fast switching
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 100 V

I_D = 100 A

$R_{DS(ON)} \leq 9\ m\Omega$

GENERAL DESCRIPTION

SiliconMAX products use the latest Philips Trench technology to achieve the lowest possible on-state resistance in each package at each voltage rating.

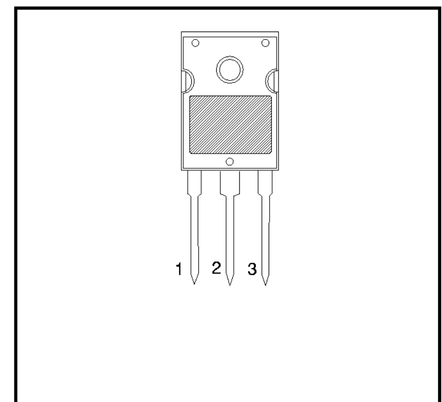
Applications:-
- d.c. to d.c. converters
- switched mode power supplies

The PSMN009-100W is supplied in the SOT429 (TO247) conventional leaded package.

PINNING

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

SOT429 (TO247)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 ˚C to 175˚C	-	100	V
V_{DGR}	Drain-gate voltage	T_j = 25 ˚C to 175˚C; R_{GS} = 20 kΩ	-	100	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	T_{mb} = 25 ˚C	-	100[1]	A
		T_{mb} = 100 ˚C	-	79	A
I_{DM}	Pulsed drain current	T_{mb} = 25 ˚C	-	300	A
P_D	Total power dissipation	T_{mb} = 25 ˚C	-	300	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	˚C

1 Maximum continuous current limited by package.

AVALANCHE ENERGY LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
E_{AS}	Non-repetitive avalanche energy	Unclamped inductive load, I_{AS} = 100 A; t_p = 100 µs; T_j prior to avalanche = 25˚C; V_{DD} ≤ 50 V; R_{GS} = 50 Ω; V_{GS} = 5 V; refer to fig:15	-	650	mJ
I_{AS}	Non-repetitive avalanche current		-	100	A

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	0.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	45	-	K/W

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	100	-	-	V
		T_j = -55˚C	89	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175˚C	1.0	-	-	V
		T_j = -55˚C	-	-	6	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	6.7	9	mΩ
		T_j = 175˚C	-	15	25	mΩ
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	2	100	nA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 100 A; V_{DD} = 80 V; V_{GS} = 10 V	-	214	-	nC
Q_{gs}	Gate-source charge		-	45	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	91	-	nC
$t_{d\ on}$	Turn-on delay time	V_{DD} = 50 V; R_D = 2 Ω;	-	40	-	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 5.6 Ω	-	100	-	ns
$t_{d\ off}$	Turn-off delay time	Resistive load	-	260	-	ns
t_f	Turn-off fall time		-	100	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	9000	-	pF
C_{oss}	Output capacitance		-	1000	-	pF
C_{rss}	Feedback capacitance		-	650	-	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	100	A
I_{SM}	Pulsed source current (body diode)		-	-	300	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.82	1.2	V
		I_F = 75 A; V_{GS} = 0 V	-	0.95	-	V
t_{rr}	Reverse recovery time	I_F = 20 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = 0 V; V_R = 30 V	-	0.5	-	µC

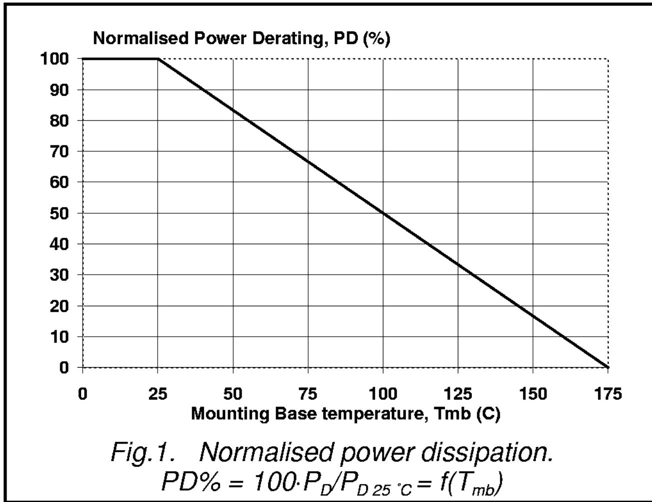


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D/P_{D\ 25\ ^\circ C} = f(T_{mb})$

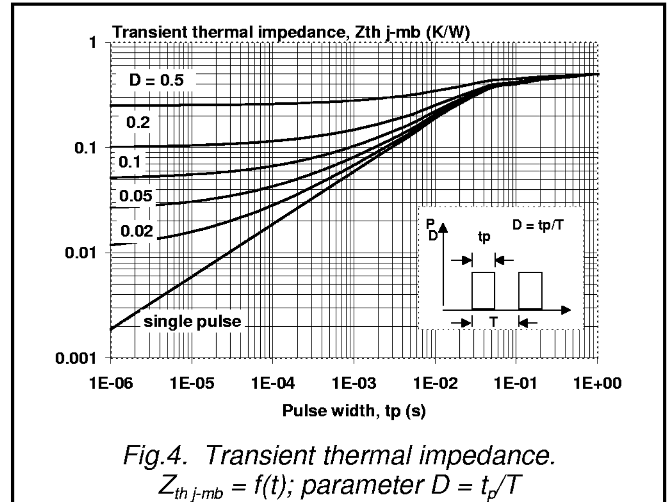


Fig.4. Transient thermal impedance.
$Z_{th\ j-mb} = f(t)$; parameter $D = t_p/T$

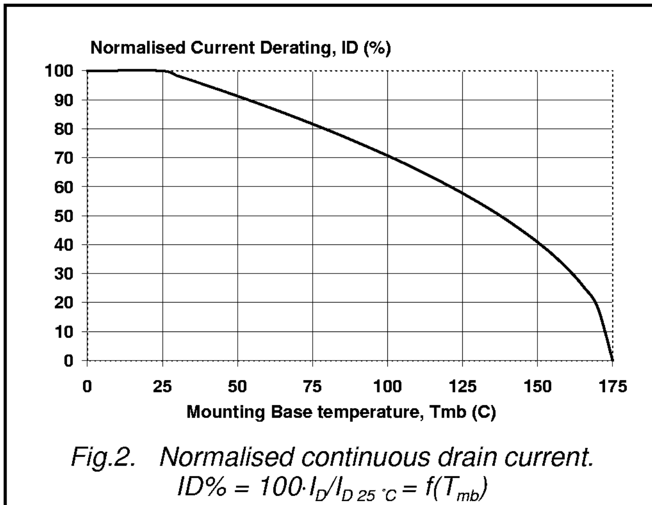


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D/I_{D\ 25\ ^\circ C} = f(T_{mb})$

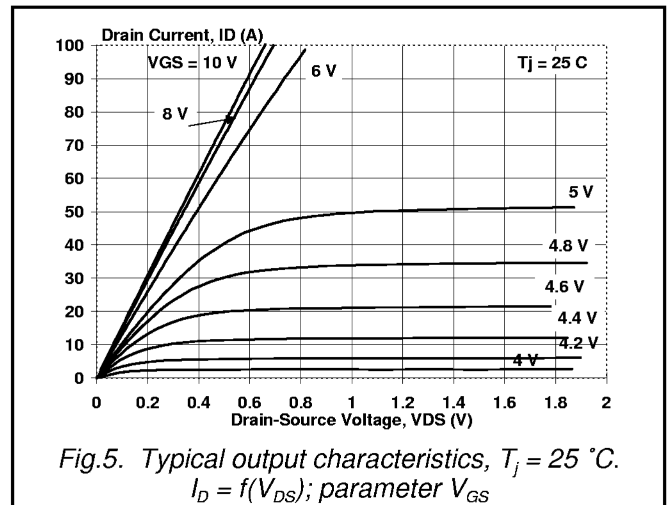


Fig.5. Typical output characteristics, $T_j = 25\ ^\circ C$.
$I_D = f(V_{DS})$; parameter V_{GS}

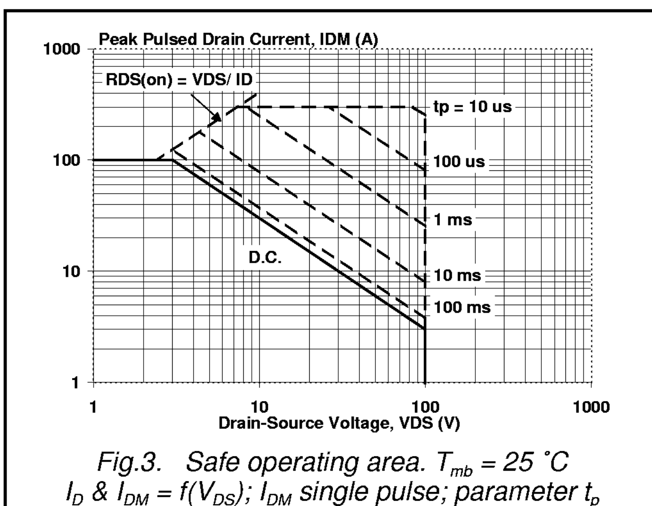


Fig.3. Safe operating area. $T_{mb} = 25\ ^\circ C$
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

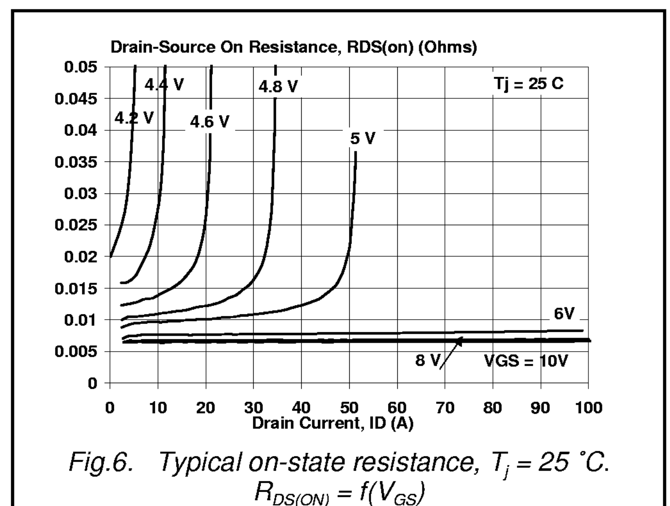


Fig.6. Typical on-state resistance, $T_j = 25\ ^\circ C$.
$R_{DS(ON)} = f(V_{GS})$

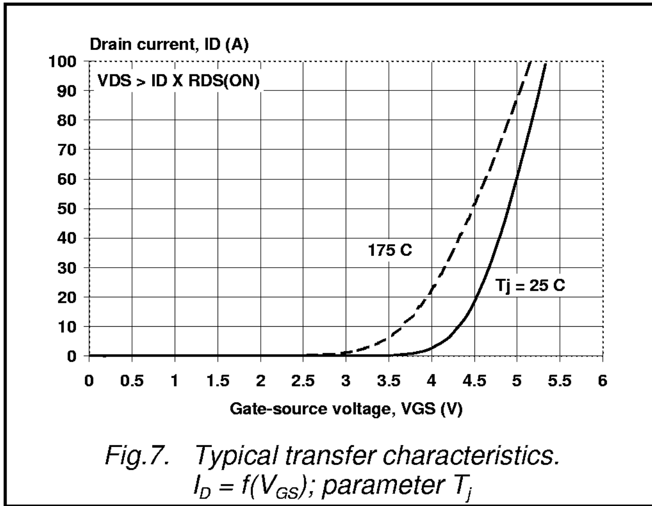


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

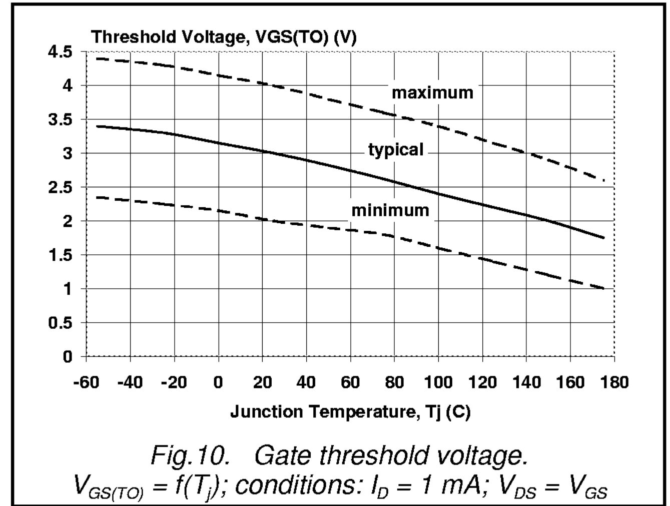


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

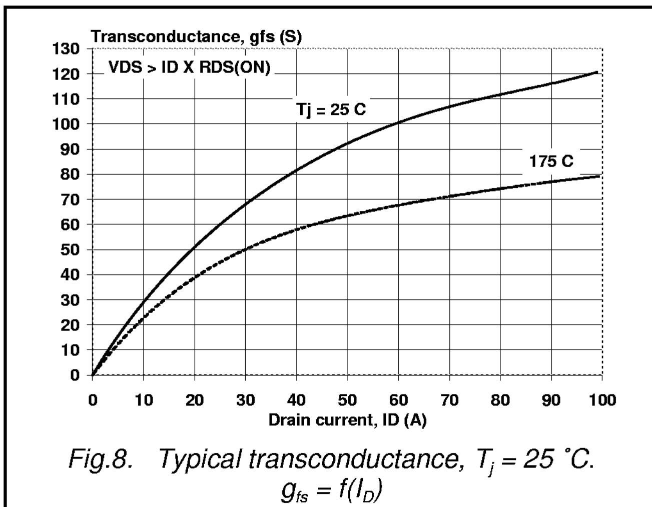


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$

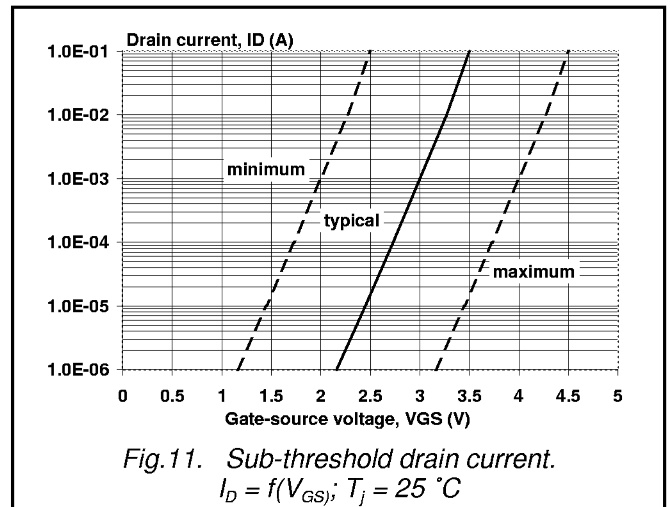


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; T_j = 25 ˚C

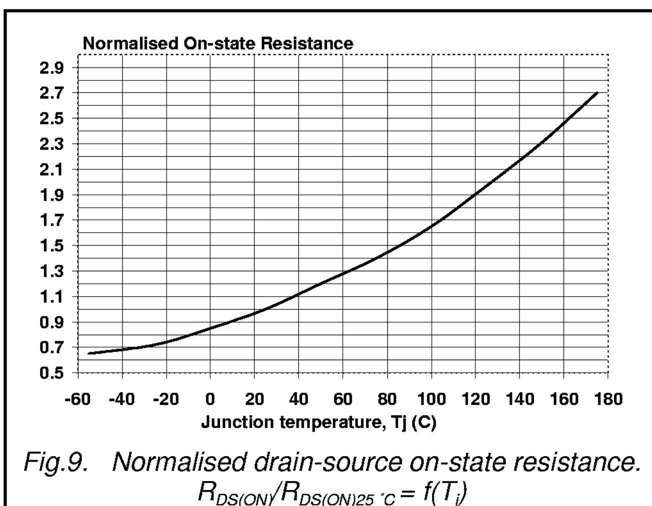


Fig.9. Normalised drain-source on-state resistance.
$R_{DS(ON)}/R_{DS(ON)25\,˚C} = f(T_j)$

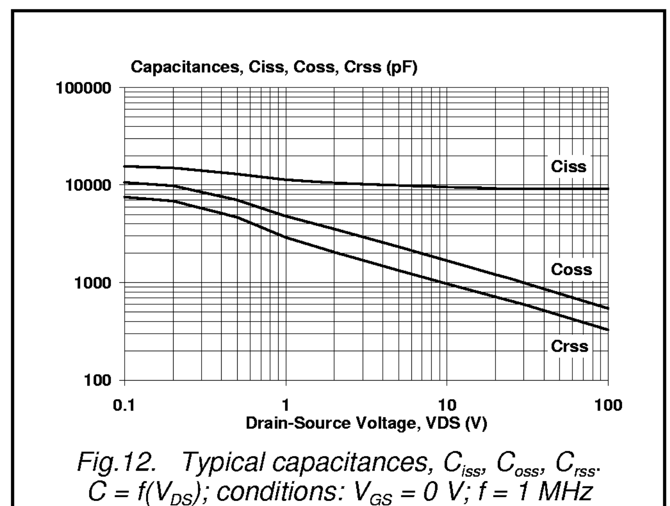


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

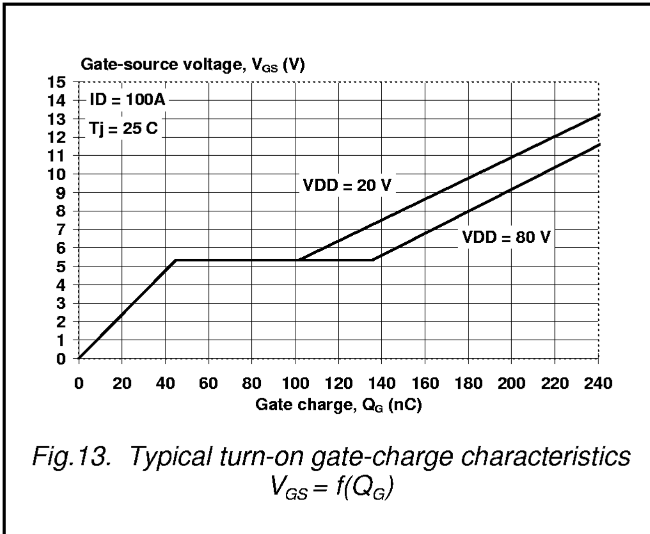


Fig.13. Typical turn-on gate-charge characteristics $V_{GS} = f(Q_G)$

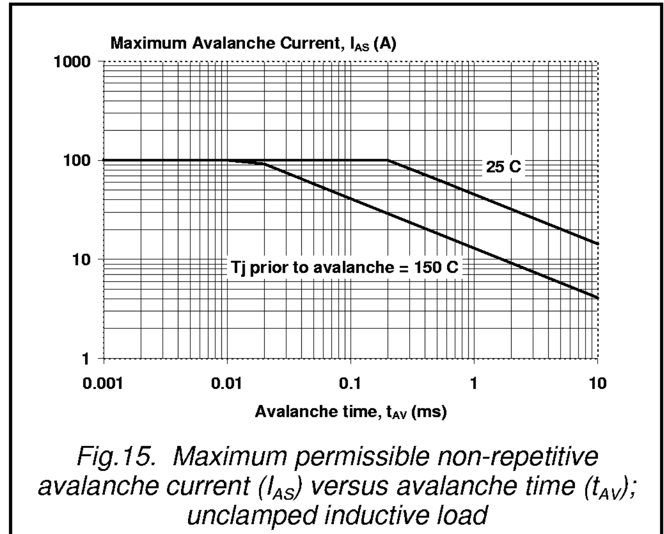


Fig.15. Maximum permissible non-repetitive avalanche current (I_{AS}) versus avalanche time (t_{AV}); unclamped inductive load

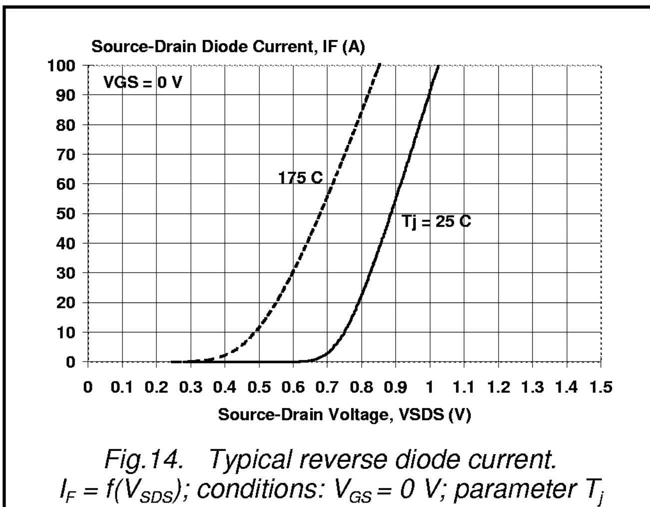


Fig.14. Typical reverse diode current. $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

MECHANICAL DATA

Plastic single-ended through-hole package; heatsink mounted; 1 mounting hole; 3-lead TO-247 **SOT429**

DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	E	e	L	L_1 (1)	P	Q	q	R	S	w	Y	α	β
mm	5.3 4.7	1.9 1.7	1.2 0.9	2.2 1.8	3.2 2.8	0.9 0.6	21 20	16 15	5.45	16 15	4.0 3.6	3.7 3.3	2.6 2.4	5.3	3.5 3.3	7.5 7.1	0.4	15.7 15.3	6° 4°	17° 13°

Note

1. Tinning of terminals are uncontrolled within zone L_1.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT429		TO-247				~~98-04-07~~ 99-08-04

Fig.16. SOT429; pin 2 connected to mounting base

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT429 envelope.
3. Epoxy meets UL94 V0 at 1/8".