PM5357

S/UNI-622-POS

SATURN USER NETWORK INTERFACE (622- POS)

S/UNI-® 622-POS

DATASHEET

ISSUE 5: JUNE 2000

REVISION HISTORY

ISSUE	DATE	DETAIL
5	June 2000	Repositioned Path Trace Buffer block to connect to Tx and Rx path overhead processor. Revised Receive FIFO. Section 10.7 Receive POS Frame Processor (RXFP) Moved Overhead Byte Receive section from Section 10.15 SONET/SDH Section Trade Buffer (SSTB) to 10.14 SONET/SDH Path Trace Buffer (SPTB). Corrected function name errors in Register 0x03: S/UNI-622 POS Clock Monitors. Changed PTCLKI to PTCLK, REFCLKI to REFCLK, RFCLKI to RFCLK, RCLKI to RCLK and TCLKI to TCLK. Added line loopback operation information to RXDINV and TXDINV in Register 0x07: S/UNI-622-POS Miscellaneous Configuration. Rewrote IINVCNT bit functionality for clarity. Register 0x30 (EXTD=1): RPOP Status/Control. Rewrote DOOLI bit functionality to indicate change to DOOLV bit and CRU out of lock conditions in Register 0.5C: CRSI Configuration. Rewrote DOOLE bit funcitonality to indicate change to DOOLV register events in Register 0x5D: CRSI Status. Corrected bit 1 function name in Register 0xD1: WANS Interrupt and Status. Was PHWVALID. Now RPHALGN.

ISSUE	DATE	DETAIL
4	Dec, 1999	#1. Modified section 9.5 (UTOPIA and POS-PHY pin description) and section 14.4 (Functional timing) to reflect operation of the RPA signal (Receive POS-PHY L2 operation requires data be qualified by RVAL). #2 DC characteristics update (Section 16) #3 Registers updated with correct defaults and descriptions: Register 0X01, Bit 4 (TFPEN), Defaults To 1, Not 0 Register 0X08, Description Incorrect Register 0X09 Description Incorrect Register 0XC1, Bit 1 (DSCR), Defaults To 1, Not 0 Register 0XC4, Bit 3 (TPAHWM), Defaults To 0, Not 1 New Register 0XFC: Concatenation Status And Enable New Register 0XFD: Concatenation Interrupt Status New Register Bit Required For OC-3 Operation (Register 0X07) Register 0X5E Bit 5 (RTYPE) To Enable LAN Or WAN Performance Register 0X00 Type Bits Incorrect Loss Of Multi-frame Tributary AIS (LOMTUAIS) Bit 2 Incorrectly Stated In Register 0X0D #4 APS pin description modified #5 Documented overflowing Transmit FIFO #6 Updated TFCLK timing specifications, RFCLK timing specifications #7 Diagnostic Loop-back Clarification #8 Bit Error Rate Monitor Table Update #9 Receive Data Requires 3 RFCLK Cycles Before Becoming Valid (Utopia Level 3 Only) #10 TPAHWM Upper Limit #11 Receive Line AIS Insertion Is Not Gated By ALLONES #12 Large Power Supply Glitch (Beyond Specification) Can Cause Clock Synthesis Unit To Lose Lock To Reference.

ISSUE	DATE	DETAIL
3	Jan 13, 1999	Corrected wrong pin number assignments in pin description.
2	Dec 12, 1998	General update in preparation for Issue 2 S/UNI-622-POS
1	Mar 30, 1998	Updated datasheet

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1 FEATURES

1.1 General

- Single chip ATM and Packet over SONET/SDH Physical Layer Device operating at 622.08 Mbit/s.
- Implements the ATM Forum User Network Interface Specification and the ATM physical layer for Broadband ISDN according to CCITT Recommendation I.432.
- Implements the Point-to-Point Protocol (PPP) over SONET/SDH specification according to RFC 2615.
- Processes duplex bit-serial 622.08 Mbit/s STS-12c/STM-4-4c data streams with on-chip clock and data recovery and clock synthesis.
- Supports a duplex byte-serial 77.76 Mbyte/s STS-12c/STM-4-4c line side interface for use in applications where by-passing clock recovery, clock synthesis, and serializer-deserializer functionality is desired.
- Supports a byte-serial 19.44 Mbyte/s STS-3c/STM-1 line side interface on the transmit and/or receive interface for use in applications where a 155.52 Mbit/s data rate is desired.
- Supports clock recovery by-pass for use in applications where external clock recovery is desired.
- Complies with Bellcore GR-253-CORE (1995 Issues) jitter tolerance, jitter transfer and intrinsic jitter criteria.
- Provides control circuitry required to comply with Bellcore GR-253-CORE WAN clocking requirements related to wander transfer, holdover and long term stability when using an external VCXO.
- Provides UTOPIA Level 2 16-bit wide System Interface (clocked up to 50 MHz) with parity support for ATM applications.
- Provides UTOPIA Level 3 compatible 8-bit wide System Interface (clocked up to 100 MHz) with parity support for ATM applications.
- Provides SATURN POS-PHY Level 2 16-bit System Interface (clocked up to 50 MHz) for Packet over SONET/SDH (POS) applications. This system interface is similar to UTOPIA Level 2, but adapted to packet transfer.

- Provides SATURN POS-PHY Level 3 8-bit System Interface (clocked up to 100 MHz) for Packet over SONET/SDH (POS) applications.
- Provides support functions for a two chip solution for 1+1 APS operation.
- Provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 3.3V CMOS with TTL compatible digital inputs and CMOS/TTL digital outputs. PECL inputs and outputs are 3.3V and 5V compatible.
- Industrial temperature range (-40°C to +85°C).
- 304 pin Super BGA package.

1.2 The SONET Receiver

- Provides a serial interface at 622.08 Mbit/s with clock and data recovery.
- Frames to and de-scrambles the received STS-12c/STM-4-4c stream.
- Optionally frames to and de-scrambles a received STS-3c/STM-1 stream.
- Interprets the received payload pointer (H1, H2) and extracts the STS-12c/STM-4-4c or STS-3c/STM-1 synchronous payload envelope and path overhead.
- Extracts the data communication channels (D1-D3, D4-D12) and serializes them at 192 kbit/s (D1-D3) and 576 kbit/s (D4-D12) for optional external processing.
- Filters and captures the automatic protection switch channel (APS) bytes in readable registers and detects APS byte failure.
- Captures and de-bounces the synchronization status (S1) nibble in a readable register.
- Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms based on received B2 errors.
- Extracts the 16-byte or 64-byte section trace (J0/Z0) sequence and the 16-byte or 64-byte path trace (J1) sequence into internal register banks.

- Detects loss of signal (LOS), out of frame (OOF), loss of frame (LOF), line alarm indication signal (AIS-L), line remote defect indication (RDI-L), loss of pointer (LOP), path alarm indication signal (AIS-P), path remote defect indication (RDI-P), path extended remote defect indicator (extended RDI-P).

- Counts received section BIP-8 (B1) errors, received line BIP-96 (B2) errors, line remote error indicates (REI-L), received path BIP-8 (B3) errors and path remote error indications (REI-P) for performance monitoring purposes.

1.3 The Receive ATM Processor

- Extracts ATM cells from the received STS-12c/STM-4-4c or STS-3c/STM-1 payload using ATM cell delineation.

- Provides ATM cell payload de-scrambling.

- Performs header check sequence (HCS) error detection and correction, and idle/unassigned cell filtering.

- Detects out of cell Delineation (OCD) and loss of cell delineation (LCD) alarms.

- Counts number of received cells, idle cells, errored cells and dropped cells.

- Provides a UTOPIA Level 2 compliant 16-bit wide datapath interface (clocked up to 50 MHz) with parity support to read extracted cells from an internal four-cell FIFO buffer.

- Provides a UTOPIA Level 3 compatible 8-bit wide datapath interface (clocked up to 100 MHz) with parity support to read extracted cells from an internal four-cell FIFO buffer.

1.4 The Receive POS Processor

- Supports packet based link layer protocols using byte synchronous HDLC framing like PPP, HDLC and Frame Relay.

- Performs self-synchronous POS data de-scrambling on the received STS-12c/STM-4-4c or STS-3c/STM-1 payload using the $x^{43}+1$ polynomial.

- Performs flag sequence detection and terminates the received POS frames.

- Performs frame check sequence (FCS) validation for CRC-CCITT and CRC-32 polynomials.

- Performs control escape de-stuffing of the HDLC stream.
- Detects for packet abort sequence.
- Checks for minimum and maximum packet lengths. Optionally deletes short packets and marks those exceeding the maximum length as errored.
- Provides a SATURN POS-PHY Level 2 compliant 16-bit datapath interface (clocked up to 50 MHz) with parity support to read packet data from an internal 256 byte FIFO buffer.
- Provides a SATURN POS-PHY Level 3 compliant 8-bit datapath interface (clocked up to 100 MHz) with parity support to read packet data from an internal 256 byte FIFO buffer.

1.5 The SONET Transmitter

- Synthesizes the 622.08 MHz transmit clock from a 77.76 MHz reference.
- Provides a differential PECL bit-serial interface at 622.08 Mbit/s.
- Inserts a register programmable path signal label (C2).
- Generates the transmit payload pointer (H1, H2) and inserts the path overhead.
- Optionally inserts the 16-byte or 64-byte section trace (J0/Z0) sequence and the 16-byte or 64-byte path trace (J1) sequence from internal register banks.
- Optionally inserts externally generated data communication channels (D1-D3, D4-D12) via a 192 kbit/s (D1-D3) serial stream and a 576 kbit/s (D4-D12) serial stream.
- Scrambles the transmitted STS-12c/STM-4-4c or STS-3c/STM-1 stream and inserts the framing bytes (A1, A2).
- Optionally inserts register programmable APS bytes.
- Provides a byte-serial transmit path data stream allowing two devices to implement 1+1 APS.
- Inserts path BIP-8 codes (B3), path remote error indications (REI-P), line BIP-96 codes (B2), line remote error indications (REI-L), and section BIP-8 codes (B1) to allow performance monitoring at the far end.

- Allows forced insertion of all-zeros data (after scrambling) and the corruption of the section, line, or path BIP-8 codes for diagnostic purposes.
- Inserts ATM cells or POS frames into the transmitted STS-12c/STM-4-4c or STS-3c/STM-1 payload.

1.6 The Transmit ATM Processor

- Provides idle/unassigned cell insertion.
- Provides HCS generation/insertion, and ATM cell payload scrambling.
- Counts number of transmitted and idle cells.
- Provides a UTOPIA Level 2 compliant 16-bit wide datapath interface (clocked up to 50 MHz) with parity support for writing cells into an internal four-cell FIFO.
- Provides a UTOPIA Level 3 compatible 8-bit wide datapath interface (clocked up to 100 MHz) with parity support for writing cells into an internal four-cell FIFO.

1.7 The Transmit POS Processor

- Supports any packet based link layer protocol using byte synchronous HDLC framing like PPP, HDLC and Frame Relay.
- Performs self-synchronous POS data scrambling using the $1+X^{43}$ polynomial.
- Encapsulates packets within a POS frame.
- Performs flag sequence insertion.
- Performs byte stuffing for transparency processing.
- Performs frame check sequence generation using the CRC-CCITT and CRC-32 polynomials.
- Aborts packets under the direction of the host or when the FIFO underflows.
- Provides a SATURN POS-PHY Level 2 compliant 16-bit wide datapath (clocked up to 50 MHz) with parity support to an internal 256 byte FIFO buffer.
- Provides a SATURN POS-PHY Level 3 compliant 8-bit wide datapath (clocked up to 100 MHz) with parity support to an internal 256 byte FIFO buffer.

2 APPLICATIONS

- WAN and Edge ATM switches.
- LAN switches and hubs.
- Packet switches and hubs.
- Routers and Layer 3 Switches
- Network Interface Cards and Uplinks

3 REFERENCES

- ATM Forum - ATM User-Network Interface Specification, V3.1, October, 1995.
- ATM Forum - “UTOPIA, An ATM PHY Interface Specification, Level 2, Version 1”, June, 1995.
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- Bell Communications Research - GR-436-CORE “Digital Network Synchronization Plan”, Issue 1 Revision 1, June 1996..
- ETS 300 417-1-1, "Generic Functional Requirements for Synchronous Digital Hierarchy (SDH) Equipment", January, 1996.
- IETF Network Working Group - RFC-2615 “Point to Point Protocol (PPP) over SONET/SDH Specification”, May 1994.
- IETF Network Working Group - RFC-1661 “The Point to Point Protocol (PPP)”, July 1994.
- IETF Network Working Group - RFC-1662 “PPP in HDLC like framing”, July 1994.
- ITU-T Recommendation G.703 - "Physical/Electrical Characteristics of Hierarchical Digital Interfaces", 1991.
- ITU-T Recommendation G.704 - "General Aspects of Digital Transmission Systems; Terminal Equipment - Synchronous Frame Structures Used At 1544, 6312, 2048, 8488 and 44 736 kbit/s Hierarchical Levels", July, 1995.
- ITU, Recommendation G.707 - "Network Node Interface For The Synchronous Digital Hierarchy", 1996.
- ITU Recommendation G781, “Structure of Recommendations on Equipment for the Synchronous Design Hierarchy (SDH)”, January 1994.
- ITU, Recommendation G.783 - "Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks", 1996.
- ITU Recommendation I.432, “ISDN User Network Interfaces”, March 93.

- PMC-971147 “Saturn Compliant Interface for Packet over SONET Physical Layer and Link Layer Devices, Level 2”, January 1998.
- PMC-980495 “Saturn Compliant Interface for Packet over SONET Physical Layer and Link Layer Devices, Level 3”, December 1998.

4 DEFINITIONS

The following table defines the abbreviations for the S/UNI-622-POS.

AIS	Alarm Indication Signal
APS	Automatic Protection Switching
ASSP	Application Specific Standard Product
ATM	Asynchronous Transfer Mode
BER	Bit Error Rate
BIP	Byte Interleaved Parity
CBI	Common Bus Interface
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
CRSI	CRU and Serial-In Parallel-Out
CRU	Clock Recovery Unit
CSPI	CSU and Parallel-In Serial-Out
CSU	Clock Synthesis Unit
DCC	Data Communication Channel
ECL	Emitter Controlled Logic
ERDI	Enhanced Remote Defect Indication
ESD	Electrostatic Discharge
FCS	Frame Check Sequence
FEBE	Far-End Block Error
FIFO	First-In First-Out
GFC	Generic Flow Control
HCS	Header Check Sequence
HDLC	High-level Data Link Layer
LAN	Local Area Network
LCD	Loss of Cell Delineation
LOF	Loss of Frame

LOH	Line Overhead
LOP	Loss of Pointer
LOS	Loss of Signal
LOT	Loss of Transition
NC	No Connect, indicates an unused pin
NDF	New Data Flag
NNI	Network-Network Interface
ODL	Optical Data Link
OOF	Out of Frame
PECL	Pseudo-ECL
PLL	Phase-Locked Loop
POS	Packet Over SONET
PPP	Point-to-Point Protocol
PSL	Path Signal Label
PSLM	Path Signal Label Mismatch
RASE	Receive APS, Synchronization Extractor and Bit Error Monitor
RDI	Remote Defect Indication
RLOP	Receive Line Overhead Processor
RPOP	Receive Path Overhead Processor
RSOP	Receive Section Overhead Processor
RXCP	Receive ATM Cell Processor
RXFP	Receive POS Frame Processor
SBGA	Super Ball Grid Array
SD	Signal Degrade (alarm), Signal Detect (pin)
SDH	Synchronous Digital Hierarchy
SF	Signal Fail
SOH	Section Overhead
SONET	Synchronous Optical Network
SPE	Synchronous Payload Envelope

SPTB	SONET/SDH Path Trace Buffer
SSTB	SONET/SDH Section Trace Buffer
TIM	Trace Identifier Mismatch
TIU	Trace Identifier Unstable
TLOP	Transmit Line Overhead Processor
TOH	Transport Overhead
TPOP	Transmit Path Overhead Processor
TSOP	Transmit Section Overhead Processor
TXCP	Transmit ATM Cell Processor
TXFP	Transmit POS Frame Processor
UI	Unit Interval
UNI	User-Network Interface
VCI	Virtual Connection Indicator
VCXO	Voltage Controlled Oscillator
VPI	Virtual Path Indicator
WAN	Wide Area Network
XOR	Exclusive OR logic operator

5 APPLICATION EXAMPLES

The PM5357 S/UNI-622-POS is applicable to equipment implementing Asynchronous Transfer Mode (ATM) User-Network Interfaces (UNI), ATM Network-Network Interfaces (NNI), as well as Packet over SONET/SDH (POS) interfaces. The POS interface can support several packet based protocols, including the Point-to-Point Protocol (PPP).

The S/UNI-622-POS may find application at either end of switch-to-switch links or switch-to-terminal links, both in public network (WAN) and private network (LAN) situations. The S/UNI-622-POS provides a comprehensive feature set as well as full compliance to WAN synchronization requirements. The S/UNI-622-POS performs the mapping of either ATM cells or POS frames into the SONET/SDH STS-12c/STM-4-4c synchronous payload envelope (SPE) and processes applicable SONET/SDH section, line and path overheads.

In a typical STS-12c/STM-4-4c ATM application, the S/UNI-622-POS performs clock and data recovery in the receive direction and clock synthesis in the transmit direction of the line interface. The S/UNI-622-POS can also be configured to by-pass the clock recovery, clock synthesis, and serializer/de-serializer functions. In this mode, an external clock and data recovery/serial-to-parallel converter device is required in the receive direction, and an external serial-to-parallel converter/clock synthesis device is required in the transmit direction.

On the system side, the S/UNI-622-POS interfaces directly with ATM layer processors and switching or adaptation functions using a UTOPIA Level 2 compliant 16-bit (clocked up to 50 MHz) or an UTOPIA Level 3 8-bit (clocked up to 100 MHz) synchronous FIFO style interface.

An application with a UTOPIA Level 2 system side interface is shown in Figure 1. An application with a UTOPIA Level 3 system side is shown in Figure 2. The initial configuration and ongoing control and monitoring of the S/UNI-622-POS are normally provided via a generic microprocessor interface.

Figure 1: Typical STS-12c/STM-4-4c ATM (UTOPIA Level 2) Switch Port Application

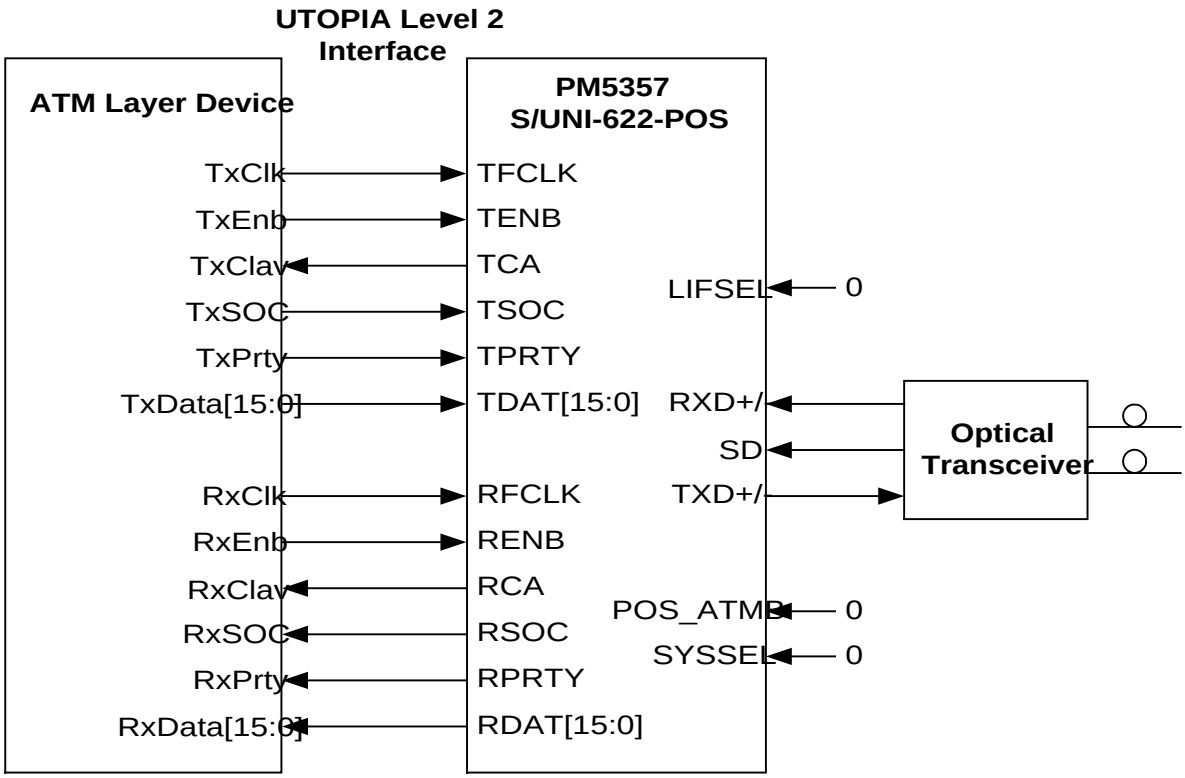
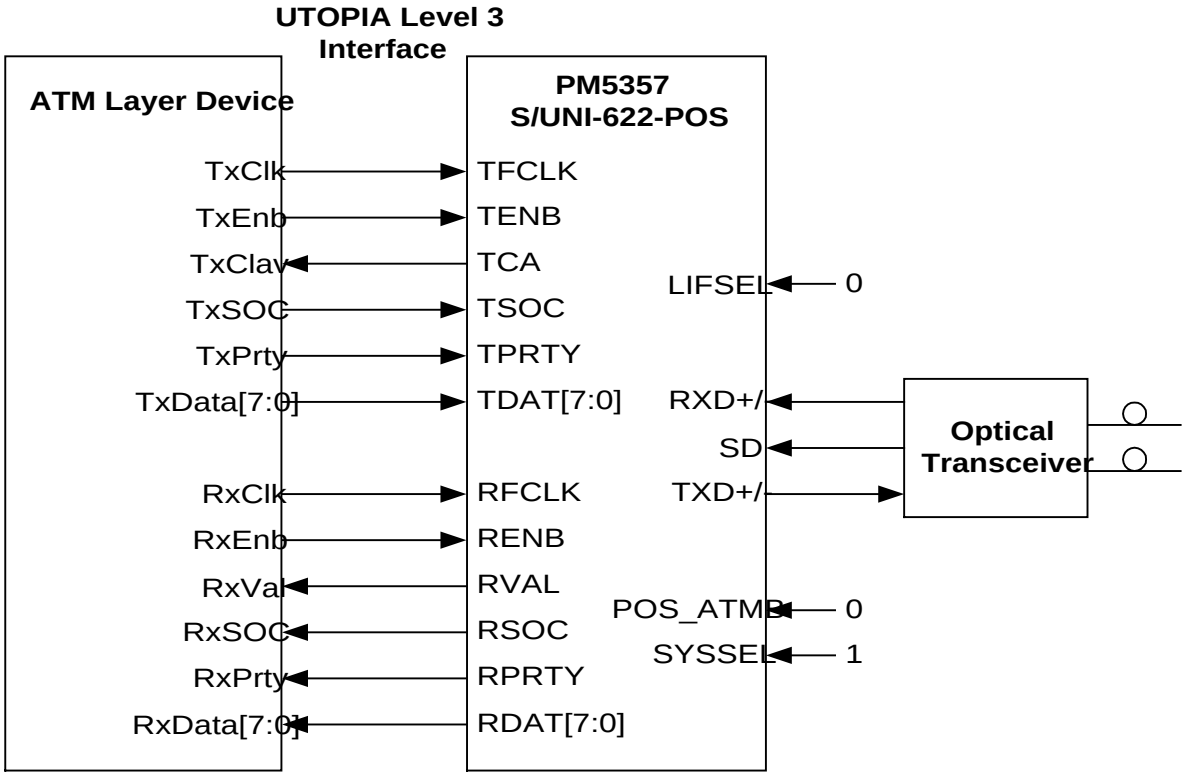


Figure 2: Typical STS-12c/STM-4-4c ATM (UTOPIA Level 3) Switch Port Application



In a typical Packet over SONET/SDH application (i.e. using the PPP protocol) the S/UNI-622-POS performs clock and data recovery in the receive direction and clock synthesis in the transmit direction of the line interface. On the system side, the S/UNI-622-POS interfaces directly with a data link layer processor using a SATURN POS-PHY Level 2 16-bit (clocked up to 50 MHz) or a SATURN POS-PHY Level 3 8-bit (clocked up to 100 MHz) synchronous FIFO interface over which packets are transferred.

An application with a POS-PHY Level 2 interface is shown in Figure 3. An application with a POS-PHY Level 2 interface is shown in Figure 4. The initial configuration and ongoing control and monitoring of the S/UNI-622-POS are normally provided via a generic microprocessor interface.

Figure 3: Typical STS-12c/STM-4-4c Packet over SONET/SDH (POS-PHY Level 2) Application

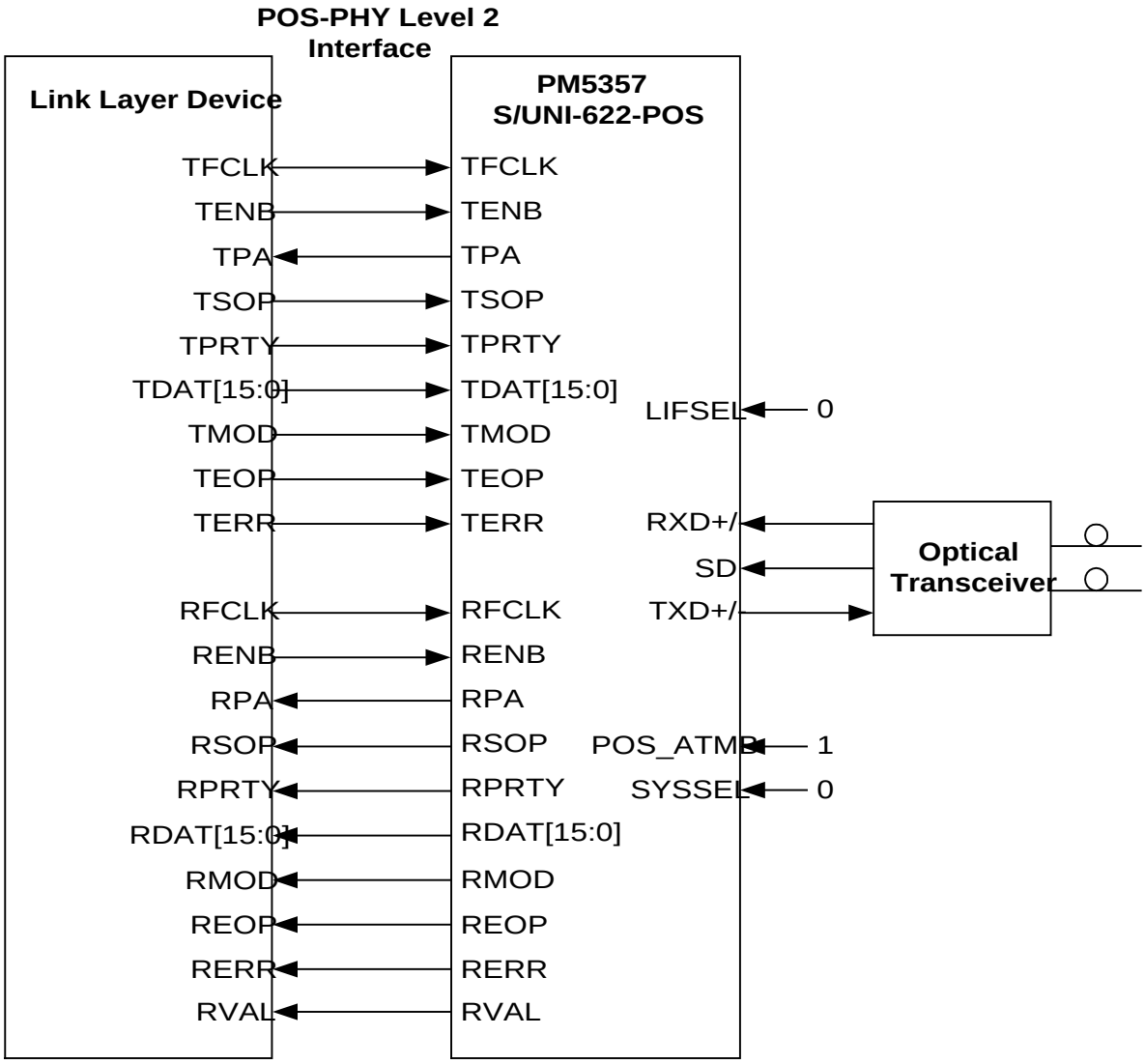
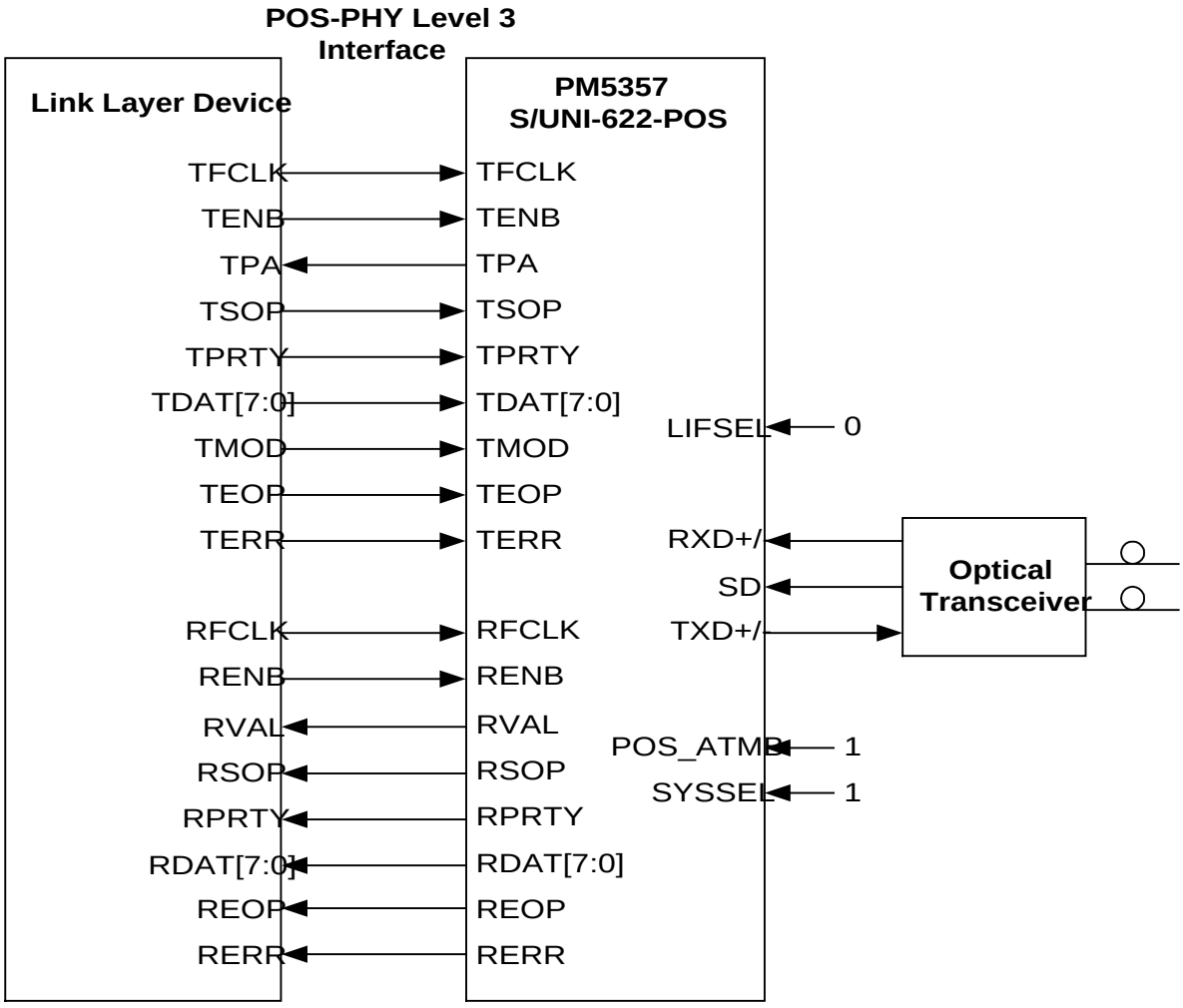
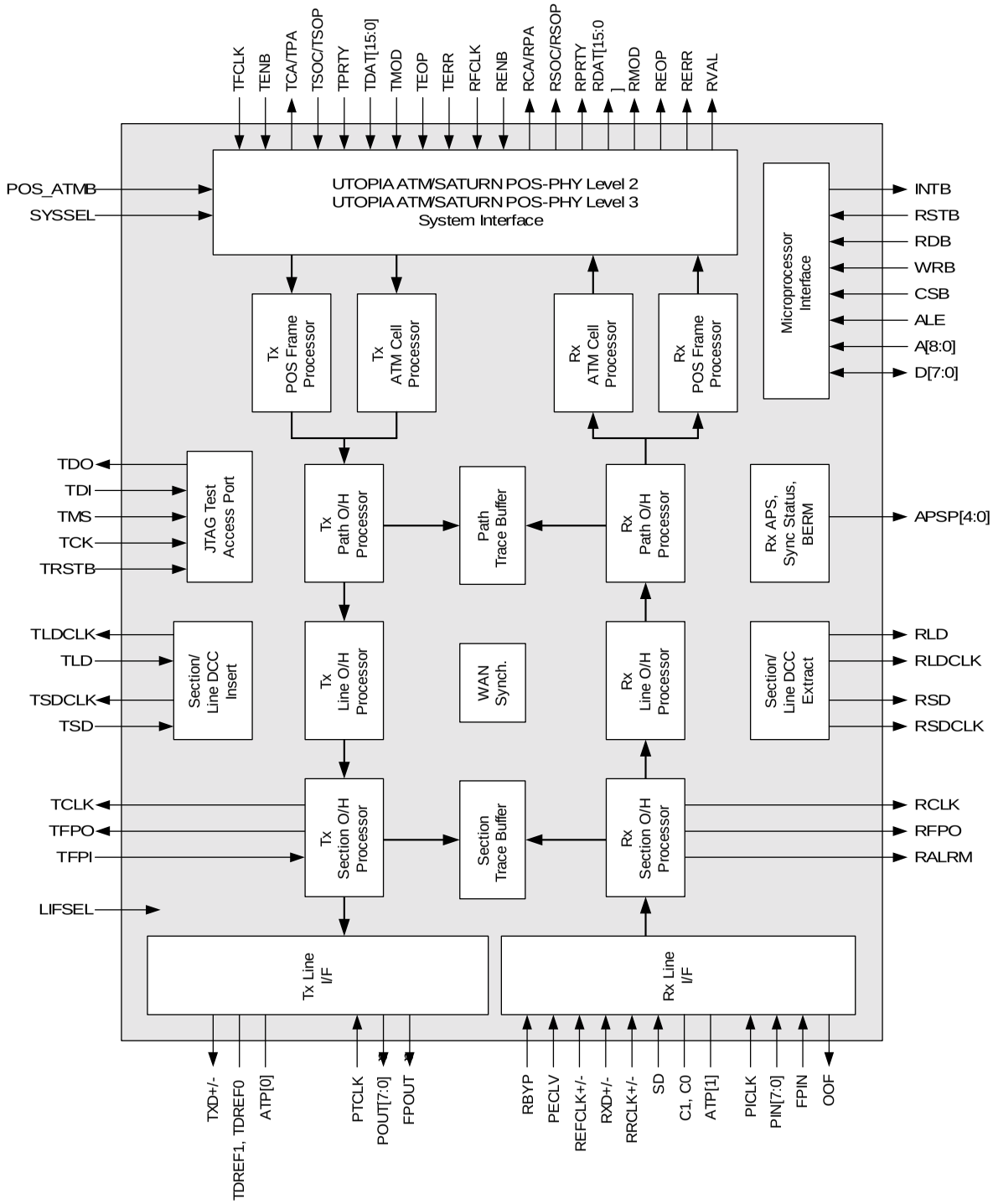


Figure 4: Typical STS-12c/STM-4-4c Packet over SONET/SDH (POS-PHY Level 3) Application



6 BLOCK DIAGRAM



7 DESCRIPTION

The PM5357 S/UNI-622-POS SATURN User Network Interface is a monolithic integrated circuit that implements SONET/SDH processing, ATM mapping and Packet over SONET/SDH mapping functions at the STS-12c/STM-4-4c 622.08 Mbit/s rate.

The S/UNI-622-POS receives SONET/SDH streams using a bit serial interface, recovers the clock and data and processes section, line, and path overhead. The S/UNI-622-POS can also be configured for clock and data recovery and clock synthesis by-pass where it receives SONET/SDH frames via a byte-serial interface. The S/UNI-622-POS performs framing (A1, A2), de-scrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path remote error indications (M1, G1) are also accumulated. The S/UNI-622-POS interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cell payload.

When used to implement an ATM UNI or NNI, the S/UNI-622-POS frames to the ATM payload using cell delineation. HCS error correction is provided. Idle/unassigned cells may be optionally dropped. Cells are also dropped upon detection of an uncorrectable header check sequence error. The ATM cell payloads are descrambled and are written to a four-cell FIFO buffer. The received cells are read from the FIFO using a 16-bit wide UTOPIA Level 2 (clocked up to 50 MHz) or an 8-bit wide UTOPIA Level 3 (clocked up to 100 MHz) datapath interface. Counts of received ATM cell headers that are errored and uncorrectable and those that are errored and correctable are accumulated independently for performance monitoring purposes.

When used to implement packet transmission over a SONET/SDH link, the S/UNI-622-POS extracts Packet over SONET/SDH (POS) frames from the SONET/SDH synchronous payload envelope. Frames are verified for correct construction and size. The control escape characters are removed. The frame check sequence is optionally verified for correctness and the extracted packets are placed in a receive FIFO. The received packets are read from the FIFO through a 16-bit POS-PHY Level 2 (clocked up to 50 MHz) or an 8-bit POS-PHY Level 3 (clocked up to 100 MHz) system side interface. Valid and FCS errored packet counts are provided for performance monitoring. The S/UNI-622-POS Packet over SONET/SDH implementation is flexible enough to support several link layer protocols, including HDLC, PPP and Frame Relay.

The S/UNI-622-POS transmits SONET/SDH streams using a bit serial interface. The S/UNI-622-POS can also be configured for clock and data recovery and clock synthesis by-pass where it transmits the SONET/SDH frames via a byte-serial interface. The S/UNI-622-POS synthesizes the transmit clock from a 77.76MHz frequency reference and performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity codes (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path remote error indications (M1, G1) are also inserted. The S/UNI-622-POS generates the payload pointer (H1, H2) and inserts the synchronous payload envelope that carries the POS frame payload. The S/UNI-622-POS also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics and tester applications.

When used to implement an ATM UNI or NNI, ATM cells are written to an internal four cell FIFO using a 16-bit wide UTOPIA Level 2 (clocked up to 50 MHz) or an 8-bit wide UTOPIA Level 3 (clocked up to 100 MHz) datapath interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one complete cell. The S/UNI-622-POS provides generation of the header check sequence and scrambles the payload of the ATM cells. Each of these transmit ATM cell processing functions can be enabled or bypassed.

When used to implement a Packet over SONET/SDH link, the S/UNI-622-POS inserts POS frames into the SONET/SDH synchronous payload envelope. Packets to be transmitted are written into a 256-byte FIFO through a 16-bit SATURN POS-PHY Level 2 (clocked up to 50 MHz) or an 8-bit SATURN POS-PHY Level 3 (clocked up to 100 MHz) system side interface. POS frames are built by inserting the flags, control escape characters and the FCS fields. Either the CRC-CCITT or CRC-32 can be computed and added to the frame. Several counters are provided for performance monitoring.

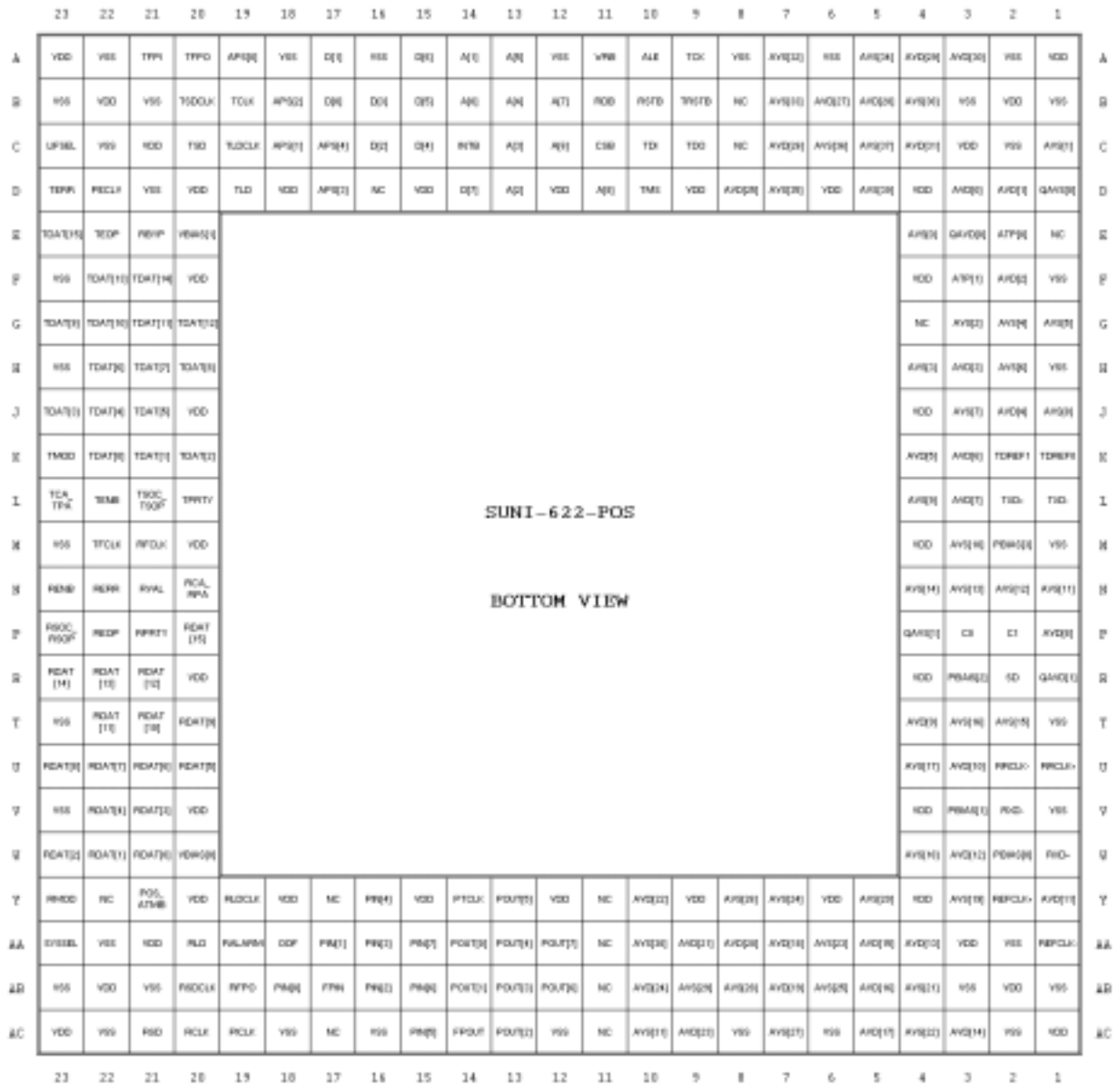
No line rate clocks are required directly by the S/UNI-622-POS as it synthesizes the transmit clock and recovers the receive clock using a 77.76 MHz reference clock. The S/UNI-622-POS outputs a differential PECL line data (TXD+/-). The S/UNI-622-POS also provides a WAN Synchronization controller that can be used to control an external VCXO in order to fully meet Bellcore GR-253-CORE jitter, wander, holdover and stability requirements.

The S/UNI-622-POS is configured, controlled and monitored via a generic 8-bit microprocessor bus interface. The S/UNI-622-POS also provides a standard 5 signal IEEE 1149.1 JTAG test port for boundary scan board test purposes.

The S/UNI-622-POS is implemented in low power, +3.3 Volt, CMOS technology. It has TTL compatible digital inputs and TTL/CMOS compatible digital outputs. High speed inputs and outputs support 3.3V and 5.0V compatible pseudo-ECL (PECL). The S/UNI-622-POS is packaged in a 304 pin SBGA package.

8 PIN DIAGRAM

The S/UNI-622-POS is available in a 304 pin SBGA package having a body size of 31 mm by 31 mm and a ball pitch of 1.27 mm.



9 PIN DESCRIPTION

9.1 Serial Line Side Interface Signals

Pin Name	Type	Pin No.	Function
RBYP	Input	E21	The receive bypass (RBYP) input disables clock recovery. If RBYP is high, RXD+/- is sampled on the rising edge of RRCLK+/-. If RBYP is low, the receive clock is recovered from the RXD+/- bit stream. Please refer to the Operation section for a discussion of the operating modes.
PECLV	Input	D22	The PECL signal voltage select (PELCV) selects between 3.3V PECL signaling and 5V PECL signaling for the PECL inputs. When PECLV is low, the PECL inputs expect a 5V PECL signal. When PECLV is high, the PECL inputs expect a 3.3V PECL signal. The PECL biasing pins PBIAS should be set to the appropriate voltage to prevent latchup. Please refer to the Operation section for a discussion of PECL interfacing issues.
REFCLK+ REFCLK-	Differential PECL Input	Y2 AA1	The differential reference clock inputs (REFCLK+/-) provides a jitter-free 77.76 MHz reference clock for both the clock recovery and the clock synthesis circuits. REFCLK+/- is not required if the clock recovery and clock synthesis features are not used. When the WAN Synchronization controller is used, REFCLK+/- is supplied using a VCXO. In that application, the transmit direction can be externally looped timed to the line receiver in order to meet wander transfer and holdover requirements. Please refer to the Operation section for a discussion of PECL interfacing issues and reference clocks.

Pin Name	Type	Pin No.	Function
RXD+ RXD-	Differential PECL Input	W1 V2	The receive differential data PECL inputs (RXD+/-) contain the NRZ bit serial receive stream. The receive clock is recovered from the RXD+/- bit stream when RBYP is set low. RXD+/- is sampled on the rising edge of RRCLK+/- when RBYP is set high. Please refer to the Operation section for a discussion of PECL interfacing issues.
RRCLK+ RRCLK-	Differential PECL Input	U1 U2	When clock recovery is bypassed (RBYP set high), RRCLK+/- is nominally a 622.08 MHz 50% duty cycle clock and provides timing for the S/UNI-622-POS receive functions. In this case, RXD+/- is sampled on the rising edge of RRCLK+/-. RRCLK+/- is ignored when RBYP is set low. Please refer to the Operation section for a discussion of PECL interfacing issues.
SD	PECL Input	R2	The receive signal detect PECL input (SD) indicates the presence of valid receive signal power from the Optical Physical Medium Dependent Device. A PECL logic high indicates the presence of valid data. A PECL logic low indicates a loss of signal. Please refer to the Operation section for a discussion of PECL interfacing issues
TXD+ TXD-	Differential PECL Output	L2 L1	The transmit differential data PECL outputs (TXD+/-) contain the 622.08 Mbit/s transmit stream. The TXD+/- outputs are driven using the synthesized clock from the CSU-622. Please refer to the Operation section for a discussion of PECL interfacing issues.

9.2 Parallel Line Side Interface Signals - CRU and CSU Bypass

Pin Name	Type	Pin No.	Function
LIFSEL	Input	C23	The line interface select (LIFSEL) selects between serial and parallel line interface modes of operation. When tied high, the parallel mode is selected by-passing the clock and data recovery, clock synthesis and the serializer/de-serializer functions. When tied low, serial mode is selected, enabling clock and data recovery, clock synthesis and the serializer/de-serializer functions. During this operation, the parallel interface may be used for 1+1 APS operation. See the Operation section for more discussion of 1+1 APS support.
PICLK	Input	AC19	The parallel input clock (PICLK) provides timing for S/UNI-622-POS receive function operation when the device is configured for the parallel interface mode of operation. When the RSOC3 bit is set high, PICLK is a 19.44 MHz nominally 50% duty cycle clock. When the RSOC3 bit is set low, PICLK is a 77.76 MHz nominally 50% duty cycle clock. When parallel operation is not used, PICLK may be used for 1+1 APS operation. See the Operation section for more discussion of 1+1 APS.
OOF	Output	AA18	The out of frame (OOF) signal is high while the S/UNI-622-POS is out of frame. OOF is set low while the S/UNI-622-POS is in-frame. An out of frame declaration occurs when four consecutive errored framing patterns (A1 and A2 bytes) have been received. OOF is intended to enable an upstream framing pattern detector to search for the framing pattern. This alarm indication is also available via register access. OOF is an asynchronous output with a minimum period of one PICLK clock.

Pin Name	Type	Pin No.	Function
FPIN	Input	AB17	The active-high framing position input (FPIN) signal indicates the SONET/SDH frame position on the PIN[7:0] bus. In parallel interface operation, the byte on the PIN[7:0] bus indicated by FPIN is the third A2 of the SONET/SDH framing pattern. FPIN is sampled on the rising edge of PICLK. When parallel interface operation is not used, FPIN may be used for 1+1 APS operation. In this mode, FPIN marks the first synchronous payload envelope byte after the J0/Z0 bytes on PIN[7:0]. See the Operation section for more discussion of 1+1 APS.
PIN[0] PIN[1] PIN[2] PIN[3] PIN[4] PIN[5] PIN[6] PIN[7]	Input	AB18 AA17 AB16 AA16 Y16 AC15 AB15 AA15	In parallel interface operation, the data input (PIN[7:0]) bus carries the byte-serial STS-12c/STM-4-4c or STS-3c/STM-1 stream. PIN[7] is the most significant bit (corresponding to bit 1 of each serial byte, the first bit received). PIN[0] is the least significant bit (corresponding to bit 8 of each serial byte, the last bit received). PIN[7:0] is sampled on the rising edge of PICLK. When parallel interface operation is not used, PIN[7:0] may be used for 1+1 APS operation. In this mode, PIN[7:0] carries the byte-serial STS-12c/STM-4-4c transmit path. See the Operation section for more discussion of 1+1 APS.
PTCLK	Input	Y14	The parallel transmit clock (PTCLK) provides timing for S/UNI-622-POS transmit function operation when the device is configured for the parallel interface mode of operation. When TOC3 is low, PTCLK should be a 77.76 MHz nominally 50% duty cycle clock free-running (non gapped) clock. When TOC3 is high, PTCLK should be a 19.44 MHz nominally 50% duty cycle clock.

Pin Name	Type	Pin No.	Function
FPOUT	Output	AC14	In parallel interface operation, the parallel outgoing stream frame pulse (FPOUT) marks the frame alignment on the POUT[7:0] bus. FPOUT marks the first synchronous payload envelope byte after the J0/Z0 bytes. FPOUT is updated on the rising edge of PTCLK. When parallel interface operation is not used, FPOUT may be used for 1+1 APS operation. In this mode, FPOUT marks the first synchronous payload envelope byte after the J0/Z0 bytes. FPOUT is updated on the rising edge of TCLK. See the Operation section for more discussion of 1+1 APS.
POUT[0] POUT[1] POUT[2] POUT[3] POUT[4] POUT[5] POUT[6] POUT[7]	Output	AA14 AB14 AC13 AB13 AA13 Y13 AB12 AA12	In parallel interface operation, the parallel outgoing stream, (POUT[7:0]) carries the scrambled STS-12c/STM-4-4c or STS-3c/STM-1 stream in byte-serial format. POUT[7] is the most significant bit (corresponding to bit 1 of each serial word, the first bit transmitted). POUT[0] is the least significant bit (corresponding to bit 8 of each serial word, the last bit transmitted). POUT[7:0] is updated on the rising edge of PTCLK. When parallel interface operation is not used, POUT[7:0] may be used for 1+1 APS operation. In this mode, POUT[7:0] carries the byte-serial STS-12c/STM-4-4c transmit path and updates on the rising edge of TCLK. See the Operation section for more discussion of 1+1 APS.

9.3 Clocks and Alarms Signals

Pin Name	Type	Pin No.	Function
RCLK	Output	AC20	The receive clock (RCLK) provides a timing reference for the S/UNI-622-POS receive function outputs. RCLK is a 77.76 MHz, 50% duty cycle clock.
RFPO	Output	AB19	The receive frame pulse output (RFPO), when the framing alignment has been found (the OOF register bit is low), is an 8 kHz signal derived from the receive clock RCLK. RFPO pulses high for one RCLK cycle every 9720 RCLK cycles (STS-12c / STM-4-4c). RFPO is updated on the rising edge of RCLK.
RALRM	Output	AA19	The receive alarm (RALRM) output indicates the state of the receive framing. RALRM is low if no receive alarms are active. RALRM is optionally high if line AIS (LAIS), path AIS (PAIS), line RDI (LRDI), path RDI (PRDI), enhanced path RDI (PERDI), loss of signal (LOS), loss of frame (LOF), out of frame (OOF), loss of pointer (LOP), loss of pointer concatenation (LOPC/AISC), loss of cell delineation (LCD), signal fail BER (SFBER), signal degrade BER (SDBER), path trace identification mismatch (TIM) or path signal label mismatch (PSLM) is detected . RALRM is an asynchronous output with a minimum period of one RCLK clock.
TCLK	Output	B19	The transmit clock (TCLK) provides timing for the S/UNI-622-POS transmit function operation. TCLK is a 77.76 MHz, 50% duty cycle clock.
TFPO	Output	A20	The active-high framing position output (TFPO) signal is an 8 kHz signal derived from the transmit clock TCLK. TFPO pulses high for one TCLK cycle every 9720 TCLK cycles (STS-12c / STM-4-4c). TFPO is updated on the rising edge of TCLK.

Pin Name	Type	Pin No.	Function
TFPI	Input	A21	The active high framing position (TFPI) signal is an 8 kHz timing marker for the transmitter. TFPI is used to align the SONET/SDH transport frame generated by the S/UNI-622-POS device to a system reference. TFPI should be brought high for a single TCLK period every 9720 TCLK cycles or a multiple thereof. TFPI must be tied low if such synchronization is not required. TFPI is sampled on the rising edge of TCLK.
APS[0] APS[1] APS[2] APS[3] APS[4]	I/O	A19 C18 B18 D17 C17	The APS Port bus (APS[4:0]) is a bi-directional control bus that can be used to implement a 1+1 APS system. When the APSPOE register bit is set low, the APS[4:0] bus is an input. Data on this bus is used by TPOP to generate the path RDI and path FEBE. When the APSPOE register bit is set high, the APS[4:0] bus is an output with data generated by RPOP. APS[0] FEBE Clock (576 kHz) APS[1] FEBE Data APS[2] RDI[0] (G1 bit 5) APS[3] RDI[1] (G1 bit 6) APS[4] RDI[2] (G1 bit 7) See the Operation section for more discussion of 1+1 APS.

9.4 Section and Line Status DCC Pins

Pin Name	Type	Pin No.	Function
RSDCLK	Output	AB20	The receive section DCC clock (RSDCLK) is a 192 kHz clock used to update the RSD input. RSDCLK is generated by gapping a 216 kHz clock.
RSD	Output	AC21	The receive section DCC (RSD) signal contains the serial section data communications channel (D1, D2 D3) extracted from the incoming stream. RSD is updated on the falling edge of RSDCLK.
RLDCLK	Output	Y19	The receive line DCC clock (RLDCLK) is a 576 kHz clock used to update the RLD output. RLDCLK is generated by gapping a 2.16 MHz clock.
RLD	Output	AA20	The receive line DCC (RLD) signal contains the serial line data communications channel (D4 - D12) extracted from the incoming stream. RLD is updated on the falling edge of RLDCLK.
TSDCLK	Output	B20	The transmit section DCC clock (TSDCLK) is a 192 kHz clock used to sample the TSD input. TSDCLK is generated by gapping a 216 kHz clock.
TSD	Input	C20	The transmit section DCC (TSD) signal contains the serial section data communications channel (D1, D2 D3). When not used, this input should be connected to logic zero. TSD is sampled on the rising edge of TSDCLK.
TLDCLK	Output	C19	The transmit line DCC clock (TLDCLK) is a 576 kHz clock used to sample the TLD input. TLDCLK is generated by gapping a 2.16 MHz clock.
TLD	Input	D19	The transmit line DCC (TLD) signal contains the serial line data communications channel (D4 - D12). When not used, this input should be connected to logic zero. TLD is sampled on the rising edge of TLDCLK.

9.5 ATM (UTOPIA) and Packet over SONET/SDH (POS) System Interface

Pin Name	Type	Pin No.	Function
POS_ ATMB	Input	Y21	The physical layer select (POS_ATMB) pin selects between the ATM and Packet over SONET/SDH modes of operation. When tied low, the device implements the ATM physical layer. When tied high, the device implements the Packet over SONET/SDH physical layer. This pin affects SONET/SDH mapping as well as the pin definitions of the system interface bus and may be overridden by software in the RUL3 and TUL3 registers.
SYSSEL	Input	AA23	The system interface select (SYSSEL) pin selects between the 16-bit UTOPIA/POS-PHY Level 2 mode and the 8-bit UTOPIA/POS-PHY Level 3 mode of the system side interfaces for both ATM and Packet over SONET/SDH operation. When tied low, the 16-bit Level 2 mode is enabled. When tied high, the 8-bit Level 3 mode is enabled. This pin setting affects the pin definitions of the system interface bus and may be overridden by software in the RUL3 and TUL3 registers.

Pin Name	Type	Pin No.	Function
TFCLK	Input	M22	UTOPIA transmit FIFO write clock (TFCLK) is used to write ATM cells to the four cell transmit FIFO. When in 16-bit Level 2 ATM mode, TFCLK must cycle at a 50 MHz to 40 MHz instantaneous rate, and must be a free running clock (cannot be gapped). When in 8-bit Level 3 ATM mode, TFCLK must cycle at a 100 MHz to 60 MHz instantaneous rate, and must be a free running clock (cannot be gapped).
			POS-PHY transmit FIFO write clock (TFCLK) is used to write packet data into the 256 byte packet FIFO. When in 16-bit Level 2 POS mode, TFCLK must cycle at a 50 MHz to 40 MHz instantaneous rate, and must be a free running clock (cannot be gapped). When in 8-bit Level 3 POS mode, TFCLK must cycle at a 100 MHz to 60 MHz instantaneous rate, and must be a free running clock (cannot be gapped).
TEOP	Input	E22	The POS-PHY transmit end of packet (TEOP) marks the end of packet on the TDAT bus when configured for packet data. In 16-bit Level 2 POS mode, the TEOP signal marks the last word of a packet on the TDAT[15:0] bus. The TMOD signal indicates how many bytes are in the last word. It is legal to set TSOP high at the same time as TEOP high in order to support one or two byte packets. In 8-bit Level 3 POS mode, the TEOP signal marks the last byte of a packet on the TDAT[7:0] bus. The TMOD signal is ignored in this mode. TEOP is only valid when TENB is simultaneously asserted. TEOP is only used for POS operation and is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7] TDAT[8] TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15]	Input	K22 K21 K20 J23 J22 J21 H22 H21 H20 G23 G22 G21 G20 F22 F21 E23	The UTOPIA transmit cell data (TDAT[15:0]) bus carries the ATM cell octets that are written to the transmit FIFO. In 16-bit Level 2 ATM mode, the TDAT[15:0] is considered valid only when TENB is simultaneously asserted. In 8-bit Level 3 ATM mode, the TDAT[7:0] bus is considered valid only when TENB is simultaneously asserted. TDAT[15:8] are ignored. TDAT[15:0] is sampled on the rising edge of TFCLK. The POS-PHY transmit packet data (TDAT[15:0]) bus carries the POS packet octets that are written to the transmit FIFO. In 16-bit Level 2 POS mode, the TDAT[15:0] bus is considered valid only when TENB is simultaneously asserted. In 8-bit Level 3 POS mode, the TDAT[7:0] signals is considered valid only when TENB is simultaneously asserted. TDAT[15:8] are ignored. TDAT[15:0] is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TSOC	Input	L21	The UTOPIA transmit start of cell (TSOC) signal marks the start of a cell structure on the TDAT bus. In 16-bit Level 2 ATM mode, the first word of the cell structure is present on the TDAT[15:0] bus when TSOC is high. It is not necessary for TSOC to be present for each cell. In 8-bit Level 3 ATM mode, the first byte of the cell structure is present on the TDAT[7:0] bus when TSOC is high. TSOC must be present for each cell. TSOC is considered valid only when TENB is simultaneously asserted. TSOC is sampled on the rising edge of TFCLK.
TSOP			POS-PHY transmit start of packet (TSOP) signal indicates the start of a packet on the TDAT bus. TSOP is required to be present at all instances for proper operation. In 16-bit Level 2 POS mode, TSOP must be set high for the first word of a packet on TDAT[15:0]. In 8-bit Level 3 POS mode, TSOP must be set high during the first byte of the packet on TDAT[7:0]. TSOP is considered valid only when TENB is simultaneously asserted. TSOP is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TPRTY	Input	L20	The UTOPIA transmit bus parity (TPRTY) signal indicates the parity on the TDAT bus. A parity error is indicated by a status bit and a maskable interrupt. Cells with parity errors are inserted in the transmit stream, so the TPRTY input may be unused. In 16-bit Level 2 ATM mode, the TPRTY signal indicates the parity on the TDAT[15:0] bus. Odd or even parity selection is made in the TXCP registers. In 8-bit Level 3 ATM mode, the TPRTY signal indicates the parity on the TDAT[7:0] bus. Odd or even parity selection is made in the TUL3 registers. TPRTY is considered valid only when TENB is simultaneously asserted. TPRTY is sampled on the rising edge of TFCLK.
			The POS-PHY transmit bus parity (TPRTY) signal indicates the parity on the TDAT bus. A parity error is indicated by a status bit and a maskable interrupt. Packets with parity errors are inserted in the transmit stream, so the TPRTY input may be unused. In 16-bit Level 2 POS mode, the TPRTY signal indicates the parity on the TDAT[15:0] bus. Odd or even parity selection is made in the TXFP registers. In 8-bit Level 3 POS mode, the TPRTY signal indicates the parity on the TDAT[7:0] bus. Odd or even parity selection is made in the TUL3 registers. TPRTY is considered valid only when TENB is simultaneously asserted. TPRTY is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TENB	Input	L22	The UTOPIA transmit write enable (TENB) signal is an active low input which is used to initiate writes to the transmit FIFO's. When TENB is sampled high, the information sampled on the TDAT, TPRTY and TSOC signals are invalid. When TENB is sampled low, the information sampled on the TDAT, TPRTY and TSOC signals are valid and are written into the transmit FIFO. TENB is sampled on the rising edge of TFCLK.
			The POS-PHY transmit write enable (TENB) signal is an active low input which is used to initiate writes to the transmit FIFO's. When TENB is sampled high, the information sampled on the TDAT, TPRTY, TSOP, TEOP, TMOD and TERR signals are invalid. When TENB is sampled low, the information sampled on the TDAT, TPRTY, TSOP, TEOP, TMOD and TERR signals are valid and are written into the transmit FIFO. TENB is sampled on the rising edge of TFCLK.
TERR	Input	D23	The POS-PHY transmit error (TERR) is used to indicate that the current packet must be aborted. Packets marked with TERR will be appended with the abort sequence (0x7D-0x7E) when transmitted. In 16-bit Level 2 POS mode, TERR should only be asserted during the last word of the packet being transferred on TDAT[15:0]. In 8-bit Level 3 POS mode, TERR should only be asserted during the last byte of the packet being transferred on TDAT[7:0]. TERR is only considered valid when TENB and TEOP are simultaneously asserted. TERR is ignored for ATM modes of operation and is sampled on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TCA	Output	L23	The UTOPIA transmit cell available (TCA) signal provides direct status indication of when cell space is available in the transmit FIFO. When set high, TCA indicates that the corresponding transmit FIFO is not full and a complete cell may be written. TCA is set low to either indicate that the transmit FIFO is near full or that the transmit FIFO is full. To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be set to one, two, three or four cells. Note that regardless of what fill level TCA is set to indicate "full" at, the transmit cell processor can store 4 complete cells. In 16-bit Level 2 ATM mode, TCA will transition low one TFCLK cycle after the payload word 19 or 23 (depending of the configuration in TXCP) is sampled on the TDAT[15:0] bus. In 8-bit Level 3 ATM mode, TCA will transition low on the rising edge of TFCLK before the payload byte 45 is sampled on the TDAT[7:0] bus. TCA is updated on the rising edge of TFCLK.
TPA			The POS-PHY transmit packet available (TPA) signal provides direct status indication the fill status of the transmit FIFO. Note that regardless of what fill level TPA is set to indicate "full" at, the transmit packet processor can store 256 bytes of data. When TPA transitions high, it indicates that the transmit FIFO has enough room to store a configurable number of data bytes. This transition level is selected in the TXFP registers. When TPA transitions low, it indicates that the transmit FIFO is either full or near full as specified by the TXFP registers. TPA is updated on the rising edge of TFCLK.

Pin Name	Type	Pin No.	Function
TMOD	Input	K23	The POS-PHY transmit word modulo (TMOD) signal indicates the size of the current word when configured for packet data in 16-bit Level 2 mode. TMOD is ignored when the system interface is configured for ATM cell data or Level 3 modes. During a packet transfer, every word on TDAT[15:0] must contain two valid bytes of packet data except at the end of the packet where the word is composed of 1 or 2 valid bytes. TMOD is set high to indicate a word with 1 valid byte present on TDAT[15:8]. TMOD must be set low during all other times. TMOD is considered valid only when TENB is simultaneously asserted. TMOD is only used for POS operation and is sampled on the rising edge of TFCLK.
RFCLK	Input	M21	The UTOPIA receive FIFO read clock (RFCLK). RFCLK is used to read ATM cells from the four cell receive FIFO. When in 16-bit Level 2 ATM mode, RFCLK must cycle at a 50 MHz to 40 MHz instantaneous rate, and must be a free running clock (cannot be gapped). When in 8-bit Level 3 ATM mode, RFCLK must cycle at a 100 MHz to 60 MHz instantaneous rate, and must be a free running clock (cannot be gapped).
			POS-PHY receive FIFO read clock (RFCLK). This signal is used to read packet data from the 256 byte packet FIFO. When in 16-bit Level 2 POS mode, RFCLK must cycle at a 50 MHz to 40 MHz instantaneous rate, and must be a free running clock (cannot be gapped). When in 8-bit Level 3 POS mode, RFCLK must cycle at a 100 MHz to 60 MHz instantaneous rate, and must be a free runnning clock (cannot be gapped).

Pin Name	Type	Pin No.	Function
RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7] RDAT[8] RDAT[9] RDAT[10] RDAT[11] RDAT[12] RDAT[13] RDAT[14] RDAT[15]	Output	W21 W22 W23 V21 V22 U20 U21 U22 U23 T20 T21 T22 R21 R22 R23 P20	UTOPIA receive cell data (RDAT[15:0]) bus carries the ATM cell octets that are read from the receive FIFO. In 16-bit Level 2 ATM mode, RDAT[15:0] is consider valid only when RENB is asserted. RDAT[15:0] is tri-stated when RENB is sampled high. In 8-bit Level 3 ATM mode, only the RDAT[7:0] signals are valid when RVAL is asserted. RDAT[15:8] contain invalid data. RDAT[15:0] is updated on the rising edge of RFCLK.
			POS-PHY receive packet data (RDAT[15:0]) bus carries the POS packet octets that are read from the receive FIFO. In 16-bit Level 2 POS mode, RDAT[15:0] is considered valid only when RVAL is asserted. RDAT[15:0] is tri-stated when RENB is sampled high. In 8-bit Level 3 POS mode, only the RDAT[7:0] signals are valid when RVAL is asserted. RDAT[15:8] contain invalid data. RDAT[15:0] is updated on the rising edge of RFCLK.
RMOD	Output	Y23	The POS-PHY receive modulo (RMOD) indicates the number of bytes carried by the RDAT[15:0] bus during the last word of a packet transfer. During a packet transfer every word must be complete except the last word which can be composed of 1 or 2 bytes. RMOD set high indicate a single valid byte in the word present on RDAT[15:8] while RMOD set low indicates two valid bytes in the word. RMOD is tri-stated when RENB is sampled high. RMOD is only used in 16-bit Level 2 POS operation and is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RVAL	Output	N21	The UTOPIA Level 3 receive data valid (RVAL) signal indicates the validity of the receive data signals. When RVAL is high, the receive signals RDAT, RSOC and RPRTY are valid. When RVAL is low, all receive signals are invalid and must be disregarded. In 16-bit Level 2 ATM mode, RVAL is invalid and must be ignored. In 8-bit Level 3 ATM mode, RVAL will be high when valid data is on the RDAT bus. The RVAL will transition low when the FIFO is empty. Once deasserted, RVAL will remain deasserted until a complete ATM cell is written into the receive FIFO. RVAL is updated on the rising edge of RFCLK.
			The POS-PHY receive data valid (RVAL) signal indicates the validity of the receive data signals. When RVAL is high, the receive signals RDAT, RSOP, REOP, RMOD, RPRTY and RERR are valid. When RVAL is low, all receive signals are invalid and must be disregarded. In 16-bit Level 2 POS mode, RVAL will transition low on a FIFO empty condition or on an end of packet. Once deasserted, RVAL will remain low until RENB is deasserted. No data will be removed from the receive FIFO while RVAL is held low. RVAL is tri-stated when RENB is deasserted. See Functional Timing section for more details on using RVAL with RPA. In 8-bit Level 3 mode, RVAL will be high when valid data is on the RDAT bus. RVAL will transition low when the FIFO is empty. RVAL will remain low until a programmable minimum number of bytes exist in the receive FIFO. The threshold is configured using the TXFP registers. RVAL will not assert until RENB is asserted. RVAL is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RSOC	Output	P23	The UTOPIA receive start of cell (RSOC) signal marks the start of a cell structure on the RDAT bus. In 16-bit Level 2 ATM mode, the first word of the cell structure is present on the RDAT[15:0] bus when RSOC is high. RSOC is tri-stated when RENB is sampled high. In 8-bit Level 3 ATM mode, the first byte of the cell structure is present on the RDAT[7:0] bus when RSOC is high. RDAT[15:8] are invalid and must be ignored. RSOC is updated on the rising edge of RFCLK.
RSOP			The POS-PHY receive start of packet (RSOP) indicates the start of a packet on the RDAT bus. In 16-bit Level 2 POS mode, RSOP is set high for the first word of a packet on RDAT[15:0]. RSOP is tri-stated when RENB is sampled high. In 8-bit Level 3 POS mode, RSOP is set high for the first byte of a packet on RDAT[7:0]. RDAT[15:8] are invalid and must be ignored. RSOP is updated on the rising edge of RFCLK
RERR	Output	N22	The POS-PHY receive error (RERR) indicates that the current packet is invalid due to an error such as invalid FCS, excessive length or received abort. In 16-bit Level 2 POS mode, RERR may only assert when REOP is asserted marking the last word of the packet. RERR is tri-stated when RENB is sampled high. In 8-bit Level 3 POS mode, RERR may only assert when REOP is asserted marking the last byte of the packet. RERR is only used in POS mode and is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RPRTY	Output	P21	The UTOPIA receive parity (RPRTY) signal indicates the parity of the RDAT bus. When in 16-bit Level 2 ATM mode, the RPRTY signal indicates the parity on the RDAT[15:0] bus. RPRTY is tri-stated when RENB is sampled high. Odd or even parity selection is made in the RXCP registers. When in 8-bit Level 3 ATM mode, the RPRTY signal indicates the parity on the RDAT[7:0] bus. Odd or even parity selection is made in the RUL3 registers. RPRTY is updated on the rising edge of RFCLK.
			The POS-PHY receive parity (RPRTY indicates the parity of the RDAT bus. When in 16-bit Level 2 POS mode, the RPRTY signal indicates the parity on the RDAT[15:0] bus. RPRTY is tri-stated when RENB is sampled high. Odd or even parity selection is made in the RXFP registers. When in 8-bit Level 3 POS mode, the RPRTY signal indicates the parity on the RDAT[7:0] bus. Odd or even parity selection is made in the RUL3 registers. RPRTY is updated on the rising edge of RFCLK.
REOP	Output	P22	The POS-PHY receive end of packet (REOP) marks the end of packet on the RDAT[15:0] bus. It is legal for RSOP to be high at the same time REOP is high. In 16-bit Level 2 mode, REOP is set high to mark the last word of the packet presented on the RDAT[15:0] bus. When REOP is high, RMOD specifies if the last word has one or two valid bytes of data. REOP is tri-stated when RENB is deasserted. In 8-bit Level 3 mode, REOP is set high to mark the last byte of the packet presented on the RDAT[7:0] bus. The RMOD signal is not used in this mode. REOP is only used for POS operation and is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RENB	Input	N23	The UTOPIA receive read enable (RENB) is used to initiate reads from the receive FIFO. The system may de-assert RENB if it is unable to accept more data. In 16-bit Level 2 ATM mode, a read is not performed and RDAT[15:0], RPRTY and RSOC will tristate when RENB is sampled high. When RENB is sampled low, the word on the RDAT[15:0] bus is read from the receive FIFO and changes to the next value on the next clock cycle. In 8-bit Level 3 ATM mode, a read is not performed and RDAT[7:0] does not change when RENB is sampled high. When RENB is sampled low, the word on the RDAT[7:0] bus is read from the receive FIFO and changes to the next value on the next clock cycle. RENB is sampled on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
			The POS-PHY receive read enable (RENB) is used to initiate reads from the receive FIFO. During a data transfer, RVAL must be monitored since it will indicate if the data is valid. The system may deassert RENB at any time if it is unable to accept more data. In 16-bit Level 2 POS mode, a read is not performed and RDAT[15:0], RPRTY, RSOP, REOP, RMOD, RVAL and RERR will tristate when RENB is sampled high. When RENB is sampled low, the word on the RDAT[15:0] bus is read from the receive FIFO and changes to the next value in the FIFO on the next clock cycle. During a data transfer, RVAL must be monitored since it will indicate if RDAT[15:0] is valid. Once RVAL deasserts, RENB must eventually be deasserted to reset RVAL. In 8-bit Level 3 POS mode, a read is not performed and RDAT[7:0] does not change when RENB is sampled high. When RENB is sampled low, the word on the RDAT[7:0] bus is read from the receive FIFO and changes to the next value on the next clock cycle. RENB is sampled on the rising edge of RFCLK.
RCA	Output	N20	The UTOPIA receive cell available (RCA) provides direct status indication of when a cell is available in the receive FIFO. In 16-bit Level 2 mode, RCA can be configured to de-assert when either zero or four bytes remain in the FIFO. RCA will thus transition low on the rising edge of RFCLK after payload word 24 or 19 is output on the RDAT[15:0] bus depending on the RXCP registers. In 8-bit Level 3 mode, RCA is ignored as the RVAL signal identifies valid data on the RDAT[7:0] bus. RCA is updated on the rising edge of RFCLK.

Pin Name	Type	Pin No.	Function
RPA			The POS-PHY receive packet available (RPA) provides a direct status indication of when a programmable number of bytes of data is available in the receive FIFO. In 16-bit Level 2 mode, the receive FIFO has at least one end of packet or a programmable minimum number of bytes to be read when RPA is high, RPA is otherwise low. The threshold is configured in the RXFP registers. In 16-bit Level 2 mode, the RPA may incorrectly indicate the FIFO fill level is above the high water mark after an end of packet is transferred over RDAT[15:0]. See the Functional Timing section for more details of using RVAL with RPA to prevent data corruption. In 8-bit Level 3 mode, RPA is ignored as the RVAL signal identifies valid data on the RDAT[7:0] bus. RPA is updated on the rising edge of RFCLK.

9.6 Microprocessor Interface Signals

Pin Name	Type	Pin No.	Function
CSB	Input	C11	The active-low chip select (CSB) signal is low during S/UNI-622-POS register accesses. When CSB is high, the RDB and WRB inputs are ignored. When CSB is low, the RDB and WRB are valid. CSB must be high when RSTB is low to properly reset the chip. If CSB is not required (i.e., registers accesses are controlled using the RDB and WRB signals only), CSB must be connected to an inverted version of the RSTB input.
RDB	Input	B11	The active-low read enable (RDB) signal is low during S/UNI-622-POS register read accesses. The S/UNI-622-POS drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	A11	The active-low write strobe (WRB) signal is low during a S/UNI-622-POS register write accesses. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	B17 A17 C16 B16 C15 B15 A15 D14	The bi-directional data bus D[7:0] is used during S/UNI-622-POS register read and write accesses.
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7]	Input	B14 A14 D13 C13 B13 A13 C12 B12	The address bus A[7:0] selects specific registers during S/UNI-622-POS register accesses.

Pin Name	Type	Pin No.	Function
A[8]	Input	D11	The test register select (A[8]) signal selects between normal and test mode register accesses. A[8] is high during test mode register accesses, and is low during normal mode register accesses. A[8] may be tied low.
RSTB	Input	B10	The active-low reset (RSTB) signal provides an asynchronous S/UNI-622-POS reset. RSTB is a Schmitt triggered input with an integral pull-up resistor. CSB must be held high when RSTB is low in order to properly reset this chip.
ALE	Input	A10	The address latch enable (ALE) is active-high and latches the address bus A[8:0] when low. When ALE is high, the internal address latches are transparent. It allows the S/UNI-622-POS to interface to a multiplexed address/data bus. ALE has an integral pull-up resistor.
INTB	Output	C14	The active-low interrupt (INTB) signal is set low when a S/UNI-622-POS interrupt source is active and that source is unmasked. The S/UNI-622-POS may be enabled to report many alarms or events via interrupts. Examples of interrupt sources are loss of signal (LOS), loss of frame (LOF), line AIS, line remote defect indication (LRDI) detect, loss of pointer (LOP), path AIS, path remote defect indication and others. INTB is tri-stated when the all enabled interrupt sources are acknowledged via an appropriate register access. INTB is an open drain output.

9.7 JTAG Test Access Port (TAP) Signals

Pin Name	Type	Pin No.	Function
TCK	Input	A9	The test clock (TCK) signal provides clock timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	Input	D10	The test mode select (TMS) signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TDI	Input	C10	The test data input (TDI) signal carries test data into the S/UNI-622-POS via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TDO	Output	C9	The test data output (TDO) signal carries test data out of the S/UNI-622-POS via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tristate output which is inactive except when shifting boundary scan data is in progress.
TRSTB	Input	B9	The active-low test reset (TRSTB) signal provides an asynchronous S/UNI-622-POS test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmitt triggered input with an integral pull-up resistor. Note that when not being used, TRSTB may be tied low or connected to the RSTB input.

9.8 Analog Signals

Pin Name	Type	Pin No.	Function
TDREF0 TDREF1	Analog	K1 K2	The transmit data reference (TDREF0 and TDREF1) analog pins are provided to create calibrated currents for the PECL output transceivers TXD+/-. A 2.00K ohm resistor is connected across the TDREF0 and TDREF1 pins.
C0 C1	Analog	P3 P2	The analog C1 and C0 pins are provided for applications that must meet SONET/SDH jitter transfer specifications. A 47nF non-polarized capacitor (ceramic ± 5% X7R or equivalent) is attached across C1 and C0 for these applications. When the capacitor is used, the RTYPE bit in the CRSI must be set to logic one for proper operation. When the capacitor is not used, these pins are left floating and the RTYPE register bit in the CRSI must be set to logic zero for proper operation.
ATP[0] ATP[1]	Analog	E2 F3	The receive and transmit analog test ports (ATP[1:0]). These pins are used for manufacturing testing only and should be tied to analog ground (AVS).

9.9 Power and Ground

Pin Name	Type	Pin No.	Function
VBIAS[0] VBIAS[1]	Bias Voltage	W20 E20	Digital input biases (VBIAS). When tied to +5V, the VBIAS inputs are used to bias the wells of the digital inputs so that the pads can tolerate up to 5V on their inputs without forward biasing internal ESD protection devices. When VBIAS are tied to +3.3V, the digital inputs will only tolerate 3.3V level voltages. The system interface inputs (RFCLK, RENB, TFCLK, TENB, TDAT[15:0], TMOD, TERR, TSOC/TSOP, TEOP and TPRTY) do not use the bias voltages and are 3.3V tolerant only.
PBIAS[0] PBIAS[1] PBIAS[2] PBIAS[3]	Bias Voltage	W2 V3 R3 M2	PECL input biases (PBIAS). When tied to +5V, the PBIAS inputs are used to bias the wells in the PECL inputs and output so that the pads can tolerate up to 5V without forward biasing internal ESD protection devices. When the PBIAS inputs are tied to +3.3V, the pads will only tolerate 3.3V level voltages. PBIAS[0] REFCLK+/- Input PBIAS[1] RXD+/- Input PBIAS[2] RRCLK+/- Input PBIAS[3] TXD+/- Output Please see the Operation section for detailed information on PECL interfacing issues.
QAVD[0] QAVD[1]	Analog Power	E3 R1	The quiet power (QAVD) pins for the analog core. QAVD should be connected to well-decoupled analog +3.3V supply. Please see the Operation section for detailed information.
QAVS[0] QAVS[1]	Analog Ground	D1 P4	The quiet ground (QAVS) pins for the analog core. QAVS should be connected to analog ground of the QAVD supply. Please see the Operation section for detailed information.

Pin Name	Type	Pin No.	Function
VDD	Digital Power	A1 A23 AA3 AA21 AB2 AB22 AC1 AC23 B2 B22 C3 C21 D4 D6 D9 D12 D15 D18 D20 F4 F20 J4 J20 M4 M20 R4 R20 V4 V20 Y4 Y6 Y9 Y12 Y15 Y18 Y20	The digital power (VDD) pins should be connected to a well-decoupled +3.3 V digital power supply.

Pin Name	Type	Pin No.	Function
VSS	Digital Ground	A2 A6 A8 A12 A16 A18 A22 AA2 AA22 AB1 AB3 AB21 AB23 AC2 AC6 AC8 AC12 AC16 AC18 AC22 B1 B3 B21 B23 C2 C22 D21 F1 F23 H1 H23 M1 M23 T1 T23 V1 V23	The digital ground (VSS) pins should be connected to the digital ground of the digital power supply.

Pin Name	Type	Pin No.	Function
AVD[0] AVD[1] AVD[2] AVD[3] AVD[4] AVD[5] AVD[6] AVD[7] AVD[8] AVD[9] AVD[10] AVD[11] AVD[12] AVD[13] AVD[14] AVD[15] AVD[16] AVD[17] AVD[18] AVD[19] AVD[20] AVD[21] AVD[22] AVD[23] AVD[24] AVD[25] AVD[26] AVD[27] AVD[28] AVD[29] AVD[30] AVD[31]	Analog Power	D3 D2 F2 H3 J2 K4 K3 L3 P1 T4 U3 Y1 W3 AA4 AC3 AA5 AB5 AC5 AA7 AB7 AA8 AA9 Y10 AC9 AB10 D8 C7 B6 B5 A4 A3 C4	The analog power (AVD) pins for the analog core. The AVD pins should be connected through passive filtering networks to a well-decoupled +3.3V analog power supply. Please see the Operation section for detailed information.

Pin Name	Type	Pin No.	Function
AVS[0] AVS[1] AVS[2] AVS[3] AVS[4] AVS[5] AVS[6] AVS[7] AVS[8] AVS[9] AVS[10] AVS[11] AVS[12] AVS[13] AVS[14] AVS[15] AVS[16] AVS[17] AVS[18] AVS[19] AVS[20] AVS[21] AVS[22] AVS[23] AVS[24] AVS[25] AVS[26] AVS[27] AVS[28] AVS[29] AVS[30] AVS[31] AVS[32] AVS[33] AVS[34] AVS[35] AVS[36] AVS[37] AVS[38] AVS[39]	Analog Ground	E4 C1 G3 H4 G2 G1 H2 J3 J1 L4 M3 N1 N2 N3 N4 T2 T3 U4 W4 Y3 Y5 AB4 AC4 AA6 Y7 AB6 Y8 AC7 AB8 AB9 AA10 AC10 A7 B7 A5 D7 C6 C5 B4 D5	The analog ground (AVS) pins for the analog core. The AVS pins should be connected to the analog ground of the analog power supply. Please see the Operation section for detailed information.

Notes on Pin Description:

1. All S/UNI-622-POS inputs and bi-directional signals present minimum capacitive loading and operate at TTL logic levels except the inputs marked as Analog or differential pseudo-ECL (PECL).

2. The RDAT[15:0], RPRTY, RSOC/RSOP, REOP, RMOD, RERR, RCA/RPA, RVAL, RCLK, RFPO, TCA/TPA, TCLK, TFPO, POUT[7:0], FPOUT and OOF outputs have a 8mA drive capability. The TDO and INTB outputs have a 2mA drive capability. All other digital outputs and bi-directional signals have 4mA drive capability.

3. The system interface inputs RFCLK, RENB, TFCLK, TENB, TDAT[15:0], TMOD, TERR, TSOC/TSOP, TEOP and TPRTY do not use the ESD bias voltages (VBIAS and PBIAS pins) and are 3.3V tolerate only. All other digital inputs (excluding inputs marked Analog), may operate with 5V signalling with appropriate ESD biasing.

4. The differential pseudo-ECL inputs and outputs should be terminated in a passive network and interface at PECL levels as described in the Operation section.

5. It is mandatory that every digital ground pin (VSS) be connected to the printed circuit board ground plane to ensure reliable device operation.

6. It is mandatory that every digital power pin (VDD) be connected to the printed circuit board power plane to ensure reliable device operation.

7. All analog power and ground pins can be sensitive to noise. They must be isolated from the digital power and ground. Care must be taken to correctly decouple these pins. Please refer to the Operation section and the S/UNI-622-POS reference design (PMC-981070) for more information.

8. Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to damage these ESD protection devices or trigger latch up. Please adhere to the recommended power supply sequencing as described in the Operation section of this document.

10 FUNCTIONAL DESCRIPTION

10.1 Receive Line Interface (CRSI-622)

The Receive Line Interface allows direct interface of the S/UNI-622-POS to optical modules (ODLs) or other medium interfaces. This block performs clock and data recovery on the incoming 622.08 Mbit/s data stream and SONET/SDH A1/A2 pattern framing.

Clock Recovery

The clock recovery unit recovers the clock from the incoming bit serial data stream and is compliant with SONET and SDH jitter tolerance requirements. The clock recovery unit utilizes a low frequency reference clock to train and monitor its clock recovery PLL. Under loss of transition conditions, the clock recovery unit continues to output a line rate clock that is locked to this reference for keep alive purposes. The clock recovery unit utilizes a 77.76 MHz reference clock. The clock recovery unit provides status bits that indicate whether it is locked to data or the reference and also supports diagnostic loopback and a loss of signal input that squelches normal input data.

Initially upon start-up, the PLL locks to the reference clock, REFCLK. When the frequency of the recovered clock is within 488 ppm of the reference clock, the PLL attempts to lock to the data. Once in data lock, the PLL reverts to the reference clock if no data transitions occur in 96 bit periods or if the recovered clock drifts beyond 488 ppm of the reference clock.

When the transmit clock is derived from the recovered clock (loop timing), the accuracy of the transmit clock is directly related to the REFCLK reference accuracy in the case of a loss of transition condition. To meet the Bellcore GR-253-CORE SONET Network Element free-run accuracy specification, the reference must be within +/-20 ppm. For LAN applications, the REFCLK accuracy may be relaxed to +/-50 ppm.

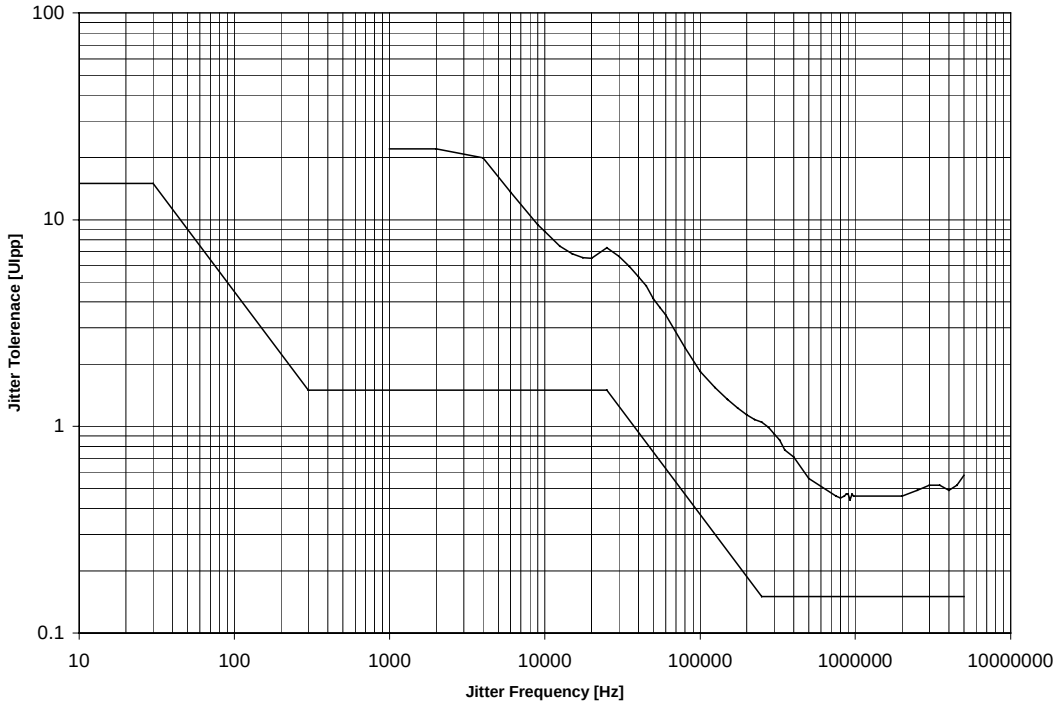
The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET/SDH data signal. The total loop dynamics of the clock recovery PLL yield a jitter tolerance that exceeds the minimum tolerance specified for SONET/SDH equipment by GR-253-CORE.

The typical jitter tolerance performance of the S/UNI-622-POS is shown in Figure 5 with the GR-253-CORE jitter tolerance specification limits. The jitter tolerance setup used a Hewlett Packard HFCT-5208M single-mode fiber optic transceiver

with approximately -10 dBm input power. A 47 nF capacitor was connected between the C0 and C1 pins on the device and the RTYPE register bit in CRSI-622 was set to logic one.

Note that for frequencies below 300Hz, the jitter tolerance is greater than 22 UIpp; 22UIpp is the maximum jitter tolerance of the test equipment. The dip in the jitter tolerance curve between 10 kHz and 30 kHz is due to the clock difference detector.

Figure 5: Typical STS-12c/STM-4-4c S/UNI-622-POS Jitter Tolerance



Serial to Parallel Converter

The Serial to Parallel Converter (SIPO) converts the received bit serial stream to a byte serial stream. The SIPO searches for the initial SONET/SDH framing pattern in the receive stream, and performs serial to parallel conversion on octet boundaries.

While out of frame, the CRSI-622 block monitors the bit-serial STS-12c/STM-4-4c data stream for an occurrence of a A1 byte. The CRSI-622 adjusts its byte alignment of the serial-to-parallel converter when three consecutive A1 bytes followed by three consecutive A2 bytes occur in the data stream. The CRSI

informs the RSOP Framer block when this framing pattern has been detected to reinitializes the RSOP to the new frame alignment.

While in frame, the CRSI-622 maintains the byte alignment of the serial-to-parallel converter until RSOP declares out of frame.

10.2 Receive Section Overhead Processor (RSOP)

The Receive Section Overhead Processor (RSOP) provides frame synchronization, descrambling, section level alarm and performance monitoring. In addition, it extracts the section data communication channel from the section overhead and provides it serially on output RSD.

Framer

The Framer Block determines the in-frame/out-of-frame status of the receive stream. While in-frame, the framing bytes (A1, A2) in each frame are compared against the expected pattern. Out-of-frame is declared when four consecutive frames containing one or more framing pattern errors have been received.

While out of frame, the CRSI-622 block monitors the bit-serial STS-12c/STM-4-4c data stream for an occurrence of the framing pattern (A1, A2). The CRSI-622 informs the RSOP Framer block when three A1 bytes followed by three A2 bytes has been detected to reinitializes the frame byte counter to the new alignment. The Framer block declares frame alignment on the next SONET/SDH frame when either all A1 and A2 bytes are seen error-free or when only the first A1 byte and the first four bits of the last A2 byte are seen error-free depending upon the selected framing algorithm.

Once in frame, the Framer block monitors the framing pattern sequence and declares out of frame (OOF) when one or more bit errors in each framing pattern are detected for four consecutive frames. Again, depending upon the algorithm either 24 framing bytes are examined for bit errors each frame, or only the first A1 byte and the first four bits of the last A2 byte are examined for bit errors each frame.

When the parallel line interface PIN[7:0] is used, upstream circuitry monitors the receive stream for an occurrence of the three A1 bytes followed by three A2 bytes framing pattern while out-of-frame. The upstream circuitry is expected to pulse input FPIN when the third A2 byte has been detected. RSOP monitors the receive data stream on PIN[7:0] for the framing pattern as before. Once in frame, RSOP monitors the framing pattern sequence and sets the OOF pin when one or more bit errors in each framing pattern are detected for four consecutive frames.

Descramble

The Descramble Block utilizes a frame synchronous descrambler to process the receive stream. The generating polynomial is $x^7 + x^6 + 1$ and the sequence length is 127. Details of the descrambling operation are provided in the references. Note that the framing bytes (A1 and A2) and the trace/growth bytes (J0/Z0) are not descrambled. A register bit is provided to disable the descrambling operation.

Data Link Extract

The Data Link Extract Block extracts the section data communication channel (bytes D1, D2, and D3) from the STS-12c/STM-4-4c stream. The extracted bytes are serialized and output on signal RSD at a nominal 192 kbit/s rate. Timing for downstream processing of the data communication channel is provided by the RSDCLK signal that is also output by the Data Link Extract Block. RSDCLK is derived from a 216 kHz clock that is gapped to yield an average frequency of 192 kHz. RSD is updated with timing aligned to RSDCLK.

Error Monitor

The Error Monitor Block calculates the received section BIP-8 error detection code (B1) based on the scrambled data of the complete STS-12c/STM-4-4c frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. The calculated BIP-8 code is compared with the BIP-8 code extracted from the B1 byte of the following frame. Differences indicate that a section level bit error has occurred. Up to 64000 (8 x 8000) bit errors can be detected per second. The Error Monitor Block accumulates these section level bit errors in a 16-bit saturating counter that can be read via the microprocessor interface. Circuitry is provided to latch this counter so that its value can be read while simultaneously resetting the internal counter to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that this counter be polled at least once per second so as not to miss bit error events.

Loss of Signal

The Loss of Signal Block monitors the scrambled data of the receive stream for the absence of 1's or 0's. When 20 ± 3 µs of all zeros patterns or all ones patterns are detected, a loss of signal (LOS) is declared. Loss of signal is cleared when two valid framing words are detected and during the intervening time, no loss of signal condition is detected. The LOS signal is optionally reported on the RALRM output pin when enabled by the LOSEN Receive Alarm Control Register bit.

Loss of Frame

The Loss of Frame Block monitors the in-frame / out-of-frame status of the Framer Block. A loss of frame (LOF) is declared when an out-of-frame (OOF) condition persists for 3 ms. The LOF is cleared when an in-frame condition persists for a period of 3 ms. To provide for intermittent out-of-frame (or in-frame) conditions, the 3 ms timer is not reset to zero until an in-frame (or out-of-frame) condition persists for 3 ms. The LOF and OOF signals are optionally reported on the RALRM output pin when enabled by the LOFEB and OOFEN Receive Alarm Control Register bits.

10.3 Receive Line Overhead Processor (RLOP)

The Receive Line Overhead Processor (RLOP) provides line level alarm and performance monitoring. In addition, it extracts the line data communication channel from the line overhead and provides it serially on output RLD.

Line RDI Detect

The Line RDI Detect Block detects the presence of Line Remote Defect Indication (LRDI) in the receive stream. Line RDI is declared when a 110 binary pattern is detected in bits 6, 7, and 8 of the K2 byte, for three or five consecutive frames. Line RDI is removed when any pattern other than 110 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The LRDI signal is optionally reported on the RALRM output pin when enabled by the LRDIEN Receive Alarm Control Register bit.

Line AIS Detect

The Line AIS Block detects the presence of a Line Alarm Indication Signal (LAIS) in the receive stream. Line AIS is declared when a 111 binary pattern is detected in bits 6, 7, and 8 of the K2 byte, for three or five consecutive frames. Line AIS is removed when any pattern other than 111 is detected in bits 6, 7, and 8 of the K2 byte for three or five consecutive frames. The LAIS signal is optionally reported on the RALRM output pin when enabled by the LAISEN Receive Alarm Control Register bit.

Data Link Extract Block

The Data Link Extract Block extracts the line data communication channel (bytes D4 to D12) from the STS-12c/STM-4-4c stream. The extracted bytes are serialized and output on the RLD output at a nominal 576 kbit/s rate. Timing for downstream processing of the data communication channel is provided by the

RLDCLK output. RLDLCLK is derived from a 2.16 MHz clock that is gapped to yield an average frequency of 576 kHz.

Error Monitor Block

The Error Monitor Block calculates the received line BIP-8 error detection codes based on the Line Overhead bytes and synchronous payload envelopes of the STS-12c/STM-4-4c stream. The line BIP-8 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 codes are compared with the BIP-8 codes extracted from the following frame. Any differences indicate that a line layer bit error has occurred. Optionally the RLOP can be configured to count a maximum of only one BIP error per frame.

This block also extracts the line FEBE code from the M1 byte. The FEBE code is contained in bits 2 to 8 of the M1 byte, and represents the number of line BIP-8 errors that were detected in the last frame by the far end. The FEBE code value has 97 legal values (0 to 96) for an STS-12c/STM-4-4c stream. Illegal values are interpreted as zero errors.

The Error Monitor Block accumulates B2 error events and FEBE events in two 20-bit saturating counters that can be read via the CBI. The contents of these counters may be transferred to internal holding registers by writing to any one of the counter addresses, or by using the TIP register bit feature. During a transfer, the counter value is latched and the counter is reset to 0 (or 1, if there is an outstanding event). Note, these counters should be polled at least once per second to avoid saturation.

The B2 error event counters optionally can be configured to accumulate only "word" errors. A B2 word error is defined as the occurrence of one or more B2 bit error events during a frame. The B2 error counter is incremented by one for each frame in which a B2 word error occurs.

In addition the FEBE events counters optionally can be configured to accumulate only "word" events. A FEBE word event is defined as the occurrence of one or more FEBE bit events during a frame. The FEBE event counter is incremented by one for each frame in which a FEBE event occurs. If the extracted FEBE value is in the range 1 to 4 the FEBE event counter will be incremented for each and every FEBE bit. If the extracted FEBE value is greater than 4 the FEBE event counter will be incremented by 4.

10.4 The Receive APS, Synchronization Extractor and Bit Error Monitor (RASE)

Automatic Protection Switch Control

The Automatic Protection Switch (APS) control block filters and captures the receive automatic protection switch channel bytes (K1 and K2) allowing them to be read via the RASE APS K1 Register and the RASE APS K2 Register. The bytes are filtered for three frames before being written to these registers. A protection switching byte failure alarm is declared when twelve successive frames have been received, where no three consecutive frames contain identical K1 bytes. The protection switching byte failure alarm is removed upon detection of three consecutive frames containing identical K1 bytes. The detection of invalid APS codes is done in software by polling the RASE APS K1 Register and the RASE APS K2 Register.

Bit Error Rate Monitor

The Bit Error Monitor Block (BERM) calculates the received line BIP-96 error detection code (B2) based on the line overhead and synchronous payload envelope of the receive data stream. The line BIP-96 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP code is compared with the BIP-96 code extracted from the B2 bytes of the following frame. Any differences indicate that a line layer bit error has occurred. Up to 768,000 (96 BIP/frame x 8000 frames/second) bit errors can be detected per second for STS-12c/STM-4-4c rate.

The BERM accumulates these line layer bit errors in a 20 bit saturating counter that can be read via the microprocessor interface. During a read, the counter value is latched and the counter is reset to 0 (or 1, if there is an outstanding event). Note, this counter should be polled at least once per second to avoid saturation that in turn may result in missed bit error events.

The BERM block is able to simultaneously monitor for signal fail (SF) or signal degrade (SD) threshold crossing and provide alarms through software interrupts. The bit error rates associated with the SF or SD alarms are programmable over a range of 10^{-3} to 10^{-9}. Details are provided in the Operation section.

Synchronization Status Extraction

The Synchronization Status Extraction (SSE) Block extracts the synchronization status (S1) byte from the line overhead. The SSE block can be configured to capture the S1 nibble after three or after eight frames with the same value (filtering turned on) or after any change in the value (filtering turned off). The S1 nibble can be read via the CBI interface.

10.5 Receive Path Overhead Processor (RPOP)

The Receive Path Overhead Processor (RPOP) provides pointer interpretation, extraction of path overhead, extraction of the synchronous payload envelope, and path level alarm indication and performance monitoring.

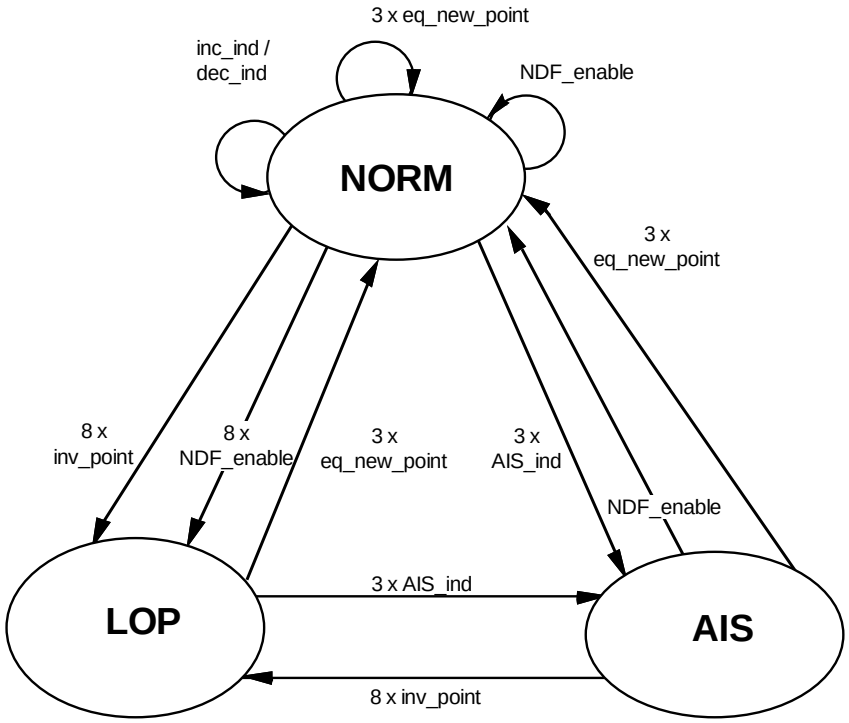
Pointer Interpreter

The Pointer Interpreter interprets the incoming pointer (H1, H2) as specified in the references. The pointer value is used to determine the location of the path overhead (the J1 byte) in the incoming STS-12c/STM-4-4c stream. The algorithm can be modeled by a finite state machine. Within the pointer interpretation algorithm three states are defined as shown below:

NORM_state (NORM)
AIS_state (AIS)
LOP_state (LOP)

The transition between states will be consecutive events (indications), e.g., three consecutive AIS indications to go from the NORM_state to the AIS_state. The kind and number of consecutive indications activating a transition is chosen such that the behavior is stable and insensitive to low BER. The only transition on a single event is the one from the AIS_state to the NORM_state after receiving a NDF enabled with a valid pointer value. It should be noted that, since the algorithm only contains transitions based on consecutive indications, this implies that, for example, non-consecutively received invalid indications do not activate the transitions to the LOP_state.

Figure 6: Pointer Interpretation State Diagram



The following table defines the events (indications) shown in the state diagram.

Table 1: Pointer Interpreter Event (Indications) Description

Event (Indication)	Description
norm_point	disabled NDF + ss + offset value equal to active offset
NDF_enable	enabled NDF + ss + offset value in range of 0 to 782 or enabled NDF + ss, if NDFPOR bit is set (Note that the current pointer is not updated by an enabled NDF if the pointer is out of range).
AIS_ind	H1 = 'hFF, H2 = 'hFF
inc_ind	disabled NDF + ss + majority of I bits inverted + no majority of D bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago
dec_ind	disabled NDF + ss + majority of D bits inverted + no majority of I bits inverted + previous NDF_enable, inc_ind or dec_ind more than 3 frames ago

inv_point	not any of above (i.e., not norm_point, and not NDF_enable, and not AIS_ind, and not inc_ind and not dec_ind)
new_point	disabled_NDF + ss + offset value in range of 0 to 782 but not equal to active offset
inc_req	majority of I bits inverted + no majority of D bits inverted
dec_req	majority of D bits inverted + no majority of I bits inverted

Note 1- active offset is defined as the accepted current phase of the SPE (VC) in the NORM_state and is undefined in the other states.

Note 2 - enabled NDF is defined as the following bit patterns: 1001, 0001, 1101, 1011, 1000.

Note 3 - disabled NDF is defined as the following bit patterns: 0110, 1110, 0010, 0100, 0111.

Note 4 - the remaining six NDF codes (0000, 0011, 0101, 1010, 1100, 1111) result in an inv_ndf indication.

Note 5 - ss bits are unspecified in SONET and has bit pattern 10 in SDH

Note 6 - the use of ss bits in definition of indications may be optionally disabled.

Note 7 - the requirement that previous NDF_enable, inc_ind or dec_ind be more than 3 frames ago may be optionally disabled.

Note 8 - new_point is also an inv_point.

Note 9 - LOP is not declared if all the following conditions exist:
- the received pointer is out of range (>782),
- the received pointer is static,
- the received pointer can be interpreted, according to majority voting on the I and D bits, as a positive or negative justification indication,
- after making the requested justification, the received pointer continues to be interpretable as a pointer justification.

When the received pointer returns to an in-range value, the S/UNI-622-POS will interpret it correctly.

Note 10 - LOP will exit at the third frame of a three frame sequence consisting of one frame with NDF enabled followed by two frames with NDF disabled, if all three pointers have the same legal value.

The transitions indicated in the state diagram are defined in the following table.

Table 2: Pointer Interpreter Transition Description

Transition	Description
inc_ind/dec_ind	offset adjustment (increment or decrement indication)
3 x eq_new_point	three consecutive equal new_point indications
NDF_enable	single NDF_enable indication
3 x AIS_ind	three consecutive AIS indications
8 x inv_point	eight consecutive inv_point indications
8 x NDF_enable	eight consecutive NDF_enable indications

Note 1 - the transitions from NORM_state to NORM_state do not represent state changes but imply offset changes.

Note 2 - 3 x new_point takes precedence over other events and if the IINVCNT bit is set resets the inv_point count.

Note 3 - all three offset values received in 3 x eq_new_point must be identical.

Note 4 - "consecutive event counters" are reset to zero on a change of state except for consecutive NDF count.

The Pointer Interpreter detects loss of pointer (LOP) in the incoming STS-12c/STM-4-4c stream. LOP is declared on entry to the LOP_state as a result of eight consecutive invalid pointers or eight consecutive NDF enabled indications. The alarm condition is reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local S/UNI-622-POS to insert a path RDI indication.

The Pointer Interpreter detects path AIS in the incoming STS-12c/STM-4-4c stream. PAIS is declared on entry to the AIS_state after three consecutive AIS indications. The alarm condition reported in the receive alarm port and is optionally returned to the source node by signaling the corresponding Transmit Path Overhead Processor in the local SONET/SDH equipment to insert a path RDI indication.

Invalid pointer indications (inv_point), invalid NDF codes, new pointer indications (new_point), discontinuous change of pointer alignment, and illegal pointer changes are also detected and reported by the Pointer Interpreter block via register bits. An invalid NDF code is any NDF code that does not match the NDF enabled or NDF disabled definitions. The third occurrence of equal new_point indications (3 x eq_new_point) is reported as a discontinuous change of pointer alignment event (DISCOPA) instead of a new pointer event and the active offset is updated with the receive pointer value. An illegal pointer change is defined as a inc_ind or dec_ind indication that occurs within three frames of the previous inc_ind, dec_ind or NDF_enable indications. Illegal pointer changes may be optionally disabled via register bits.

The active offset value is used to extract the path overhead from the incoming stream and can be read from an internal register.

SPE Timing

The SPE Timing Block provides SPE timing information to the Error Monitor and the Extract blocks. The block contains a free running timeslot counter that is initialized by a J1 byte identifier (which identifies the first byte of the SPE). Control signals are provided to the Error Monitor and the Extract blocks to identify the Path Overhead bytes and to downstream circuitry to extract the ATM cell or POS payload.

Error Monitor

The Error Monitor Block contains two 16-bit counters that are used to accumulate path BIP-8 errors (B3), and far end block errors (FEBEs). The contents of the two counters may be transferred to holding registers, and the counters reset under microprocessor control.

Path BIP-8 errors are detected by comparing the path BIP-8 byte (B3) extracted from the current frame, to the path BIP-8 computed for the previous frame.

FEBEs are detected by extracting the 4-bit FEBE field from the path status byte (G1). The legal range for the 4-bit field is between 0000 and 1000, representing zero to eight errors. Any other value is interpreted as zero errors.

Path RDI alarm is detected by extracting bit 5 of the path status byte. The PRDI signal is set high when bit 5 is set high for five/ten consecutive frames. PRDI is set low when bit 5 is low for five/ten consecutive frames. Auxiliary RDI alarm is detected by extracting bit 6 of the path status byte. The Auxiliary RDI alarm is indicated when bit 6 is set high for five/ten consecutive frames. The Auxiliary RDI alarm is removed when bit 6 is low for five/ten consecutive frames. The

Enhanced RDI alarm is detected when the enhanced RDI code in bits 5,6,7 of the path status byte indicates the same error codepoint for five/ten consecutive frames. The Enhanced RDI alarm is removed when the enhanced RDI code in bits 5,6,7 of the path status byte indicates the same non error codepoint for five/ten consecutive frames. The ERDII maskable interrupt is set high when bits 5, 6 & 7 of the path status byte (G1) byte are set to a new codepoint for five or ten consecutive frames. The ERDIV[2:0] signal reflects the state of the filtered ERDI value (G1 byte bits 5, 6, & 7).

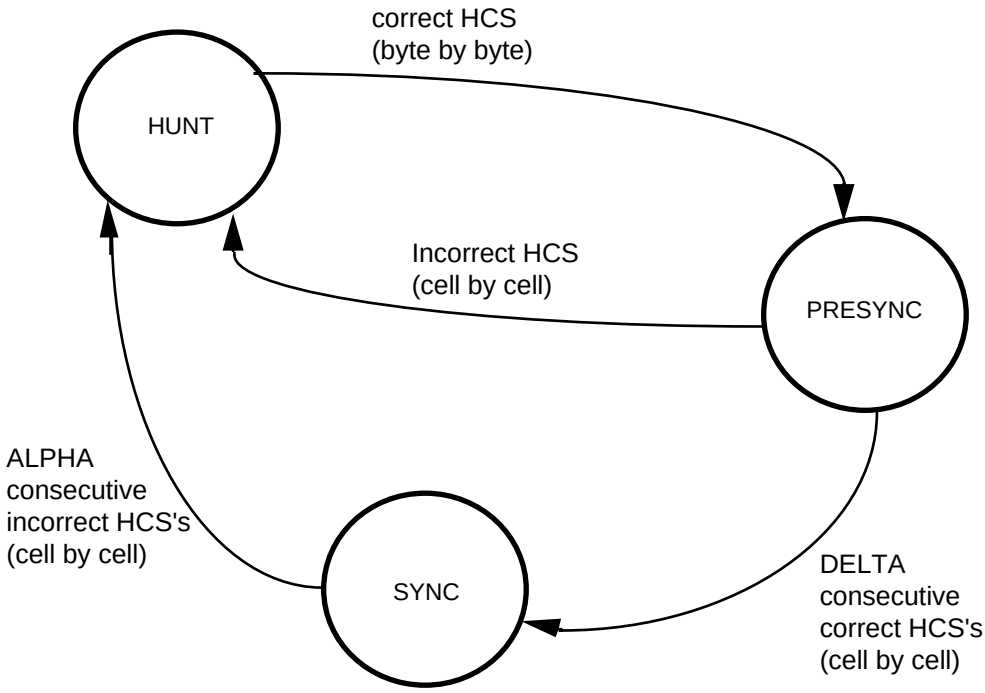
10.6 Receive ATM Cell Processor (RXCP)

The Receive ATM Cell Processor (RXCP) performs ATM cell delineation, provides cell filtering based on idle/unassigned cell detection and HCS error detection, and performs ATM cell payload descrambling. The RXCP also provides a four-cell deep receive FIFO. This FIFO is used to separate the STS-12c/STM-4-4c line timing from the higher layer ATM system timing.

Cell Delineation

Cell Delineation is the process of framing to ATM cell boundaries using the header check sequence (HCS) field found in the cell header. The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. When performing delineation, correct HCS calculations are assumed to indicate cell boundaries. Cells are assumed to be byte-aligned to the synchronous payload envelope. The cell delineation algorithm searches the 53 possible cell boundary candidates individually to determine the valid cell boundary location. While searching for the cell boundary location, the cell delineation circuit is in the HUNT state. When a correct HCS is found, the cell delineation state machine locks on the particular cell boundary, corresponding to the correct HCS, and enters the PRESYNC state. The PRESYNC state validates the cell boundary location. If the cell boundary is invalid, an incorrect HCS will be received within the next DELTA cells, at which time a transition back to the HUNT state is executed. If no HCS errors are detected in this PRESYNC period, the SYNC state is entered. While in the SYNC state, synchronization is maintained until ALPHA consecutive incorrect HCS patterns are detected. In such an event a transition is made back to the HUNT state. The state diagram of the delineation process is shown in Figure 5.

Figure 7: Cell Delineation State Diagram



The values of ALPHA and DELTA determine the robustness of the delineation process. ALPHA determines the robustness against false misalignments due to bit errors. DELTA determines the robustness against false delineation in the synchronization process. ALPHA is chosen to be 7 and DELTA is chosen to be 6. These values result in an average time to delineation of 8 µs for the STS-12c/STM-4-4c rate.

Descrambler

The self-synchronous descrambler operates on the 48 byte cell payload only. The circuitry descrambles the information field using the $x^{43} + 1$ polynomial. The descrambler is disabled for the duration of the header and HCS fields and may optionally be disabled for the payload.

Cell Filter and HCS Verification

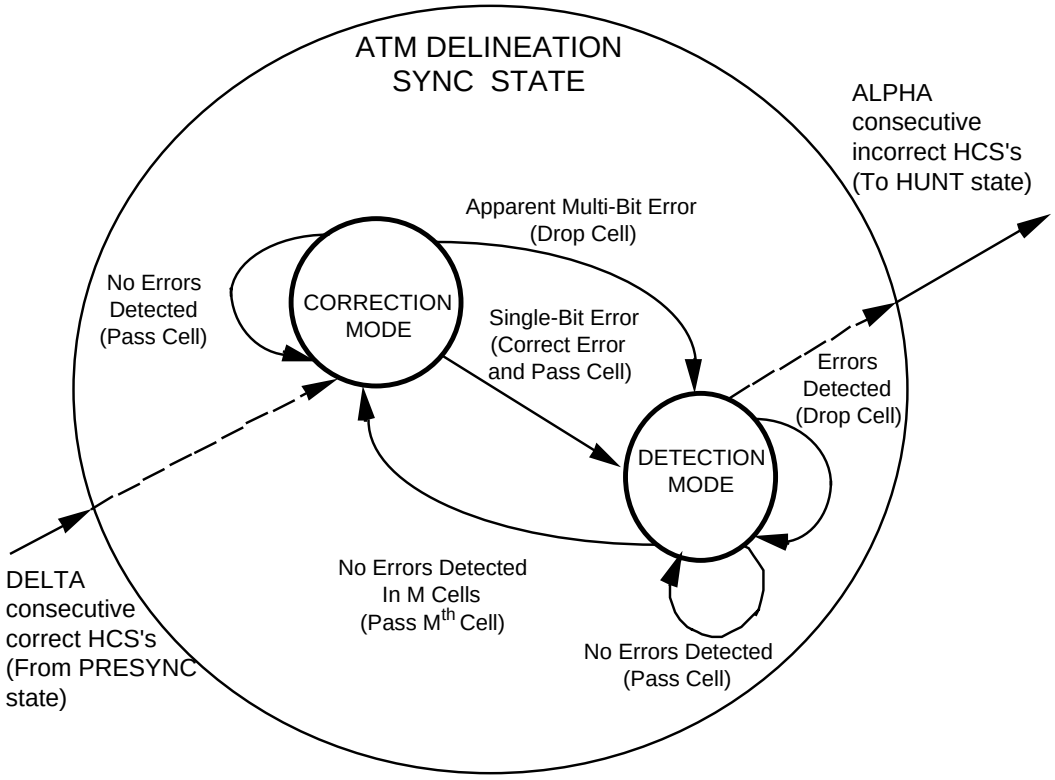
Cells are filtered (or dropped) based on HCS errors and/or a cell header pattern. Cell filtering is optional and is enabled through the RXCP registers. Cells are passed to the receive FIFO while the cell delineation state machine is in the SYNC state as described above. When both filtering and HCS checking are enabled, cells are dropped if uncorrectable HCS errors are detected, or if the

corrected header contents match the pattern contained in the RXCP Match Header Pattern and RXCP Match Header Mask registers. Idle or unassigned cell filtering is accomplished by writing the appropriate cell header pattern into the RXCP Match Header Pattern and RXCP Match Header Mask registers. Idle/Unassigned cells are assumed to contain the all zeros pattern in the VCI and VPI fields. The RXCP Match Header Pattern and RXCP Match Header Mask registers allow filtering control over the contents of the GFC, PTI, and CLP fields of the header.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RXCP block verifies the received HCS using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial, $x^6 + x^4 + x^2 + 1$, is added (modulo 2) to the received HCS octet before comparison with the calculated result. While the cell delineation state machine in Figure 7 is in the SYNC state, the HCS verification circuit implements the state machine shown in Figure 8.

In normal operation, the HCS verification state machine remains in the 'Correction Mode' state. Incoming cells containing no HCS errors are passed to the receive FIFO. Incoming single-bit errors are corrected, and the resulting cell is passed to the FIFO. Upon detection of a single-bit error or a multi-bit error, the state machine transitions to the 'Detection Mode' state. In this state, programmable HCS error filtering is provided. The detection of any HCS error causes the corresponding cell to be dropped. The state machine transitions back to the 'Correction Mode' state when M (where M = 1, 2, 4, 8) cells are received with correct HCSs. The Mth cell is not discarded.

Figure 8: HCS Verification State Diagram



Performance Monitor

The Performance Monitor consists of two 8-bit saturating HCS error event counters and a 24-bit saturating receive cell counter. The first error counter accumulates correctable HCS errors, which are HCS single-bit errors, detected and corrected while the HCS Verification state machine is in the 'Correction Mode' state. The second error counter accumulates uncorrectable HCS errors, which are HCS bit errors detected while the HCS Verification state machine is in the 'Detection Mode' state or HCS bit errors detected but not corrected while the state machine is in the 'Correction Mode' state. The 24-bit receive cell counter counts all cells written into the receive FIFO. Filtered cells are not counted.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, if appropriate, so that a new period of accumulation can begin without loss of any events. It is intended that the counter be polled at least once per second so as not to miss any counted events.

Receive FIFO

The Receive FIFO block contains storage for 4 cells, along with management circuitry for reading and writing the FIFO. The receive FIFO provides for the separation of the physical layer timing from the system timing.

Receive FIFO management functions include filling the receive FIFO, indicating when cells are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun conditions. Upon detection of an overrun, the FIFO discards the current cell and discards the incoming cells until there is room in the FIFO. FIFO overruns are indicated through a maskable interrupt and register bit and are considered a system error.

10.7 Receive POS Frame Processor (RXFP)

The Receive POS Frame Processor (RXFP) performs packet extraction, provides FCS error correction, performs packet payload descrambling, and provides performance monitoring functions. The RXFP also provides a 256 byte deep receive FIFO. This FIFO is used to separate the STS-12c/STM-4-4c line timing from the link layer system timing and to handle timing differences caused by the removal of escape characters.

Overhead Removal

The overhead removal consists of stripping SONET/SDH overhead bytes from the data stream. Once overhead bytes are removed, the data stream consists of POS frame octets that can be fed directly to the descrambler or the POS Frame Delineation block.

Descrambler

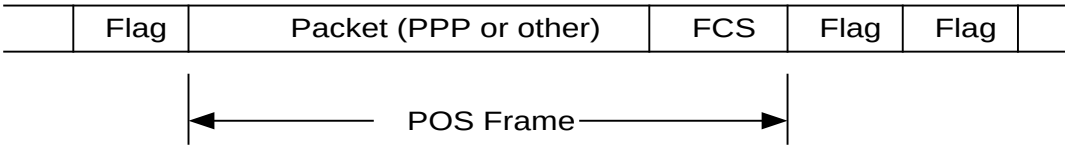
When enabled, the self-synchronous descrambler operates on the POS Frame data, descrambling the data with the polynomial $x^{43} + 1$. Descrambling is performed on the raw data stream, before any POS frame delineation or byte destuffing is performed. Data scrambling can provide for a more robust system, preventing the injection of hostile patterns into the data stream.

POS Frame Delineation

This block accepts data one byte at a time and arranges it as POS framed octets. Frame boundaries are found by searching for the Flag Character (0x7E). Flags are also used to fill inter-packet spacing. This block removes the Flag Sequence and passes the data onto the Byte Destuffing block.

The POS Frame Delineation is performed on the descrambled data and consists of arranging the POS framed octets. Frame boundaries are found by searching for the Flag Character (0x7E). Flags are also used to fill inter-packet spacing. This block removes the Flag Sequence and passes the data onto the Byte Destuffing block. The POS Frame format is shown on Figure 9.

Figure 9: Packet Over SONET/SDH Frame Format



In the event of a FIFO overflow caused by the FIFO being full while a packet is being received, the packet is marked with an error so it can be discarded by the system. Subsequent bytes associated with this now aborted frame are discarded. Reception of POS data resumes when a Start of Packet is encountered and the FIFO level is below the programmable Reception Initialization Level (RIL[7:0]).

Byte Destuffing

The byte destuffing algorithm searches the Control Escape character (0x7D). These characters, listed in Table 3, are added for transparency in the transmit direction and must be removed to recover the user data. When the Control Escape character is encountered, it is removed and the following data byte is XORed with 0x20. Therefore, any escaped data byte will be processed properly by the S/UNI-622-POS.

Table 3: HDLC Byte Sequences

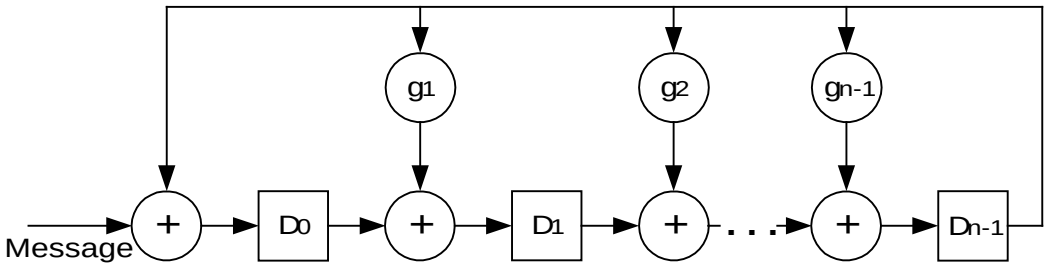
Data Value	Sequence
0x7E (Flag Sequence)	0x7D 0x5E
0x7D (Control Escape)	0x7D 0x5D
HDLC Aborted Packet	0x7D 0x7E

FCS Check

The FCS Generator performs a CRC-CCITT or CRC-32 calculation on the whole POS frame, after byte destuffing and data descrambling scrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-CCITT or CRC-32 function. The CRC-CCITT is two bytes in size and has a generating polynomial $g(x) = 1 + x^5 +$

$x^{12} + x^{16}$. The CRC-32 is four bytes in size and has a generating polynomial g(x) = $1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$. The first FCS bit transmitted is the coefficient of the highest term. Packets with FCS errors are marked as such and should be discarded by the system.

Figure 10: CRC Decoder



Performance Monitor

The Performance Monitor consists of four 16-bit saturating error event counters and one 24-bit saturating received good packet counter. One of the error event counters accumulates FCS errors. The second error event counter accumulates minimum length violation packets. The third error event counter accumulates maximum length violation packets. The fourth error event counter accumulates aborted packets. The 24-bit receive good packet counter counts all error free packets.

Each counter may be read through the microprocessor interface. Circuitry is provided to latch these counters so that their values can be read while simultaneously resetting the internal counters to 0 or 1, whichever is appropriate, so that a new period of accumulation can begin without loss of any events. The counters should be polled at least once per second so error events will not be missed.

The RXFP monitors the packets for both minimum and maximum length errors. When a packet size is smaller than MINPL[7:0], the packet is marked with an error but still written into the FIFO. Malformed packets, that is packets that do not at least contain the FCS field plus one byte, are treated differently. If a malformed packet is received and FCS stripping is enabled, the packet is discarded, not written in the FIFO, and counted as a minimum packet size violation. If a malformed packet is received and FCS stripping is disabled, it is written into the FIFO since in this case the misformed packet criteria is reduced to one byte, but will still count as a minimum packet size violation. When the

packet size exceeds MAXPL[15:0] the packet is marked with an error and the bytes beyond the maximum count are discarded.

Receive FIFO

The Receive FIFO block contains storage for 256 octets, along with management circuitry for reading and writing the FIFO. The receive FIFO provides for the separation of the physical layer timing from the system timing.

Receive FIFO management functions include filling the receive FIFO, indicating when packets or bytes are available to be read from the receive FIFO, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun conditions. Upon detection of an overrun, the FIFO aborts the current packet and discards the current incoming bytes until there is room in the FIFO. Once enough room is available, as defined by the RIL[7:0] register, the RXFP will wait for the next start of packet before writing any data into the FIFO. FIFO overruns are indicated through a maskable interrupt and register bit, and are considered a system error.

10.8 Transmit Line Interface (CSPI-622)

The Transmit Line Interface allows to directly interface the S/UNI-622-POS with optical modules (ODLs) or other medium interfaces. This block performs clock synthesis and performs parallel to serial conversion on the incoming outgoing 622.08 Mbit/s data stream.

Clock Synthesis

The transmit clock is synthesized from a 77.76 MHz reference by the clock synthesis unit (CSU). The transfer function yields a typical low pass corner of 1 MHz, above which reference jitter is attenuated at least 20 dB per octave. The design of the loop filter and PLL is optimized for minimum intrinsic jitter. With a jitter free 77.76 MHz reference, the intrinsic jitter is typically less than 0.07 UI RMS when measured using a high pass filter with a 12 kHz cutoff frequency.

The REFCLK reference should be within ±20 ppm to meet the SONET/SDH free-run accuracy requirements specified in GR-253-CORE. The CSU may require a software reset when the supply voltage drops below the minimum operating level. See the CSPI-622 register description for more information.

Parallel to Serial Converter

The Parallel to Serial Converter (PISO) converts the transmit byte serial stream to a bit serial stream. The transmit bit serial stream appears on the TXD+/-

PECL output. When the parallel transmit interface mode is used, the PISO block is not used.

10.9 Transmit Section Overhead Processor (TSOP)

The Transmit Section Overhead Processor (TSOP) provides frame pattern insertion (A1, A2), scrambling, section level alarm signal insertion, and section BIP-8 (B1) insertion. In addition, it inserts the section data communication channel provided serially on input TSD.

Line AIS Insert

Line AIS insertion results in all bits of the SONET/SDH frame being set to 1 before scrambling except for the section overhead. The Line AIS Insert Block substitutes all ones as described when enabled by the TLAIS input or through an internal register accessed through the microprocessor interface. Activation or deactivation of line AIS insertion is synchronized to frame boundaries.

Data Link Insert

The Data Link Insert Block inserts the section data communication channel (bytes D1, D2, and D3) into the STS-12c/STM-4-4c stream when enabled by an internal register accessed via the common bus interface. The bytes to be inserted are serially input on signal TSLD at a nominal 192 kbit/s rate. Timing for upstream processing of the data communication channel is provided by the TSDCLK signal that is output by the Data Link Insert Block. TSDCLK is derived from a 216 kHz clock that is gapped to yield an average frequency of 192 kHz. TSD is sampled with timing aligned to TSDCLK.

BIP-8 Insert

The BIP-8 Insert Block calculates and inserts the BIP-8 error detection code (B1) into the transmit stream.

The BIP-8 calculation is based on the scrambled data of the complete STS-12c/STM-4-4c frame. The section BIP-8 code is based on a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-8 code is then inserted into the B1 byte of the following frame before scrambling. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

Framing and Identity Insert

The Framing and Identity Insert Block inserts the framing bytes (A1, A2) and trace/growth bytes (J0/Z0) into the STS-12c/STM-4-4c frame. Framing bit errors may be continuously inserted under register control for diagnostic purposes.

Scrambler

The Scrambler Block utilizes a frame synchronous scrambler to process the transmit stream when enabled through an internal register accessed via the microprocessor interface. The generating polynomial is $x^7 + x^6 + 1$. Precise details of the scrambling operation are provided in the references. Note that the framing bytes and the identity bytes are not scrambled. All zeros may be continuously inserted (after scrambling) under register control for diagnostic purposes.

The POUT[7:0] outputs are provided by the Scrambler block and are updated with timing aligned to TCLK. It also provides the FPOUT signal.

10.10 Transmit Line Overhead Processor (TLOP)

The Transmit Line Overhead Processor (TLOP) provides line level alarm signal insertion, and line BIP-96 insertion (B2). In addition, it inserts the line data communication provided serially on input TLD.

APS Insert

The APS Insert Block inserts the two automatic protection switch (APS) channel bytes in the Line Overhead (K1 and K2) into the transmit stream when enabled by an internal register.

Data Link Insert

The Data Link Insert Block inserts the line data communication channel (DCC) (bytes D4 to D12) into the STS-12c/STM-4-4c stream when enabled by an internal register. The D4 to D12 bytes are input serially using the TLD signal at a nominal 576 kbit/s rate. Timing for processing of the line DCC is provided by the TLDCLK output. TLDCLK is derived from a 2.16 MHz clock that is gapped to yield an average frequency of 576 kHz.

Line BIP Calculate

The Line BIP Calculate Block calculates the line BIP-96 error detection code (B2) based on the line overhead and synchronous payload envelope of the transmit

stream. The line BIP-96 code is a bit interleaved parity calculation using even parity. Details are provided in the references. The calculated BIP-96 code is inserted into the B2 byte positions of the following frame. BIP-96 errors may be continuously inserted under register control for diagnostic purposes.

Line RDI Insert

The Line RDI Insert Block controls the insertion of line remote defect indication. Line RDI insertion is enabled through register control. Line RDI is inserted by transmitting the code 110 (binary) in bit positions 6, 7, and 8 of the K2 byte contained in the transmit stream.

Line FEBE Insert

The Line FEBE Insert Block accumulates line BIP-96 errors (B2) detected by the Receive Line Overhead Processor and encodes far end block error indications in the transmit Z2 byte.

10.11 Transmit Path Overhead Processor (TPOP)

The Transmit Path Overhead Processor (TPOP) provides transport frame alignment generation, pointer generation (H1, H2), path overhead insertion and the insertion of path level alarm signals.

Pointer Generator

The Pointer Generator Block generates the outgoing payload pointer (H1, H2) as specified in the references. The concatenation indication (the NDF field set to 1001, I-bits and D-bits set to all ones, and unused bits set to all zeros) is inserted in the second and third pointer byte locations in the transmit stream.

(1) A "normal pointer value" locates the start of the SPE. Note: $0 \leq$ "normal pointer value" ≤ 782, and the new data flag (NDF) field is set to 0110. Note that values greater than 782 may be inserted, using internal registers, to generate a loss of pointer alarm in downstream circuitry.

(2) Arbitrary "pointer values" may be generated using internal registers. These new values may optionally be accompanied by a programmable new data flag. New data flags may also be generated independently using internal registers.

(3) Positive pointer movements may be generated using a bit in an internal register. A positive pointer movement is generated by inverting the five I-bits of the pointer word. The SPE is not inserted during the positive stuff opportunity

byte position, and the pointer value is incremented by one. Positive pointer movements may be inserted once per frame for diagnostic purposes.

(4) Negative pointer movements may be generated using a bit in an internal register. A negative pointer movement is generated by inverting the five D-bits of the pointer word. The SPE is inserted during the negative stuff opportunity byte position, the H3 byte, and the pointer value is decremented by one. Negative pointer movements may be inserted once per frame for diagnostic purposes.

The pointer value is used to insert the path overhead into the transmit stream. The current pointer value may be read via internal registers.

BIP-8 Calculate

The BIP-8 Calculate Block performs a path bit interleaved parity calculation on the SPE of the transmit stream. Details are provided in the references. The resulting parity byte is inserted in the path BIP-8 (B3) byte position of the subsequent frame. BIP-8 errors may be continuously inserted under register control for diagnostic purposes.

FEBE Calculate

The FEBE Calculate Block accumulates far end block errors on a per frame basis, and inserts the accumulated value (up to maximum value of eight) in the FEBE bit positions of the path status (G1) byte. The FEBE information is derived from path BIP-8 errors detected by the receive path overhead processor, RPOP. Far end block errors may be inserted under register control for diagnostic purposes.

10.12 Transmit ATM Cell Processor (TXCP)

The Transmit ATM Cell Processor (TXCP) provides rate adaptation via idle/unassigned cell insertion, provides HCS generation and insertion, and performs ATM cell scrambling. The TXCP contains a four cell transmit FIFO. An idle or unassigned cell is transmitted if a complete ATM cell has not been written into the FIFO.

Transmit FIFO

The Transmit FIFO is responsible for holding cell provided through the Transmit System Interface until they are transmitted. The transmit FIFO can accommodate a maximum of 4 cells. The cells are written in with a single 16 bit data bus running off TFCLK and are read out using the SONET/SDH clock. Internal read and write pointers track the cells and indicate the fill status of the

Transmit FIFO. Separate read and write clock domains provide for separation of the physical layer line timing from the System Link layer timing (TFCLK).

Idle/Unassigned Cell Generator

The Idle/Unassigned Cell Generator inserts idle or unassigned cells into the cell stream when enabled. Registers are provided to program the GFC, PTI, and CLP fields of the idle cell header and the idle cell payload. The idle cell HCS is automatically calculated and inserted.

Scrambler

The Scrambler scrambles the 48 octet information field. Scrambling is performed using a parallel implementation of the self-synchronous scrambler ($x^{43} + 1$ polynomial). The cell headers are transmitted unscrambled, and the scrambler may optionally be disabled.

HCS Generator

The HCS Generator performs a CRC-8 calculation over the first four header octets. A parallel implementation of the polynomial, x^8+x^2+x+1, is used. The coset polynomial, $x^6+x^4+x^2+1$, is added (modulo 2) to the residue. The HCS Generator optionally inserts the result into the fifth octet of the header.

10.13 Transmit POS Frame Processor (TXFP)

The Transmit POS Frame Processor (TXFP) provides rate adaptation by transmitting flag sequences (0x7E) between packets, provides FCS generation and insertion, performs packet data scrambling, and provides performance monitoring functions. The TXFP contains a 256 byte transmit FIFO. This FIFO is used to separate the STS-12c/STM-4-4c line timing from the link layer system timing and to handle timing differences caused by insertion of escape characters.

Transmit FIFO

The Transmit FIFO is responsible for holding packets provided through the Input Interface until they are transmitted. The transmit FIFO can accommodate a maximum of 256 bytes. There is no limit on the number of packets that can be stored. Octets are written in with a single 16 bit data bus running off TFCLK and are read out with a single 8-bit data bus running off the SONET/SDH clock. Separate read and write clock domains provide for separation of the physical layer line timing from the system link layer timing (TFCLK).

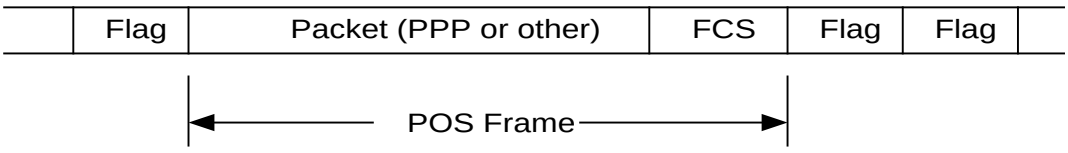
Internal read and write pointers track the insertion and removal of octets, and indicate the fill status of the Transmit FIFO. These status indications are used to detect underrun and overrun conditions, abort packets as appropriate on both system and line sides, control flag insertion and to generate the TPA outputs.

The TXFP does not abort packets under an FIFO overrun condition. The corrupted packet will be send with properly calculated FCS if the FCS feature is enabled. Since overruns can be avoided by setting the FIFO high and low watermarks, this limitation should not affect system performance.

POS Frame Generator

The POS Frame Generator runs off of the SONET/SDH sequencer to create the POS frames to be transmitted, whose format is shown in Figure 9. Flags are inserted whenever the Transmit FIFO is empty and there is no data to transmit. When there is enough data to be transmitted, the block operates normally; it removes packets from the Transmit FIFO and transmits them. In addition, FCS generation, error insertion, byte stuffing, and scrambling can be optionally enabled.

Figure 11: Packet Over SONET/SDH Frame Format



In the event of a FIFO underflow caused by the FIFO being empty while a packet is being transmitted, the packet is aborted by transmitting the Abort Sequence. The Abort Sequence consists of an Escape Control character (0x7D) followed by the Flag Sequence (0x7E). Bytes associated with this aborted frame are still read from the FIFO but are discarded and replaced with the Flag Sequence in the outgoing data stream. Transmission of data resumes a start of the next packet is encountered in the FIFO data stream.

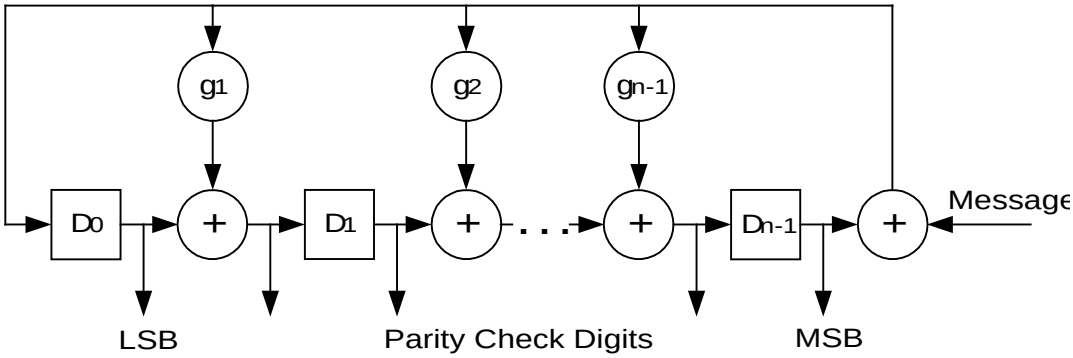
The POS Frame Generator also performs inter-packet gaping. This operation consists of inserting a programmable number of Flag Sequence characters between each POS frame transmission. This feature allows to control the system effective data transmission rate if required.

For correct operation, the TXFP only supports packets ranging in size from 2 bytes to 65534 bytes in length.

FCS Generator

The FCS Generator performs a CRC-CCITT or CRC-32 calculation on the whole POS frame, before byte stuffing and data scrambling. A parallel implementation of the CRC polynomial is used. The CRC algorithm for the frame checking sequence (FCS) field is either a CRC-CCITT or CRC-32 function. The CRC-CCITT is two bytes in size and has a generating polynomial $g(x) = 1 + x^5 + x^{12} + x^{16}$. The CRC-32 is four bytes in size and has a generating polynomial $g(x) = 1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$. The first FCS bit transmitted is the coefficient of the highest term. When transmitting a packet from the Transmit FIFO, the FCS Generator appends the result after the last data byte, before the closing flag. Note that the Frame Check Sequence is the one's complement of the CRC register after calculation ends. FCS calculation and insertion can be disabled.

Figure 12: CRC Generator



An error insertion mechanism is provided for system diagnosis purposes. Error insertion is performed by inverting the resulting FCS value, before transmission. This should cause an FCS Error at the far end.

Byte Stuffing

The POS Frame generator provides transparency by performing byte stuffing. This operation is done after the FCS calculation. Two characters are being escaped, the Flag Sequence (0x7E) and the Escape Character itself (0x7D). When a character is being escaped, it is XORed with 0x20 before transmission and preceded by the Control Escape (0x7D) character.

Table 4: HDLC Byte Sequences

Data Value	Sequence
0x7E (Flag Sequence)	0x7D 0x5E
0x7D (Control Escape)	0x7D 0x5D
HDLC Abort Sequence	0x7D 0x7E

Data Scrambling

The Scrambler will optionally scramble the whole packet data, including the FCS and the flags. Scrambling is performed after the POS frame is formed using a parallel implementation of the self-synchronous scrambler polynomial, $x^{43}+1$. On reset, the scrambler is set to all ones to ensure scrambling on start-up. The scrambler may optionally be completely disabled. Data scrambling can provide for a more robust system preventing the injection of hostile patterns into the data stream.

SONET/SDH Framer

The SONET/SDH Framer gaps the POS frames in order to insert the SONET/SDH framing and overhead bytes (Section/Line Overhead and Path Overhead). The framer uses framing alignment information provided by the TPOP TSB to perform its function. The TXFP does not set any SONET/SDH overhead bytes.

10.14 SONET/SDH Path Trace Buffer (SPTB)

The SONET/SDH Section Trace Buffer (SPTB) block can handle both 64-byte CLLI messages in SONET and 16-byte E.164 messages in SDH. This block operates similarly to the SONET/SDH Section Trace Buffer (SSTB).

Receive Trace Message Receiver

The Trace Message Receiver (TMR) processes the receive trace message, and consists of three sub-processes: Framer, Persistency, and Compare.

The Framer handles the incoming 16-byte message by synchronizing to the byte with the most significant bit set high, and places that byte in the first location in the capture page of the internal RAM. In the case of the 64-byte message, the Framer synchronizes to the trailing carriage return (0x0D), line feed (0x0A) sequence and places the next byte in the first location in the capture page of the internal RAM. The Framer block maintains an internal representation of the resulting 16-byte or 64-byte "frame" cycle. If the phase of the start of frame

shifts, the framer adjusts accordingly and resets the persistency counter and increments the unstable counter. Frame synchronization may be disabled, in which case the RAM acts as a circular buffer.

The Persistency process checks for repeated reception of the same 16-byte or 64-byte trace message. An unstable counter is incremented for each message that differs from the previous received message. For example, a single corrupted message in a field of constant messages causes the unstable count to increment twice, once on receipt of the corrupted message, and again on the next (uncorrupted) message. A section/path trace message unstable alarm is declared when the count reaches eight.

The persistency counter is reset to zero, the unstable alarm is removed, and the trace message is accepted when the same 16-byte or 64-byte message is received three or five times consecutively (as determined by an internal register bit). The accepted message is passed to the Compare process for comparison with the expected message.

A receive trace message mismatch alarm is declared if the accepted message (i.e. the message that passed the persistency check) does not match the expected message (previously downloaded to the receive expected page by the microprocessor). The mismatch alarm is removed if the accepted message is all-zero, or if the accepted message is identical to the expected message.

Overhead Byte Receiver

The Overhead Byte Receiver (OBR) processes the path signal label byte (C2)The OBR consists of two sub-processes: Persistency and Compare.

The Persistency process checks for the repeated reception of the same C2 byte. An unstable counter is incremented for each received C2 byte that differs from the byte received in the previous frame. For example, a single corrupted byte value in a sequence of constant values causes the unstable count to increment twice, once on receipt of the corrupted value, and again on the next (uncorrupted) value. A path signal label unstable alarm or a synchronization status unstable alarm is declared when either unstable counter reaches five.

The unstable counter is reset to zero, the unstable alarm is removed, and the byte value is accepted when the same label is received in five consecutive frames. The accepted value is passed to the Compare process for comparison with the expected value.

A path signal label mismatch alarm or a synchronization status mismatch alarm is declared if the accepted C2 byte (i.e. the byte value that has passed the

persistency check) does not match the expected C2 byte (previously downloaded by the microprocessor).

The OBR mismatch mechanism follows the table below:

Table 5: OBR Mismatch Mechanism

Expect	Receive	Action
00	00	Match
00	01	Mismatch
00	XX	Mismatch
01	00	Mismatch
01	01	Match
01	XX	Match
XX	00	Mismatch
XX	01	Match
XX	XX	Match
XX	YY	Mismatch

Note: XX, YY are equal to anything except 00H or 01H and are not equal to each other.

Transmit Trace Buffer

The Trace Transmit Buffer (TTB) sources the 16-byte or 64-byte trace identifier message. The TTB contains one page of transmit trace identifier message memory. Identifier message data bytes are written by the microprocessor into the message buffer and inserted in the transmit stream. When the microprocessor is updating the transmit page buffer, the TTB may be programmed to transmit null characters to prevent transmission of partial messages.

10.15 SONET/SDH Section Trace Buffer (SSTB)

The SONET/SDH Section Trace Buffer (SSTB) block can handle both 64-byte CLLI messages in SONET and 16-byte E.164 messages in SDH. This block operates similarly to the SONET/SDH Path Trace Buffer (SPTB) except the C2 byte is also processed.

Receive Trace Message Receiver

The Trace Message Receiver (TMR) processes the receive trace message, and consists of three sub-processes: Framer, Persistency, and Compare.

The Framer handles the incoming 16-byte message by synchronizing to the byte with the most significant bit set high, and places that byte in the first location in the capture page of the internal RAM. In the case of the 64-byte message, the Framer synchronizes to the trailing carriage return (0x0D), line feed (0x0A) sequence and places the next byte in the first location in the capture page of the internal RAM. The Framer block maintains an internal representation of the resulting 16-byte or 64-byte "frame" cycle. If the phase of the start of frame shifts, the framer adjusts accordingly and resets the persistency counter and increments the unstable counter. Frame synchronization may be disabled, in which case the RAM acts as a circular buffer.

The Persistency process checks for repeated reception of the same 16-byte or 64-byte trace message. An unstable counter is incremented for each message that differs from the previous received message. For example, a single corrupted message in a field of constant messages causes the unstable count to increment twice, once on receipt of the corrupted message, and again on the next (uncorrupted) message. A section/path trace message unstable alarm is declared when the count reaches eight.

The persistency counter is reset to zero, the unstable alarm is removed, and the trace message is accepted when the same 16-byte or 64-byte message is received three or five times consecutively (as determined by an internal register bit). The accepted message is passed to the Compare process for comparison with the expected message.

A receive trace message mismatch alarm is declared if the accepted message (i.e. the message that passed the persistency check) does not match the expected message (previously downloaded to the receive expected page by the microprocessor). The mismatch alarm is removed if the accepted message is all-zero, or if the accepted message is identical to the expected message.

Transmit Trace Buffer (TTB)

The TTB sources the 16-byte or 64-byte trace identifier message. The TTB contains one page of transmit trace identifier message memory. Identifier message data bytes are written by the microprocessor into the message buffer and inserted in the transmit stream. When the microprocessor is updating the transmit page buffer, the TTB may be programmed to transmit null characters to prevent transmission of partial messages.

10.16 ATM UTOPIA and Packet over SONET/SDH POS-PHY System Interfaces

The S/UNI-622-POS system interface can be configured for ATM or POS mode. When configured for ATM applications, the system interface provides either a UTOPIA level 2 compliant bus or a UTOPIA Level 3 compatible bus to allow the transfer of ATM cells between the ATM layer device and the S/UNI-622-POS. When configured for POS applications, the system interface provides either a POS-PHY Level 2 or POS-PHY Level 3 compliant bus and provides a byte level transfer interface that allows the transfer of data packets between the link layer device and the S/UNI-622-POS. The link layer device can implement various protocols, including PPP.

10.16.1 Receive ATM Interface

The Receive ATM FIFO (RXCP) provides FIFO management at the S/UNI-622-POS receive cell interface. The receive FIFO contains four cells. The FIFO provides the cell rate decoupling function between the transmission system physical layer and the ATM layer.

In general, the management functions include filling the receive FIFO, indicating when the receive FIFO contains cells, maintaining the receive FIFO read and write pointers, and detecting FIFO overrun and underrun conditions.

UTOPIA Level 2 Interface

The UTOPIA Level 2 compliant interface accepts a read clock (RFCLK) and read enable signal (RENB). The interface indicates the start of a cell (RSOC) and the receive cell available status (RCA) when data is read from the receive FIFO (using the rising edges of RFCLK). The RCA status changes from available to unavailable when the FIFO is either empty (when RCALEVEL0 is high) or near empty (when RCALEVEL0 is low). This interface also indicates FIFO overruns via a maskable interrupt and register bits. Read accesses while RCA is a logic zero will output invalid data. The FIFO is reset on FIFO overrun, causing up to 4 cells to be lost.

UTOPIA Level 3 Interface

The UTOPIA Level 3 compliant interface accepts a read clock (RFCLK) and read enable signal (RENB). The interface indicates the start of a cell (RSOC) when data is read from the receive FIFO (using the rising edges of RFCLK). The RVAL signal indicates when data on the receive data bus RDAT[7:0] is valid. The RPRTY signal reports the parity on the RDAT[7:0] bus (selectable as odd or even parity). RVAL will not assert until RENB is asserted. This interface also indicates FIFO overruns via a maskable interrupt and register bits. Read accesses while

RVAL is low are ignored and will output invalid data. The FIFO is reset on FIFO overrun, causing up to 4 cells to be lost.

10.16.2 Receive POS Interface

The Receive POS FIFO (RXFP) provides FIFO management at the S/UNI-622-POS receive packet interface. The receive FIFO contains 256 bytes. The FIFO provides the system rate decoupling function between the transmission system physical layer and the link layer, and to handle timing differences caused by the removal of escape characters.

The interface can be configured either as a 16-bit POS-PHY Level 2 compliant interface, or as an 8-bit POS-PHY Level 3 compliant interface.

POS-PHY Level 2

The POS-PHY Level 2 Interface is an extension to the UTOPIA interface defined for the transfer of ATM cells.

The RSOP signal is used to identify the start of a packet, the RPA signal notifies the system side that data is in the receive FIFO (when a programmable number of bytes in a single packet is received or when an end of packet is available); the RDATA[15:0] bus transfer the data from the FIFO across the system interface; the RPRTY signal determines the parity on the RDAT bus (selectable as odd or even parity); the RFCLK is used to read words from the FIFO interface; and the RENB is used to initiate reads from the receive FIFO. Signal REOP (Receive End of Packet) is used to identify the end of a packet. Signal RMOD (Receive Mod) is provided to indicate whether 1 or 2 bytes are valid on the final word transfer when in 16-bit mode (REOP is asserted). Signal RERR (Receive Error) is provided to indicate that an error in the received packet has occurred (may have several causes, including an abort sequence and an FCS error).

The receive data valid signal, RVAL, plays a special role in this interface. The data signals shall be considered valid only when RVAL is asserted. RVAL is asserted when a data transfer is initiated, conditional to RPA being also asserted. Once the transfer is initiated, RVAL will remain asserted until either the FIFO is empty or an end of packet is encountered. Once deasserted, RVAL will remain low until the current PHY is deselected and another or the same PHY is reselected. RVAL allows the link layer device to align data transfers with packet boundaries, making it easier to manage packet buffers. RVAL should be used at all times when RENB is low to qualify the receive data stream due to RPA falsely indicating data in the FIFO. See the Functional Timing section for more information.

POS-PHY Level 3

The POS-PHY Level 3 compliant interface is an extension to the POS-PHY Level 2 Interface.

The interface accepts a read clock (RFCLK) and read enable signal (RENB) when data is read from the receive FIFO (using the rising edge of the RFCLK). The start of packet RSOP marks the first byte of receive packet data on the RDAT[7:0]. The RPRTY signal determine the parity on the RDAT[7:0] bus (selectable as odd or even parity). The end of a packet is indicated by the REOP signal. Signal RERR is provided to indicate that an error in the received packet has occurred (the error may have several causes include an abort sequence or an FCS error).

The RVAL signal is used to indicate when RSOP, REOP, RERR and RDAT[7:0] are valid. This interface also indicates FIFO overruns via a maskable interrupt and register bits. Read accesses while RVAL is low are ignored and will output invalid data. RVAL will not assert until RENB is asserted.

10.16.3 Transmit ATM Interface

The ATM Transmit FIFO (TXCP) provides FIFO management and the S/UNI-622-POS transmit cell interface. The transmit FIFO contains four cells. The FIFO depth may be programmed to four, three, two, or one cells. The FIFO provides the cell rate decoupling function between the transmission system physical layer and the ATM layer.

In general, the management functions include emptying cells from the transmit FIFO, indicating when the transmit FIFO is full, maintaining the transmit FIFO read and write pointers and detecting a FIFO overrun condition.

The interface can be configured either as a 16-bit UTOPIA Level 2 interface, or as an 8-bit UTOPIA Level 3 interface.

UTOPIA Level 2 Interface

The UTOPIA Level 2 compliant interface accepts a write clock (TFCLK), a write enable signal (TENB), the start of a cell (TSOC) indication, and the parity bit (TPRTY), when data is written to the transmit FIFO (using the rising edges of TFCLK). The interface provides the transmit cell available status (TCA) which can transition from "available" to "unavailable" when the transmit FIFO is near full (when TCALEVEL0 is low) or when the FIFO is full (when TCALEVEL0 is high) and can accept no more writes. To reduce FIFO latency, the FIFO depth at which TCA indicates "full" can be set to one, two, three or four cells by the FIFODP[1:0]

bits of the TXCP Configuration 2 register. If the programmed depth is less than four, more than one cell may be written after TCA is asserted as the TXCP still allows four cells to be stored in its FIFO.

This interface also indicates FIFO overruns via a maskable interrupt and register bit, but write accesses while TCA is low are not processed. The TXCP automatically transmits idle cells until a full cell is available to be transmitted.

UTOPIA Level 3 Interface

The UTOPIA Level 3 compliant interface accepts a write clock (TFCLK), a write enable signal (TENB), the start of a cell (TSOC) indication and the parity bit (TPRTY) when data is written to the transmit FIFO (using the rising edges of the TFCLK). To reduce FIFO latency, the FIFO depth at which TCA indicates “full” can be set to one, two, three or four cells by the FIFODP[1:0] bits of the TXCP Configuration 2 register. If the programmed depth is less than four, more than one cell may be written after TCA is asserted as the TXCP still allows four cells to be stored in its FIFO.

The interface also indicates FIFO overruns via a maskable interrupt and register bits. The TXCP automatically transmits idle cells until a full cell is available to be transmitted.

10.16.4 Transmit POS Interface

The Transmit POS FIFO (RXFP) provides FIFO management at the S/UNI-622-POS transmit packet interface. The transmit FIFO contains 256 bytes. The FIFO provides the system rate decoupling function between the transmission system physical layer and the link layer, and to handle timing differences caused by the insertion of escape characters.

POS-PHY Level 2 Interface

The POS-PHY Level 2 Interface is an extension to the UTOPIA 2 interface defined for the transfer of ATM cells. POS-PHY byte-level transfer mode is supported.

The TSOP signal is used to identify the start of a packet; the TPA signal notify the system side that the transmit FIFO is not full (the POS processor will not start transmitting a packet until a programmable number of bytes for a single packet or the entire packet is in the FIFO; the TDAT[15:0] bus transfer the data to the FIFO from the system interface; the TPRTY signal determines the parity on the TDAT bus (selectable as odd or even parity); the TFCLK is used to write words to the FIFO interface; and finally the TENB is used to initiate writes to the transmit

FIFO. The TXCP automatically transmits idle flag characters until sufficient data is available in the transmit FIFO to start transmission.

The TEOP signal (Transmit End of Packet) is used to identify the end of a packet. The TMOD signal (Transmit Mod) is provided to indicate whether 1 or 2 bytes are valid of the final word transfer (TEOP is asserted). TMOD is only valid in 16-bit mode of operation. The TERR signal (Transmit Error) is provided to error a packet that has begun transmission (the packet will be aborted).

POS-PHY Level 3 Interface

The POS-PHY Level 3 compliant interface accepts a write clock (TFCLK), a write enable signal (TENB), the start of packet (TSOP) indication, the end of packet (TEOP) indication, errored packet (TERR) indication and the parity bit (TPRTY) when data is written to the transmit FIFO (using the rising edges of the TFCLK). The TPA signal notifies that the transmit FIFO is not full (the POS processor will not start transmitting a packet until a programmable number of bytes for a single packet or the entire packet is in the FIFO). A packet may be aborted by asserting the TERR signal at the end of the packet.

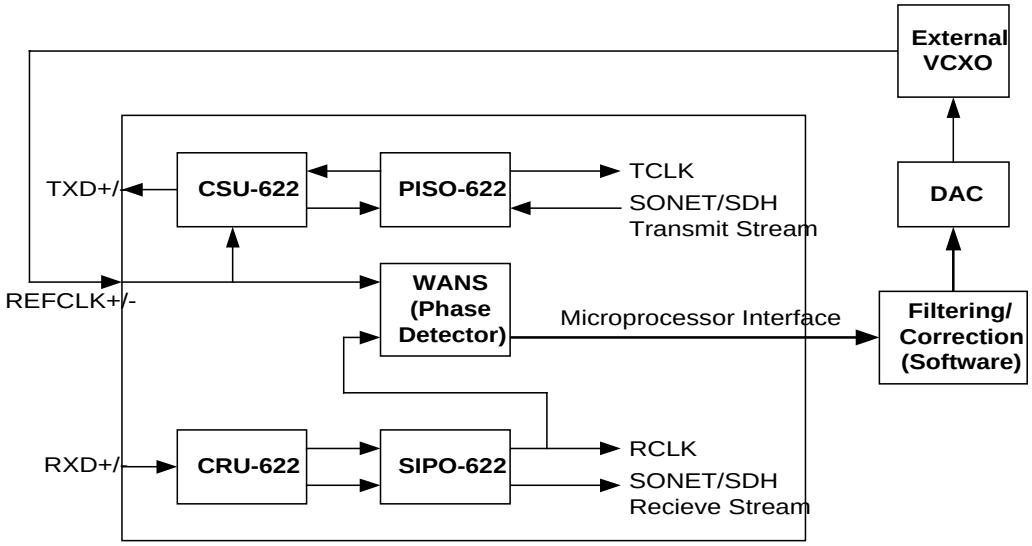
The interface also indicates FIFO overruns via a maskable interrupt and register bits. The TXCP automatically transmits idle flag characters until sufficient data is available in the transmit FIFO to start transmission.

10.17 WAN Synchronization Controller (WANS)

The WANS provides hardware support to implement a local clock reference compliant to SONET/SDH Stratum 3 clock specifications (GR-253-CORE & GR-1244-CORE) in wander transfer, long term and holdover stability. The WANS block is intended to be used in conjunction with an external processor, digital to analog converter (DAC), analog circuitry and voltage control crystal oscillator (VCXO).

In general, WANS block implements the phase detector of a phase lock loop structure which relies on an external processor and a VCXO to produce the Stratum 3 clock as shown in Figure 13. The WANS performs a digital phase comparison between the recovered receive clock (receive line rate clock RCLK from the CRU-622) and the reference clock used to generate the transmit stream (REFCLK+/- supplied by the VCXO).

Figure 13. WANS PLL Block Diagram



The software running on the external processor is responsible for performing: digital loop filtering, temperature compensation, VCXO linearity compensation; determining the validity of the timing reference; and performing reference switchover. The VCXO creates the 77.76 MHz Stratum 3 reference clock which the CSU-622 will synthesize to the desired 622.08 MHz transmit clock.

Thus, the WANS PLL structure can phase lock the SONET/SDH transmit serial stream to the SONET/SDH receive serial stream. With appropriate software filtering and compensation, the device may meet SONET/SDH Stratum 3 clock specifications (GR-253-CORE & GR-1244-CORE) in wander transfer, long term and holdover stability.

A description of how to program and use the WANS feature is available in the S/UNI-622-POS reference design (PMC-981070). A description of the functionality supplied by the WANS block is given below.

Phase Comparison

The phase comparison between the receive recovered clock (RCLK) and the transmit reference clock (REFCLK+/-) is implemented by sampling, at a fixed interval specified by the Reference Counter, the output of the Phase Counter. The Reference Counter is clocked by RCLK while the Phase Counter is clocked by the REFCLK+/- clock.

Successive reading of the value obtained, referred as the phase sample (PHSAMP), can be used to calculate the phase relation between both clocks. Both the Reference Counter and the Phase Counter are programmable counters

and are set to have equal cycle period. Therefore, if REFCLK+/- was phased locked to RCLK, successive readings of the phase sample would be equal. The phase sample value will increase or decrease depending if REFCLK+/- is faster or slower than RCLK.

At each reference period, a signal enabling the sampling (SAMPLEN) of the Phase Counter is produced. This signal is resynchronized to REFCLK+/- to avoid any potential metastability problem that could result due to the asynchronous nature of both clocks.

Phase Reacquisition Control

The Phase Reacquisition Control circuit prevents using the phase sample from both sides of the counter wrap-around point when performing the Phase Sample averaging. The Phase Count is first divided in four quadrants, each equal to approximately a quarter of the Phase Count. Comparators are used to determine in which quadrant each phase sample is located. When two successive samples (one in the first quadrant and the other in the last quadrant) are seen, the Reference Phase Alignment Flag (RPHALFLG) is generated.

Upon reception of this signal, the Phase Counter is reset to align the phase count sampling point towards its middle count. This signal is also sent to the Phase Averager circuit. The generation of this signal may be squelched by setting the AUTOREAC bit of the WANS configuration register.

Phase Averager

To provide some noise immunity and improve the resolution of the phase detector algorithm of the WANS, the phase samples are averaged over a programmable number of samples.

Although referred to as an averaging process, it is truly an accumulation process. It retains full resolution, i.e. no division is performed on the accumulated value. The Phase Word includes an integer and a fractional part. The number of averaging samples sets the size of the fractional part.

A programmable counter, the Sample Counter, is incremented at each SAMPLEN signal. This Sample Counter defines the Phase Averaging Period, equal to the Reference Period times the programmed number of phase samples. At the end of this period, the accumulated phase sample value is transferred to the Phase Word register. The Phase Word (PHAWORD) is then accessible by an external processor. A timer flag (TIMFLG) is raised at the end of each averaging period. The flag may be used to generate an interrupt request to an external processor.

Because it indicates that the averaging process includes invalid sample values, the RPHALFLG signal also prevents the Phase Word register from being updated at the end of the current Phase Averaging period. The RPHAFLG signal indicates this event by sending the Reference Phase Alignment condition signal (RPHALGN) to the CBI status register. The RPHALGN signal is reset at the end of the following valid Phase Averaging period.

10.18 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The S/UNI-622-POS identification code is 0x353570CD hexadecimal.

10.19 Microprocessor Interface

The microprocessor interface block provides normal and test mode registers, and the logic required to connect to the microprocessor interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the S/UNI-622-POS. In the following section every register is documented and identified using the register number (REG #). Addresses that are not shown are not used and must be treated as Reserved.

Table 6: Register Memory Map

Address	Register Description
000	S/UNI-622-POS Master Reset and Identity
001	S/UNI-622-POS Master Configuration #1
002	S/UNI-622-POS Master Configuration #2
003	S/UNI-622-POS Clock Monitors
004	S/UNI-622-POS Master Interrupt Status #1
005	S/UNI-622-POS Master Interrupt Status #2
006	S/UNI-622-POS APS Control and Status
007	S/UNI-622-POS Miscellaneous Configuration
008	S/UNI-622-POS Auto Line RDI Control
009	S/UNI-622-POS Auto Path RDI Control
00A	S/UNI-622-POS Auto Enhanced Path RDI Control
00B	S/UNI-622-POS Receive RDI and Enhanced RDI Control
00C	S/UNI-622-POS Receive Line AIS Control
00D	S/UNI-622-POS Receive Path AIS Control
00E	S/UNI-622-POS Receive Alarm Control #1
00F	S/UNI-622-POS Receive Alarm Control #2

Address	Register Description
010	RSOP Control/Interrupt Enable
011	RSOP Status/Interrupt Status
012	RSOP Section BIP-8 LSB
013	RSOP Section BIP-8 MSB
014	TSOP Control
015	TSOP Diagnostic
016	TSOP Reserved
017	TSOP Reserved
018	RLOP Control/Status
019	RLOP Interrupt Enable/Interrupt Status
01A	RLOP Line BIP-96 LSB
01B	RLOP Line BIP-96
01C	RLOP Line BIP-96 MSB
01D	RLOP Line FEBE LSB
01E	RLOP Line FEBE
01F	RLOP Line FEBE MSB
020	TLOP Control
021	TLOP Diagnostic
022	TLOP Transmit K1
023	TLOP Transmit K2
024	TLOP Transmit Synchronization Message (S1)
025	TLOP Transmit J0/Z0
026	Reserved
027	Reserved
028	SSTB Control
029	SSTB Section Trace Identifier Status
02A	SSTB Indirect Address Register
02B	SSTB Indirect Data Register
02C	SSTB Reserved
02D	SSTB Reserved
02E	SSTB Reserved
02F	SSTB Reserved
030	RPOP Status/Control (EXTD=0)
030	RPOP Status/Control (EXTD=1)
031	RPOP Interrupt Status (EXTD=0)
031	RPOP Interrupt Status (EXTD=1)
032	RPOP Pointer Interrupt Status
033	RPOP Interrupt Enable (EXTD=0)
033	RPOP Interrupt Enable (EXTD=1)
034	RPOP Pointer Interrupt Enable
035	RPOP Pointer LSB

Address	Register Description
036	RPOP Pointer MSB
037	RPOP Path Signal Label
038	RPOP Path BIP-8 LSB
039	RPOP Path BIP-8 MSB
03A	RPOP Path FEBE LSB
03B	RPOP Path FEBE MSB
03C	RPOP RDI
03D	RPOP Ring Control
03E	RPOP Reserved
03F	RPOP Reserved
040	TPOP Control/Diagnostic
041	TPOP Pointer Control
042	TPOP Reserved
043	TPOP Current Pointer LSB
044	TPOP Current Pointer MSB
045	TPOP Arbitrary Pointer LSB
046	TPOP Arbitrary Pointer MSB
047	TPOP Path Trace
048	TPOP Path Signal Label
049	TPOP Path Status
04A	TPOP Reserved
04B	TPOP Reserved
04C	TPOP Reserved
04D	TPOP Reserved
04E	TPOP Concatenation LSB
04F	TPOP Concatenation MSB
050	SPTB Control
051	SPTB Path Trace Identifier Status
052	SPTB Indirect Address Register
053	SPTB Indirect Data Register
054	SPTB Expected Path Signal Label
055	SPTB Path Signal Label Status
056	SPTB Reserved
057	SPTB Reserved
058	CSPI Configuration
059	CSPI Status
05A	CSPI Reserved
05B	CSPI Reserved
05C	CRSI Configuration
05D	CRSI Status
05E	CRSI Reserved

Address	Register Description
05F	CRSI Reserved
060	RXCP Configuration 1
061	RXCP Configuration 2
062	RXCP FIFO/UTOPIA Control and Configuration
063	RXCP Interrupt Enable and Counter Status
064	RXCP Status/Interrupt Status
065	RXCP LCD Count Threshold LSB
066	RXCP LCD Count Threshold MSB
067	RXCP Idle Cell Header Pattern
068	RXCP Idle Cell Header Mask
069	RXCP Corrected HCS Error Count
06A	RXCP Uncorrected HCS Error Count
06B	RXCP Received Cell Count LSB
06C	RXCP Received Cell Count
06D	RXCP Received Cell Count MSB
06E	RXCP Idle Cell Count LSB
06F	RXCP Idle Cell Count
070	RXCP Idle Cell Count MSB
071	RXCP Reserved
072	RXCP Reserved
073	RXCP Reserved
074	RXCP Reserved
075	RXCP Reserved
076	RXCP Reserved
077	RXCP Reserved
078	RXCP Reserved
079	RXCP Reserved
07A	RXCP Reserved
07B	RXCP Reserved
07C	RXCP Reserved
07D	RXCP Reserved
07E	RXCP Reserved
07F	RXCP Reserved
080	TXCP Configuration 1
081	TXCP Configuration 2
082	TXCP Transmit Cell Status
083	TXCP Interrupt Enable/Status
084	TXCP Idle Cell Header Control
085	TXCP Idle Cell Payload Control
086	TXCP Transmit Cell Counter LSB
087	TXCP Transmit Cell Counter

Address	Register Description
088	TXCP Transmit Cell Counter MSB
089	TXCP Reserved
08A	TXCP Reserved
08B	TXCP Reserved
08C	TXCP Reserved
08D	TXCP Reserved
08E	TXCP Reserved
08F	TXCP Reserved
090	RUL3 Configuration
091	RUL3 Reserved
092	TUL3 Configuration
093	TUL3 Reserved
095	DLL RFCLK
096	DLL RFCLK
097	DLL RFCLK
098	DLL TFCLK
099	DLL TFCLK
09A	DLL TFCLK
09B	DLL TFCLK
09C	DLL PTCLK
09D	DLL PTCLK
09E	DLL PTCLK
09F	DLL PTCLK
0A0	RXFP Configuration
0A1	RXFP Configuration/Interrupt Enable
0A2	RXFP Interrupt Status
0A3	RXFP Minimum Packet Length
0A4	RXFP Maximum Packet Length LSB
0A5	RXFP Maximum Packet Length MSB
0A6	RXFP Receive Initiation Level
0A7	RXFP Receive Packet Available High Mark
0A8	RXFP Receive Byte Counter LSB
0A9	RXFP Receive Byte Counter
0AA	RXFP Receive Byte Counter
0AB	RXFP Receive Byte Counter MSB
0AC	RXFP Receive Frame Counter LSB
0AD	RXFP Receive Frame Counter
0AE	RXFP Receive Frame Counter MSB
0AF	RXFP Aborted Frame Count LSB
0B0	RXFP Aborted Frame Count MSB
0B1	RXFP FCS Error Frame Count LSB

Address	Register Description
0B2	RXFP FCS Error Frame Count MSB
0B3	RXFP Minimum Length Frame Count LSB
0B4	RXFP Minimum Length Frame Count MSB
0B5	RXFP Maximum Length Frame Count LSB
0B6	RXFP Maximum Length Frame Count MSB
0B7	RXFP Reserved
0B8	RXFP Reserved
0B9	RXFP Reserved
0BA	RXFP Reserved
0BB	RXFP Reserved
0BC	RXFP Reserved
0BD	RXFP Reserved
0BE	RXFP Reserved
0BF	RXFP Reserved
0C0	TXFP Interrupt Enable/Status
0C1	TXFP Configuration
0C2	TXFP Control
0C3	TXFP Transmit Packet Available Low Water Mark
0C4	TXFP Transmit Packet Available High Water Mark
0C5	TXFP Transmit Byte Count LSB
0C6	TXFP Transmit Byte Count
0C7	TXFP Transmit Byte Count
0C8	TXFP Transmit Byte Count MSB
0C9	TXFP Transmit Frame Count LSB
0CA	TXFP Transmit Frame Count
0CB	TXFP Transmit Frame Count MSB
0CC	TXFP Transmit User Aborted Frame Count LSB
0CD	TXFP Transmit User Aborted Frame Count MSB
0CE	TXFP Transmit Underrun Aborted Frame Count LSB
0CF	TXFP Transmit Underrun Aborted Frame Count MSB
0D0	WANS Configuration
0D1	WANS Interrupt and Status
0D2	WANS Phase Word LSB
0D3	WANS Phase Word
0D4	WANS Phase Word
0D5	WANS Phase Word MSB
0D6	WANS Reserved
0D7	WANS Reserved
0D8	WANS Reserved
0D9	WANS Reference Period LSB
0DA	WANS Reference Period MSB

Address	Register Description
0DB	WANS Phase Counter Period LSB
0DC	WANS Phase Counter Period MSB
0DD	WANS Phase Average Period
0DE	WANS Reserved
0DF	WANS Reserved
0E0	RASE Interrupt Enable
0E1	RASE Interrupt Status
0E2	RASE Configuration/Control
0E3	RASE SF BERM Accumulation Period LSB
0E4	RASE SF BERM Accumulation Period
0E5	RASE SF BERM Accumulation Period MSB
0E6	RASE SF BERM Saturation Threshold LSB
0E7	RASE SF BERM Saturation Threshold MSB
0E8	RASE SF BERM Declaring Threshold LSB
0E9	RASE SF BERM Declaring Threshold MSB
0EA	RASE SF BERM Clearing Threshold LSB
0EB	RASE SF BERM Clearing Threshold MSB
0EC	RASE SD BERM Accumulation Period LSB
0ED	RASE SD BERM Accumulation Period
0EE	RASE SD BERM Accumulation Period MSB
0EF	RASE SD BERM Saturation Threshold LSB
0F0	RASE SD BERM Saturation Threshold MSB
0F1	RASE SD BERM Declaring Threshold LSB
0F2	RASE SD BERM Declaring Threshold MSB
0F3	RASE SD BERM Clearing Threshold LSB
0F4	RASE SD BERM Clearing Threshold MSB
0F5	RASE Receive K1
0F6	RASE Receive K2
0F7	RASE Receive Z1/S1
0F8	Reserved
0F9	Reserved
0FA	Reserved
0FB	Reserved
0FC	S/UNI-622-POS Concatenation Status and Enable
0FD	S/UNI-622-POS Concatenation Interrupt Status
0FE	Reserved
0FF	Reserved
100	S/UNI-622-POS Master Test Register
101 -- 1FF	Reserved for Test

Notes on Register Memory Map:

- For all register accesses, CSB must be low.
- Addresses that are not shown must be treated as Reserved.
- A[8] is the test resister select (TRS) and should be set low for normal mode register access.

11 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the S/UNI-622-POS. Normal mode registers (as opposed to test mode registers) are selected when TRS (A[8]) is low.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. All configuration bits that can be written into can also be read back. This allows the processor controlling the S/UNI-622-POS to determine the programming state of the block.

3. Writable normal mode register bits are cleared to logic zero upon reset unless otherwise noted.

4. Writing into read-only normal mode register bit locations does not affect S/UNI-622-POS operation unless otherwise noted. Performance monitoring counter registers are a common exception.

5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the S/UNI-622-POS operates as intended, reserved register bits must be written with their default value as indicated by the register bit description.

6. Writing any data to the Master Reset and Identity register (0x00) simultaneously loads all the performance monitoring registers in RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP and TXFP blocks in the device.

   Writing any data to the performance register in question may individually trigger the performance registers in each block. In some cases, all performance registers in the block are loaded. In other cases, only the specific register being written will load. See the register descriptions for the performance register in question for more information.

Register 0x00: S/UNI-622-POS Master Reset and Identity

Bit	Type	Function	Default
Bit 7	R/W	RESET	0
Bit 6	R	TYPE[3]	0
Bit 5	R	TYPE[2]	0
Bit 4	R	TYPE[1]	1
Bit 3	R	TYPE[0]	1
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	1
Bit 0	R	ID[0]	0

This register allows the revision number of the S/UNI-622-POS to be read by software permitting graceful migration to newer, feature-enhanced versions of the S/UNI-622-POS.

In addition, writing to this register simultaneously loads all the performance monitor registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks.

ID[2:0]:

The ID bits can be read to provide a binary S/UNI-622-POS revision number.

TYPE[3:0]:

The TYPE bits can be read to distinguish the S/UNI-622-POS from the other members of the S/UNI family of devices.

RESET:

The RESET bit allows the S/UNI-622-POS to be reset under software control. If the RESET bit is a logic one, the entire S/UNI-622-POS is held in reset. This bit is not self-clearing. Therefore, a logic zero must be written to bring the S/UNI-622-POS out of reset. Holding the S/UNI-622-POS in a reset state places it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus negating the software reset. Otherwise, the effect of a software reset is equivalent to that of a hardware reset.

Register 0x01: S/UNI-622-POS Master Configuration #1

Bit	Type	Function	Default
Bit 7	R/W	TPTBEN	0
Bit 6	R/W	TSTBEN	0
Bit 5	R/W	SDH_J0/Z0	0
Bit 4	R/W	TFPEN	1
Bit 3	R/W	DLE	0
Bit 2	R/W	PDLE	0
Bit 1	R/W	PCM	0
Bit 0	R	TIP	X

TIP:

The TIP bit is set to a logic one when the performance meter registers are being loaded. Writing to the S/UNI-622-POS Master Reset and Identity register initiates an accumulation interval transfer and loads all the performance meter registers in the RSOP, RLOP, RPOP, SSTB, SPTB, RXCP, TXCP, RXFP and TXFP blocks.

TIP remains high while the transfer is in progress, and is set to a logic zero when the transfer is complete. TIP can be polled by a microprocessor to determine when the accumulation interval transfer is complete.

PCM:

The pointer concatenation mode select (PCM) determines the number of H1/H2 pointer pairs used to determine loss of pointer concatenation (LOPC) and pointer AIS (AISC). When PCM is set high, all H1/H2 pointer pairs are processed. When PCM is set low, only four H1/H2 pointer pairs (corresponding to the active STM-4-4c pointers) are processed.

PDLE:

The Parallel Diagnostic Loopback, PDLE bit enables the S/UNI-622-POS diagnostic loopback where the S/UNI-622-POS's Transmit Section Overhead Processor (TSOP) is directly connected to its Receive Section Overhead Processor (RSOP). When PDLE is logic one, loopback is enabled. Under this operating condition, the S/UNI-622-POS continues to operate normally in the transmit direction. When PDLE is logic zero, the S/UNI-622-POS operates normally in both directions.

DLE:

The Diagnostic Loopback, DLE bit enables the S/UNI-622-POS diagnostic loopback where the S/UNI-622-POS's Transmit ATM and POS Processors (TXCP and TXFP respectively) are directly connected to the Receive ATM and POS Processor (RXCP and RXFP respectively). When DLE is logic one, loopback is enabled. Under this operating condition, the S/UNI-622-POS does not operate normally in the transmit direction or receive direction. When DLE is logic zero, the S/UNI-622-POS operates normally.

TFPEN:

The Transmit Frame Pulse Enable (TFPEN) enables the TFPI input. When TFPEN is set low, the TFPI input is disabled. When TFPEN is set high, the TFPI input is enabled.

SDH_J0/Z0

The SDH_J0/Z0 bit selects whether to insert SONET or SDH format J0/Z0 section overhead bytes into the transmit stream. When SDH_J0/Z0 is set high, SDH format J0/Z0 bytes are selected for insertion. For this case, all the J0/Z0 bytes are forced to the value programmed in the S/UNI-622-POS Transmit J0/Z0 register. When SDH_J0/Z0 is set low, SONET format J0/Z0 bytes are selected for insertion. For this case, the J0/Z0 bytes of a STS-N signal are numbered incrementally from 1 to N.

When SDH_J0/Z0 is set high, the transmit section trace buffer enable bit, TSTBEN can be used to overwrite the first J0/Z0 byte of a STS-N signal.

TSTBEN:

The TSTBEN bit controls whether the section trace message stored in the SSTB block is inserted into the transmit stream (i.e., the first J0/Z0 byte). When TSTBEN is set high and the SDH_J0/Z0 is set high, the message stored in the SSTB is inserted into the transmit stream. When TSTBEN is set low or SDH_J0/Z0 is set low, the section trace message is supplied by the TSOP block.

TPTBEN:

The TPTBEN bit controls whether the path trace message stored in the SPTB block is inserted into the transmit stream (i.e., the J1 byte). When TPTBEN is set high, the message stored in the SPTB is inserted into the transmit stream. When TPTBEN is set low, the path trace message is supplied by the TPOP block.

Register 0x02: S/UNI-622-POS Master Configuration #2

Bit	Type	Function	Default
Bit 7	R/W	SLLE	0
Bit 6	R/W	SDLE	0
Bit 5	R/W	LOOPT	0
Bit 4	R/W	DPLE	0
Bit 3	R/W	AUTOLRDI	1
Bit 2	R/W	AUTOPRDI	1
Bit 1	R/W	AUTOLFEBE	1
Bit 0	R/W	AUTOPFEBE	1

AUTOPFEBE

The AUTOPFEBE bit determines if the remote path block errors are sent upon detection of an incoming path BIP error event. When AUTOPFEBE is set to logic one, one path FEBE is inserted for each path BIP error event, respectively. When AUTOPFEBE is set to logic zero, incoming path BIP error events do not generate FEBE events.

AUTOLFEBE

The AUTOLFEBE bit determines if remote line block errors are sent upon detection of an incoming line BIP error event. When AUTOLFEBE is set to logic one, one line FEBE is inserted for each line BIP error event, respectively. When AUTOLFEBE is set to logic zero, incoming line BIP error events do not generate FEBE events.

AUTOPRDI

The AUTOPRDI bit determines whether STS path remote defect indication (RDI) is sent immediately upon detection of an incoming alarm. When AUTOPRDI is set to logic one, STS path RDI is inserted immediately upon declaration of several alarms. Each alarm can individually be enabled and disabled using the S/UNI-622-POS Path RDI Control Registers.

AUTOLRDI

The AUTOLRDI bit determines if line remote defect indication (RDI) is sent immediately upon detection of an incoming alarm. When AUTOLRDI is set to logic one, line RDI is inserted immediately upon declaration of several alarms.

Each alarm can individually be enabled and disabled using the S/UNI-622-POS Line RDI Control Registers.

DPLE:

The Diagnostic Path Loopback, DPLE bit enables the S/UNI-622-POS diagnostic loopback where the S/UNI-622-POS's Transmit Path Overhead Processor (TPOP) is directly connected to its Receive Path Overhead Processor (RPOP). When DPLE is logic one, loopback is enabled. Under this operating condition, the S/UNI-622-POS continues to operates normally in the transmit direction. When DPLE is logic zero, the S/UNI-622-POS operates normally.

LOOPT:

The LOOPT bit selects the source of timing for the transmit section of the channel. When LOOPT is a logic zero, the transmitter timing is derived from input REFCLK (Clock Synthesis Unit). When LOOPT is a logic one, the transmitter timing is derived from the recovered clock (Clock Recovery Unit). LOOPT should not be set if the WANS is being used. The SDLE, SLLE or LOOPT bits should not be set high simultaneously.

SDLE:

The SDLE bit enables the serial diagnostic loopback. When SDLE is a logic one, the transmit serial stream on the TXD+/- differential outputs is internally connected to the received serial RXD+/- differential inputs. Under this operating condition, the S/UNI-622-POS continues to operates normally in the transmit direction. The SDLE, SLLE or LOOPT bits should not be set high simultaneously.

SLLE:

The SLLE bit enables the S/UNI-622-POS line loopback mode when the device is configured for 622.08 Mbit/s serial line interface mode of operation. When SLLE is a logic one, the recovered data from the receive serial RXD+/- differential inputs is mapped to the TXD+/- differential outputs. Under this operating condition, the S/UNI-622-POS continues to operates normally in the receive direction. The SDLE, SLLE or LOOPT bits should not be set high simultaneously.

Register 0x03: S/UNI-622-POS Clock Monitors

Bit	Type	Function	Default
Bit 7	R	TCLKA	X
Bit 6	R	RCLKA	X
Bit 5	R	RFCLKA	X
Bit 4	R	TFCLKA	X
Bit 3	R	Unused	X
Bit 2	R	REFCLKA	X
Bit 1	R	PICLKA	X
Bit 0	R	PTCLKA	X

This register provides activity monitoring of the S/UNI-622-POS clocks. When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

PTCLKA:

The PTCLK active (PTCLKA) bit monitors for low to high transition on the PTCLK parallel transmit clock input. PTCLKA is set high on a rising edge of PTCLK and is set low when this register is read.

PICLKA:

The PICLK active (PICLKA) bit monitors for low to high transition on the PICLK parallel receive clock input. PICLKA is set high on a rising edge of PICLK and is set low when this register is read.

REFCLKA:

The REFCLK active (REFCLKA) bit monitors for low to high transition on the REFCLK CSU-622 and CRU-622 reference clock input. REFCLKA is set high on a rising edge of REFCLK and is set low when this register is read.

TFCLKA:

The TFCLK active (TFCLKA) bit monitors for low to high transition on the TFCLK transmit system interface clock input. TFCLKI is set high on a rising edge of PTLCK and is set low when this register is read.

RFCLKA:

The RFCLK active (RFCLKA) bit monitors for low to high transition on the RFCLK receive system interface clock input. RFCLKA is set high on a rising edge of RFCLK and is set low when this register is read.

RCLKA:

The RCLK active (RCLKA) bit monitors for low to high transition on the RCLK receive line rate clock. RCLKA is set high on a rising edge of RCLK and is set low when this register is read.

TCLKA:

The TCLK active (TCLKA) bit monitors for low to high transition on the TCLK transmit line rate clock. TCLKA is set high on a rising edge of TCLK and is set low when this register is read.

Register 0x04: S/UNI-622-POS Master Interrupt Status #1

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	CONCATI	X
Bit 5	R	RASEI	X
Bit 4	R	TXCPI	X
Bit 3	R	RXCPI	X
Bit 2	R	RPOPI	X
Bit 1	R	RLOPI	X
Bit 0	R	RSOPI	X

When the interrupt output INTB goes low, this register allows the source of the active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

RSOPI:

The RSOPI bit is high when an interrupt request is active from the RSOP block. The RSOP interrupt sources are enabled in the RSOP Control/Interrupt Enable Register.

RLOPI:

The RLOPI bit is high when an interrupt request is active from the RLOP block. The RLOP interrupt sources are enabled in the RLOP Interrupt Enable/Status Register.

RPOPI:

The RPOPI bit is high when an interrupt request is active from the RPOP block. The RPOP interrupt sources are enabled in the RPOP Interrupt Enable Register.

RXCPI:

The RXCPI bit is high when an interrupt request is active from the RXCP block. The RXCP interrupt sources are enabled in the RXCP Interrupt Enable/Status Register.

TXCPI:

The TXCPI bit is high when an interrupt request is active from the TXCP block. The TXCP interrupt sources are enabled in the TXCP Interrupt Control/Status Register.

RASEI:

The RASEI bit is high when an interrupt request is active from the RASE block. The RASE interrupt sources are enabled in the RASE Interrupt Enable Register.

CONCATI:

The CONCATI bit is high when an interrupt request is active from the Concatenation Interrupt Status Register. The CONCAT interrupt sources are enabled in the Concatenation Status and Enable Register.

Register 0x05: S/UNI-622-POS Master Interrupt Status #2

Bit	Type	Function	Default
Bit 7	R	Reserved	X
Bit 6	R	CSPII	X
Bit 5	R	CRSII	X
Bit 4	R	TXFPI	X
Bit 3	R	RXFPI	X
Bit 2	R	WANSI	X
Bit 1	R	SSTBI	X
Bit 0	R	SPTBI	X

When the interrupt output INTB goes low, this register allows the source of the active interrupt to be identified down to the block level. Further register accesses are required for the block in question to determine the cause of an active interrupt and to acknowledge the interrupt source.

SPTBI:

The SPTBI bit is a logic one when an interrupt request is active from the SPTB block. The SPTB interrupt sources are enabled in the SPTB Control Register and the SPTB Path Signal Label Status Register.

SSTBI:

The SSTBI bit is a logic one when an interrupt request is active from the SSTB block. The SSTB interrupt sources are enabled in the SSTB Control Register and the SSTB Synchronization Message Status Register.

WANSI:

The WANSI bit is a logic one when an interrupt request is active from the WANS block. The WANS interrupt sources are enabled in the WANS Interrupt Enable/Status Register.

RXFPI:

The RXFPI bit is high when an interrupt request is active from the RXFP block. The RXFP interrupt sources are enabled in the RXFP Interrupt Enable/Status Register.

TXFPI:

The TXFPI bit is high when an interrupt request is active from the TXFP block. The TXFP interrupt sources are enabled in the TXFP Interrupt Control/Status Register.

CRSII:

The CRSII bit is high when an interrupt request is active from the Clock Recovery and SIPO block (CRSI-622). The CRSI interrupt sources are enabled in the Clock Recovery Interrupt Control/Status Register.

CSPII:

The CSPII bit is high when an interrupt request is active from the Clock Synthesis and PISO block (CSPI-622). The CSPII interrupt sources are enabled in the Clock Synthesis Interrupt Control/Status Register.

Register 0x06: S/UNI-622-POS APS Configuration and Control

Bit	Type	Function	Default
Bit 7	R/W	APSFRST	0
Bit 6	R	APSI	X
Bit 5		Unused	X
Bit 4	R/W	APSFEBE	0
Bit 3	R/W	APSRDI	0
Bit 2	R/W	APSPD	0
Bit 1	R/W	APSOE	0
Bit 0	R/W	APSEN	0

This register controls the APS transmit path override and the transmit path RDI and FEBE controls for 1+1 APS operation. See the Operation section for more discussion

APSEN:

The APSEN bit controls the 1+1 APS mode of the S/UNI-622-POS. When APSEN is set high, the S/UNI-622-POS transmit path data stream may be supplied to another S/UNI-622-POS using the POUT[7:0] bus. When APSEN is set low, the S/UNI-622-POS operates normally and POUT[7:0] is held at a constant value.

APSOE:

The APSOE bit controls the direction of the APS[4:0] pins. When APSOE is set low, the APS[4:0] pins are inputs and supply path RDI and FEBE information to TPOP. When APSEN is set high, the APS[4:0] pins are outputs and supply the receive path RDI and FEBE information from RPOP.

APSPD:

The APSPD bit controls overwriting of the transmit path data stream. When APSPD is set high, the transmit path data stream from TPOP is overwritten from the data sampled on the parallel input PIN[7:0] bus. A four-byte FIFO is used to handle minor phase variations between the transmit clock TCLK and the parallel input clock PICLK. When APSPD is set low, the TPOP path data stream is used.

APSRDI:

The APSRDI bit control the overwriting of the transmit path RDI values. When APSRDI is set high, the RDI information on the APS[4:0] pins is transmitted by TPOP. When APSRDI is set low, the RDI information from RPOP is transmitted by TPOP. The APSOE bit must be set low when APSRDI is set high.

APSFEBE

The APSFEBE bit controls the overwriting of the transmit path FEBE values. When APSFEBE is set high, the FEBE information on the APS[4:0] pins is transmitted by TPOP. When APSFEBE is set low, the FEBE information from RPOP is transmitted by TPOP. The APSOE bit must be set low when APSFEBE is set high.

APSI:

The APS FIFO interrupt indicates if the APS FIFO has underrun or overrun. The APSI register is set high when a FIFO underrun or overrun has occurred since the register was last read. The APSI register is set low when the register is read. This interrupt register should be periodically polled to ensure the APS FIFO is operating normally when configured for 1+1 APS operation.

APSFRST:

The APS FIFO Reset bit controls the four-byte FIFO which handles minor phase variations between the parallel input clock PTCLK and the transmit clock TCLK. When APSFRST is set high, the FIFO is held in reset. When APSFRST is set low, the FIFO may be reset during system reset. The APSFRST should be set high for at least 4 TCLK cycles when either S/UNI-622-POS devices in the 1+1 APS configuration are reset.

Register 0x07: S/UNI-622-POS Miscellaneous Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	TX_LIFINV	0
Bit 4	R/W	RX_LIFINV	0
Bit 3	R/W	TSOC3	0
Bit 2	R/W	RSOC3	0
Bit 1	R/W	TXDINV	0
Bit 0	R/W	RXDINV	0

RXDINV:

The receive inversion RXDINV controls the polarity of the receive data. When RXDINV is set high, the polarity of the RXD+/- is inverted. When RXDINV is set low, the RXD+/- inputs operate normally.

RXDINV and TXDINV are ignored during line loopback operation (SLLE set high).

TXDINV:

The transmit inversion TXDINV controls the polarity of the transmit data. When TXDINV is set high, the polarity of the TXD+/- is inverted. When TXDINV is set low, the TXD+/- outputs operate normally.

RXDINV and TXDINV are ignored during line loopback operation (SLLE set high).

RSOC3:

The Receive SONET/SDH OC3 enable allows the S/UNI-622-POS to process receive STS-3c/STM-1 data streams using the parallel line interface. When RSOC3 is set high, the SONET/SDH receive processors RSOP/RLOP/RPOP are configured for STS-3c/STM-1 operation. When RSOC3 is set low, the receive side of the S/UNI-622-POS is configured for STS-12c/STM-4-4c operation. Setting RSOC3 high when LIFSEL is low is invalid as the analog interface only operates at STS-12c/STM-4-4c line rates.

TSOC3:

The Transmit SONET/SDH OC3 enable allows the S/UNI-622-POS to process transmit STS-3c/STM-1 data streams using the parallel line interface. When TSOC3 is set high, the SONET/SDH transmit processors TSOP/TLOP/TPOP are configured for STS-3c/STM-1 operation. When TSOC3 is set low, the transmit side of the S/UNI-622-POS is configured for STS-12c/STM-1 operation. Setting TSOC3 high when LIFSEL is low is invalid as the analog interface only operates at STS-12c/STM-4-4c line rates.

RX_LIFINV:

The Receive LIFSEL Inversion select (RX_LIFINV) controls the interpretation of the LIFSEL pin for the receive side. When RX_LIFINV is set high, the polarity of the LIFSEL input is inverted. When RX_LIFINV is set low, the LIFSEL input operates normally for the receive side.

TX_LIFINV:

The Transmit LIFSEL Inversion select (TX_LIFINV) controls the interpretation of the LIFSEL pin for the transmit side. When TX_LIFINV is set high, the polarity of the LIFSEL input is inverted. When TX_LIFINV is set low, the LIFSEL input operates normally for the transmit side.

Register 0x08: S/UNI-622-POS Auto Line RDI Control

Bit	Type	Function	Default
Bit 7	R/W	SDLRDI	0
Bit 6	R/W	SFLRDI	0
Bit 5	R/W	LOFLRDI	1
Bit 4	R/W	LOSLRDI	1
Bit 3	R/W	RTIMLDRI	0
Bit 2	R/W	RTIULRDI	0
Bit 1	R/W	LAISLRDI	1
Bit 0		Unused	X

This register controls the auto assertion of the line RDI in TLOP for the entire SONET/SDH stream.

LAISLRDI:

The Line Alarm Indication Signal LRDI (LAISLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When LAISLRDI is set high, the transmit line RDI will be inserted. When LAISLRDI is set low, no action is taken. This register bit is used only if the AUTOLRDI register bit is also set high.

RTIULRDI:

The Section Trace Identifier Unstable LRDI (RTIULRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When RTIULRDI is set high, the transmit line RDI will be inserted. When RTIULRDI is set low, no action is taken. This register bit is used only if the AUTOLRDI register bit is also set high.

RTIMLRDI:

The Section Trace Identifier Mismatch LRDI (RTIMLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When RTIMLDRI is set high, the transmit line RDI will be inserted. When RTIMLDRI is set low, no action is taken. This register bit is used only if the AUTOLRDI register bit is also set high.

LOSLRDI:

The Loss of Signal LRDI (LOSLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When LOSLRDI is set high, the transmit line RDI will be inserted. When LOSLRDI is set low, no action is taken. This register bit is used only if the AUTOLRDI register bit is also set high.

LOFLRDI:

The Loss of Frame LRDI (LOFLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When LOFLRDI is set high, the transmit line RDI will be inserted. When LOFLRDI is set low, no action is taken. This register bit is used only if the AUTOLRDI register bit is also set high.

SFLRDI:

The Signal Fail BER LRDI (SFLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When SFLRDI is set high, the transmit line RDI will be inserted. When SFLRDI is set low, no action is taken. This register bit is used only if the AUTOLRDI register bit is also set high.

SDLRDI:

The Signal Degrade BER LRDI (SDLRDI) controls the insertion of a Line RDI in the transmit data stream upon detection of this alarm condition. When SDLRDI is set high, the transmit line RDI will be inserted. When SDLRDI is set low, no action is taken. This register bit is used only if the AUTOLRDI register bit is also set high.

Register 0x09: S/UNI-622-POS Auto Path RDI Control

Bit	Type	Function	Default
Bit 7	R/W	LCDPRDI	0
Bit 6	R/W	ALRMPRDI	0
Bit 5	R/W	PAISPRDI	1
Bit 4	R/W	PSLMPRDI	1
Bit 3	R/W	LOPPRDI	1
Bit 2	R/W	LOPCONPRDI	1
Bit 1	R/W	PTIUPRDI	1
Bit 0	R/W	PTIMPRDI	1

This register controls the auto assertion of path RDI (G1 bit 5) in the TPOP for the entire SONET/SDH stream. Also see the Auto Enhanced Path RDI register.

PTIMPRDI:

The Path Trace Identifier Mismatch PRDI (PTIMPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When PTIMPRDI is set high, the transmit line RDI will be inserted. When PTIMPRDI is set low, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set high.

PTIUPRDI:

The Path Trace Identifier Unstable PRDI (PTIUPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When PTIUPRDI is set high, the transmit line RDI will be inserted. When PTIUPRDI is set low, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set high.

LOPCONPRDI:

The Loss of Pointer Concatenation Indication PRDI (LOPCONPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When LOPCONPRDI is set high, the transmit line RDI will be inserted. When LOPCONPRDI is set low, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set high.

LOPPRDI:

The Loss of Pointer Indication PRDI (LOPPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When LOPPRDI is set high, the transmit line RDI will be inserted. When LOPPRDI is set low, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set high.

PSLMPRDI:

The Path Signal Label Mismatch PRDI (PSLMPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When PSLMPRDI is set high, the transmit line RDI will be inserted. When PSLMPRDI is set low, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set high.

PAISPRDI:

The Path Alarm Indication Signal PRDI (PAISPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm condition. When PAISPRDI is set high, the transmit line RDI will be inserted. When PAISPRDI is set low, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set high.

ALRMPRDI:

The Line Alarm Indication Signal PRDI (ALRMPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of one of the following alarm conditions: Loss of Signal (LOS), Loss of Frame (LOF) and Line Alarm Indication Signal (LAIS). When ALRMPRDI is set high, the transmit line RDI will be inserted When ALRMPRDI is set low, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set high.

LCDPRDI:

The Loss of ATM Cell Delineation Signal PRDI (LCDPRDI) controls the insertion of a Path RDI in the transmit data stream upon detection of this alarm. When LCDPRDI is set high, the transmit path RDI will be inserted. When LCDPRDI is set low, no action is taken. This register bit is used only if the AUTOPRDI register bit is also set high.

Register 0x0A: S/UNI-622-POS Auto Enhanced Path RDI Control

Bit	Type	Function	Default
Bit 7	R/W	LCDEPRDI	0
Bit 6	R/W	NOALMEPRDI	0
Bit 5	R/W	NOPAISEPRDI	0
Bit 4	R/W	PSLMEPRDI	1
Bit 3	R/W	NOLOPEPRDI	0
Bit 2	R/W	NOLOPCONEPRDI	0
Bit 1	R/W	TIUEPRDI	0
Bit 0	R/W	TIMEPRDI	1

This register controls the auto assertion of enhanced path RDI (G1 bit 5, 6 and 7) in the TPOP for the entire SONET/SDH stream.

TIMEPRDI:

When set high, the TIMEPRDI bit enables enhanced path RDI assertion when path trace message mismatch (TIM) events are detected in the receive stream. When TIMEPRDI is set high and TIM occurs, bit 6 of the G1 byte is set high while bit 7 of the G1 byte is set low.

When TIMEPRDI is set low, trace identifier mismatch events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

TIUEPRDI:

When set high, the TIUEPRDI bit enables enhanced path RDI assertion when path trace message unstable events are detected in the receive stream. When TIUEPRDI is set high and path trace message unstable occurs, bit 6 of the G1 byte is set high while bit 7 of the G1 byte is set low.

When TIUEPRDI is set low, trace identifier unstable events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

NOLOPCONEPRDI:

When set high, the NOLOPCONEPRDI bit disables enhanced path RDI assertion when loss of pointer concatenation (LOPCON) events are detected in the receive stream. When NOLOPCONEPRDI is set high and LOPCON occurs, bit 6 of the G1 byte is set low while bit 7 of the G1 byte is set high.

NOLOPCONEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOLOPCONEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

NOLOPEPRDI:

When set high, the NOLOPEPRDI bit disables enhanced path RDI assertion when loss of pointer (LOP) events are detected in the receive stream. When NOLOPEPRDI is set high and LOP occurs, bit 6 of the G1 byte is set low while bit 7 of the G1 byte is set high. NOLOPEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOLOPEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

PSLMEPRDI:

When set high, the PSLMEPRDI bit enables enhanced path RDI assertion when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMEPRDI is set high and PSLM occurs, bit 6 of the G1 byte is set high while bit 7 of the G1 byte is set low.

When PSLMEPRDI is set low, path signal label mismatch events have no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

NOPAISEPRDI:

When set high, the NOPAISEPRDI bit disables enhanced path RDI assertion when the path alarm indication signal state (PAIS) is detected in the receive stream. When NOPAISEPRDI is set high and PAIS occurs, bit 6 of the G1 byte is set low while bit 7 of the G1 byte is set high. NOPAISEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOPAISEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

NOALMEPRDI:

When set high, the NOALMEPRDI bit disables enhanced path RDI assertion when loss of signal (LOS), loss of frame (LOF) or line alarm indication signal (LAIS) events are detected in the receive stream. When NOALMEPRDI is set

high and one of the listed events occur, bit 6 of the G1 byte is set low while bit 7 of the G1 byte is set high. NOALMEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOALMEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

LCDEPRDI:

When set high, the LCDEPRDI bit enables enhanced path RDI assertion when loss of ATM cell delineation (LCD) events are detected in the receive stream. If enabled, when the event occurs, bit 6 of the G1 byte is set high while bit 7 of the G1 byte is set low.

When LCDEPRDI is set low, loss of ATM cell delineation has no effect on path RDI. In addition, this bit has no effect when EPRDI_EN is set low.

Register 0x0B: S/UNI-622-POS Receive RDI and Enhanced RDI Control

Bit	Type	Function	Default
Bit 7	R/W	PAISCONPRDI	0
Bit 6	R/W	NOPAISCONEPRDI	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	EPRDI_EN	0
Bit 1	R/W	UNEQPRDI	1
Bit 0	R/W	UNEQEPRDI	1

This register along with the Enhanced Path RDI Control register controls the auto assertion of path RDI (G1 bit 5, 6 and 7) in the TPOP for the entire SONET/SDH stream.

UNEQEPRDI:

When set high, the UNEQEPRDI bit enables enhanced path RDI assertion when the path signal label in the receive stream indicates unequipped status. When UNEQEPRDI is set high and the path signal label indicates unequipped, bit 6 of the G1 byte is set high while bit 7 of the G1 byte is set low.

When UNEQEPRDI is set low, path signal label unequipped status has no effect on enhanced path RDI.

UNEQPRDI:

When set high, the UNEQPRDI bit enables path RDI assertion when the path signal label in the receive stream indicates unequipped status. When UNEQPRDI is set low, the path signal label unequipped status has no effect on path RDI.

EPRDI_EN:

The EPRDI_EN bit enables the automatic insertion of enhanced RDI in the local transmitter. When EPRDI_EN is a logic one, auto insertion is enabled using the event enable bits in this register. When EPRDI_EN is a logic zero, enhanced path RDI is not automatically inserted in the transmit stream.

NOPAISCONEPRDI:

When set high, the NOPAISCONEPRDI bit disables enhanced path RDI assertion when path AIS concatenation (PAISCON) events are detected in the receive stream. When NOPAISCONEPRDI is set high and PAISCON occurs, bit 6 of the G1 byte is set low while bit 7 of the G1 byte is set high. NOPAISCONEPRDI has precedence over PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI.

When NOPAISCONEPRDI is set low, reporting of enhanced RDI is according to PSLMERDI, TIUEPRDI, TIMEPRDI and UNEQERDI and the associated alarm states.

PAISCONPRDI:

When set high, the PAISCONPRDI bit enables path RDI assertion when path AIS concatenation (PAISCON) events are detected in the receive stream. When PAISCONPRDI is set low, path AIS concatenation events have no effect on path RDI.

Register 0x0C: S/UNI-622-POS Received Line AIS Control

Bit	Type	Function	Default
Bit 7	R/W	SDINS	0
Bit 6	R/W	SFINS	0
Bit 5	R/W	LOFINS	1
Bit 4	R/W	LOSINS	1
Bit 3	R/W	RTIMINS	0
Bit 2	R/W	RTIUINS	0
Bit 1		Unused	X
Bit 0	R/W	DCCAIS	0

This register controls the auto assertion of the receive line AIS for the entire SONET/SDH stream.

DCCAIS:

The DCCAIS bit enables the insertion of all ones in the section DCC (RSLD) and the line DCC (RLD) when loss of frame (LOF) or LOS is declared. When DCCAIS is a logic one, all ones is inserted in RSLD and RLD when LOF or LOS is declared.

RTIUINS:

The RTIUINS bit enables the insertion of path AIS in the receive direction upon the declaration of section trace unstable. If RTIUINS is a logic one, path AIS is inserted into the SONET/SDH frame when the current received section trace identifier message has not matched the previous message for eight consecutive messages. Path AIS is terminated when the current message becomes the accepted message.

RTIMINS:

The RTIMINS bit enables the insertion of path AIS in the receive direction upon the declaration of section trace mismatch. If RTIMINS is a logic one, path AIS is inserted into the SONET/SDH frame when the accepted identifier message differs from the expected message. Path AIS is terminated when the accepted message matches the expected message.

LOSINS:

The LOSINS bit enables the insertion of path AIS in the receive direction upon the declaration of loss of signal (LOS). If LOSINS is a logic one, path AIS is inserted into the SONET/SDH frame when LOS is declared. Path AIS is terminated when LOS is removed.

LOFINS:

The LOFINS bit enables the insertion of path AIS in the receive direction upon the declaration of loss of frame (LOF). If LOFINS is a logic one, path AIS is inserted into the SONET/SDH frame when LOF is declared. Path AIS is terminated when LOF is removed.

SFINS:

The SFINS bit enables the insertion of path AIS in the receive direction upon the declaration of signal fail (SF). If SFINS is a logic one, path AIS is inserted into the SONET/SDH frame when SF is declared. Path AIS is terminated when SF is removed.

SDINS:

The SDINS bit enables the insertion of path AIS in the receive direction upon the declaration of signal degrade (SD). If SDINS is a logic one, path AIS is inserted into the SONET/SDH frame when SD is declared. Path AIS is terminated when SD is removed.

Register 0x0D: S/UNI-622-POS Receive Path AIS Control

Bit	Type	Function	Default
Bit 7	R/W	PAISCONPAIS	1
Bit 6	R/W	LOPCONPAIS	1
Bit 5	R/W	PSLUPAIS	1
Bit 4	R/W	PSLMPAIS	1
Bit 3	R/W	LOPPAIS	1
Bit 2	R/W	Reserved	1
Bit 1	R/W	TIUPAIS	1
Bit 0	R/W	TIMPAIS	1

This register controls the auto assertion of path AIS, which will force a loss of cell delineation by the receive cell processor.

TIMPAIS:

When set high, the TIMPAIS bit enables path AIS insertion when path trace message mismatch (TIM) events are detected in the receive stream. When TIMPAIS is set low, trace identifier mismatch events will not assert path AIS.

TIUPAIS:

When set high, the TIUPAIS bit enables path AIS insertion when path trace message unstable events are detected in the receive stream. When TIUPAIS is set low, trace identifier unstable events will not assert path AIS.

LOPPAIS:

When set high, the LOPPAIS bit enables path AIS insertion when loss of pointer (LOP) events are detected in the receive stream. When LOPPAIS is set low, loss of pointer events will not assert path AIS.

PSLMPAIS:

When set high, the PSLMPAIS bit enables path AIS insertion when path signal label mismatch (PSLM) events are detected in the receive stream. When PSLMPAIS is set low, path signal label mismatch events will not assert path AIS.

PSLUPAIS:

When set high, the PSLUPAIS bit enables path AIS insertion when path signal label unstable (PSLU) events are detected in the receive stream. When PSLUPAIS is set low, path signal label unstable events will not assert path AIS.

LOPCONPAIS:

When set high, the LOPCONPAIS bit enables path AIS insertion when loss of pointer concatenation (LOPCON) events are detected in the receive stream. When LOPCONPAIS is set low, loss of pointer concatenation events will not assert path AIS.

PAISCONPAIS:

When set high, the PAISCONPAIS bit enables path AIS insertion when Path AIS concatenation (PAISCON) events are detected in the receive direction. When PAISCONPAIS is set low, Path AIS concatenation events will not assert path AIS.

Reserved:

The reserved bit must be programmed to logic zero for proper operation.

Register 0x0E: S/UNI-622-POS Receive Alarm Control #1

Bit	Type	Function	Default
Bit 7	R/W	CONEN	0
Bit 6	R/W	PTIMEN	0
Bit 5	R/W	PSLMEN	0
Bit 4	R/W	PERDIEN	0
Bit 3	R/W	PRDIEN	0
Bit 2	R/W	PAISEN	0
Bit 1	R/W	LCDEN	0
Bit 0	R/W	LOPEN	0

Register 0x0F: S/UNI-622-POS Receive Alarm Control #2

Bit	Type	Function	Default
Bit 7	R/W	STIMEN	0
Bit 6	R/W	SFBEREN	0
Bit 5	R/W	SDBEREN	0
Bit 4	R/W	LRDIEN	0
Bit 3	R/W	LAISEN	0
Bit 2	R/W	OOFEN	0
Bit 1	R/W	LOFEN	0
Bit 0	R/W	LOSEN	0

LOSEN, LOFEN, OOFEN, LAISEN, LRDIEN, SDBEREN, SFBEREN, STIMEN, LOPEN, LCDEN, PAISEN, PRDIEN, PERDIEN, PSLMEN, PTIMEN, CONEN:

The above enable bits allow the corresponding alarm indications to be reported (ORed) into the RALRM output. When the enable bit is high, the corresponding alarm indication is combined with other alarm indications and output on RALRM. When the enable bit is low, the corresponding alarm indication does not affect the RALRM output.

Alarm	Description
LOS	Loss of signal
LOF	Loss of frame
OOF	Out of Frame
LAIS	Line Alarm Indication Signal
LRDI	Line Remote Defect Indication
SDBER	Signal Degrade Bit Error Rate
SFBER	Signal Fail Bit Error Rate
STIM	Section Trace Identifier Mismatch
LOP	Loss of Pointer
LCD	Loss of Cell Delineation
PAIS	Path Alarm Indication Signal
PRDI	Path Remote Defect Indication
PERDI	Path Enhanced Remote Defect Indication
PSLM	Path Signal Label Mismatch
PTIM	Path Trace Identifier Mismatch
CON	Pointer Concatenation Violation or Pointer AIS

Reserved:

The reserved bit must be programmed to logic zero for proper operation.

Register 0x10: RSOP Control/Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	BLKBIP	0
Bit 6	R/W	DDS	0
Bit 5	W	FOOF	X
Bit 4	R/W	ALGO2	0
Bit 3	R/W	BIPEE	0
Bit 2	R/W	LOSE	0
Bit 1	R/W	LOFE	0
Bit 0	R/W	OOFE	0

OOFE:

The OOFE bit is an interrupt enable for the out-of-frame alarm. When OOFE is set to logic one, an interrupt is generated when the out-of-frame alarm changes state.

LOFE:

The LOFE bit is an interrupt enable for the loss of frame alarm. When LOFE is set to logic one, an interrupt is generated when the loss of frame alarm changes state.

LOSE:

The LOSE bit is an interrupt enable for the loss of signal alarm. When LOSE is set to logic one, an interrupt is generated when the loss of signal alarm changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the section BIP-8 errors. When BIPEE is set to logic one, an interrupt is generated when a section BIP-8 error (B1) is detected.

ALGO2:

The ALGO2 bit position selects the framing algorithm used to determine and maintain the frame alignment. When a logic one is written to the ALGO2 bit position, the framer is enabled to use the second of the framing algorithms where only the first A1 framing byte and the first 4 bits of the last A2 framing

byte (12 bits total) are examined. This algorithm examines only 12 bits of the framing pattern regardless; all other framing bits are ignored. When a logic zero is written to the ALGO2 bit position, the framer is enabled to use the first of the framing algorithms where all the A1 framing bytes and all the A2 framing bytes are examined.

FOOF:

The FOOF bit controls the framing of the RSOP. When a logic one is written to FOOF, the RSOP is forced out of frame at the next frame boundary. The FOOF bit is a write only bit. Register reads may yield a logic one or a logic zero.

DDS:

The DDS bit is set to logic one to disable the descrambling of the STS-12c/STM-4-4c stream. When DDS is a logic zero, descrambling is enabled.

BLKBIP:

The BLKBIP bit position enables the accumulating of section BIP word errors. When a logic one is written to the BLKBIP bit position, one or more errors in the BIP-8 byte result in a single error being accumulated in the B1 error counter. When a logic zero is written to the BLKBIP bit position, all errors in the B1 byte are accumulated in the B1 error counter.

Register 0x11: RSOP Status/Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	BIPEI	X
Bit 5	R	LOSI	X
Bit 4	R	LOFI	X
Bit 3	R	OOFI	X
Bit 2	R	LOSV	X
Bit 1	R	LOFV	X
Bit 0	R	OOFV	X

OOFV:

The OOFV bit is read to determine the out-of-frame state of the RSOP. When OOFV is high, the RSOP is out of frame. When OOFV is low, the RSOP is in-frame.

LOFV:

The LOFV bit is read to determine the loss of frame state of the RSOP. When LOFV is high, the RSOP has declared loss of frame.

LOSV:

The LOSV bit is read to determine the loss of signal state of the RSOP. When LOSV is high, the RSOP has declared loss of signal.

OOFI:

The OOFI bit is the out-of-frame interrupt status bit. OOFI is set high when a change in the out-of-frame state occurs. This bit is cleared when this register is read.

LOFI:

The LOFI bit is the loss of frame interrupt status bit. LOFI is set high when a change in the loss of frame state occurs. This bit is cleared when this register is read.

LOSI:

The LOSI bit is the loss of signal interrupt status bit. LOSI is set high when a change in the loss of signal state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the section BIP-8 interrupt status bit. BIPEI is set high when a section layer (B1) bit error is detected. This bit is cleared when this register is read.

Register 0x12: RSOP Section BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	SBE[7]	X
Bit 6	R	SBE[6]	X
Bit 5	R	SBE[5]	X
Bit 4	R	SBE[4]	X
Bit 3	R	SBE[3]	X
Bit 2	R	SBE[2]	X
Bit 1	R	SBE[1]	X
Bit 0	R	SBE[0]	X

Register 0x13: RSOP Section BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	SBE[15]	X
Bit 6	R	SBE[14]	X
Bit 5	R	SBE[13]	X
Bit 4	R	SBE[12]	X
Bit 3	R	SBE[11]	X
Bit 2	R	SBE[10]	X
Bit 1	R	SBE[9]	X
Bit 0	R	SBE[8]	X

SBE[15:0]:

Bits SBE[15:0] represent the number of section BIP-8 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RSOP Section BIP-8 Register addresses. Such a write transfers the internally accumulated error count to the Section BIP-8 registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The count can also be polled by writing to the S/UNI-622-POS Master Reset and Identity register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks.

Register 0x14: TSOP Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	DS	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LAIS	0

LAIS:

The LAIS bit controls the insertion of line alarm indication signal (AIS). When LAIS is set to logic one, the TSOP inserts AIS into the transmit SONET/SDH stream. Activation or deactivation of line AIS insertion is synchronized to frame boundaries. Line AIS insertion results in all bits of the SONET/SDH frame being set to 1 prior to scrambling except for the section overhead.

DS:

The DS bit is set to logic one to disable the scrambling of the STS-12c/STM-4-4c stream. When DS is a logic zero, scrambling is enabled.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x15: TSOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	DLOS	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	DFP	0

DFP:

The DFP bit controls the insertion of a single bit error continuously in the most significant bit (bit 1) of the A1 section overhead framing byte. When DFP is set to logic one, the A1 bytes are set to 0x76 instead of 0xF6.

DBIP8:

The DBIP8 bit controls the insertion of bit errors continuously in the section BIP-8 byte (B1). When DBIP8 is set to logic one, the B1 byte is inverted.

DLOS:

The DLOS bit controls the insertion of all zeros in the STS-12c/STM-4-4c stream. When DLOS is set to logic one, the transmit stream is forced to 0x00.

Register 0x18: RLOP Control/Status

Bit	Type	Function	Default
Bit 7	R/W	BIPWORD	0
Bit 6	R/W	ALLONES	0
Bit 5	R/W	AISDET	0
Bit 4	R/W	LRDIDET	0
Bit 3	R/W	BIPWORDO	0
Bit 2	R/W	FEBEWORD	0
Bit 1	R	LAISV	X
Bit 0	R	LRDIV	X

LRDIV:

The LRDIV bit is read to determine the remote defect indication state of the RLOP. When LRDIV is high, the RLOP has declared line RDI.

LAISV:

The LAISV bit is read to determine the line AIS state of the RLOP. When LAISV is high, the RLOP has declared line AIS.

FEBEWORD:

The FEBEWORD bit controls the accumulation of FEBEs. When FEBEWORD is high, if the FEBE event has a value from 1 to 4, the FEBE event counter is incremented for each and every FEBE bit. However, if the FEBE event has a value greater than 4 and is valid, the FEBE event counter is incremented by 4. When FEBEWORD is low, the FEBE event counter is incremented for each and every FEBE bit that occurs during that frame (the counter can be incremented up to 24.).

BIPWORDO:

The BIPWORDO bit controls the indication of B2 errors reported to the TLOP block for insertion as FEBEs. When BIPWORDO is logic one, the BIP errors are indicated once per frame whenever one or more B2 bit errors occur during that frame. When BIPWORDO is logic zero, BIP errors are indicated once for every B2 bit error that occurs during that frame. The accumulation of B2 error events functions independently and is controlled by the BIPWORD register bit.

LRDIDET:

The LRDIDET bit determines the line RDI alarm detection algorithm. When LRDIDET is set to logic one, line RDI is declared when a 110 binary pattern is detected in bits 6, 7 and 8 of the K2 byte for three consecutive frames. When LRDIDET is set to logic zero, line RDI is declared when a 110 binary pattern is detected in bits 6, 7 and 8 of the K2 byte for five consecutive frames.

AISDET:

The AISDET bit determines the line AIS alarm detection algorithm. When AISDET is set to logic one, line AIS is declared when a 111 binary pattern is detected in bits 6, 7 and 8 of the K2 byte for three consecutive frames. When AISDET is set to logic zero, line AIS is declared when a 111 binary pattern is detected in bits 6, 7 and 8 of the K2 byte for five consecutive frames.

ALLONES:

The ALLONES bit controls automatically forcing the SONET/SDH frame passed to downstream blocks to logical all-ones whenever line AIS is detected. When ALLONES is set to logic one, the SONET/SDH frame is forced to logic one immediately when the line AIS alarm is declared. When line AIS is removed, the downstream data stream is immediately returned to carrying the receive data. When ALLONES is set to logic zero, the downstream data stream always carries the receive data regardless of the line AIS alarm state.

BIPWORD:

The BIPWORD bit controls the accumulation of B2 errors. When BIPWORD is logic one, the B2 error event counter is incremented only once per frame whenever one or more B2 bit errors occur during that frame. When BIPWORD is logic zero, the B2 error event counter is increment for each and every B2 bit error that occurs during that frame.

Register 0x19: RLOP Interrupt Enable/Interrupt Status

Bit	Type	Function	Default
Bit 7	R/W	FEBEE	0
Bit 6	R/W	BIPEE	0
Bit 5	R/W	LAISE	0
Bit 4	R/W	LRDIE	0
Bit 3	R	FEBEI	X
Bit 2	R	BIPEI	X
Bit 1	R	LAISI	X
Bit 0	R	LRDII	X

LRDII:

The LRDII bit is the remote defect indication interrupt status bit. LRDII is set high when a change in the line RDI state occurs. This bit is cleared when this register is read.

LAISI:

The LAISI bit is the line AIS interrupt status bit. LAISI is set high when a change in the line AIS state occurs. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the line BIP-96 interrupt status bit. BIPEI is set high when a line layer (B2) bit error is detected. This bit is cleared when this register is read.

FEBEI:

The FEBEI bit is the line far end block error interrupt status bit. FEBEI is set high when a line layer FEBE (M1) is detected. This bit is cleared when this register is read.

LRDIE:

The LRDIE bit is an interrupt enable for the line remote defect indication alarm. When LRDIE is set to logic one, an interrupt is generated when the line RDI state changes.

LAISE:

The LAISE bit is an interrupt enable for line AIS. When LAISE is set to logic one, an interrupt is generated when line AIS changes state.

BIPEE:

The BIPEE bit is an interrupt enable for the line BIP-96 errors. When BIPEE is set to logic one, an interrupt is generated when a line BIP-96 error (B2) is detected.

FEBEE:

The FEBEE bit is an interrupt enable for the line far end block errors. When FEBEE is set to logic one, an interrupt is generated when FEBE (Z2) is detected.

Register 0x1A: RLOP Line BIP-96 LSB

Bit	Type	Function	Default
Bit 7	R	LBE[7]	X
Bit 6	R	LBE[6]	X
Bit 5	R	LBE[5]	X
Bit 4	R	LBE[4]	X
Bit 3	R	LBE[3]	X
Bit 2	R	LBE[2]	X
Bit 1	R	LBE[1]	X
Bit 0	R	LBE[0]	X

Register 0x1B: RLOP Line BIP-96

Bit	Type	Function	Default
Bit 7	R	LBE[15]	X
Bit 6	R	LBE[14]	X
Bit 5	R	LBE[13]	X
Bit 4	R	LBE[12]	X
Bit 3	R	LBE[11]	X
Bit 2	R	LBE[10]	X
Bit 1	R	LBE[9]	X
Bit 0	R	LBE[8]	X

Register 0x1C: RLOP Line BIP-96 MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LBE[19]	X
Bit 2	R	LBE[18]	X
Bit 1	R	LBE[17]	X
Bit 0	R	LBE[16]	X

LBE[19:0]

Bits LBE[19:0] represent the number of line BIP-96 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP-96 Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line BIP-96 Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The count can also be polled by writing to the S/UNI-622-POS Master Reset and Identity register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP and TXFP blocks.

Register 0x1D: RLOP Line FEBE LSB

Bit	Type	Function	Default
Bit 7	R	LFE[7]	X
Bit 6	R	LFE[6]	X
Bit 5	R	LFE[5]	X
Bit 4	R	LFE[4]	X
Bit 3	R	LFE[3]	X
Bit 2	R	LFE[2]	X
Bit 1	R	LFE[1]	X
Bit 0	R	LFE[0]	X

Register 0x1E: RLOP Line FEBE

Bit	Type	Function	Default
Bit 7	R	LFE[15]	X
Bit 6	R	LFE[14]	X
Bit 5	R	LFE[13]	X
Bit 4	R	LFE[12]	X
Bit 3	R	LFE[11]	X
Bit 2	R	LFE[10]	X
Bit 1	R	LFE[9]	X
Bit 0	R	LFE[8]	X

Register 0x1F: RLOP Line FEBE MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LFE[19]	X
Bit 2	R	LFE[18]	X
Bit 1	R	LFE[17]	X
Bit 0	R	LFE[16]	X

LFE[19:0]

Bits LFE[19:0] represent the number of line FEBE errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to any of the RLOP Line BIP-96 Register or Line FEBE Register addresses. Such a write transfers the internally accumulated error count to the Line FEBE Registers within approximately 7 µs and simultaneously resets the internal counter to begin a new cycle of error accumulation.

The count can also be polled by writing to the S/UNI-622-POS Master Reset and Identity register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP and TXFP blocks.

Register 0x20: TLOP Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	APSREG	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	LRDI	0

LRDI:

The LRDI bit controls the insertion of line remote defect indication (LRDI). When LRDI is set to logic one, the TLOP inserts line RDI into the transmit SONET/SDH stream. Line RDI is inserted by transmitting the code 110 in bit positions 6, 7 and 8 of the K2 byte of the STS-12c stream.

APSREG:

The APSREG bit selects the source for the transmit APS channel K1/K2 bytes. When APSREG is a logic zero, 0x0000 is inserted in the transmit APS K1 and K2 bytes. When APSREG is a logic one, the transmit APS channel is inserted from the TLOP Transmit K1 Register and the TLOP Transmit K2 Register.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x21: TLOP Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	DBIP96	0

DBIP96:

The DBIP96 bit controls the insertion of bit errors continuously in the line BIP-96 bytes (B2). When DBIP96 is set to logic one, the B2 bytes are inverted.

Register 0x22: TLOP Transmit K1

Bit	Type	Function	Default
Bit 7	R/W	K1[7]	0
Bit 6	R/W	K1[6]	0
Bit 5	R/W	K1[5]	0
Bit 4	R/W	K1[4]	0
Bit 3	R/W	K1[3]	0
Bit 2	R/W	K1[2]	0
Bit 1	R/W	K1[1]	0
Bit 0	R/W	K1[0]	0

K1[7:0]:

The K1[7:0] bits contain the value inserted in the K1 byte when the APSREG bit in the TLOP Control Register is logic one. K1[7] is the most significant bit corresponding to bit 1, the first bit transmitted. K1[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to this register. The contents of this register, and the TLOP Transmit K2 Register are inserted in the SONET/SDH stream starting at the next frame boundary. Successive writes to this register must be spaced at least two frames (250 µs) apart.

Register 0x23: TLOP Transmit K2

Bit	Type	Function	Default
Bit 7	R/W	K2[7]	0
Bit 6	R/W	K2[6]	0
Bit 5	R/W	K2[5]	0
Bit 4	R/W	K2[4]	0
Bit 3	R/W	K2[3]	0
Bit 2	R/W	K2[2]	0
Bit 1	R/W	K2[1]	0
Bit 0	R/W	K2[0]	0

K2[7:0]:

The K2[7:0] bits contain the value inserted in the K2 byte when the APSREG bit in the TLOP Control Register is logic one. K2[7] is the most significant bit corresponding to bit 1, the first bit transmitted. K2[0] is the least significant bit, corresponding to bit 8, the last bit transmitted. The bits in this register are double buffered so that register writes do not need to be synchronized to SONET/SDH frame boundaries. The insertion of a new APS code value is initiated by a write to the TLOP Transmit K1 Register. A coherent APS code value is ensured by writing the desired K2 APS code value to this register before writing the TLOP Transmit K1 Register.

Register 0x24: S/UNI-622-POS Transmit Sync. Message (S1)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	TS1[3]	0
Bit 2	R/W	TS1[2]	0
Bit 1	R/W	TS1[1]	0
Bit 0	R/W	TS1[0]	0

TS1[3:0]:

The value written to these bit positions is inserted in the first S1 byte position of the transmit stream. The S1 byte is used to carry synchronization status messages between line terminating network elements. TS1[3] is the most significant bit, corresponding to the first bit transmitted. TS1[0] is the least significant bit, corresponding to the last bit transmitted.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x25: S/UNI-622-POS Transmit J0/Z0

Bit	Type	Function	Default
Bit 7	R/W	J0/Z0[7]	1
Bit 6	R/W	J0/Z0[6]	1
Bit 5	R/W	J0/Z0[5]	0
Bit 4	R/W	J0/Z0[4]	0
Bit 3	R/W	J0/Z0[3]	1
Bit 2	R/W	J0/Z0[2]	1
Bit 1	R/W	J0/Z0[1]	0
Bit 0	R/W	J0/Z0[0]	0

J0/Z0[7:0]:

The value written to this register is inserted into the J0/Z0 byte positions of the transmit stream when enabled using the SDH_J0/Z0 register. J0/Z0[7] is the most significant bit, corresponding to the first bit (bit 1) transmitted. J0/Z0[0] is the least significant bit, corresponding to the last bit (bit 8) transmitted.

Register 0x28: SSTB Control

Bit	Type	Function	Default
Bit 7	R/W	ZEROEN	0
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

This register controls the receive and transmit portions of the SSTB.

LEN16:

The section trace message length bit (LEN16) selects the length of the section trace message to be 16 bytes or 64 bytes. When set high, a 16-byte section trace message is selected. If set low, a 64-byte section trace message is selected.

NOSYNC:

The section trace message synchronization disable bit (NOSYNC) disables the writing of the section trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is set high and NOSYNC is set low, the receive section trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 is set low, and NOSYNC is also set low, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is set high, synchronization is disabled, and the section trace message buffer behaves as a circular buffer.

TNULL:

The transmit null bit (TNULL) controls the insertion of an all-zeros section trace identifier message in the transmit stream. When TNULL is set high, the contents of the transmit buffer is ignored and all-zeros bytes are provided to the TSOP block. When TNULL is set low the contents of the transmit section trace buffer is sent to TSOP for insertion into the J0/Z0 transmit section

overhead byte. TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5:

The receive trace identifier persistence bit (PER5) controls the number of times a section trace identifier message must be received unchanged before being accepted. When PER5 is set high, a message is accepted when it is received unchanged five times consecutively. When PER5 is set low, the message is accepted after three identical repetitions.

RTIMIE:

The RTIMIE bit controls the activation of the interrupt output when the comparison between accepted identifier message and the expected message changes state. When RTIMIE is a logic one, changes in match state activates the interrupt (INTB) output.

RTIUIE:

The RTIUIE bit controls the activation of the interrupt output when the receive identifier message changes state. When RTIUIE is a logic one, changes in the received section trace identifier message stable/unstable state will activate the interrupt (INTB) output.

RRAMACC:

The receive RAM access control bit (RRAMACC) directs read and writes access to between the receive and transmit portion of the S/UNI-622-POS. When RRAMACC is set high, subsequent microprocessor read and write accesses are directed to the receive side trace buffers. When RRAMACC is set low, microprocessor accesses are directed to the transmit side trace buffer.

ZEROEN:

The zero enable bit (ZEROEN) enables TIM assertion and removal based on an all ZERO's section trace message string. When ZEROEN is set high, all ZERO's section trace message strings are considered when entering and exiting TIM states. When ZEROEN is set low, all ZERO's section trace message strings are ignored.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x29: SSTB Section Trace Identifier Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

This register reports the section trace identifier status of the SSTB.

RTIMV:

The RTIMV bit reports the match/mismatch status of the identifier message framer. RTIMV is a logic one when the accepted identifier message differs from the expected message written by the microprocessor. RTIMV is a logic zero when the accepted message matches the expected message.

RTIMI:

The RTIMI bit is a logic one when match/mismatch status of the trace identifier framer changes state. This bit is cleared when this register is read.

RTIUV:

The RTIUV bit reports the stable/unstable status of the identifier message framer. RTIUV is a logic one when the current received section trace identifier message has not matched the previous message for eight consecutive messages. RTIUV is a logic zero when the current message becomes the accepted message as determined by the PER5 bit in the SPTB Control register.

RTIUI:

The RTIUI bit is a logic one when stable/unstable status of the trace identifier framer changes state. This bit is cleared when this register is read.

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to a message buffer has been completed. BUSY is set high upon writing to the SSTB Indirect Address register, and stays high until the initiated access has completed, at which point BUSY is set low. This register should be polled to determine when new data is available in the SSTB Indirect Data register.

Register 0x2A: SSTB Indirect Address Register

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into section trace identifier buffers.

A[6:0]:

The indirect read address bits (A[6:0]) indexes into the section trace identifier buffers. When RRAMACC is set high, addresses 0 to 63 reference the receive capture page while addresses 64 to 127 reference the receive expected page. The receive capture page contains the identifier bytes extracted from the receive stream. The receive expected page contains the expected trace identifier message downloaded from the microprocessor. When RRAMACC is set low, addresses 0 to 63 reference the transmit message buffer which contains the identifier message to be inserted in the section trace byte, the first J0/Z0 byte, of each frame in the transmit stream. When RRAMACC is set low, addresses 64 to 127 are unused and must not be accessed.

RWB:

The access control bit (RWB) selects between an indirect read or write access to the static page of the section trace message buffer. Writing to this register initiates an external microprocessor access to the static page of the section trace message buffer. When RWB is set high, a read access is initiated. The data read can be found in the SSTB Indirect Data register. When RWB is set low, a write access is initiated. The data in the SSTB Indirect Data register will be written to the addressed location in the static page.

Register 0x2B: SSTB Indirect Data Register

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the section trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D[7:0]:

The indirect data bits (D[7:0]) reports the data read from a message buffer after an indirect read operation has completed. The data to be written to a buffer must be set up in this register before initiating an indirect write operation.

Register 0x30 (EXTD=0): RPOP Status/Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5	R	LOPV	X
Bit 4		Unused	X
Bit 3	R	PAISV	X
Bit 2	R	PRDIV	X
Bit 1	R	NEWPTRI	X
Bit 0	R/W	NEWPTRE	0

NOTE: To facilitate additional register mapping, shadow registers have been added to registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers.

This register allows the status of path level alarms to be monitored.

NEWPTRE:

The NEWPTRE bit is the interrupt enable for the receive new pointer status. When NEWPTRE is a logic one, an interrupt is generated when the pointer interpreter validates a new pointer.

NEWPTRI:

The NEWPTRI bit is the receive new pointer interrupt status bit. NEWPTRI is a logic one when the pointer interpreter has validated a new pointer value (H1, H2). NEWPTRI is cleared when this register is read.

PRDIV:

The PRDIV bit is read to determine the remote defect indication state. When PRDIV is a logic one, the S/UNI-622-POS has declared path RDI.

PAISV:

The PAISV bit is read to determine the path AIS state. When PAISV is a logic one, the S/UNI-622-POS has declared path AIS.

PLOPV:

The PLOPV bit is read to determine the loss of pointer state. When PLOPV is a logic one, the S/UNI-622-POS has declared LOP.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x30 (EXTD=1): RPOP Status/Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	IINVCNT	0
Bit 5	R/W	PSL5	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R	ERDIV[2]	X
Bit 1	R	ERDIV[1]	X
Bit 0	R/W	ERDIV[0]	X

NOTE: To facilitate additional register mapping, shadow registers have been added to registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers.

The Status Register is provided at RPOP read address 0, if the extend register (EXTD) bit is set in register 6.

ERDIV[2:0]:

The ERDIV[2:0] bits reflect the current state of the detected enhanced RDI, (filtered G1 bits 5, 6, & 7).

IINVCNT:

When IINVCNT (Intuitive Invalid Pointer Counter) bit is set to 1, if the RPOP pointer interpreter state machine is in the LOP state, a new pointer received 3 consecutive times resets the inv_point count. If this bit is set to 0, the inv_point count will not be reset if pointer interpreter is in the LOP state and a new pointer received 3 consecutive times.

PSL5:

The PSL5 bit controls the filtering of the path signal label byte (C2). When PSL5 is set high, the PSL is updated when the same value is received for 5 consecutive frames. When the PSL5 is set low, the PSL is updated when the same value is received for 3 consecutive frames.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x31 (EXTD=0): RPOP Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSLI	X
Bit 6		Unused	X
Bit 5	R	LOPI	X
Bit 4		Unused	X
Bit 3	R	PAISI	X
Bit 2	R	PRDII	X
Bit 1	R	BIPEI	X
Bit 0	R	FEBEI	X

NOTE: To facilitate additional register mapping, shadow registers have been added to registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers.

This register allows identification and acknowledgment of path level alarm and error event interrupts.

FEBEI:

The FEBEI bit is the path FEBE interrupt status bit. FEBEI is a logic one when a FEBE error is detected. This bit is cleared when this register is read.

BIPEI:

The BIPEI bit is the path BIP-8 interrupt status bit. BIPEI is a logic one when a B3 error is detected. This bit is cleared when this register is read.

PRDII:

The PRDII bit is the path remote defect indication interrupt status bit. PRDII is a logic one when a change in the path RDI state or the auxiliary path RDI state occurs. This bit is cleared when this register is read.

PAISI:

The PAISI bit is the path alarm indication signal interrupt status bit. PAISI is a logic one when a change in the path AIS state occurs. This bit is cleared when this register is read.

LOPI:

The LOPI bit is the loss of pointer interrupt status bit. LOPI is a logic one when a change in the LOP state occurs. This bit is cleared when this register is read.

PSLI:

The PSLI bit is the change of path signal label interrupt status bit. PSLI is a logic one when a change is detected in the path signal label register. The current path signal label can be read from the RPOP Path Signal Label register. This bit is cleared when this register is read.

Register 0x31 (EXTD=1): RPOP Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	ERDII	X

NOTE: To facilitate additional register mapping, shadow registers have been added to registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers.

This register allows identification and acknowledgment of path level alarm and error event interrupts.

ERDII:

The ERDII bit is set high when a change is detected in the received enhanced RDI state. This bit is cleared when the RPOP Interrupt Status register is read.

Register 0x32: RPOP Pointer Interrupt Status

Bit	Type	Function	Default
Bit 7	R	ILLJREQI	X
Bit 6		Unused	X
Bit 5	R	DISCOPAI	X
Bit 4	R	INVNDFI	X
Bit 3	R	ILLPTRI	X
Bit 2	R	NSEI	X
Bit 1	R	PSEI	X
Bit 0	R	NDFI	X

This register allows identification and acknowledgment of pointer event interrupts.

NDFI:

The NDFI bit is set to logic one when the RPOP detects an active NDF event to a valid pointer value. NDFI is cleared when the RPOP Pointer Interrupt Status register is read.

PSEI:

The PSEI bit is set to logic one when the RPOP detects a positive stuff event. PSEI is cleared when the RPOP Pointer Interrupt Status register is read.

NSEI:

The NSEI bit is set to logic one when the RPOP detects a negative stuff event. NSEI is cleared when the RPOP Pointer Interrupt Status register is read.

ILLPTRI:

The ILLPTRI bit is set to logic one when the RPOP detects an illegal pointer event. ILLPTRI is cleared when the RPOP Pointer Interrupt Status register is read.

INVNDFI:

The INVNDFI bit is set to logic one when the RPOP detects an invalid NDF event. INVNDFI is cleared when the RPOP Pointer Interrupt Status register is read.

DISCOPAI:

The DISCOPAI bit is set to logic one when the RPOP detects a discontinuous change of pointer. DISCOPAI is cleared when the RPOP Pointer Interrupt Status register is read.

ILLJREQI:

The ILLJREQI bit is set to logic one when the RPOP detects an illegal pointer justification request event. ILLJREQI is cleared when the RPOP Pointer Interrupt Status register is read.

Register 0x33 (EXTD=0): RPOP Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	PSLE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	LOPE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	PAISE	0
Bit 2	R/W	PRDIE	0
Bit 1	R/W	BIPEE	0
Bit 0	R/W	FEBEE	0

NOTE: To facilitate additional register mapping, shadow registers have been added to registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers.

This register allows interrupt generation to be enabled for path level alarm and error events.

FEBEE:

The FEBEE bit is the interrupt enable for path FEBEs. When FEBEE is a logic one, an interrupt is generated when a path FEBE is detected.

BIPEE:

The BIPEE bit is the interrupt enable for path BIP-8 errors. When BIPEE is a logic one, an interrupt is generated when a B3 error is detected.

PRDIE:

The PRDIE bit is the interrupt enable for path RDI. When PRDIE is a logic one, an interrupt is generated when the path RDI state changes.

PAISE:

The PAISE bit is the interrupt enable for path AIS. When PAISE is a logic one, an interrupt is generated when the path AIS state changes.

LOPE:

The LOPE bit is the interrupt enable for LOP. When LOPE is a logic one, an interrupt is generated when the LOP state changes.

PSLE:

The PSLE bit is the interrupt enable for changes in the received path signal label. When PSLE is a logic one, an interrupt is generated when the received C2 byte changes.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x33 (EXTD=1): RPOP Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	ERDIE	0

NOTE: To facilitate additional register mapping, shadow registers have been added to registers 0x30, 0x31 and 0x33. These shadow registers are accessed in the same way as the normal registers.

The EXTD (extend register) bit must be set in register 0x36 to allow switching between accessing the normal registers and the shadow registers.

This register allows interrupt generation to be enabled for path level alarm and error events.

ERDIE:

When REDIE is a logic one, an interrupt is generated when a path enhanced RDI is detected.

Register 0x34: RPOP Pointer Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	ILLJREQE	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	DISCOPAE	0
Bit 4	R/W	INVNDFE	0
Bit 3	R/W	ILLPTRE	0
Bit 2	R/W	NSEE	0
Bit 1	R/W	PSEE	0
Bit 0	R/W	NDFE	0

This register is used to enable pointer event interrupts.

NDFE:

When a logic one is written to the NDFE interrupt enable bit position, an interrupt is generated when a change in active offset due to the reception of an enabled NDF (NDF_enabled indication) occurs.

PSEE:

When a logic one is written to the PSEE interrupt enable bit position, an interrupt is generated when a positive pointer adjustment event is received.

NSEE:

When a logic one is written to the NSEE interrupt enable bit position, an interrupt is generated when a negative pointer adjustment is received.

ILLPTRE:

When a logic one is written to the ILLPTRE interrupt enable bit position, an interrupt is generated when an illegal pointer is received.

INVNDFE:

When a logic one is written to the INVNDFE interrupt enable bit position, an interrupt is generated when an invalid NDF code is received.

DISCOPAE:

When a logic one is written to the DISCOPAE interrupt enable bit position, an interrupt is generated when a change of pointer alignment event occurs.

ILLJREQE:

When a logic one is written to the ILLJREQE interrupt enable bit position, an interrupt is generated when an illegal pointer justification request is received.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x35: RPOP Pointer LSB

Bit	Type	Function	Default
Bit 7	R	PTR[7]	X
Bit 6	R	PTR[6]	X
Bit 5	R	PTR[5]	X
Bit 4	R	PTR[4]	X
Bit 3	R	PTR[3]	X
Bit 2	R	PTR[2]	X
Bit 1	R	PTR[1]	X
Bit 0	R	PTR[0]	X

Register 0x36: RPOP Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDFPOR	0
Bit 6	R/W	EXTD	0
Bit 5	R/W	RDI10	0
Bit 4		Unused	X
Bit 3	R	S1	X
Bit 2	R	S0	X
Bit 1	R	PTR[9]	X
Bit 0	R	PTR[8]	X

PTR[9:0]:

The PTR[7:0] bits contain the current pointer value as derived from the H1 and H2 bytes. To ensure reading a valid pointer, the NDFI, NSEI and PSEI bits of the RPOP Pointer Interrupt Status register should be read before and after reading this register to ensure that the pointer value did not changed during the register read.

S0, S1:

The S0 and S1 bits contain the two S bits received in the last H1 byte. These bits should be software debounced to ensure the proper values are received.

RDI10:

The RDI10 bit controls the filtering of the remote defect indication and the auxiliary remote defect indication. When RDI10 is set to logic one, the PRDI and ARDI statuses are updated when the same value is received in the corresponding bit of the G1 byte for 10 consecutive frames. When PRDI10 is set to logic zero, the PRDI and ARDI statuses are updated when the same value is received for 5 consecutive frames.

NDFPOR:

The NDFPOR (new data flag pointer outside range) bit allows an NDF counter enable, if the pointer value is outside the range (0-782). If this bit is set high the definition for NDF counter enable is enabled NDF + ss. If this bit is set low the definition for NDF counter enable is enabled NDF + ss + offset in the range of 0 to 782. Note that this bit only allows the NDF counter to count towards LOP when the pointer is out of range and no active offset change will occur.

EXTD:

The EXTD bit extends the registers to facilitate additional mapping. If this bit is set high, the register mapping, for registers 0x30, 0x31 and 0x33, are extended.

Register 0x37: RPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R	PSL[7]	X
Bit 6	R	PSL[6]	X
Bit 5	R	PSL[5]	X
Bit 4	R	PSL[4]	X
Bit 3	R	PSL[3]	X
Bit 2	R	PSL[2]	X
Bit 1	R	PSL[1]	X
Bit 0	R	PSL[0]	X

PSL[7:0]:

The PSL[7:0] bits contain the path signal label byte (C2). The value in this register is updated to a new path signal label value if the same new value is observed for three of five consecutive frames, depending on the status of the PSL5 bit.

Register 0x38: RPOP Path BIP-8 LSB

Bit	Type	Function	Default
Bit 7	R	PBE[7]	X
Bit 6	R	PBE[6]	X
Bit 5	R	PBE[5]	X
Bit 4	R	PBE[4]	X
Bit 3	R	PBE[3]	X
Bit 2	R	PBE[2]	X
Bit 1	R	PBE[1]	X
Bit 0	R	PBE[0]	X

Register 0x39: RPOP Path BIP-8 MSB

Bit	Type	Function	Default
Bit 7	R	PBE[15]	X
Bit 6	R	PBE[14]	X
Bit 5	R	PBE[13]	X
Bit 4	R	PBE[12]	X
Bit 3	R	PBE[11]	X
Bit 2	R	PBE[10]	X
Bit 1	R	PBE[9]	X
Bit 0	R	PBE[8]	X

These registers allow path BIP-8 errors to be accumulated.

PBE[15:0]:

PBE[15:0] represent the number of B3 errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path BIP-8 registers within a maximum of 7 µs and simultaneously resets the internal counter to begin a

new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The count can also be polled by writing to the S/UNI-622-POS Master Reset and Identity register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP, and TXFP blocks.

Register 0x3A: RPOP Path FEBE LSB

Bit	Type	Function	Default
Bit 7	R	PFE[7]	X
Bit 6	R	PFE[6]	X
Bit 5	R	PFE[5]	X
Bit 4	R	PFE[4]	X
Bit 3	R	PFE[3]	X
Bit 2	R	PFE[2]	X
Bit 1	R	PFE[1]	X
Bit 0	R	PFE[0]	X

Register 0x3B: RPOP Path FEBE MSB

Bit	Type	Function	Default
Bit 7	R	PFE[15]	X
Bit 6	R	PFE[14]	X
Bit 5	R	PFE[13]	X
Bit 4	R	PFE[12]	X
Bit 3	R	PFE[11]	X
Bit 2	R	PFE[10]	X
Bit 1	R	PFE[9]	X
Bit 0	R	PFE[8]	X

These registers allow path FEBEs to be accumulated.

PFE[15:0]:

Bits PFE[15:0] represent the number of path FEBE errors (individual or block) that have been detected since the last time the error count was polled. The error count is polled by writing to either of the RPOP Path BIP-8 Register addresses or to either of the RPOP Path FEBE Register addresses. Such a write transfers the internally accumulated error count to the Path FEBE Registers within approximately 7 µs and simultaneously resets the internal

counter to begin a new cycle of error accumulation. This transfer and reset is carried out in a manner that ensures that coincident events are not lost.

The count can also be polled by writing to the S/UNI-622-POS Master Reset and Identity register (0x00). Writing to register address 0x00 loads all the counter registers in the RSOP, RLOP, RPOP, SPTB, SSTB, RXCP, TXCP, RXFP and TXFP blocks.

Register 0x3C: RPOP RDI

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	BLKFEBE	0
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	ARDIE	0
Bit 0	R	ARDIV	X

ARDIV:

The auxiliary RDI bit (ARDIV) reports the current state of the path auxiliary RDI within the receive path overhead processor.

ARDIE:

When a logic one is written to the ARDIE interrupt enable bit position, an interrupt is generated when a change in the path auxiliary RDI state occurs.

BLKFEBE:

When set high, the block FEBE bit (BLKFEBE) causes path FEBE errors to be reported and accumulated on a block basis. A single path FEBE error is accumulated for a block if the received FEBE code for that block is between 1 and 8 inclusive. When BLKFEBE is set low, path FEBE errors are accumulated on a error basis.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x3D: RPOP Ring Control

Bit	Type	Function	Default
Bit 7	R/W	SOS	0
Bit 6	R/W	ENSS	0
Bit 5	R/W	BLKBIP	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	BLKBIPO	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

BLKBIPO:

When set high, the block BIP-8 output bit (BLKBIPO) indicates that path BIP-8 errors are to be reported on a block basis to the transmit path overhead processor (TPOP) block. A single path BIP error is reported to the return transmit path overhead processor if any of the path BIP-8 results indicates a mismatch. When BLKBIP is set low, BIP-8 errors are reported on a bit basis.

BLKBIP:

When set high, the block BIP-8 bit (BLKBIP) indicates that path BIP-8 errors are to be accumulated on a block basis. A single BIP error is accumulated if any of the BIP-8 results indicates a mismatch. When BLKBIP is set low, BIP-8 errors are accumulated on a bit basis.

ENSS:

The enable size bit (ENSS) controls whether the SS bits in the payload pointer are used to determine offset changes in the pointer interpreter state machine. When a logic one is written to this bit, an incorrect SS bit pattern (i.e., not equal to 10) will prevent RPOP from issuing NDF_enable, inc_ind, new_point and dec_ind indications. When a logic zero is written to this bit, the received SS bits do not affect active offset change events.

SOS:

The stuff opportunity spacing control bit (SOS) controls the spacing between consecutive pointer justification events on the receive stream. When a logic one is written to this bit, the definition of inc_ind and dec_ind indications

includes the requirement that active offset changes have occurred a least three frame ago. When a logic zero is written to this bit, pointer justification indications in the receive stream are followed without regard to the proximity of previous active offset changes.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x40: TPOP Control/Diagnostic

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	EPRDIEN	0
Bit 5	R/W	EPRDISRC	0
Bit 4	R/W	PERSIST	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	DBIP8	0
Bit 0	R/W	PAIS	0

PAIS:

The PAIS bit controls the insertion of STS path alarm indication signal. When a logic one is written to this bit position, the complete SPE, and the pointer bytes (H1, H2, and H3) are overwritten with the all-ones pattern. When a logic zero is written to this bit position, the pointer bytes and the SPE are processed normally.DBIP8:

The DBIP8 bit controls the insertion of bit errors continuously in the B3 byte. When DBIP8 is a logic one, the B3 byte is inverted.

PERSIST

The path far end receive failure alarm persistence bit (PERSIST) controls the persistence of the RDI asserted into the transmit stream. When PERSIST is a logic one, the RDI code inserted into the transmit stream as a result of consequential actions is asserted for a minimum of 20 frames in non-enhanced RDI mode, or the last valid RDI code before an idle code (idle codes are when bits 5,6,7 are 000, 001, or 011) is asserted for 20 frames in enhanced RDI mode. When PERSIST is logic zero, the transmit RDI code changes immediately based on received alarm conditions.

EPRDISRC

The enhanced path receive defect indication alarm source bit (EPRDISRC) controls the source of RDI input to be inserted onto the G1 byte. When EPRDIEN is logic zero, the extended RDI bits of the G1 byte not overwritten by the TPOP block, regardless of EPRDISRC. When EPRDIEN is logic one and EPRDISCR is logic zero, the extended RDI bits of the G1 byte, bits 6 and

7, are inserted according to the value in the G1[1:0] register bits (register 0x49). When EPRDIEN is logic one and EPRDISCR is logic one, the value register 0x49 G1[1:0] is ignored and the EPRDI bits in the G1 byte are set according to the setting of the Channel Auto Enhanced Path RDI Control registers (0x92 and 0x93).

EPRDIEN

The enhanced path receive defect indication alarm enable bit (EPRDIEN) controls the use of 3-bit RDI mode. When EPRDIEN is set to logic zero, the basic path RDI scheme is used and only G1[5] is used to indicate PRDI. When EPRDIEN is set to logic one, the enhanced path RDI scheme is used and the three G1[7:5] bits are used to indicate PRDI. The actual three bit code will be controlled according to the EPRDISRC.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x41: TPOP Pointer Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	FTPTR	0
Bit 5	R/W	SOS	0
Bit 4	R/W	PLD	0
Bit 3	R/W	NDF	0
Bit 2	R/W	NSE	0
Bit 1	R/W	PSE	0
Bit 0	R/W	Reserved	0

This register allows control over the transmitted payload pointer for diagnostic purposes.

PSE:

The PSE bit controls the insertion of positive pointer movements. A zero to one transition on this bit enables the insertion of a single positive pointer justification in the outgoing stream. This register bit is automatically cleared when the pointer movement is inserted.

NSE:

The NSE bit controls the insertion of negative pointer movements. A zero to one transition on this bit enables the insertion of a single negative pointer justification in the outgoing stream. This register bit is automatically cleared when the pointer movement is inserted.

NDF:

The NDF bit controls the insertion of new data flags in the inserted payload pointer. When a logic one is written to this bit position, the pattern contained in the NDF[3:0] bit positions in the TPOP Arbitrary Pointer MSB Register is inserted continuously in the payload pointer. When a logic zero is written to this bit position, the normal pattern (0110) is inserted in the payload pointer.

PLD:

The PLD bit controls the loading of the pointer value contained in the TPOP Arbitrary Pointer Registers. Normally the TPOP Arbitrary Pointer Registers

are written to set up the arbitrary new pointer value, the S-bit values, and the NDF pattern. A logic one is then written to this bit position to load the new pointer value. The new data flag bit positions are set to the programmed NDF pattern for the first frame; subsequent frames have the new data flag bit positions set to the normal pattern (0110) unless the NDF bit described above is set to a logic one.

Note: When loading an out of range pointer (that is a pointer with a value greater than 782), the TPOP continues to operate with timing based on the last valid pointer value. The out of range pointer value will of course be inserted in the STS-12c/STM-4-4c stream. Although a valid SPE will continue to be generated, it is unlikely to be extracted by downstream circuitry, which should be in a loss of pointer state.

This bit is automatically cleared after the new payload pointer has been loaded.

SOS:

The SOS bit controls the stuff opportunity spacing between consecutive SPE positive or negative stuff events. When SOS is a logic zero, stuff events may be generated every frame as controlled by the PSE and NSE register bits described above. When SOS is a logic one, stuff events may be generated at a maximum rate of once every four frames.

FTPTR:

The force transmit pointer bit (FTPTR) enables the insertion of the pointer value contained in the Arbitrary Pointer Registers into the POUT[7:0] stream for diagnostic purposes. This allows the ATM/POS payload mapping circuitry to continue functioning normally and a valid SPE to continue to be generated, although it is unlikely to be extracted by downstream circuitry as the downstream pointer processor should be in a loss of pointer state.

If FTPTR is set to logic one, the APTR[9:0] bits of the Arbitrary Pointer Registers are inserted into the H1 and H2 bytes of the transmit stream. At least one corrupted pointer is guaranteed to be sent. If FTPTR is a logic zero, a valid pointer is inserted.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x43: TPOP Current Pointer LSB

Bit	Type	Function	Default
Bit 7	R	CPTR[7]	X
Bit 6	R	CPTR[6]	X
Bit 5	R	CPTR[5]	X
Bit 4	R	CPTR[4]	X
Bit 3	R	CPTR[3]	X
Bit 2	R	CPTR[2]	X
Bit 1	R	CPTR[1]	X
Bit 0	R	CPTR[0]	X

Register 0x44: TPOP Current Pointer MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	CPTR[9]	X
Bit 0	R	CPTR[8]	X

CPTR[9:0]:

The CPTR[9:0] bits reflect the value of the current payload pointer being inserted in the outgoing stream. The value may be changed by loading a new pointer value using the TPOP Arbitrary Pointer LSB and MSB Registers, or by inserting positive and negative pointer movements using the PSE and NSE register bits.

It is recommended the CPTR[9:0] value be software debounced to ensure a correct value is received.

Register 0x45: TPOP Arbitrary Pointer LSB

Bit	Type	Function	Default
Bit 7	R/W	APTR[7]	0
Bit 6	R/W	APTR[6]	0
Bit 5	R/W	APTR[5]	0
Bit 4	R/W	APTR[4]	0
Bit 3	R/W	APTR[3]	0
Bit 2	R/W	APTR[2]	0
Bit 1	R/W	APTR[1]	0
Bit 0	R/W	APTR[0]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[7:0]:

The APTR[7:0] bits, along with the APTR[9:8] bits in the TPOP Arbitrary Pointer MSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is inserted in the outgoing stream by writing a logic one to the PLD bit in the TPOP Pointer Control Register.

If the FTPTR bit in the TPOP Pointer Control register is a logic one, the current APTR[9:0] value is inserted into the payload pointer bytes (H1 and H2) in the transmit stream.

Register 0x46: TPOP Arbitrary Pointer MSB

Bit	Type	Function	Default
Bit 7	R/W	NDF[3]	1
Bit 6	R/W	NDF[2]	0
Bit 5	R/W	NDF[1]	0
Bit 4	R/W	NDF[0]	1
Bit 3	R/W	S[1]	1
Bit 2	R/W	S[0]	0
Bit 1	R/W	APTR[9]	0
Bit 0	R/W	APTR[8]	0

This register allows an arbitrary pointer to be inserted for diagnostic purposes.

APTR[9:8]:

The APTR[9:8] bits, along with the APTR[7:0] bits in the TPOP Arbitrary Pointer LSB Register are used to set an arbitrary payload pointer value. The arbitrary pointer value is inserted in the outgoing stream by writing a logic one to the PLD bit in the TPOP Pointer Control Register.

If the FTPTR bit in the TPOP Pointer Control register is a logic one, the current APTR[9:0] value is inserted into the payload pointer bytes (H1 and H2) in the transmit stream.

S[1:0]:

The S[1:0] bits contain the value inserted in the S[1:0] bit positions (also referred to as the unused bits) in the payload pointer. These bits are continuously inserted into the transmit stream.

NDF[3:0]:

The NDF[3:0] bits contain the value inserted in the NDF bit positions when an arbitrary new payload pointer value is inserted (using the PLD bit in the TPOP Pointer Control Register) or when new data flag generation is enabled using the NDF bit in the TPOP Pointer Control Register.

Register 0x47: TPOP Path Trace

Bit	Type	Function	Default
Bit 7	R/W	J1[7]	0
Bit 6	R/W	J1[6]	0
Bit 5	R/W	J1[5]	0
Bit 4	R/W	J1[4]	0
Bit 3	R/W	J1[3]	0
Bit 2	R/W	J1[2]	0
Bit 1	R/W	J1[1]	0
Bit 0	R/W	J1[0]	0

This register allows control over the path trace byte.

J1[7:0]:

The J1[7:0] bits are inserted in the J1 byte position in the transmit stream .

Register 0x48: TPOP Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	C2[7]	0
Bit 6	R/W	C2[6]	0
Bit 5	R/W	C2[5]	0
Bit 4	R/W	C2[4]	0
Bit 3	R/W	C2[3]	0
Bit 2	R/W	C2[2]	0
Bit 1	R/W	C2[1]	0
Bit 0	R/W	C2[0]	1

This register allows control over the path signal label. Upon reset the register defaults to 0x01, which signifies an equipped unspecific payload.

C2[7:0]:

The C2[7:0] bits are inserted in the C2 byte position in the transmit stream.

C2 should be reprogrammed with the value 0x13 when transmitting ATM payload data.

C2 should be reprogrammed with the value 0x16 when transmitting scrambled packet over SONET payload data.

C2 may be reprogrammed with the value 0xCF when transmitting unscrambled packet over SONET payload data. However, POS scrambling in the TXFP block must be turned off.

Register 0x49: TPOP Path Status

Bit	Type	Function	Default
Bit 7	R/W	FEBE[3]	0
Bit 6	R/W	FEBE[2]	0
Bit 5	R/W	FEBE[1]	0
Bit 4	R/W	FEBE[0]	0
Bit 3	R/W	PRDI	0
Bit 2	R/W	APRDI	0
Bit 1	R/W	G1[1]	0
Bit 0	R/W	G1[0]	0

This register allows control over the path status byte.

G1[1:0]:

The G1[1:0] bits are inserted in bits 1 and 2 of the Path Status Byte G1. These bits are ignored when EPRDIEN is logic zero or when EPRDIEN and EPRDISRC are both logic one. See the description of EPRDIEN and EPRDISRC for more details on how G1 can be controlled.

APRDI:

The APRDI bit controls the insertion of the auxiliary path remote defect indication. When APRDI is a logic one, the APRDI bit position in the path status byte is set high. When APRDI is a logic zero, the APRDI bit position in the path status byte is set low.

PRDI:

The PRDI bit controls the insertion of the path remote defect indication. When a logic one is written to this bit position, the PRDI bit position in the path status byte is set high. When a logic zero is written to this bit position, the PRDI bit position in the path status byte is set low. This bit is ignored when EPRDIEN is logic zero or when EPRDIEN and EPRDISRC are both logic one.

FEBE[3:0]:

The FEBE[3:0] bits are inserted in the FEBE bit positions in the path status byte. The value contained in FEBE[3:0] is cleared after being inserted in the

path status byte. Any non-zero FEBE[3:0] value overwrites the value that would normally have been inserted based on the number of FEBEs accumulated on primary input FEBE during the last frame. When reading this register, a non-zero value in these bit positions indicates that the insertion of this value is still pending.

Register 0x4E: TPOP Concatenation LSB

Bit	Type	Function	Default
Bit 7	R/W	CONCAT[7]	1
Bit 6	R/W	CONCAT[6]	1
Bit 5	R/W	CONCAT[5]	1
Bit 4	R/W	CONCAT[4]	1
Bit 3	R/W	CONCAT[3]	1
Bit 2	R/W	CONCAT[2]	1
Bit 1	R/W	CONCAT[1]	1
Bit 0	R/W	CONCAT[0]	1

Register 0x4F: TPOP Concatenation MSB

Bit	Type	Function	Default
Bit 7	R/W	CONCAT[15]	1
Bit 6	R/W	CONCAT[14]	0
Bit 5	R/W	CONCAT[13]	0
Bit 4	R/W	CONCAT[12]	1
Bit 3	R/W	CONCAT[11]	0
Bit 2	R/W	CONCAT[10]	0
Bit 1	R/W	CONCAT[9]	1
Bit 0	R/W	CONCAT[8]	1

These registers allow control over the concatenation indication values transmitted in SONET/SDH pointers.

CONCAT[15:0]:

The CONCAT[15:0] bits control the value inserted in the some of the H1 and H2 byte positions when transmitting an STS-12c or STM-4-4c stream. The value written to CONCAT[15:8] is inserted in the H1 byte position of STS-1 #5 and STS-1 #9 in the concatenated stream. The value written to CONCAT[7:0] is inserted in the H2 byte position of STS-1 #5 and STS-1 #9 in the concatenated stream. The default values represent the normal concatenation

indication (all ones in the pointer bits, zeros in the unused bits, and NDF indication).

Register 0x50: SPTB Control

Bit	Type	Function	Default
Bit 7	R/W	ZEROEN	0
Bit 6	R/W	RRAMACC	0
Bit 5	R/W	RTIUIE	0
Bit 4	R/W	RTIMIE	0
Bit 3	R/W	PER5	0
Bit 2	R/W	TNULL	1
Bit 1	R/W	NOSYNC	0
Bit 0	R/W	LEN16	0

This register controls the receive and transmit portions of the SPTB.

LEN16:

The LEN16 bit selects the length of the path trace message to be 16 bytes or 64 bytes. When LEN16 is a logic one, a 16 byte path trace message is selected. When LEN16 is a logic zero, a 64 byte path trace message is selected.

NOSYNC:

The NOSYNC bit disables the writing of the path trace message into the trace buffer to be synchronized to the content of the message. When LEN16 is a logic one and NOSYNC is a logic zero, the receive path trace message byte with its most significant bit set will be written to the first location in the buffer. When LEN16 and NOSYNC are logic zero, the byte after the carriage return/linefeed (CR/LF) sequence will be written to the first location in the buffer. When NOSYNC is a logic one, synchronization is disabled, and the path trace message buffer behaves as a circular buffer.

TNULL:

The TNULL bit controls the insertion of an all-zero path trace identifier message in the transmit stream. When TNULL is a logic one, the contents of the transmit buffer is ignored and all-zeros bytes are inserted. When TNULL is a logic zero, the contents of the transmit path trace buffer is sent to TPOP for insertion into the J1 transmit path overhead byte. TNULL should be set high before changing the contents of the trace buffer to avoid sending partial messages.

PER5:

The PER5 bit controls the number of times a path trace identifier message must be received unchanged before being accepted. When PER5 is a logic one, a message is accepted when it is received unchanged five times consecutively. When PER5 is a logic zero, the message is accepted after three identical repetitions.

RTIMIE:

The RTIMIE bit controls the activation of the interrupt output when the comparison between accepted identifier message and the expected message changes state. When RTIMIE is a logic one, changes in match state activates the interrupt output.

RTIUIE:

The RTIUIE bit controls the activation of the interrupt output when the receive identifier message changes state. When RTIUIE is a logic one, changes in the received path trace identifier message stable/unstable state will activate the interrupt output.

RRAMACC:

The RRAMACC bit directs read and writes access to either the receive or transmit path trace buffer. When RRAMACC is a logic one, microprocessor accesses are directed to the receive path trace buffer. When RRAMACC is a logic zero, microprocessor accesses are directed to the transmit path trace buffer.

ZEROEN:

The zero enable bit (ZEROEN) enables TIM assertion and removal based on an all ZERO's path trace message string. When ZEROEN is set high, all ZERO's path trace message strings are considered when entering and exiting TIM states. When ZEROEN is set low, all ZERO's path trace message strings are ignored.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x51: SPTB Path Trace Identifier Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RTIUI	X
Bit 2	R	RTIUV	X
Bit 1	R	RTIMI	X
Bit 0	R	RTIMV	X

This register reports the path trace identifier status of the SPTB.

RTIMV:

The RTIMV bit reports the match/mismatch status of the identifier message framer. RTIMV is a logic one when the accepted identifier message differs from the expected message written by the microprocessor. RTIMV is a logic zero when the accepted message matches the expected message.

RTIMI:

The RTIMI bit is a logic one when match/mismatch status of the trace identifier framer changes state. This bit is cleared when this register is read.

RTIUV:

The RTIUV bit reports the stable/unstable status of the identifier message framer. RTIUV is a logic one when the current received path trace identifier message has not matched the previous message for eight consecutive messages. RTIUV is a logic zero when the current message becomes the accepted message as determined by the PER5 bit in the SPTB Control register.

RTIUI:

The RTIUI bit is a logic one when stable/unstable status of the trace identifier framer changes state. This bit is cleared when this register is read.

BUSY:

The BUSY bit reports whether a previously initiated indirect read or write to a message buffer has been completed. BUSY is set to a logic one immediately upon writing to the SPTB Indirect Address register, and stays high until the initiated access is completed. This register should be polled to determine when new data is available in the SPTB Indirect Data register.

Register 0x52: SPTB Indirect Address Register

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

This register supplies the address used to index into path trace identifier buffers.

A[6:0]:

The indirect read address bits (A[6:0]) are used to address the path trace identifier buffers. When RRAMACC is set high, addresses 0 to 63 reference the captured message page while addresses 64 to 127 reference the expected message page of the receive path trace buffer. The captured message page contains the identifier bytes extracted from the receive stream. The expected message page contains the path trace message to which the captured message page is compared. When RRAMACC is set low, addresses 0 to 63 reference the transmit path trace buffer which contains the path trace message inserted in the transmit stream.

RWB:

The access control bit (RWB) selects between an indirect read or write access to the selected path trace buffer (receive or transmit as determined by the RRAMACC bit). Writing to this register initiates an access to the selected path trace buffer. When RWB is a logic one, a read access is initiated. The addressed location's contents are placed in the SPTB Indirect Data register. When RWB is a logic zero, a write access is initiated. The data in the SPTB Indirect Data register is written to the addressed location in the selected buffer.

Register 0x53: SPTB Indirect Data Register

Bit	Type	Function	Default
Bit 7	R/W	D[7]	0
Bit 6	R/W	D[6]	0
Bit 5	R/W	D[5]	0
Bit 4	R/W	D[4]	0
Bit 3	R/W	D[3]	0
Bit 2	R/W	D[2]	0
Bit 1	R/W	D[1]	0
Bit 0	R/W	D[0]	0

This register contains the data read from the path trace message buffer after a read operation or the data to be written into the buffer before a write operation.

D[7:0]:

The indirect data bits (D[7:0]) contain the data read from either the transmit or receive path trace buffer after an indirect read operation is completed. The data that is written to a buffer is set up in this register before initiating the indirect write operation.

Register 0x54: SPTB Expected Path Signal Label

Bit	Type	Function	Default
Bit 7	R/W	EPSL[7]	0
Bit 6	R/W	EPSL[6]	0
Bit 5	R/W	EPSL[5]	0
Bit 4	R/W	EPSL[4]	0
Bit 3	R/W	EPSL[3]	0
Bit 2	R/W	EPSL[2]	0
Bit 1	R/W	EPSL[1]	0
Bit 0	R/W	EPSL[0]	0

EPSL[7:0]:

The EPSL[7:0] bits contain the expected path signal label byte (C2). EPSL[7:0] is compared with the C2 byte extracted from the receive stream. A path signal label match or mismatch is declared based upon the following table:

Expect	Receive	Action Declared
00	00	Match
00	01	Mismatch
00	XX	Mismatch
01	00	Mismatch
01	01	Match
01	XX	Match
XX	00	Mismatch
XX	01	Match
XX	XX	Match
XX	YY	Mismatch

EPSL[7:0] should be reprogrammed with the value 0x13 when receiving ATM payload data.

EPSL[7:0] should be reprogrammed with the value 0x16 when receiving scrambled packet over SONET payload data.

Register 0x55: SPTB Path Signal Label Status

Bit	Type	Function	Default
Bit 7	R/W	RPSLUIE	0
Bit 6	R/W	RPSLMIE	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	RPSLUI	X
Bit 2	R	RPSLUV	X
Bit 1	R	RPSLMI	X
Bit 0	R	RPSLMV	X

RPSLMV:

The RPSLMV bit reports the match/mismatch status between the expected and the accepted path signal label. RPSLMV is a logic one when the accepted PSL results in a mismatch with the expected PSL written by the microprocessor. RPSLMV is a logic zero when the accepted PSL results in a match with the expected PSL.

RPSLMI:

The RPSLMI bit is a logic one when the match/mismatch status between the accepted and the expected path signal label changes state. This bit is cleared when this register is read.

RPSLUV:

The RPSLUV reports the stable/unstable status of the path signal label in the receive stream. RPSLUV is a logic one when the current received C2 byte differs from the previous C2 byte for five consecutive frames. RPSLUV is a logic zero when the same PSL code is received for five consecutive frames.

RPSLUI:

The RPSLUI bit is a logic one when the stable/unstable status of the path signal label changes state. This bit is cleared when this register is read.

RPSLMIE:

The RPSLMIE bit is the interrupt enable for the path signal label match/mismatch status. When RPSLMIE is a logic one, changes in the match state generate an interrupt.

RPSLUIE:

The RPSLUIE bit is the interrupt enable for the path signal label stable/unstable status. When RPSLUIE is a logic one, changes in the stable/unstable state generate an interrupt.

Register 0x58: CSPI Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	ROOLI	X

ROOLI:

The ROOLI bit is the reference out of lock interrupt status bit. ROOLI is set high when the ROOLV register goes high, indicating that the PLL is not locked to the reference clock REFCLK. ROOLI is cleared when this register is read.

Register 0x59: CSPI Status and Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	ROOLV	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	ROOLE	0

ROOLE:

The ROOLE bit enables the reference out of lock indication interrupt. When ROOLE is set high, an interrupt is generated upon assertion and negation events of the ROOLV register. When ROOLE is set low, changes in the ROOL status do not generate an interrupt.

ROOLV:

The transmit reference out of lock status indicates the clock synthesis phase lock loop is unable to lock to the reference clock on REFCLK. ROOLV is a logic one if the divided down synthesized clock frequency is not within approximately 488ppm of the REFCLK frequency. At startup, ROOLV may remain high for several hundred millisecond while the PLL obtains lock.

When the AVD power supply of the S/UNI-622-POS is subjected to a change greater than the ±5% tolerance specified for the 3.3V analog supply pins, the Clock Synthesis Unit may lose lock to the reference. When this occurs, the ROOLV will remain high until the CSU is reset using the CSURESETLPF and CSURSET registers.

Register 0x5A: CSPI Clock Synthesis Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	CSURESET	0
Bit 5	R/W	CSURESETLPF	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The CSU Control register provides direct access to the CSU. When the CSU does not lock properly (ROOLV remains high), the CSU may be re-initialized using this register.

When the AVD power supply of the S/UNI-622-POS is subjected to a change greater than the ±5% tolerance specified for the 3.3V analog supply pins, the Clock Synthesis Unit may lose lock to the reference clock. When this occurs, the ROOLV will remain high until the CSU is reset using the CSURESETLPF and CSURSET registers.

The S/UNI-622-POS will operate normally if the power supply does not vary beyond the specified ±5% tolerance.

CSURESETLPF:

The CSU low pass filter (LPF) reset control CSURESETLPF bit provides a software reset for the CSU-622 ABC. When CSURESETLPF is set high, the CSU RESETLPF input is set high forcing the CSU LPF into reset. When CSURESETLPF is set low, the CSU RESETLPF input is controlled by the system reset.

The CSURESETLPF and CSURESET should be held high for 10ms to properly reset the CSU.

CSURESET:

The CSU reset control CSURESET bit provides a software reset for the CSU-622 ABC. When CSURESET is set high, the CSU RESET input is set high forcing the CSU into reset. When CSURESET is set low, the CSU RESET input is controlled by the system reset and digital test mode.

The CSURESETLPF and CSURESET should be held high for 10ms to properly reset the CSU.

Register 0x5C: CRSI Configuration

Bit	Type	Function	Default
Bit 7	R/W	SDINV	0
Bit 6	R/W	PFPEN	0
Bit 5	R/W	SENB	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2	R	LOTI	X
Bit 1	R	ROOLI	X
Bit 0	R	DOOLI	X

DOOLI:

The DOOLI bit is the data out of lock interrupt status bit. DOOLI is set high when the DOOLV bit goes high, indicating the CRU has gone out of lock. DOOLI is cleared when this register is read.

ROOLI:

The ROOLI bit is the reference out of lock interrupt status bit. ROOLI is set high when the ROOLV register changes state, indicating that either the PLL is locked to the reference clock REFCLK or is in out of lock. ROOLI is cleared when this register is read.

LOTI:

The LOTI bit is the loss of transition interrupt status bit. LOTI is set high when a loss of transition event occurs. A loss of transition is defined as either the SD input set low or more than 96 consecutive ones or zeros received. LOTI is cleared when this register is read.

SENB:

The loss of signal transition detector enable (SENB) bit enables the declaration of loss of transition (LOT) when more than 96 consecutive ones or zeros occurs in the receive data. When SENB is a logic zero, a loss of transition is declared when more than 96 consecutive ones or zeros occurs in the receive data or when the SD input is low. When SENB is a logic one, a loss of transition is declared only when the SD input is low.

PFPEN:

The parallel frame pulse enable (PFPEN) enables the parallel frame pulse operation when the parallel data interface is enabled (LIFSEL is set high). When PFPEN is a logic zero, the FPIN input is ignored and the SONET/SDH framing is performed on the PIN[7:0] data. When PFPEN is logic one, the SONET/SDH framer is ignored and the PIN[7:0] bus is assumed to be byte aligned marked with the FPIN frame pulse. PFPEN is ignored when the LIFSEL input is set low.

SDINV:

The signal detect input invert (SDINV) controls the polarity of the SD input. The value of the SD input is logically XOR'ed with the value of the SDINV register. Therefore, when SDINV is a logic zero, valid signal power is indicated by the SD input high. When SDINV is a logic one, valid signal power is indicated by the SD input low.

Register 0x5D: CRSI Status

Bit	Type	Function	Default
Bit 7	R	LOCK	X
Bit 6	R	LOTV	X
Bit 5	R	ROOLV	X
Bit 4	R	DOOLV	X
Bit 3		Unused	X
Bit 2	R/W	LOTE	0
Bit 1	R/W	ROOLE	0
Bit 0	R/W	DOOLE	0

DOOLE:

The DOOLE bit is an interrupt enable for the recovered data out of lock status. When DOOLE is set to logic one, an interrupt is generated upon assertion events of the DOOLV register. When ROOLE is set low, changes in the DOOL status do not generate an interrupt.

ROOLE:

The ROOLE bit enables the reference out of lock indication interrupt. When ROOLE is set high, an interrupt is generated upon assertion and negation events of the ROOLV register. When ROOLE is set low, changes in the ROOL status do not generate an interrupt.

LOTE:

The LOTE bit enables the loss of transition indication interrupt. When LOTE is set high, an interrupt is generated upon assertion events of the LOTV register. When LOTE is set low, changes in the LOTV status do not generate an interrupt.

DOOLV:

The recovered data out of lock status indicates the clock recovery phase locked loop is unable to recover and lock to the input data stream. DOOLV is a logic one if the divided down recovered clock frequency is not within approximately 488ppm of the REFCLK frequency or if no transitions have occurred on the RXD input for more than 96 bits.

ROOLV:

The recovered reference out of lock status indicates the clock recovery phase locked loop is unable to lock to the reference clock on REFCLK. ROOLV is a logic one if the divided down synthesized clock frequency is not within approximately 488ppm of the REFCLK frequency. At startup, ROOLV may remain high for several hundred millisecond while the PLL obtains lock.

LOTV:

The loss of transition status indicates the receive power is lost or at least 97 consecutive ones or zeros have been received. LOTV is a logic zero if the SD input is high or fewer than 97 consecutive ones or zeros have been received. LOTV is a logic one if the SD input is low or more than 96 consecutive ones or zeros have been received.

LOCK:

The CRU reference locking status indicates if the CRU is locking to the reference clock or is locking to the receive data. LOCK is a logic zero if the CRU is locking or locked to the reference clock. LOCK is a logic one if the CRU is locking or locked to the receive data. LOCK is invalid if the CRU is not used.

Register 0x5E: CRSI Clock Recovery Control

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	RTYPE	0
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

RTYPE:

The CRU recovery mode register sets the PLL recovery mode for jitter transfer and jitter tolerance. When RTYPE is a logic zero, the CRU operates in LAN mode with improved tolerance and relaxed jitter transfer. When RTYPE is a logic one, the CRU operates in WAN mode with compliant jitter transfer.

For proper operation, leave pins C0 and C1 floating when RTYPE is logic zero. When RTYPE is logic one, the specified capacitor must be connected between C0 and C1 for proper operation.

Register 0x60: RXCP Configuration 1

Bit	Type	Function	Default
Bit 7	R/W	DDSCR	0
Bit 6	R/W	HDSCR	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	HCSADD	1
Bit 1	R/W	Reserved	0
Bit 0	R/W	DISCOR	0

DISCOR:

The DISCOR bit controls the HCS error correction algorithm. When DISCOR is a logic zero, the error correction algorithm is enabled, and single-bit errors detected in the cell header are corrected. When DISCOR is a logic one, the error correction algorithm is disabled, and any error detected in the cell header is treated as an uncorrectable HCS error.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to comparison. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is compared. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is compared.

HDSCR:

HDSCR enables the self-synchronous $x^{43} + 1$ descrambler to continue running through the bytes which should contain the ATM cell headers. When HSCR is set low, the descrambling polynomial will function only over the ATM payload bytes. When HDSCR is set high, the descrambling polynomial will function over all bytes, including the 5 ATM header bytes. This function is available for use with PPP packets and flags which are scrambled at the source to prevent the generation of “killer” sequences.

DDSCR:

The DDSCR bit controls the descrambling of the cell payload with the polynomial $x^{43} + 1$. When DDSCR is set high, cell payload descrambling is disabled. When DDSCR is set low, payload descrambling is enabled.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x61: RXCP Configuration 2

Bit	Type	Function	Default
Bit 7	R/W	CCDIS	0
Bit 6	R/W	HCSPASS	0
Bit 5	R/W	IDLEPASS	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	Reserved	0
Bit 1	R/W	HCSFTR[1]	0
Bit 0	R/W	HCSFTR[0]	0

HCSFTR[1:0]:

The HCS filter bits, HCSFTR[1:0] indicate the number of consecutive error-free cells required, while in detection mode, before reverting back to correction mode.

HCSFTR[1:0]	Cell Acceptance Threshold
00	One ATM cell with correct HCS before resumption of cell acceptance. This cell is accepted.
01	Two ATM cells with correct HCS before resumption of cell acceptance. The last cell is accepted.
10	Four ATM cells with correct HCS before resumption of cell acceptance. The last cell is accepted.
11	Eight ATM cells with correct HCS before resumption of cell acceptance. The last cell is accepted.

IDLEPASS:

The IDLEPASS bit controls the function of the Idle Cell filter. When IDLEPASS is written with a logic zero, all cells that match the Idle Cell Header Pattern and Idle Cell Header Mask are filtered out. When IDLEPASS is a logic one, the Idle Cell Header Pattern and Mask registers are ignored. The default state of this bit and the bits in the Idle Cell Header Mask and Idle Cell Header Pattern Registers enable the dropping of idle cells.

HCSPASS:

The HCSPASS bit controls the dropping of cells based on the detection of an uncorrectable HCS error. When HCSPASS is a logic zero, cells containing an uncorrectable HCS error are dropped. When HCSPASS is a logic one, cells are passed to the receive FIFO regardless of errors detected in the HCS. Additionally, the HCS verification finite state machine never exits the correction mode.

Regardless of the programming of this bit, cells are always dropped while the cell delineation state machine is in the 'HUNT' or 'PRESYNC' states unless the CCDIS bit in this register is set high.

CCDIS:

The CCDIS bit can be used to disable all cell filtering and cell delineation. All payload data read from the RXCP is passed into its FIFO without the requirement of having to find cell delineation first.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x62: RXCP FIFO/UTOPIA Control and Configuration

Bit	Type	Function	Default
Bit 7	R/W	RXPTYP	0
Bit 6		Unused	X
Bit 5	R/W	RCAINV	0
Bit 4	R/W	RCALEVEL0	1
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four-cell receive FIFO. When FIFORST is set low, the FIFO operates normally. When FIFORST is set high, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST. Activating this bit during a cell transfer may result in a truncated cell on the System Interface.

RCALEVEL0:

The RCA level 0 bit, RCALEVEL0, determines when the RCA transitions low for Level 2 operation. When RCALEVEL0 is set high, a high-to-low transition on output RCA indicates that the receive FIFO is empty and RCA will de-assert on the rising RFCLK edge after word 27 (of the 27 word cell structure) is output. When RCALEVEL0 is set low, a high-to-low transition on output RCA indicates that the receive FIFO is near empty and RCA will de-assert on the rising RFCLK edge after word 13 (of the 27 word cell structure) is output.

RCALEVEL0 must be set high when the system interface is configured for Level 3 operation.

RCAINV:

The RCAINV bit inverts the polarity of the RCA output signal for Level 2 operation. When RCAINV is a logic one, the polarity of RCA is inverted (RCA at logic zero means there is a receive cell available to be read). When RCAINV is a logic zero, the polarity of RCA is not inverted.

RCAINV must be set low when the system interface is configured for Level 3 operation.

RXPTYP:

The RXPTYP bit selects even or odd parity for output RPRTY for Level 2 operation. When set high, output RPRTY is the even parity bit for outputs RDAT[15:0]. When RXPTYP is set low, RPRTY is the odd parity bit for outputs RDAT[15:0].

RXPTYP must be set low when the system interface is configured for Level 3 operation.

Register 0x63: RXCP Interrupt Enable and Counter Status

Bit	Type	Function	Default
Bit 7	R	XFERI	X
Bit 6	R	OVR	X
Bit 5		Unused	X
Bit 4	R/W	XFERE	0
Bit 3	R/W	OOCDE	0
Bit 2	R/W	HCSE	0
Bit 1	R/W	FOVRE	0
Bit 0	R/W	LCDE	0

LCDE:

The LCDE bit enables the generation of an interrupt due to a change in the LCD state. When LCDE is set high, the interrupt is enabled.

FOVRE:

The FOVRE bit enables the generation of an interrupt due to a FIFO overrun error condition. When FOVRE is set high, the interrupt is enabled.

HCSE:

The HCSE bit enables the generation of an interrupt due to the detection of a corrected or an uncorrected HCS error. When HCSE is set high, the interrupt is enabled.

OOCDE:

The OOCDE bit enables the generation of an interrupt due to a change in cell delineation state. When OOCDE is set high, the interrupt is enabled.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the RXCP Count registers. When XFERE is set high, the interrupt is enabled.

OVR:

The OVR bit is the overrun status of the RXCP Performance Monitoring Count registers. A logic one in this bit position indicates that a previous transfer

(indicated by XFERI being logic one) has not been acknowledged before the next accumulation interval has occurred and that the contents of the RXCP Count registers have been overwritten. OVR is set low when this register is read.

XFERI:

The XFERI bit indicates that a transfer of RXCP Performance Monitoring Count data has occurred. A logic one in this bit position indicates that the RXCP Count registers have been updated. This update is initiated by writing to one of the RXCP Count register locations or to the S/UNI-622-POS, Master Reset and Identity register. XFERI is set low when this register is read.

Register 0x64: RXCP Status/Interrupt Status

Bit	Type	Function	Default
Bit 7	R	OOCDV	X
Bit 6	R	LCDV	X
Bit 5		Unused	X
Bit 4	R	OOCDI	X
Bit 3	R	CHCSI	X
Bit 2	R	UHCSI	X
Bit 1	R	FOVRI	X
Bit 0	R	LCDI	X

LCDI:

The LCDI bit is set high when there is a change in the loss of cell delineation (LCD) state. This bit is reset immediately after a read to this register.

FOVRI:

The FOVRI bit is set high when an attempt is made to write into the FIFO when it is already full. This bit is reset immediately after a read to this register. Continuous over-writing of the FIFO results in only one interrupt.

UHCSI:

The UHCSI bit is set high when an uncorrected HCS error is detected. This bit is reset immediately after a read to this register.

CHCSI:

The CHCSI bit is set high when a corrected HCS error is detected. This bit is reset immediately after a read to this register.

OOCDI:

The OOCDI bit is set high when the RXCP enters or exits the SYNC state. The OOCDV bit indicates whether the RXCP is in the SYNC state or not. The OOCDI bit is reset immediately after a read to this register.

LCDV:

The LCDV bit gives the Loss of Cell Delineation state. When LCD is high, an out of cell delineation (OCD) defect has persisted for the number of cells

specified in the LCD Count Threshold register. When LCD is low, no OCD has persisted for the number of cells specified in the LCD Count Threshold register. The cell time period can be varied by using the LCDC[7:0] register bits in the RXCP LCD Count Threshold register.

OOCDV:

The OOCDV bit indicates the cell delineation state. When OOCDV is high, the cell delineation state machine is in the 'HUNT' or 'PRESYNC' state and is hunting for the cell boundaries. When OOCDV is low, the cell delineation state machine is in the 'SYNC' state and cells are passed through the receive FIFO.

Register 0x65: RXCP LCD Count Threshold MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	LCDC[10]	0
Bit 1	R/W	LCDC[9]	0
Bit 0	R/W	LCDC[8]	1

Register 0x66: RXCP LCD Count Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	LCDC[7]	0
Bit 6	R/W	LCDC[6]	1
Bit 5	R/W	LCDC[5]	1
Bit 4	R/W	LCDC[4]	0
Bit 3	R/W	LCDC[3]	1
Bit 2	R/W	LCDC[2]	0
Bit 1	R/W	LCDC[1]	0
Bit 0	R/W	LCDC[0]	0

LCDC[10:0]:

The LCDC[10:0] bits represent the number of consecutive cell periods the receive cell processor must be out of cell delineation before loss of cell delineation (LCD) is declared. Likewise, LCD is not de-asserted until receive cell processor is in cell delineation for the number of cell periods specified by LCDC[10:0].

The default value of LCD[10:0] is 360, which translates to an average cell period of 0.71 µs and a default LCD integration period of 255 µs.

Register 0x67: RXCP Idle Cell Header Pattern

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[3]	0
Bit 2	R/W	PTI[2]	0
Bit 1	R/W	PTI[1]	0
Bit 0	R/W	CLP	1

GFC[3:0]:

The GFC[3:0] bits contain the pattern to match in the first, second, third, and fourth bits of the first octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the RXCP Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern. Note that an all-zeros pattern must be present in the VPI and VCI fields of the idle or unassigned cell.

PTI[2:0]:

The PTI[2:0] bits contain the pattern to match in the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell, in conjunction with the Idle Cell Header Mask Register. The IDLEPASS bit in the RXCP Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern.

CLP:

The CLP bit contains the pattern to match in the eighth bit of the fourth octet of the 53-octet cell, in conjunction with the Match Header Mask Register. The IDLEPASS bit in the RXCP Configuration 2 Register must be set to logic zero to enable dropping of cells matching this pattern.

Register 0x68: RXCP Idle Cell Header Mask

Bit	Type	Function	Default
Bit 7	R/W	MGFC[3]	1
Bit 6	R/W	MGFC[2]	1
Bit 5	R/W	MGFC[1]	1
Bit 4	R/W	MGFC[0]	1
Bit 3	R/W	MPTI[3]	1
Bit 2	R/W	MPTI[2]	1
Bit 1	R/W	MPTI[1]	1
Bit 0	R/W	MCLP	1

MGFC[3:0]:

The MGFC[3:0] bits contain the mask pattern for the first, second, third, and fourth bits of the first octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MPTI[3:0]:

The MPTI[3:0] bits contain the mask pattern for the fifth, sixth, and seventh bits of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in any bit position enables the corresponding bit in the pattern register to be compared. A logic zero causes the masking of the corresponding bit.

MCLP:

The CLP bit contains the mask pattern for the eighth bit of the fourth octet of the 53-octet cell. This mask is applied to the Idle Cell Header Pattern Register to select the bits included in the cell filter. A logic one in this bit position enables the MCLP bit in the pattern register to be compared. A logic zero causes the masking of the MCLP bit.

Register 0x69: RXCP Corrected HCS Error Count

Bit	Type	Function	Default
Bit 7	R	CHCS[7]	X
Bit 6	R	CHCS[6]	X
Bit 5	R	CHCS[5]	X
Bit 4	R	CHCS[4]	X
Bit 3	R	CHCS[3]	X
Bit 2	R	CHCS[2]	X
Bit 1	R	CHCS[1]	X
Bit 0	R	CHCS[0]	X

CHCS[7:0]:

The CHCS[7:0] bits indicate the number of corrected HCS error events that occurred during the last accumulation interval. The contents of these registers are valid a maximum of 40 RCLK periods after a transfer is triggered by a write to one of RXCP's performance monitor counters or to the S/UNI-622-POS Master Reset, and Identity register.

Register 0x6A: RXCP Uncorrected HCS Error Count

Bit	Type	Function	Default
Bit 7	R	UHCS[7]	X
Bit 6	R	UHCS[6]	X
Bit 5	R	UHCS[5]	X
Bit 4	R	UHCS[4]	X
Bit 3	R	UHCS[3]	X
Bit 2	R	UHCS[2]	X
Bit 1	R	UHCS[1]	X
Bit 0	R	UHCS[0]	X

UHCS[7:0]:

The UHCS[7:0] bits indicate the number of uncorrectable HCS error events that occurred during the last accumulation interval. The contents of these registers are valid a maximum of 40 RCLK periods after a transfer is triggered by a write to one of RXCP's performance monitor counters or to the S/UNI-622-POS Master Reset and Identity register.

Register 0x6B: RXCP Receive Cell Counter LSB

Bit	Type	Function	Default
Bit 7	R	RCELL[7]	X
Bit 6	R	RCELL[6]	X
Bit 5	R	RCELL[5]	X
Bit 4	R	RCELL[4]	X
Bit 3	R	RCELL[3]	X
Bit 2	R	RCELL[2]	X
Bit 1	R	RCELL[1]	X
Bit 0	R	RCELL[0]	X

Register 0x6C: RXCP Receive Cell Counter

Bit	Type	Function	Default
Bit 7	R	RCELL[15]	X
Bit 6	R	RCELL[14]	X
Bit 5	R	RCELL[13]	X
Bit 4	R	RCELL[12]	X
Bit 3	R	RCELL[11]	X
Bit 2	R	RCELL[10]	X
Bit 1	R	RCELL[9]	X
Bit 0	R	RCELL[8]	X

Register 0x6D: RXCP Receive Cell Counter MSB

Bit	Type	Function	Default
Bit 7	R	RCELL[23]	X
Bit 6	R	RCELL[22]	X
Bit 5	R	RCELL[21]	X
Bit 4	R	RCELL[20]	X
Bit 3	R	RCELL[19]	X
Bit 2	R	RCELL[18]	X
Bit 1	R	RCELL[17]	X
Bit 0	R	RCELL[16]	X

RCELL[23:0]:

The RCELL[23:0] bits indicate the number of cells received and written into the receive FIFO during the last accumulation interval. Cells received and filtered due to HCS errors or Idle cell matches are not counted. The counter should be polled every second to avoid saturation. The contents of these registers are valid a maximum of 67 RCLK periods after a transfer is triggered by a write to one of RXCP's performance monitor counters or to the S/UNI-622-POS Master Reset and Identity register.

Register 0x6E: RXCP Idle Cell Counter LSB

Bit	Type	Function	Default
Bit 7	R	ICELL[7]	X
Bit 6	R	ICELL[6]	X
Bit 5	R	ICELL[5]	X
Bit 4	R	ICELL[4]	X
Bit 3	R	ICELL[3]	X
Bit 2	R	ICELL[2]	X
Bit 1	R	ICELL[1]	X
Bit 0	R	ICELL[0]	X

Register 0x6F: RXCP Idle Cell Counter

Bit	Type	Function	Default
Bit 7	R	ICELL[15]	X
Bit 6	R	ICELL[14]	X
Bit 5	R	ICELL[13]	X
Bit 4	R	ICELL[12]	X
Bit 3	R	ICELL[11]	X
Bit 2	R	ICELL[10]	X
Bit 1	R	ICELL[9]	X
Bit 0	R	ICELL[8]	X

Register 0x70: RXCP Idle Cell Counter MSB

Bit	Type	Function	Default
Bit 7	R	ICELL[23]	X
Bit 6	R	ICELL[22]	X
Bit 5	R	ICELL[21]	X
Bit 4	R	ICELL[20]	X
Bit 3	R	ICELL[19]	X
Bit 2	R	ICELL[18]	X
Bit 1	R	ICELL[17]	X
Bit 0	R	ICELL[16]	X

ICELL[23:0]:

The ICELL[23:0] bits indicate the number of idle cells received during the last accumulation interval. The counter should be polled every second to avoid saturation. The contents of these registers are valid a maximum of 67 RCLK periods after a transfer is triggered by a write to one of RXCP's performance monitor counters or to the S/UNI-622-POS's Master Reset, and Identity register.

Register 0x80: TXCP Configuration 1

Bit	Type	Function	Default
Bit 7	R/W	TPTYP	0
Bit 6	R/W	TCALEVEL0	0
Bit 5	R/W	HSCR	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	HCSB	0
Bit 2	R/W	HCSADD	1
Bit 1	R/W	DSCR	0
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the four cell transmit FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST. Null/unassigned cells are transmitted until a subsequent cell is written to the FIFO.

DSCR:

The DSCR bit controls the scrambling of the cell payload. When DSCR is a logic one, cell payload scrambling is disabled. When DSCR is a logic zero, payload scrambling is enabled.

HCSADD:

The HCSADD bit controls the addition of the coset polynomial, $x^6+x^4+x^2+1$, to the HCS octet prior to insertion in the synchronous payload envelope. When HCSADD is a logic one, the polynomial is added, and the resulting HCS is inserted. When HCSADD is a logic zero, the polynomial is not added, and the unmodified HCS is inserted. HCSADD takes effect unconditionally regardless of whether a null/unassigned cell is being transmitted or whether the HCS octet has been read from the FIFO.

HCSB:

The active low HCSB bit enables the internal generation and insertion of the HCS octet into the transmit cell stream. When HCSB is logic zero, the HCS is

generated and inserted internally. If HCSB is logic one, then no HCS octet is inserted in the transmit data stream.

HSCR:

The Header Scramble enable bit, HSCR, enables scrambling of the ATM five octet header along with the payload. When set to logic one, the ATM header and payload are both scrambled. When set to logic zero, the header is left unscrambled and payload scrambling is determined by the DSCR bit.

TCALEVEL0:

The TCA level control (TCALEVEL0) determines when the TCA will transition low as the FIFO fills for Level 2 operation. When TCALEVEL0 is logic zero, TCA will deassert on the same rising TFCLK edge that samples word 21 of the 27 word ATM cell structure. When TCALEVEL0 is logic one, TCA will deassert on the same rising TFCLK edge that samples word 26 of the 27 word ATM cell structure.

TCALEVEL0 must be set low when the system interface is configured for Level 3 operation.

TPTYP:

The TPTYP bit selects even or odd parity for input TPRTY for Level 2 operation. When set to logic one, input TPRTY is the even parity bit for the TDAT input bus. When set to logic zero, input TPRTY is the odd parity bit for the TDAT input bus.

TPTYP must be set low when the system interface is configured for Level 3 operation.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0x81: TXCP Configuration 2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	TCAINV	0
Bit 3	R/W	FIFODP[1]	0
Bit 2	R/W	FIFODP[0]	0
Bit 1	R/W	DHCS	0
Bit 0	R/W	HCSCTLEB	0

HCSCTLEB:

The active low HCS control enable, HCSCTLEB bit enables the XORing of the HCS Control byte with the generated HCS. When set to logic zero, the HCS Control byte provided in the third word of the 27 word data structure is XORed with the generated HCS. When set to logic one, XORing is disabled and the HCS Control byte is ignored.

For normal operation, the HCS Control byte in the ATM cell structure transferred on the system interface should always be 0x00. If not, the HCSCTLEB register should be set to logic one to prevent corruption of the HCS byte.

DHCS:

The DHCS bit controls the insertion of HCS errors for diagnostic purposes. When DHCS is set to logic one, the HCS octet is inverted prior to insertion in the synchronous payload envelope. DHCS takes effect unconditionally regardless of whether a null/unassigned cell is being transmitted or whether the HCS octet has been read from the FIFO. DHCS occurs after any error insertion caused by the Control Byte in the 27-word data structure.

FIFODP[1:0]:

The FIFODP[1:0] bits determine the transmit FIFO cell depth at which TCA is de-asserted. FIFO depth control may be important in systems where the cell latency through the TXCP must be minimized. When the FIFO is filled to the specified depth, the transmit cell available signal, TCA is deasserted. Note that regardless of what fill level FIFODP[1:0] is set to, the transmit cell

processor can store 4 complete cells. The selectable FIFO cell depths are shown below:

FIFODP[1]	FIFODP[0]	FIFO DEPTH
0	0	4 cells
0	1	3 cells
1	0	2 cells
1	1	1 cell

TCAINV:

The TCAINV bit inverts the polarity of the TCA output signal for Level 2 operation. When TCAINV is a logic one, the polarity of TCA is inverted (TCA at logic zero means there is transmit cell space available to be written to). When TCAINV is a logic zero, the polarity of TCA is not inverted.

TCAINV must be set low when the system interface is configured for Level 3 operation.

Register 0x82: TXCP Cell Count Status

Bit	Type	Function	Default
Bit 7	R/W	XFERE	0
Bit 6	R	XFERI	X
Bit 5	R	OVR	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	1
Bit 2	R/W	Reserved	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

XFERI:

The XFERI bit indicates that a transfer of Transmit Cell Count data has occurred. A logic one in this bit position indicates that the Transmit Cell Count registers have been updated. This update is initiated by writing to one of the Transmit Cell Count register locations or to the S/UNI-622-POS, Master Reset and Identity register. XFERI is set low when this register is read.

OVR:

The OVR bit is the overrun status of the Transmit Cell Count registers. A logic one in this bit position indicates that a previous transfer (indicated by XFERI being logic one) has not been acknowledged before the next accumulation interval has occurred and that the contents of the Transmit Cell Count registers have been overwritten. OVR is set low when this register is read.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the Transmit Cell Count registers. When XFERE is set high, the interrupt is enabled.

Reserved:

These bits should be set to their default values for proper operation.

Register 0x83: TXCP Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	TPRTYE	0
Bit 6	R/W	FOVRE	0
Bit 5	R/W	TSOCE	0
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	TPRTYI	X
Bit 1	R	FOVRI	X
Bit 0	R	TSOCI	X

TSOCI:

The TSOCI bit is set high when the TSOC input is sampled high during any position other than the first word of the selected data structure. The write address counter is reset to the first word of the data structure when TSOC is sampled high. This bit is reset immediately after a read to this register.

FOVRI:

The FOVRI bit is set high when an attempt is made to write into the FIFO when it is already full. This bit is reset immediately after a read to this register.

TPRTYI:

The TPRTYI bit indicates if a parity error was detected on the TDAT input bus. When logic one, the TPRTYI bit indicates a parity error over the active TDAT bus. This bit is cleared when this register is read. Odd or even parity is selected using the TPTYP bit.

TSOCE:

The TSOCE bit enables the generation of an interrupt when the TSOC input is sampled high during any position other than the first word of the selected data structure. When TSOCE is set to logic one, the interrupt is enabled.

FOVRE:

The FOVRE bit enables the generation of an interrupt due to an attempt to write the FIFO when it is already full. When FOVRE is set to logic one, the interrupt is enabled.

TPRTYE:

The TPRTYE bit enables transmit parity interrupts. When set to logic one, parity errors are indicated on INTB and TPRTYI. When set to logic zero, parity errors are indicated using bit TPRTYI, but are not indicated on output INTB.

Register 0x84: TXCP Idle Cell Header Control

Bit	Type	Function	Default
Bit 7	R/W	GFC[3]	0
Bit 6	R/W	GFC[2]	0
Bit 5	R/W	GFC[1]	0
Bit 4	R/W	GFC[0]	0
Bit 3	R/W	PTI[2]	0
Bit 2	R/W	PTI[1]	0
Bit 1	R/W	PTI[0]	0
Bit 0	R/W	CLP	1

CLP:

The CLP bit contains the eighth bit position of the fourth octet of the idle/unassigned cell pattern. Cell rate decoupling is accomplished by transmitting idle cells when the TXCP detects that no outstanding cells exist in the transmit FIFO.

PTI[3:0]:

The PTI[3:0] bits contain the fifth, sixth, and seventh bit positions of the fourth octet of the idle/unassigned cell pattern. Idle cells are transmitted when the TXCP detects that no outstanding cells exist in the transmit FIFO.

GFC[3:0]:

The GFC[3:0] bits contain the first, second, third, and fourth bit positions of the first octet of the idle/unassigned cell pattern. Idle/unassigned cells are transmitted when the TXCP detects that no outstanding cells exist in the transmit FIFO. The all zeros pattern is transmitted in the VCI and VPI fields of the idle cell.

Register 0x85: TXCP Idle Cell Payload Control

Bit	Type	Function	Default
Bit 7	R/W	PAYLD[7]	0
Bit 6	R/W	PAYLD[6]	1
Bit 5	R/W	PAYLD[5]	1
Bit 4	R/W	PAYLD[4]	0
Bit 3	R/W	PAYLD[3]	1
Bit 2	R/W	PAYLD[2]	0
Bit 1	R/W	PAYLD[1]	1
Bit 0	R/W	PAYLD[0]	0

PAYLD[7:0]:

The PAYLD[7:0] bits contain the pattern inserted in the idle cell payload. Idle cells are inserted when the TXCP detects that the transmit FIFO contains no outstanding cells. PAYLD[7] is the most significant bit and is the first bit transmitted. PAYLD[0] is the least significant bit.

Register 0x86: TXCP Transmit Cell Count LSB

Bit	Type	Function	Default
Bit 7	R	TCELL[7]	X
Bit 6	R	TCELL[6]	X
Bit 5	R	TCELL[5]	X
Bit 4	R	TCELL[4]	X
Bit 3	R	TCELL[3]	X
Bit 2	R	TCELL[2]	X
Bit 1	R	TCELL[1]	X
Bit 0	R	TCELL[0]	X

Register 0x87: TXCP Transmit Cell Count

Bit	Type	Function	Default
Bit 7	R	TCELL[15]	X
Bit 6	R	TCELL[14]	X
Bit 5	R	TCELL[13]	X
Bit 4	R	TCELL[12]	X
Bit 3	R	TCELL[11]	X
Bit 2	R	TCELL[10]	X
Bit 1	R	TCELL[9]	X
Bit 0	R	TCELL[8]	X

Register 0x88: TXCP Transmit Cell Count MSB

Bit	Type	Function	Default
Bit 7	R	TCELL[23]	X
Bit 6	R	TCELL[22]	X
Bit 5	R	TCELL[21]	X
Bit 4	R	TCELL[20]	X
Bit 3	R	TCELL[19]	X
Bit 2	R	TCELL[18]	X
Bit 1	R	TCELL[17]	X
Bit 0	R	TCELL[16]	X

TCELL[23:0]:

The TCELL[23:0] bits indicate the number of cells read from the transmit FIFO and inserted into the transmission stream during the last accumulation interval. Idle cells inserted into the transmission stream are not counted.

A write to any one of the TXCP Transmit Cell Counter registers or to the S/UNI-622-POS Master Reset and Identity register loads the registers with the current counter value and resets the internal 19 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Cell Counter registers. The counter should be polled every second to avoid saturating. The contents of these registers are valid after a maximum of 67 TCLK cycles after a transfer is triggered by a write to a TXCP Transmit Cell count Register or the S/UNI-622-POS Master Reset and Identity register.

Register 0x90: RUL3 Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	RL3PP	0
Bit 3		Unused	X
Bit 2	R/W	RMOVR	0
Bit 1	R/W	RPOS_ATMB	X
Bit 0	R/W	RSYSSEL	X

RSYSSEL:

The Receive System Interface Select RSYSSEL allows the SYSSEL pin to be observed and overridden by software. When the RMOVR bit is set low, the RSYSSEL bit is read-only and reports the status of the SYSSEL pin. When RMOVR is set high, the value of the RSYSSEL bit is used to determine the system mode and the SYSEL pin is ignored.

When RMOVR is set high and RSYSSEL is set low, the receive side of the system interface is configured for Level 2 operation. When RMOVR is set high and RSYSSEL is set high, the receive side of the system interface is configured for Level 3 operation.

RPOS_ATMB:

The Receive ATM/POS Mode Select RPOS_ATMB allows the POS_ATMB pin to be observed and overridden by software. When the RMOVR bit is set low, the RPOS_ATMB bit is read-only and reports the status of the POS_ATMB pin. When RMOVR is set high, the value of the RPOS_ATMB bit is used to determine the receive side of the system interface mode and the POS_ATMB pin is ignored. When RMOVR is set high and RPOS_ATMB is set low, the receive side of the system interface is configured for ATM cells. When RMOVR is set high and RPOS_ATMB is set high, the system interface is configured for packet data.

RMOVR:

The Receive Mode Over-Ride bit RMOVR enables the RSYSSEL and RPOS_ATMB bits to override the mode selected by the SYSSEL and

POS_ATMB pins. When RMOVR is low, the receive side of the system interface is selected by the external pins, and can be read from the RSYSSEL and RPOS_ATMB register bits. When RMOVR is high, the mode is controlled by writing to the RSYSSEL and RPOS_ATMB bits, and the external mode pins are ignored.

RL3PP:

The Receive Level 3 Parity RL3PP bit selects even or odd parity for output RPRTY when the system interface is configured for Level 3 operation. When set high, output RPRTY is the even parity bit for outputs RDAT[7:0]. When RL3PP is set to low, RPRTY is the odd parity bit for outputs RDAT[7:0]. RL3PP is ignored when the system interface is configured for Level 2 operation.

RL3PP is ignored when the system interface is configured for Level 2 operation.

Register 0x92: TUL3 Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	TL3PP	0
Bit 3		Unused	X
Bit 2	R/W	TMOVR	0
Bit 1	R/W	TPOS_ATMB	X
Bit 0	R/W	TSYSSEL	X

TSYSSEL:

The Transmit System Interface Select TSYSSEL allows the SYSSEL pin to be observed and overridden by software. When the TMOVR bit is set low, the TSYSSEL bit is read-only and reports the status of the SYSSEL pin. When TMOVR is set high, the value of the TSYSSEL bit is used to determine the system mode and the SYSEL pin is ignored.

When TMOVR is set high and TSYSSEL is set low, the transmit side of the system interface is configured for Level 2 operation. When TMOVR is set high and TSYSSEL is set high, the transmit side of the system interface is configured for Level 3 operation.

TPOS_ATMB:

The Transmit ATM/POS Mode Select TPOS_ATMB allows the POS_ATMB pin to be observed and overridden by software. When the TMOVR bit is set low, the TPOS_ATMB bit is read-only and reports the status of the POS_ATMB pin. When TMOVR is set high, the value of the RPOS_ATMB bit is used to determine the system interface mode and the POS_ATMB pin is ignored. When TMOVR is set high and TPOS_ATMB is set low, the transmit side of the system interface is configured for ATM cells. When TMOVR is set high and TPOS_ATMB is set high, the transmit side of the system interface is configured for packet data.

TMOVR:

The Transmit Mode Over-Ride bit TMOVR enables the TSYSSEL and TPOS_ATMB bits to override the mode selected by the SYSSEL and

POS_ATMB pins. When TMOVR is low, the system interface mode is selected by the external pins, and can be read from the TSYSSEL and TPOS_ATMB register bits. When TMOVR is high, the mode is controlled by writing to the TSYSSEL and TPOS_ATMB bits, and the external mode pins are ignored.

TL3PP:

The Transmit Level 3 Parity TL3PP bit selects even or odd parity for input RPRTY when the system interface is configured for Level 3 operation. When set high, input TPRTY is the even parity bit for inputs TDAT[7:0]. When TL3PP is set to low, TPRTY is the odd parity bit for input RDAT[7:0]. TL3PP is ignored when the system interface is configured for Level 2 operation.

TL3PP is ignored when the system interface is configured for Level 2 operation.

Register 0x94: DLL RUL3 Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The DLL Configuration Register controls the basic operation of the DLL for the receive system interface clock RFCLK.

Register 0x96: DLL RUL3 Delay Tap Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

Writing to this register performs a software reset of the DLL. The software reset will disrupt the Receive Level 2/3 interface controlled by RFCLK clock. Any FIFOs associated with the RFCLK (RXCP and RXFP) must be reset using FIFORST after the DLL is reset.

Register 0x97: DLL RUL3 Control Status

Bit	Type	Function	Default
Bit 7	R	RFCLKI	X
Bit 6	R	Reserved	X
Bit 5	R	ERRORI	X
Bit 4	R	Reserved	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Reserved	X
Bit 0	R	RUN	X

The DLL Control Status Register provides information of the DLL operation.

RUN:

The DLL lock status register bit RUN indicates the DLL has found an initial lock condition. When the phase detector first indicates lock, RUN is set high. The RUN register bit is cleared only by a system reset or a software reset.

ERROR:

The delay line error register ERROR indicates the DLL is currently at the end of the delay line. ERROR is set high when the DLL tries to move beyond the end of the delay line.

ERRORI:

The error event register bit ERRORI indicates the ERROR register bit has been a logic one. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

RFCLKI:

The clock event register bit RFCLKI provides a method to monitor activity on the RFCLK clock. When the RFCLK input changes from a logic zero to a logic one, the RFCLKI register bit is set to logic one. The RFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Register 0x98: DLL TUL3 Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The DLL Configuration Register controls the basic operation of the DLL for the receive system interface clock TFCLK.

Register 0x9A: DLL TUL3 Delay Tap Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

Writing to this register performs a software reset of the DLL. The software reset will disrupt the Transmit Level 2/3 interface controlled by TFCLK clock. Any FIFOs associated with the TFCLK (TXCP and TXFP) must be reset using FIFORST after the DLL is reset.

Register 0x9B: DLL TUL3 Control Status

Bit	Type	Function	Default
Bit 7	R	TFCLKI	X
Bit 6	R	Reserved	X
Bit 5	R	ERRORI	X
Bit 4	R	Reserved	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Reserved	X
Bit 0	R	RUN	X

The DLL Control Status Register provides information of the DLL operation.

RUN:

The DLL lock status register bit RUN indicates the DLL has found an initial lock condition. When the phase detector first indicates lock, RUN is set high. The RUN register bit is cleared only by a system reset or a software reset.

ERROR:

The delay line error register ERROR indicates the DLL is currently at the end of the delay line. ERROR is set high when the DLL tries to move beyond the end of the delay line.

ERRORI:

The error event register bit ERRORI indicates the ERROR register bit has been a logic one. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

TFCLKI:

The clock event register bit TFCLKI provides a method to monitor activity on the TFCLK clock. When the TFCLK input changes from a logic zero to a logic one, the TFCLKI register bit is set to logic one. The TFCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Register 0x9C: DLL Parallel Transmit Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	OVERRIDE	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

The DLL Configuration Register controls the basic operation of the DLL for the receive system interface clock PTCLK.

OVERRIDE:

The override control (OVERRIDE) disables the DLL operation. When OVERRIDE is set low, the DLL generates the internal clock by delaying the PTCLK to ensure the best possible output propagation on the system interface. When OVERRIDE is set high, the system interface output propagation will not meet the specified timing. This feature provides a back-up strategy for very low frequency PTCLK operation.

Register 0x9E: DLL Parallel Transmit Delay Tap Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	Reserved	X
Bit 5	R	Reserved	X
Bit 4	R	Reserved	X
Bit 3	R	Reserved	X
Bit 2	R	Reserved	X
Bit 1	R	Reserved	X
Bit 0	R	Reserved	X

Writing to this register performs a software reset of the DLL. The software reset will disrupt the Transmit parallel interface controlled by PTCLK clock.

Register 0x9F: DLL Parallel Transmit Control Status

Bit	Type	Function	Default
Bit 7	R	PTCLKI	X
Bit 6	R	Reserved	X
Bit 5	R	ERRORI	X
Bit 4	R	Reserved	X
Bit 3		Unused	X
Bit 2	R	ERROR	X
Bit 1	R	Reserved	X
Bit 0	R	RUN	X

The DLL Control Status Register provides information of the DLL operation.

RUN:

The DLL lock status register bit RUN indicates the DLL has found an initial lock condition. When the phase detector first indicates lock, RUN is set high. The RUN register bit is cleared only by a system reset or a software reset.

ERROR:

The delay line error register ERROR indicates the DLL is currently at the end of the delay line. ERROR is set high when the DLL tries to move beyond the end of the delay line.

ERRORI:

The error event register bit ERRORI indicates the ERROR register bit has been a logic one. When the ERROR register changes from a logic zero to a logic one, the ERRORI register bit is set to logic one. The ERRORI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

PTCLKI:

The clock event register bit PTCLKI provides a method to monitor activity on the PTCLK clock. When the PTCLK input changes from a logic zero to a logic one, the PTCLKI register bit is set to logic one. The PTCLKI register bit is cleared immediately after it is read, thus acknowledging the event has been recorded.

Register 0xA0: RXFP Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	FCSPASS	0
Bit 5	R/W	RPAINV	0
Bit 4	R/W	FCSSEL[1]	1
Bit 3	R/W	FCSSEL[0]	0
Bit 2	R/W	RXPTYP	0
Bit 1	R/W	DDSCR	1
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the 256-byte receive FIFO. When FIFORST is set low, the FIFO operates normally. When FIFORST is set high, the FIFO is immediately emptied and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST.

DDSCR:

The DDSCR bit controls the descrambling of the frame payload with the polynomial $x^{43} + 1$. When DDSCR is set low, frame payload descrambling is disabled. When DDSCR is set high, payload descrambling is enabled.

RXPTYP:

The RXPTYP bit selects even or odd parity for output RPRTY for Level 2 operation. When set high, output RPRTY is the even parity bit for outputs RDAT[15:0]. When RXPTYP is set low, RPRTY is the odd parity bit for outputs RDAT[15:0].

RXPTYP must be set low when the system interface is configured for Level 3 operation.

FCSSEL[1:0]:

The Frame Control Sequence select (FCSSEL[1:0]) bits control the FCS calculation according to the table below. The FCS is calculated over the whole packet data, after byte destuffing and descrambling.

FCSSEL[1:0]	FCS Operation
00	No FCS calculated
01	CRC-CCITT (2 bytes)
10	CRC-32 (4 bytes)
11	Reserved

RPAINV:

The RPAINV bit inverts the polarity of the RPA output signal for Level 2 operation. When RPAINV is a logic one, the polarity of RPA is inverted (RPA at logic zero means there is a receive cell available to be read). When RPAINV is a logic zero, the polarity of RPA is not inverted.

RPAINV must be set low when the system interface is configured for Level 3 operation.

FCSPASS:

FCSPASS determines if the FCS field will be passed through the system interface or stripped. When FCSPASS is set to logic one, the POS frame FCS field is written into the FIFO as part of the packet, and can thus be read through the system interface. When FCSPASS is set to logic zero, the FCS field is stripped from the POS frame.

Reserved:

The reserved bit must be programmed to logic zero for proper operation.

Register 0xA1: RXFP Configuration/Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	MINLE	0
Bit 4	R/W	MAXLE	0
Bit 3	R/W	ABRTE	0
Bit 2	R/W	FCSE	0
Bit 1	R/W	FOVRE	0
Bit 0	R/W	Reserved	0

FOVRE:

The FOVRE bit enables the generation of an interrupt due to a FIFO overrun error condition. When FOVRE is set high, the interrupt is enabled.

FCSE:

The FCSE bit enables the generation of an interrupt due to the detection of an FCS error. When FCSE is set high, the interrupt is enabled.

ABRTE:

The Abort Packet Enable bit enables the generation of an interrupt due to the reception of an aborted packet. When ABRTE is set high, the interrupt is enabled.

MAXLE:

The Maximum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet exceeding the programmable maximum packet length. When MAXLE is set high, the interrupt is enabled.

MINLE:

The Minimum Length Packet Enable bit enables the generation of an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. When MINLE is set high, the interrupt is enabled.

Reserved:

The reserved bit must be programmed to logic zero for proper operation.

Register 0xA2: RXFP Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	MINLI	X
Bit 4	R	MAXLI	X
Bit 3	R	ABRTI	X
Bit 2	R	FCSI	X
Bit 1	R	FOVRI	X
Bit 0		Unused	X

FOVRI:

The FOVRI bit indicates an interrupt due to a FIFO overrun error condition. This interrupt can be masked using FOVRE.

FCSI:

The FCSI bit indicates an interrupt due to the detection of an FCS error. This interrupt can be masked using FCSE.

ABRTI:

The ABRTI bit indicates the generation of an interrupt due to the reception of an aborted packet. This interrupt can be masked using ABRTE.

MAXLI:

The MAXLI bit indicates an interrupt due to the reception of a packet exceeding the programmable maximum packet length. This interrupt can be masked using MAXLE.

MINLI:

The MINLI bit indicates an interrupt due to the reception of a packet that is smaller than the programmable minimum packet length. This interrupt can be masked using MINLE.

Register 0xA3: RXFP Minimum Packet Length

Bit	Type	Function	Default
Bit 7	R/W	MINPL[7]	0
Bit 6	R/W	MINPL[6]	0
Bit 5	R/W	MINPL[5]	0
Bit 4	R/W	MINPL[4]	0
Bit 3	R/W	MINPL[3]	0
Bit 2	R/W	MINPL[2]	1
Bit 1	R/W	MINPL[1]	0
Bit 0	R/W	MINPL[0]	0

MINPL[7:0]:

The Minimum Packet Length (MINPL[7:0]) bits are used to set the minimum packet length. Packets smaller than this length are marked with an error. The packet length used here is defined as the number of bytes encapsulated into the POS frame, including the FCS but excluding byte stuffing.

Register 0xA4: RXFP Maximum Packet Length LSB

Bit	Type	Function	Default
Bit 7	R/W	MAXPL[7]	0
Bit 6	R/W	MAXPL[6]	0
Bit 5	R/W	MAXPL[5]	0
Bit 4	R/W	MAXPL[4]	0
Bit 3	R/W	MAXPL[3]	0
Bit 2	R/W	MAXPL[2]	0
Bit 1	R/W	MAXPL[1]	0
Bit 0	R/W	MAXPL[0]	0

Register 0xA5: RXFP Maximum Packet Length MSB

Bit	Type	Function	Default
Bit 7	R/W	MAXPL[15]	0
Bit 6	R/W	MAXPL[14]	0
Bit 5	R/W	MAXPL[13]	0
Bit 4	R/W	MAXPL[12]	0
Bit 3	R/W	MAXPL[11]	0
Bit 2	R/W	MAXPL[10]	1
Bit 1	R/W	MAXPL[9]	1
Bit 0	R/W	MAXPL[8]	0

MAXPL[15:0]:

The Maximum Packet Length (MAXPL[15:0]) bits are used to set the maximum packet length. Packets larger than this length are marked with an error. The packet length used here is defined as the number of bytes encapsulated into the POS frame, including the FCS but excluding byte stuffing.

The maximum packet length supported by the RXFP is 65534 bytes (0xFFFE).

Register 0xA6: RXFP Receive Initiation Level

Bit	Type	Function	Default
Bit 7	R/W	Reserved	1
Bit 6	R/W	Reserved	0
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	RIL[3]	1
Bit 2	R/W	RIL[2]	1
Bit 1	R/W	RIL[1]	0
Bit 0	R/W	RIL[0]	0

RIL[3:0]:

The Reception Initiation Level (RIL[3:0]) bits are used to set the minimum number of bytes that must be available in the FIFO before received packets can be written into it. RIL[3:0] is only used after a FIFO overrun has been detected and FIFO writes have been suspended. This avoids restarting the reception of data too quickly after an overrun condition. If the system does not cause any FIFO overrun, then this register will not be used. RIL[3:0] breaks the FIFO in 16 sections; for example a value of 0x4 correspond to a FIFO level of 64 bytes. The value of RIL must not be too large in order to prevent repetitive FIFO overruns.

Table 7: Receive Initiation Level Values

RIL[3:0]	FIFO Fill Level	RIL[3:0]	FIFO Fill Level
0000	0	1000	128
0001	16	1001	144
0010	32	1010	160
0011	48	1011	176
0100	64	1100	192
0101	80	1101	208
0110	96	1110	224
0111	112	1111	240

Reserved:

These bits must be programmed as indicated by the default column.

Register 0xA7: RXFP Receive Packet Available High Water Mark

Bit	Type	Function	Default
Bit 7	R/W	RPAHWM[7]	0
Bit 6	R/W	RPAHWM[6]	1
Bit 5	R/W	RPAHWM[5]	0
Bit 4	R/W	RPAHWM[4]	0
Bit 3	R/W	RPAHWM[3]	0
Bit 2	R/W	RPAHWM[2]	0
Bit 1	R/W	RPAHWM[1]	0
Bit 0	R/W	RPAHWM[0]	0

RPAHWM[7:0]:

The Receive FIFO High Water Mark (RPAHWM[7:0]) bits are used to generate the RPA output in POS-PHY Level 2 interface. RPA is set to logic one when the number of bytes stored in the FIFO exceeds RPAHWM[7:0] or when there is at least one end of packet in the FIFO. The RPAHWM value is used to determine when data is transferred on the POS-PHY Level 3 interface.

The programmed value for RPAHWM[7:0] must be less than 0xF0 and greater than 0x00 for proper operation.

When a packet with less than 6 bytes arrives (from the line side), the receive packet available signal (RPA) may assert before data is available. In this condition, RPA will assert between 1 to 3 RFCLK clock cycles before the data is available and will remain asserted for 1 to 3 RFCLK clock cycles. When the Link Layer device attempts to read the packet by asserting read enable (RENB), it may find that there is no valid data available (receive data valid signal (RVAL) remains de-asserted). RPA will correctly assert again later when data is available. At this time the RVAL signal will be asserted indicating valid data.

With packets greater than 6 bytes, the RPA signal will assert, de-assert and then reassert 1 to 3 RFCLK cycles later (same as the above case with packets less than 6 bytes). However, if the Link layer device attempts to read the packet on the basis of the first occurrence of RPA, it will read valid data (RVAL will be asserted), even if RPA may be de-asserted.

This early assertion of RPA will not cause any data corruption if RVAL is used to qualify the data that is read. It is recommended that RVAL always be used to qualify receive data. The operation of RPA may cause a slight reduction bandwidth on receive side of the POS-PHY interface. However, since there is ample bandwidth on the POS-PHY interface there will be no impact on performance of functionality.

Register 0xA8: RXFP Receive Byte Count LSB

Bit	Type	Function	Default
Bit 7	R	RBYTE[7]	X
Bit 6	R	RBYTE[6]	X
Bit 5	R	RBYTE[5]	X
Bit 4	R	RBYTE[4]	X
Bit 3	R	RBYTE[3]	X
Bit 2	R	RBYTE[2]	X
Bit 1	R	RBYTE[1]	X
Bit 0	R	RBYTE[0]	X

Register 0xA9: RXFP Receive Byte Count

Bit	Type	Function	Default
Bit 7	R	RBYTE[15]	X
Bit 6	R	RBYTE[14]	X
Bit 5	R	RBYTE[13]	X
Bit 4	R	RBYTE[12]	X
Bit 3	R	RBYTE[11]	X
Bit 2	R	RBYTE[10]	X
Bit 1	R	RBYTE[9]	X
Bit 0	R	RBYTE[8]	X

Register 0xAA: RXFP Receive Byte Count

Bit	Type	Function	Default
Bit 7	R	RBYTE[23]	X
Bit 6	R	RBYTE[22]	X
Bit 5	R	RBYTE[21]	X
Bit 4	R	RBYTE[20]	X
Bit 3	R	RBYTE[19]	X
Bit 2	R	RBYTE[18]	X
Bit 1	R	RBYTE[17]	X
Bit 0	R	RBYTE[16]	X

Register 0xAB: RXFP Receive Byte Count MSB

Bit	Type	Function	Default
Bit 7	R	RBYTE[31]	X
Bit 6	R	RBYTE[30]	X
Bit 5	R	RBYTE[29]	X
Bit 4	R	RBYTE[28]	X
Bit 3	R	RBYTE[27]	X
Bit 2	R	RBYTE[26]	X
Bit 1	R	RBYTE[25]	X
Bit 0	R	RBYTE[24]	X

RBYTE[31:0]:

The RBYTE[31:0] bits indicate the number of received bytes written into the receive FIFO during the last accumulation interval. This counter does not count any byte from errored and aborted frames.

A write to any one of the RXFP Receive Byte Counter registers or the S/UNI-622-POS Master Reset and Identity register loads the registers with the current counter value and resets the internal 24 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Receive Byte Counter registers. The counter should be polled every second to avoid saturating. The contents of these

registers are valid three RCLK cycles after a transfer is triggered by a write to any of the RXFP Receive Frame Count Registers.

Register 0xAC: RXFP Receive Frame Count LSB

Bit	Type	Function	Default
Bit 7	R	RFRAME[7]	X
Bit 6	R	RFRAME[6]	X
Bit 5	R	RFRAME[5]	X
Bit 4	R	RFRAME[4]	X
Bit 3	R	RFRAME[3]	X
Bit 2	R	RFRAME[2]	X
Bit 1	R	RFRAME[1]	X
Bit 0	R	RFRAME[0]	X

Register 0xAD: RXFP Receive Frame Count

Bit	Type	Function	Default
Bit 7	R	RFRAME[15]	X
Bit 6	R	RFRAME[14]	X
Bit 5	R	RFRAME[13]	X
Bit 4	R	RFRAME[12]	X
Bit 3	R	RFRAME[11]	X
Bit 2	R	RFRAME[10]	X
Bit 1	R	RFRAME[9]	X
Bit 0	R	RFRAME[8]	X

Register 0xAE: RXFP Receive Frame Count MSB

Bit	Type	Function	Default
Bit 7	R	RFRAME[23]	X
Bit 6	R	RFRAME[22]	X
Bit 5	R	RFRAME[21]	X
Bit 4	R	RFRAME[20]	X
Bit 3	R	RFRAME[19]	X
Bit 2	R	RFRAME[18]	X
Bit 1	R	RFRAME[17]	X
Bit 0	R	RFRAME[16]	X

RFRAME[23:0]:

The RFRAME[23:0] bits indicate the number of successfully received POS frames written into the receive FIFO after their extraction from the SONET/SDH stream during the last accumulation interval. This counter does not count any errored and aborted frames.

A write to any one of the RXFP Receive Frame Counter registers or S/UNI-622-POS the Master Reset and Identity register loads the registers with the current counter value and resets the internal 24 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Receive Frame Counter registers. The counter should be polled every second to avoid saturating. The contents of these registers are valid three RCLK cycles after a transfer is triggered by a write to any of the RXFP Receive Frame Count Registers.

Register 0xAF: RXFP Receive Aborted Frame Count LSB

Bit	Type	Function	Default
Bit 7	R	RABRF[7]	X
Bit 6	R	RABRF[6]	X
Bit 5	R	RABRF[5]	X
Bit 4	R	RABRF[4]	X
Bit 3	R	RABRF[3]	X
Bit 2	R	RABRF[2]	X
Bit 1	R	RABRF[1]	X
Bit 0	R	RABRF[0]	X

Register 0xB0: RXFP Receive Aborted Frame Count MSB

Bit	Type	Function	Default
Bit 7	R	RABRF[15]	X
Bit 6	R	RABRF[14]	X
Bit 5	R	RABRF[13]	X
Bit 4	R	RABRF[12]	X
Bit 3	R	RABRF[11]	X
Bit 2	R	RABRF[10]	X
Bit 1	R	RABRF[9]	X
Bit 0	R	RABRF[8]	X

RABRF[15:0]:

The RABRF[15:0] bits indicate the number of aborted POS frames received and written into the receive FIFO during the last accumulation interval.

A write to any one of the RXFP Receive Aborted Frame Counter registers or the S/UNI-622-POS Master Reset and Identity register loads the registers with the current counter value and resets the internal 16 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to these registers. The counter should be polled every second to avoid saturating. The contents of these registers are valid three RCLK cycles after a transfer is triggered.

Register 0xB1: RXFP Receive FCS Error Frame Count LSB

Bit	Type	Function	Default
Bit 7	R	RFCSEF[7]	X
Bit 6	R	RFCSEF[6]	X
Bit 5	R	RFCSEF[5]	X
Bit 4	R	RFCSEF[4]	X
Bit 3	R	RFCSEF[3]	X
Bit 2	R	RFCSEF[2]	X
Bit 1	R	RFCSEF[1]	X
Bit 0	R	RFCSEF[0]	X

Register 0xB2: RXFP Receive FCS Error Frame Count MSB

Bit	Type	Function	Default
Bit 7	R	RFCSEF[15]	X
Bit 6	R	RFCSEF[14]	X
Bit 5	R	RFCSEF[13]	X
Bit 4	R	RFCSEF[12]	X
Bit 3	R	RFCSEF[11]	X
Bit 2	R	RFCSEF[10]	X
Bit 1	R	RFCSEF[9]	X
Bit 0	R	RFCSEF[8]	X

RFCSEF[15:0]:

The RFCSEF[15:0] bits indicate the number of POS frames received with an FCS error and written into the receive FIFO during the last accumulation interval.

A write to any one of the RXFP Receive FCS Error Frame Counter registers or the S/UNI-622-POS Master Reset and Identity register loads the registers with the current counter value and resets the internal 16 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to these registers. The counter should be polled every

second to avoid saturating. The contents of these registers are valid three RCLK cycles after a transfer is triggered.

Register 0xB3: RXFP Receive Minimum Length Error Frame Count LSB

Bit	Type	Function	Default
Bit 7	R	RMINLF[7]	X
Bit 6	R	RMINLF[6]	X
Bit 5	R	RMINLF[5]	X
Bit 4	R	RMINLF[4]	X
Bit 3	R	RMINLF[3]	X
Bit 2	R	RMINLF[2]	X
Bit 1	R	RMINLF[1]	X
Bit 0	R	RMINLF[0]	X

Register 0xB4: RXFP Receive Minimum Length Error Frame Counter MSB

Bit	Type	Function	Default
Bit 7	R	RMINLF[15]	X
Bit 6	R	RMINLF[14]	X
Bit 5	R	RMINLF[13]	X
Bit 4	R	RMINLF[12]	X
Bit 3	R	RMINLF[11]	X
Bit 2	R	RMINLF[10]	X
Bit 1	R	RMINLF[9]	X
Bit 0	R	RMINLF[8]	X

RMINLF[15:0]:

The RMINLF[15:0] bits indicate the number of minimum packet length POS frames received and written into the receive FIFO during the last accumulation interval.

A write to any one of the RXFP Minimum Length Error Frame Counter registers or the S/UNI-622-POS Master Reset and Identity register loads the registers with the current counter value and resets the internal 16 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to these registers. The counter should be

polled every second to avoid saturating. The contents of these registers are valid three RCLK cycles after a transfer is triggered.

Register 0xB5: RXFP Receive Maximum Length Error Frame Counter LSB

Bit	Type	Function	Default
Bit 7	R	RMAXLF[7]	X
Bit 6	R	RMAXLF[6]	X
Bit 5	R	RMAXLF[5]	X
Bit 4	R	RMAXLF[4]	X
Bit 3	R	RMAXLF[3]	X
Bit 2	R	RMAXLF[2]	X
Bit 1	R	RMAXLF[1]	X
Bit 0	R	RMAXLF[0]	X

Register 0xB6: RXFP Receive Maximum Length Error Frame Counter MSB

Bit	Type	Function	Default
Bit 7	R	RMAXLF[15]	X
Bit 6	R	RMAXLF[14]	X
Bit 5	R	RMAXLF[13]	X
Bit 4	R	RMAXLF[12]	X
Bit 3	R	RMAXLF[11]	X
Bit 2	R	RMAXLF[10]	X
Bit 1	R	RMAXLF[9]	X
Bit 0	R	RMAXLF[8]	X

RMAXLF[15:0]:

The RMAXLF[15:0] bits indicate the number of POS frames exceeding the maximum packet length that were received and written into the receive FIFO during the last accumulation interval.

A write to any one of the RXFP Receive Maximum Length Error Frame Counter registers or the S/UNI-622-POS Master Reset and Identity register loads the registers with the current counter value and resets the internal 16 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to these registers. The counter

should be polled every second to avoid saturating. The contents of these registers are valid three RCLK cycles after a transfer is triggered.

Register 0xC0: TXFP Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R	FIFOERR	X
Bit 5	R/W	FUDRE	0
Bit 4	R	FUDRI	X
Bit 3	R/W	FOVRE	0
Bit 2	R	FOVRI	X
Bit 1	R/W	TPRTYE	0
Bit 0	R	TPRTYI	X

TPRTYI:

The TPRTYI bit indicates if a parity error was detected on the TDAT system interface bus. When logic one, the TPRTYI bit indicates a parity error over the TDAT[15:0] bus. This bit is cleared when this register is read. Odd or even parity is selected using the TPTYP bit.

TPRTYE:

The TPRTYE bit enables transmit parity interrupts. When set to logic one, parity errors are indicated on INTB and TPRTYI. When set to logic zero, parity errors are indicated using bit TPRTYI, but are not indicated on output INTB.

FOVRI:

The FOVRI bit is set high when an attempt is made to write into the FIFO while it has already been filled-up. This is considered a system error. This bit is reset immediately after a read to this register.

FOVRE:

The FOVRE bit enables the generation of an interrupt due to an attempt to write the FIFO when it is already full. When FOVRE is set to logic one, the interrupt is enabled and causes FOVRI and an interrupt is asserted. When set to logic zero, FOVRI will be asserted but not INTB.

FUDRI:

The FUDRI bit is set high when the FIFO underruns while reading a packet data from the FIFO. This bit is reset immediately after a read to this register.

FUDRE:

The FUDRE bit enables the generation of an interrupt due to a FIFO underrun. When FUDRE is set to logic one, the interrupt is enabled and causes FUDRI and the output INTB to be asserted. When set to logic zero, FUDRI will be asserted, but not INTB.

FIFOERR:

The FIFOERR bit is set high when a packet is not properly delineated by a RSOP and REOP pair on the system interface. If the FIFO sees two start of packet indications (RSOP high) or two end of packet indications (REOP high), the current packet is aborted and FIFOERR is set high. This bit is reset immediately after a read to this register.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0xC1: TXFP Configuration

Bit	Type	Function	Default
Bit 7	R/W	XOFF	0
Bit 6	R/W	TPAINV	0
Bit 5	R/W	FCSERR	0
Bit 4	R/W	FCSSEL[1]	1
Bit 3	R/W	FCSSEL[0]	0
Bit 2	R/W	TPTYP	0
Bit 1	R/W	DSCR	1
Bit 0	R/W	FIFORST	0

FIFORST:

The FIFORST bit is used to reset the 256-byte transmit FIFO. When FIFORST is set to logic zero, the FIFO operates normally. When FIFORST is set to logic one, the FIFO is emptied of all octets (including the current packet being transmitted) and ignores writes. The FIFO remains empty and continues to ignore writes until a logic zero is written to FIFORST. Flags are transmitted until a subsequent packet is written to the FIFO.

DSCR:

The DSCR bit controls the scrambling of the POS frames. When DSCR is a logic one, scrambling is enabled. When DSCR is a logic zero, payload scrambling is disabled.

TPTYP:

The TPTYP bit selects even or odd parity for input TPRTY for Level 2 operation. When set to logic one, the TPRTY input must report even parity for the TDAT system interface bus. When set to logic zero, input TPRTY must report odd parity for the TDAT bus.

TPTYP must be set low when the system interface is configured for Level 3 operation.

FCSSEL[1:0]:

The Frame Control Sequence select (FCSSEL[1:0]) bits control the FCS calculation according to the table below. The FCS is calculated over the

whole packet data, before byte stuffing and scrambling.

FCSSEL[1:0]	FCS Operation
00	No FCS inserted
01	CRC-CCITT (2 bytes)
10	CRC-32 (4 bytes)
11	Reserved

FCSERR:

The FCSERR bit controls the insertion of FCS errors for diagnostic purposes. When FCSERR is set to logic one, if FCS insertion is enabled, the FCS octets are inverted prior to insertion in the POS frame. When FCSERR is set low, the FCS is inserted normally.

TPAINV:

The TPAINV bit inverts the polarity of the TPA output signal for Level 2 operation. When TPAINV is a logic one, the polarity of TPA is inverted. When TPAINV is a logic zero, TPA operates normally.

TPAINV must be set low when the system interface is configured for Level 3 operation.

XOFF:

The XOFF serves as a transmission enable bit. When XOFF is set to logic zero, POS frames are transmitted normally. When XOFF is set to logic one, the current frame being transmitted is completed and then POS frame transmission is suspended. When XOFF is asserted the FIFO still accepts data and can overflow. XOFF is provided to facilitate system debugging rather than flow control, which is better achieved using inter-packet gapping.

Register 0xC2: TXFP Control

Bit	Type	Function	Default
Bit 7	R/W	IPGAP[3]	0
Bit 6	R/W	IPGAP[2]	0
Bit 5	R/W	IPGAP[1]	1
Bit 4	R/W	IPGAP[0]	0
Bit 3	R/W	TIL[3]	0
Bit 2	R/W	TIL[2]	1
Bit 1	R/W	TIL[1]	0
Bit 0	R/W	TIL[0]	0

TIL[3:0]:

The Transmit Initiation Level (TIL[3:0]) bits are used to determine when to initiate a POS frame transmission. After the FIFO is emptied, data transmission starts only when either there is a complete packet or when the number of bytes stored in the FIFO exceeds the value of TIL[3:0] times 16.

Once initiated, the transmission will continue until the packet is transmitted or an underrun occurs. Before starting another packet, a complete packet must be in the FIFO or the FIFO fill level must exceed the level specified by TIL[3:0].

TIL[3:0] breaks the FIFO in 16 sections; for example a value of 0x4 correspond to a FIFO level of 64 bytes.

Table 8: Transmit Initiation Level Values

TIL[3:0]	FIFO Fill Level	TIL[3:0]	FIFO Fill Level
0000	0	1000	128
0001	16	1001	144
0010	32	1010	160
0011	48	1011	176
0100	64	1100	192
0101	80	1101	208
0110	96	1110	224
0111	112	1111	240

IPGAP[3:0]:

The Inter Packet Gaping (IPGAP[3:0]) bits are used to program the number of Flag Sequence characters inserted between each POS Frame. The programmed value is encoded as indicated in Table 9.

Table 9: Inter Packet Gaping Values

IPGAP[3:0]	Number of Flag	IPGAP[3:0]	Number of Flag
0000	1	1000	256
0001	2	1001	512
0010	4	1010	1024
0011	8	1011	2048
0100	16	1100	4096
0101	32	1101	8192
0110	64	1110	16384
0111	128	1111	32768

Register 0xC3: TXFP Transmit Packet Available Low Water Mark

Bit	Type	Function	Default
Bit 7	R/W	TPALWM[7]	0
Bit 6	R/W	TPALWM[6]	1
Bit 5	R/W	TPALWM[5]	0
Bit 4	R/W	TPALWM[4]	0
Bit 3	R/W	TPALWM[3]	0
Bit 2	R/W	TPALWM[2]	0
Bit 1	R/W	TPALWM[1]	0
Bit 0	R/W	TPALWM[0]	0

TPALWM[7:0]:

The Transmit FIFO Low Water Mark (TPALWM[7:0]) bits are used to generate the TPA output. TPALWM must not be programmed with a value less than 0x0F for proper operation. Due to internal pipeline delay, the TPA output may not assert until the FIFO level has dropped a maximum of 16 bytes below the value specified by TPALWM.

For Level 2 system interfaces, TPA is set to logic one when the number of bytes stored in the FIFO is lower than TPALWM[7:0].

For Level 3 system interfaces, TPA is set to logic one when the number of bytes sorted in the FIFO is lower than TPALWM[7:0] plus 2 bytes.

Register 0xC4: TXFP Transmit Packet Available High Water Mark

Bit	Type	Function	Default
Bit 7	R/W	TPAHWM[7]	1
Bit 6	R/W	TPAHWM[6]	1
Bit 5	R/W	TPAHWM[5]	1
Bit 4	R/W	TPAHWM[4]	1
Bit 3	R/W	TPAHWM[3]	0
Bit 2	R/W	TPAHWM[2]	0
Bit 1	R/W	TPAHWM[1]	0
Bit 0	R/W	TPAHWM[0]	0

TPAHWM[7:0]:

The Transmit FIFO High Water Mark (TPAHWM[7:0]) bits are used to generate the TPA output. TPAHWM must not be programmed with a value greater than 0xF0 for proper operation. Due to internal pipeline delay, the TPA output may not deassert until the FIFO level has raised a maximum of 8 bytes above the value specified by TPAHWM.

For Level 2 system interfaces, TPA is set to logic zero when the number of bytes stored in the FIFO exceeds TPAHWM[7:0].

For Level 3 system interfaces, TPA is set to logic zero when the number of bytes stored in the FIFO exceeds TPAHWM[7:0] less four bytes.

Register 0xC5: TXFP Transmit Byte Count LSB

Bit	Type	Function	Default
Bit 7	R	TBYTE[7]	X
Bit 6	R	TBYTE[6]	X
Bit 5	R	TBYTE[5]	X
Bit 4	R	TBYTE[4]	X
Bit 3	R	TBYTE[3]	X
Bit 2	R	TBYTE[2]	X
Bit 1	R	TBYTE[1]	X
Bit 0	R	TBYTE[0]	X

Register 0xC6: TXFP Transmit Byte Count

Bit	Type	Function	Default
Bit 7	R	TBYTE[15]	X
Bit 6	R	TBYTE[14]	X
Bit 5	R	TBYTE[13]	X
Bit 4	R	TBYTE[12]	X
Bit 3	R	TBYTE[11]	X
Bit 2	R	TBYTE[10]	X
Bit 1	R	TBYTE[9]	X
Bit 0	R	TBYTE[8]	X

Register 0xC7: TXFP Transmit Byte Count

Bit	Type	Function	Default
Bit 7	R	TBYTE[23]	X
Bit 6	R	TBYTE[22]	X
Bit 5	R	TBYTE[21]	X
Bit 4	R	TBYTE[20]	X
Bit 3	R	TBYTE[19]	X
Bit 2	R	TBYTE[18]	X
Bit 1	R	TBYTE[17]	X
Bit 0	R	TBYTE[16]	X

Register 0xC8: TXFP Transmit Byte Count MSB

Bit	Type	Function	Default
Bit 7	R	TBYTE[31]	X
Bit 6	R	TBYTE[30]	X
Bit 5	R	TBYTE[29]	X
Bit 4	R	TBYTE[28]	X
Bit 3	R	TBYTE[27]	X
Bit 2	R	TBYTE[26]	X
Bit 1	R	TBYTE[25]	X
Bit 0	R	TBYTE[24]	X

TBYTE[31:0]:

The TBYTE[31:0] bits indicate the number of bytes read from the transmit FIFO and transmitted during the last accumulation interval. This counter does not count bytes within aborted frames.

A write to any one of the TXFP Transmit Byte Counter registers or the S/UNI-622-POS Master Reset and Identity register loads the registers with the current counter value and resets the internal 32 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Byte Counter registers. The counter should be polled every second to avoid saturating. The contents of these

registers are valid three TCLK cycles after a transfer is triggered by a write to any of the TXFP Transmit Byte Count Registers.

Register 0xC9: TXFP Transmit Frame Count LSB

Bit	Type	Function	Default
Bit 7	R	TFRAME[7]	X
Bit 6	R	TFRAME[6]	X
Bit 5	R	TFRAME[5]	X
Bit 4	R	TFRAME[4]	X
Bit 3	R	TFRAME[3]	X
Bit 2	R	TFRAME[2]	X
Bit 1	R	TFRAME[1]	X
Bit 0	R	TFRAME[0]	X

Register 0xCA: TXFP Transmit Frame Count

Bit	Type	Function	Default
Bit 7	R	TFRAME[15]	X
Bit 6	R	TFRAME[14]	X
Bit 5	R	TFRAME[13]	X
Bit 4	R	TFRAME[12]	X
Bit 3	R	TFRAME[11]	X
Bit 2	R	TFRAME[10]	X
Bit 1	R	TFRAME[9]	X
Bit 0	R	TFRAME[8]	X

Register 0xCB: TXFP Transmit Frame Count MSB

Bit	Type	Function	Default
Bit 7	R	TFRAME[23]	X
Bit 6	R	TFRAME[22]	X
Bit 5	R	TFRAME[21]	X
Bit 4	R	TFRAME[20]	X
Bit 3	R	TFRAME[19]	X
Bit 2	R	TFRAME[18]	X
Bit 1	R	TFRAME[17]	X
Bit 0	R	TFRAME[16]	X

TFRAME[23:0]:

The TFRAME[23:0] bits indicate the number of POS frames read from the transmit FIFO and inserted into the transmission stream during the last accumulation interval. This counter does not count aborted frames.

A write to any one of the TXFP Transmit Frame Counter registers or the S/UNI-622-POS Master Reset and Identity register loads the registers with the current counter value and resets the internal 24 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to the Transmit Frame Counter registers. The counter should be polled every second to avoid saturating. The contents of these registers are valid three TCLK cycles after a transfer is triggered by a write to any of the TXFP Transmit Frame Count Registers.

Register 0xCC: TXFP Transmit User Aborted Frame Count LSB

Bit	Type	Function	Default
Bit 7	R	TUSRABF[7]	X
Bit 6	R	TUSRABF[6]	X
Bit 5	R	TUSRABF[5]	X
Bit 4	R	TUSRABF[4]	X
Bit 3	R	TUSRABF[3]	X
Bit 2	R	TUSRABF[2]	X
Bit 1	R	TUSRABF[1]	X
Bit 0	R	TUSRABF[0]	X

Register 0xCD: TXFP Transmit User Aborted Frame Count MSB

Bit	Type	Function	Default
Bit 7	R	TUSRABF[15]	X
Bit 6	R	TUSRABF[14]	X
Bit 5	R	TUSRABF[13]	X
Bit 4	R	TUSRABF[12]	X
Bit 3	R	TUSRABF[11]	X
Bit 2	R	TUSRABF[10]	X
Bit 1	R	TUSRABF[9]	X
Bit 0	R	TUSRABF[8]	X

TUSRABF[15:0]:

The TUSRABF[15:0] bits indicate the number of user aborted POS frames read from the transmit FIFO and inserted into the transmission stream during the last accumulation interval. User can abort frames by asserting TERR.

A write to any one of the TXFP Transmit User Aborted Frame Counter registers or the S/UNI-622-POS Master Reset and Identity register loads the registers with the current counter value and resets the internal 16 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to these registers. The counter should be

polled every second to avoid saturating. The contents of these registers are valid three TCLK cycles after a transfer is triggered.

Register 0xCE: TXFP Transmit Underrun/Error Aborted Frame Count LSB

Bit	Type	Function	Default
Bit 7	R	TFERABF[7]	X
Bit 6	R	TFERABF[6]	X
Bit 5	R	TFERABF[5]	X
Bit 4	R	TFERABF[4]	X
Bit 3	R	TFERABF[3]	X
Bit 2	R	TFERABF[2]	X
Bit 1	R	TFERABF[1]	X
Bit 0	R	TFERABF[0]	X

Register 0xCF: TXFP Transmit Underrun/Error Aborted Frame Count MSB

Bit	Type	Function	Default
Bit 7	R	TFERABF[15]	X
Bit 6	R	TFERABF[14]	X
Bit 5	R	TFERABF[13]	X
Bit 4	R	TFERABF[12]	X
Bit 3	R	TFERABF[11]	X
Bit 2	R	TFERABF[10]	X
Bit 1	R	TFERABF[9]	X
Bit 0	R	TFERABF[8]	X

TRERABF[15:0]:

The TFERABF[15:0] bits indicate the number of FIFO underrun error aborted POS frames read from the transmit FIFO and inserted into the transmission stream during the last accumulation interval. FIFO underruns errors are caused when the FIFO runs empty and the last byte read was not an end of packet or also when the FIFO overruns and corrupts the end of packet/start of packet sequence (example: when another RSOP is high when expecting an REOP). This is considered a system error and should not occur when the system works normally.

A write to any one of the TXFP Transmit User Aborted Frame Counter registers or the S/UNI-622-POS Master Reset and Identity register loads the registers with the current counter value and resets the internal 16 bit counter to 1 or 0. The counter reset value is dependent on if there was a count event during the transfer of the count to these registers. The counter should be polled every second to avoid saturating. The contents of these registers are valid three TCLK cycles after a transfer is triggered.

Register 0xD0: WANS Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	FORCEREAC	0
Bit 2	R/W	AUTOREAC	0
Bit 1	R/W	INTEN	0
Bit 0	R/W	PHACOMPEN	0

PHACOMPEN:

The Phase Comparison Enable (PHACOMPEN) bit is used to enable the phase comparison process. Setting this bit to a logic one will enable the phase comparison process. When set low, the phase and reference period counters are kept in reset state, further disabling the WANS process

INTEN:

The Interrupt Enable (INTEN) bit controls the generation of the interrupt signal. When set high, this bit allows the generation of an interrupt signal at the beginning of the Phase Detector averaging period. Setting this bit to logic zero disables the generation of the interrupts.

AUTOREAC:

The Auto Reacquisition Mode Select (AUTOREAC) bit can be used to set the WANS to automatic phase reacquisition mode. When operating in this mode, the WANS will automatically align the phase sampling point toward the middle of the Phase Counter period upon detection of two consecutive Phase Sample located on each side of the Phase Counter wrap around value. The Phase Word register will keep its previous value till. Setting this bit to logic one enables the automatic reacquisition mode.

FORCEREAC:

The Force Phase Reacquisition (FORCEREAC) bit can be used to force a phase reacquisition of the Phase Detector. A logic zero to logic one transition

on this bit triggers a phase reacquisition sequence of the Phase Detector. Setting this bit to logic zero allows the Phase detector to operate normally.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0xD1: WANS Interrupt and Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	RPHALGN	X
Bit 0	R	TIMI	X

TIMI:

The Timer Interrupt (TIMI) bit indicates a Timer Interrupt condition. This bit will be raised at the beginning of the Phase Detector averaging period. In addition to indicating the interrupt status, this bit can also be polled to synchronize read access to the WANS output register. This interrupt can be masked using the INTEN bit of the configuration register. A read access to the Interrupt & Status Register resets the value of this bit.

RPHALGN:

The Reference Phase Alignment (RPHALNG) bit indicates a Reference Phase Alignment event. In normal operating mode, this bit remains set to logic zero. Upon the occurrence of a Reference Phase Alignment, this bit is set to logic one, indicating that the phase averaging process was aborted and that the value of the Phase Word register is frozen to the previous valid value. This bit is reset low after the completion of a valid phase averaging cycle.

Register 0xD2: WANS Phase Word LSB

Bit	Type	Function	Default
Bit 7	R	PHAWORD[7]	X
Bit 6	R	PHAWORD[6]	X
Bit 5	R	PHAWORD[5]	X
Bit 4	R	PHAWORD[4]	X
Bit 3	R	PHAWORD[3]	X
Bit 2	R	PHAWORD[2]	X
Bit 1	R	PHAWORD[1]	X
Bit 0	R	PHAWORD[0]	X

Register 0xD3: WANS Phase Word

Bit	Type	Function	Default
Bit 7	R	PHAWORD[15]	X
Bit 6	R	PHAWORD[14]	X
Bit 5	R	PHAWORD[13]	X
Bit 4	R	PHAWORD[12]	X
Bit 3	R	PHAWORD[11]	X
Bit 2	R	PHAWORD[10]	X
Bit 1	R	PHAWORD[9]	X
Bit 0	R	PHAWORD[8]	X

Register 0xD4: WANS Phase Word

Bit	Type	Function	Default
Bit 7	R	PHAWORD[23]	X
Bit 6	R	PHAWORD[22]	X
Bit 5	R	PHAWORD[21]	X
Bit 4	R	PHAWORD[20]	X
Bit 3	R	PHAWORD[19]	X
Bit 2	R	PHAWORD[18]	X
Bit 1	R	PHAWORD[17]	X
Bit 0	R	PHAWORD[16]	X

Register 0xD5: WANS Phase Word MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PHAWORD[30]	X
Bit 5	R	PHAWORD[29]	X
Bit 4	R	PHAWORD[28]	X
Bit 3	R	PHAWORD[27]	X
Bit 2	R	PHAWORD[26]	X
Bit 1	R	PHAWORD[25]	X
Bit 0	R	PHAWORD[24]	X

PHAWORD[30:0]:

The Phase Word (PHAWORD[30:0]) bits are the output bus of the Phase Detector. This bus outputs the result of the Phase Count Averaging function. Depending on the number of samples included in the averaging, from 0 to 15 of the LSB(s) of the PHAWORD bus may represent the fractional part of the average value while the 16 following bits hold the integer part. This value can be used to externally implement in software the PLL filtering function and bypass the Digital Loop Filter block.

Register 0xD9: WANS Reference Period LSB

Bit	Type	Function	Default
Bit 7	R/W	REFPER[7]	0
Bit 6	R/W	REFPER[6]	0
Bit 5	R/W	REFPER[5]	0
Bit 4	R/W	REFPER[4]	0
Bit 3	R/W	REFPER[3]	0
Bit 2	R/W	REFPER[2]	0
Bit 1	R/W	REFPER[1]	0
Bit 0	R/W	REFPER[0]	0

Register 0xDA: WANS Reference Period MSB

Bit	Type	Function	Default
Bit 7	R/W	REFPER[15]	0
Bit 6	R/W	REFPER[14]	0
Bit 5	R/W	REFPER[13]	0
Bit 4	R/W	REFPER[12]	0
Bit 3	R/W	REFPER[11]	0
Bit 2	R/W	REFPER[10]	0
Bit 1	R/W	REFPER[9]	0
Bit 0	R/W	REFPER[8]	0

REFPER[15:0]:

The Reference Period REFPER[15:0] bits are used to program the timing reference period of the Phase Detector. These bits are used to set the end of count of the Reference Period Counter. The Reference Period Counter is reset on the next clock cycle following the detection of its end of count. The Reference Period Counter counts (Nref) is equal to the REFPER value plus 1.

Register 0xDB: WANS Phase Counter Period LSB

Bit	Type	Function	Default
Bit 7	R/W	PHCNTPER[7]	0
Bit 6	R/W	PHCNTPER[6]	0
Bit 5	R/W	PHCNTPER[5]	0
Bit 4	R/W	PHCNTPER[4]	0
Bit 3	R/W	PHCNTPER[3]	0
Bit 2	R/W	PHCNTPER[2]	0
Bit 1	R/W	PHCNTPER[1]	0
Bit 0	R/W	PHCNTPER[0]	0

Register 0xDC: WANS Phase Counter Period MSB

Bit	Type	Function	Default
Bit 7	R/W	PHCNTPER[15]	0
Bit 6	R/W	PHCNTPER[14]	0
Bit 5	R/W	PHCNTPER[13]	0
Bit 4	R/W	PHCNTPER[12]	0
Bit 3	R/W	PHCNTPER[11]	0
Bit 2	R/W	PHCNTPER[10]	0
Bit 1	R/W	PHCNTPER[9]	0
Bit 0	R/W	PHCNTPER[8]	0

PHCNTPER[15:0]:

The Phase Counter Period (PHCNTPER15:0]) bits are used to program the Phase Counter period of the Phase Detector. These bits are used to set the end of count of the Phase Counter. The Phase Counter is reset on the next clock cycle following the detection of its end of count. The Phase Counter count (Nphcnt) is equal to the PHCNTPER value plus 1.

For the system to operate properly, Nphcnt need to be greater than 1023.

Register 0xDD: WANS Phase Average Period

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	PHAVGPER[3]	0
Bit 2	R/W	PHAVGPER[2]	0
Bit 1	R/W	PHAVGPER[1]	0
Bit 0	R/W	PHAVGPER[0]	0

PHAVGPER[3:0]:

The Phase Average Period (FRACQPER[3:0]) bits are used to set the number of consecutive valid Phase Samples accumulated to form the Phase Word. The number of samples is expressed as a power of 2, i.e.:

$$Nfracq = 2^{FRACQPER}$$

Register 0xE0: RASE Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	PSBFE	0
Bit 6	R/W	COAPSE	0
Bit 5	R/W	Z1/S1E	0
Bit 4	R/W	SFBERE	0
Bit 3	R/W	SDBERE	0
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

SDBERE:

The SDBERE bit is the interrupt enable for the signal degrade threshold alarm. When SDBERE is a logic one, an interrupt is generated when the SD alarm is declared or removed.

SFBERE:

The SFBERE bit is the interrupt enable for the signal fail threshold alarm. When SFBERE is a logic one, an interrupt is generated when the SF alarm is declared or removed.

Z1/S1E:

The Z1/S1 interrupt enable is an interrupt mask for changes in the received synchronization status. When Z1/S1E is a logic one, an interrupt is generated when a new synchronization status message is extracted into the Receive Z1/S1 register.

COAPSE:

The COAPS interrupt enable is an interrupt mask for changes in the received APS code. When COAPSE is a logic one, an interrupt is generated when a new K1/K2 code value is extracted into the RASE Receive K1 and RASE Receive K2 registers.

PSBFE:

The PSBF interrupt enable is an interrupt mask for protection switch byte failure alarms. When PSBFE is a logic one, an interrupt is generated when PSBF is declared or removed.

Register 0xE1: RASE Interrupt Status

Bit	Type	Function	Default
Bit 7	R	PSBFI	X
Bit 6	R	COAPSI	X
Bit 5	R	Z1/S1I	X
Bit 4	R	SFBERI	X
Bit 3	R	SDBERI	X
Bit 2	R	SFBERV	X
Bit 1	R	SDBERV	X
Bit 0	R	PSBFV	X

PSBFV:

The PSBFV bit indicates the protection switching byte failure alarm state. The alarm is declared (PSBFV is set high) when twelve successive frames have been received without three consecutive frames containing identical K1 bytes. The alarm is removed (PSBFV is set low) when three consecutive frames containing identical K1 bytes have been received.

SDBERV:

The SDBERV bit indicates the signal degrade threshold crossing alarm state. The alarm is declared (SDBERV is set high) when the bit error rate exceeds the threshold programmed in the RASE SD Declaring Threshold registers. The alarm is removed (SDBERV is set low) when the bit error rate is below the threshold programmed in the RASE SD Clearing Threshold registers.

SFBERV:

The SFBERV bit indicates the signal failure threshold crossing alarm state. The alarm is declared (SFBERV is set high) when the bit error rate exceeds the threshold programmed in the RASE SF Declaring Threshold registers. The alarm is removed (SFBERV is set low) when the bit error rate is below the threshold programmed in the RASE SF Clearing Threshold registers.

SDBERI:

The SDBERI bit is set high when the signal degrade threshold crossing alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

SFBERI:

The SFBERI bit is set high when the signal failure threshold crossing alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

Z1/S1I:

The Z1/S1I bit is set high when a new synchronization status message has been extracted into the RASE Receive Z1/S1 register. This bit is cleared when the RASE Interrupt Status register is read.

COAPSI:

The COAPSI bit is set high when a new APS code value has been extracted into the RASE Receive K1 and RASE Receive K2 registers. This bit is cleared when the RASE Interrupt Status register is read.

PSBFI:

The PSBFI bit is set high when the protection switching byte failure alarm is declared or removed. This bit is cleared when the RASE Interrupt Status register is read.

Register 0xE2: RASE Configuration/Control

Bit	Type	Function	Default
Bit 7	R/W	Z1/S1_CAP	0
Bit 6	R/W	SFBERTEN	0
Bit 5	R/W	SFSMODE	0
Bit 4	R/W	SFCMODE	0
Bit 3	R/W	SDBERTEN	0
Bit 2	R/W	SDSMODE	0
Bit 1	R/W	SDCMODE	0
Bit 0	R/W	Reserved	0

SDCMODE:

The SDCMODE alarm bit selects the RASE window size to use for clearing the SD alarm. When SDCMODE is a logic zero, the RASE clears the SD alarm using the same window size used for declaration. When SDCMODE is a logic one, the RASE clears the SD alarm using a window size that is 8 times longer than the alarm declaration window size. The declaration window size is determined by the RASE SD Accumulation Period registers.

SDSMODE:

The SDSMODE bit selects the RASE saturation mode. When SDSMODE is a logic zero, the RASE limits the number of B2 errors accumulated in one frame period to the RASE SD Saturation Threshold register value. When SDSMODE is a logic one, the RASE limits the number of B2 errors accumulated in one window subtotal accumulation period to the RASE SD Saturation Threshold register value. Note that the number of frames in a window subtotal accumulation period is determined by the RASE SD Accumulation Period register value.

SDBERTEN:

The SDBERTEN bit selects automatic monitoring of line bit error rate threshold events by the RASE. When SDBERTEN is a logic one, the RASE continuously monitors line BIP errors over a period defined in the RASE configuration registers. When SDBERTEN is a logic zero, the RASE BIP accumulation logic is disabled, and the RASE logic is reset to the declaration monitoring state.

All RASE accumulation period and threshold registers should be set up before SDBERTEN is written.

SFCMODE:

The SFCMODE alarm bit selects the RASE window size to use for clearing the SF alarm. When SFCMODE is a logic zero, the RASE clears the SF alarm using the same window size used for declaration. When SFCMODE is a logic one, the RASE clears the SF alarm using a window size that is 8 times longer than the alarm declaration window size. The declaration window size is determined by the RASE SF Accumulation Period registers.

SFSMODE:

The SFSMODE bit selects the RASE saturation mode. When SFSMODE is a logic zero, the RASE limits the number of B2 errors accumulated in one frame period to the RASE SF Saturation Threshold register value. When SFSMODE is a logic one, the RASE limits the number of B2 errors accumulated in one window subtotal accumulation period to the RASE SF Saturation Threshold register value. Note that the number of frames in a window subtotal accumulation period is determined by the RASE SF Accumulation Period register value.

SFBERTEN:

The SFBERTEN bit enables automatic monitoring of line bit error rate threshold events by the RASE. When SFBERTEN is a logic one, the RASE continuously monitors line BIP errors over a period defined in the RASE configuration registers. When SFBERTEN is a logic zero, the RASE BIP accumulation logic is disabled, and the RASE logic is reset to the declaration monitoring state.

All RASE accumulation period and threshold registers should be set up before SFBERTEN is written.

Z1/S1_CAP:

The Z1/S1_CAP bit enables the Z1/S1 Capture algorithm. When Z1/S1_CAP is a logic one, the Z1/S1 clock synchronization status message nibble must have the same value for eight consecutive frames before writing the new value into the RASE Receive Z1/S1 register. When Z1/S1_CAP is logic zero, the Z1/S1 nibble value is written directly into the RASE Receive Z1/S1 register.

Reserved:

The reserved bits must be programmed to logic zero for proper operation.

Register 0xE3: RASE SF Accumulation Period LSB

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[7]	0
Bit 6	R/W	SFSAP[6]	0
Bit 5	R/W	SFSAP[5]	0
Bit 4	R/W	SFSAP[4]	0
Bit 3	R/W	SFSAP[3]	0
Bit 2	R/W	SFSAP[2]	0
Bit 1	R/W	SFSAP[1]	0
Bit 0	R/W	SFSAP[0]	0

Register 0xE4: RASE SF Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[15]	0
Bit 6	R/W	SFSAP[14]	0
Bit 5	R/W	SFSAP[13]	0
Bit 4	R/W	SFSAP[12]	0
Bit 3	R/W	SFSAP[11]	0
Bit 2	R/W	SFSAP[10]	0
Bit 1	R/W	SFSAP[9]	0
Bit 0	R/W	SFSAP[8]	0

Register 0xE5: RASE SF Accumulation Period MSB

Bit	Type	Function	Default
Bit 7	R/W	SFSAP[23]	0
Bit 6	R/W	SFSAP[22]	0
Bit 5	R/W	SFSAP[21]	0
Bit 4	R/W	SFSAP[20]	0
Bit 3	R/W	SFSAP[19]	0
Bit 2	R/W	SFSAP[18]	0
Bit 1	R/W	SFSAP[17]	0
Bit 0	R/W	SFSAP[16]	0

SFSAP[23:0]:

The SFSAP[23:0] bits represent the number of 8 KHz frames used to accumulate the B2 error subtotal. The total evaluation window to declare the SF alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operation section for recommended settings.

Register 0xE6: RASE SF Saturation Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	SFSTH[7]	0
Bit 6	R/W	SFSTH[6]	0
Bit 5	R/W	SFSTH[5]	0
Bit 4	R/W	SFSTH[4]	0
Bit 3	R/W	SFSTH[3]	0
Bit 2	R/W	SFSTH[2]	0
Bit 1	R/W	SFSTH[1]	0
Bit 0	R/W	SFSTH[0]	0

Register 0xE7: RASE SF Saturation Threshold MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFSTH[11]	0
Bit 2	R/W	SFSTH[10]	0
Bit 1	R/W	SFSTH[9]	0
Bit 0	R/W	SFSTH[8]	0

SFSTH[11:0]:

The SFSTH[11:0] value represents the allowable number of B2 errors that can be accumulated during an evaluation window before an SF threshold event is declared. Setting this threshold to 0xFFF disables the saturation functionality. Refer to the Operation section for the recommended settings.

Register 0xE8: RASE SF Declaring Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	SFDTH[7]	0
Bit 6	R/W	SFDTH[6]	0
Bit 5	R/W	SFDTH[5]	0
Bit 4	R/W	SFDTH[4]	0
Bit 3	R/W	SFDTH[3]	0
Bit 2	R/W	SFDTH[2]	0
Bit 1	R/W	SFDTH[1]	0
Bit 0	R/W	SFDTH[0]	0

Register 0xE9: RASE SF Declaring Threshold MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFDTH[11]	0
Bit 2	R/W	SFDTH[10]	0
Bit 1	R/W	SFDTH[9]	0
Bit 0	R/W	SFDTH[8]	0

SFDTH[11:0]:

The SFDTH[11:0] value determines the threshold for the declaration of the SF alarm. The SF alarm is declared when the number of B2 errors accumulated during an evaluation window is greater than or equal to the SFDTH[11:0] value. Refer to the Operation section for the recommended settings.

Register 0xEA: RASE SF Clearing Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	SFCTH[7]	0
Bit 6	R/W	SFCTH[6]	0
Bit 5	R/W	SFCTH[5]	0
Bit 4	R/W	SFCTH[4]	0
Bit 3	R/W	SFCTH[3]	0
Bit 2	R/W	SFCTH[2]	0
Bit 1	R/W	SFCTH[1]	0
Bit 0	R/W	SFCTH[0]	0

Register 0xEB: RASE SF Clearing Threshold MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SFCTH[11]	0
Bit 2	R/W	SFCTH[10]	0
Bit 1	R/W	SFCTH[9]	0
Bit 0	R/W	SFCTH[8]	0

SFCTH[11:0]:

The SFCTH[11:0] value determines the threshold for the removal of the SF alarm. The SF alarm is removed when the number of B2 errors accumulated during an evaluation window is less than the SFCTH[11:0] value. Refer to the Operation section for the recommended settings.

Register 0xEC: RASE SD Accumulation Period LSB

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[7]	0
Bit 6	R/W	SDSAP[6]	0
Bit 5	R/W	SDSAP[5]	0
Bit 4	R/W	SDSAP[4]	0
Bit 3	R/W	SDSAP[3]	0
Bit 2	R/W	SDSAP[2]	0
Bit 1	R/W	SDSAP[1]	0
Bit 0	R/W	SDSAP[0]	0

Register 0xED: RASE SD Accumulation Period

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[15]	0
Bit 6	R/W	SDSAP[14]	0
Bit 5	R/W	SDSAP[13]	0
Bit 4	R/W	SDSAP[12]	0
Bit 3	R/W	SDSAP[11]	0
Bit 2	R/W	SDSAP[10]	0
Bit 1	R/W	SDSAP[9]	0
Bit 0	R/W	SDSAP[8]	0

Register 0xEE: RASE SD Accumulation Period MSB

Bit	Type	Function	Default
Bit 7	R/W	SDSAP[23]	0
Bit 6	R/W	SDSAP[22]	0
Bit 5	R/W	SDSAP[21]	0
Bit 4	R/W	SDSAP[20]	0
Bit 3	R/W	SDSAP[19]	0
Bit 2	R/W	SDSAP[18]	0
Bit 1	R/W	SDSAP[17]	0
Bit 0	R/W	SDSAP[16]	0

SDSAP[23:0]:

The SDSAP[23:0] bits represent the number of 8 KHz frames used to accumulate the B2 error subtotal. The total evaluation window to declare the SD alarm is broken into 8 subtotals, so this register value represents 1/8 of the total sliding window size. Refer to the Operation section for recommended settings.

Register 0xEF: RASE SD Saturation Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	SDSTH[7]	0
Bit 6	R/W	SDSTH[6]	0
Bit 5	R/W	SDSTH[5]	0
Bit 4	R/W	SDSTH[4]	0
Bit 3	R/W	SDSTH[3]	0
Bit 2	R/W	SDSTH[2]	0
Bit 1	R/W	SDSTH[1]	0
Bit 0	R/W	SDSTH[0]	0

Register 0xF0: RASE SD Saturation Threshold MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDSTH[11]	0
Bit 2	R/W	SDSTH[10]	0
Bit 1	R/W	SDSTH[9]	0
Bit 0	R/W	SDSTH[8]	0

SDSTH[11:0]:

The SDSTH[11:0] value represents the allowable number of B2 errors that can be accumulated during an evaluation window before an SD threshold event is declared. Setting this threshold to 0xFFF disables the saturation functionality. Refer to the Operation section for the recommended settings.

Register 0xF1: RASE SD Declaring Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	SDDTH[7]	0
Bit 6	R/W	SDDTH[6]	0
Bit 5	R/W	SDDTH[5]	0
Bit 4	R/W	SDDTH[4]	0
Bit 3	R/W	SDDTH[3]	0
Bit 2	R/W	SDDTH[2]	0
Bit 1	R/W	SDDTH[1]	0
Bit 0	R/W	SDDTH[0]	0

Register 0xF2: RASE SD Declaring Threshold MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDDTH[11]	0
Bit 2	R/W	SDDTH[10]	0
Bit 1	R/W	SDDTH[9]	0
Bit 0	R/W	SDDTH[8]	0

SDDTH[11:0]:

The SDDTH[11:0] value determines the threshold for the declaration of the SD alarm. The SD alarm is declared when the number of B2 errors accumulated during an evaluation window is greater than or equal to the SDDTH[11:0] value. Refer to the Operation section for the recommended settings.

Register 0xF3: RASE SD Clearing Threshold LSB

Bit	Type	Function	Default
Bit 7	R/W	SDCTH[7]	0
Bit 6	R/W	SDCTH[6]	0
Bit 5	R/W	SDCTH[5]	0
Bit 4	R/W	SDCTH[4]	0
Bit 3	R/W	SDCTH[3]	0
Bit 2	R/W	SDCTH[2]	0
Bit 1	R/W	SDCTH[1]	0
Bit 0	R/W	SDCTH[0]	0

Register 0xF4: RASE SD Clearing Threshold MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	SDCTH[11]	0
Bit 2	R/W	SDCTH[10]	0
Bit 1	R/W	SDCTH[9]	0
Bit 0	R/W	SDCTH[8]	0

SDCTH[11:0]:

The SDCTH[11:0] value determines the threshold for the removal of the SD alarm. The SD alarm is removed when the number of B2 errors accumulated during an evaluation window is less than the SDCTH[11:0] value. Refer to the Operation section for the recommended settings.

Register 0xF5: RASE Receive K1

Bit	Type	Function	Default
Bit 7	R	K1[7]	X
Bit 6	R	K1[6]	X
Bit 5	R	K1[5]	X
Bit 4	R	K1[4]	X
Bit 3	R	K1[3]	X
Bit 2	R	K1[2]	X
Bit 1	R	K1[1]	X
Bit 0	R	K1[0]	X

K1[7:0]:

The K1[7:0] bits contain the current K1 code value. The contents of this register are updated when a new K1 code value (different from the current K1 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K1[7] is the most significant bit corresponding to bit 1, the first bit received. K1[0] is the least significant bit, corresponding to bit 8, the last bit received.

Register 0xF6: RASE Receive K2

Bit	Type	Function	Default
Bit 7	R	K2[7]	X
Bit 6	R	K2[6]	X
Bit 5	R	K2[5]	X
Bit 4	R	K2[4]	X
Bit 3	R	K2[3]	X
Bit 2	R	K2[2]	X
Bit 1	R	K2[1]	X
Bit 0	R	K2[0]	X

K2[7:0]:

The K2[7:0] bits contain the current K2 code value. The contents of this register are updated when a new K2 code value (different from the current K2 code value) has been received for three consecutive frames. An interrupt may be generated when a new code value is received (using the COAPSE bit in the RASE Interrupt Enable Register). K2[7] is the most significant bit corresponding to bit 1, the first bit received. K2[0] is the least significant bit, corresponding to bit 8, the last bit received.

Register 0xF7: RASE Receive Z1/S1

Bit	Type	Function	Default
Bit 7	R	Z1/S1[7]	X
Bit 6	R	Z1/S1[6]	X
Bit 5	R	Z1/S1[5]	X
Bit 4	R	Z1/S1[4]	X
Bit 3	R	Z1/S1[3]	X
Bit 2	R	Z1/S1[2]	X
Bit 1	R	Z1/S1[1]	X
Bit 0	R	Z1/S1[0]	X

Z1/S1[3:0]:

The lower nibble of the first Z1/S1 byte contained in the receive stream is extracted into this register. The Z1/S1 byte is used to carry synchronization status messages between line terminating network elements. Z1/S1[3] is the most significant bit corresponding to bit 5, the first bit received. Z1/S1[0] is the least significant bit, corresponding to bit 8, the last bit received. An interrupt may be generated when a byte value is received that differs from the value extracted in the previous frame (using the Z1/S1E bit in the RASE Interrupt Enable Register). In addition, debouncing can be performed where the register is not loaded until eight of the same consecutive nibbles are received. Debouncing is controlled using the Z1/S1_CAP bit in the RASE Configuration/Control register.

Z1/S1[7:4]:

The upper nibble of the first Z1/S1 byte contained in the receive stream is extracted into this register. No interrupt is asserted on the change of this nibble. In addition, when the Z1/S1_CAP bit in the RASE Configuration/Control register selects debouncing, the upper nibble is only updated when eight of the same consecutive lower nibbles are received.

Register 0xFC: S/UNI-622-POS Concatenation Status and Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	AISCV	X
Bit 4	R	LOPCV	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	AISCE	0
Bit 0	R/W	LOPCE	0

LOPCE:

The LOPCE bit is the interrupt enable for the Loss of Pointer Concatenation event. When LOPCE is a logic one, an interrupt is generated when the state of the Loss of Pointer Concatenation indicator changes.

AISCE:

The AISCE bit is the interrupt enable for the Pointer AIS event. When AISCE is a logic one, an interrupt is generated when the state of the Pointer AIS indicator changes.

LOPCV:

The LOPCV bit is the Loss of Pointer Concatenation indicator. When LOPCV is logic one, the STS-12c/STM-4-4c pointers do not indicate a concatenated payload. When LOPCV and AISCV are both logic zero, a STS-12c/STM-4-4c payload is indicated.

AISCV:

The ASICV bit is the Pointer AIS indicator. When AISCV is logic one, the STS-12c/STM-4-4c pointer indicates a pointer AIS condition. When LOPC and AISCV are both logic zero, a STS-12c/STM-4-4c payload is indicated.

Register 0xFD: S/UNI-622-POS Concatenation Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	AISCI	X
Bit 0	R	LOPCI	X

LOPCI:

A logic one on the LOPCI bit indicates that a transition has occurred on the Loss of Pointer Concatenation indicator. This bit is cleared when this register is read.

AISCI:

A logic one on the AISCI bit indicates that a transition has occurred on the Pointer AIS indicator. This bit is cleared when this register is read.

12 TEST FEATURES DESCRIPTION

Simultaneously asserting (low) the CSB, RDB and WRB inputs causes all digital output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the S/UNI-622-POS. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[8]) is high.

In addition, the S/UNI-622-POS also supports a standard IEEE 1149.1 five-signal JTAG boundary scan test port for use in board testing. All digital device inputs may be read and all digital device outputs may be forced via the JTAG test port.

Table 10: Test Mode Register Memory Map

Address	Register
0x000-0x0FF	Normal Mode Registers
0x100	Master Test Register
0x101-0x1FF	Reserved For Production Test

12.1 Master Test and Test Configuration Registers

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic zero. Reading back unused bits can produce either a logic one or a logic zero; hence, unused register bits should be masked off by software when read.

2. Writable test mode register bits are not initialized upon reset unless otherwise noted.

Register 0x100: Master Test Register

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	W	Reserved	X
Bit 5	W	PMCATST	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	X
Bit 2		Reserved	0
Bit 1	W	HIZDATA	X
Bit 0	R/W	HIZIO	0

This register is used to enable S/UNI-622-POS test features. All bits, except PMCTST, PMCATST and BYPASS are reset to zero by a reset of the S/UNI-622-POS using either the RSTB input or the Master Reset register. PMCTST and BYPASS are reset when CSB is high. PMCTST, PMCATST and BYPASS can also be reset by writing a logic zero to the corresponding register bit.

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the S/UNI-622-POS . While the HIZIO bit is a logic one, all output pins of the S/UNI-622-POS except the data bus and output TDO are held tri-state. The microprocessor interface is still active. While the HIZDATA bit is a logic one, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles. The HIZDATA bit is overridden by the DBCTRL bit.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic one and PMCTST is set to logic one, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the S/UNI-622-POS to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

PMCTST:

The PMCTST bit is used to configure the S/UNI-622-POS for PMC's manufacturing tests. When PMCTST is set to logic one, the S/UNI-622-POS microprocessor port becomes the test access port used to run the PMC "canned" manufacturing test vectors. The PMCTST bit can be cleared by setting CSB to logic one and RSTB to logic zero or by writing logic zero to the bit.

PMCATST:

The PMCATST bit is used to configure the analog portion of the S/UNI-622-POS for PMC's manufacturing tests. The PMCTST bit can be cleared by setting CSB to logic one and RSTB to logic zero or by writing logic zero to the bit.

Reserved:

The reserved bit must be programmed to logic one for proper operation

12.2 JTAG Test Port

The JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operation section.

Table 11: Instruction Register (Length - 3 bits)

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 12: S/UNI-622-POS Identification Register

Length	32 bits
Version Number	2H
Part Number	5357H
Manufacturer's Identification Code	0CDH
Device Identification	053570CDH

Table 13: S/UNI-622-POS Boundary Scan Register

Pin/Enable	Register Bit	Cell Type	Device I.D.
RSTB	134	IN_CELL	0
ALE	133	IN_CELL	0
CSB	132	IN_CELL	0
RDB	131	IN_CELL	0
WRB	130	IN_CELL	0
A[8]	129	IN_CELL	1
A[7]	128	IN_CELL	0
A[6]	127	IN_CELL	1
A[5]	126	IN_CELL	0

Pin/Enable	Register Bit	Cell Type	Device I.D.
A[4]	125	IN_CELL	0
A[3]	124	IN_CELL	1
A[2]	123	IN_CELL	1
A[1]	122	IN_CELL	0
A[0]	121	IN_CELL	1
TFPI	120	IN_CELL	0
TLD	119	IN_CELL	1
TSD	118	IN_CELL	0
Tied to Logic ‘0’	117	IN_CELL	1
LIFSEL	116	IN_CELL	1
PECLV	115	IN_CELL	1
RBYP	114	IN_CELL	0
TERR	113	IN_CELL	0
TEOP	112	IN_CELL	0
TDAT[15]	111	IN_CELL	0
TDAT[14]	110	IN_CELL	1
TDAT[13]	109	IN_CELL	1
TDAT[12]	108	IN_CELL	0
TDAT[11]	107	IN_CELL	0
TDAT[10]	106	IN_CELL	1
TDAT[9]	105	IN_CELL	1
TDAT[8]	104	IN_CELL	0
TDAT[7]	103	IN_CELL	1
TDAT[6]	102	IN_CELL	-
TDAT[5]	101	IN_CELL	-
TDAT[4]	100	IN_CELL	-
TDAT[3]	99	IN_CELL	-
TDAT[2]	98	IN_CELL	-
TDAT[1]	97	IN_CELL	-
TDAT[0]	96	IN_CELL	-
TMOD	95	IN_CELL	-
TPRTY	94	IN_CELL	-
TSOC/TSOP	93	IN_CELL	-
TENB	92	IN_CELL	-
TCA/TPA	91	OUT_CELL	-
TFCLK	90	IN_CELL	-
REON	89	OUT_CELL	-
RFCLK	88	IN_CELL	-
RENB	87	IN_CELL	-
RERR	86	OUT_CELL	-
RVAL	85	OUT_CELL	-

Pin/Enable	Register Bit	Cell Type	Device I.D.
RCA/RPA	84	OUT_CELL	-
RSOC/RSOP	83	OUT_CELL	-
REOP	82	OUT_CELL	-
RPRTY	81	OUT_CELL	-
RDAT[15]	80	OUT_CELL	-
RDAT[14]	79	OUT_CELL	-
RDAT[13]	78	OUT_CELL	-
RDAT[12]	77	OUT_CELL	-
RDAT[11]	76	OUT_CELL	-
RDAT[10]	75	OUT_CELL	-
RDAT[9]	74	OUT_CELL	-
RDAT[8]	73	OUT_CELL	-
RDAT[7]	72	OUT_CELL	-
RDAT[6]	71	OUT_CELL	-
RDAT[5]	70	OUT_CELL	-
RDAT[4]	69	OUT_CELL	-
RDAT[3]	68	OUT_CELL	-
RDAT[2]	67	OUT_CELL	-
RDAT[1]	66	OUT_CELL	-
RMOD	65	OUT_CELL	-
RDAT[0]	64	OUT_CELL	-
SYSSEL	63	IN_CELL	-
POS_ATMB	62	IN_CELL	-
RLD	61	OUT_CELL	-
RLDCLK	60	OUT_CELL	-
RSD	59	OUT_CELL	-
RSDCLK	58	OUT_CELL	-
RALRM	57	OUT_CELL	-
RCLK	56	OUT_CELL	-
RFPO	55	OUT_CELL	-
OOF	54	OUT_CELL	-
PICLK	53	IN_CELL	-
PIN[0]	52	IN_CELL	-
PIN[1]	51	IN_CELL	-
PIN[3]	50	IN_CELL	-
PIN[4]	49	IN_CELL	-
FPIN	48	IN_CELL	-
PIN[2]	47	IN_CELL	-
PIN[7]	46	IN_CELL	-
PIN[6]	45	IN_CELL	-
PTCLK	44	IN_CELL	-

Pin/Enable	Register Bit	Cell Type	Device I.D.
PIN[5]	43	IN_CELL	-
POUT[0]	42	OUT_CELL	-
POUT[1]	41	OUT_CELL	-
FPOUT	40	OUT_CELL	-
POUT[5]	39	OUT_CELL	-
POUT[4]	38	OUT_CELL	-
POUT[3]	37	OUT_CELL	-
POUT[2]	36	OUT_CELL	-
POUT[6]	35	OUT_CELL	-
POUT[7]	34	OUT_CELL	-
INTB_OEN	33	OUT_CELL	-
INTB	32	OUT_CELL	-
D[7]	31	IO_CELL	-
D[7]_OEN	30	OUT_CELL	-
D[6]	29	IO_CELL	-
D[6]_OEN	28	OUT_CELL	-
D[5]	27	IO_CELL	-
D[5]_OEN	26	OUT_CELL	-
D[4]	25	IO_CELL	-
D[4]_OEN	24	OUT_CELL	-
D[3]	23	IO_CELL	-
D[3]_OEN	22	OUT_CELL	-
D[2]	21	IO_CELL	-
D[2]_OEN	20	OUT_CELL	-
D[1]	19	IO_CELL	-
D[1]_OEN	18	OUT_CELL	-
D[0]	17	IO_CELL	-
D[0]_OEN	16	OUT_CELL	-
APS[4]	15	IO_CELL	-
APS[4]_OEN	14	OUT_CELL	-
APS[3]	13	IO_CELL	-
APS[3]_OEN	12	OUT_CELL	-
APS[2]	11	IO_CELL	-
APS[2]_OEN	10	OUT_CELL	-
APS[1]	9	IO_CELL	-
APS[1]_OEN	8	OUT_CELL	-
APS[0]	7	IO_CELL	-
APS[0]_OEN	6	OUT_CELL	-
TCLK	5	OUT_CELL	-
TFPO	4	OUT_CELL	-
TLDCLK	3	OUT_CELL	-

Pin/Enable	Register Bit	Cell Type	Device I.D.
TSDCLK	2	OUT_CELL	-
HIZ	1	OUT_CELL	-
TCK		TAP Input	-
TMS		TAP Input	-
TDI		TAP Input	-
TDO		TAP Output	-
TRSTB		TAP Input	-

NOTES:

1. Enable “pinname_OEN” tristates pin “pinname” when set high.

2. ROEN is the active low output enable for RDAT[15:0], RSOC/RSOP, RVAL, RPRTY, REOP, RERR and RMOD.

3. HIZ is the active low output enable for all OUT_CELL types except D[7:0], RDAT[15:0], RSOC/RSOP, RVAL, RPRTY, REOP, RERR, RMOD, APS[4:0] and INTB.

4. RSTB is the first bit of the boundary scan chain closest to the TDI TAP input.

12.2.1 Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table located above.

Figure 14: Input Observation Cell (IN_CELL)

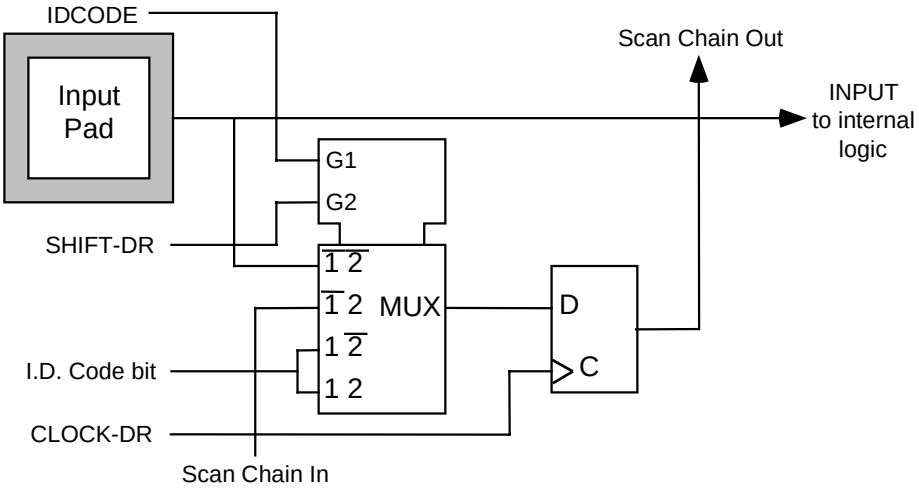


Figure 15: Output Cell (OUT_CELL)

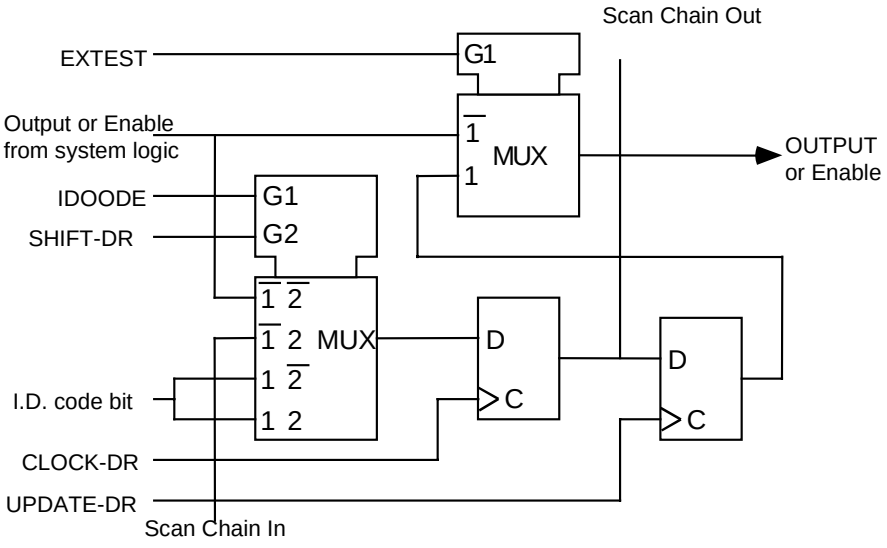


Figure 16: Bidirectional Cell (IO_CELL)

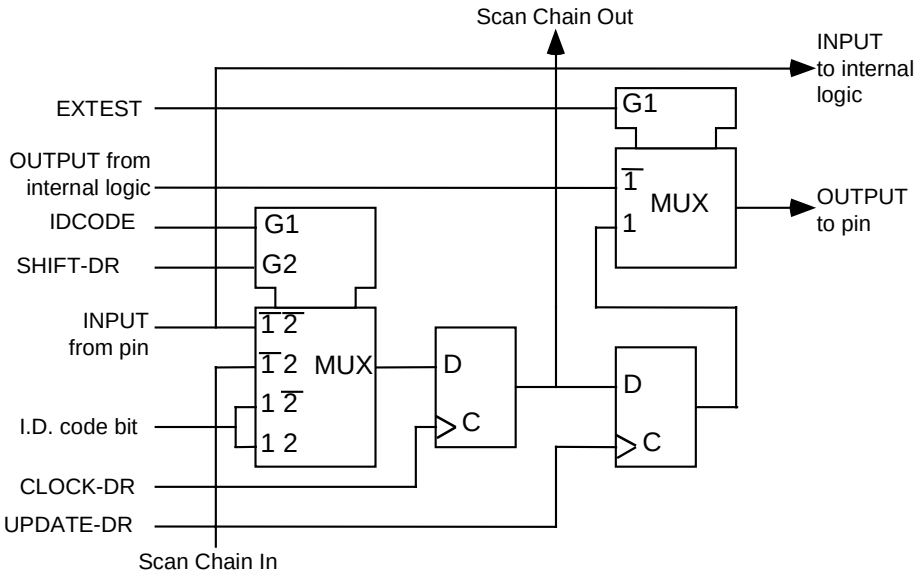
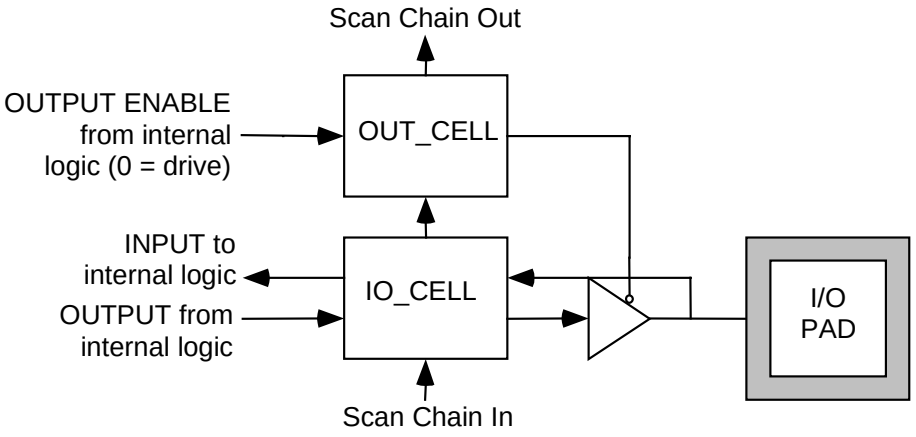


Figure 17: Layout of Output Enable and Bidirectional Cells



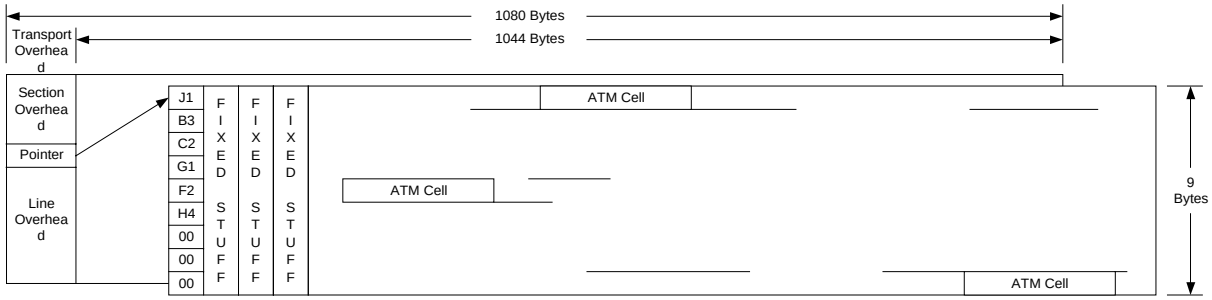
13 OPERATION

13.1 SONET/SDH Frame Mappings and Overhead Byte Usage

13.1.1 ATM Mapping

The S/UNI-622-POS processes the ATM cell mapping for STS-12c/STM-4-4c as shown below in Figure 18. The S/UNI-622-POS processes the transport and path overhead required to support ATM UNIs and NNIs. In addition, the S/UNI-622-POS provides support for the APS bytes, the data communication channels and provides full control and observability of the transport and path overhead bytes through register access. In Figure 18, the STS-12c/STM-4-4c mapping is shown. In this mapping, three stuff columns are included in the SPE. No other options are provided.

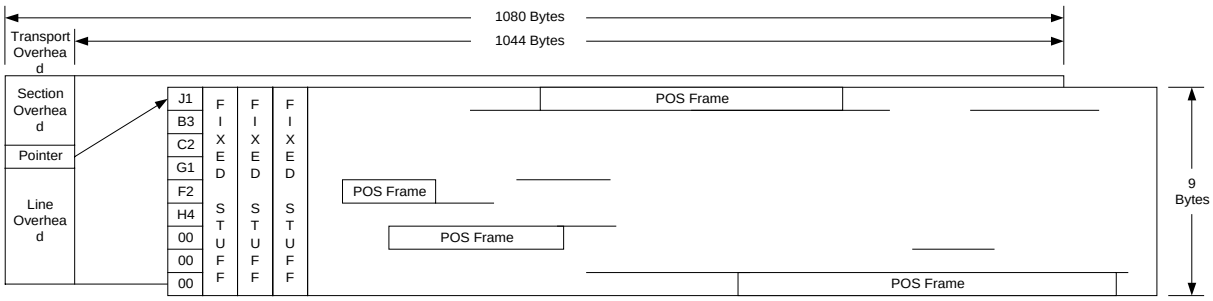
Figure 18: ATM Mapping into the STS-12c/STM-4-4c SPE



13.1.2 Packet over SONET/SDH Mapping

The S/UNI-622-POS processes the Packet over SONET/SDH mapping for STS-12c/STM-4-4c as shown below in Figure 19. The S/UNI-622-POS processes the transport and path overhead required to support Packet over SONET/SDH applications. In addition, the S/UNI-622-POS provides support for the APS bytes, the data communication channels and provides full control and observability of the transport and path overhead bytes through register access. In Figure 19, the STS-12c/STM-4-4c mapping is shown. In this mapping, the entire SPE is used for POS Frames.

Figure 19: POS Mapping into the STS-12c/STM-4-4c SPE



13.1.3 Transport and Path Overhead Bytes

Under normal operating conditions, the S/UNI-622-POS processes a subset of the complete transport overhead present in an STS-12c/STM-4-4c stream. The byte positions processed by the S/UNI-622-POS are indicated in Figure 20.

Figure 20: STS-12c/STM-4-4c Overhead

STS-12c Transport Overhead
STM-4 Section Overhead

A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A1	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	A2	J0	Z0	Z0	Z0								
B1												E1												F1											
D1												D2												D3											
H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H1	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3
B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	B2	K1												K2											
D4												D5												D6											
D7												D8												D9											
D10												D11												D12											
S1	Z1	Z1										Z2	Z2	M1										E2											

Transport Overhead Bytes

A1, A2: The frame alignment bytes (A1, A2) locate the SONET/SDH frame in the STS-12c/STM-4-4c serial stream.

J0 The J0 byte is currently defined as the STS-12c/STM-4-4c section trace byte for SONET/SDH. J0 byte is not scrambled by the frame synchronous scrambler.

Z0: The Z0 bytes are currently defined as the STS-12c/STM-4-4c section growth bytes for SONET/SDH. Z0 bytes are not scrambled by the frame synchronous scrambler.

B1: The section bit interleaved parity byte provides a section error monitoring function.

In the transmit direction, the S/UNI-622-POS calculates the B1 byte over all bits of the previous frame after scrambling. The calculated code is then placed in the current frame before scrambling.

In the receive direction, the S/UNI-622-POS calculates the B1 code over the current frame and compares this calculation with the B1 byte received in the following frame. B1 errors are accumulated in an error event counter.

D1 - D3: The section data communications channel provides a 192 kbit/s data communications channel for network element to network element communications.

In the transmit direction, the section DCC byte is inserted from a dedicated 192 kbit/s input, TSD.

In the receive direction, the section DCC is extracted on a dedicated 192 kbit/s output, RSD.

H1, H2: The pointer value bytes locate the path overhead column in the SONET/SDH frame.

In the transmit direction, the S/UNI-622-POS inserts a fixed pointer value, with a normal new data flag indication in the first H1-H2 pair. The concatenation indication is inserted in the remaining H1-H2 pairs (STS-12c/STM-4-4c). Pointer movements can be induced using the TPOP registers.

In the receive direction, the pointer is interpreted to locate the SPE. The loss of pointer state is entered when a valid pointer cannot be found. Path AIS is detected when H1, H2 contain an all ones pattern.

H3: The pointer action bytes contain synchronous payload envelope data when a negative stuff event occurs. The all zeros pattern is inserted in the transmit direction. This byte is ignored in the receive direction unless a negative stuff event is detected.

B2: The line bit interleaved parity bytes provide a line error monitoring function.

In the transmit direction, the S/UNI-622-POS calculates the B2 values. The calculated code is then placed in the next frame.

In the receive direction, the S/UNI-622-POS calculates the B2 code over the current frame and compares this calculation with the B2 code receive in the following frame. Receive B2 errors are accumulated in an error event counter.

K1, K2: The K1 and K2 bytes provide the automatic protection switching channel. The K2 byte is also used to identify line layer maintenance signals. Line RDI is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '110'. Line AIS is indicated when bits 6, 7, and 8 of the K2 byte are set to the pattern '111'.

In the transmit direction, the S/UNI-622-POS provides register control for the K1 and K2 bytes.

In the receive direction, the S/UNI-622-POS provides register access to the filtered APS channel. Protection switch byte failure alarm detection is provided. The K2 byte is examined to determine the presence of the line AIS, or the line RDI maintenance signals

D4 - D12: The line data communications channel provides a 576 kbit/s data communications channel for network element to network element communications.

In the transmit direction, the line DCC byte is inserted from a dedicated 576 kbit/s input, TLD.

In the receive direction, the line DCC is extracted on a dedicated 576 kbit/s output, RLD.

S1: The S1 byte provides the synchronization status byte. Bits 5 through 8 of the synchronization status byte identifies the synchronization source of the STS-12c/STM-4-4c signal. Bits 1 through 4 are currently undefined.

In the transmit direction, the S/UNI-622-POS provides register control for the synchronization status byte.

In the receive direction, the S/UNI-622-POS provides register access to the synchronization status byte. The SSTB block also provides circuitry to detect synchronization status mismatch and unstable alarms.

Z1: The Z1 bytes are located in the second and third STS-1's locations of an STS-12c/STM-4-4c and are allocated for future growth.

M1: The M1 byte is located in the third STS-1 locations of a STS-12c/STM-4-4c and provides a line far end block error function for remote performance monitoring.

Z2: The Z2 bytes are located in the first and second STS-1's locations of a STS-12c/STM-4-4c and are allocated for future growth.

In the transmit direction, Z2 byte is internally generated. The number of B2 errors detected in the previous interval is inserted.

In the receive direction, a legal Z2 byte value is added to the line FEBE event counter.

Path Overhead Bytes

J1: The Path Trace byte is used to repetitively transmit a 64-byte CLLI message (for SONET/SDH networks), or a 16-byte E.164 address (for SDH networks). When not used, this byte should be set to transmit continuous null characters. Null is defined as the ASCII code, 0x00.

In the transmit direction, characters can be inserted using the TPOP Path Trace register or the SPTB block. The register is the default selection and resets to 0x00 to enable the transmission of NULL characters from a reset state.

In the receive direction, the path trace message is optionally extracted into the 16 or 64 byte path trace message buffer.

B3: The path bit interleaved parity byte provides a path error monitoring function.

In the transmit direction, the S/UNI-622-POS calculates the B3 bytes. The calculated code is then placed in the next frame.

In the receive direction, the S/UNI-622-POS calculates the B3 code and compares this calculation with the B3 byte received in the next frame. B3 errors are accumulated in an error event counter.

C2: The path signal label indicator identifies the equipped payload type. For ATM payloads, the identification code is 0x13. For Packet over SONET/SDH (including $X^{43}+1$ payload scrambling), the identification code is 0x16.

In the transmit direction, the S/UNI-622-POS inserts the value 0x13 or 0x16 using the TPOP Path Signal Label register.

In the receive direction, the code is available in the RPOP Path Signal Label register. In addition, the SPTB block also provides circuitry to detect path signal label mismatch and unstable alarms.

G1: The path status byte provides a path FEBE function, and a path remote defect indication function. Three bits are allocated for remote defect indications: bit 5 (the path RDI bit), bit 6 (the auxiliary path RDI bit) and bit 7 (Enhanced RDI bit). Taken together these bits provide a eight state path RDI code that can be used to categorize path defect indications.

In the transmit direction, the S/UNI-622-POS provides register bits to control the path RDI (bit 5) and auxiliary path RDI (bit 6) states. For path FEBE, the number of B3 errors detected in the previous interval is inserted either automatically or using a register. This path FEBE code has 9 legal values, namely 0 to 8 errors.

In the receive direction, a legal path FEBE value is accumulated in the path FEBE event counter. In addition, the path RDI and auxiliary path RDI signal states are available in internal registers.

H4: The multi-frame indicator byte is a payload specific byte, and is not used for ATM payloads. This byte is forced to 0x00 in the transmit direction, and is ignored in the receive direction.

Z3 - Z5: The path growth bytes provide three unused bytes for future use.

In the transmit direction, the growth bytes may be inserted from the three TPOP Path Growth byte registers.

13.2 ATM Cell Data Structure

ATM cells may be passed to/from the S/UNI-622-POS using a 27 word, 16-bit UTOPIA level 2 compliant data structure or using a 54 byte, 8-bit UTOPIA level 3 compliant data structure. The former data structure is shown in Figure 21 and described below.

Figure 21: 16-bit Wide, 27 Word ATM Cell Structure

	Bit 15 Bit 8	Bit 7 Bit 0
Word 1	H1	H2
Word 2	H3	H4
Word 3	H5	HCS Status/Control
Word 4	Payload 1	Payload 2
Word 5	Payload 3	Payload 4
Word 6	Payload 5	Payload 6
Word 7	Payload 7	Payload 8
Word 8	Payload 9	Payload 10
	⋮	⋮
Word 27	Payload 47	Payload 48

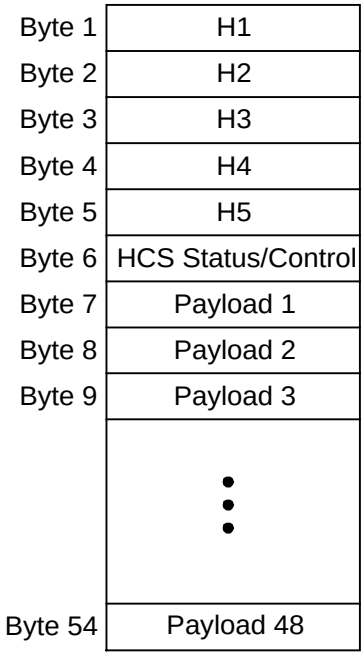
Bit 15 of each word is the most significant bit (which corresponds to the first bit transmitted or received). The header check sequence octet (HCS) is passed through this structure. The start of cell indication input and output (TSOC and RSOC) are coincident with Word 1 (containing the first two header octets). Word 3 of this structure contains the HCS octet in bits 15 to 8.

In the receive direction, the lower 8 bits of Word 3 contain the HCS status octet. An all-zeros pattern in these 8 bits indicates that the associated header is error free. An all-ones pattern indicates that the header contains an uncorrectable error (if the HCSPASS bit in the RXCP Control Register is set to logic zero, the all-ones pattern will never be passed in this structure). An alternating ones and zeros pattern (0xAA) indicates that the header contained a correctable error. In this case the header passed through the structure is the "corrected" header.

In the transmit direction, the HCS bit in the TXCP Control register determines whether the HCS is calculated internally or is inserted directly from the upper 8 bits of Word 3. The lower 8 bits of Word 3 contain the HCS control octet. The HCS control octet is an error mask that allows the insertion of one or more errors in the HCS octet. A logic one in a given bit position causes the inversion of the corresponding HCS bit position (for example a logic one in bit 7 causes the most significant bit of the HCS to be inverted). The HDCL control octet may be disabled by setting the HCSCTLEB register in the TXCP.

ATM cells can also be passed to/from the S/UNI-622-POS using a 54 byte, 8-bit UTOPIA level 3 compliant data structure shown in Figure 22.

Figure 22: 8-bit Wide, 54 Byte ATM Cell Structure



Bit 7 of each byte is the most significant bit (which corresponds to the first bit transmitted or received). The header check sequence octet (HCS) is passed through this structure. The start of cell indication input and output (TSOC and RSOC) are coincident with Byte 1.

13.3 Packet over SONET/SDH Data Structure

Packets may be written into the TXFP FIFO and read from the RXFP FIFO using either a 16-bit POS-PHY Level 2 or an 8-bt POS-PHY Level 3 defined data structure.

The 16-bit POS-PHY Level 2 data structure is shown in Figure 23. The packet length of 63 bytes is chosen arbitrarily for illustrative purposes only. Other lengths are acceptable. Octets are written in the same order they are to be transmitted or they were received on the SONET/SDH line. Within an octet, the MSB (bit 7) is the first bit to be transmitted. All words are composed of two octets, except the last word of a packet which can have one or two bytes. If the TXFP is configured to not insert the FCS field, then these bytes should be included at the end of the packet. Similarly, if the RXFP is configured to not strip the FCS field, then these bytes will be included at the end of the packet.

Figure 23: A 63 Byte Packet Data Structure

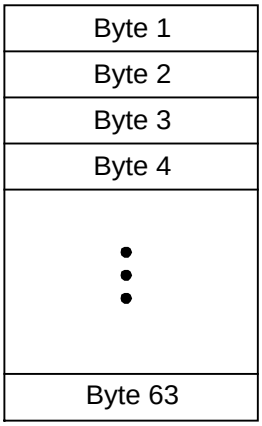
	Bit 15 Bit 8	Bit 7 Bit 0
Word 1	Byte 1	Byte 2
Word 2	Byte 3	Byte 4
Word 3	Byte 5	Byte 6
Word 4	Byte 7	Byte 8
Word 5	Byte 9	Byte 10
Word 6	Byte 11	Byte 12
Word 7	Byte 13	Byte 14
	⋮	⋮
Word 32	Byte 63	XX

A 63 Byte Frame

The 8-bit POS-PHY Level 3 data structure is shown in Figure 24. The packet length of 63 bytes is chosen arbitrarily for illustrative purposes only. Other lengths are acceptable. However, on the transmit interface, packets with an odd number of bytes must be transferred with a one clock pause (TENB high).

Octets are written in the same order they are to be transmitted or they were received on the SONET/SDH line. Within an octet, the MSB (bit 7) is the first bit to be transmitted. If the TXFP does not insert the FCS field, then these bytes should be included at the end of the packet. If the RXFP does not strip the FCS field, then these bytes will be included at the end of the packet.

Figure 24: A 63 Byte Packet Data Structure



A 63 Byte Frame

Both the start of the packet and the end of the packet must be identified by the TSOP/RSOP and TEOP/REOP signals. When the first section of a packet is transferred over the interface, the TSOP/RSOP signals will be high for Byte 1 of the packet only.

13.4 Setting ATM Mode of Operation

The following sequence of operation should be used to prepare the device for the ATM operation.

1- Input pin POS_ATMB (Y21) should be tied low to enable ATM operation. This pin can be overridden in software by writing a logic one to the RMOVR bit (Register 0x90) and TMOVR bit (Register 0x92). Writing a logic zero to the RPOS_ATMB bit (Register 0x90) and the TPOS_ATMB bit (Register 0x92) can then be used to enable ATM operation.

When using the software override feature, these bits must be set after step (2), as resetting the device restores the registers to their default values. This feature is useful for building a single PHY card that can be configured in software as a POS or ATM card.

2- Reset the device. This can be done by asserting the RSTB pin or setting the RESET bit in the Master Reset and ID Register (Register 0x00).

3- If the TFCLK, RFCLK and/or the PTCLK (if used) clock inputs are not stable clocks, wait until these clock inputs stabilize. Reset the DLL units associated with each clock input (write 0x00 to Registers 0x96, 0x9A and 0x9E respectively).

4- Reset the receive and transmit FIFO's by setting the FIFORST register bit in the TXCP (Register 0x80) and RXCP (Register 0x62) blocks. Keep this bit set for at least 1 µs, then set the bit back to its inactive logic zero value.

5- Set the path signal label C2 byte (offset 0x054 and 0x048) to 0x13 to identify ATM payload data.

6- Reset the performance monitoring counters in TXCP and RXCP blocks by writing a logic zero to the Master Reset and Identity register (Register 0x00). TIP remains high as the performance monitoring registers are loaded, and is set to a logic zero when the transfer is complete.

13.5 Setting Packet-Over-SONET/SDH Mode of Operation

The following sequence of operation should be used to prepare the device for the Packet over SONET/SDH (POS) operation.

1- Input pin POS_ATMB (Y21) should be tied high to enable POS operation. This pin can be overridden in software by writing a logic one to the RMOVR bit (Register 0x90) and TMOVR bit (Register 0x92). Writing a logic one to the RPOS_ATMB bit (Register 0x90) and the TPOS_ATMB bit (Register 0x92) can then be used to enable POS operation.

When using the software override feature, these bits must be set after step (2), as resetting the device restores the registers to their default values. This feature is useful for building a single PHY card that can be configured in software as a POS or ATM card.

2- Reset the device. This can be done by asserting the RSTB pin or setting the RESET bit in the Master Reset and ID Register (Register 0x00).

3- If the TFCLK, RFCLK and/or the PTCLK (if used) clock inputs are not stable clocks, wait until these clock inputs stabilize. Reset the DLL units associated with each clock input (write 0x00 to Registers 0x96, 0x9A and 0x9E respectively).

4- Reset the receive and transmit FIFO's by setting the FIFORST register bit in the TXFP (Register 0xC1) and RXFP (Register 0xA0) blocks. Keep this bit set for at least 1 μs, then set the bit back to its inactive logic zero value.

5- Set the path signal label C2 byte (offset 0x054 and 0x048) to 0x16 to identify POS payload data.

6- Reset the performance monitoring counters in TXFP and RXFP blocks by writing a logic zero to the Master Reset and Identity register (Register 0x00). TIP remains high as the performance monitoring registers are loaded, and is set to a logic zero when the transfer is complete.

13.6 Setting SONET or SDH Mode of Operation

The SONET and SDH standard for optical networking are very similar with only minor difference in overhead processing. The main difference between the SONET (Bellcore GR-253-CORE) and SDH (ITU.707) standards lies in the handling of some of the overhead bytes. Other details, like framing and data payload mappings are equivalent in SONET and SDH.

The bit error rate (BER) monitoring requirements are also slightly different between SONET and SDH. An application note, PMC-950820, explains the different parameters in detail for the RASE block.

The list below shows the various register setting to configure the S/UNI-16x155 for either SONET or SDH operation.

Table 14: Settings for SONET or SDH Operation

Configuration Registers	SONET	SDH
SDH_J0/Z0 (register offset 0x004)	0	X
ENSS (register offset 0x03D)	0	1
Path LEN16 (register offset 0x028)	0	1
Section LEN16 (register offset 0x050)	0	1
S[1:0] (register offset 0x46)	00	10

Notes:

1. SONET requires Z0 bytes to be set to the number corresponding to the STS-1 column number. SDH considers those bytes reserved.

2. When forcing a constant Z0 pattern (SDH_J0/ZO is high), the Z0 bytes must be DC balanced (approximately the same number of ones and zeros) as the bytes are not scrambled. Failure to do so may cause downstream clock recovery to lose lock.

3. SONET uses 64 byte trace messages while SDH uses 16 byte trace messages.

4. SDH specification requires the detector of SS bits to be “10”.

5. The SS bits are undefined for SONET, but must be set to “10” for SDH.

13.7 Bit Error Rate Monitor

The S/UN-622-POS provides two BERM blocks. One can be dedicated to monitor at the Signal Degrade (SD) error rate and the other dedicated to monitor at the Signal Fail (SF) error rate.

The Bit Error Rate Monitor (BERM) block counts and monitors line BIP errors over programmable periods of time (window size). It can monitor to declare an alarm or to clear it if the alarm is already set. A different threshold and accumulation period must be used to declare or clear the alarm, whether or not those two operations are not performed at the same BER. The following table lists the recommended content of the BERM registers for different error rates (BER). Both BERMs in the TSB are equivalent and are programmed similarly. In a normal application they will be set to monitor different BER.

When the SF/SD CMODE bit is set to one, the clearing monitoring is recommended to be performed using a window size that is 8 times longer than the declaration window size. When the SF/SD CMODE bit is set to zero, the clearing monitoring is recommended to be performed using a window size equal to the declaration window size. In all cases the clearing threshold is calculated for a BER that is 10 times lower than the declaration BER, as required in the references. The table indicates the declare BER and evaluation period only.

The saturation threshold is not listed in the table, and should be programmed with the value 0xFFF by default, deactivating saturation. Saturation capabilities are provided to allow the user to address issues associated with error bursts.

For additional information, please refer to the BERM application note (PMC-950820) for more detailed information.

Table 15: Recommended BERM settings

STS	Declare BER	Evals / Second	SF/SD SMODE	SF/SD CMODE	SF/SD SAP	SF/SD DTH	SF/SD CTH
STS-12c	10^{-3}	0.008	0	0	0x000008	0x956	0x1E9
STS-12c	10^{-4}	0.008	0	0	0x000008	0x1A5	0x03D
STS-12c	10^{-5}	0.025	0	1	0x000019	0x084	0x08E
STS-12c	10^{-6}	0.250	0	1	0x0000FA	0x085	0x08E
STS-12c	10^{-7}	2.500	0	1	0x0009C4	0x085	0x08E
STS-12c	10^{-8}	21.000	0	1	0x005208	0x06E	0x079
STS-12c	10^{-9}	167.000	0	1	0x028C58	0x056	0x062
STS-3c	10^{-3}	0.008	0	0	0x000008	0x245	0x083
STS-3c	10^{-4}	0.013	0	1	0x00000D	0x0A3	0x0B4
STS-3c	10^{-5}	0.100	0	1	0x000064	0x084	0x08E
STS-3c	10^{-6}	1.000	0	1	0x0003E8	0x085	0x08E
STS-3c	10^{-7}	10.000	0	1	0x002710	0x085	0x08E
STS-3c	10^{-8}	83.000	0	1	0x014438	0x06D	0x077
STS-3c	10^{-9}	667.000	0	1	0x0A2D78	0x055	0x061

13.8 Auto Alarm Control Configuration

The S/UNI-622-POS supports the automatic generation of transmit alarm information based on the detected receive alarms. This functionality is controlled by the master AUTOxx register bits in register 0x02 and the Auto Path and Line Configuration registers 0x08 to 0x0F.

When consequential action is enabled for a given alarm condition, other S/UNI-622-POS configuration registers become important. For instance, if consequential action for signal degrade is enabled, the RASE must be configured for the desired alarm thresholds. The following table lists register settings for path RDI and extended path RDI interfaces.

Table 16: Path RDI and Extended RDI Register Settings

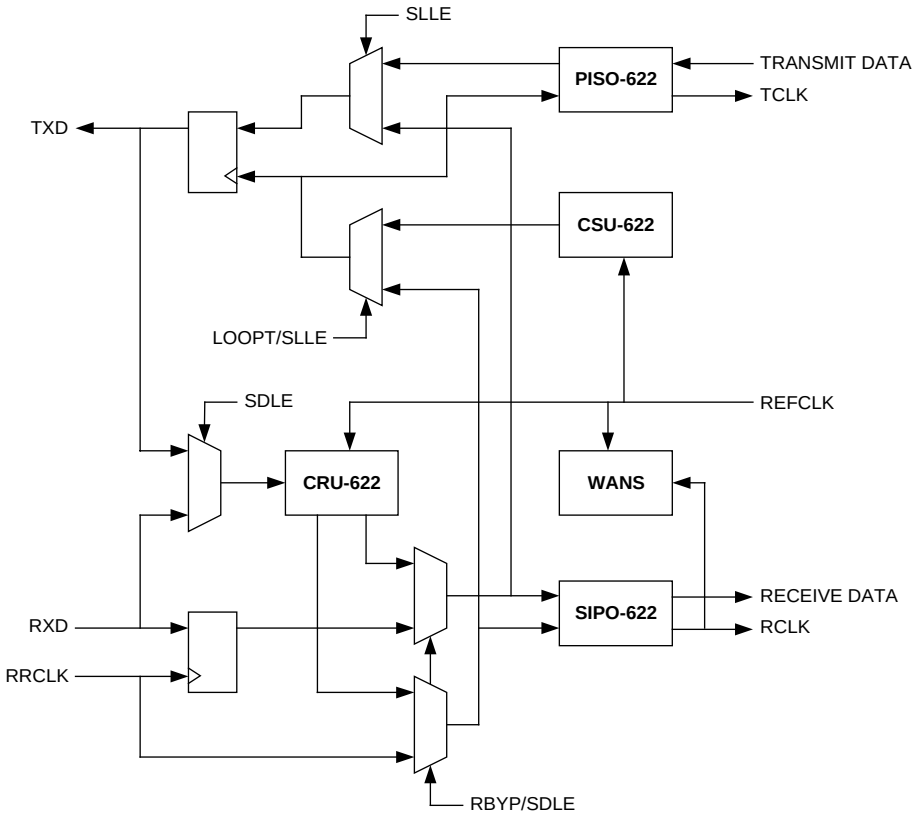
Register	RDI	EPRDI
0x09	11111111	01101111
0x0A	Xxxxxxxx	11111111

0x0B	10xxx010	11xxx111
0x40	x00x00xx	x11x00xx

13.9 Clocking Options

The S/UNI-622-POS supports several clocking modes. Figure 25 is an abstraction of the clocking topology. The S/UNI-622-POS can operate in source time, internally loop timed and externally loop timed.

Figure 25: Clocking Structure



Source timed operation is used for all public user network interfaces (UNIs) and for private UNIs and private network node interfaces (NNIs) that are not synchronized to the recovered clock.

The transmit clock in a public UNI must conform to SONET/SDH Network Element (NE) requirements specified in Bellcore GR-253-CORE. These requirements include jitter generation, short term clock stability, phase transients during synchronization failure, and holdover. The 77.76 MHz clock source is

typically a VCO (or temperature compensated VCXO) locked to a primary reference source for public UNI applications. The accuracy of this clock source should be within ±20 ppm of 77.76 MHz to comply with the SONET/SDH network element free-run accuracy requirements. The S/UNI-622-POS WANS block can be used to implement the system timing reference.

The transmit clock in a private UNI or a private NNI may be locked to an external reference or may free-run. The simplest implementation requires an oscillator free-running at 77.76 MHz.

Source timed operation is selected by clearing the LOOPT bit of the Master Configuration register. REFCLK is multiplied by 8 to become the 622.08 MHz transmit clock. REFCLK must be jitter free. The source REFCLK is also internally used as the clock recovery reference during receive loss of transition conditions.

Internally loop timed operation is used for private UNIs and private NNIs that require synchronization to the recovered clock. This mode is selected by setting the LOOPT bit of the Master Control register to logic one. Normally, the transmit clock is locked to the receive data. In the event of a loss of signal/transition condition, the transmit clock is synthesized from REFCLK.

Externally loop timed operation makes use of the WAN Synchronization block capabilities. This mode can be achieved when LOOPT is set to logic zero. The timing loop is achieved at the system level, through a microprocessor, an external VCXO and back through the REFCLK input. This mode allows an S/UNI-622-POS to meet Bellcore wander transfer and holdover stability requirements.

13.10 WAN Synchronization (WANS Block)

The WANS provides a means to implement a Stratum 3 or lower system timing reference with a minimum amount of external circuitry. The WANS implements a phase detector necessary to create a digital control PLL.

A description of how to program and use the WANS feature will be made available in the S/UNI-622-POS reference design (PMC-981070).

13.11 Loopback Operation

The S/UNI-622-POS supports five loopback functions: path loopback, line loopback, data diagnostic loopback, parallel diagnostic loopback and serial diagnostic loopback. Each channel's loopback modes operate independently.

The loopback modes are activated by the PDLE, LLE, DLE, DPLE and SDLE bits contained in the S/UNI-622-POS Master Configuration registers.

The line loopback, see Figure 26, connects the high speed receive data and clock to the high speed transmit data and clock, and can be used for line side investigations (including clock recovery and clock synthesis). While in this mode, the entire receive path is operating normally and cells can be received through the FIFO interface.

The serial diagnostic loopback, see Figure 27, connects the high speed transmit data and clock to the high speed receive data and clock. While in this mode, the entire transmit path is operating normally and data is transmitted on the TXD+/- outputs.

The parallel diagnostic loopback, see Figure 28, connects the byte wide transmit data and clock to the byte wide receive data and clock. While in this mode, the entire transmit path is operating normally and data is transmitted on the TXD+/- outputs.

The path diagnostic loopback, see Figure 29, connects the transmit path processor TPOP output to the receive path processor RPOP. While in this mode, the entire transmit path is operating normally and data is transmitted on the TXD+/- outputs.

The data diagnostic loopback, see Figure 30, connects the transmit POS/ATM processor TXFP/TXCP) to the corresponding receive POS/ATM processor (RXFP/RXCP). While in this mode, the transmit path does not operate normally and the data transmitted on the TXD+/- outputs is invalid.

Figure 26: Line Loopback Mode

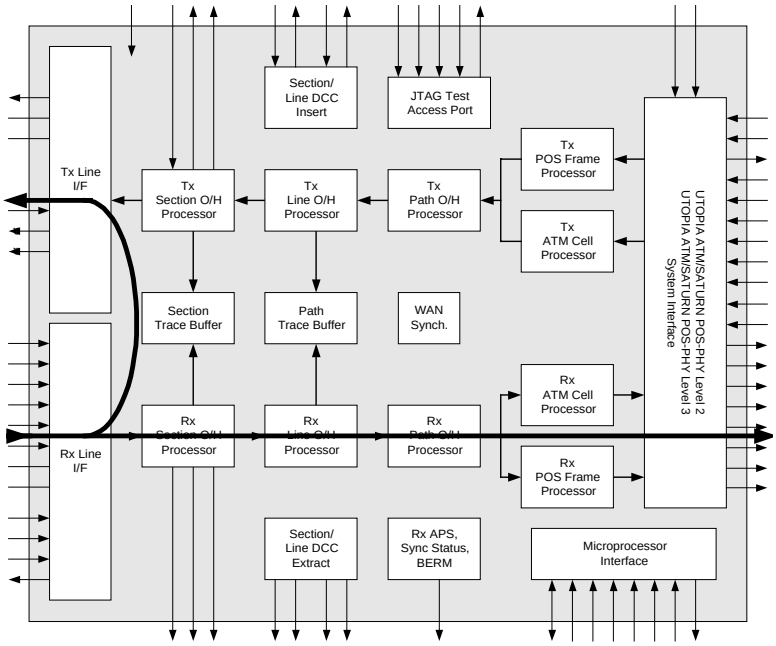


Figure 27: Serial Diagnostic Loopback Mode

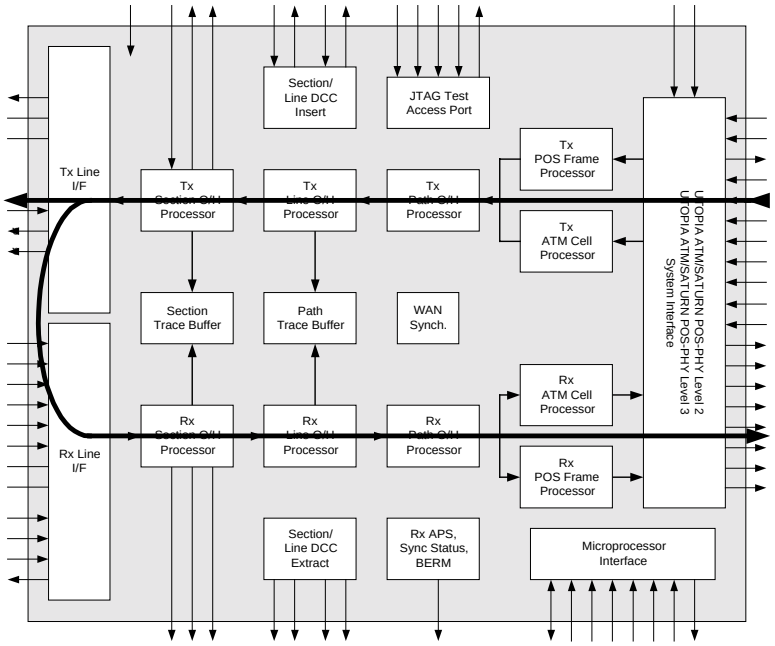


Figure 28: Parallel Diagnostic Loopback Mode

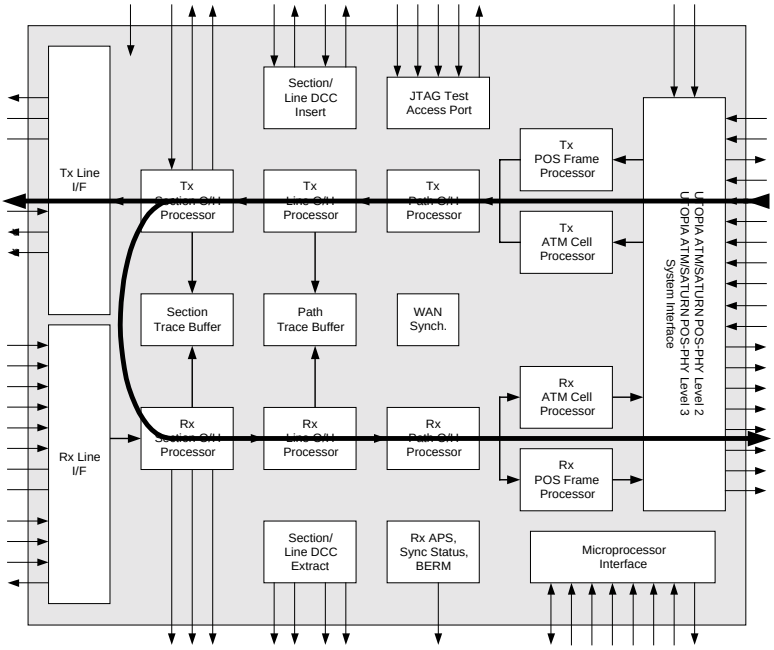


Figure 29: Path Diagnostic Loopback Mode

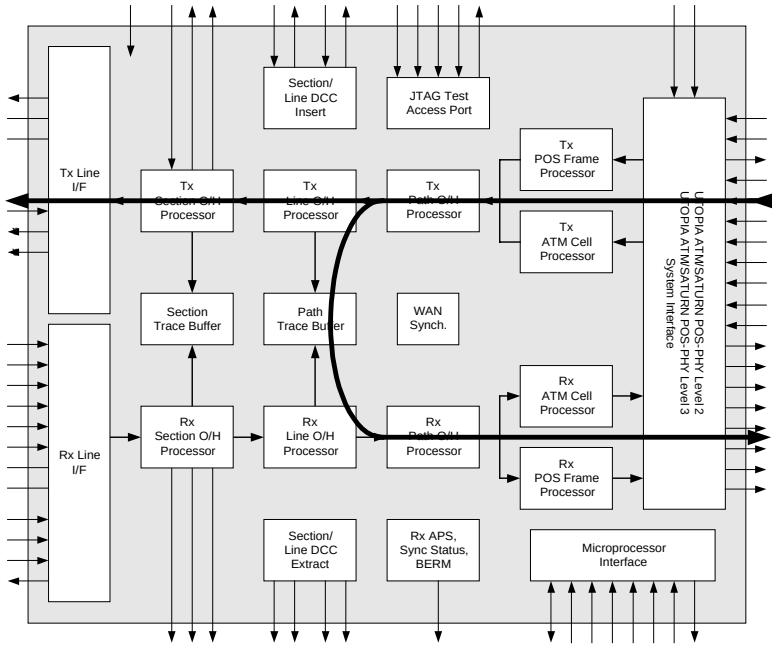
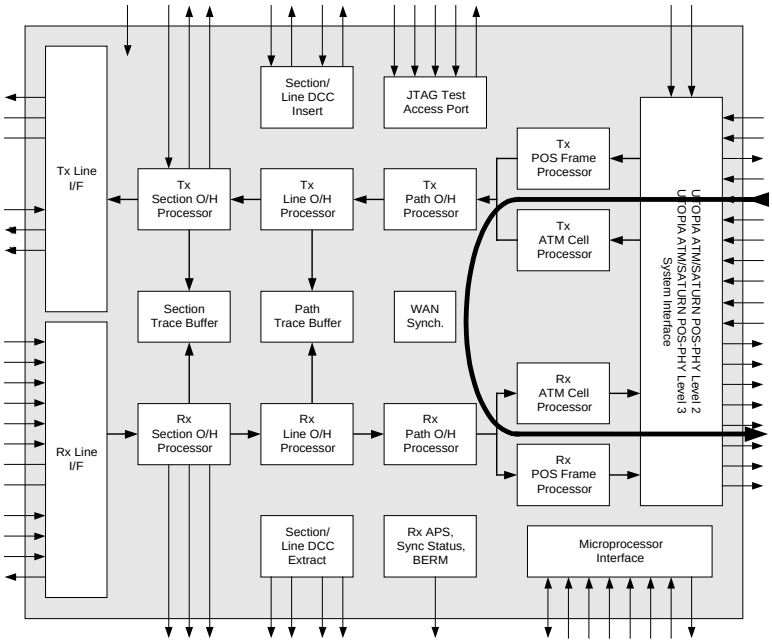


Figure 30: Data Diagnostic Loopback Mode

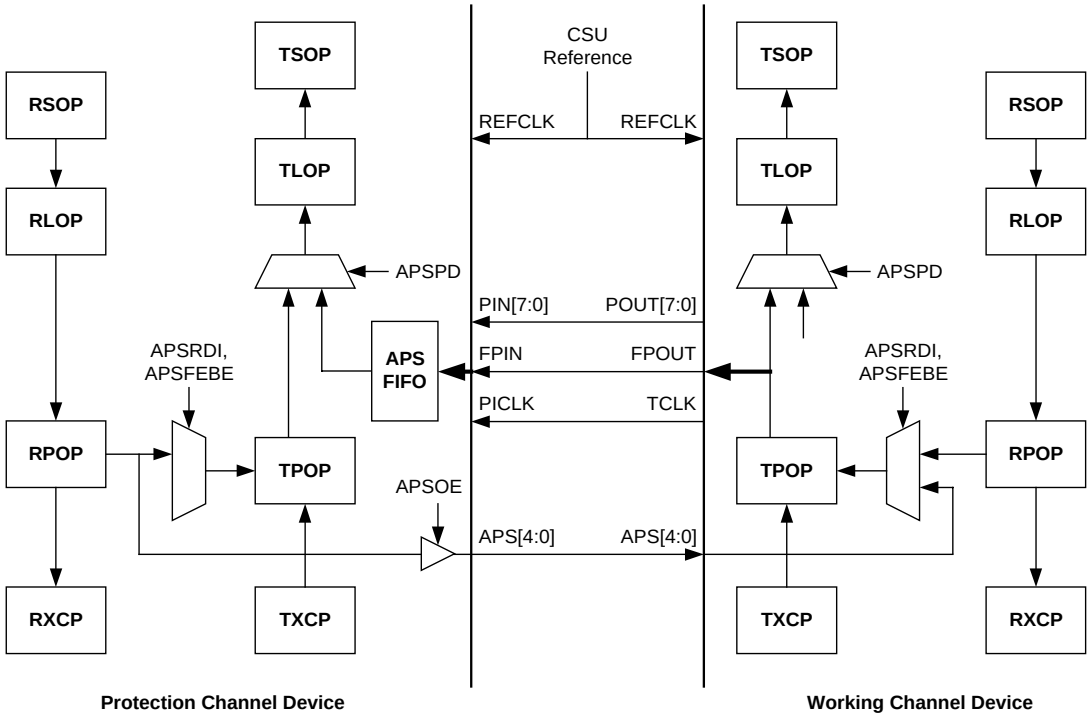


13.12 1+1 APS Support

The S/UNI-622-POS has the ability to exchange transmit path data in order to implement a 1+1 APS interface. In order to use this capability, the serial line side interface must be used (1+1 APS support is not available in OC3 operation) as the parallel line side interface is used as the transmit path APS port.

The diagram in Figure 31 shows how to connect two S/UNI-622-POS devices for 1+1 APS operation. The working device is the source of transmit path for both the working and the protection channels. The transmit path process TPOP as well as the TXCP and TXFP processors are unused in the protection device. The working device sends the transmit path data steam to the protection device using the parallel line interface pins. The protection device adds section and line overhead to the transmit path data stream using its TSOP and TLOP units. Thus, each channel has unique K1/K2 byte control and monitoring.

Figure 31: 1+1 APS Architecture



A 4-byte FIFO is used to handle wander between the TCLK of the working device and the TCLK of the protection device. Both transmit clocks TCLK must be the same frequency in order for this FIFO to operate normally. Therefore, the clock synthesis units (CSU) of both device must have the same reference clock input REFCLK. The working and protection devices cannot operate in loop time as the frequency difference between the receive clock and the reference clock will cause the FIFO to underrun or overrun corrupting the protection transmit path. In order to perform loop-time operation, an external clocking source must be used (for instance, the WANS functionality).

The APS FIFO must be reset after both CSU units lock to the reference clock in order to center the FIFO. This the APSRST bit must be toggled when the ROOLV in the CSPI-622 indicates a CSU has lost lock or after a system reset. The ASPI register will indicate when the FIFO has corrupted data due to an overrun or an underrun.

The active channel is selected using the receive ATM and POS System Interface. Thus, if the protection device is active, the receive System Interface of the protection device is used. If the working device is active, the receive System

Interface of the working device is used. In all cases, the transmit System Interface of the working device is used for the transmit data stream.

In order for the S/UNI-622-POS to support path AUTORDI and AUTOPFEBE functions, the APS[4:0] pins are used to exchange alarm information from the protection device to the TPOP of the working device. Thus, when the protection device is active, the working device must be configured to use the receive path alarm information from the protection device. Table 17 shows the register configurations for both normal operation and protection operation for both devices.

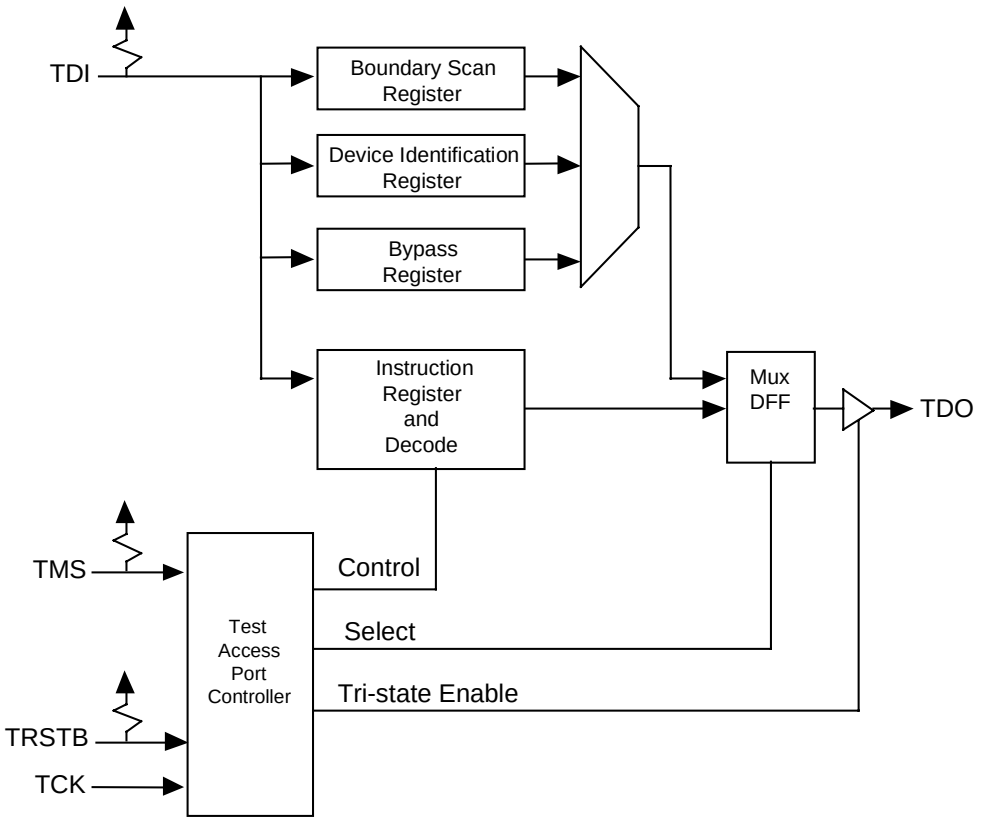
Table 17: 1+1 APS Register 0x06 Settings

Bit	Work Device (Normal)	Protect Device (Normal)	Work Device (Protection)	Protect Device (Protection)
APSEN	1	1	1	1
APSOE	0	1	0	1
APSPD	0	1	0	1
APSFEBE	0	X	1	X
APSRDI	0	X	1	X

13.13 JTAG Support

The S/UNI-622-POS supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 32: Boundary Scan Architecture



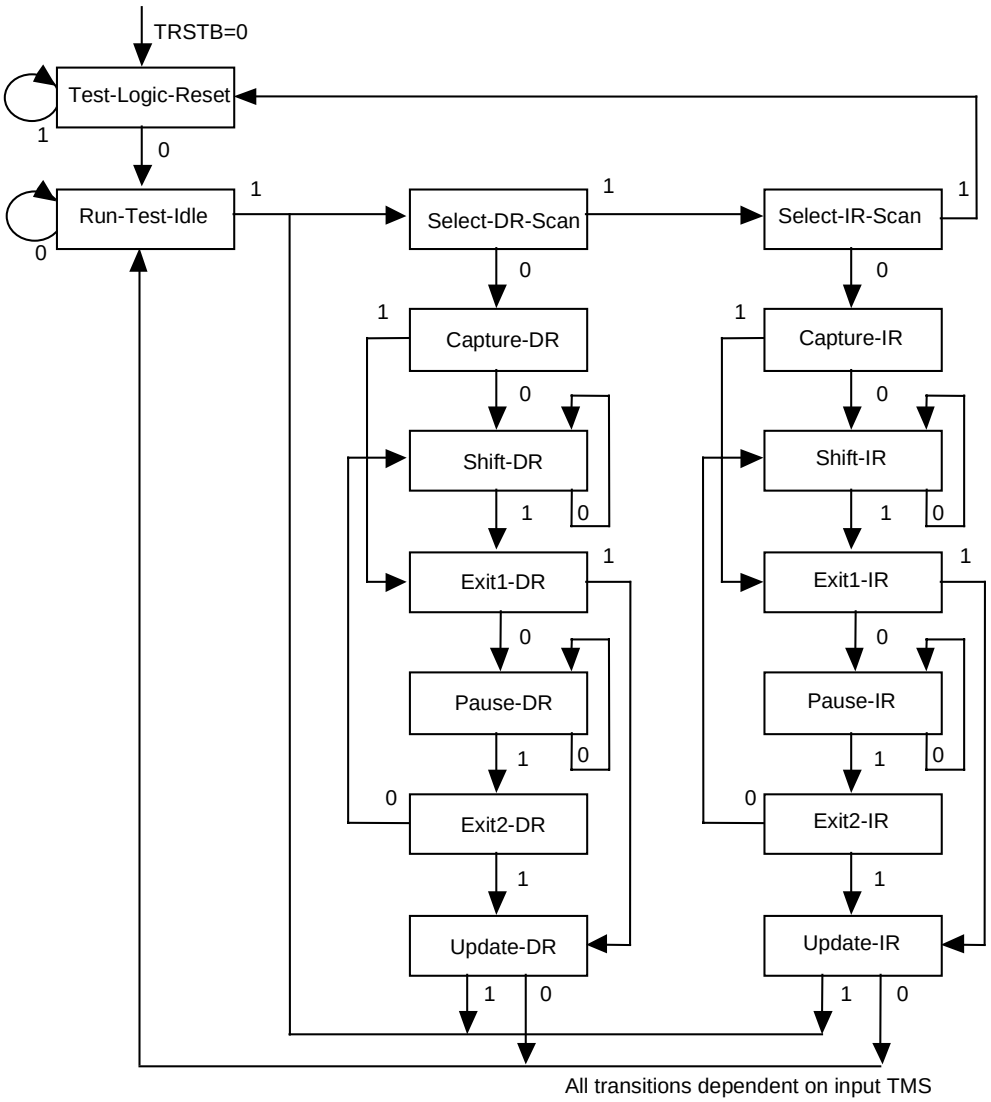
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

13.13.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 33: TAP Controller Finite State Machine



13.13.2 States

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

13.13.3 Instructions

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state.

13.14 Board Design Recommendations

The noise environment and signal integrity are often the limiting factors in system performance. Therefore, the following board design guidelines must be followed in order to ensure proper operation:

1. Use a single plane for both digital and analog grounds.

2. Provide separate +3.3 volt analog and +3.3 volt digital supplies, but otherwise connect the supply voltages together at one point close to the connector where +3.3 volts is brought to the card.

3. VBIAS biasing supply must be driven at a higher potential than the expected maximum digital input level. For 3.3 volt designs where all digital inputs are 3.3 volt TTL levels, VBIAS may be set to 3.3 volts or greater. For designs with 5.0 volt TTL levels, VBIAS must be set to 5.0 volts.

   PBIAS biasing supplies operate similarly. For designs using optical modules with 3.3 volt PECL levels, the PBIAS pins may be set to 3.3 volts or greater. For designs using optical modules with 5.0 volt PECL levels, the PBIAS pins must be set to 5.0 volts. If the serial interface is not being used, the PBIAS pins may be set to 3.3 volts. See the section on interfacing to ECL and PECL devices for more details

4. Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is the best approach provided care is taken to ensure the IR drop in the resistance does not lower the supply voltage below the recommended operating voltage.

5. High-frequency decoupling capacitors are recommended for each biasing pins (VBIAS, PBIAS and QAVD) as close to the package pin as possible. Separate decoupling is required to prevent the transmitter from coupling noise into the receiver and to prevent power supply transients from coupling into some internal reference circuitry. See the section on Power Supplies for more details.

6. Low-pass filtering networks are recommended for analog power supplies as close to the package pin as possible. Separate decoupling is required to prevent the transmitter from coupling noise into the receiver and to prevent power supply transients from coupling into some internal reference circuitry. See the section on Power Supplies for more details.

7. The high speed serial streams (TXD+/-, RXD+/, and RRCLK+/-) must be routed with 50 ohm controlled impedance circuit board traces and must be terminated with a matched load. Normal TTL-type design rules are not recommended and will reduce the performance of the device. See the section on interfacing to ECL and PECL devices for more details.

8. PECL traces between the S/UNI-622-POS and optical modules should not exceed 4 cm for proper jitter operation.

Please refer to the S/UNI-622-POS reference design (PMC-981070) for further recommendations

13.15 Power Supplies

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to blow these ESD protection devices or trigger latch up. The recommended power supply sequencing follows:

1. The VBIAS supply must be equal to or greater than the VDD supply during power up. By placing a decoupled 1 kohm in series with VBIAS as shown in Figure 34, this restriction may be ignored.

2. The PBIAS supplies must be equal to or greater than the AVD supply during power up. By placing a decoupled 1 kohm in series with the PBIAS supply as shown in Figure 34, this restriction may be ignored.

3. The VDD supply must be applied before or at the same time as QAVD and AVD supplies (the voltage difference between any two pins must be less than 0.5 volts).

4. VDD and VBIAS supplies must be applied before digital input pins are driven or the current per pin limited to less than the maximum DC input current specification.

5. AVD and PBIAS supplies must be applied before analog input pins are driven or the current per pin limited to less than the maximum DC input current specification.

6. The differential voltage between VDD and AVD must be less than 1.0 volts including peak to peak noise.. The differential voltage between VDD and QAVD must be less than 0.5 volts including peak to peak noise. Otherwise, digital noise on VDD will be coupled into the sensitive analog circuitry.

7. Power down the device in the reverse sequence. Use the above current limiting technique for the analog power supplies. Small offsets in VDD / AVD discharge times will not damage the device.

Analog circuitry is particularly susceptible to noise and thus we recommend the following analog power filter scheme shown Figure 34 and Figure 35. Sensitive analog power pins require RC filter networks in order to meet SONET/SDH jitter specifications. Some recommended notes follows:

8. Place each 0.1uF capacitor as close to its associated power pin as possible as shown in Figure 35.

9. The 0.1uF capacitors are ceramic X7R or X5R.

10. The 10uF capacitors are 10V X5R ceramic, 1210 size, from Tayio-Yuden, LMK325BJ106MN (visit their web site at www.t-yuden.com).

11. The 10uF capacitors and resistors do not have to be very close to power pins as they are filtering the power supply and not decoupling it.

12. The two 10uF X5R capacitors on pin C4 can be replaced by one 22uF, 10V, X5R LMK432BJ226MM from Tayio Yuden.

13. All resistors shown are 1/10 watt.

14. All other power pins not mentioned do not need any extra filtering or decoupling.

Please refer to the S/UNI-622-POS reference design (PMC-981070) for further recommendations.

Figure 34: Power Supply Filtering and Decoupling

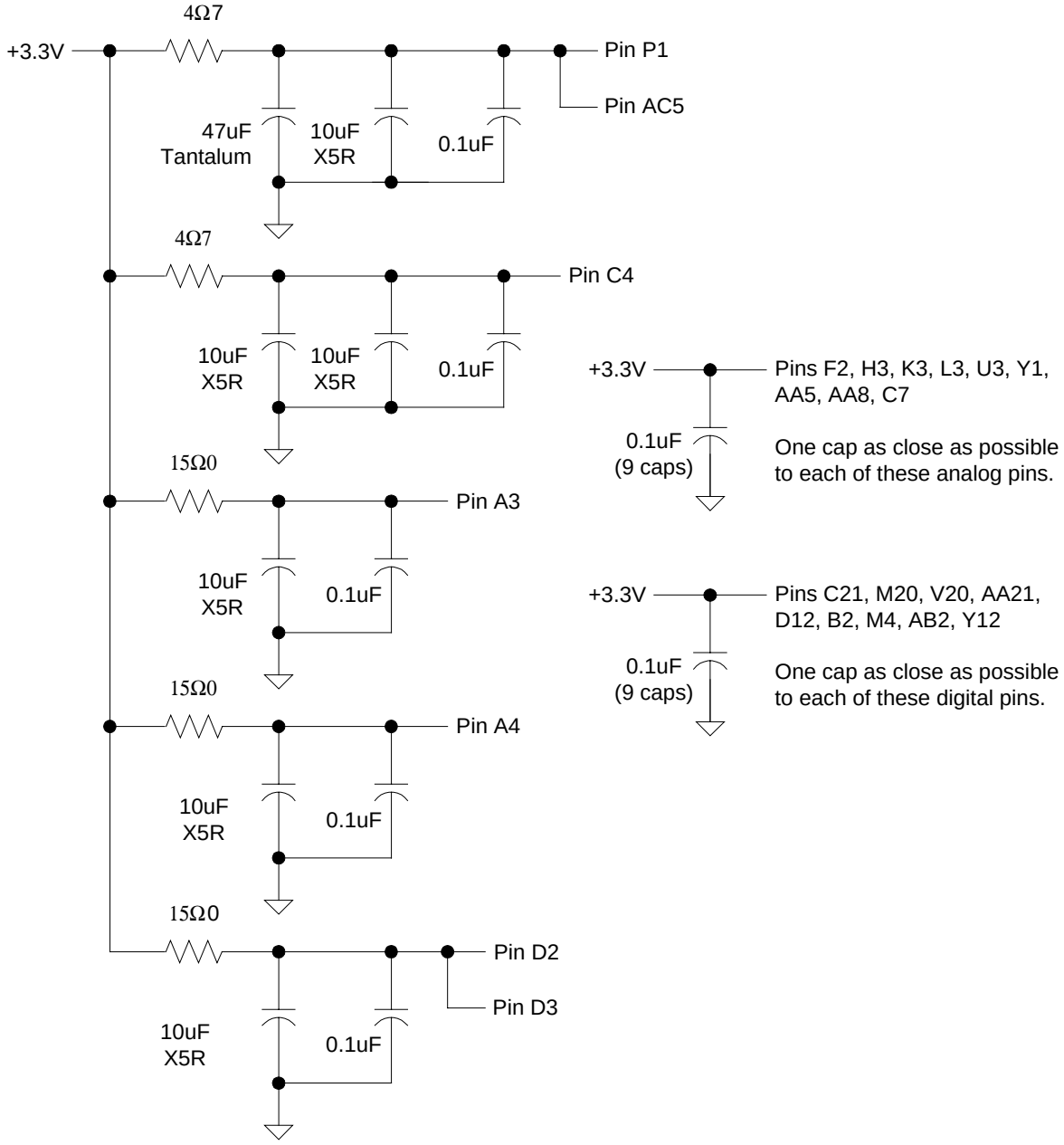
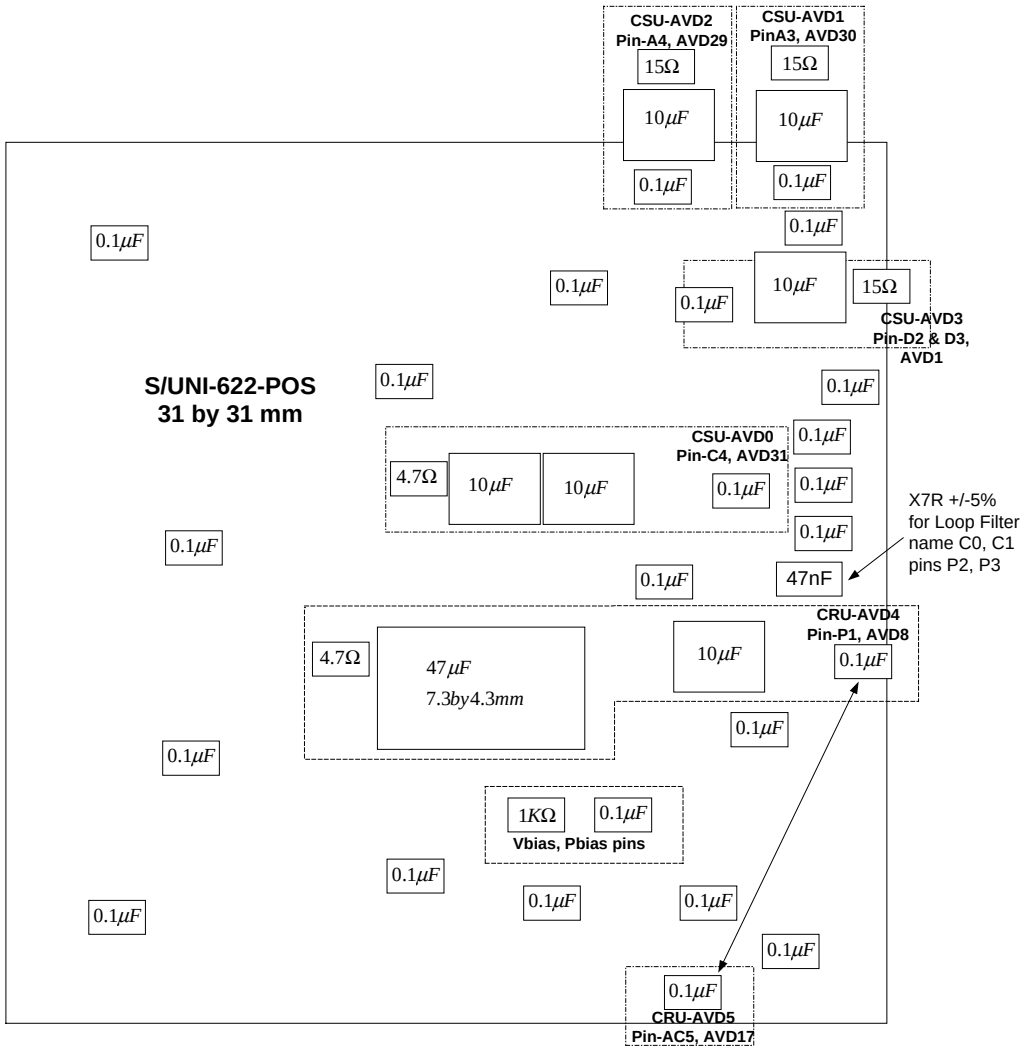


Figure 35: Power Supply Component Layout



13.16 Interfacing to ECL or PECL Devices

In normal operation, the S/UNI-622-POS performs clock and data recovery on the incoming serial stream. As an option, internal clock and data recovery may be bypassed by setting the RBYP pin high and use an externally recovered receive clock on the RRCLK+/- pins. In this mode RXD+/- is sampled on the rising edge of RRCLK+/-. For example, Hewlett Packard provides HFCT/HFBR-5207 optical transceivers with clock and data recovery and HFCT/HFBR-5208 transceivers without clock and data recovery. The HFCT-5207 has a 2x9 pin out having one 9 pin row matching the pin out of the HFCT-5208 and another 9 pin

row which provides extra signals for the recovered clock. By using a footprint that will fit both devices, either device may be used.

Only a few passive components are required to convert the optical transceivers signals to ECL (or PECL) logic levels. Figure 36 and Figure 37 illustrate the recommended configurations for both types of ECL voltage levels. The PECLV pin must be set appropriately for the selected configuration.

Each PECL input and output has an associated ESD biasing pin PBIAS[3:0]. These biasing pins should be biased at the proper level to ensure the internal ESD diode structure is not forward biased. This means for 3.3V volt ECL logic levels (PECLV set high), the PBIAS pins may be biased from 3.3 volts to 5.0 volts. For 5.0 volt ECL logic levels (PECLV set low), the PBIAS pins must be biased at 5.0 volts. The bias pins should be high-frequency decoupled to prevent noise from coupling through the ESD structures and affecting the high-speed signals.

The 50 ohm control impedance traces must be less than 4 cm in length to reduce the effect of signal reflections between the optical module and the S/UNI-622-POS. Vias should be avoided on the signal path between the optical module and the S/UNI-622-POS as they can affect the jitter performance of the interface. Vias may be used for the termination networks as the inductive effective of a via will not significantly affect the termination performance.

Figure 36: Interfacing S/UNI-622-POS PECL Pins to 3.3V Devices

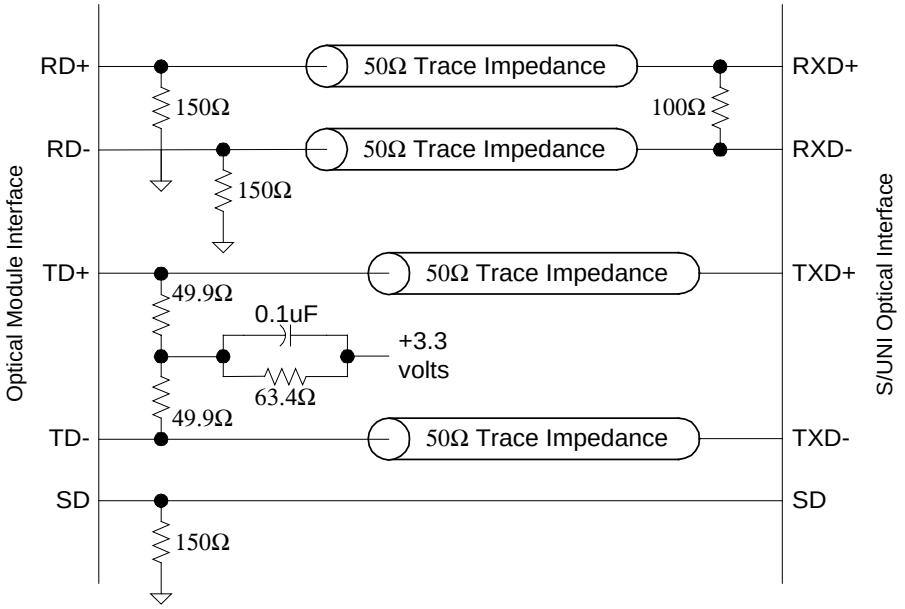
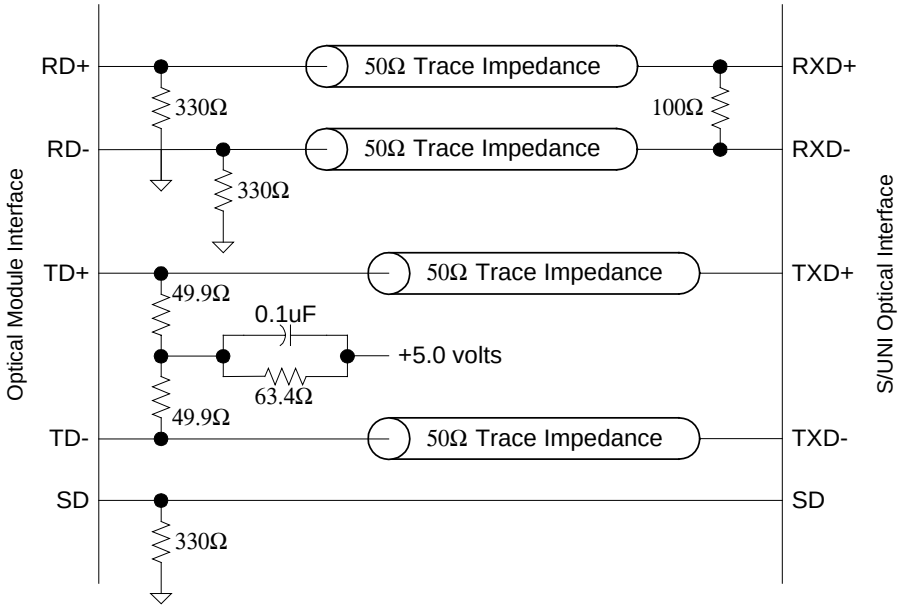


Figure 37: Interfacing S/UNI-622-POS PECL Pins to 5.0V Devices



When a PECL input is not being used, the positive differential input must be tied to analog power (AVD) and the negative differential input must be tied to analog ground (AVS). In all cases, the PECL inputs must be driven with a differential voltage (do not connect both pins to AVD or AVS).

When the PECL output is not being used, the external reference resistor TDREF1 may be tied to analog power (AVD) and TDREF0 may be tied to analog group (AVS) to disable the PECL output. Both positive and negative differential outputs of the PECL output may be tied both to analog ground (AVS).

Please refer to the S/UNI-622-POS reference design (PMC-981070) for further recommendations.

13.17 Clock Synthesis and Recovery

The Clock Synthesizer unit (CSU) in the S/UNI-622-POS requires an external reference clock REFCLK to generate the 622 MHz transmit clock. The REFCLK input is a PECL input in order to reduce the amount of noise coupled into the CSU. In most cases, the reference clock must be generated and propagated using PECL logic in order for the CSU to meet SONET/SDH intrinsic jitter specifications.

In general, the reference clock REFCLK is supplied by a crystal oscillator with PECL outputs. The oscillator must have at least -115dBc/√Hz between 12 kHz and 5 MHz frequency offset in order for the CSU to meet SONET/SDH intrinsic jitter specifications. Do not use a TTL type crystal oscillator with a TTL to PECL converter as the TTL signal conversion will generate significant jitter on the reference clock.

The Clock Recovery unit (CRU) in the S/UNI-622-POS requires an external capacitor between the C0 and C1 pins to control the amount of "peaking" in the jitter transfer curve. The capacitor should be located as close as possible to the C0 and C1 pins in order to prevent noise from coupling into CRU.

When the CRU is used in WAN mode (RTYPE bit in register 0x5E is set high), a 47nF non-polarized capacitor (ceramic ± 5% X7R or equivalent) must be connected between the C0 and C1 pins. The capacitor controls the amount of "peaking" in the jitter transfer response. It must be non-polarized as the capacitor may operate with a D.C. reverse-bias depending on process, voltage and temperature extremes. When the CRU is used in LAN mode (RTYPE bit in register 0x5E is set low), the C0 and C1 pins must be left floating.

Please refer to the S/UNI-622-POS reference design (PMC-981070) for further recommendations.

13.18 System Interface DLL Operation

The S/UNI-622-POS use digital delay lock loop (DLL) units to improve the output propagation timing on certain digital output pins. The TFCLK, RFCLK and PTCLK clock inputs each have a DLL to improve the timing on their associated interfaces.

The DLL compensate for internal timing and output pad delays by adaptively delaying the input clock signal by approximately one clock period (1 UI) to create a new clock which controls the internal device logic. A side effect is that the DLL units imposes a minimum clock rate on each of the clock signals. For certain operation modes, such as 19.44MHz OC3 clocking on PTCLK, the DLL is bypassed.

When the S/UNI-622-POS is reset, the DLL units find the initial delay lock. This process may take up to 3100 clock cycles to identify the lock position. During this intial lock period, device interface timing will not meet the timing specifications listed in A.C. Timing section. The TCA/TPA pin is held low when the TFCLK DLL is finding lock. If the clock inputs are not stable during this period (for instance, a clock is generated using an external PLL), the S/UNI-622-POS

should be held in reset until the clocks are stable or the DLL should be reset using software control.

The RFCLK, TFCLK and PTCLK DLL software resets are performed by writing 0x00 to registers 0x96, 0x9A and 0x9E respectively. When resetting the RFCLK or TFCLK DLL units, the associated FIFOs in the RXCP, RXFP, TXCP and RXCP must also be reset using the their FIFORST register bits. The RUN register bit is set high when the DLL finds lock after a system or software reset.

The DLL units are sensitive to jitter on the clock inputs. The reason is that the DLL must track the changes in clock edges cause by changes in clock frequency, temperature, voltage and jitter. While the DLL may tolerate up to 0.4UIpp of clock jitter without losing phase lock, the output timing may degrade with excessive input jitter. Therefore, the high frequency clock jitter (above 1 MHz) should be less than value specified by the A.C. Timing section.

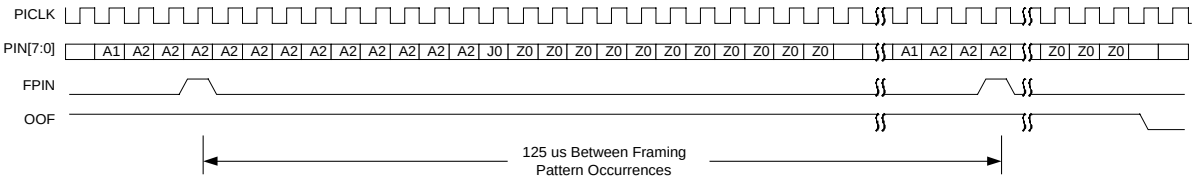
14 FUNCTIONAL TIMING

All functional timing diagrams assume that polarity control is not being applied to input and output data and clock lines (i.e. polarity control bits in the S/UNI-622-POS registers are set to their default states).

14.1 Parallel Line Interface

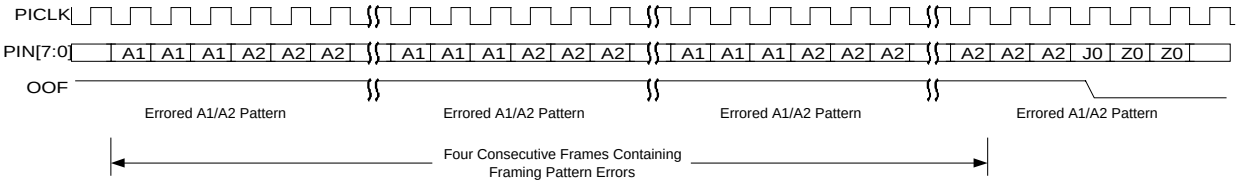
The In Frame Declaration Timing diagram (Figure 38) illustrates the declaration of the in-frame state by the SUNI-622-POS when processing a 77.76 Mbyte/s STS-12c/STM-4-4c stream on PIN[7:0]. An upstream serial-to-parallel converter indicates the location of the SONET/SDH frame using the FPIN input. The frame verification is initialized by a pulse on FPIN when the SUNI-622-POS is out of frame. The in-frame state is declared if the framing pattern is observed in the correct byte positions in the following frame, and in the intervening period (125 us) no additional pulse were present of FPIN. The SUNI-622-POS ignores pulses of FPIN while in frame. The algorithm results in a maximum average reframe time of 250 us in the absence of mimic framing patterns.

Figure 38: In Frame Declaration Timing



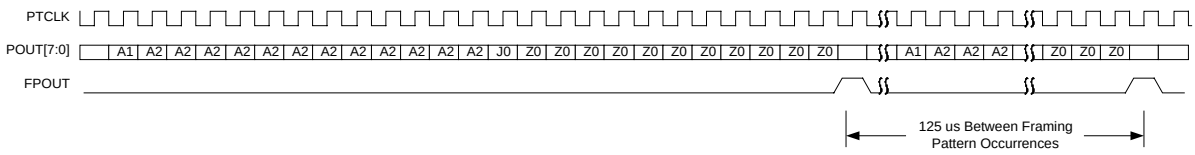
The Out of Frame Declaration Timing diagram (Figure 39) illustrates the declaration of out of frame for a STS-12c stream. The framing pattern is a 196-bit pattern that repeats once per frame. For the purposes of OOF declaration, the framing pattern may be modified using the ALGO2 bit in the RSOP Control register. Out of frame is declared when one or more errors are detected in this pattern for four consecutive frames as illustrated. In the presence of random data, out of frame will normally be declared within 500 us.

Figure 39: Out of Frame Declaration Timing



The Parallel Transmit Timing diagram (Figure 40) illustrates the S/UNI-622-POS transmit STS-12c data stream on the parallel interface. The FPOUT signal marks the SONET/SDH frame alignment on the POUT[7:0] bus. FPOUT pulses high during the first synchronous payload envelope byte after the J0/Z0 bytes.

Figure 40: Parallel Transmit Interface Timing



14.2 ATM UTOPIA Level 2 System Interface

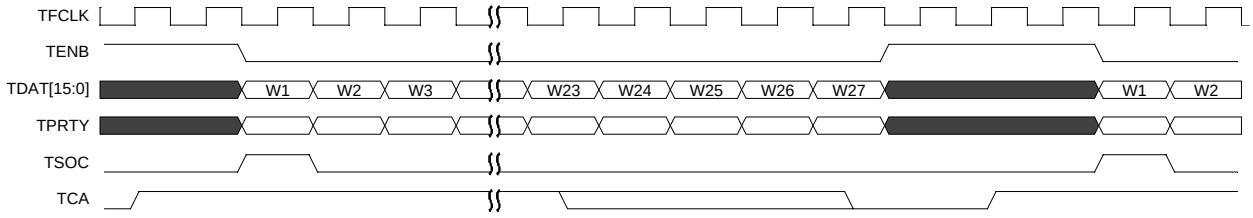
The ATM UTOPIA Level 2 System Interface is compatible with the UTOPIA Level 2 specification (see References). The S/UNI-622-POS only supports the 16-bit mode of operation.

The Transmit UTOPIA Level 2 System Interface Timing diagram (Figure 41) illustrates the operation of the system side transmit FIFO interface. Assertion of the transmit cell available output, TCA, indicates that there is space available in the transmit FIFO for at least one ATM cell structure. Deassertion of TCA occurs when the FIFO is filled with the number of ATM cells indicated by the register bits FIFODP[1:0]. If the TCA is configured to deassert early before the FIFO is truly full, the FIFO will accept additional cells even if TCA is inactive. At any time, if the upstream does not have a word to write, it must deassert TENB.

As well, the TCA may be configured to deassert after the last word of a cell is written into the FIFO (FIFO is full) or as the cell is being written into the FIFO (FIFO is near full). In addition, the register bit TCAINV can be used to invert the polarity of TCA.

TSOC must be high during the first word of the ATM cell structure and must be present for the start of each cell. When TSOC is asserted and the previous word transfer was not the end of an ATM cell structure, the system interface realigns itself to the new timing, and the previous partially transferred cell is dropped.

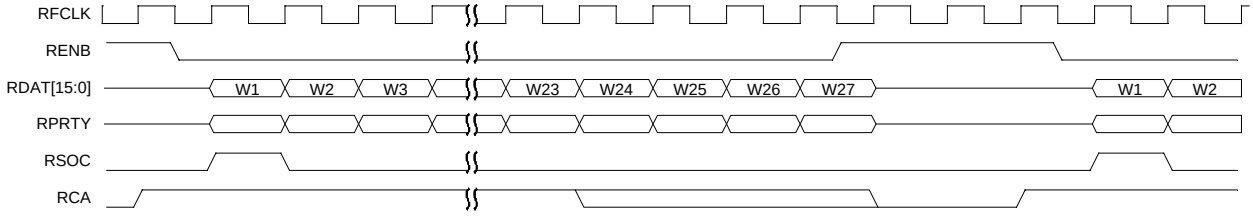
Figure 41: Transmit UTOPIA Level 2 System Interface Timing



The Receive UTOPIA Level 2 System Interface Timing diagram (Figure 42) illustrates the operation of the system side receive interface. The RXCP indicates that a cell is available by asserting the receive cell available output RCA. RCA remains high until the receive FIFO is empty. After RCA is deasserted, it remains low for a minimum of one RFCLK clock cycle and can then reassert to indicate that there are additional cells available in the FIFO.

At any time, the downstream reader can throttle back the reception of words by deasserting RENB. The RDAT[15:0], RPRTY and RSOC signals tri-state when RENB is sampled deasserted. RSOC is high during the first word of the cell and is present for each cell.

Figure 42: Receive UTOPIA Level 2 System Interface Timing



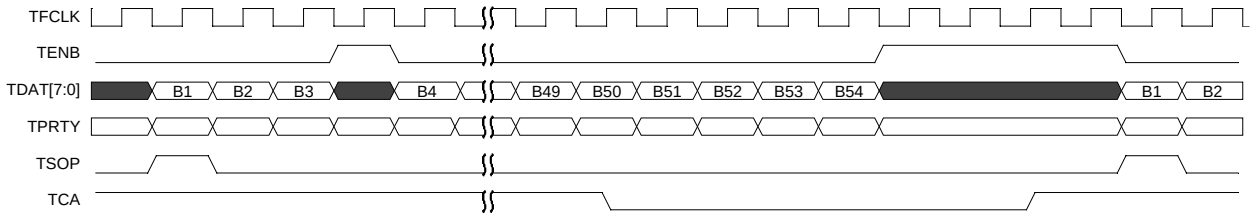
14.3 ATM UTOPIA Level 3 System Interface

The ATM UTOPIA Level 3 System Interface is compatible with the UTOPIA Level 3 specification (see References). The S/UNI-622-POS only supports the 8-bit mode of operation.

The Transmit UTOPIA Level 3 System Interface Timing diagram (Figure 43) illustrates the operation of the system side transmit FIFO interface. Assertion of the transmit cell available output, TCA, indicates that there is space available in the transmit FIFO for at least one ATM cell structure. Deassertion of TCA occurs when the FIFO is filled with the number of ATM cells indicated by the register bits FIFODP[1:0]. If the TCA is configured to deassert early before the FIFO is truly full, the FIFO will accept additional cells even if TCA is inactive. At any time, if the upstream does not have a byte to write, it must deassert TENB. When TCA desserts, it will do so within 4 clocks cycles before the last byte of the cell.

TSOC must be high during the first byte of the ATM cell structure and must be present for the start of each cell. Thus, TSOC will mark the H1 byte. When TSOC is asserted and the previous byte transferred was not the end of an ATM cell structure, the system interface realigns itself to the new timing, and the previous partially transferred cell is dropped.

Figure 43: Transmit UTOPIA Level 3 System Interface Timing

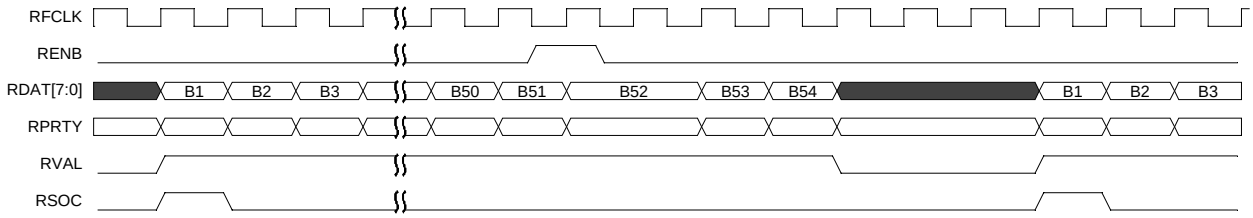


The Receive UTOPIA Level 3 System Interface Timing diagram (Figure 44) illustrates the operation of the system side receive interface. Unlike traditional UTOPIA interfaces, the SUNI-622-POS controls the bus. Because the bus is point to point, the SUNI-622-POS pushes received data to the downstream reader. As well, the control of RENB is pipelined to improve the speed of the interface.

When a cell is available, the RVAL signal is asserted and the first byte of the cell appears on the RDAT[7:0] bus when RENB is low. The first byte of the structure is marked with RSOC being set high. Thus, RSOC will identify the H1 byte. The downstream reader may control the flow of data using RENB. If RENB is sampled low on the rising edge of RFCLK, the data on RDAT[7:0], RVAL and RSOC signals will be updated on the next rising edge of RFCLK. When RENB is sampled high on the rising edge of RFCLK, the data on RDAT[7:0], RVAL and RSOC will not change on the next rising edge of RFCLK. RENB must be low for at least 3 RFCLK clock cycles before RVAL will assert for the first byte of the first ATM cell.

After the end of a cell, the SUNI-622-POS will keep the RVAL signal high and mark the first byte of the next cell with RSOC asserted if the receive FIFO contained more than one cell.

Figure 44: Receive UTOPIA Level 3 System Interface Timing



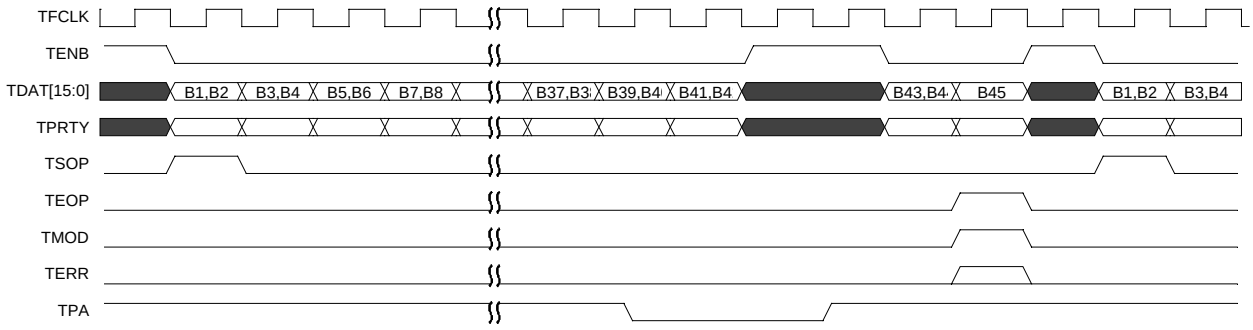
14.4 Packet over SONET/SDH (POS) Level 2 System Interface

The Packet over SONET/SDH (POS) System Interface is compatible with the POS-PHY Level 2 specification (see References). The S/UNI-622-POS supports the byte level and packet level transfer modes of POS-PHY.

The Transmit POS Level 2 System Interface Timing diagram (Figure 45) illustrates the operation of the system side transmit FIFO interface. Assertion of the transmit packet available output, TPA, indicates that there is space available in the transmit FIFO. Deassertion of TPA occurs when the FIFO is filled to the depth indicated by the register TPAHWM[7:0]. The exact octet that triggers the deassertion of TPA depends on the particular timing relationship between the internal SONET/SDH clock and TFCLK, and for that reason is not precise. However the TXFP is always conservative. Thus, when TPA deasserts with no more than TPAHWM[7:0] bytes in the FIFO remains. If TPA is asserted and the upstream is ready to write a byte, the upstream device should assert TENB. At any time, if the upstream does not have a word to write, it must deassert TENB. In addition, the register bit TPAINV can be used to invert the meaning of TPA.

TSOP must be high during the first word of the packet and must be present for the start of each packet. TEOP must be high during the last packet word/byte transferred. During a packet transfer, every word must be composed of two bytes and TMOD shall be low. TMOD is used to during the last word of the packet transfer to determine if the word is composed of one or two bytes. It is legal to assert TSOP and TEOP at the same time. This case occurs when a 1-byte or a 2-byte packet is transferred. When TSOP is asserted and the previous word transfer was not marked with TEOP, the system interface realigns itself to the new timing, and the previous packet is aborted.

Figure 45: Transmit POS Level 2 System Interface Timing



The Receive POS Level 2 System Interface Timing diagram (Figure 46) illustrates the operation of the system side receive interface. The RXFP indicates that a packet is available by asserting the receive packet available output RPA. RPA remains high until the receive FIFO is empty. After RPA is deasserted, it remains low for a minimum of one RFCLK clock cycle and then can assert to indicate that there are additional packets available in the FIFO. At any time, the downstream reader can throttle back the reception of words by deasserting RENB.

RSOP is high during the first word of the packet. REOP is high during the last packet word. During a packet transfer every word is composed of two bytes. RMOD is used during the last word of the packet transfer to determine if the last word is composed of one or two bytes. It is legal to assert RSOP and REOP at the same time. This case occurs when a 1-byte or a 2-byte packet is transferred. Packets that were subject to an error (aborted, length violation, FIFO overrun, etc) will be marked by RERR high during the last word transfer.

When a packet with less than 6 bytes arrives (from the line side), the receive packet available signal (RPA) may assert before data is available. In this condition, RPA will assert between 1 to 3 RFCLK clock cycles before the data is available and will remain asserted for 1 to 3 RFCLK clock cycles. When the Link Layer device attempts to read the packet by asserting read enable (RENB), it may find that there is no valid data available (receive data valid signal (RVAL) remains de-asserted). RPA will correctly assert again later when data is available. At this time the RVAL signal will be asserted indicating valid data.

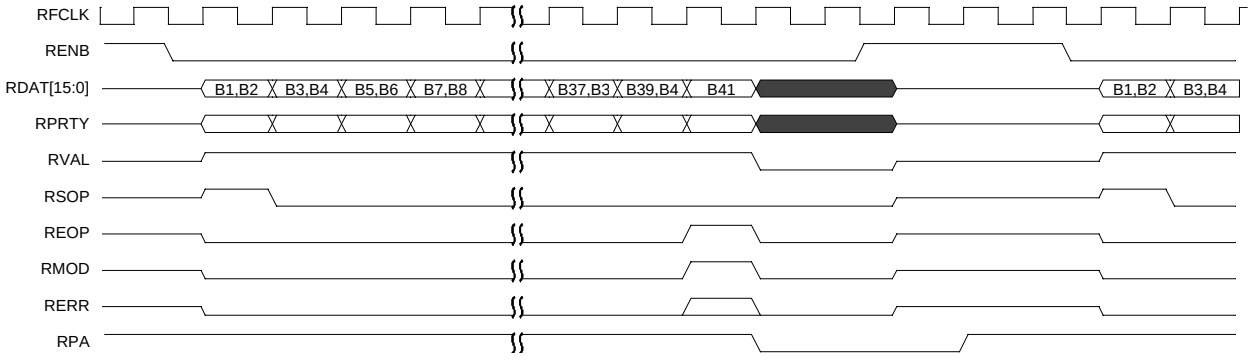
With packets greater than 6 bytes, the RPA signal will assert, de-assert and then reassert 1 to 3 RFCLK cycles later (same as the above case with packets less than 6 bytes). However, if the Link layer device attempts to read the packet on

the basis of the first occurrence of RPA, it will read valid data (RVAL will be asserted), even if RPA may be de-asserted.

This early assertion of RPA will not cause any data corruption if RVAL is used to qualify the data that is read. It is recommended that RVAL always be used to qualify receive data. The operation of RPA may cause a slight reduction bandwidth on receive side of the POS-PHY interface. However, since there is ample bandwidth on the POS-PHY interface there will be no impact on performance of functionality.

During the transfer of a packet, valid data is marked by RVAL high. If the FIFO under-runs, or if REOP is encountered, the RXFP will de-assert RVAL to halt the transfer, and the link layer device must deassert RENB. A new transfer may then be started by asserting RENB when RPA indicates that more packet data is available.

Figure 46: Receive POS Level 2 System Interface Timing



The receive POS-PHY Level 2 interface cannot support full bandwidth with arbitrarily small consecutive packets. In general, the minimum consecutive packet size the interface can transfer without overruning the receive FIFO in the TXFP is a function of how quickly the downstream logic reselects the S/UNI-622-POS after an end of packet is transferred on the bus. If the number of cycles between packet transfers (that is, the number of RFCLK cycles between RVAL going low, RENB deasserting and then reasserting) is keep small, the minimum full-bandwidth packet size can be as low as 15 to 20 bytes.

14.5 Packet over SONET/SDH (POS) Level 3 System Interface

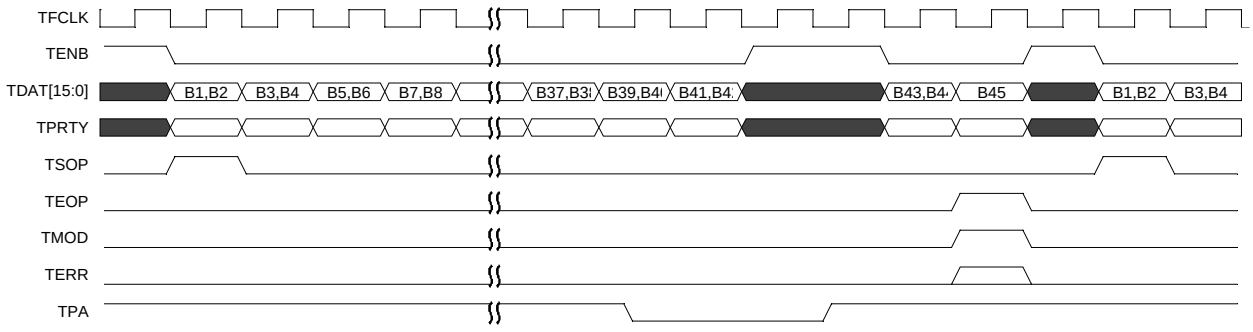
The Packet over SONET/SDH (POS) Level 3 System Interface is compatible with the POS-PHY Level 3 specification (see References). The S/UNI-622-POS only supports the 8-bit mode of operation.

The Transmit POS Level 3 System Interface Timing diagram (Figure 47) illustrates the operation of the system side transmit FIFO interface. Assertion of the transmit packet available output, TPA, indicates that there is space available in the transmit FIFO. Deassertion of TPA occurs when the FIFO is filled to the depth indicated by the register TPAHWM[7:0]. The exact octet that triggers the deassertion of TPA depends on the particular timing relationship between the internal SONET/SDH clock and TFCLK, and for that reason is not precise. However the TXFP is always conservative. Thus, when TPA deasserts with no more than TPAHWM[7:0] bytes in the FIFO remains. If TPA is asserted and the upstream is ready to write a byte, the upstream device should assert TENB. At any time, if the upstream does not have a byte to write, it must deassert TENB. In addition, the register bit TPAINV can be used to invert the meaning of TPA.

TSOP must be high during the first byte of each packet. TEOP must be high during the last byte of the packet. It is legal to assert TSOP and TEOP at the same time. This case occurs when a one byte packet is transferred. When TSOP is asserted and the previous byte transfer was not marked with TEOP, the system interface realigns itself to the new timing, and the previous packet is marked to be aborted.

When a packet with an odd number of bytes is transferred, the TENB signal must be deasserted for at least one clock cycle after TEOP is asserted (last byte of the packet is written into the FIFO). Transferring back-to-back packets (without deasserting TENB between the TEOP and TSOP) with odd number of bytes will cause the system interface to malfunction.

Figure 47: Transmit POS Level 3 System Interface Timing



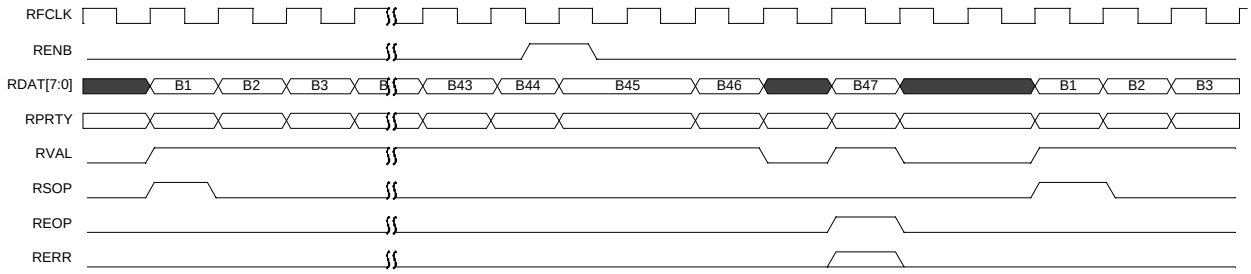
The Receive POS Level 3 System Interface Timing diagram (Figure 48) illustrates the operation of the system side receive interface. Unlike POS Level 2 interfaces, the SUNI-622-POS controls the bus. Because the bus is point to

point, the SUNI-622-POS pushes received data to the downstream reader. As well, the control of RENB is pipelined to improve the speed of the interface.

When a cell is available, the RVAL signal is asserted and the first byte of the packet appears on the RDAT[7:0] bus when RENB is low. Thus, the RSOP signal marks the first byte of the packet. The downstream reader may control the flow of data using RENB. If RENB is sampled low on the rising edge of RFCLK, the data on RDAT[7:0], RVAL and RSOP signals will be updated on the next rising edge of RFCLK. When RENB is sampled high on the rising edge of RFCLK, the data on RDAT[7:0], RVAL and RSOP will not change on the next rising edge of RFCLK. RENB must be low for at least 3 RFCLK clock cycles before RVAL will assert for the first byte of the first packet.

At the end of a packet, the SUNI-622-POS will keep the RVAL signal high and mark the first byte of the next packet if the receive FIFO contained more than one packet. It is legal to assert RSOP and REOP during the first byte of the packet to transfer a 1-byte packet. Packets that were subject to an error (aborted, length violation, FIFO overrun, etc) will be marked by RERR set high during the last byte of the transfer (when REOP is set high).

Figure 48: Receive POS Level 3 System Interface Timing



The receive POS-PHY Level 3 interface cannot support full bandwidth with arbitrarily small consecutive packets. The Level 3 interface relies on an internal Level 2 interface which restricts the bandwidth on the Level 3 interface. In general, the Level 3 interface can support 15 byte packets consecutively full-bandwidth without the FIFO in the TXFP overruning.

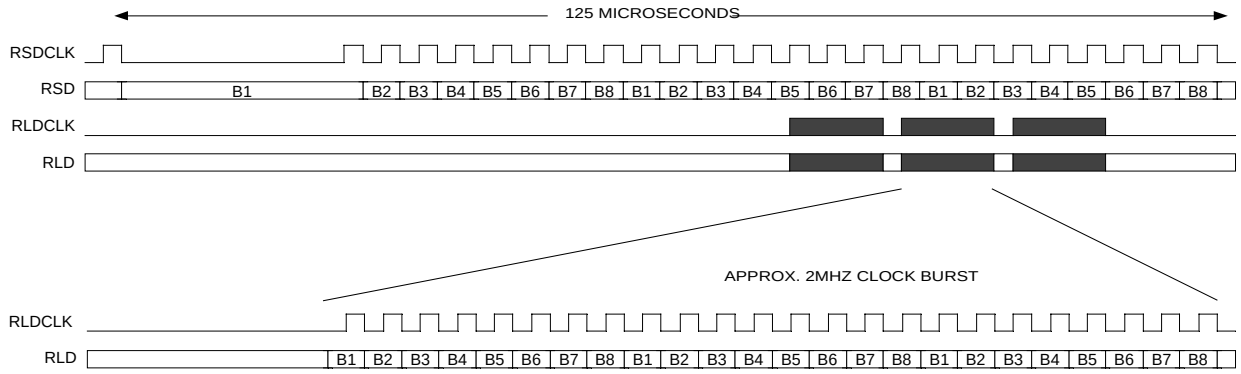
14.6 Section and Line Data Communication Channels

The SUNI-622-POS provides access to both Line and Section Data Communications Channels (DCC). Both channels are accessed using the serial

interface pins RSD, RLD, TSD and TLD and their clocks RSDCLK, RLDCLK, TSDCLK and TLDCLK respectively.

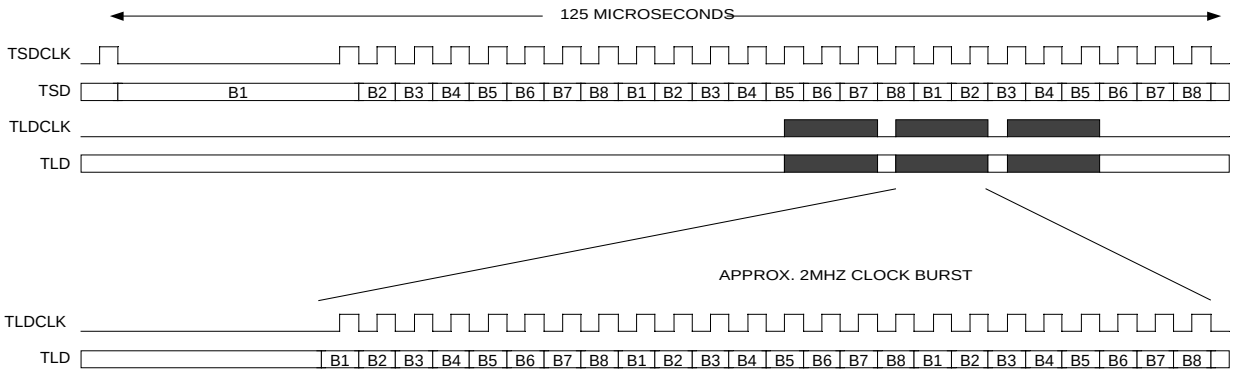
The Transport Overhead Data Link Clock and Data Extraction Timing diagram (Figure 49) shows the relationship between the RSD and RLD serial data outputs and their associated clocks, RSDCLK and RLDCLK. RSDCLK is a 216 kHz, 50% duty cycle clock that is gapped to produce a 192 kHz nominal rate. RLDCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock that is gapped to produce a 576 kHz nominal rate. RSD is updated on the falling edge of RSDCLK. RLD is updated on the falling edge of RLDCLK. The D1-D3, and D4-D12 bytes shifted out of the S/UNI-622-POS in the frame shown are extracted from the corresponding transport overhead channels in the previous frame.

Figure 49: Transport Overhead Data Link Clock and Data Extraction



The Transport Overhead Data Link Clock and Data Insertion diagram (Figure 50) shows the relationship between the TSD and TLD serial data inputs, and their associated clock TSDCLK and TLDCLK respectively. TSDCLK is a 216 kHz, 50% duty cycle clock that is gapped to produce a 192 kHz nominal rate. TLDCLK is a 2.16 MHz, 67%(high)/33%(low) duty cycle clock that is gapped to produce a 576 kHz nominal rate. TSD is sampled on the rising edge of TSDCLK. TLD is sampled on the rising edge of TLDCLK. The D1-D3, and D4-D12 bytes shifted in to the S/UNI-622-POS in the frame shown are inserted in the corresponding transport overhead channels in the next frame.

Figure 50: Transport Overhead Data Link Clock and Data Insertion



15 ABSOLUTE MAXIMUM RATINGS

Maximum rating are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 18: Absolute Maximum Ratings

Ambient Temperature under Bias	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Supply Voltage	-0.3V to +4.6V
Bias Voltage (V_{BIAS})	(V_{DD} - .3) to +5.5V
Voltage on PECL Pin	-0.3V to V_{PBIAS}+0.3V
Voltage on 3.3V Tolerant Digital Pin	-0.3V to V_{VDD}+0.3V
Voltage on 5.0V Tolerant Digital Pin	-0.3V to V_{VBIAS}+0.3V
Static Discharge Voltage	±1000 V
Latch-Up Current per Pin	±100 mA
DC Input Current	±20 mA
Lead Temperature	+230°C
Absolute Maximum Junction Temperature	+150°C

16 D.C. CHARACTERISTICS

T_A = -40°C to +85°C, V_{DD} = 3.3V ± 10%, V_{AVD} = 3.3V ± 5%, V_{DD} < V_{VBIAS} < 5.5V

(Typical Conditions: T_A = 25°C, V_{DD} = 3.3V, V_{AVD} = 3.3V, V_{BIAS} = 5V)

Table 19: D.C Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Power Supply	2.97	3.3	3.63	Volts	
BIAS	5V Tolerant Bias	VDD	5.0	5.5	Volts	
V_{IL}	Input Low Voltage	0	1.2	0.8	Volts	Guaranteed Input Low voltage.
V_{IH}	Input High Voltage	2.0	1.2		Volts	Guaranteed Input High voltage.
V_{OL}	Output or Bi-directional Low Voltage		0.2	0.4	Volts	Guaranteed output Low voltage at VDD=2.97V and I_{OL}=maximum rated for pad.
V_{OH}	Output or Bi-directional High Voltage	2.4	2.6		Volts	Guaranteed output High voltage at VDD=2.97V and I_{OH}=maximum rated current for pad.
V_{T+}	Reset Input High Voltage	2.0			Volts	Applies to RSTB and TRSTB only.
V_{T-}	Reset Input Low Voltage			0.8	Volts	Applies to RSTB and TRSTB only.
V_{TH}	Reset Input Hysteresis Voltage		0.3		Volts	Applies to RSTB and TRSTB only.
V_{PECLI+}	Input PECL High Voltage	V_{PECL} - 1.165	V_{PECL} - 0.955	V_{PECL} -0.880	Volts	V_{PECL} = 5.0V or 3.3V See note 4.
V_{PECLI-}	Input PECL Low Voltage	V_{PECL} - 1.810	V_{PECL} - 1.700	V_{PECL} - 1.470	Volts	V_{PECL} = 5.0V or 3.3V See note 4.
V_{PECLIC}	Input PECL Common Mode Voltage	V_{PECL} - 1.490	V_{PECL} - 1.329	V_{PECL} - 1.180	Volts	V_{PECL} = 5.0V or 3.3V See note 4.

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{PECLO+}	Output PECL High Voltage	V_{PECL} - 0.880	V_{PECL} - 0.955	V_{PECL} - 1.025	Volts	V_{PECL} = 5.0V or 3.3V
V_{PCLO5-}	Output PECL Low Voltage	V_{PECL} - 1.620	V_{PECL} - 1.705	V_{PECL} - 1.810	Volts	V_{PECL} = 5.0V or 3.3V
I_{ILPU}	Input Low Current	-100	-50	-4	µA	V_{IL} = GND. Notes 1 and 3.
I_{IHPU}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$. Notes 1 and 3.
I_{IL}	Input Low Current	-10	0	+10	µA	V_{IL} = GND. Notes 2 and 3.
I_{IH}	Input High Current	-10	0	+10	µA	$V_{IH} = V_{DD}$. Notes 2 and 3.
C_{IN}	Input Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{OUT}	Output Capacitance		5		pF	t_A=25°C, f = 1 MHz
C_{IO}	Bi-directional Capacitance		5		pF	t_A=25°C, f = 1 MHz
I_{DDOP1}	ATM Operation with CRU and CSU.		490	580	mA	V_{DD} = 3.63V, Outputs Unloaded
I_{DDOP2}	ATM Operation with CSU, CRU bypassed		440	550	mA	V_{DD} = 3.63V, Outputs Unloaded
I_{DDOP3}	ATM Operation with Parallel Line Interface (STS-12c/STM-4-4c)		402	510	mA	V_{DD} = 3.63V, Outputs Unloaded
I_{DDOP4}	POS Operation with CRU and CSU		530	620	mA	V_{DD} = 3.63V, Outputs Unloaded
I_{DDOP5}	POS Operation with CSU, CRU bypassed.		490	600	mA	V_{DD} = 3.63V, Outputs Unloaded
I_{DDOP6}	POS Operation with Parallel Line Interface (STS-12c/STM-4-4c)		440	550	mA	V_{DD} = 3.63V, Outputs Unloaded

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.

2. Input pin or bi-directional pin without internal pull-up resistor

3. Negative currents flow into the device (sinking); positive currents flow out of the device (sourcing).

4. The PECL inputs derive the common mode voltage from the differential signal pair. Differential input swings must be between 310mV and 1000mV for proper error-free operation. Specified maximum and minimun PECL input levels must be respected during normal operation.

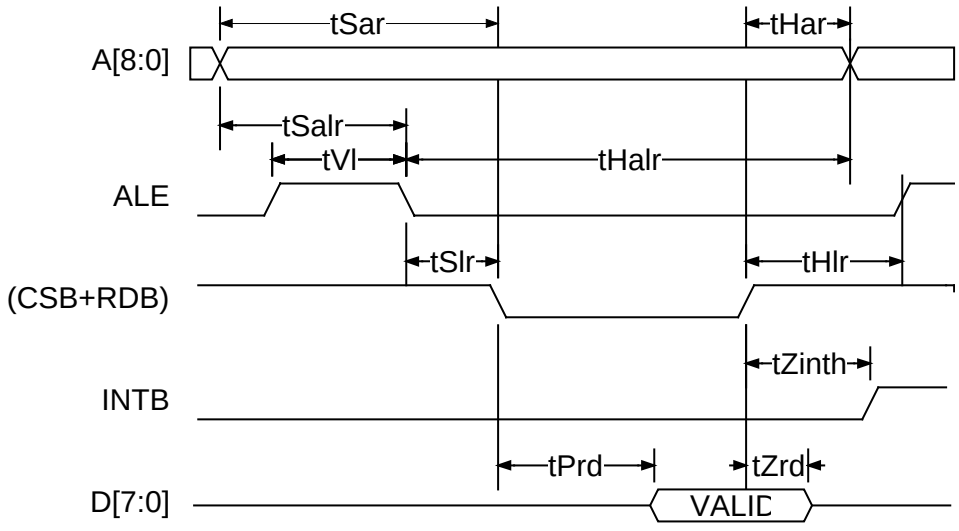
17 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

(T_A = -40°C to +85°C, V_{DD} = 3.3V ± 10%, V_{AVD} = 3.3V ± 5%)

Table 20: Microprocessor Interface Read Access (Figure 51)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	5		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		70	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to INTB High		50	ns

Figure 51: Microprocessor Interface Read Timing



Notes on Microprocessor Interface Read Timing:

15. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

16. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).

17. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.

18. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALR}, tH_{ALR}, tV_L, tS_{LR}, and tH_{LR} are not applicable.

19. Parameter tH_{AR} is not applicable if address latching is used.

20. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

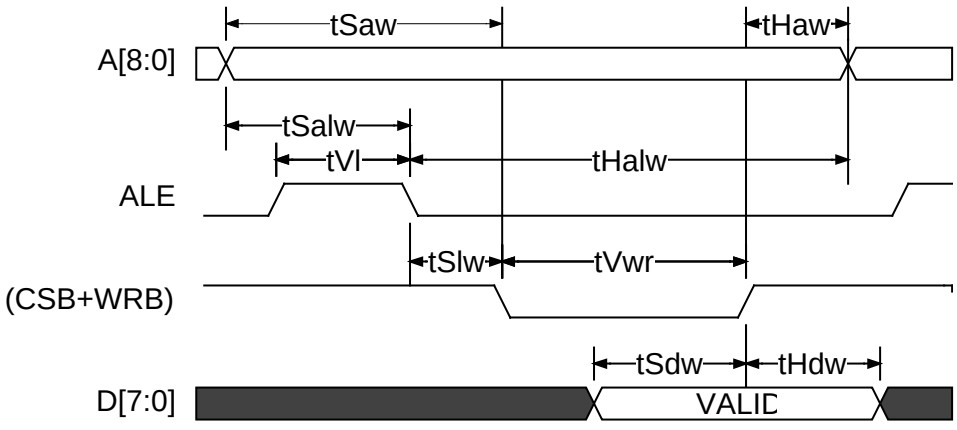
21. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

22. Output tri-state delay is the time in nanoseconds from the 1.4 Volt of the reference signal to the point where the total current delivered through the output is less than or equal to the leakage current.

Table 21: Microprocessor Interface Write Access (Figure 52)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	5		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 52: Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1 A valid write cycle is defined as a logical OR of the CSB and the WRB signals.

2 In non-multiplexed address/data bus architectures, ALE should be held high so parameters tS_{ALW}, tH_{ALW}, tV_L, tS_{LW}, and tH_{LW} are not applicable.

3 Parameter tH_{AW} is not applicable if address latching is used.

4 When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

5 When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

18 A.C. TIMING CHARACTERISTICS

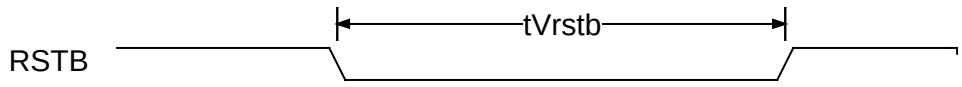
(T_A = -40°C to +85°C, V_{DD} = 3.3V ± 10%, V_{AVD} = 3.3V ± 5%)

18.1 System Reset Timing

Table 22: RSTB Timing (Figure 53)

Symbol	Description	Min	Max	Units
tV_{RSTB}	RSTB Pulse Width	100		ns

Figure 53: RSTB Timing Diagram



18.2 Parallel Line Interface Timing

Table 23: Transmit Parallel Line Interface Timing (Figure 54)

Symbol	Description	Min	Max	Units
f_{PTCLK}	STS12c PTCLK Frequency	60	77.76	MHz
D_{PTCLK}	STS12c PTCLK Duty Cycle	40	60	%
J_{PTCLK}	STS12c PTCLK Peak to Peak Jitter (>1 MHz)		1	ns
tP_{POUT}	STS12c PTCLK High to POUT[7:0] Valid	1	7	ns
tP_{FPOUT}	STS12c PTCLK High to FPOUT Valid	1	7	ns
f_{PTCLK}	STS3c PTCLK Frequency		19.44	MHz
D_{PTCLK}	STS3c PTCLK Duty Cycle	40	60	%
tP_{POUT}	STS3c PTCLK High to POUT[7:0] Valid	1	20	ns
tP_{FPOUT}	STS3c PTCLK High to FPOUT Valid	1	20	ns

Figure 54: Transmit Parallel Line Interface Timing Diagram

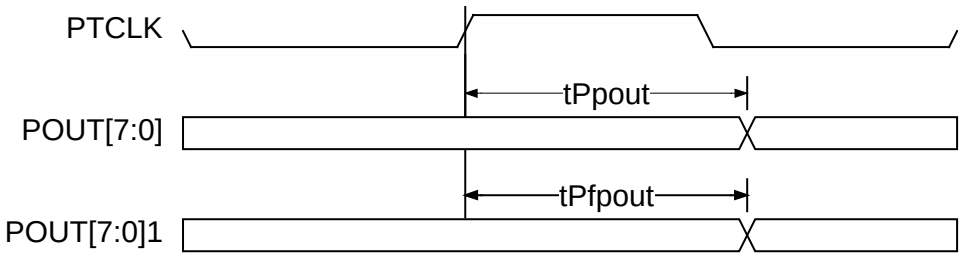
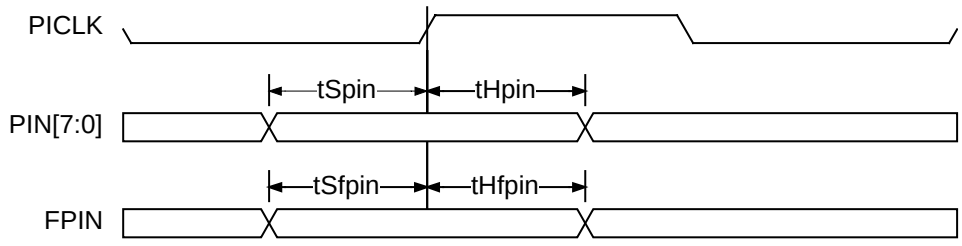


Table 24: Receive Parallel Line Interface Timing (Figure 55)

Symbol	Description	Min	Max	Units
f_{PICLK}	STS-12c PICLK Frequency		77.76	MHz
D_{PICLK}	STS-12c PICLK Duty Cycle	40	60	%
tS_{PIN}	STS-12c PIN[7:0] Set-up time to TFCLK	2.5		ns
tH_{PIN}	STS-12c PIN[7:0] Hold time to TFCLK	1		ns
tS_{FPIN}	STS-12c FPIN Set-up time to TFCLK	2.5		ns
tH_{FPIN}	STS-12c FPIN Hold time to TFCLK	1		ns
f_{PICLK}	STS-3c PICLK Frequency		19.44	MHz
D_{PICLK}	STS-3c PICLK Duty Cycle	40	60	%
tS_{PIN}	STS-3c PIN[7:0] Set-up time to TFCLK	2.5		ns
tH_{PIN}	STS-3c PIN[7:0] Hold time to TFCLK	1		ns
tS_{FPIN}	STS-3c FPIN Set-up time to TFCLK	2.5		ns
tH_{FPIN}	STS-3c FPIN Hold time to TFCLK	1		ns

Figure 55: Receive Parallel Line Interface Timing Diagram

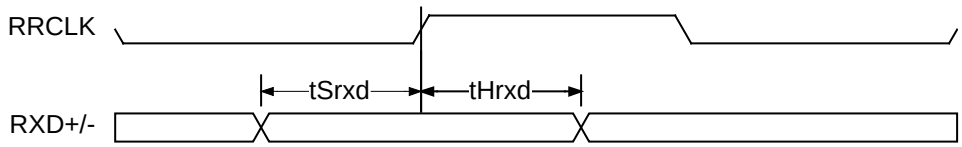


18.3 Serial Line Interface Timing

Table 25: Receive Serial Line Interface Timing (Figure 56)

Symbol	Description	Min	Max	Units
f_{RRCLK}	RRCLK Frequency	1	622.04	MHz
D_{RRCLK}	RRCLK Duty Cycle	45	55	%
tS_{RXD}	RXD+/- Set-up time to RRCLK		200	ps
tH_{RXD}	RXD+/- Hold time to RRCLK		800	ps

Figure 56: Receive Serial Line Interface Timing Diagram



18.4 UTOPIA Level 2 System Interface Timing

Table 26: Transmit UTOPIA Level 2 System Interface Timing (Figure 57)

Symbol	Description	Min	Max	Units
f_{TFCLK}	TFCLK Frequency	40	50	MHz
D_{TFCLK}	TFCLK Duty Cycle	40	60	%
J_{TFCLK}	TFCLK Peak to Peak Jitter (> 1 MHz)		1.4	ns
tS_{TENB}	TENB Set-up time to TFCLK	2		ns
tH_{TENB}	TENB Hold time to TFCLK	0		ns
tS_{TDAT}	TDAT[15:0] Set-up time to TFCLK	2		ns
tH_{TDAT}	TDAT[15:0] Hold time to TFCLK	0		ns
tS_{TPRTY}	TPRTY Set-up time to TFCLK	2		ns
tH_{TPRTY}	TPRTY Hold time to TFCLK	0		ns
tS_{TSOC}	TSOC Set-up time to TFCLK	2		ns
tH_{TSOC}	TSOC Hold time to TFCLK	0		ns
tP_{TCA}	TFCLK High to TCA Valid	1	8.5	ns

Figure 57: Transmit UTOPIA Level 2 System Interface Timing Diagram

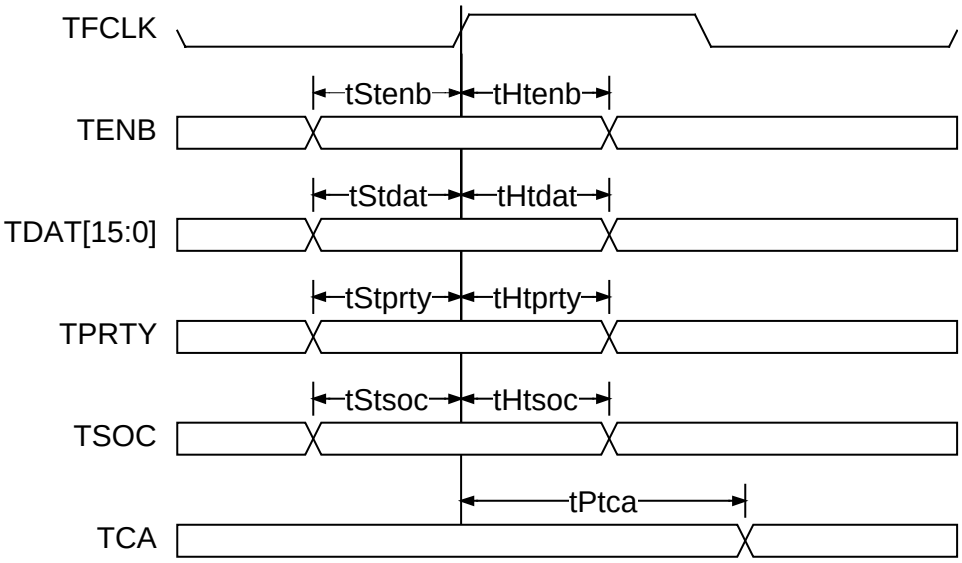
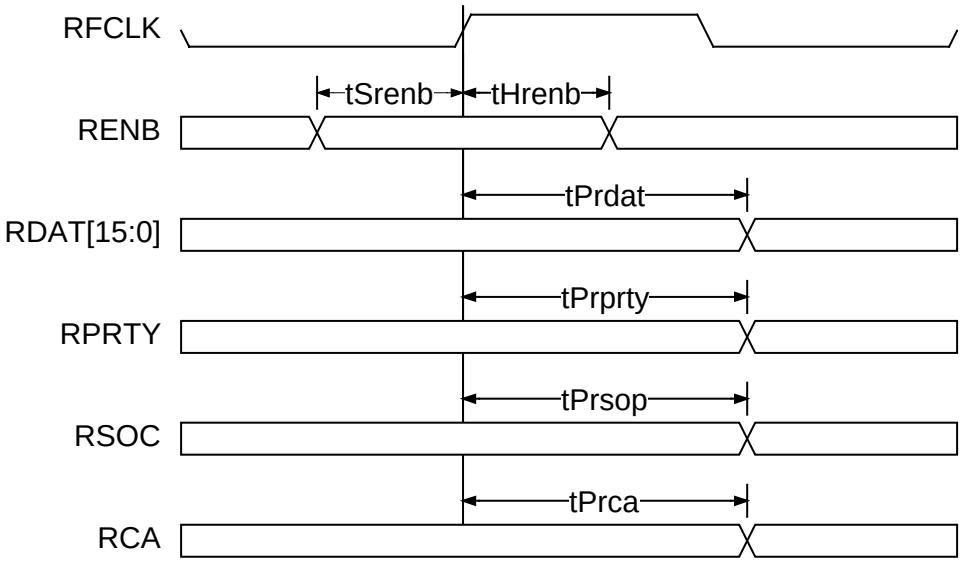


Table 27: Receive UTOPIA Level 2 System Interface Timing (Figure 58)

Symbol	Description	Min	Max	Units
f_{RFCLK}	RFCLK Frequency	40	50	MHz
D_{RFCLK}	RFCLK Duty Cycle	40	60	%
J_{RFCLK}	RFCLK Peak to Peak Jitter (> 1 MHz)		1.4	ns
tS_{RENB}	RENB Set-up time to RFCLK	2		ns
tH_{RENB}	RENB Hold time to RFCLK	0		ns
tP_{RDAT}	RFCLK High to RDAT[15:0] Valid	1	8	ns
tZ_{RDAT}	RFCLK High to RDAT[15:0] Tri-state	1	8	ns
tZB_{RDAT}	RFCLK High to RDAT[15:0] Driven	0		ns
tP_{RSOC}	RFCLK High to RSOC Valid	1	8	ns
tZ_{RSOC}	RFCLK High to RSOC Tri-state	1	8	ns
tZB_{RSOC}	RFCLK High to RSOC Driven	1		ns
tP_{RPRTY}	RFCLK High to RPRTY Valid	1	8	ns
tZ_{RPRTY}	RFCLK High to RPRTY Tri-state	1	8	ns
tZB_{RPRTY}	RFCLK High to RPRTY Driven	0		ns
tP_{RCA}	RFCLK High to RCA Valid	1	8.5	ns

Figure 58: Receive UTOPIA Level 2 System Interface Timing Diagram



18.5 UTOPIA Level 3 System Interface Timing

Table 28: Transmit UTOPIA Level 3 System Interface Timing (Figure 59)

Symbol	Description	Min	Max	Units
f_{TFCLK}	TFCLK Frequency	60	100	MHz
D_{TFCLK}	TFCLK Duty Cycle	40	60	%
J_{TFCLK}	TFCLK Peak to Peak Jitter (> 1 MHz)		1	ns
tS_{TENB}	TENB Set-up time to TFCLK	2		ns
tH_{TENB}	TENB Hold time to TFCLK	0		ns
tS_{TDAT}	TDAT[7:0] Set-up time to TFCLK	2		ns
tH_{TDAT}	TDAT[7:0] Hold time to TFCLK	0		ns
tS_{TPRTY}	TPRTY Set-up time to TFCLK	2		ns
tH_{TPRTY}	TPRTY Hold time to TFCLK	0		ns
tS_{TSOC}	TSOC Set-up time to TFCLK	2		ns
tH_{TSOC}	TSOC Hold time to TFCLK	0		ns
tP_{TCA}	TFCLK High to TCA Valid	1	5	ns

Figure 59: Transmit UTOPIA Level 3 System Interface Timing Diagram

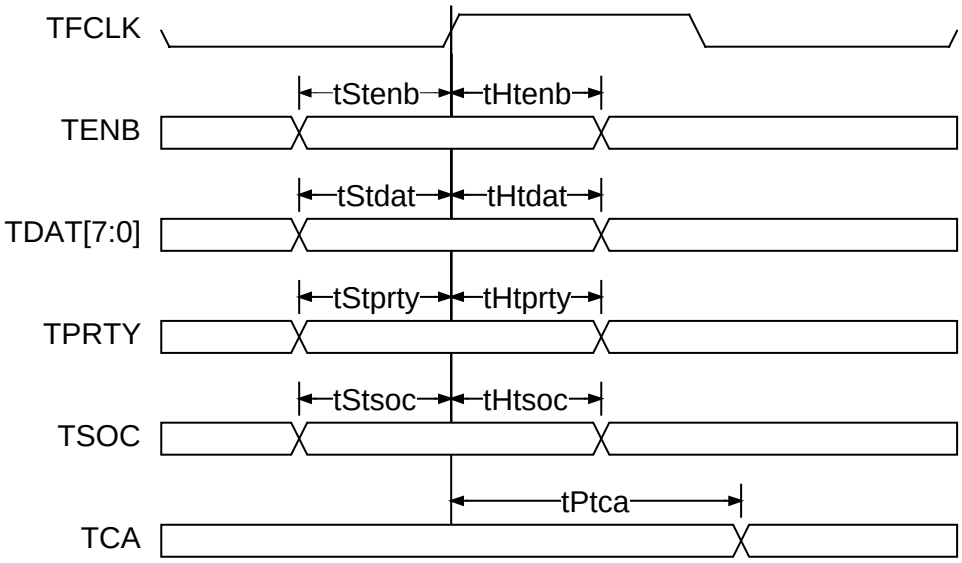
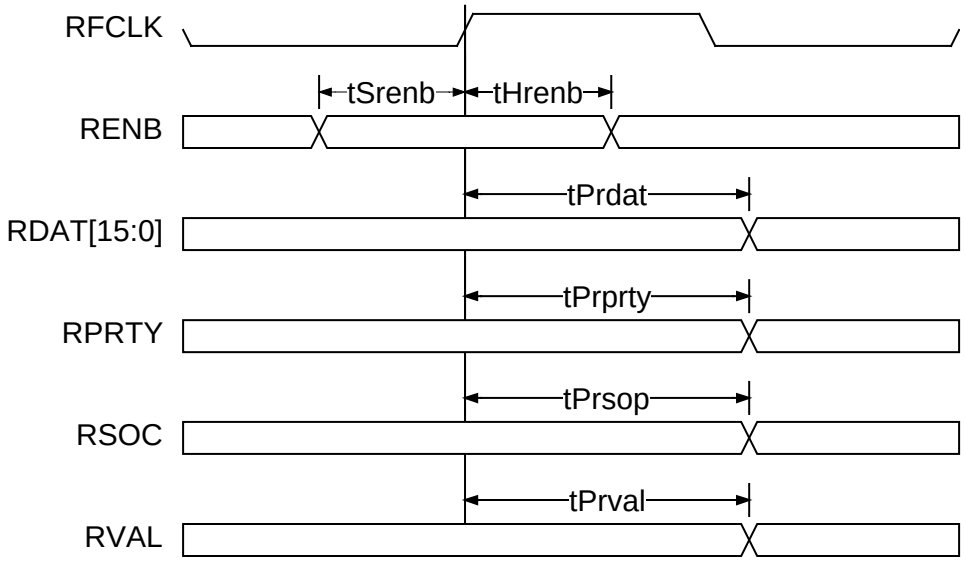


Table 29: Receive UTOPIA Level 3 System Interface Timing (Figure 60)

Symbol	Description	Min	Max	Units
f_{RFCLK}	RFCLK Frequency	60	100	MHz
D_{RFCLK}	RFCLK Duty Cycle	40	60	%
J_{RFCLK}	RFCLK Peak to Peak Jitter (> 1 MHz)		1	ns
tS_{RENB}	RENB Set-up time to RFCLK	2		ns
tH_{RENB}	RENB Hold time to RFCLK	0		ns
tP_{RDAT}	RFCLK High to RDAT[7:0] Valid	1	5	ns
tP_{RSOC}	RFCLK High to RSOC Valid	1	5	ns
tP_{RPRTY}	RFCLK High to RPRTY Valid	1	5	ns
tP_{RVAL}	RFCLK High to RVAL Valid	1	5	ns

Figure 60: Receive UTOPIA Level 3 System Interface Timing Diagram



18.6 POS Level 2 System Interface Timing

Table 30: Transmit POS-PHY Level 2 System Interface Timing (Figure 61)

Symbol	Description	Min	Max	Units
f_{TFCLK}	TFCLK Frequency	40	50	MHz
D_{TFCLK}	TFCLK Duty Cycle	40	60	%
J_{TFCLK}	TFCLK Peak to Peak Jitter (> 1 MHz)		1	ns
tS_{TENB}	TENB Set-up time to TFCLK	2		ns
tH_{TENB}	TENB Hold time to TFCLK	0		ns
tS_{TDAT}	TDAT[15:0] Set-up time to TFCLK	2		ns
tH_{TDAT}	TDAT[15:0] Hold time to TFCLK	0		ns
tS_{TPRTY}	TPRTY Set-up time to TFCLK	2		ns
tH_{TPRTY}	TPRTY Hold time to TFCLK	0		ns
tS_{TSOP}	TSOP Set-up time to TFCLK	2		ns
tH_{TSOP}	TSOP Hold time to TFCLK	0		ns
tS_{TEOP}	TEOP Set-up time to TFCLK	2		ns
tH_{TEOP}	TEOP Hold time to TFCLK	0		ns
tS_{TMOD}	TMOD Set-up time to TFCLK	2		ns
tH_{TMOD}	TMOD Hold time to TFCLK	0		ns
tS_{TERR}	TERR Set-up time to TFCLK	2		ns
tH_{TERR}	TERR Hold time to TFCLK	0		ns
tP_{TPA}	TFCLK High to TPA Valid	1	8.5	ns

Figure 61: Transmit POS-PHY Level 2 System Interface Timing

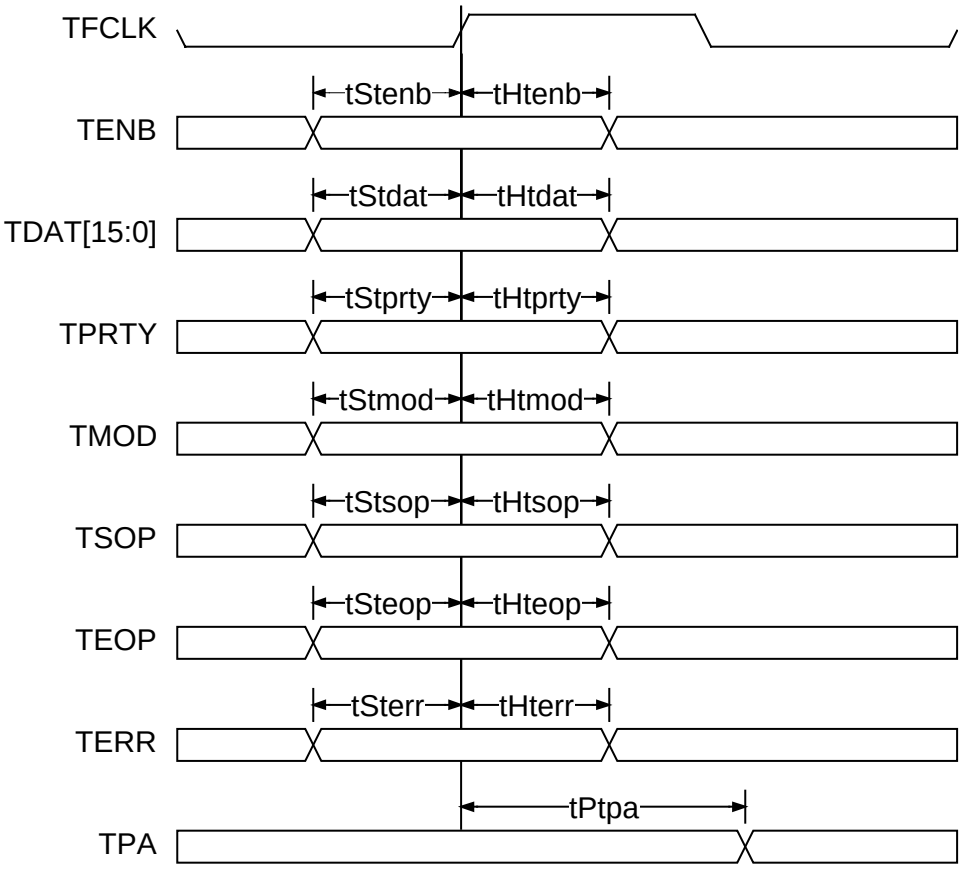
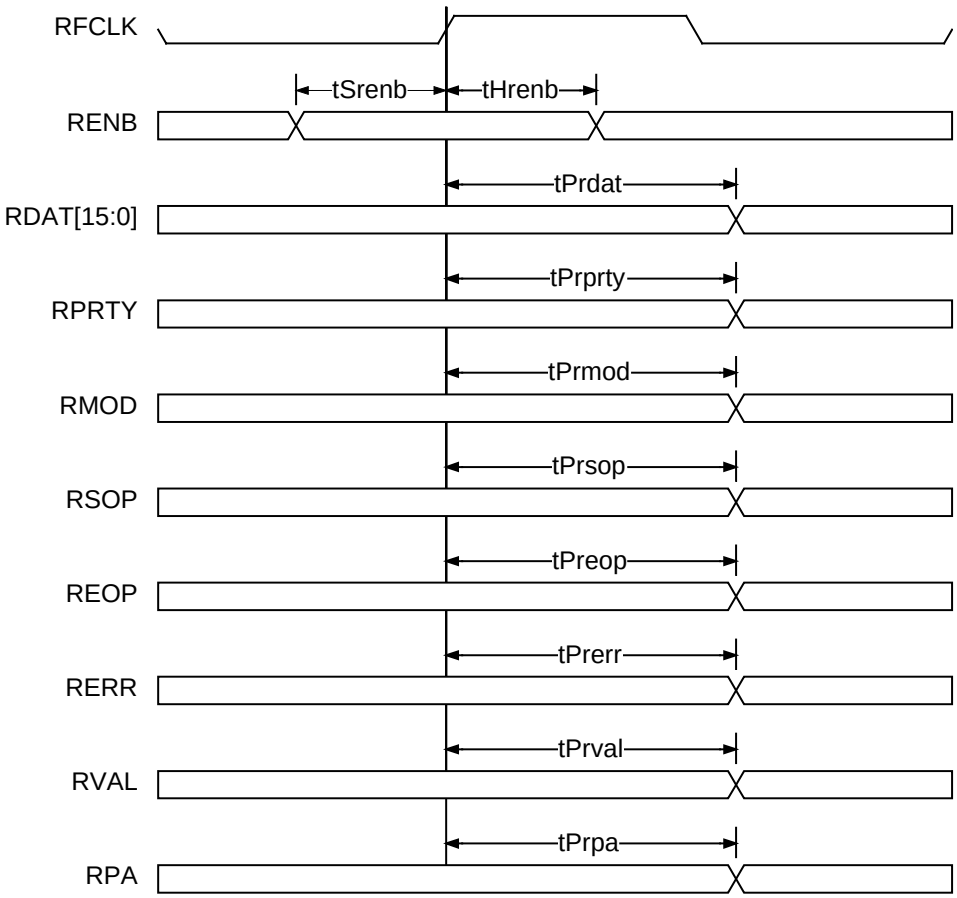


Table 31: Receive POS-PHY Level 2 System Interface Timing (Figure 62)

Symbol	Description	Min	Max	Units
f_{RFCLK}	RFCLK Frequency	40	50	MHz
D_{RFCLK}	RFCLK Duty Cycle	40	60	%
J_{RFCLK}	RFCLK Peak to Peak Jitter (> 1 MHz)		1	ns
tS_{RENB}	RENB Set-up time to RFCLK	2		ns
tH_{RENB}	RENB Hold time to RFCLK	0		ns
tP_{RDAT}	RFCLK High to RDAT[15:0] Valid	1	8	ns
tZ_{RDAT}	RFCLK High to RDAT[15:0] Tri-state	1	8	ns
tZB_{RDAT}	RFCLK High to RDAT[15:0] Driven	0		ns
tP_{RPRTY}	RFCLK High to RPRTY Valid	1	8	ns
tZ_{RPRTY}	RFCLK High to RPRTY Tri-state	1	8	ns
tZB_{RPRTY}	RFCLK High to RPRTY Driven	0		ns
tP_{RSOP}	RFCLK High to RSOP Valid	1	8	ns
tZ_{RSOP}	RFCLK High to RSOP Tri-state	1	8	ns
tZB_{RSOP}	RFCLK High to RSOP Driven	0		ns
tP_{REOP}	RFCLK High to REOP Valid	1	8	ns
tZ_{REOP}	RFCLK High to REOP Tri-state	1	8	ns
tZB_{REOP}	RFCLK High to REOP Driven	0		ns
tP_{RMOD}	RFCLK High to RMOD Valid	1	8	ns
tZ_{RMOD}	RFCLK High to RMOD Tri-state	1	8	ns
tZB_{RMOD}	RFCLK High to RMOD Driven	0		ns
tP_{RERR}	RFCLK High to RERR Valid	1	8	ns
tZ_{RERR}	RFCLK High to RERR Tri-state	1	8	ns
tZB_{RERR}	RFCLK High to RERR Driven	0		ns
tP_{RVAL}	RFCLK High to RVAL Valid	1	8	ns
tZ_{RVAL}	RFCLK High to RVAL Tri-state	1	8	ns
tZB_{RVAL}	RFCLK High to RVAL Driven	0		ns
tP_{RPA}	RFCLK High to RPA Valid	1	8.5	ns

Figure 62: Receive POS-PHY Level 2 System Interface Timing



18.7 POS Level 3 System Interface Timing

Table 32: Transmit POS-PHY Level 3 System Interface Timing (Figure 63)

Symbol	Description	Min	Max	Units
f_{TFCLK}	TFCLK Frequency	60	100	MHz
D_{TFCLK}	TFCLK Duty Cycle	40	60	%
J_{TFCLK}	TFCLK Peak to Peak Jitter (> 1 MHz)		1	ns
tS_{TENB}	TENB Set-up time to TFCLK	2		ns
tH_{TENB}	TENB Hold time to TFCLK	0		ns
tS_{TDAT}	TDAT[7:0] Set-up time to TFCLK	2		ns
tH_{TDAT}	TDAT[7:0] Hold time to TFCLK	0		ns
tS_{TPRTY}	TPRTY Set-up time to TFCLK	2		ns
tH_{TPRTY}	TPRTY Hold time to TFCLK	0		ns
tS_{TSOP}	TSOP Set-up time to TFCLK	2		ns
tH_{TSOP}	TSOP Hold time to TFCLK	0		ns
tS_{TEOP}	TEOP Set-up time to TFCLK	2		ns
tH_{TEOP}	TEOP Hold time to TFCLK	0		ns
tS_{TERR}	TERR Set-up time to TFCLK	2		ns
tH_{TERR}	TERR Hold time to TFCLK	0		ns
tP_{TPA}	TFCLK High to TPA Valid	1	5	ns

Figure 63: Transmit POS-PHY Level 3 System Interface Timing

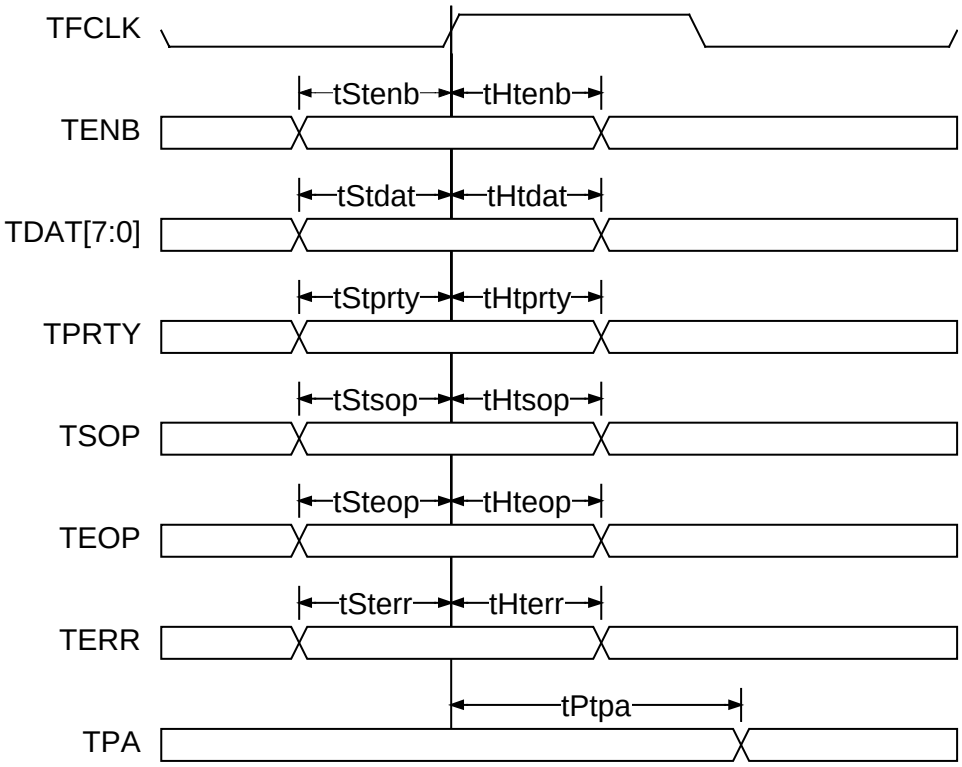
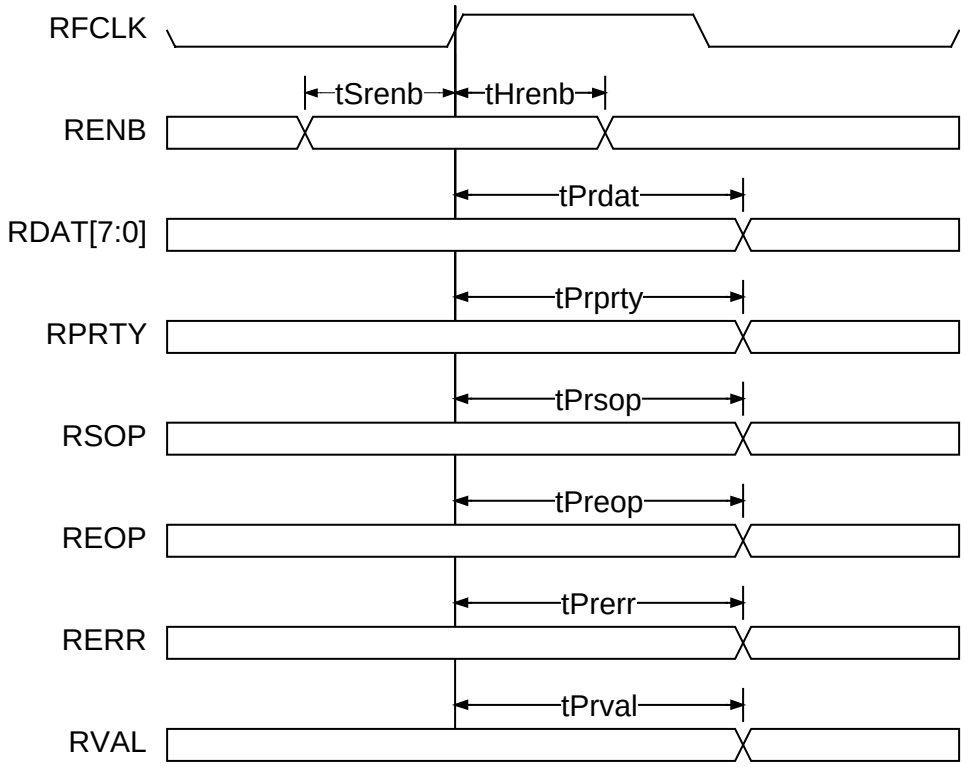


Table 33: Receive POS-PHY Level 3 System Interface Timing (Figure 64)

Symbol	Description	Min	Max	Units
f_{RFCLK}	RFCLK Frequency	60	100	MHz
D_{RFCLK}	RFCLK Duty Cycle	40	60	%
J_{RFCLK}	RFCLK Peak to Peak Jitter (> 1 MHz)		1	ns
tS_{RENB}	RENB Set-up time to RFCLK	2		ns
tH_{RENB}	RENB Hold time to RFCLK	0		ns
tP_{RDAT}	RFCLK High to RDAT[7:0] Valid	1	5	ns
tP_{RPRTY}	RFCLK High to RPRTY Valid	1	5	ns
tP_{RSOP}	RFCLK High to RSOP Valid	1	5	ns
tP_{REOP}	RFCLK High to REOP Valid	1	5	ns
tP_{RERR}	RFCLK High to RERR Valid	1	5	ns
tP_{RVAL}	RFCLK High to RVAL Valid	1	5	ns

Figure 64: Receive POS-PHY Level 3 System Interface Timing

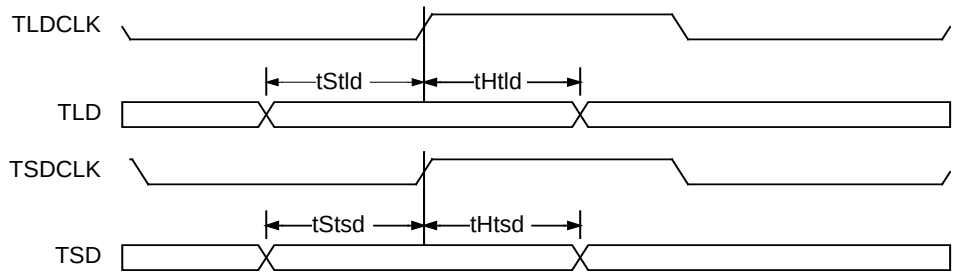


18.8 Transmit DCC Interface Timing

Table 34: Transmit DCC Interface Timing (Figure 65)

Symbol	Description	Min	Max	Units
tS_{TLD}	TLD Set-up time to TLDCLK	25		ns
tH_{TLD}	TLD Hold time to TLDCLK	25		ns
tS_{TSD}	TSD Set-up time to TSDCLK	25		ns
tH_{TSD}	TSD Hold time to TSDCLK	25		ns

Figure 65: Transmit DCC Interface Timing

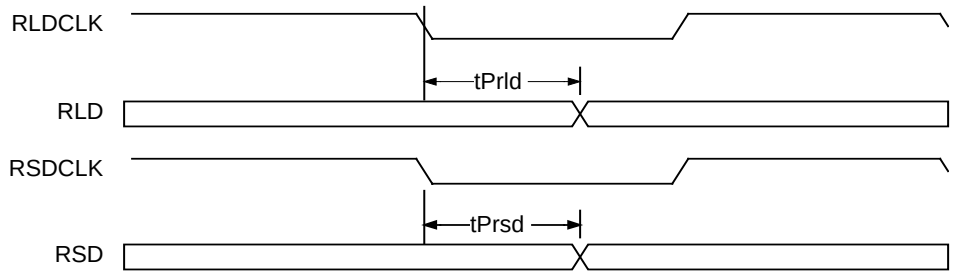


18.9 Receive DCC Interface Timing

Table 35: Receive DCC Interface Timing (Figure 66)

Symbol	Description	Min	Max	Units
tP_{RLD}	RLDCLK low to RLD valid	-20	20	ns
tP_{RSD}	RSDCLK low to RSD valid	-20	20	ns

Figure 66: Receive DCC Interface Timing

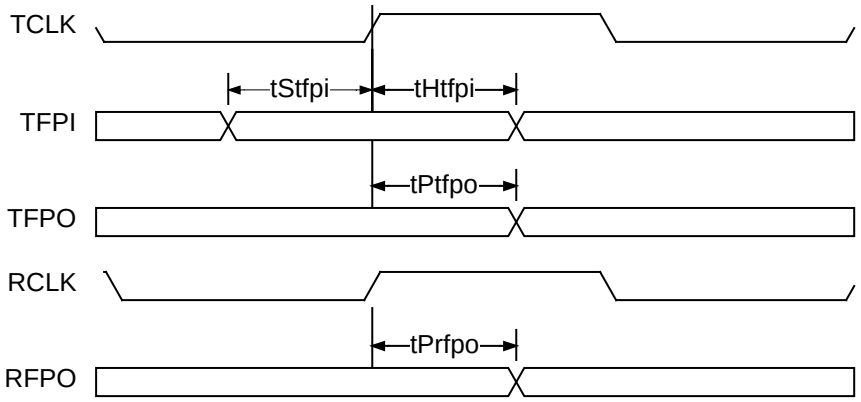


18.10 Clock and Frame Pulse Interface Timing

Table 36: Clock and Frame Pulse Interface Timing (Figure 67)

Symbol	Description	Min	Max	Units
	TCLK Frequency		77.76	MHz
	TCLK Duty Cycle	40	60	%
	RCLK Frequency		77.76	MHz
	RCLK Duty Cycle	40	60	%
tS_{TFPI}	TFPI Set-up time to TCLK	2.5		ns
tH_{TFPI}	TFPI Hold time to TCLK	0		ns
tP_{TFPO}	TCLK High FPO Valid	1	6	ns
tP_{RFPO}	RCLK High FPO Valid	1	6	ns

Figure 67: Clock and Frame Pulse Interface Timing

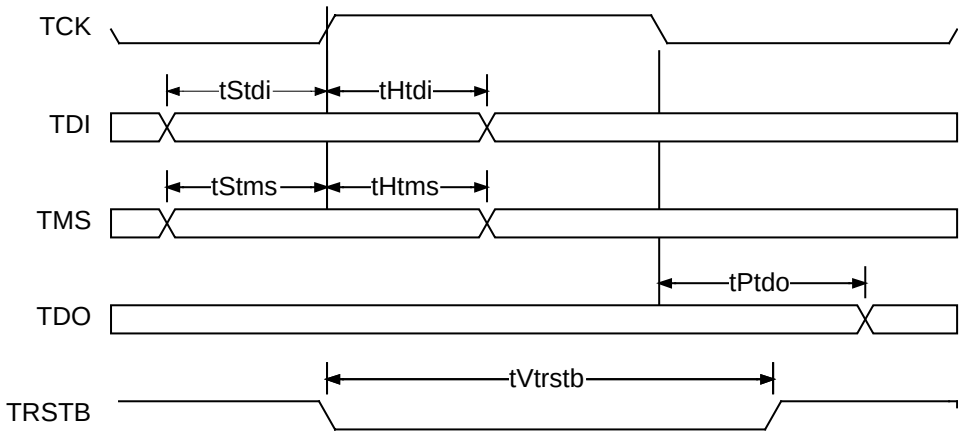


18.11 JTAG Test Port Timing

Table 37: JTAG Port Interface (Figure 68)

Symbol	Description	Min	Max	Units
	TCK Frequency		4	MHz
	TCK Duty Cycle	40	60	%
tS_{TMS}	TMS Set-up time to TCK	25		ns
tH_{TMS}	TMS Hold time to TCK	25		ns
tS_{TDI}	TDI Set-up time to TCK	25		ns
tH_{TDI}	TDI Hold time to TCK	25		ns
tP_{TDO}	TCK Low to TDO Valid	2	50	ns
tV_{TRSTB}	TRSTB Pulse Width	100		ns

Figure 68: JTAG Port Interface Timing



Notes on Input Timing:

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 50 pF load on the outputs.

3. Output tri-state delay is the time in nanoseconds from the 1.4 Volt of the reference signal to the point where the total current delivered through the output is less than or equal to the leakage current.

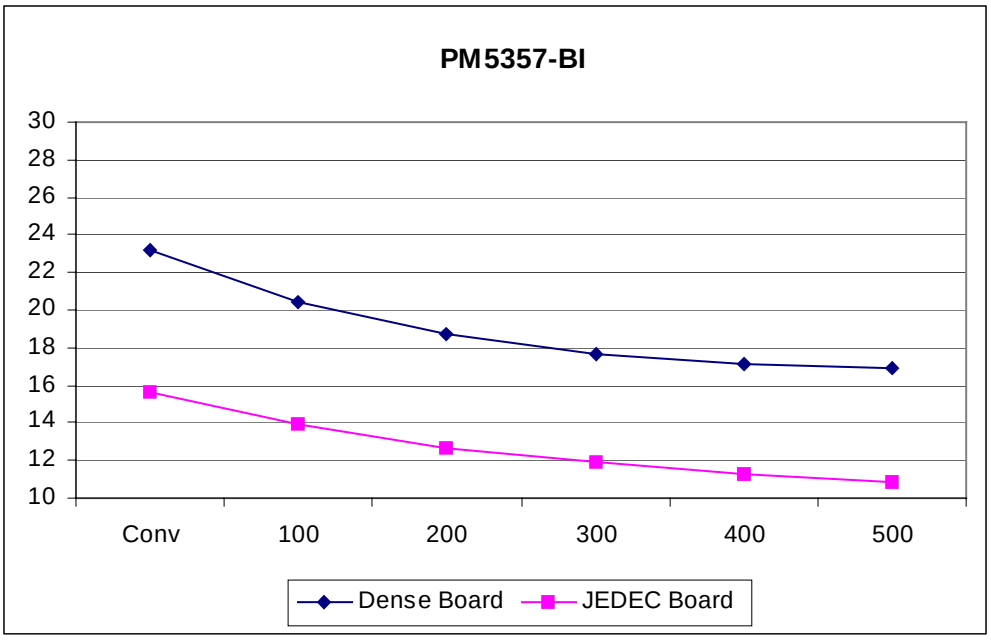
19 ORDERING AND THERMAL INFORMATION

Table 38: Ordering Information

PART NO.	DESCRIPTION
PM5357-BI	304-pin Ball Grid Array (SBGA)

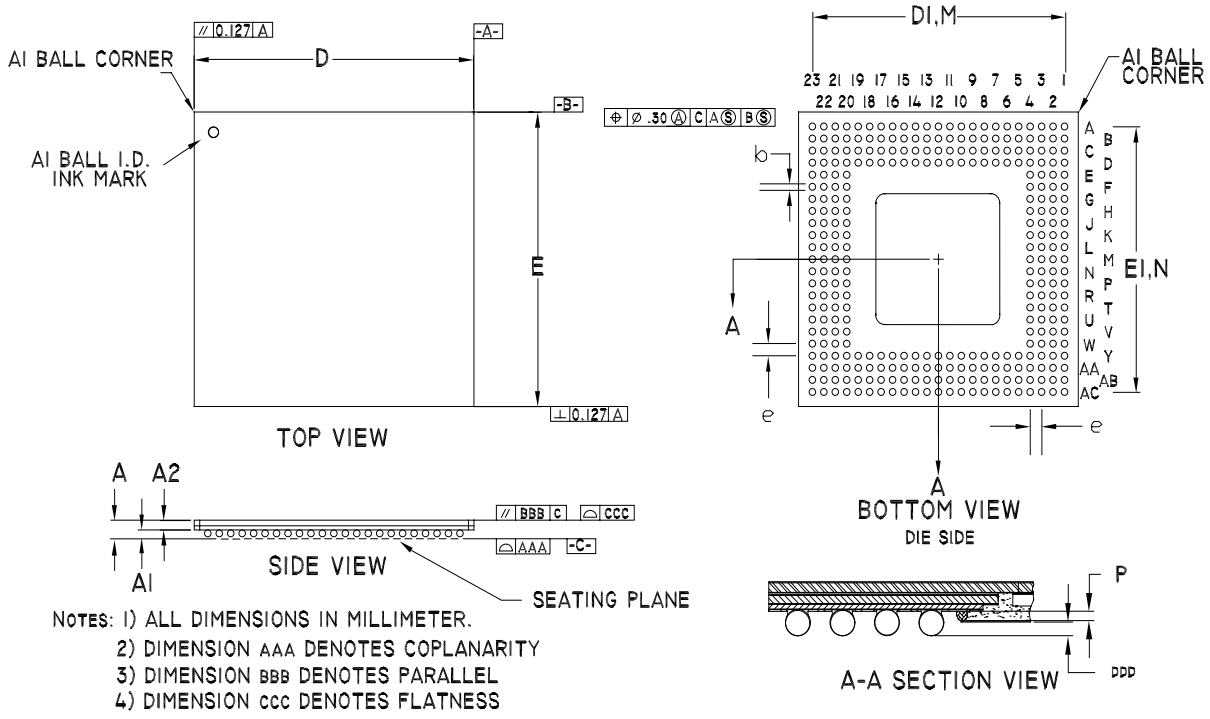
Table 39: Thermal Information

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM5357-BI	-40°C to 85°C	22 °C/W	1 °C/W



20 MECHANICAL INFORMATION

Figure 69: Mechanical Drawing 304 Pin Super Ball Grid Array (SBGA)



PACKAGE TYPE: 304 PIN THERMAL BALL GRID ARRAY															
BODY SIZE: 31 x 31 x 1.45 MM															
DIM.	A	A1	A2	D	D1	E	E1	M,N	e	b	aaa	bbb	ccc	ddd	P
MIN.	1.41	0.56	0.85	30.90	27.84	30.90	27.84			0.60				0.15	0.20
NOM.	1.54	0.63	0.91	31.00	27.94	31.00	27.94	23x23	1.27	0.75				0.33	0.30
MAX.	1.67	0.70	0.97	31.10	28.04	31.10	28.04			0.90	0.15	0.15	0.20	0.50	0.35

NOTES

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