PM4354

COMET-QUAD

FOUR CHANNEL COMBINED E1/T1 TRANSCEIVER/FRAMER

DATA SHEET

PROPRIETARY AND CONFIDENTIAL

ADVANCED

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CONTENTS

LIST OF FIGURES

LIST OF TABLES

FEATURES

- Monolithic device which integrates four, software selectable, full-featured T1 and E1 framers and T1 and E1 short haul and long haul line interfaces.
- Meets or exceeds T1 and E1 shorthaul and longhaul network access specifications including ANSI T1.102, T1.403, T1.408, AT&T TR 62411, ITU-T G.703, G.704 as well as ETSI 300-011, CTR-4, CTR-12 and CTR-13.
- Provides encoding and decoding of B8ZS, HDB3 and AMI line codes.
- Provides receive equalization, clock recovery and line performance monitoring.
- Provides transmit and receive jitter attenuation.
- Provides digitally programmable long haul and short haul line build out.
- Provides four full-featured HDLC controllers, each with 128-byte transmit and receive FIFO buffers.
- Automatically generates and transmits DS-1 performance report messages to ANSI T1.231 and ANSI T1.408 specifications.
- Supports Nx64Kbit/s fractional bandwidth backplane.
- Supports transfer of PCM data to/from 1.544MHz and 2.048MHz system-side devices. Also supports a fractional T1 or E1 system interface with independent backplane receive/backplane transmit Nx64Kbit/s rates. Supports a 2.048 MHz system-side interface for T1 mode without external clock gapping.
- Supports 8Mbit/s, H-100 compatible, H-MVIP on the system interface for all T1 or E1 links, a separate 8Mbit/s H-MVIP system interface for all T1 or E1 CAS channels and a separate 8Mbit/s H-MVIP system interface for all T1 or E1 CCS, V5.1/V5.2, and GR.303 channels.
- Provides a selectable, per channel independent de-jittered T1 or E1 recovered clock for system timing and redundancy.
- Provides PRBS generators and detectors on each tributary for error testing at DS1, E1 and Nx64Kbit/s rates as recommended in ITU-T O.151 and O.152.
- Provides robbed bit signaling extraction and insertion on a per-DS0 basis.
- Register level compatibility with the PM4388 TOCTL Octal T1 Framer, the PM6388 EOCTL Octal E1 Framer, the PM4351 COMET E1/T1 transceiver, and the PM8315 TEMUX T1/E1 Framer with integrated Mapper and M13 MUX.
- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Uses line rate system clock.

- Provides a IEEE P1149.1 (JTAG) compliant test access port (TAP) and controller for boundary scan test.
- Implemented in a low power 5 V tolerant 2.5/3.3 V CMOS technology.
- Available in a high density 208-pin fine pitch PBGA (17 mm by 17 mm) package.
- Provides a -40°C to +85°C Industrial temperature operating range.

1.1 Receiver section:

- Supports T1 signal reception for distances with up to 36 dB of cable attenuation (at 772 kHz).
- Supports E1 signal reception for distances with up to 36 dB of cable attenuation (at 1.024 MHz).
- Recovers clock and data using a digital phase locked loop for high jitter tolerance.
- Frames to ITU-T G.704 basic and CRC-4 multiframe formatted E1 signals. The framing procedures are consistent ITU-T G.706 specifications.
- Frames to DSX/DS-1 signals in SF, and ESF formats.
- Frames to TTC JT-G704 multiframe formatted J1 signals. Supports the alternate CRC-6 calculation for Japanese applications. Frames in the presence of and detects the “Japanese Yellow” alarm.
- Tolerates more than 0.3 UI peak-to-peak, high frequency jitter as required by AT&T TR 62411 and Bellcore TR-TSY-000170.
- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window.
- Provides loss of signal detection as per ITU-T G.775 and ANSI T1.231. Red, Yellow, and AIS alarm detection and integration are according to ANSI T1.231 specifications.
- Provides programmable in-band loopback activate and deactivate code detection.
- Supports line and path performance monitoring according to AT&T and ANSI specifications. Accumulators are provided for counting ESF CRC-6 errors, framing bit errors, line code violations and loss of frame or change of frame alignment events.
- Provides performance monitoring counters sufficiently large as to allow performance monitor counter polling at a minimum rate of once per second. Optionally, updates the performance monitoring counters and interrupts the microprocessor once per second, timed to the receive line.
- Provides ESF bit-oriented code detection and an HDLC/LAPD interface for terminating the ESF facility data link.
- Supports polled or interrupt-driven servicing of the HDLC interface.
- Extracts the data link in ESF mode and extracts a datalink in the E1 national use bits.

- Extracts 4-bit codewords from the E1 national use bits as specified in ETS 300 233
- Extracts up to three HDLC links, to an H-MVIP Bus, to support the D-channel for ISDN Primary Rate Interfaces and the C-channels for V5.1/V5.2 interfaces. Detects the V5.2 link identification signal.
- Provides a two-frame elastic store buffer for backplane rate adaptation that performs controlled slips and indicates slip occurrence and direction.
- Provides DS-1 robbed bit signaling extraction, with optional data inversion, programmable idle code substitution, digital milliwatt code substitution, bit fixing, and two superframes of signaling debounce on a per-channel basis.
- Frames to the E1 signaling multiframe alignment when enabled and extracts channel associated signaling. Alternatively, a common channel signaling data link may be extracted from timeslot 16.
- Indicates signaling state change, and two superframes of signaling debounce on a per-DS0 basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all channels or on selected channels.
- Provides diagnostic, line loopbacks and per-DS0 payload loopback.
- A pseudo-random sequence user selectable from 2^{11} –1, 2^{15} –1 or 2^{20} –1, may be detected in the T1/E1 stream in either the backplane receive or backplane transmit directions. The detector counts pattern errors using a 24-bit saturating PRBS error counter.

1.2 Transmitter section:

- Generates DSX-1 shorthaul and DS-1 longhaul pulses with programmable pulse shape compatible with AT&T, ANSI and ITU requirements.
- Generates E1 pulses compliant to G.703 recommendations.
- Provides a digitally programmable pulse shape extending up to 5 transmitted bit periods for custom long haul pulse shaping applications.
- Provides line outputs that are current limited and may be tristated for protection or in redundant applications.
- Provides a digital phase locked loop for generation of a low jitter transmit clock complying with all jitter attenuation, jitter transfer and residual jitter specifications of AT&T TR 62411 and ETSI TBR 12 and TBR 13.
- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmit path.
- Provides a two-frame payload slip buffer to allow independent backplane and line timing.
- A pseudo-random sequence user selectable from 2^{11} –1, 2^{15} –1 or2^{20} –1, may be inserted into or detected from the T1 or E1 stream in either the backplane receive or backplane transmit directions.

- Transmits G.704 basic and CRC-4 multiframe formatted E1 signals or D4, SF or ESF formatted DSX/DS-1 signals.
- Transmits the “Japanese Yellow” alarm. Transmits TTC JT-G704 multiframe formatted J1 signals. Supports the alternate ESF CRC-6 calculation for Japanese applications.
- Supports unframed mode and framing bit, CRC, or data link by-pass.
- Provides signaling insertion, programmable idle code substitution, digital milliwatt code substitution, and data inversion on a per channel basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all channels or on selected channels.
- Provides minimum ones density through Bell (bit 7), GTE or DDS zero code suppression on a per channel basis.
- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window and optionally stuffs ones to maintain minimum ones density.
- Allows insertion of framed or unframed in-band loopback code sequences.
- Allows insertion of a data link in ESF mode. Optionally inserts a datalink in the E1 national use bits.
- Supports 4-bit codeword insertion in the E1 national use bits as specified in ETS 300 233
- Inserts, from an H-MVIP bus, up to three HDLC links to support the D-channel for ISDN Primary Rate Interfaces and the C-channels for V5.1/V5.2 interfaces.
- Supports transmission of the alarm indication signal (AIS) and the Yellow alarm signal. Supports “Japanese Yellow” alarm generation.
- Provides ESF bit-oriented code generation.

Synchronous System Interfaces:

- Provides an 8 Mbit/s H-MVIP data interface for synchronous access to all the T1 DS0s or E1 timeslots. Compatible with H-MVIP PCM backplanes supporting 8.192 Mbit/s.
- Provides an 8 Mbit/s H-MVIP interface for synchronous access to all channel associated signaling (CAS) bits for all T1 DS0s or E1 timeslots. The CAS bits occupy one nibble of every byte on the H-MVIP interfaces and are repeated over the entire T1 or E1 multi-frame.
- Provides an 8Mbit/s H-MVIP interface for common channel signaling (CCS) channels as well as V5.1 and V5.2 channels. In T1 mode DS0 24 is available through this interface. In E1 mode timeslots 15, 16 and 31 are available through this interface.
- All links accessed via the H-MVIP interface will be synchronously timed to the common H-MVIP clock and frame alignment signals, CMV8MCLK, CMVFPB, CMVFPC.

APPLICATIONS

- T1/E1 Wireless Digital Loop Carriers (DLC's) and Cellular Base Stations
- T1/E1 Internet Access Equipment
- T1/E1 Channel Service Units (CSU)
- T1/E1 Frame Relay Interfaces
- T1/E1 ATM Interfaces
- T1/E1 Multiplexers (CPE MUX)
- Digital Private Branch Exchanges (PBX)
- Digital Access Cross-Connect Systems (DACS) and Electronic DSX Cross-Connect Systems (EDSX)
- ISDN Primary Rate Interfaces (PRI)
- Test Equipment

REFERENCES

1. ANSI - T1.101-1987 - American National Standard for Telecommunications - Digital Hierarchy - Timing Synchronization.
2. ANSI - T1.102-1993 - American National Standard for Telecommunications - Digital Hierarchy - Electrical Interfaces.
3. ANSI - T1.107-1995 - American National Standard for Telecommunications - Digital Hierarchy - Formats Specification.
4. ANSI - T1.231-1993 - American National Standard for Telecommunications - Layer 1 In-Service Digital Transmission Performance Monitoring
5. ANSI - T1.403-1995 - American National Standard for Telecommunications - Carrier to Customer Installation - DS-1 Metallic Interface Specification.
6. ANSI - T1.408-1990 - American National Standard for Telecommunications - Integrated Services Digital Network (ISDN) Primary Rate - Customer Installation Metallic Interfaces Layer 1 Specification.
7. T1M1.3/91-003R3 - American National Standard for Telecommunications - In-Service Digital Transmission Performance Monitoring Draft Standard.
8. TA-TSY-000147 - Bell Communications Research - DS-1 Rate Digital Service Monitoring Unit Functional Specification, Issue 1, October, 1987.

9. AT&T - PUB 54016 - Requirements For Interfacing Digital Terminal Equipment To Services Employing The Extended Superframe Format, October 1984.

10. AT&T - TR 62411 - Accunet T1.5 - Service Description and Interface Specification, December 1990.

11. AT&T - TR 62411 - Accunet T1.5 - Service Description and Interface Specification, Addendum 1, March 1991.

12. AT&T - TR 62411 - Accunet T1.5 - Service Description and Interface Specification, Addendum 2, October 1992.

13. AT&T - Interface Specification - Concentration Highway Interface - November 1990.

14. TR-TSY-000170 - Bellcore – Digital Cross-Connect System Requirements and Objectives, Issue 1, November 1985.

15. TR-N1WT-000233 - Bell Communications Research - Wideband and Broadband Digital Cross-Connect Systems Generic Criteria, Issue 3, November 1993.

16. TR-NWT-000303 - Bell Communications Research - Integrated Digital Loop Carrier Generic Requirements, Objectives, and Interface, Issue 2, December, 1992.

17. TR-TSY-000499 - Bell Communications Research - Transport Systems Generic Requirements (TSGR): Common Requirement, Issue 5, December, 1993.

18. TR-TSY-000820 - Bell Communications Research - OTGR: Network Maintenance Transport Surveillance - Generic Digital Transmission Surveillance, Section 5.1, Issue 1, June 1990.

19. ETSI - ETS 300 011 - ISDN Primary Rate User-Network Interface Specification and Test Principles, 1992.

20. ETSI - ETS 300 233 - Access Digital Section for ISDN Primary Rates.

21. ETSI - ETS 300 324-1 - Signaling Protocols and Switching (SPS); V interfaces at the Digital Local Exchange (LE) V5.1 Interface for the Support of Access Network (AN) Part 1: V5.1 Interface Specification, February 1994.

22. ETSI - ETS 300 347-1 - Signaling Protocols and Switching (SPS); V Interfaces at the Digital Local Exchange (LE) V5.2 Interface for the Support of Access Network (AN) Part 1: V5.2 Interface Specification, September 1994.

23. ETSI - CTR 4 - Integrated Services Digital Network (ISDN); Attachment requirements for terminal equipment to connect to an ISDN using ISDN primary rate access, November 1995.

24. ETSI - CTR 12 - Business Telecommunications (BT); Open Network Provision (ONP) technical requirements; 2 048 kbit/s digital unstructured leased lines (D2048U) Attachment requirements for terminal equipment interface, December 1993.

25. ETSI - CTR 13 - Business Telecommunications (BTC); 2 048 kbit/s digital structured leased lines (D2048S); Attachment requirements for terminal equipment interface, January 1996.

26. FCC Rules - Part 68.308 - Signal Power Limitations.

27. ITU-T - Recommendation G.703 - Physical/Electrical Characteristics of Hierarchical Digital Interface, Geneva, 1991.

28. ITU-T - Recommendation G.704 - Synchronous Frame Structures Used at Primary Hierarchical Levels, July 1995.

29. ITU-T - Recommendation G.706 - Frame Alignment and CRC Procedures Relating to G.704 Frame Structures, 1991.

30. ITU-T - Recommendation G.732 – Characteristics of Primary PCM Multiplex Equipment Operating at 2048 kbit/s, 1993.

31. ITU-T - Recommendation G.711 – Pulse Code Modulation (PCM) of Voice Frequencies, 1993.

32. ITU-T - Recommendation G.775 - Loss of Signal (LOS), November 1994.

33. ITU-T Recommendation G.802, - Interworking Between Networks Based on Different Digital Hierarchies and Speech Encoding Laws, 1993.

34. ITU-T Recommendation G.823, - The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy, 1993.

35. ITU-T Recommendation G.964, - V-Interfaces at the Digital Local Exchange (LE) - V5.1 Interface (Based on 2048 kbit/s) for the Support of Access Network (AN), June 1994.

36. ITU-T Recommendation G.965, - V-Interfaces at the Digital Local Exchange (LE) - V5.2 Interface (Based on 2048 kbit/s) for the Support of Access Network (AN), March 1995.

37. ITU-T - Recommendation I.431 - Primary Rate User-Network Interface – Layer 1 Specification, 1993.

38. ITU-T Recommendation O.151, - Error Performance Measuring Equipment For Digital Systems at the Primary Bit Rate and Above, 1988.

39. ITU-T Recommendation O.152 - Error Performance Measuring Equipment for Bit Rates of 64 kbit/s and N X 64 kbit/s, October 1992

40. ITU-T Recommendation O.153 - Basic Parameters for the Measurement of Error Performance at Bit Rates below the Primary Rate, October 1992.

41. ITU-T Recommendation Q.921 - ISDN User-Network Interface Data Link Layer Specification, March 1993.

42. International Organization for Standardization, ISO 3309:1984 - High-Level Data Link Control Procedures -- Frame Structure.

43. TTC Standard JT-G703 - Physical/Electrical Characteristics of Hierarchical Digital Interfaces, 1995.

44. TTC Standard JT-G704 - Frame Structures on Primary and Secondary Hierarchical Digital Interfaces, 1995.

45. TTC Standard JT-G706 - Frame Synchronization and CRC Procedure

46. TTC Standard JT-I431 - ISDN Primary Rate User-Network Interface Layer 1 - Specification, 1995.

47. Nippon Telegraph and Telephone Corporation - Technical Reference for High-Speed Digital Leased Circuit Services, Third Edition, 1990.

48. GO-MVIP - Multi-Vendor Integration Protocol, MVIP-90 Release 1.1, 1994.

49. GO-MVIP – H-MVIP Standard, Release 1.1a, 1997.

APPLICATION EXAMPLE

Figure 1 - Wireless Base Station Application

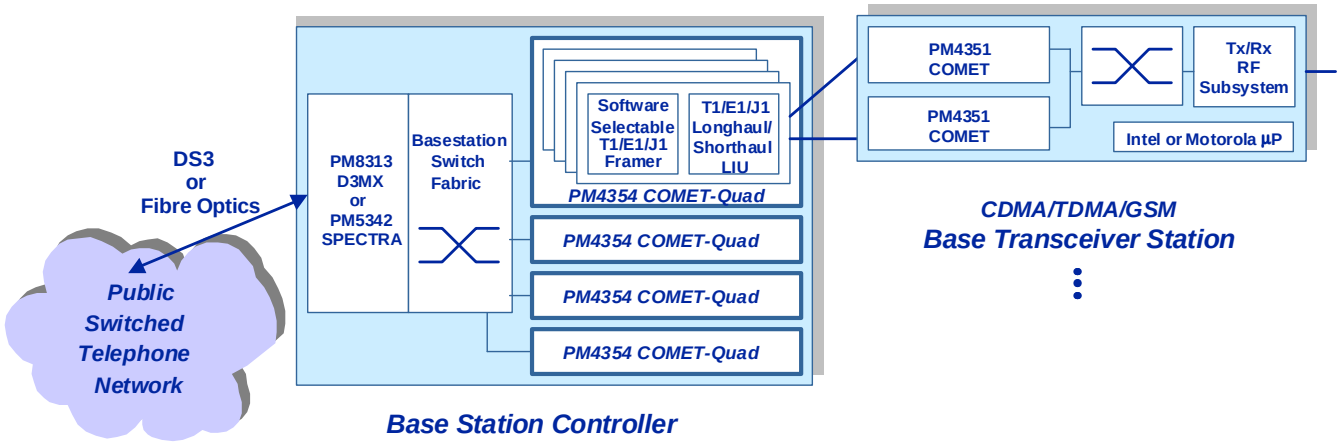
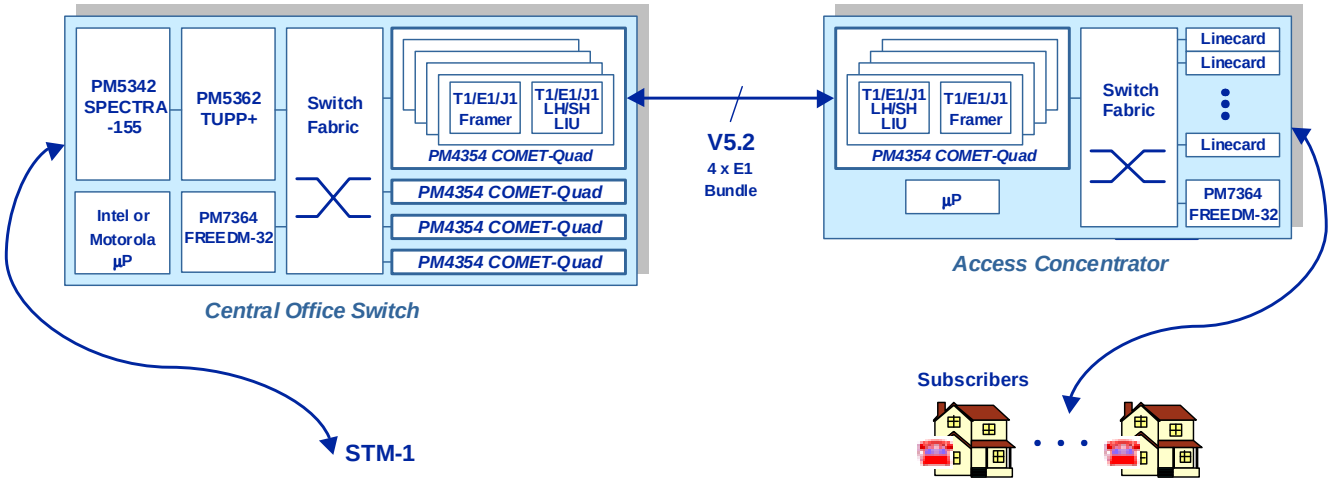
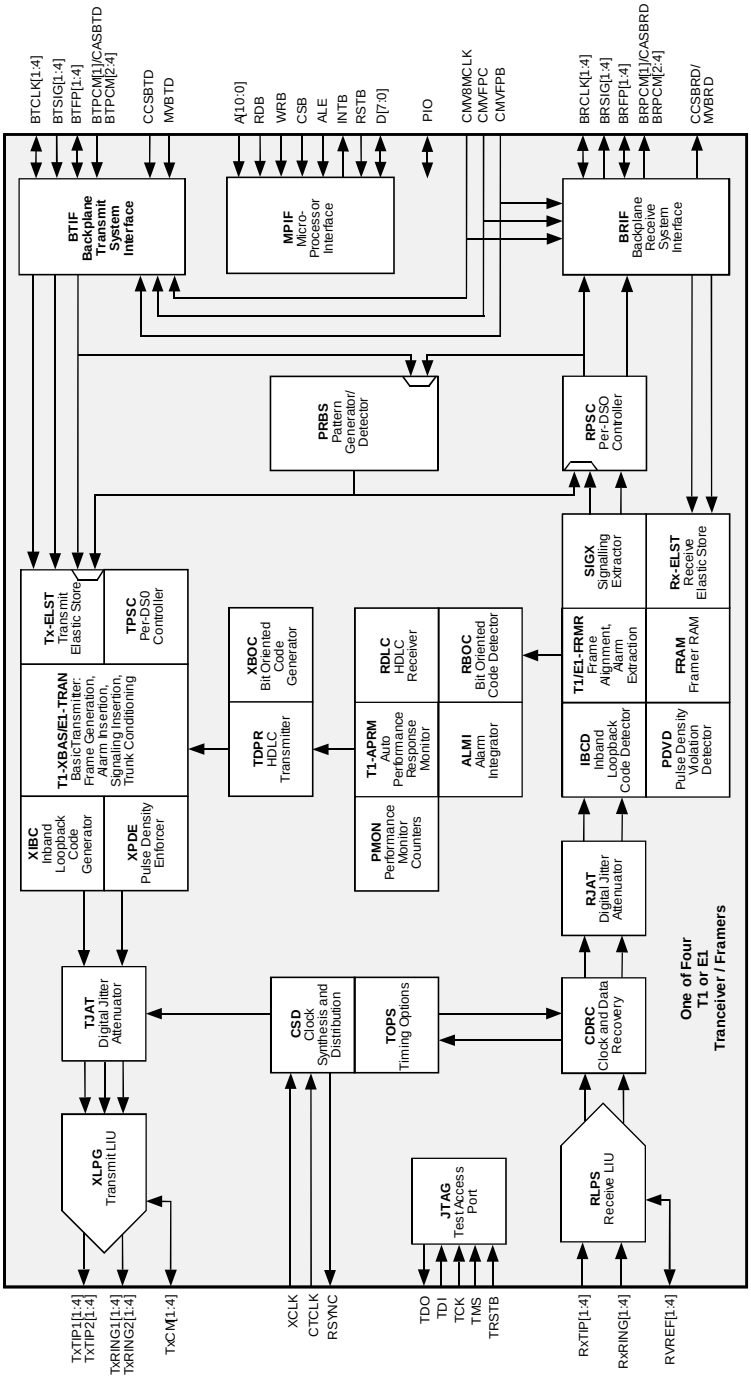


Figure 2 - V5.2 Interface Application



BLOCK DIAGRAM

Figure 3 - COMET-Quad Block Diagram



DESCRIPTION

The PM4354 Four Channel Combined E1/T1/J1 Transceiver and Framer (COMET-Quad) is a feature-rich monolithic integrated circuit suitable for use in long haul and short haul T1, J1 and E1

systems with a minimum of external circuitry. The COMET-Quad is software configurable, allowing feature selection without changes to external wiring.

Analog circuitry is provided to allow direct reception of long haul E1 and T1 compatible signals with up to 36 dB cable loss (at 1.024 MHz in E1 mode) or up to 36 dB cable loss (at 772 kHz in T1 mode) using a minimum of external components. Typically, only line protection, a transformer and a line termination resistor are required.

The COMET-Quad recovers clock and data from the line and frames to incoming data. In T1 mode, it can frame to SF and ESF signal formats. In E1 mode, the COMET-Quad frames to basic G.704 E1 signals and CRC-4 multiframe alignment signals, and automatically performs the G.706 interworking procedure. AMI, HDB3 and B8ZS line codes are supported.

The COMET-Quad supports detection of various alarm conditions such as loss of signal, pulse density violation, Red alarm, Yellow alarm, and AIS alarm in T1 mode and loss of signal, loss of frame, loss of signaling multiframe and loss of CRC multiframe in E1 mode. The COMET-Quad also supports reception of remote alarm signal, remote multiframe alarm signal, alarm indication signal, and timeslot 16 alarm indication signal in E1 mode. The presence of Yellow and AIS patterns in T1 mode and remote alarm and AIS patterns in E1 mode is detected and indicated. In T1 mode, the COMET-Quad integrates Yellow, Red, and AIS alarms as per industry specifications. In E1 mode, the COMET-Quad integrates Red and AIS alarms.

Performance monitoring with accumulation of CRC-6 errors, framing bit errors, line code violations, and loss of frame events are provided in T1 mode. In E1 mode, CRC-4 errors, far end block errors, framing bit errors, and line code violation are monitored and accumulated.

The COMET-Quad provides one receive HDLC controller per channel for the detection and termination of messages on the ESF facility data link (T1) or national use bits (E1). In T1 mode, the COMET-Quad also detects the presence of in-band loop back codes and ESF bit oriented codes. Detection and optional debouncing of the 4-bit Sa-bit codewords defined in ITU-T G.704 and ETSI 300-233 is supported. An interrupt may be generated on any change of state of the Sa codewords.

Dual (transmit and receive) elastic stores for slip buffering and rate adaptation to backplane timing are provided, as is a signaling extractor that supports signaling debounce, signaling freezing, idle code substitution, digital milliwatt tone substitution, data inversion, and signaling bit fixing on a per-channel basis. Receive side data and signaling trunk conditioning is also provided.

In T1 mode, the COMET-Quad generates framing for SF and ESF formats. In E1 mode, the COMET-Quad generates framing for a basic G.704 E1 signal. The signaling multiframe alignment structure and the CRC multiframe structure may be optionally inserted. Framing can be optionally disabled.

Internal analog circuitry allows direct transmission of long haul and short haul T1 and E1 compatible signals using a minimum of external components. Typically, only line protection, a transformer and an optional line termination resistor are required. Digitally programmable pulse shaping allows transmission of DSX-1 compatible signals up to 655 feet from the cross-connect,

E1 short haul pulses into 120 ohm twisted pair or 75 ohm coaxial cable, E1 long haul pulses into 120 ohm twisted pair as well as long haul DS-1 pulses into 100 ohm twisted pair with integrated support for LBO filtering as required by the FCC rules. In addition, the programmable pulse shape extending over 5-bit periods allows customization of short haul and long haul line interface circuits to application requirements.

In the transmit path, the COMET-Quad supports signaling insertion, idle code substitution, digital milliwatt tone substitution, data inversion, and zero code suppression on a per-channel basis. Zero code suppression may be configured to Bell (bit 7), GTE, or DDS standards, and can also be disabled. Transmit side data and signaling trunk conditioning is also provided. Signaling bit transparency from the backplane may be enabled.

The COMET-Quad provides one transmit HDLC controller per channel. These controllers may be used for the transmission of messages on the ESF data link (T1) or national use bits (E1) and in any timeslot. In T1 mode, the COMET-Quad can be configured to generate in-band loop back codes and ESF bit oriented codes. In E1 mode, transmission of the 4-bit Sa codewords defined in ITU-T G.704 and ETSI 300-233 is supported.

To provide for V5 applications where up to three HDLC channels are contained in each E1, the COMET-Quad provides a CCS H-MVIP interface. This interface allows the HDLC channels to be extracted for external processing.

Each channel of the COMET-Quad can generate a low jitter transmit clock from a variety of clock references, and also provides jitter attenuation in the receive path. A low jitter recovered T1 clock can be routed outside the COMET-Quad for network timing applications.

Serial PCM interfaces to each T1 framer allow 1.544 Mbit/s backplane receive/backplane transmit system interfaces to be directly supported. Tolerance of gapped clocks allows other backplane rates to be supported with a minimum of external logic.

In synchronous backplane systems 8 Mbit/s H-MVIP interfaces are provided for access to channel associated signaling (CAS) and common channel signaling (CCS) for each T1 or E1. The CCS signaling H-MVIP interface is independent of the 64 Kbit/s channel and CAS H-MVIP access. The use of the H-MVIP interface requires that common clocks and frame pulse be used along with T1/E1 slip buffers.

The COMET-Quad is configured, controlled and monitored via a generic 8-bit microprocessor bus through which all internal registers are accessed. All sources of interrupts can be masked and acknowledged through the microprocessor interface.

PIN DIAGRAM

The COMET-Quad is packaged in a 208-pin PBGA package having a body size of 17mm by 17mm and a ball pitch of 1.0 mm. The center 16 balls are not used as signal I/Os and are thermal balls.

Figure 4 - Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	D (2)	D (1)	TXRING1 (1)	TAVD2 (1)	TAVD3 (1)	TAVD1 (1)	RXRING (1)	RVREF (1)	RAVS1 (2)	RAVD2 (2)	TXTIP2 (2)	TAVS3 (2)	TXTIP1 (2)	A (1)	A (3)	A (5)	A
B	D (3)	VSS33 (1)	D (0)	TXTIP1 (1)	TAVS3 (1)	TXTIP2 (1)	RAVD2 (1)	RAVD1 (1)	RAVD1 (2)	RAVS2 (2)	TXRING2 (2)	TAVS2 (2)	A (0)	A (2)	A (4)	A (6)	B
C	D (4)	D (5)	VDD33 (1)	TAVS2 (1)	TXCM (1)	TAVS1 (1)	RXTIP (1)	QAVD (1)	RVREF (2)	RXRING (2)	TAVD1 (2)	TAVD3 (2)	TXRING1 (2)	VSS33 (9)	A (7)	A (8)	C
D	VSS33 (2)	D (6)	D (7)	VDD33 (2)	TXRING2 (1)	RAVS2 (1)	RAVS1 (1)	RES (5)	QAVS (1)	RXTIP (2)	TAVS1 (2)	TXCM (2)	TAVD2 (2)	RDB	A (10)	A (9)	D
E	CASBRD_BRPCM (1)	BRCLK (1)	BRSIG (1)	BRFP (1)									RSTB	ALE	WRB	CSB	E
F	CMVFPC	CMVFPB	BTCLK (1)	CASBTD_BTPCM (1)									BRPCM (2)	VSS33 (5)	INTB	BRCLK (2)	F
G	VDDC25 (1)	VSSC25 (1)	BTSIG (1)	VSSQ33 (1)				GND	GND	GND	GND		VSSC25 (5)	BRFP (2)	BRSIG (2)	VDD33 (5)	G
H	VSSC25 (2)	VDDQ33 (1)	VDDC25 (2)	BTFP (1)				GND	GND	GND	GND		BTPCM (2)	BTFP (2)	VDDC25 (5)	BTCLK (2)	H
J	VDDC25 (3)	VSS33 (3)	VSSC25 (3)	RES[4]				GND	GND	GND	GND		XCLK	BTSIG (2)	RES[3]	VDDC25 (8)	J
K	MVBTD	CCSBTD	CMV8MCLK	VDD33 (3)				GND	GND	GND	GND		VSSQ33 (2)	VDDQ33 (2)	VDDC25 (6)	VSSC25 (6)	K
L	VDDC25 (4)	BTCLK (3)	VSSC25 (4)	MVBRD_CCSBRD									VSS33 (6)	RES[1]	VSSC25 (7)	CTCLK	L
M	BTFP (3)	VSS33 (8)	BTSIG (3)	BTPCM (3)									VDDC25 (7)	BTCLK (4)	BTSIG (4)	BTPCM (4)	M
N	BRCLK (3)	VDD33 (4)	RES[2]	TAVS2 (3)	TXRING2 (3)	RAVS2 (3)	RAVS1 (3)	CAVS	CAVD	RXTIP (4)	TAVS1 (4)	TXCM (4)	BTFP (4)	VDD33 (6)	BRPCM (4)	BRCLK (4)	N
P	BRPCM (3)	BRSIG (3)	TRSTB	TXTIP1 (3)	TXCM (3)	TAVS1 (3)	RXTIP (3)	RES (6)	RVREF (4)	RXRING (4)	TAVD1 (4)	TAVD3 (4)	TAVD2 (4)	VSS33 (7)	BRFP (4)	BRSIG (4)	P
R	BRFP (3)	VSS33 (4)	TMS	TXRING1 (3)	TAVS3 (3)	TXTIP2 (3)	RAVD2 (3)	RAVD1 (3)	RAVS1 (4)	RAVS2 (4)	TXRING2 (4)	TAVS2 (4)	TXTIP1 (4)	QAVD (2)	PIO	RSYNC	R
T	TDO	TCK	TDI	TAVD2 (3)	TAVD3 (3)	TAVD1 (3)	RXRING (3)	RVREF (3)	RAVD1 (4)	RAVD2 (4)	TXTIP2 (4)	TAVS3 (4)	TXRING1 (4)	QAVS (2)	RES (8)	RES (7)	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

208 PBGA

TOP VIEW

PIN DESCRIPTION

By convention, where a bus of four pins is present, the index indicates to which quadrant the pin applies. With BRCLK[1:4], for example, BRCLK[1] applies to quadrant #1, BRCLK[2] applies to quadrant #2, BRCLK[3] applies to quadrant #3, and BRCLK[4] applies to quadrant #4.

Pin Name	Type	Pin No.	Function
T1 and E1 System Side Serial Clock and Data Interface			
BRCLK[1] BRCLK[2] BRCLK[3] BRCLK[4]	I/O	E2 F16 N1 N16	**Backplane Receive Clocks (BRCLK[1:4]).** The Backplane Receive Clock, BRCLK[x], is used to update BRPCM[x] and BRSIG[x] and to either update or sample BRFP[x], depending on the direction of BRFP[x]. The active edge of BRCLK[x] for sampling/updating BRPCM[x], BRSIG[x], and BRFP[x] is configurable. In Receive Clock Master Mode, BRCLK[x] is configured as an output and can be either a 1.544 MHz or 2.048 MHz clock derived from the recovered line rate timing, with optional jitter attenuation. When in Receive Clock Master: Nx64Kbit/s mode, BRCLK[x] is gapped during the framing bit position (T1 mode only) and optionally for between 1 and 24 DS0 channels or 1 and 32 channel timeslots in the associated BRPCM[x] stream. When in Receive Clock Slave: Full T1/E1 mode, BRCLK[x] is configured as an input and is either a 1.544MHz clock in T1 mode or a 2.048MHz clock in T1 or E1 modes. BRCLK[x] is a nominal 1.544 or 2.048 MHz clock +/- 50ppm with a 50% duty cycle. When in Receive Clock Slave: H-MVIP mode, BRCLK[x] is configured as an input and is unused. In this mode, it is recommended that BRCLK[x] be connected via an external resistor to ground. After a reset, BRCLK[x] is configured as an input.
BRSIG[1] BRSIG[2] BRSIG[3] BRSIG[4]	Output	E3 G15 P2 P16	**Backplane Receive Signaling (BRSIG[1:4]).** Each BRSIG[x] contains the extracted channel associated signaling bits for each channel in the frame, repeated for the entire superframe. Each channel's associated signaling bits are valid in bit locations 5,6,7,8 of the channel and are channel-aligned with the BRPCM[x] data stream. When in Receive Clock Slave: H-MVIP mode, BRSIG[x] is unused and driven low. BRSIG[x] is updated on the active edge of BRCLK[x].

Pin Name	Type	Pin No.	Function
BRFP[1] BRFP[2] BRFP[3] BRFP[4]	I/O	E4 G14 R1 P15	**Backplane Receive Frame Pulse (BRFP[1:4]).** When the Receive Clock Master mode is active, BRFP[x] is configured as an output and indicates the frame alignment or the superframe alignment of the backplane receive stream, BRPCM[x]. BRFP[x] is updated on the active edge of BRCLK[x]. Receive Clock Master T1 mode: If basic frame alignment is desired, BRFP[x] pulses high for one BRCLK[x] cycle during bit 1 of each 193-bit frame. Optionally, BRFP[x] may pulse high every second frame to ease the identification of data link bits. If superframe alignment is desired, BRFP[x] pulses high for one BRCLK[x] cycle during bit 1 of frame 1 of every 12-frame or 24-frame superframe. Optionally, BRFP[x] may pulse high every second superframe to ease the conversion between SF and ESF. Receive Clock Master E1 mode: If basic frame alignment is desired, BRFP[x] pulses high for one BRCLK[x] cycle during bit 1 of each 256-bit frame. Optionally, BRFP[x] may pulse high every second frame to ease the identification of NFAS frames. If multiframe alignment is desired, BRFP[x] transitions high to mark bit 1 of frame 1 of every 16-frame signaling multiframe and transitions low following bit 1 of frame 1 of every 16-frame CRC multiframe. Note that if the signaling and CRC multiframe alignments are coincident, BRFP[x] pulses high for one BRCLK cycle every 16 frames. When the elastic store is enabled (Clock Slave mode is active on the backplane receive side), BRFP[x] is configured as an input and is used to frame align the backplane receive data to the system frame alignment. When frame alignment is required, a pulse at least 1 BRCLK[x] cycle wide must be provided on BRFP[x] a maximum of once every frame (193 bit times in T1, 256 bit times in E1). BRFP[x] is sampled on the active edge of BRCLK[x]. When in the Receive Clock Master: Clear Channel or Receive Clock Slave: H-MVIP mode, BRFP[x] is unused and it is recommended that BRFP[x] be configured as an input and be connected via an external resistor to ground. After a reset, BRFP[x] is configured as an input.

Pin Name	Type	Pin No.	Function
BRPCM[1] / CASBRD BRPCM[2] BRPCM[3] BRPCM[4]	Output	E1 F13 P1 N15	**Backplane Receive Data (BRPCM[1:4]).** Each BRPCM[x] signal contains the recovered data stream that may have been passed through the elastic store. When a Clock Slave backplane receive mode is active, the BRPCM[x] stream has passed through the elastic store and is aligned to the backplane receive timing. When in T1 Receive Clock Slave mode with BRCLK[x] configured as a 2.048MHz clock, the mapping of the BRPCM[x] data stream is configurable. In Receive Clock Slave: H-MVIP mode, BRPCM[2], BRPCM[3], and BRPCM[4] are unused and driven low. BRPCM[1] shares the same pin as the H-MVIP CAS signal CASBRD. In Receive Clock Slave: H-MVIP mode, the output becomes CASBRD. Out of reset, this output defaults to BRPCM[1]. When in Receive Clock Master: Clear Channel mode the unframed backplane receive data appears on BRPCM[x] with no frame alignment or signaling. BRPCM[x] update on the active edge of BRCLK[x].

Pin Name	Type	Pin No.	Function
BTCLK[1] BTCLK[2] BTCLK[3] BTCLK[4]	I/O	F3 H16 L2 M14	**Backplane Transmit Clock (BTCLK[1:4]).** The active edge of the Backplane Transmit Clock, BTCLK[x], is used to sample the associated BTSIG[x] and BTPCM[x], and is used to update BTFP[x]. The active edge is configured in the BTIF Configuration register. When a Transmit Clock Master mode is active, BTCLK[x] is an output and is a version of the transmit clock[x] which is generated from the receive recovered clock or the common transmit clock, CTCLK. When in T1 Transmit Clock Master: Nx64Kbit/s mode, BTCLK[x] is gapped during the framing bit position and optionally for between 1 and 23 DS0 channels in the associated BTPCM[x] stream. When in E1 Transmit Clock Master: Nx64Kbit/s mode, BTCLK[x] is gapped for between 1 and 31 channel timeslots in the associated BTPCM[x] stream. When in Transmit Clock Master: Clear Channel mode, the unframed backplane transmit data is sampled on BTPCM[x] with no frame alignment or signaling. When in a Transmit Clock Slave mode, BTCLK[x] is configured as an input and is used to time the backplane transmit interface. BTCLK[x] is either a 1.544MHz clock in T1 mode or a 2.048MHz clock in T1 or E1 modes. BTCLK[x] is a nominal 1.544 or 2.048 MHz clock +/- 50ppm with a 50% duty cycle. When in Transmit Clock Slave: H-MVIP mode, BTCLK[x] is configured as an input and is unused. In this mode, it is recommended that BTCLK[x] be connected via an external resistor to ground. After a reset, BTCLK[x] is configured as an input.
BTSIG[1] BTSIG[2] BTSIG[3] BTSIG[4]	Input	G3 J14 M3 M15	**Backplane Transmit Signaling (BTSIG[1:4]).** The BTSIG[x] input carries the signaling bits for each channel in the transmit data frame, repeated for the entire superframe. Each channel's signaling bits are in bit locations 5,6,7,8 of the channel and are channel-aligned with the BTPCM[x] data stream. BTSIG[x] is sampled on the configured active edge of BTCLK[x].

Pin Name	Type	Pin No.	Function
BTFP[1] BTFP[2] BTFP[3] BTFP[4]	I/O	H4 H14 M1 N13	**Backplane Transmit Frame Pulse (BTFP[1:4]).** When the Clock Master mode is active, BTFP[x] is configured as an output, transmit frame alignment is derived internally, and BTFP[x] is updated on the configured active edge of BTCLK[x]. BTFP[x] pulses high for one cycle to indicate the first bit of each frame or multiframe, as optioned. When the Transmit Clock Slave mode is active, BTFP[x] is configured as an input, and may be used to frame align the transmitters to the system backplane. T1 Transmit Clock Slave mode: If only frame alignment is required, a pulse at least one BTCLK[x] cycle wide must be provided on BTFP[x] at multiples of 193 bit periods. If superframe alignment is required, transmit superframe alignment must be enabled, and BTFP[x] must be brought high for at least one BTCLK[x] cycle to mark bit 1 of frame 1 of every 12-frame or 24-frame superframe. E1 Transmit Clock Slave mode: If basic frame alignment only is required, a pulse at least one BTCLK[x] cycle wide must be provided on BTFP[x] at multiples of 256 bit periods. If multiframe alignment is required, transmit multiframe alignment must be enabled, and BTFP[x] must be brought high to mark bit 1 of frame 1 of every 16-frame signaling multiframe and brought low following bit 1 of frame 1 of every 16-frame CRC multiframe. This mode allows both multiframe alignments to be independently controlled using the single BTFP[x] signal. Note that if the signaling and CRC multiframe alignments are coincident, BTFP[x] must pulse high for one BTCLK[x] cycle every 16 frames. When in Transmit Clock Slave: H-MVIP mode, BTFP[x] is configured as an input and is unused. In this mode, it is recommended that BTFP[x] be connected via an external resistor to ground. After a reset, BTFP[x] is configured as an input.

Pin Name	Type	Pin No.	Function
BTPCM[1] / CASBTD BTPCM[2] BTPCM[3] BTPCM[4]	Input	F4 H13 M4 M16	**Backplane Transmit Data (BTPCM[1:4]).** The non-return to zero, digital backplane transmit data streams to be transmitted are input on these pins. BTPCM[x] is sampled on the configured active edge of BTCLK[x]. BTPCM[2:4] are unused in Transmit Clock Slave: H-MVIP mode. BTPCM[1] shares the same pin as the Transmit Clock Slave: H-MVIP Channel Associated Signaling pin, CASBTD. By default this input is BTPCM[1].
MVIP System Side Interfaces			
MVBTD	Input	K1	**MVIP Backplane Transmit Data (MVBTD).** In Transmit Clock Slave: H-MVIP mode, the 8.192 Mbit/s backplane transmit data streams to be transmitted are input on MVBTD. MVBTD carries the channels of four complete T1's or E1's formatted according to the H-MVIP standard. MVBTD carries the backplane transmit data equivalent to BTPCM[1:4]. MVBTD is aligned to the common H-MVIP 16.384 MHz clock, CMV8MCLK, the 4.096 MHz frame pulse clock, CMVFPC, and frame pulse, CMVFPB. MVBTD is sampled on every second rising edge of MV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. When not in Transmit Clock Slave: H-MVIP mode, MVBTD is unused.
CASBTD / BTPCM[1]	Input	F4	**Channel Associated Signaling Backplane Transmit Data (CASBTD).** CASBTD carries the Channel Associated Signaling (CAS) stream to be transmitted in the T1 DS0s or E1 timeslots. CASBTD signal carries CAS for four complete T1's or E1's formatted according to the H-MVIP standard. CASBTD carries the corresponding CAS values of the channel data carried in MVBTD. CASBTD is aligned to the common H-MVIP 16.384MHz clock, CMV8MCLK, the 4.096 MHz frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CASBTD is sampled on every second rising edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. CASBTD shares the same pin as BTPCM[1]. In Transmit Clock Slave: H-MVIP Mode, this input is CASBTD. In all other Transmit modes, this input is BTPCM[1].

Pin Name	Type	Pin No.	Function
CCSBTD	Input	K2	**Common Channel Signaling Backplane Transmit Data (CCSBTD).** In T1 mode, CCSBTD carries the common channel signaling to be transmitted in timeslot 24 of each of the 4 T1's. In E1 mode, CCSBTD carries up to 3 timeslots (15,16, 31) to be transmitted in each of the 4 E1's. CCSBTD is formatted according to the H-MVIP standard. CCSBTD is aligned to the common H-MVIP 16.384 MHz clock, CMV8MCLK, the 4.096 MHz frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CCSBTD is sampled on every second rising edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. CCSBTD can be optionally enabled in either Transmit Clock Slave: Full T1/E1 mode or Transmit Clock Slave: H-MVIP mode. In other modes, CCSBTD is unused.
CMV8MCLK	Input	K3	**Common 8M H-MVIP Clock (CMV8MCLK).** The Common 8.192 Mbit/s H-MVIP Data Clock, CMV8MCLK, provides the data clock for receive and transmit links configured for operation in 8.192 Mbit/s H-MVIP mode. CMV8MCLK is used to sample data on MVBRD, MVBTD, CASBRD, CASBTD, CCSBRD and CCSBTD. CMV8MCLK is nominally a 50% duty cycle clock with a frequency of 16.384 MHz. The Transmitter and Receiver streams are independently enabled for H-MVIP access. When enabled, all four Transmitter (or Receiver) streams are enabled for H-MVIP access. When both the Transmitter and the Receiver H-MVIP accesses are disabled, CMV8MCLK is unused.
CMVFPB	Input	F2	**Common H-MVIP Frame Pulse (CMVFPB).** The active low Common H-MVIP Frame Pulse, CMVFPB, for 8.192 Mbit/s H-MVIP signals references the beginning of each frame for links operating in 8.192 Mbit/s H-MVIP mode. The CMVFPB frame pulse occurs every 125us and is sampled on the falling edge of CMVFPC. The Transmitter and Receiver streams are independently enabled for H-MVIP access. When enabled, all four Transmitter (or Receiver) streams are enabled for H-MVIP access. When both the Transmitter and the Receiver H-MVIP accesses are disabled, CMVFPB is unused.

Pin Name	Type	Pin No.	Function
MVBRD /	Output	L4	**H-MVIP Backplane Receive Data (MVBRD).** MVBRD carries the recovered T1 or E1 channels that have passed through the elastic store. Each MVBRD signal carries the channels of four complete T1's or E1's. MVBRD carries the T1 or E1 data equivalent to BRPCM[1:4]. MVBRD is aligned to the common H-MVIP 16.384 MHz clock, CMV8MCLK, frame pulse clock, CMVFPC, and frame pulse, CMVFPB. MVBRD is updated on every second rising edge of the common H-MVIP 16.384 MHz clock, CMV8MCLK, as fixed by the common H-MVIP frame pulse clock, CMVFPC.
CCSBRD			**Common Channel Signaling Backplane Receive Data (CCSBRD).** In T1 mode, CCSBRD carries the Common Channel Signaling (CCS) channels extracted from each of the 4 T1's. In E1 mode, CCSBRD carries up to 3 timeslots (15,16, 31) from each of the 4 E1's. CCSBRD is formatted according to the H-MVIP standard. CCSBRD is aligned to the common H-MVIP 16.384 MHz clock, CMV8MCLK, the 4.096 MHz frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CCSBRD is updated on every second rising edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. CCSBRD shares the same pin as MVBRD. In Receive Clock Slave: H-MVIP mode, this output is MVBRD. In Receive Clock Slave: Full T1/E1 mode, CCSBRD can be optionally enabled. In all other modes, this output is unused.
CASBRD / BRPCM[1]	Output	E1	**Channel Associated Signaling Backplane Receive Data (CASBRD).** CASBRD carries the Channel Associated Signaling (CAS) stream extracted from all the T1 or E1 channels. CASBRD carries CAS for four complete T1's or E1's. CASBRD carries the corresponding CAS values of the channel carried in MVBRD. CASBRD is aligned to the common H-MVIP 16.384 MHz clock, CMV8MCLK, the 4.096 MHz frame pulse clock, CMVFPC, and frame pulse, CMVFPB. CASBRD is updated on every second rising edge of CMV8MCLK as fixed by the common H-MVIP frame pulse clock, CMVFPC. CASBRD shares the same pin as BRPCM[1]. In Receive Clock Slave: H-MVIP mode, this input is CASBRD. In all other modes, this input is BRPCM[1]. By default this input is BRPCM[1].

Pin Name	Type	Pin No.	Function
CMVFPC	Input	F1	**Common H-MVIP Frame Pulse Clock (CMVFPC).** The common 8.192 Mbit/s H-MVIP frame pulse clock provides the frame pulse clock for operation with 8.192 Mbit/s H-MVIP access. CMVFPC is used to sample CMVFPB. CMVFPC is nominally a 50% duty cycle clock with a frequency of 4.096 MHz. The falling edge of CMVFPC must be aligned with the falling edge of CMV8MCLK with no more than ±10ns skew. The Transmitter and Receiver streams are independently enabled for H-MVIP access. When H-MVIP access is enabled, all four Transmitter (or Receiver) streams are enabled for H-MVIP access. When both the Transmitter and the Receiver H-MVIP accesses are disabled, CMVFPC is unused.
Transmit Line Interface			
TXTIP1[1] TXTIP1[2] TXTIP1[3] TXTIP1[4] TXTIP2[1] TXTIP2[2] TXTIP2[3] TXTIP2[4]	Analog Output	B4 A13 P4 R13 B6 A11 R6 T11	**Transmit Analog Positive Pulse (TXTIP1[1:4] and TXTIP2[1:4]).** When the transmit analog line interface is enabled, the TXTIP1 and TXTIP2 analog outputs drive the transmit line pulse signal through an external matching transformer. Both TXTIP1 and TXTIP2 are normally connected to the positive lead of the transformer primary. Two outputs are provided for better signal integrity and must be shorted together on the board. After a reset, TXTIP1 and TXTIP2 are high impedance.
TXRING1[1] TXRING1[2] TXRING1[3] TXRING1[4] TXRING2[1] TXRING2[2] TXRING2[3] TXRING2[4]	Analog Output	A3 C13 R4 T13 D5 B11 N5 R11	**Transmit Analog Negative Pulse (TXRING1[1:4] and TXRING2[1:4]).** When the transmit analog line interface is enabled, the TXRING1 and TXRING2 analog outputs drive the transmit line pulse signal through an external matching transformer. Both TXRING1 and TXRING2 are normally connected to the negative lead of the transformer primary. Two outputs are provided for better signal integrity and must be shorted together on the board. After a reset, TXRING1 and TXRING2 are high impedance.
TXCM[1] TXCM[2] TXCM[3] TXCM[4]	Analog I/O	C5 D12 P5 N12	**Transmit Common Mode (TXCM[1:4]).** This pin is the common mode for the Transmit analog. It requires a 4.7µF capacitor to analog ground and two 12.7Ω resistors to the corresponding TXRING and TXTIP.

Pin Name	Type	Pin No.	Function
Receive Line Interface			
RXTIP[1] RXTIP[2] RXTIP[3] RXTIP[4]	Analog Input	C7 D10 P7 N10	**Receive Analog Positive Pulse (RXTIP[1:4]).** When the analog receive line interface is enabled, RXTIP samples the received line pulse signal from an external isolation transformer. RXTIP is normally connected directly to the positive lead of the receive transformer secondary.
RVREF[1] RVREF[2] RVREF[3] RVREF[4]	Analog I/O	A8 C9 T8 P9	**Receive Voltage Reference (RVREF[1:4]).** This pin must be connected to an external RC network consisting of a 100 kΩ resistor connected in parallel with a 10 nF capacitor to analog ground.
RXRING[1] RXRING[2] RXRING[3] RXRING[4]	Analog Input	A7 C10 T7 P10	**Receive Analog Negative Pulse (RXRING[1:4]).** When the analog receive line interface is enabled, RXRING samples the received line pulse signal from an external isolation transformer. RXRING is normally connected directly to the negative lead of the receive transformer secondary.
Timing Options Control			
XCLK	Input	J13	**Crystal Clock Input (XCLK).** This signal provides a stable, global timing reference for the COMET-Quad internal circuitry via an internal clock synthesizer. XCLK is a nominally jitter free clock at 1.544 MHz in T1 mode and 2.048 MHz in E1 mode. In T1 mode, a 2.048 MHz clock may be used as a reference. When used in this way, however, the intrinsic jitter specifications to AT&T TR62411 may not be met.
CTCLK	Input	L16	**Common Transmit Clock (CTCLK).** This input signal is used as a reference transmit clock which can be used in backplane transmit Clock Master modes. Depending on the configuration of the COMET-Quad, CTCLK may be a 12.352 MHz or 16.384 MHz clock (so the transmit clock is generated by dividing CTCLK by 8), or a line rate clock (so the transmit clock is generated directly from CTCLK, or from CTCLK after jitter attenuation), or a multiple of 8kHz (Nx8khz, where 1≤N≤256) so long as CTCLK is jitter-free when divided down to 8kHz (in which case the transmit clock is derived by the JAT PLL using CTCLK as a reference). The COMET-Quad may be configured to ignore the CTCLK input and utilize the Receive recovered clock, or each channel's backplane transmit clock BTCLK[x]. Receive recovered clock[x] is automatically substituted for CTCLK if line loopback is enabled.

Pin Name	Type	Pin No.	Function
RSYNC	Output	R16	**Recovered Clock Synchronization Signal (RSYNC).** This output signal is the recovered receiver line rate clock (1.544 or 2.048 MHz) of one of the four T1 or E1 channels or, optionally, the recovered clock synchronously divided by 193 (T1 mode) or 256 (E1 mode) to create a 8 kHz timing reference signal. When 8 kHz, the RSYNC phase is independent of frame alignment and is not affected by framing events. The default is to source RSYNC from COMET quadrant #1. When the COMET-Quad is in a loss of signal state, RSYNC is derived from the XCLK input or, optionally, is held high.
PIO	I/O	R15	**Programmable I/O (PIO).** PIO is an input/output pin controlled by a COMET-Quad register bit. When configured as an output, the PIO pin can, under software control, be used to configure external circuitry. When configured as an input, a COMET-Quad register bit reflects the state of the PIO pin.
RES[1] RES[2] RES[3] RES[4] RES[8]	Output	L14 N3 J15 J4 T15	**Reserved (RES[1:4], RES[8]).** Reserved for COMET-Quad production test. These pins must be left unconnected.
RES[5] RES[6]	Analog I/O	D8 P8	**Reserved (RES[5:6]).** Reserved for COMET-Quad production test. These pins must be connected to an analog ground.
RES[7]	Input	T16	**Reserved (RES[7]).** Reserved for COMET-Quad production test. This pin must be tied low.
Microprocessor Interface			
A[0] A[1] A[2] A[3] A[4] A[5] A[6] A[7] A[8] A[9] A[10]	Input	B13 A14 B14 A15 B15 A16 B16 C15 C16 D16 D15	**Address Bus (A[10:0]).** This bus selects specific registers during COMET-Quad register accesses. Signal A[10] selects between normal mode and test mode register access. A[10] has an internal pull down resistor. In PMC production testing mode, A[9] and A[8] are replaced with values from the Master Test Control register.

Pin Name	Type	Pin No.	Function
RDB	Input	D14	**Active Low Read Enable (RDB).** This signal is low during COMET-Quad register read accesses. The COMET-Quad drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are low.
WRB	Input	E15	**Active Low Write Strobe (WRB).** This signal is low during a COMET-Quad register write access. The D[7:0] bus contents are clocked into the addressed register on the rising WRB edge while CSB is low.
CSB	Input	E16	**Active Low Chip Select (CSB).** CSB must be low to enable COMET-Quad register accesses. CSB must go high at least once after power up to clear internal test modes. If CSB is not used, it should be tied to an inverted version of RSTB, in which case, RDB and WRB determine register accesses.
ALE	Input	E14	**Address Latch Enable (ALE).** This signal is active high and latches the address bus contents, A[10:0], when low. When ALE is high, the internal address latches are transparent. ALE allows the COMET-Quad to interface to a multiplexed address/data bus. The ALE input has an internal pull up resistor.
INTB	Output OD	F15	**Active low Open-Drain Interrupt (INTB).** This signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source at which time, INTB will tristate.
RSTB	Input	E13	**Active Low Reset (RSTB).** This signal provides an asynchronous COMET-Quad reset. RSTB is a Schmidt triggered input with an internal pull up resistor.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	B3 A2 A1 B1 C1 C2 D2 D3	**Bidirectional Data Bus (D[7:0]).** This bus provides COMET-Quad register read and write accesses.
JTAG Interface			

Pin Name	Type	Pin No.	Function
TDO	Output	T1	**Test Data Output (TDO).** This signal carries test data out of the COMET-Quad via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tri-state output that is tri-stated except when scanning of data is in progress.
TDI	Input	T3	**Test Data Input (TDI).** This signal carries test data into the COMET-Quad via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull up resistor.
TCK	Input	T2	**Test Clock (TCK).** This signal provides timing for test operations that can be carried out using the IEEE P1149.1 test access port.
TMS	Input	R3	**Test Mode Select (TMS).** This signal controls the test operations that can be carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull up resistor.
TRSTB	Input	P3	**Active low Test Reset (TRSTB).** This signal provides an asynchronous COMET-Quad test access port reset via the IEEE P1149.1 test access port. TRSTB is a Schmidt triggered input with an internal pull up resistor. TRSTB must be asserted during the power up sequence. Note that if not used, TRSTB must be connected to the RSTB input.
Analog Power and Ground Pins			
TAVD1[1] TAVD1[2] TAVD1[3] TAVD1[4]	Analog Power	A6 C11 T6 P11	**Transmit Analog Power (TAVD1[1:4]).** TAVD1 provides power for the transmit LIU reference circuitry. TAVD1 should be connected to analog +3.3 V.
TAVD2[1] TAVD2[2] TAVD2[3] TAVD2[4] TAVD3[1] TAVD3[2] TAVD3[3] TAVD3[4]	Analog Power	A4 D13 T4 P13 A5 C12 T5 P12	**Transmit Analog Power (TAVD2[1:4], TAVD3[1:4]).** TAVD2 and TAVD3 supply power for the transmit LIU output drivers. TAVD2 and TAVD3 should be connected to analog +3.3 V.
CAVD	Analog Power	N9	**Clock Synthesis Unit Analog Power (CAVD).** CAVD supplies power for the transmit clock synthesis unit. CAVD should be connected to analog +3.3 V.

Pin Name	Type	Pin No.	Function
TAVS1[1] TAVS1[2] TAVS1[3] TAVS1[4]	Analog Ground	C6 D11 P6 N11	**Transmit Analog Ground (TAVS1[1:4]).** TAVS1 provides ground for the transmit LIU reference circuitry. TAVS1 should be connected to analog GND.
TAVS2[1] TAVS2[2] TAVS2[3] TAVS2[4] TAVS3[1] TAVS3[2] TAVS3[3] TAVS3[4]	Analog Ground	C4 B12 N4 R12 B5 A12 R5 T12	**Transmit Analog Ground (TAVS2[1:4], TAVS3[1:4]).** TAVS2 and TAVS3 supply ground for the transmit LIU output drivers. TAVS2 and TAVS3 should be connected to analog GND.
CAVS	Analog Ground	N8	**Clock Synthesis Unit Analog Ground (CAVS).** CAVS supplies ground for the transmit clock synthesis unit. CAVS should be connected to analog GND.
RAVD1[1] RAVD1[2] RAVD1[3] RAVD1[4]	Analog Power	B8 B9 R8 T9	**Receive Analog Power (RAVD1[1:4]).** RAVD1 supplies power for the receive LIU input equalizer. RAVD1 should be connected to analog +3.3 V.
RAVD2[1] RAVD2[2] RAVD2[3] RAVD2[4]	Analog Power	B7 A10 R7 T10	**Receive Analog Power (RAVD2[1:4]).** RAVD2 supplies power for the receive LIU peak detect and slicer. RAVD2 should be connected to analog +3.3 V.
RAVS1[1] RAVS1[2] RAVS1[3] RAVS1[4]	Analog Ground	D7 A9 N7 R9	**Receive Analog Ground (RAVS1[1:4]).** RAVS1 supplies ground for the receive LIU input equalizer. RAVS1 should be connected to analog GND.
RAVS2[1] RAVS2[2] RAVS2[3] RAVS2[4]	Analog Ground	D6 B10 N6 R10	**Receive Analog Ground (RAVS2[1:4]).** RAVS2 supplies ground for the receive LIU peak detect and slicer. RAVS2 should be connected to analog GND.
QAVD[1] QAVD[2]	Analog Power	C8 R14	**Quiet Analog Power (QAVD).** QAVD supplies power for the core analog circuitry. QAVD should be connected to analog +3.3 V.
QAVS[1] QAVS[2]	Analog Ground	D9 T14	**Quiet Analog Ground (QAVS).** QAVS supplies ground for the core analog circuitry. QAVS should be connected to analog GND.

Pin Name	Type	Pin No.	Function
Digital Power and Ground Pins			
VDDC25[1] VDDC25[2] VDDC25[3] VDDC25[4] VDDC25[5] VDDC25[6] VDDC25[7] VDDC25[8]	Power	G1 H3 J1 L1 H15 K15 M13 J16	**Core Power (VDDC25[1:8]).** The VDDC25[1:8] pins should be connected to a well decoupled +2.5V DC power supply.
VSSC25[1] VSSC25[2] VSSC25[3] VSSC25[4] VSSC25[5] VSSC25[6] VSSC25[7] GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND	Ground	G2 H1 J3 L3 G13 K16 L15 G7 G8 G9 G10 H7 H8 H9 H10 J7 J8 J9 J10 K7 K8 K9 K10	**Core Ground (VSSC25[1:7]).** The VSSC25[1:7] pins should be connected to GND. The 16 thermal balls should also be connected to GND.
VDDQ33[1] VDDQ33[2]	Power	H2 K14	**Quiet Power (VDDQ33[1:2]).** The VDDQ33[1:2] pins should be connected to a well decoupled +3.3V DC power supply.
VSSQ33[1] VSSQ33[2]	Ground	G4 K13	**Quiet Ground (VSSQ33[1:2]).** The VSSQ33[1:2] pins should be connected to GND.

Pin Name	Type	Pin No.	Function
VDD33[1] VDD33[2] VDD33[3] VDD33[4] VDD33[5] VDD33[6]	Power	C3 D4 K4 N2 G16 N14	**Switching Power (VDD33[1:6]).** The VDD33[1:6] pins should be connected to a well decoupled +3.3V DC power supply.
VSS33[1] VSS33[2] VSS33[3] VSS33[4] VSS33[5] VSS33[6] VSS33[7] VSS33[8] VSS33[9]	Ground	B2 D1 J2 R2 F14 L13 P14 M2 C14	**Switching Ground (VSS33[1:9]).** The VSS33[1:9] pins should be connected to GND.

NOTES ON PIN DESCRIPTIONS:

1. All COMET-Quad inputs and bi-directionals present minimum capacitive loading.
2. All COMET-Quad inputs and bi-directionals, when configured as inputs, tolerate TTL logic levels.
3. All COMET-Quad outputs and bi-directionals have at least 2 mA drive capability. The data bus outputs, D[7:0], the INTB output, and the BRCLK[4:1] and BTCLK[4:1] outputs have 4 mA drive capability. The transmit analog outputs (TXTIP and TXRING) have built-in short circuit current limiting.
4. Inputs RSTB, ALE, TMS, TDI and TRSTB have internal pull-up resistors.
5. Bi-directional VCLK has an internal pull-up resistor
6. Inputs A[10] and PIO have internal pull-down resistors.
7. All unused inputs should be connected to GROUND.
8. The VSS33 and VSSC25 pins be connected to a common GROUND Plane.
9. Power to the 3.3 V power pins should be applied *before* power to the 2.5 V pins is applied. Similarly, power to the 2.5 V pins should be removed *before* power to the 3.3V pins is removed.
10. VDD33 and VDDQ should not be allowed to drop below the VDD25 voltage level except when VDD25 is not powered.

FUNCTIONAL DESCRIPTION

1.3 Receive Interface

The analog receive interface is configurable to operate in both E1 and T1 short-haul and long-haul applications. Short-haul T1 is defined as transmission over less than 655 ft of cable. Short-haul E1 is defined as transmission on any cable that attenuates the signal by less than 6 dB.

For long-haul signals, unequalized long- or short-haul bipolar alternate mark inversion (AMI) signals are received as the differential voltage between the RXTIP and RXRING inputs. The COMET-Quad typically accepts unequalized signals that are attenuated by 36 dB for both T1 and E1 signals and are non-linearly distorted by typical cables.

For short-haul, the slicing threshold is set to a fraction of the input signal's peak amplitude, and adapts to changes in this amplitude. The slicing threshold is programmable, but is typically 67% and 50% for DSX-1 and E1 applications, respectively. Abnormally low input signals are detected when the input level is below a programmable threshold, which is typically 140 mV for E1 and 105 mV for T1.

Figure 5 - External Analog Interface Circuits

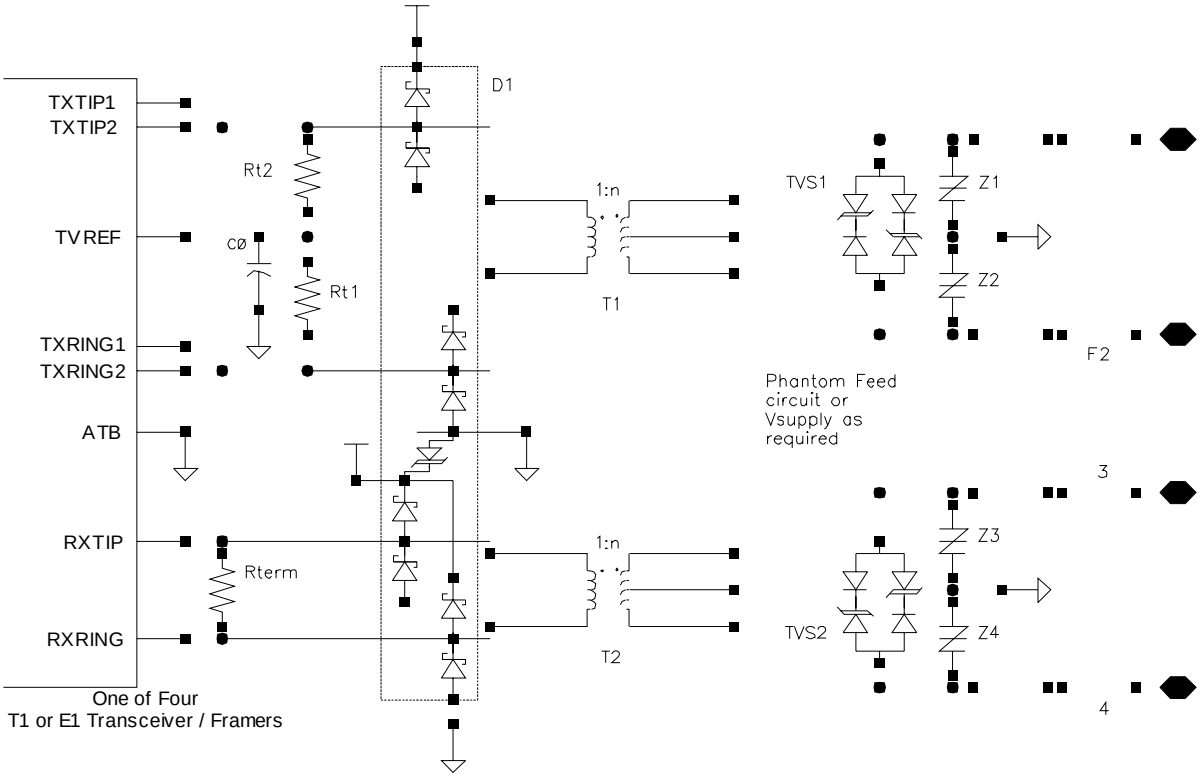


Figure 5 gives the recommended external protection circuitry for designs required to meet the major surge immunity and electrical safety standards including FCC Part 68, UL1449, and Bellcore TR-NWT-001089. This circuit has not been tested as of December, 1999. Please refer to an upcoming PMC application note for more details.

For systems not requiring phantom feed or inter-building line protection, the Bi-directional Transient Surge Suppressors (Z1-Z4), their associated ground connection and the center tap of the transformer can be removed from the circuit.

See Table 1 for the descriptions of components for Figure 5. See Table 2 for the descriptions of values for the transformer turns ratio, n, Rt1 and Rt2 for Figure 5.

Note that the crowbar devices (Z1 – Z4) are not required if the transformer's isolation rating is not exceeded.

Table 1: - External Component Descriptions

Component	Description	Part #	Source
Rt1 & Rt2	Typically 12.7Ω ±1% Resistors (see Table 2)		
Rterm	18.2Ω ±1% Resistor for T1 & 120Ω E1 13Ω ±1% Resistor for 75Ω E1 (assuming a 1:2.42 transformer)		
C0 & C1	4.7µF±10% Capacitors		
F1 – F4	1 Amp, 600V Fuses		
Rf1 – Rf4	2Ω ±1%, 2W, Resistors		
TVS1 & TVS2	6V Bi-directional Transient Voltage Suppressor Diode	LC01-6	Semtech
D1	Surge Protector Diode Array	SRDA3.3-4	Semtech
Z1 – Z4	Bi-directional Transient Surge Suppressors	SGT27B13	Harris
T1 & T2	Generally 1:2.42CT Transformers (see Table 2)	50436 (single) T1137 (dual) TG23-1505NS (single) TG23-1505N1 (dual)	Midcom Pulse Halo Halo
T3 & T4	Generally 1:2.42CT Transformers with center taps floating (see Table 2)	50436 (single) T1137 (dual) TG23-1505NS (single) TG23-1505N1 (dual)	Midcom Pulse Halo Halo

Table 2 : - Termination Resistors, Transformer Ratios and TRL

Case	n	Rt1	Rt2	Typical TRL
SH T1: Zo=100Ω	1:2.42	12.7Ω ±1%	12.7Ω ±1%	14.1dB
SH E1: Zo=120Ω	1:2.42	12.7Ω ±1%	12.7Ω ±1%	19.4dB
SH E1: Zo=75Ω SH E1: Zo=75Ω[1]	1:2.42 1:2.42[1]	12.7Ω ±1% 8.06Ω ±1%	12.7Ω ±1% 8.06Ω ±1%	9.6dB 18.8dB
LH T1 LBO=0dB: Zo=100Ω	1:2.42	12.7Ω ±1%	12.7Ω ±1%	14.1dB
LH T1 LBO=-7.5dB: Zo=100Ω	1:2.42	12.7Ω ±1%	12.7Ω ±1%	14.1dB
LH T1 LBO=-15dB: Zo=100Ω	1:2.42	12.7Ω ±1%	12.7Ω ±1%	14.1dB
LH T1 LBO=-22.5dB: Zo=100Ω	1:2.42	12.7Ω ±1%	12.7Ω ±1%	14.1dB

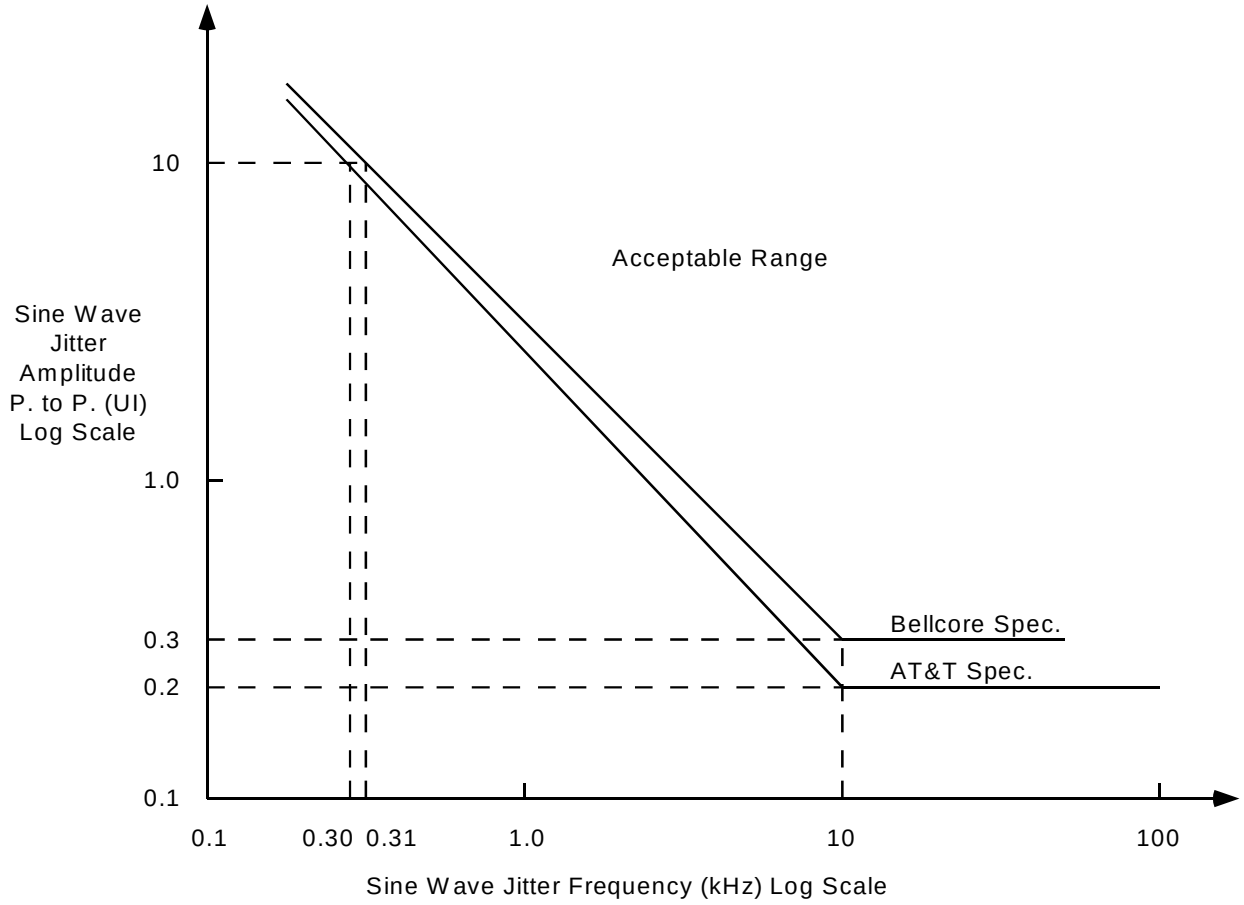
Notes:
1) Headroom power is about 30% higher in this case.

1.4 Clock and Data Recovery (CDRC)

The Clock and Data Recovery function is provided by the Clock and Data Recovery (CDRC) block. The CDRC provides clock and PCM data recovery, B8ZS and HDB3 decoding, line code violation detection, and loss of signal detection. It recovers the clock from the incoming RZ data pulses using a digital phase-locked-loop and reconstructs the NRZ data. Loss of signal is indicated after a programmable threshold of consecutive bit periods of the absence of pulses on both the positive and negative line pulse inputs and is cleared after the occurrence of a single line pulse. An alternate loss of signal indication is provided which is cleared upon meeting an 1-in-8 pulse density criteria for T1 and a 1-in-4 pulse density criteria for E1. If enabled, a microprocessor interrupt is generated when a loss of signal is detected and when the signal returns. A line code violation is defined as a bipolar violation (BPV) for AMI-coded signals, is defined as a BPV that is not part of a zero substitution code for B8ZS-coded signals, and is defined as a bipolar violation of the same polarity as the last bipolar violation for HDB3-coded signals.

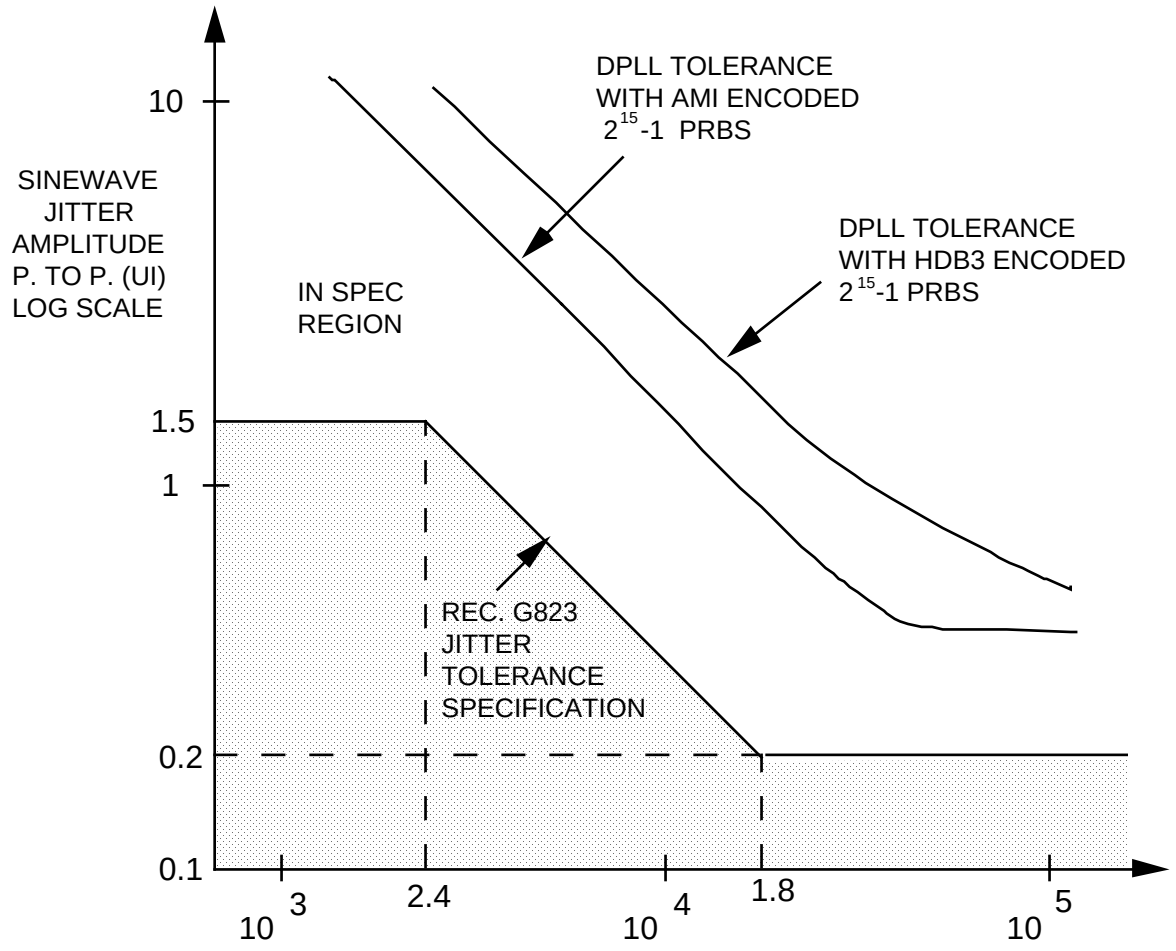
In T1 mode, the input jitter tolerance of the COMET-Quad complies with the Bellcore Document TA-TSY-000170 and with the AT&T specification TR62411, as shown in Figure 6. The tolerance is measured with a QRSS sequence (2^{20}-1 with 14 zero restriction). The CDRC block provides two algorithms for clock recovery that result in differing jitter tolerance characteristics. The first algorithm (when the ALGSEL register bit is logic 0) provides good low frequency jitter tolerance, but the high frequency tolerance is close to the TR62411 limit. The second algorithm (when ALGSEL is logic 1) provides much better high frequency jitter tolerance at the expense of the low frequency tolerance; the low frequency tolerance of the second algorithm is approximately 80% that of the first algorithm.

Figure 6: - T1 Jitter Tolerance



For E1 applications, the input jitter tolerance complies with the ITU-T Recommendation G.823 "The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy." Figure 7 illustrates this specification and the performance of the phase-locked loop when the ALGSEL register bit is logic 0.

Figure 7: - Compliance with ITU-T Specification G.823 for E1 Input Jitter



1.5 Receive Jitter Attenuator (RJAT)

The Receive Jitter Attenuator (RJAT) digital PLL attenuates the jitter present on the RXTIP/RXRING inputs. The attenuation is only performed when the RJATEN register bit is a logic 1.

The jitter characteristics of the Receive Jitter Attenuator (RJAT) are the same as the Transmit Jitter Attenuator (TJAT).

1.6 T1 Inband Loopback Code Detector (IBCD)

The T1 Inband Loopback Code Detection function is provided by the IBCD block. This block detects the presence of either of two programmable INBAND LOOPBACK ACTIVATE and

DEACTIVATE code sequences in either framed or unframed data streams. Each INBAND LOOPBACK code sequence is defined as the repetition of the programmed code in the PCM stream for at least 5.1 seconds. The code sequence detection and timing is compatible with the specifications defined in T1.403-1993, TA-TSY-000312, and TR-TSY-000303. LOOPBACK ACTIVATE and DEACTIVATE code indication is provided through internal register bits. An interrupt is generated to indicate when either code status has changed.

1.7 T1 Pulse Density Violation Detector (PDVD)

The Pulse Density Violation Detection function is provided by the PDVD block. The block detects pulse density violations of the requirement that there be N ones in each and every time window of 8(N+1) data bits (where N can equal 1 through 23). The PDVD also detects periods of 16 consecutive zeros in the incoming data. Pulse density violation detection is provided through an internal register bit. An interrupt is generated to signal a 16 consecutive zero event, and/or a change of state on the pulse density violation indication.

1.8 T1 Framer (T1-FRMR)

The T1 framing function is provided by the T1-FRMR block. This block searches for the framing bit position in the backplane receive stream. It works in conjunction with the FRAM block to search for the framing bit pattern in the standard superframe (SF), or extended superframe (ESF) framing formats. When searching for frame, the FRMR simultaneously examines each of the 193 (SF) or each of the 772 (ESF) framing bit candidates. The FRAM block is addressed and controlled by the FRMR while frame synchronization is acquired.

The time required to acquire frame alignment to an error-free backplane receive stream, containing randomly distributed channel data (i.e. each bit in the channel data has a 50% probability of being 1 or 0), is dependent upon the framing format. For SF format, the T1-FRMR block will determine frame alignment within 4.4ms 99 times out of 100. For ESF format, the T1-FRMR will determine frame alignment within 15 ms 99 times out of 100.

Once the T1-FRMR has found frame, the backplane receive data is continuously monitored for framing bit errors, bit error events (a framing bit error in SF or a CRC-6 error in ESF), and severely errored framing events. The T1-FRMR also detects out-of-frame, based on a selectable ratio of framing bit errors.

The T1-FRMR can also be disabled to allow reception of unframed data.

1.9 E1 Framer (E1-FRMR)

The E1 framing function is provided by the E1-FRMR block. The E1-FRMR block searches for basic frame alignment, CRC multiframe alignment, and channel associated signaling (CAS) multiframe alignment in the incoming recovered PCM stream.

Once the E1-FRMR has found basic (or FAS) frame alignment, the incoming PCM data stream is continuously monitored for FAS/NFAS framing bit errors. Framing bit errors are accumulated in the framing bit error counter contained in the PMON block. Once the E1-FRMR has found CRC

multiframe alignment, the PCM data stream is continuously monitored for CRC multiframe alignment pattern errors, and CRC-4 errors. CRC-4 errors are accumulated in the CRC error counter of the PMON block. Once the E1-FRMR has found CAS multiframe alignment, the PCM data is continuously monitored for CAS multiframe alignment pattern errors. The E1-FRMR also detects and indicates loss of basic frame, loss of CRC multiframe, and loss of CAS multiframe, based on user-selectable criteria. The reframe operation can be initiated by software (via the E1-FRMR Frame Alignment Options Register), by excessive CRC errors, or when CRC multiframe alignment is not found within 400 ms. The E1-FRMR also identifies the position of the frame, the CAS multiframe, and the CRC multiframe.

The E1-FRMR extracts the contents of the International bits (from both the FAS frames and the NFAS frames), the National bits, and the Extra bits (from timeslot 16 of frame 0 of the CAS multiframe), and stores them in the E1-FRMR International/National Bits register and the E1-FRMR Extra Bits register. Moreover, the FRMR also extracts submultiframe-aligned 4-bit codewords from each of the National bit positions Sa4 to Sa8, and stores them in microprocessor-accessible registers that are updated every CRC submultiframe.

The E1-FRMR identifies the raw bit values for the Remote (or distant frame) Alarm (bit 3 in timeslot 0 of NFAS frames) and the Remote Signaling Multiframe (or distant multiframe) Alarm (bit 6 of timeslot 16 of frame 0 of the CAS multiframe) via the E1-FRMR International/National Bits Register, and the E1-FRMR Extra Bits Register respectively. Access is also provided to the "debounced" remote alarm and remote signaling multiframe alarm bits which are set when the corresponding signals have been a logic 1 for 2 or 3 consecutive occurrences, as per Recommendation O.162. Detection of AIS and timeslot 16 AIS are provided. AIS is also integrated, and an AIS Alarm is indicated if the AIS condition has persisted for at least 100 ms. The out of frame (OOF=1) condition is also integrated, indicating a Red Alarm if the OOF condition has persisted for at least 100 ms.

An interrupt may be generated to signal a change in the state of any status bits (OOF, OOSMF, OOCMF, AIS or RED), and to signal when any event (RAI, RMAI, AISD, TS16AISD, COFA, FER, SMFER, CMFER, CRCE or FEBE) has occurred. Additionally, interrupts may be generated every frame, CRC submultiframe, CRC multiframe or signaling multiframe.

Basic Frame Alignment Procedure

The E1-FRMR searches for basic frame alignment using the algorithm defined in ITU-T Recommendation G.706 sections 4.1.2 and 4.2.

The algorithm finds frame alignment by using the following sequence:

1. Search for the presence of the correct 7-bit FAS (‘0011011’);

2. Check that the FAS is absent in the following frame by verifying that bit 2 of the assumed non-frame alignment sequence (NFAS) TS 0 byte is a logic 1;

3. Check that the correct 7-bit FAS is present in the assumed TS 0 byte of the next frame.

If either of the conditions in steps 2 or 3 are not met, a new search for frame alignment is initiated in the bit immediately following the second 7-bit FAS sequence check. This "hold-off" is done to ensure that new frame alignment searches are done in the next bit position, modulo 512. This facilitates the discovery of the correct frame alignment, even in the presence of fixed timeslot data imitating the FAS.

These algorithms provide robust framing operation even in the presence of random bit errors: framing with algorithm #1 or #2 provides a 99.98% probability of finding frame alignment within 1 ms in the presence of 10^{-3} bit error rate and no mimic patterns.

Once frame alignment is found, the block sets the OOF indication low, indicates a change of frame alignment (if it occurred), and monitors the frame alignment signal, indicating errors occurring in the 7-bit FAS pattern and in bit 2 of NFAS frames, and indicating the debounced value of the Remote Alarm bit (bit 3 of NFAS frames). Using debounce, the Remote Alarm bit has <0.00001% probability of being falsely indicated in the presence of a 10^{-3} bit error rate. The block declares loss of frame alignment if 3 consecutive FAS's have been received in error or, additionally, if bit 2 of NFAS frames has been in error for 3 consecutive occasions. In the presence of a random 10^{-3} bit error rate the frame loss criteria provides a mean time to falsely lose frame alignment of >12 minutes.

The E1-FRMR can be forced to initiate a basic frame search at any time when any of the following conditions are met:

- the software re-frame bit in the E1-FRMR Frame Alignment Options register goes to logic 1;
- the CRC Frame Find Block is unable to find CRC multiframe alignment; or
- the CRC Frame Find Block accumulates excessive CRC evaluation errors (≥ 915 CRC errors in 1 second) and is enabled to force a re-frame under that condition.

CRC Multiframe Alignment Procedure

The E1-FRMR searches for CRC multiframe alignment by observing whether the International bits (bit 1 of TS 0) of NFAS frames follow the CRC multiframe alignment pattern. Multiframe alignment is declared if at least two valid CRC multiframe alignment signals are observed within 8 ms, with the time separating two alignment signals being a multiple of 2 ms

Once CRC multiframe alignment is found, the OOCMFV register bit is set to logic 0, and the E1-FRMR monitors the multiframe alignment signal, indicating errors occurring in the 6-bit MFAS pattern, errors occurring in the received CRC and the value of the FEBE bits (bit 1 of frames 13 and 15 of the multiframe). The E1-FRMR declares loss of CRC multiframe alignment if basic frame alignment is lost. However, once CRC multiframe alignment is found, it cannot be lost due to errors in the 6-bit MFAS pattern.

Under the CRC-to-non-CRC interworking algorithm, if the E1-FRMR can achieve basic frame alignment with respect to the incoming PCM data stream, but is unable to achieve CRC-4 multiframe alignment within the subsequent 400 ms, the distant end is assumed to be a non CRC-4 interface. The details of this algorithm are illustrated in the state diagram in Figure 8.

Figure 8: - CRC Multiframe Alignment Algorithm

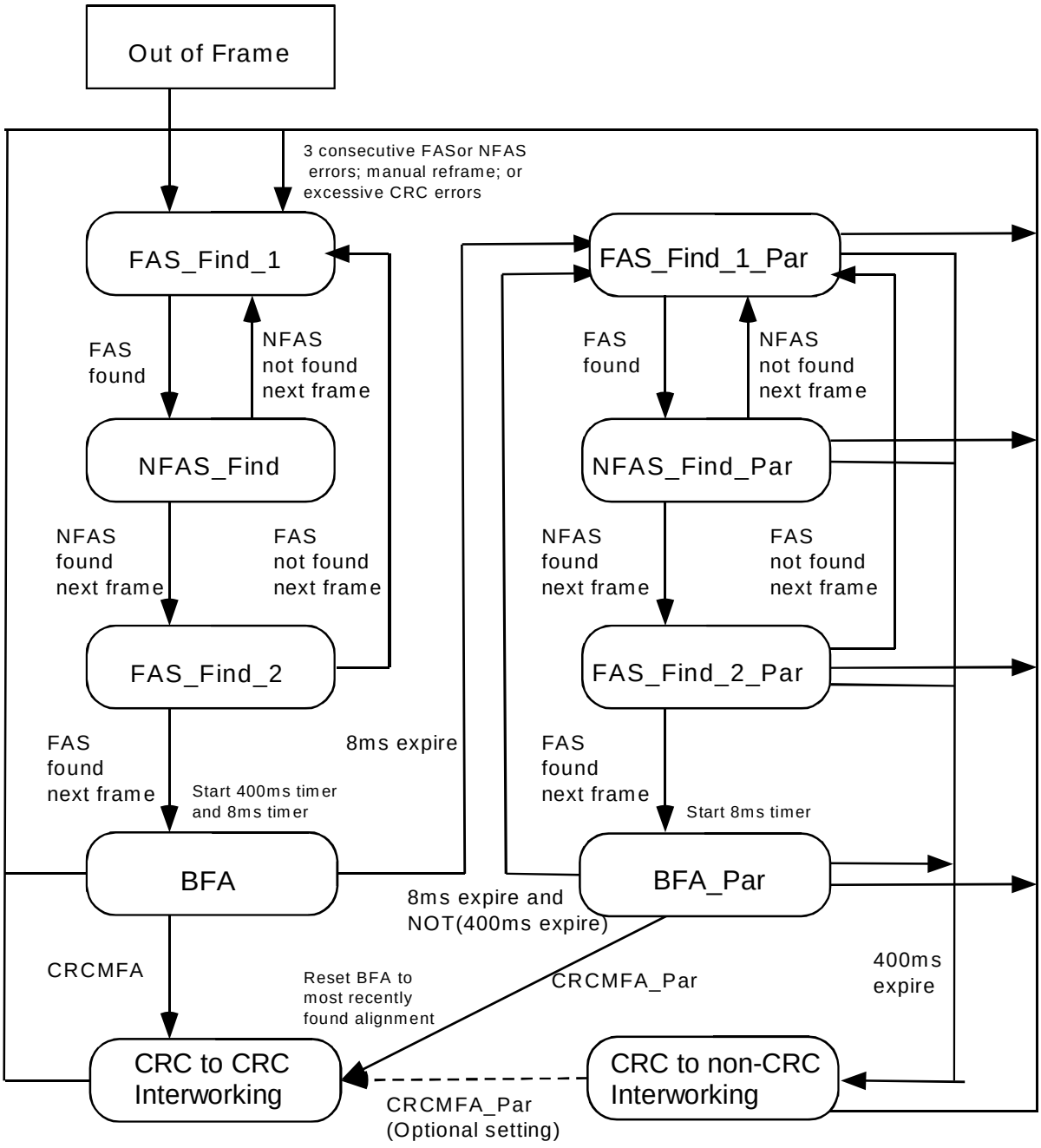


Table 3: - E1-FRMR Framing States

State	Out of Frame	Out of Offline Frame
FAS_Find_1	Yes	No
NFAS_Find	Yes	No
FAS_Find_2	Yes	No
BFA	No	No
CRC to CRC Interworking	No	No
FAS_Find_1_Par	No	Yes
NFAS_Find_Par	No	Yes
FAS_Find_2_Par	No	Yes
BFA_Par	No	No
CRC to non-CRC Interworking	No	No

The states of the primary basic framer and the parallel/offline framer in the E1-FRMR block at each stage of the CRC multiframe alignment algorithm are shown in Table 3.

From an out of frame state, the E1-FRMR attempts to find basic frame alignment in accordance with the FAS/NFAS/FAS G.706 Basic Frame Alignment procedure outlined above. Upon achieving basic frame alignment, a 400 ms timer is started, as well as an 8 ms timer. If two CRC multiframe alignment signals separated by a multiple of 2 ms are observed before the 8 ms timer has expired, CRC multiframe alignment is declared.

If the 8 ms timer expires without achieving multiframe alignment, a new offline search for basic frame alignment is initiated. This search is performed in accordance with the Basic Frame Alignment procedure outlined above. However, this search does not immediately change the actual basic frame alignment of the system (i.e., PCM data continues to be processed in accordance with the first basic frame alignment found after an out of frame state while this frame alignment search occurs as a parallel operation).

When a new basic frame alignment is found by this offline search, the 8 ms timer is restarted. If two CRC multiframe alignment signals separated by a multiple of 2 ms are observed before the 8 ms timer has expired, CRC multiframe alignment is declared and the basic frame alignment is set accordingly (i.e., the basic frame alignment is set to correspond to the frame alignment found by the parallel offline search, which is also the basic frame alignment corresponding to the newly found CRC multiframe alignment).

Subsequent expirations of the 8 ms timer will likewise reinitiate a new search for basic frame alignment. If, however, the 400 ms timer expires at any time during this procedure, the E1-FRMR stops searching for CRC multiframe alignment and declares CRC-to-non-CRC interworking. In this mode, the E1-FRMR may be optionally set to either halt searching for CRC multiframe altogether, or may continue searching for CRC multiframe alignment using the established basic frame alignment. In either case, no further adjustments are made to the basic frame alignment, and no offline searches for basic frame alignment occur once CRC-to-non-CRC interworking is declared: it is assumed that the established basic frame alignment at this point is correct.

AIS Detection

When an unframed all-ones receive data stream is received, an AIS defect is indicated by setting the AISD bit to logic 1 when fewer than three zero bits are received in 512 consecutive bits or, optionally, in each of two consecutive periods of 512 bits. The AISD bit is reset to logic 0 when three or more zeros in 512 consecutive bits or in each of two consecutive periods of 512 bits. Finding frame alignment will also cause the AISD bit to be set to logic 0.

Signaling Frame Alignment

Once the basic frame alignment has been found, the E1-FRMR searches for Channel Associated Signaling (CAS) multiframe alignment using the following G.732 compliant algorithm: signaling multiframe alignment is declared when at least one non-zero timeslot 16 bit is observed to precede a timeslot 16 containing the correct CAS alignment pattern, namely four zeros (“0000”) in the first four bit positions of timeslot 16.

Once signaling multiframe alignment has been found, the E1-FRMR sets the OOSMFV bit of the E1-FRMR Framing Status register to logic 0, and monitors the signaling multiframe alignment signal, indicating errors occurring in the 4-bit pattern, and indicating the debounced value of the Remote Signaling Multiframe Alarm bit (bit 6 of timeslot 16 of frame 0 of the multiframe). Using debounce, the Remote Signaling Multiframe Alarm bit has < 0.00001% probability of being falsely indicated in the presence of a 10^{-3} bit error rate.

This E1-FRMR also indicates the reception of TS 16 AIS when timeslot 16 has been received with three or fewer zeros in each of two consecutive multiframe periods. The TS16AIS signal is cleared when each of two consecutive signaling multiframe periods contain four or more zeros OR when the signaling multiframe signal is found.

The block declares loss of CAS multiframe alignment if two consecutive CAS multiframe alignment signals have been received in error, or additionally, if all the bits in timeslot 16 are logic 0 for 1 or 2 (selectable) CAS multiframes. Loss of CAS multiframe alignment is also declared if basic frame alignment has been lost.

National Bit Extraction

The E1-FRMR extracts and assembles the submultiframe-aligned National bit codewords Sa4[1:4], Sa5[1:4], Sa6[1:4], Sa7[1:4] and Sa8[1:4]. The corresponding register values are updated upon generation of the CRC submultiframe interrupt.

This E1-FRMR also detects the V5.2 link ID signal, which is detected when 2 out of 3 Sa7 bits are zeros. Upon reception of this Link ID signal, the V52LINKV bit of the E1-FRMR Framing Status register is set to logic 1. This bit is cleared to logic 0 when 2 out of 3 Sa7 bits are ones.

Alarm Integration

The OOF and the AIS defects are integrated, verifying that each condition has persisted for 104 ms (± 6 ms) before indicating the alarm condition. The alarm is removed when the condition has been absent for 104 ms (± 6 ms).

The AIS alarm algorithm accumulates the occurrences of AISD (AIS detection). The E1-FRMR counts the occurrences of AISD over a 4 ms interval and indicates a valid AIS is present when 13 or more AISD indications (of a possible 16) have been received. Each interval with a valid AIS presence indication increments an interval counter which declares AIS Alarm when 25 valid intervals have been accumulated. An interval with no valid AIS presence indication decrements the interval counter. The AIS Alarm declaration is removed when the counter reaches 0. This algorithm provides a 99.8% probability of declaring an AIS Alarm within 104 ms in the presence of a 10^{-3} mean bit error rate.

The Red alarm algorithm monitors occurrences of OOF over a 4 ms interval, indicating a valid OOF interval when one or more OOF indications occurred during the interval, and indicating a valid in frame (INF) interval when no OOF indication occurred for the entire interval. Each interval with a valid OOF indication increments an interval counter which declares Red Alarm when 25 valid intervals have been accumulated. An interval with valid INF indication decrements the interval counter; the Red Alarm declaration is removed when the counter reaches 0. This algorithm biases OOF occurrences, leading to declaration of Red alarm when intermittent loss of frame alignment occurs.

The E1-FRMR can also be disabled to allow reception of unframed data.

1.10 Receive Elastic Store (RX-ELST)

The Elastic Store (ELST) synchronizes backplane receive frames to the backplane receive clock and frame pulse (BRCLK, BRFP) in the Clock Slave backplane receive modes or to the common backplane receive H-MVIP clock and frame pulse (CMV8MCLK, CMVFP, CMVFPC) in H-MVIP modes. The frame data is buffered in a two frame circular data buffer. Input data is written to the buffer using a write pointer and output data is read from the buffer using a read pointer.

When the elastic store is being used, if the average frequency of the incoming data is greater than the average frequency of the backplane clock, the write pointer will catch up to the read pointer and the buffer will be filled. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The subsequent backplane receive frame is deleted.

If the average frequency of the incoming data is less than the average frequency of the backplane clock, the read pointer will catch up to the write pointer and the buffer will be empty. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The previous backplane receive frame is repeated.

A slip operation is always performed on a frame boundary.

When the backplane receive timing is recovered from the receive data the elastic store can be bypassed to eliminate the one frame delay. In this configuration (the Clock Master backplane receive modes), the elastic store is used to synchronize the backplane receive frames to the transmit line clock (TLCLK[x]) so that per-DS0 loopbacks may be enabled.

To allow for the extraction of signaling information in the data channels, superframe identification is also passed through the ELST.

For payload conditioning, the ELST may optionally insert a programmable idle code into all channels when the framer is out of frame synchronization. This code is set to all 1's when the ELST is reset.

If the data is required to pass through the COMET-Quad unchanged during an out-of-frame condition, then the elastic store may be bypassed.

1.11 Signaling Extractor (SIGX)

The Signaling Extraction (SIGX) block provides channel associated signaling (CAS) extraction from an E1 signaling multi-frame or from ESF, and SF T1 formats.

In T1 mode, the SIGX block provides signaling bit extraction from the received data stream for ESF and SF framing formats. It selectively debounces the bits, and serializes the results onto the BRSIG[x] outputs. Debouncing is performed on individual signaling bits. This BRSIG[x] output is channel aligned with BRPCM[x] output, and the signaling bits are repeated for the entire superframe, allowing downstream logic to reinsert signaling into any frame, as determined by system timing. The signaling data stream contains the A,B,C,D bits in the lower 4 channel bit locations (bits 5, 6, 7 and 8) in ESF framing format; in SF format the A and B bits are repeated in locations C and D (i.e. the signaling stream contains the bits ABAB for each channel).

The SIGX block contains three superframes worth of signal buffering to ensure that there is a greater than 95% probability that the signaling bits are frozen in the correct state for a 50% ones density out-of-frame condition, as specified in TR-TSY-000170 and BELL PUB 43801. With signaling debounce enabled, the per-channel signaling state must be in the same state for 2 superframes before appearing on the serial output stream.

The SIGX block provides one superframe or signaling-multiframe of signal freezing on the occurrence of slips. When a slip event occurs, the SIGX freezes the output signaling for the entire superframe in which the slip occurred; the signaling is unfrozen when the next slip-free superframe occurs.

The SIGX also provides control over timeslot signaling bit fixing, data inversion and signaling debounce on a per-timeslot basis.

The SIGX block also provides an interrupt to indicate a change of signaling state on a per channel basis.

1.12 Performance Monitor Counters (T1/E1-PMON)

The Performance Monitor Counters function is provided by the PMON block. The block accumulates CRC error events, Frame Synchronization bit error events, and Out Of Frame events, or optionally, Change of Frame Alignment (COFA) events with saturating counters over consecutive intervals as defined by the period of the supplied transfer clock signal (typically 1 second). When the transfer clock signal is applied, the PMON transfers the counter values into holding registers and resets the counters to begin accumulating events for the interval. The counters are reset in such a manner that error events occurring during the reset are not missed. If the holding registers are not read between successive transfer clocks, an OVERRUN register bit is asserted.

Generation of the transfer clock within a quadrant is performed by writing to any counter register location within the quadrant or by writing to the Revision/Chip ID/Quadrant PMON Update register. The holding register addresses are contiguous to facilitate faster polling operations.

1.13 T1 Automatic Performance Report Generation (APRM)

In compliance with the ANSI T1.231, T1.403 and T1.408 standards, a performance report is generated each second for T1 ESF applications. The report conforms to the HDLC protocol and is inserted into the ESF facility data link.

The performance report can only be transmitted if the TDPR is configured to insert the ESF Facility Data Link and the PREN bit of the TDPR Configuration register is logic 1. The performance report takes precedence over incompletely written packets, but it does not pre-empt packets already being transmitted.

See the Operation section for details on the performance report encoding.

1.14 T1 Alarm Integrator (ALMI)

The T1 Alarm Integration function is provided by the ALMI block. This block detects the presence of Yellow, Red, and AIS Carrier Fail Alarms (CFA) in SF, or ESF formats. The alarm detection and integration is compatible with the specifications defined in ANSI T1.403 and TR-TSY-000191.

The ALMI block declares the presence of Yellow alarm when the Yellow pattern has been received for 425 ms (± 50 ms); the Yellow alarm is removed when the Yellow pattern has been absent for 425 ms (± 50 ms). The presence of Red alarm is declared when an out-of-frame condition has been present for 2.55 sec (± 40 ms); the Red alarm is removed when the out-of-frame condition has been absent for 16.6 sec (± 500 ms). The presence of AIS alarm is declared when an out-of-frame condition and all-ones in the PCM data stream have been present for 1.5 sec (±100 ms); the AIS alarm is removed when the AIS condition has been absent for 16.8 sec (±500 ms).

CFA alarm detection algorithms operate in the presence of a 10^{-3} bit error rate.

The ALMI also indicates the presence or absence of the Yellow, Red, and AIS alarm signal conditions over 40 ms, 40 ms, and 60 ms intervals, respectively, allowing an external microprocessor to integrate the alarm conditions via software with any user-specific algorithms. Alarm indication is provided through internal register bits.

1.15 HDLC Receiver (RDLC)

The RDLC is a microprocessor peripheral used to receive HDLC frames on the 4kHz ESF facility data link, the E1 Sa-bit data link.

The RDLC detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data, and calculates the CRC-CCITT frame check sequence (FCS).

In the address matching mode, only those packets whose first data byte matches one of two programmable bytes or the universal address (all ones) are stored in the FIFO. The two least significant bits of the address comparison can be masked for LAPD SAPI matching.

Received data is placed into a 128-level FIFO buffer. An interrupt is generated when a programmable number of bytes are stored in the FIFO buffer. Other sources of interrupt are detection of the terminating flag sequence, abort sequence, or FIFO buffer overrun.

The Status Register contains bits that indicate the overrun or empty FIFO status, the interrupt status, and the occurrence of first flag or end of message bytes written into the FIFO. The Status Register also indicates the abort, flag, and end of message status of the data just read from the FIFO. On end of message, the Status Register indicates the FCS status and if the packet contained a non-integer number of bytes.

1.16 Bit Oriented Code Detector (RBOC)

The Bit Oriented Code detection function is provided by the RBOC block. This block detects the presence of 63 of the possible 64 bit oriented codes transmitted in the T1 Facility Data Link channel in ESF framing format, as defined in ANSI T1.403 and in TR-TSY-000194. The 64Th code (111111) is similar to the HDLC flag sequence and is used by the RBOC to indicate no valid code received.

Bit oriented codes are received on the Facility Data Link channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0). BOCs are validated when repeated at least 10 times. The RBOC can be enabled to declare a received code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the RBOC Configuration/Interrupt Enable register. The RBOC declares that the code is removed if two code sequences containing code values different from the detected code are received in a moving window of ten code periods.

Valid BOC are indicated through the RBOC Interrupt Status register. The BOC bits are set to all ones (111111) if no valid code has been detected. An interrupt is generated to signal when a

detected code has been validated, or optionally, when a valid code goes away (i.e. the BOC bits go to all ones).

1.17 Receive Per-Channel Serial Controller (RPSC)

The RPSC allows data and signaling trunk conditioning to be applied on the backplane receive stream on a per-channel basis. It also allows per-channel control of data inversion, the extraction of clock and data on BRCLK[x] and BRPCM[x] (when the Clock Master: Nx64Kbit/s mode is active), and the detection or generation of pseudo-random patterns. The RPSC operates on the data after its passage through ELST, so that data and signaling conditioning may overwrite the ELST trouble code.

1.18 Pseudo Random Binary Sequence Generation and Detection (PRBS)

The Pseudo Random Binary Sequence Generator/Detector (PRBS) block is a software programmable test pattern generator, receiver, and analyzer. PRBS Patterns may be generated in either the transmit or receive directions, and detected in the opposite direction.

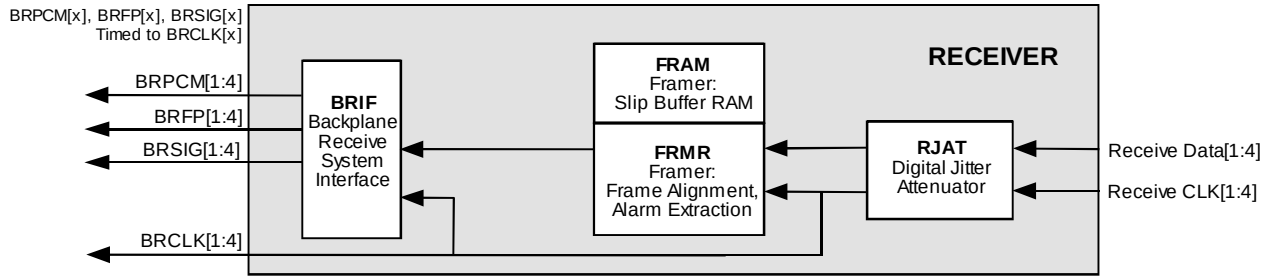
The PRBS can be programmed to check for the generated pseudo random pattern. The PRBS accumulates the total number of bits received and the total number of bit errors in a 24-bit counter.

1.19 Backplane Receive System Interface (BRIF)

The Backplane Receive System Interface (BRIF) block provides system side serial clock and data access as well as H-MVIP access for up to 4 T1 or E1 receive streams. There are several master and slave clock modes for serial clock and data system side access to the T1 and E1 streams. When enabled for 8.192 Mbit/s H-MVIP, there are three separate signals for data and signaling. Information on programming the COMET-Quad for the modes can be found in the Operation section.

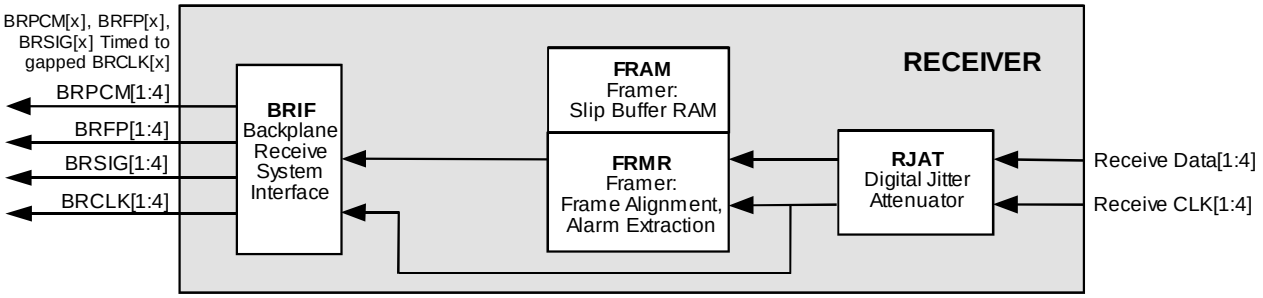
Three Clock Master modes provide a serial clock and data backplane receive interface with clocking provided by COMET-Quad: Clock Master: Full T1/E1, Clock Master: Nx64Kbit/s, Clock Master: Clear Channel. Three Clock slave modes provide a serial clock and data backplane receive mode, an H-MVIP mode, and a mixed clock-and-data/H-MVIP mode. All Clock Slave modes accept externally sourced clocking. The modes are Clock Slave: Full T1/E1, Clock Slave: Full T1/E1 with CCS H-MVIP, and Clock Slave: H-MVIP.

Figure 9: - Receive Clock Master: Full T1/E1



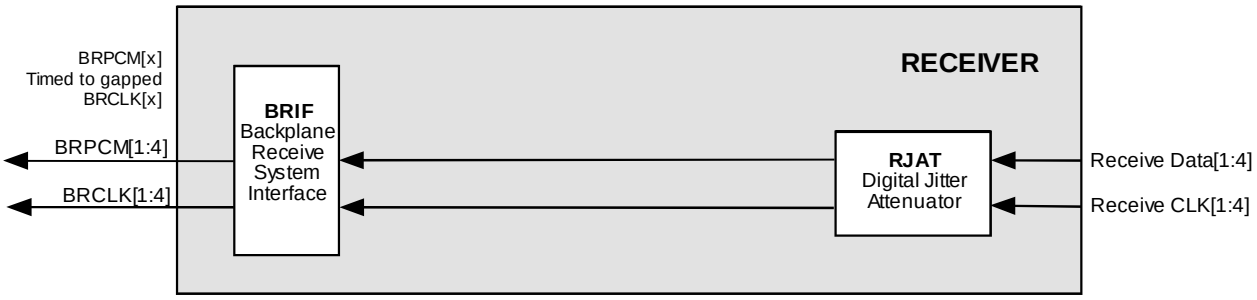
In Receive Clock Master: Full T1/E1 mode, the elastic store is bypassed and the backplane receive clock (BRCLK[x]) is, optionally, a jitter attenuated version of the 1.544 MHz or 2.048 MHz receive clock. The backplane receive data appears on BRPCM[x], the backplane receive signaling appears on BRSIG[x], and the backplane receive frame alignment is indicated by BRFP[x]. In this mode, T1 or E1 data passes through the COMET-Quad unchanged during out-of-frame conditions, similar to an offline framer system. When the COMET-Quad is the clock master in the backplane receive direction, the receive elastic store is used to buffer between the backplane receive and backplane transmit clocks to facilitate per-Channel loopback.

Figure 10: - Receive Clock Master: Nx64Kbit/s



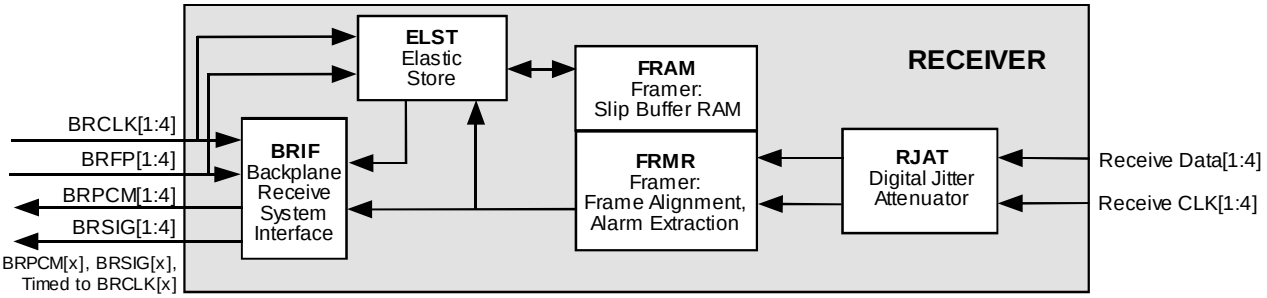
In Receive Clock Master: Nx64Kbit/s mode, BRCLK[x] is a gapped version of the optionally jitter attenuated 1.544 MHz or 2.048 MHz receive clock. BRCLK[x] is gapped on a per channel basis so that a subset of the 24 channels in the T1 frame or 32 channels in an E1 frame is extracted on BRPCM[x]. BRFP[x] indicates frame alignment but, in T1 mode, has no clock since it is gapped during the framing bit positions. Channel extraction is controlled by the RPSC block. The framing bit position is always gapped in T1 mode, so the number of BRCLK[x] pulses is controllable from 0 to 192 pulses per T1 frame or 0 to 256 pulses per E1 frame on a per-channel basis. In this mode, T1 or E1 streams pass through the COMET-Quad unchanged during out-of-frame conditions. The parity functions are not usable in Channel mode. When the COMET-Quad is the clock master in the backplane receive direction, the elastic store is used to buffer between the backplane receive and backplane transmit clocks to facilitate per-Channel loopback.

Figure 11: - Receive Clock Master: Clear Channel



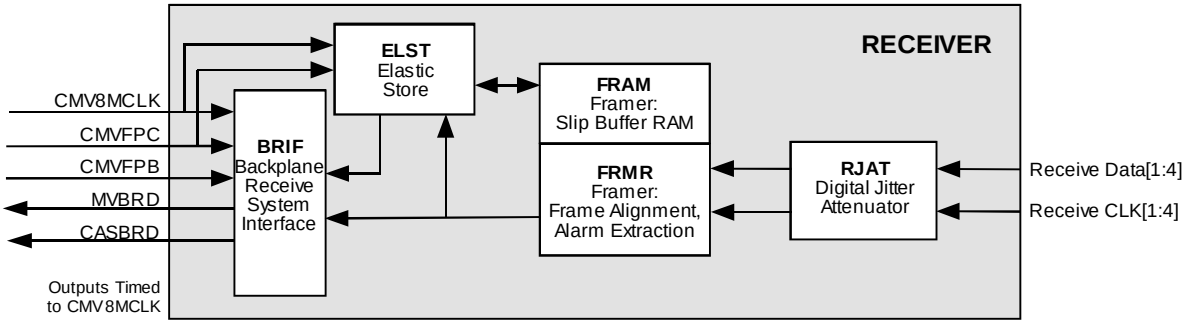
In Receive Clock Master: Clear Channel mode, the elastic store is bypassed and the backplane receive clock (BRCLK[x]) is optionally a jitter attenuated version of the 1.544 MHz or 2.048 MHz receive clock. The backplane receive data appears on BRPCM[x] with no frame alignment indication.

Figure 12: - Receive Clock Slave: Full T1/E1



In Receive Clock Slave: Full T1/E1 mode, the elastic store is enabled to permit the input BRCLK[x] to specify the backplane receive-side timing. The backplane receive data on BRPCM[x] and signaling BRSIG[x] are bit aligned to the 1.544 MHz or 2.048 MHz backplane receive clock (BRCLK[x]) and are frame aligned to the backplane receive frame pulse (BRFP). BRSIG[x] contains the signaling state (ABCD or ABAB) in the lower four bits of each channel.

Figure 13: - Receive Clock Slave: H-MVIP



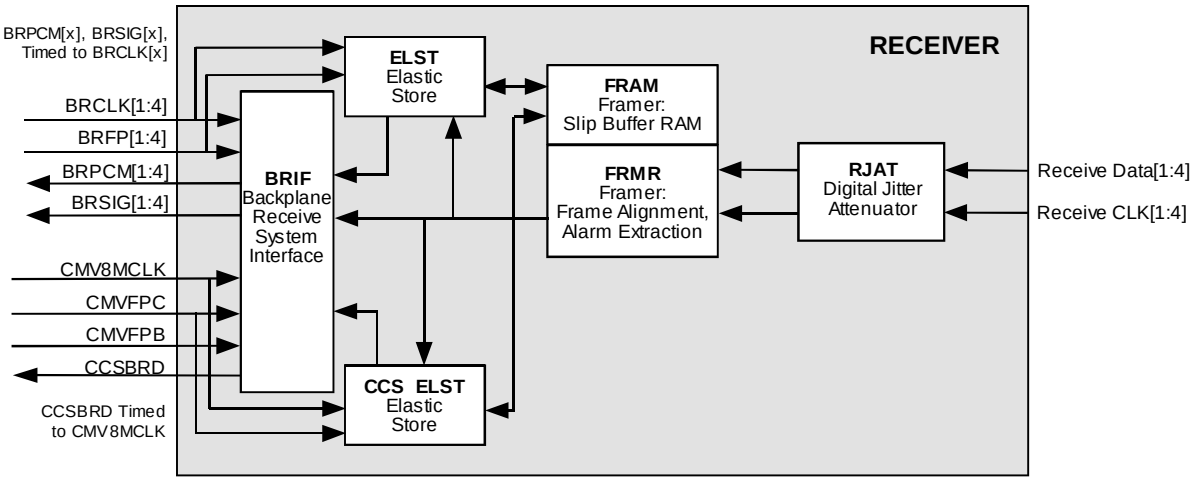
When Receive Clock Slave: H-MVIP mode is enabled a 8.192 Mbit/s H-MVIP backplane transmit interface multiplexes up to 128 channels from 4 T1s or E1s, up to 128 channel associated signaling (CAS) channels from 4 T1s or E1s and common channel signaling from up to 4 T1s or E1s. The H-MVIP interface uses common clocks, CMV8MCLK and CMVFPC, and frame pulse, CMVFPB, for synchronization.

Using the H-MVIP interface forces the T1 or E1 receiver to operate in synchronous mode, meaning that elastic stores are used.

The H-MVIP backplane receive data pins are multiplexed with serial data outputs to provide H-MVIP access to 128 data channels.

The CASBRD H-MVIP signal provides access to the Channel Associated Signaling (CAS) for all of the 128 data channels. The CAS is time division multiplexed exactly the same way as the data channels and is synchronized with the H-MVIP data channels. Over a T1 or E1 multi-frame the four CAS bits per channel are repeated with each data byte. Four stuff bits are used to pad each CAS nibble (ABCD bits) out to a full byte in parallel with each data byte.

Figure 14: - Receive Clock Slave: Full T1/E1 with CCS H-MVIP



In Receive Clock Slave: Full T1/E1 with CCS H-MVIP mode, the elastic store is enabled to permit the input BRCLK[x] to specify the backplane receive-side timing. The backplane receive data on BRPCM[x] and signaling BRSIG[x] are bit aligned to the 1.544 MHz or 2.048 MHz backplane receive clock (BRCLK[x]) and are frame aligned to the backplane receive frame pulse (BRFP). BRSIG[x] contains the signaling state (ABCD or ABAB) in the lower four bits of each channel.

The H-MVIP interface (CMV8MCLK, CMVFPC, CMVFPB, and CCSBRD) extracts Common Channel Signaling (CCS) from the 24th DS0 in T1 mode and up to 3 timeslots (15, 16, 31) in E1 mode. The H-MVIP interface uses common clocks, CMV8MCLK and CMVFPC, and frame pulse, CMVFPB, for synchronization.

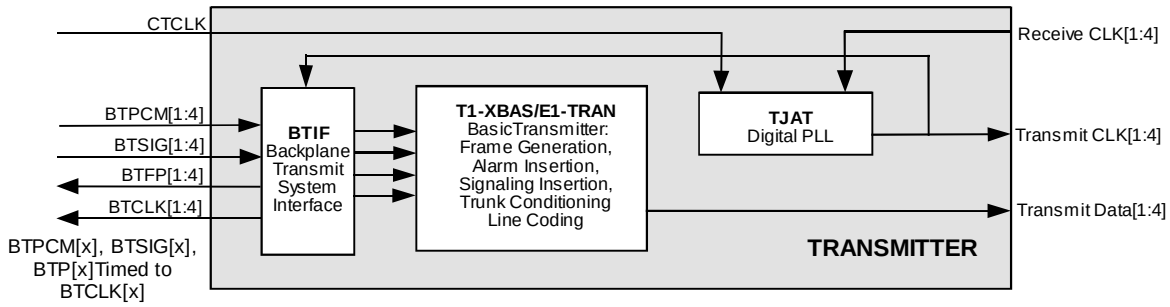
1.20 Backplane Transmit System Interface (BTIF)

The Backplane Transmit System Interface (BTIF) block provides system side serial clock and data access as well as H-MVIP access for up to 4 T1 or E1 transmit streams. There are several master and slave clocking modes for serial clock and data system side access to the T1 and E1 streams. When enabled for 8.192 Mbit/s H-MVIP there are three separate signals for data and signaling. These modes of operation must be the same across all 4 T1 or E1 streams. Information on programming the COMET-Quad for the modes can be found in the Operation section.

Three Clock Master modes provide a serial clock and data backplane transmit interface with per link clocking provided by COMET-Quad: Clock Master: Full T1/E1, Clock Master: Nx64Kbit/s and Clock Master: Clear Channel. Four Clock slave modes provide two serial clock and data backplane transmit modes, a mixed clock-and-data/H-MVIP mode, and a pure H-MVIP mode all with externally sourced clocking: Clock Slave: Full T1/E1, Clock Slave: Full T1/E1 with CCS H-MVIP, Clock Slave: Clear Channel and Clock Slave: H-MVIP.

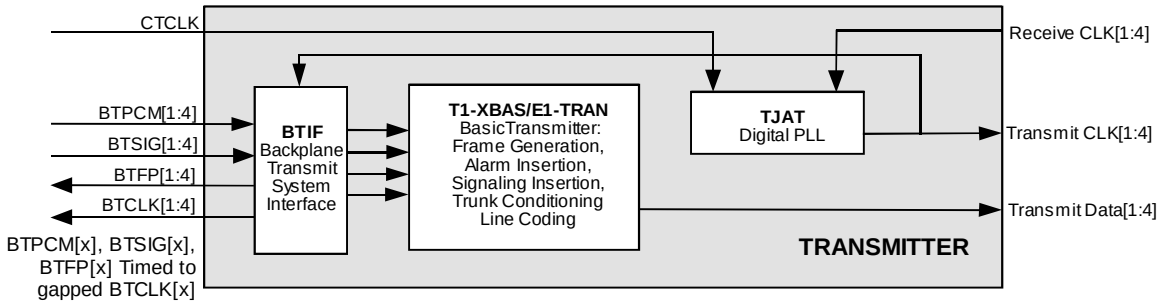
In Clock Master modes the transmit clock can be sourced from either the common transmit clock, CTCLK, the received clock for that link, or one of the two recovered clocks.

Figure 15: - Transmit Clock Master: Full T1/E1



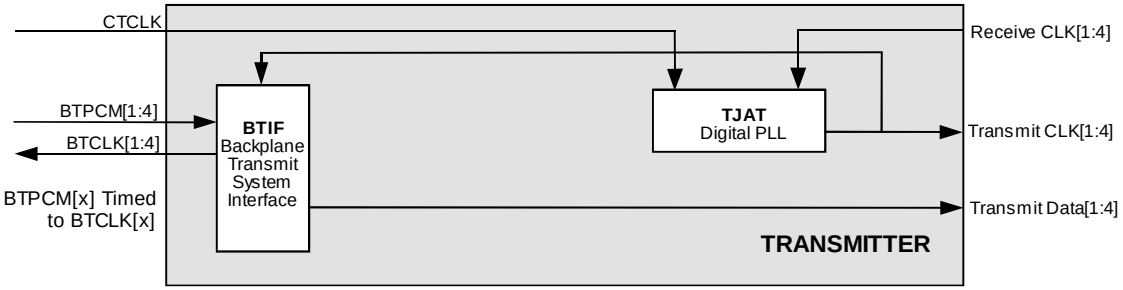
In Transmit Clock Master: Full T1/E1 mode, backplane transmit clock (BTCLK[x]) is a jitter attenuated version of the 1.544 MHz or 2.048 MHz receive clock. BTCLK[x] is pulsed for each bit in the 193 bit T1 frame or for each bit in the 256 bit E1 frame. The backplane transmit data is sampled from BTPCM[x], the backplane transmit signaling is sampled from BRSIG[x], and the backplane transmit frame alignment is indicated by BTFP[x].

Figure 16: - Transmit Clock Master: Nx64Kbit/s



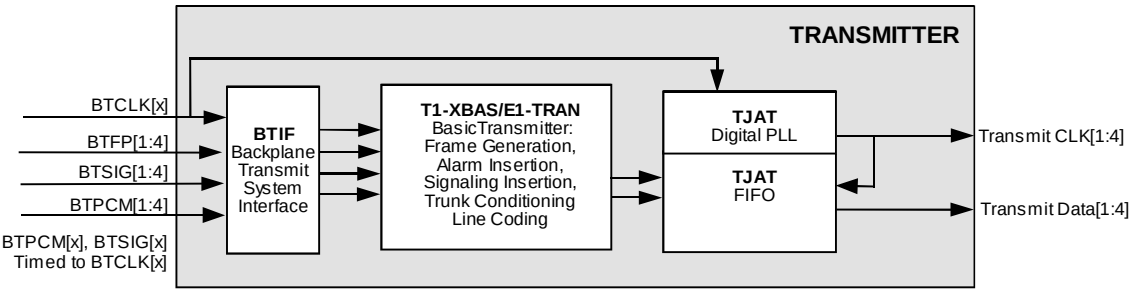
In Transmit Clock Master: Nx64Kbit/s mode, BTCLK[x] is gapped on a per channel basis so that a subset of the 24 channels in a T1 frame or 32 channels in an E1 frame are inserted on BTPCM[x]. BTFP[x] indicates frame alignment but, in T1 mode, has no clock since it is gapped during the framing bit positions. Channel insertion is controlled by the IDLE_CHAN bits in the TPSC block's Backplane Transmit Control Bytes. The framing bit position is always gapped, so the number of BTCLK[x] pulses is controllable from 0 to 192 pulses per T1 frame or 0 to 256 pulses per E1 frame on a per-channel basis. The parity functions are not usable in Nx64Kbit/s mode.

Figure 17: - Transmit Clock Master: Clear Channel



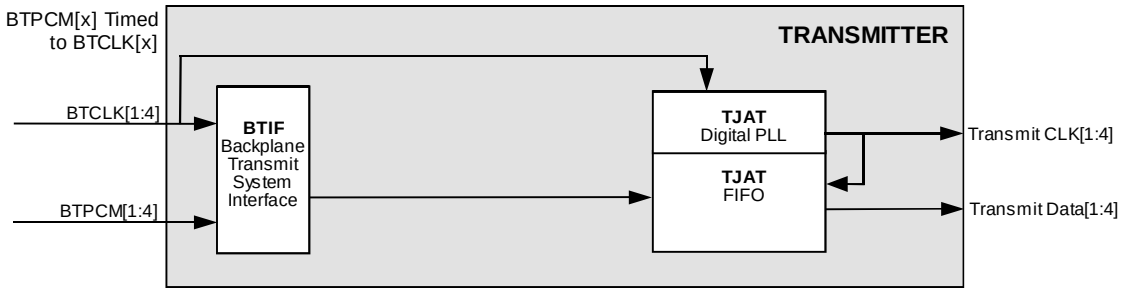
Transmit Clock Master: Clear Channel mode has no frame alignment therefore no frame alignment is indicated to the upstream device. BTCLK[x] is a continuous clock at 1.544Mbit/s for T1 links or 2.048Mbit/s for E1 links.

Figure 18: - Transmit Clock Slave: Full T1/E1



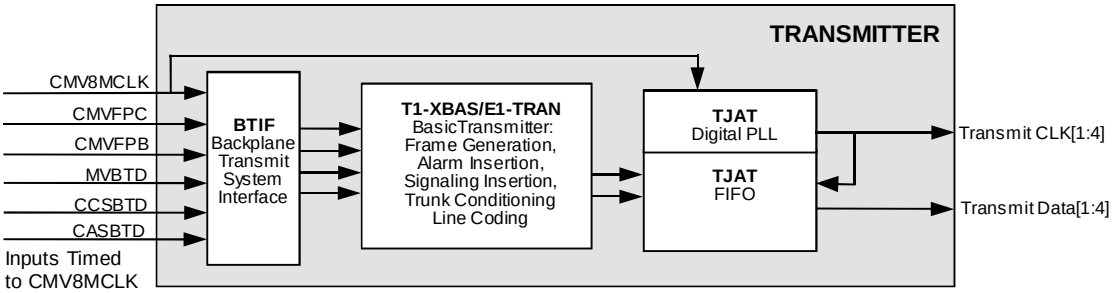
In Transmit Clock Slave: Full T1/E1 mode, the backplane transmit interface is clocked by the backplane transmit clock (BTCLK[x]). The transmitter is either frame-aligned or superframe-aligned to the backplane transmit frame pulse (BTFP[x]). BTFP[x] is configurable to indicate the frame alignment or the superframe alignment of BTPCM[x]. The BTSIG[x] contain the signaling data to be inserted into Transmit Data[x], with the four least significant bits of each channel on BTSIG[x] representing the signaling state (ABCD or ABAB). BTCLK[x] can be enabled to be either a 1.544 MHz clock for T1 links or a 2.048 MHz clock for T1 and E1 links.

Figure 19: - Transmit Clock Slave: Clear Channel



In Transmit Clock Slave: Clear Channel mode, the backplane transmit interface is clocked by the externally provided backplane transmit clock (BTCLK[x]). BTCLK[x] must be a 1.544 MHz clock for T1 links or a 2.048 MHz clock for E1 links. The Transmit Clock[x] is a jitter attenuated version of BTCLK[x].

Figure 20: - Transmit Clock Slave: H-MVIP



When Transmit Clock Slave: H-MVIP mode is enabled a 8.192 Mbit/s H-MVIP backplane transmit interface multiplexes up to 128 channels from 4 T1's or E1's, up to 128 Channel Associated Signaling (CAS) channels from 4 T1's or E1's and Common Channel Signaling (CCS) from up to 4 T1's or E1's. The H-MVIP interface uses common clocks, CMV8MCLK and CMVFPC, and frame pulse, CMVFPB, for synchronization.

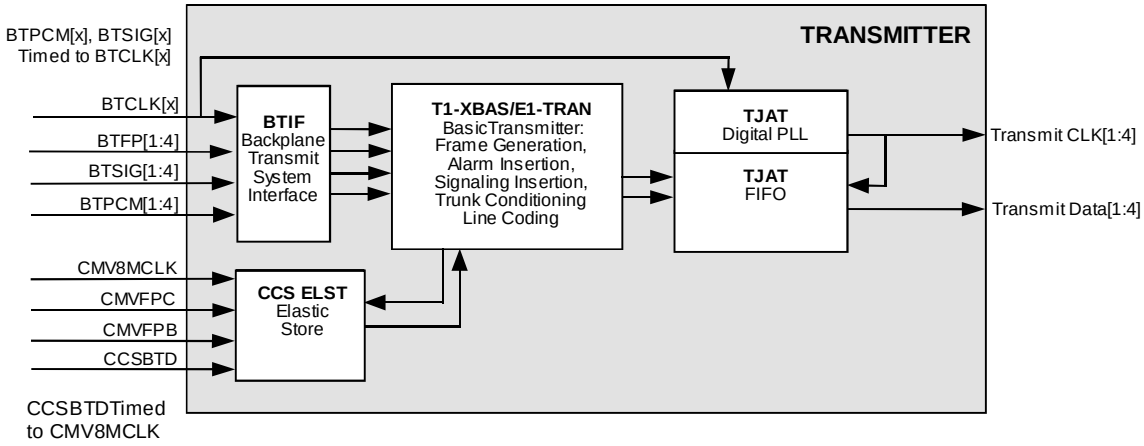
The H-MVIP data signal, MVBTD, provides H-MVIP access to 128 data channels.

A separate H-MVIP signal, CASBTD, provides access to the Channel Associated Signaling (CAS) for 128 channels. The CAS H-MVIP signal is time division multiplexed exactly the same way as the data channels and should be synchronized with the H-MVIP data channels. Over a T1 or E1

multi-frame the four CAS bits per channel are repeated with each data byte. Four stuff bits are used to pad each CAS nibble (ABCD bits) out to a full byte in parallel with each data byte.

The third H-MVIP signal, CCSBTD, is used to time division multiplex the Common Channel Signaling (CCS) for all 4 T1's and E1's plus V5.1 and V5.2 channels in E1 mode.

Figure 21: - Transmit Clock Slave: Full T1/E1 with CCS H-MVIP



Transmit Clock Slave: Full T1/E1 with CCS H-MVIP mode is the same as Transmit Clock Slave: Full T1/E1 mode except that Common Channel Signaling (CCS) is inserted into the transmit stream via an H-MVIP interface. The CCSBTD H-MVIP signal is used to time division multiplex the Common Channel Signaling (CCS) for all 4 T1's and E1's plus V5.1 and V5.2 channels in E1 mode. The H-MVIP interface use common clocks, CMV8MCLK and CMVFPC, and frame pulse, CMVFPB, for synchronization.

1.21 Transmit Per-Channel Serial Controller (TPSC)

The Transmit Per-Channel Serial Controller allows data and signaling trunk conditioning or idle code to be applied on the transmit DS-1 stream on a per-channel basis. It also allows per-channel control of zero code suppression, data inversion, channel loopback (from the backplane receive stream), channel insertion, and the detection or generation of pseudo-random or repetitive patterns.

The TPSC interfaces directly to the E1-TRAN and T1-XBAS block and provides serial streams for signaling control, idle code data and backplane transmit data control.

1.22 Transmit Elastic Store (TX-ELST)

The Transmit Elastic Store (TX-ELST) provides the ability to decouple the line timing from the backplane timing. The TX-ELST is required whenever the backplane and lineside clocks are not traceable to a common source.

When the elastic store is being used, if the average frequency of the backplane data is greater than the average frequency of the line clock, the buffer will fill. Under this condition a controlled slip will occur upon the next frame boundary. The following frame of PCM data will be deleted.

If the average frequency of the backplane data is less than the average frequency of the line clock, the buffer will empty. Under this condition a controlled slip will occur upon the next frame boundary. The last frame will be repeated.

A slip operation is always performed on a frame boundary. The TX-ELST is upstream of the frame overhead insertion; therefore, frame slips do not corrupt the frame alignment signal.

When the line timing is derived from CTCLK or BTCLK is an output, the elastic store is bypassed to eliminate the one frame delay.

1.23 Basic Transmitter (XBAS)

The T1 Basic Transmitter (XBAS) block generates the 1.544 Mbit/s T1 data stream according to SF or ESF frame formats.

In concert with the Transmit Per-Channel Serial Controller (TPSC), the XBAS block, provides per-channel control of idle code substitution, data inversion (either all 8 bits, sign bit magnitude or magnitude only), and zero code suppression. Three types of zero code suppression (GTE, Bell and "jammed bit 8") are supported and selected on a per-channel basis to provide minimum ones density control. An internal signaling control stream provides per-channel control of robbed bit signaling and selection of the signaling source. All channels can be forced into a trunk conditioning state (idle code substitution and signaling conditioning) by use of the Master Trunk Conditioning bit in the Configuration Register.

A data link is provided for ESF mode. The data link sources include bit oriented codes and HDLC messages. Support is provided for the transmission of framed or unframed Inband Code sequences and transmission of AIS or Yellow alarm signals for all formats.

The transmitter can be disabled for framing via the disable bit in the Transmit Functions Enable register. When transmitting ESF formatted data, the framing bit, datalink bit, or the CRC-6 bit from the backplane transmit stream can be by-passed to the output PCM stream. Finally, the transmitter can be by-passed completely to provide an unframed operating mode.

1.24 E1 Transmitter (E1-TRAN)

The E1 Transmitter (E1-TRAN) generates a 2048 kbit/s data stream according to ITU-T recommendations, providing individual enables for frame generation, CRC multiframe generation, and channel associated signaling (CAS) multiframe generation.

In concert with Transmit Per-Channel Serial Controller (TPSC), the E1-TRAN block provides per-timeslot control of idle code substitution, data inversion, digital milliwatt substitution, selection of the signaling source and CAS data. All timeslots can be forced into a trunk conditioning state

(idle code substitution and signaling substitution) by use of the master trunk conditioning bit in the Configuration Register.

Common Channel Signaling (CCS) is supported in timeslot 16 through the Transmit Channel Insertion (TXCI) block. Support is provided for the transmission of AIS and TS16 AIS, and the transmission of remote alarm (RAI) and remote multiframe alarm signals.

The National Use bits (Sa-bits) can be sourced from the E1-TRAN National Bits Codeword registers as 4-bit codewords aligned to the submultiframe. Alternatively, the Sa-bits may individually carry data links sourced from the internal HDLC controller, or may be passed transparently from the BTPCM[x] input.

1.25 T1 Inband Loopback Code Generator (XIBC)

The T1 Inband Loopback Code Generator (XIBC) block generates a stream of inband loopback codes (IBC) to be inserted into a T1 data stream. The IBC stream consists of continuous repetitions of a specific code and can be either framed or unframed. When the XIBC is enabled to generate framed IBC, the framing bit overwrites the inband code pattern. The contents of the code and its length are programmable from 3 to 8 bits. The XIBC interfaces directly to the XBAS Basic Transmitter block.

1.26 Pulse Density Enforcer (XPDE)

The Pulse Density Enforcer function is provided by the XPDE block. Pulse density enforcement is enabled by a register bit within the XPDE.

This block monitors the digital output of the transmitter and detects when the stream is about to violate the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window. If a density violation is detected, the block can be enabled to insert a logic 1 into the digital stream to ensure the resultant output no longer violates the pulse density requirement. When the XPDE is disabled from inserting logic 1s, the digital stream from the transmitter is passed through unaltered.

1.27 Signaling Aligner (SIGA)

When enabled, the Signaling Aligner is positioned in the backplane transmit path before the E1-TRAN and T1-XBAS. Its purpose is to ensure that, if the signaling on BTSIG[x] is changed in the middle of a superframe, the XBAS completes transmitting the A,B,C, and D bits for the current superframe before switching to the new values. This permits signaling integrity to be preserved independent of the superframe alignment of the E1-TRAN and T1-XBAS or the signaling data source.

1.28 Bit Oriented Code Generator (XBOC)

The Bit Oriented Code Generator function is provided by the XBOC block. This block transmits 63 of the possible 64 bit oriented codes in the Facility Data Link (FDL) channel in ESF framing format, as defined in ANSI T1.403-1989. The 64th code (111111) is similar to the HDLC Flag

sequence and is used in the XBOC to disable transmission of any bit oriented codes. When transmission is disabled the FDL channel is set to all ones.

Bit oriented codes are transmitted on the T1 Facility Data Link channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111. When driving the T1 facility data link the transmitted bit oriented codes have priority over any data transmitted except for ESF Yellow Alarm. The code to be transmitted is programmed by writing to the XBOC code registers when it is held until the last code has been transmitted at least 10 times. An interrupt or polling mechanism is used to determine when the most recent code written the XBOC register is being transmitted and a new code can be accepted.

1.29 HDLC Transmitters (TDPR)

The HDLC Transmitter (TDPR) provides a serial data link for the 4 kHz ESF facility data link, E1 Sa-bit data link. The TDPR is used under microprocessor control to transmit HDLC data frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, and abort sequence insertion. Upon completion of the message, a CRC-CCITT frame check sequence (FCS) may be appended, followed by flags. If the TDPR transmit data FIFO underflows, an abort sequence is automatically transmitted.

When enabled, the TDPR continuously transmits the flag sequence (01111110) until data is ready to be transmitted. Data bytes to be transmitted are written into the Transmit Data Register. The TDPR performs a parallel-to-serial conversion of each data byte before transmitting it.

The default procedure provides automatic transmission of data once a complete packet is written. All complete packets of data will be transmitted. After the last data byte of a packet, the CRC word (if CRC insertion has been enabled) and a flag, or just a flag (if CRC insertion has not been enabled) is transmitted. The TDPR then returns to the transmission of flag characters until the next packet is available for transmission. While working in this mode, the user must only be careful to avoid overfilling the FIFO; underruns cannot occur unless the packet is greater than 128 bytes long. The TDPR will force transmission if the FIFO is filled up regardless of whether or not the packet has been completely written into the FIFO.

The second procedure transmits data only when the FIFO depth has reached a user configured upper threshold. The TDPR will continue to transmit data until the FIFO depth has fallen below the upper threshold and the transmission of the last packet with data above the upper threshold has completed. In this mode, the user must be careful to avoid overruns and underruns. An interrupt can be generated once the FIFO depth has fallen below a user configured lower threshold as an indicator for the user to write more data.

Interrupts can also be generated if the FIFO underflows while transmitting a packet, when the FIFO falls below a lower threshold, when the FIFO is full, or if the FIFO is overrun.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort sequences.

Abort characters can be continuously transmitted at any time by setting a control bit. During packet transmission, an underrun situation can occur if data is not written to the TDPR Transmit Data register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the UDRI interrupt.

1.30 Transmit Jitter Attenuator (TJAT)

The Transmit Jitter Attenuation function is provided by a digital phase lock loop and 80-bit deep FIFO. The TJAT receives jittery, dual-rail data in NRZ format on two separate inputs, which allows bipolar violations to pass through the block uncorrected. The incoming data streams are stored in a FIFO timed to the transmit clock (either CTCLK or the recovered clock). The respective input data emerges from the FIFO timed to the jitter attenuated clock (Transmit clock) referenced to either CTCLK, BTCLK[x], or the recovered clock.

The jitter attenuator generates the jitter-free 1.544 MHz or 2.048 MHz Transmit clock output transmit clock by adjusting Transmit clock's phase in 1/96 UI increments to minimize the phase difference between the generated Transmit clock and input data clock to TJAT (either CTCLK or the recovered clock). Jitter fluctuations in the phase of the input data clock are attenuated by the phase-locked loop within TJAT so that the frequency of Transmit clock is equal to the average frequency of the input data clock. For T1 applications, to best fit the jitter attenuation transfer function recommended by TR 62411, phase fluctuations with a jitter frequency above 5.7 Hz are attenuated by 6 dB per octave of jitter frequency. Wandering phase fluctuations with frequencies below 5.7 Hz are tracked by the generated Transmit clock. In E1 applications, the corner frequency is 7.6 Hz. To provide a smooth flow of data out of TJAT, Transmit clock is used to read data out of the FIFO.

If the FIFO read pointer (timed to Transmit clock) comes within one bit of the write pointer (timed to the input data clock, CTCLK or RSYNC), TJAT will track the jitter of the input clock. This permits the phase jitter to pass through unattenuated, inhibiting the loss of data.

Jitter Characteristics

The TJAT Block provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. It can accommodate up to 61 UIpp of input jitter at jitter frequencies above 5.7 Hz (7.6 Hz for E1). For jitter frequencies below 5.7 Hz (7.6 Hz for E1), more correctly called wander, the tolerance increases 20 dB per decade. In most applications the TJAT Block will limit jitter tolerance at lower jitter frequencies only. For high frequency jitter, above 10 kHz for example, other factors such as clock and data recovery circuitry may limit jitter tolerance and must be considered. For low frequency wander, below 10 Hz for example, other factors such as slip buffer hysteresis may limit wander tolerance and must be considered. The TJAT block meets the stringent low frequency jitter tolerance requirements of AT&T TR 62411 and thus allows compliance with this standard and the other less stringent jitter tolerance standards cited in the references.

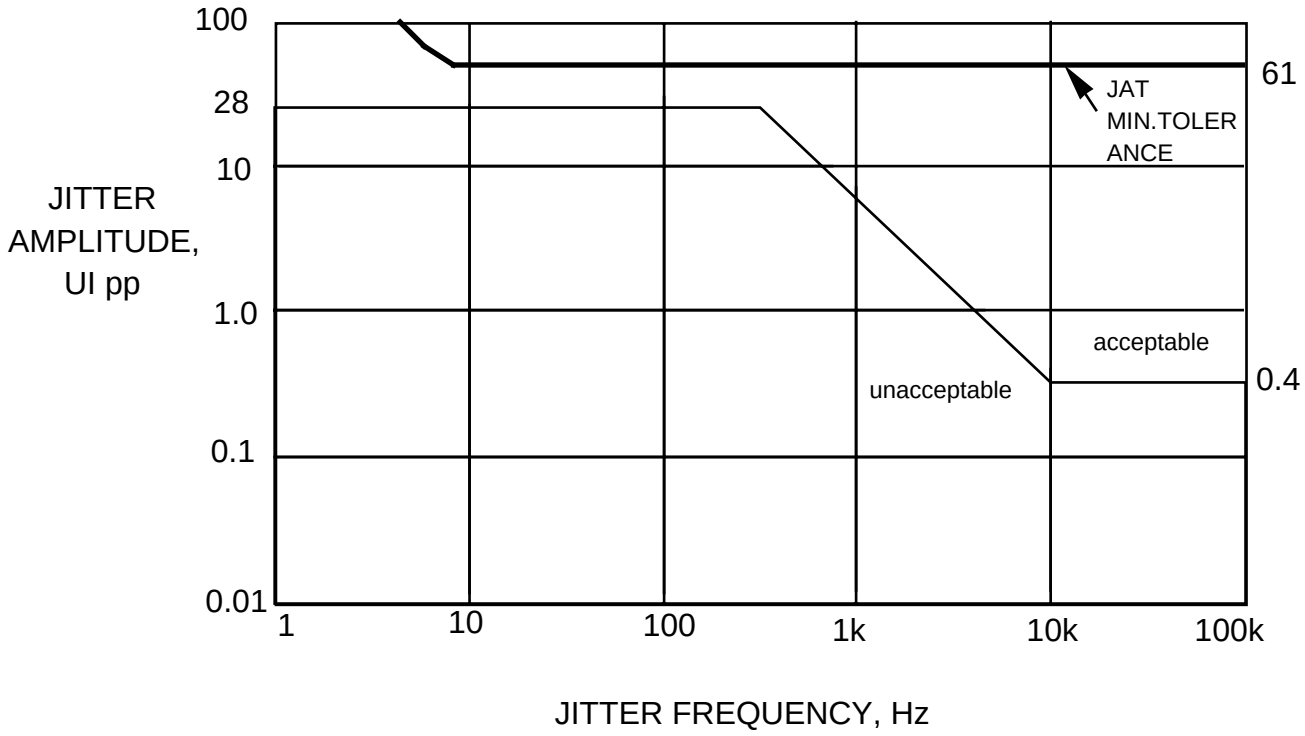
The corner frequency in the jitter transfer response can be altered by programming. Refer to the Operation section for details.

TJAT exhibits negligible jitter gain for jitter frequencies below 5.7 Hz (7.6 Hz for E1), and attenuates jitter at frequencies above 5.7 Hz (7.6 Hz for E1) by 20 dB per decade. In most applications, the TJAT block will determine jitter attenuation for higher jitter frequencies only. Wander, below 10 Hz for example, will essentially be passed unattenuated through TJAT. Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter may be dominated by the generated residual jitter in cases where incoming jitter is insignificant. This generated residual jitter is directly related to the use of a 1/96 UI phase adjustment quantum. TJAT meets the jitter attenuation requirements of AT&T TR 62411. The block allows the implied jitter attenuation requirements for a TE or NT1 given in ANSI Standard T1.408, and the implied jitter attenuation requirements for a type II customer interface given in ANSI T1.403 to be met.

Jitter Tolerance

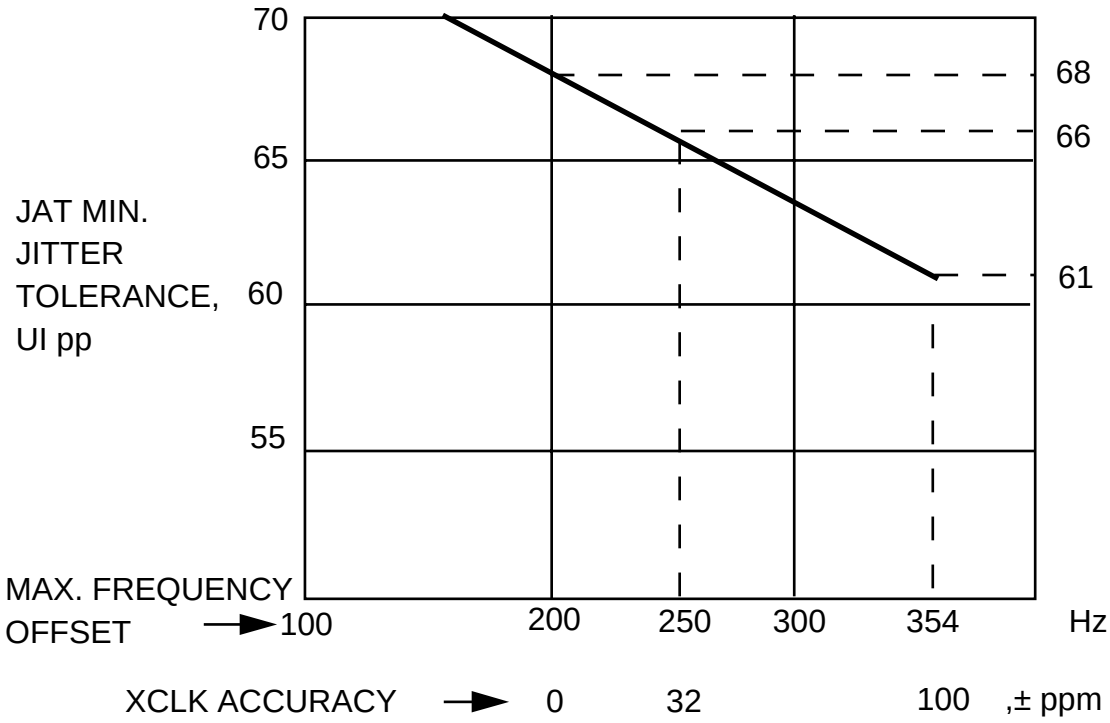
Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For TJAT, the input jitter tolerance is 61 Unit Intervals peak-to-peak (UIpp) with a worst case frequency offset of 354 Hz. It is 80 UIpp with no frequency offset. The frequency offset is the difference between the frequency of XCLK and that of the input data clock.

Figure 22: - TJAT Jitter Tolerance



The accuracy of the XCLK frequency and that of the TJAT PLL reference input clock used to generate the jitter-free Transmit clock output have an effect on the minimum jitter tolerance. Given that the TJAT PLL reference clock accuracy can be ±200 Hz and that the XCLK input accuracy can be ±100 ppm, the minimum jitter tolerance for various differences between the frequency of PLL reference clock and XCLK are shown in Figure 23.

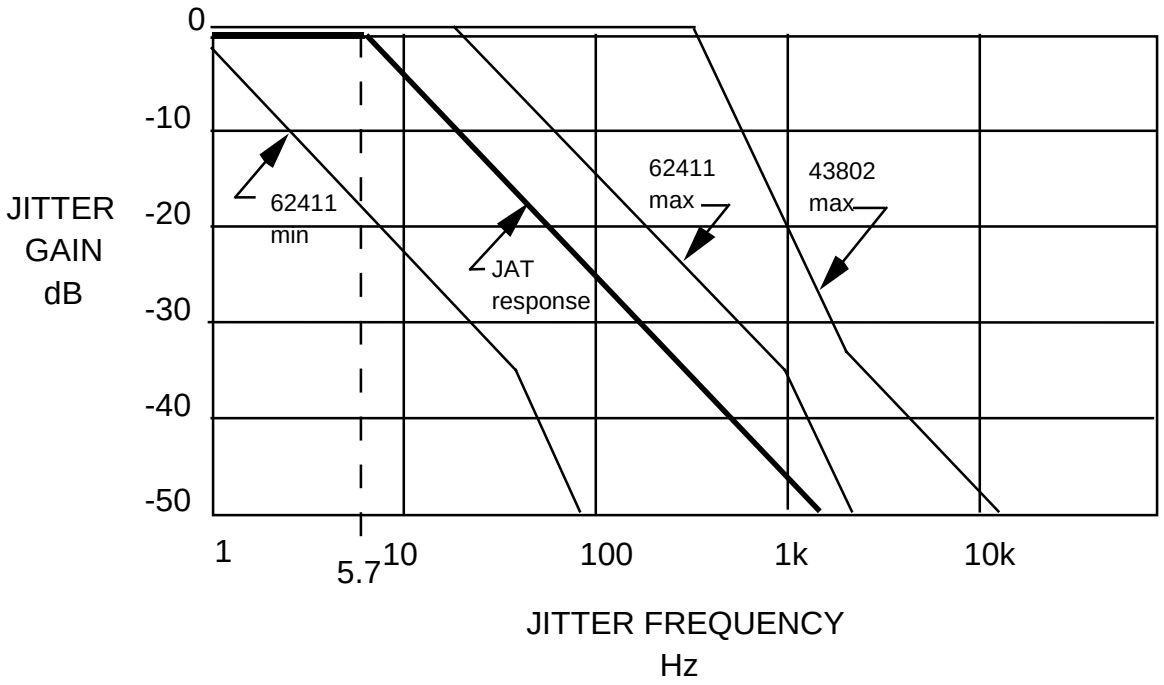
Figure 23: - TJAT Minimum Jitter Tolerance vs. XCLK Accuracy



Jitter Transfer

For T1 applications, the output jitter for jitter frequencies from 0 to 5.7 Hz (7.6 Hz for E1) is no more than 0.1 dB greater than the input jitter, excluding residual jitter. Jitter frequencies above 5.7 Hz (7.6 Hz for E1) are attenuated at a level of 6 dB per octave, as shown in Figure 24.

Figure 24: - TJAT Jitter Transfer



T1

In the non-attenuating mode, when the FIFO is within one UI of overrunning or under running, the tracking range is 1.48 MHz to 1.608 MHz.

The guaranteed linear operating range for the jittered input clock is 1.544 MHz ± 200 Hz with worst case jitter (61 UIpp), and maximum system clock frequency offset (± 100 ppm). The nominal range is 1.544 MHz ± 963 Hz with no jitter or system clock frequency offset.

E1

In the non-attenuating mode, when the FIFO is within one UI of overrunning or under running, the tracking range is 2.13 MHz to 1.97 MHz.

The guaranteed linear operating range for the jittered input clock is 2.048 MHz ± 300 Hz with worst case jitter (61 UIpp), and maximum system clock frequency offset (± 100 ppm). The nominal range is 2.048 MHz ± 1277 Hz with no jitter or system clock frequency offset.

Jitter Generation

In the absence of input jitter, the output jitter shall be less than 0.025 UIpp. This complies with the AT&T TR 62411 requirement of less than 0.025 UIpp of jitter generation.

1.31 Line Transmitter

The line transmitter generates Alternate Mark Inversion (AMI) transmit pulses suitable for use in the DSX-1 (short haul T1), short haul E1, long haul T1 and long haul E1 environments. The voltage pulses are produced by applying a current to a known termination (termination resistor plus line impedance). The use of current (instead of a voltage driver) simplifies transmit Input Return Loss (IRL), transmit short circuit protection (none needed) and transmit tri-stating.

The output pulse shape is synthesized digitally with current digital-to-analog (DAC) converters, which produce 24 samples per symbol. The current DAC's produce differential bipolar outputs that directly drive the TXTIP[1:0] and TXRING[1:0] pins. The current output is applied to a terminating resistor and line-coupling transformer in a differential manner, which when viewed from the line side of the transformer produce the output pulses at the required levels and insures a small positive to negative pulse imbalance.

The pulse shape is user programmable. For T1 short haul, the cable length between the TLONG and the cross-connect (where the pulse template specifications are given) greatly affects the resulting pulse shapes. Hence, the data applied to the converter must account for different cable lengths. For CEPT E1 applications the pulse template is specified at the transmitter, thus only one setting is required. For T1 long haul with a LBO of 7.5 dB the previous bits effect what the transmitter must drive to compensate for inter-symbol interference; for LBO's of 15 dB or 22.5 dB the previous 3 or 4 bits effect what the transmitter must send out.

Refer to the Operation section for details on creating the synthesized pulse shape.

1.32 Timing Options (TOPS)

The Timing Options block provides a means of selecting the source of the internal input clock to the TJAT block, and the reference clock for the TJAT digital PLL.

1.33 JTAG Test Access Port

The JTAG Test Access Port block provides JTAG support for boundary scan. The standard JTAG EXTEST, SAMPLE, BYPASS, IDCODE and STCTEST instructions are supported. The COMET-Quad identification code is 083140CD hexadecimal.

1.34 Microprocessor Interface

The Microprocessor Interface Block provides normal and test mode registers, the interrupt logic, and the logic required to connect to the Microprocessor Interface. The normal mode registers are required for normal operation, and test mode registers are used to enhance the testability of the COMET-Quad.

NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the COMET-Quad. Normal mode registers (as opposed to test mode registers) are selected when A[10] is low.

The Register Memory Map in Table 4 below shows where the normal mode registers are accessed. The registers are organized so that backward software compatibility with existing PMC devices is optimized. The COMET-Quad contains 1 set of master configuration, H-MVIP, and CSU registers and 4 sets of T1/E1 Framer registers. Where only 1 set is present, the registers apply to the entire device. Where 4 sets are present, the registers apply to a single quadrant of the COMET-Quad. By convention, where 4 sets of registers are present, address space 000H – 0FFH applies to quadrant #1, 100H – 1FFH applies to quadrant #2, 200H – 2FFH applies to quadrant #3, and 300H – 3FFH applies to quadrant #4.

On reset the COMET-Quad defaults to T1 mode. For proper operation some register configuration is expected. System side access defaults to the serial clock and data signals. By default interrupts will not be enabled, and automatic alarm generation is disabled.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.
2. All configuration bits that can be written into can also be read back. This allows the processor controlling the COMET-Quad to determine the programming state of the chip.
3. Writeable normal mode register bits are cleared to zero upon reset unless otherwise noted.
4. Writing into read-only normal mode register bit locations does not affect COMET-Quad operation unless otherwise noted.
5. Certain register bits are reserved. These bits are associated with megacell functions that are unused in this application. To ensure that the COMET-Quad operates as intended, reserved register bits must only be written with their default values unless otherwise stated. Similarly, writing to reserved registers should be avoided unless otherwise stated.

1.35 Normal Mode Register Memory Map

Table 4 - Normal Mode Register Memory Map

Addr	Addr	Addr	Addr	Register
000H	100H	200H	300H	Global Configuration
001H	101H	201H	301H	Clock Monitor
002H	102H	202H	302H	Receive Options

Addr	Addr	Addr	Addr	Register
003H	103H	203H	303H	Receive Line Interface Configuration
004H	104H	204H	304H	Transmit Line Interface Configuration
005H	105H	205H	305H	Transmit Framing and Bypass Options
006H	106H	206H	306H	Transmit Timing Options
007H	107H	207H	307H	Interrupt Source #1
008H	108H	208H	308H	Interrupt Source #2
009H	109H	209H	309H	Interrupt Source #3
00AH	10AH	20AH	30AH	Master Diagnostics
00BH				Master Test
	10BH	20BH	30BH	Reserved
00CH	10CH	20CH	30CH	Reserved
00DH	10DH	20DH	30DH	Revision/Chip ID/Quadrant PMON Update
00EH				Reset
	10EH	20EH	30EH	Reserved
00FH	10FH	20FH	30FH	PRBS Positioning/Control and HDLC Control
010H	110H	210H	310H	CDRC Configuration
011H	111H	211H	311H	CDRC Interrupt Enable
012H	112H	212H	312H	CDRC Interrupt Status
013H	113H	213H	313H	CDRC Alternate Loss of Signal
014H	114H	214H	314H	RJAT Interrupt Status
015H	115H	215H	315H	RJAT Reference Clock Divisor (N1) Control
016H	116H	216H	316H	RJAT Output Clock Divisor (N2) Control
017H	017H	217H	317H	RJAT Configuration
018H	118H	218H	318H	TJAT Interrupt Status
019H	119H	219H	319H	TJAT Reference Clock Divisor (N1) Control
01AH	11AH	21AH	31AH	TJAT Output Clock Divisor (N2) Control
01BH	11BH	21BH	31BH	TJAT Configuration
01CH	11CH	21CH	31CH	RX-ELST Configuration
01DH	11DH	21DH	31DH	RX-ELST Interrupt Enable/Status

Addr	Addr	Addr	Addr	Register
01EH	11EH	21EH	31EH	RX-ELST Idle Code
01FH	11FH	21FH	31FH	RX-ELST Reserved
020H	120H	220H	320H	TX-ELST Configuration
021H	121H	221H	321H	TX-ELST Interrupt Enable/Status
022H-023H	122H-123H	222H-223H	322H-323H	TX-ELST Reserved
024H-027H	124H-127H	224H-227H	324H-327H	Reserved
028H	128H	228H	328H	RXCE Receive Data Link Control
029H	129H	229H	329H	RXCE Receive Data Link Bit Select
02AH-02FH	12AH-12FH	22AH-22FH	032AH-32FH	RXCE Reserved
030H	130H	230H	330H	BRIF Receive Backplane Configuration
031H	131H	231H	331H	BRIF Receive Backplane Frame Pulse Configuration
032H	132H	232H	332H	BRIF Receive Backplane Parity/F-Bit Configuration
033H	133H	233H	333H	BRIF Receive Backplane Timeslot Offset
034H	134H	234H	334H	BRIF Receive Backplane Bit Offset
035H-037H	135H-137H	235H-237H	335H-337H	BRIF Receive Backplane Reserved
038H	138H	238H	338H	TXCI Transmit Data Link Control
039H	139H	239H	339H	TXCI Transmit Data Link Bit Select
03AH-03FH	13AH-13FH	23AH-23FH	033AH-33FH	TXCI Reserved
040H	140H	240H	340H	BTIF Transmit Backplane Configuration
041H	141H	241H	341H	BTIF Transmit Backplane Frame Pulse Configuration
042H	142H	242H	342H	BTIF Transmit Backplane Parity Configuration and Status
043H	143H	243H	343H	BTIF Transmit Backplane Timeslot Offset
044H	144H	244H	344H	BTIF Transmit Backplane Bit Offset Register
045H-047H	145H-147H	245H-247H	345H-347H	BTIF Transmit Backplane Reserved
048H	148H	248H	348H	T1-FRMR Configuration

Addr	Addr	Addr	Addr	Register
049H	149H	249H	349H	T1-FRMR Interrupt Enable
04AH	14AH	24AH	34AH	T1-FRMR Interrupt Status
04BH	14BH	24BH	34BH	Reserved
04CH	14CH	24CH	34CH	IBCD Configuration
04DH	14DH	24DH	34DH	IBCD Interrupt Enable/Status
04EH	14EH	24EH	34EH	IBCD Activate Code
04FH	14FH	24FH	34FH	IBCD Deactivate Code
050H	150H	250H	350H	SIGX Configuration/Change of Signaling State
051H	151H	251H	351H	SIGX µP Access Status/Change of Signaling State
052H	152H	252H	352H	SIGX Channel Indirect Address/Control/ Change of Signaling State
053H	153H	253H	353H	SIGX Channel Indirect Data Buffer/Change of Signaling State
054H	154H	254H	354H	T1 XBAS Configuration
055H	155H	255H	355H	T1 XBAS Alarm Transmit
056H	156H	256H	356H	T1 XIBC Control
057H	157H	257H	357H	T1 XIBC Loopback Code
058H	158H	258H	358H	PMON Interrupt Enable/Status
059H	159H	259H	359H	PMON Framing Bit Error Count
05AH	15AH	25AH	35AH	PMON OOF/COFA/Far End Block Error Count (LSB)
05BH	15BH	25BH	35BH	PMON OOF/COFA/Far End Block Error Count (MSB)
05CH	15CH	25CH	35CH	PMON Bit Error/CRCE Count (LSB)
05DH	15DH	25DH	35DH	PMON Bit Error/CRCE Count (MSB)
05EH	15EH	25EH	35EH	PMON LCV Count (LSB)
05FH	15FH	25FH	35FH	PMON LCV Count (MSB)
060H	160H	260H	360H	T1 ALMI Configuration
061H	161H	261H	361H	T1 ALMI Interrupt Enable
062H	162H	262H	362H	T1 ALMI Interrupt Status
063H	163H	263H	363H	T1 ALMI Alarm Detection Status
064H	164H	264H	364H	T1 PDVD Reserved

Addr	Addr	Addr	Addr	Register
065H	165H	265H	365H	T1 PDVD Interrupt Enable/Status
066H	166H	266H	366H	T1 XBOC Control
067H	167H	267H	367H	T1 XBOC Code
068H	168H	268H	368H	T1 XPDE Reserved
069H	169H	269H	369H	T1 XPDE Interrupt Enable/Status
06AH	16AH	26AH	36AH	T1 RBOC Enable
06BH	16BH	26BH	36BH	T1 RBOC Code Status
06CH	16CH	26CH	36CH	TPSC Configuration
06DH	16DH	26DH	36DH	TPSC µP Access Status
06EH	16EH	26EH	36EH	TPSC Channel Indirect Address/Control
06FH	16FH	26FH	36FH	TPSC Channel Indirect Data Buffer
070H	170H	270H	370H	RPSC Configuration
071H	171H	271H	371H	RPSC µP Access Status
072H	172H	272H	372H	RPSC Channel Indirect Address/Control
073H	173H	273H	373H	RPSC Channel Indirect Data Buffer
074H-077H	174H-177H	274H-277H	374H-377H	Reserved
078H	178H	278H	378H	T1 APRM Configuration/Control
079H	179H	279H	379H	T1 APRM Reserved
07AH	17AH	27AH	37AH	T1 APRM Interrupt Status
07BH	17BH	27BH	37BH	T1 APRM One Second Content Octet 2
07CH	17CH	27CH	37CH	T1 APRM One Second Content Octet 3
07DH	17DH	27DH	37DH	T1 APRM One Second Content Octet 4
07EH	17EH	27EH	37EH	T1 APRM One Second Content MSB (Octet 5)
07FH	17FH	27FH	37FH	T1 APRM One Second Content LSB (Octet 6)
080H	180H	280H	380H	E1 TRAN Configuration
081H	181H	281H	381H	E1 TRAN Transmit Alarm/Diagnostic Control
082H	182H	282H	382H	E1 TRAN International Control
083H	183H	283H	383H	E1 TRAN Extra Bits Control

Addr	Addr	Addr	Addr	Register
084H	184H	284H	384H	E1 TRAN Interrupt Enable
085H	185H	285H	385H	E1 TRAN Interrupt Status
086H	186H	286H	386H	E1 TRAN National Bit Codeword Select
087H	187H	287H	387H	E1 TRAN National Bit Codeword
088H-08BH	188H-18BH	288H-28BH	388H-38BH	Reserved
08CH-08DH	18CH-18DH	28CH-28DH	38CH-38DH	T1-FRMR Reserved
08EH-08FH	18EH-18FH	28EH-28FH	38EH-38FH	Reserved
090H	190H	290H	390H	E1-FRMR Frame Alignment Options
091H	191H	291H	391H	E1-FRMR Maintenance Mode Options
092H	192H	292H	392H	E1-FRMR Framing Status Interrupt Enable
093H	193H	293H	393H	E1-FRMR Maintenance/Alarm Status Interrupt Enable
094H	194H	294H	394H	E1-FRMR Framing Status Interrupt Indication
095H	195H	295H	395H	E1-FRMR Maintenance/Alarm Status Interrupt Indication
096H	196H	296H	396H	E1-FRMR Framing Status
097H	197H	297H	397H	E1-FRMR Maintenance/Alarm Status
098H	198H	298H	398H	E1-FRMR International/National Bits
099H	199H	299H	399H	E1-FRMR CRC Error Count - LSB
09AH	19AH	29AH	39AH	E1-FRMR CRC Error Count - MSB
09BH	19BH	29BH	39BH	E1-FRMR National Bit Codeword Interrupt Enables
09CH	19CH	29CH	39CH	E1-FRMR National Bit Codeword Interrupts
09DH	19DH	29DH	39DH	E1-FRMR National Bit Codewords
09EH	19EH	29EH	39EH	E1-FRMR Frame Pulse/Alarm Interrupt Enables
09FH	19FH	29FH	39FH	E1-FRMR Frame Pulse/Alarm Interrupt
0A0H-0A7H	1A0H-1A7H	2A0H-2A7H	3A0H-3A7H	Reserved
0A8H	1A8H	2A8H	3A8H	TDPR Configuration
0A9H	1A9H	2A9H	3A9H	TDPR Upper Transmit Threshold

Addr	Addr	Addr	Addr	Register
0AAH	1AAH	2AAH	3AAH	TDPR Lower Transmit Threshold
0ABH	1ABH	2ABH	3ABH	TDPR Interrupt Enable
0ACH	1ACH	2ACH	3ACH	TDPR Interrupt Status/UDR Clear
0ADH	1ADH	2ADH	3ADH	TDPR1 Transmit Data
0AEH-0AFH	0AEH-1AFH	2AEH-2AFH	3AEH-3AFH	Reserved
0B0H	1B0H	2B0H	3B0H	RX-ELST CCS Configuration
0B1H	1B1H	2B1H	3B1H	RX-ELST CCS Interrupt Enable/Status
0B2H	1B2H	2B2H	3B2H	RX-ELST CCS Idle Code
0B3H	1B3H	2B3H	3B3H	RX-ELST CCS Reserved
0B4H	1B4H	2B4H	3B4H	TX-ELST CCS Configuration
0B5H	1B5H	2B5H	3B5H	TX-ELST CCS Interrupt Enable/Status
0B6H-0B7H	1B6H-1B7H	2B6H-2B7H	3B6H-3B7H	TX-ELST CCS Reserved
0B8H				Receive H-MVIP/CCS Enable
	1B8H	2B8H	3B8H	Reserved
0B9H	1B9H	2B9H	3B9H	Transmit H-MVIP/CCS Enable and Configuration
0BAH	1BAH	2BAH	3BAH	Reserved
0BBH				RSYNC Select
	1BBH	2BBH	3BBH	Reserved
0BCH				COMET-Quad Master Interrupt Source
	1BCH	2BCH	3BCH	Reserved
0BDH-0BFH	1BDH-1BFH	2BDH-2BFH	3BDH-3BFH	Reserved
0C0H	1C0H	2C0H	3C0H	RDLC Configuration
0C1H	1C1H	2C1H	3C1H	RDLC Interrupt Control
0C2H	1C2H	2C2H	3C2H	RDLC Status
0C3H	1C3H	2C3H	3C3H	RDLC Data
0C4H	1C4H	2C4H	3C4H	RDLC Primary Address Match
0C5H	1C5H	2C5H	3C5H	RDLC Secondary Address Match

Addr	Addr	Addr	Addr	Register
0C6H-0D5H	1C6H-1D5H	2C6H-2D5H	3C6H-3D5H	Reserved
0D6H				CSU Configuration
	1D6H	2D6H	3D6H	Reserved
0D7H				CSU Reserved
	1D7H	2D7H	3D7H	Reserved
0D8H	1D8H	2D8H	3D8H	RLPS Indirect Data Register
0D9H	1D9H	2D9H	3D9H	RLPS Indirect Data Register
0DAH	1DAH	2DAH	3DAH	RLPS Indirect Data Register
0DBH	1DBH	2DBH	3DBH	RLPS Indirect Data Register
0DCH	1DCH	2DCH	3DCH	RLPS Equalizer Loop Voltage Reference
0DDH-0DFH	1DDH-1DFH	2DDH-2DFH	3DDH-3DFH	RLPS Reserved
0E0H	1E0H	2E0H	3E0H	PRBS Generator/Checker Control
0E1H	1E1H	2E1H	3E1H	PRBS Checker Interrupt Enable/Status
0E2H	1E2H	2E2H	3E2H	PRBS Pattern Select
0E3H	1E3H	2E3H	3E3H	PRBS Reserved
0E4H	1E4H	2E4H	3E4H	PRBS Error Count #1
0E5H	1E5H	2E5H	3E5H	PRBS Error Count #2
0E6H	1E6H	2E6H	3E6H	PRBS Error Count #3
0E7H-0EFH	1E7H-1EFH	2E7H-2EFH	3E7H-3EFH	Reserved
0F0H	1F0H	2F0H	3F0H	XLPG Line Driver Configuration
0F1H	1F1H	2F1H	3F1H	XLPG Control/Status
0F2H	1F2H	2F2H	3F2H	XLPG Pulse Waveform Storage Write Address
0F3H	1F3H	2F3H	3F3H	XLPG Pulse Waveform Storage Data
0F4H	1F4H	2F4H	3F4H	XLPG Analog Test Positive Control
0F5H	1F5H	2F5H	3F5H	XLPG Analog Test Negative Control
0F6H	1F6H	2F6H	3F6H	XLPG Fuse Data Select
0F7H	1F7H	2F7H	3F7H	XLPG Reserved

Addr	Addr	Addr	Addr	Register
0F8H	1F8H	2F8H	3F8H	RLPS Configuration and Status
0F9H	1F9H	2F9H	3F9H	RLPS ALOS Detection/Clearance Threshold
0FAH	1FAH	2FAH	3FAH	RLPS ALOS Detection Period
0FBH	1FBH	2FBH	3FBH	RLPS ALOS Clearance Period
0FCH	1FCH	2FCH	3FCH	RLPS Equalization Indirect Address
0FDH	1FDH	2FDH	3FDH	RLPS Equalization Read/WriteB Select
0FEH	1FEH	2FEH	3FEH	RLPS Equalizer Loop Status and Control
0FFH	1FFH	2FFH	3FFH	RLPS Equalizer Configuration
400H-7FFH				Reserved for Test

Register 000H, 100H, 200H, 300H: Global Configuration

Bit	Type	Function	Default
Bit 7	R/W	PIO_OE	0
Bit 6	R/W	PIO	0
Bit 5	R/W	IBCD_IDLE	0
Bit 4	R/W	RSYNC_ALOSB	0
Bit 3	R/W	OOSMFAIS	0
Bit 2	R/W	TRKEN	0
Bit 1	R/W	RXMTKC	0
Bit 0	R/W	E1/T1B	0

PIO_OE:

The programmable I/O output enable, PIO_OE, bit controls the PIO pin. When PIO_OE is logic 1, the PIO pin is configured as an output and driven by the COMET-QUAD. When PIO_OE is logic 0, the PIO pin is configured as an input. Upon reset, the PIO pin is configured as an input.
PIO_OE is only defined for Register 000H. In Registers 100H, 200H, and 300H the bit is unused, and the Default value is 'X'.

PIO:

The programmable I/O, PIO, bit controls/reflects the state of the PIO pin. When the PIO pin is configured as an output, the PIO bit controls the state of the PIO pin. When the PIO pin is configured as an input, the PIO bit reflects the state of the PIO pin. Upon reset, the PIO pin is an input.
PIO is only defined for Register 000H. In Registers 100H, 200H, and 300H the bit is unused, and the Default value is 'X'.

OOSMFAIS:

In E1 mode, this bit controls the receive backplane signaling trunk conditioning in an out of signaling multiframe condition. If OOSMFAIS is set to a logic 0, an OOSMF indication from the E1-FRMR does not affect the BRSIG output. When OOSMFAIS is a logic 1, an OOSMF indication from the E1-FRMR will cause the BRSIG output to be set to all 1's.

RSYNC_ALOSB:

The RSYNC_ALOSB bit controls the source of the loss of signal condition used to control the behaviour of the receive reference presented on the RSYNC. If RSYNC_ALOSB is a logic 0, analog loss of signal is used. If RSYNC_ALOSB is a logic 1, digital loss of signal is used. When the COMET-Quad quadrant is in a loss of signal state, the RSYNC output is derived from XCLK. When the COMET-Quad quadrant is not in a loss of signal state, the RSYNC

output is derived from the receive recovered clock of the selected quadrant.

The quadrant becoming the source of RSYNC is configured in the RSYNC Select register.

IBCD_IDLE:

When the IBCD_IDLE bit is set to logic 1 gaps the data to the inband code detector (IBCD) block during the framing bit. This allows the IBCD to be used to detect an idle code that is inserted only in the payload of the receive DS1 PCM stream. The IBCD must still be programmed to detect the desired pattern, and otherwise operates unchanged. The IBCD_IDLE bit is only valid in T1 mode.

TRKEN:

The TRKEN bit enables receive trunk conditioning upon an out-of-frame condition. If TRKEN is logic 1, the contents of the RX-ELST Idle Code register are inserted into all timeslots (including TS0 and TS16) of BRPCM if the framer is out-of-basic frame (i.e. the OOF status bit is logic 1). The TRKEN bit only has effect if RXELSTBYP bit is logic 0. If TRKEN is a logic 0, receive trunk conditioning can still be performed on a per-timeslot basis via the RPSC Data Trunk Conditioning and Signaling Trunk Conditioning registers.

RXMTKC:

The RXMTKC bit allows global trunk conditioning to be applied to the received data and signaling streams, BRPCM and BRSIG. When RXMTKC is set to logic 1, the data on BRPCM for each channel is replaced with the data contained in the data trunk conditioning registers within RPSC; similarly, the signaling data on BRSIG for each channel is replaced with the data contained in the signaling trunk conditioning registers. When RXMTKC is set to logic 0, the data and signaling signals are modified on a per-channel basis in accordance with the control bits contained in the per-channel control registers within the RPSC.

E1/T1B:

The global E1/T1B bit selects the operating mode of all four of the COMET-Quad quadrants. If E1/T1B is logic 1, the 2.048 Mbit/s E1 mode is selected for all four quadrants. If E1/T1B is logic 0, the 1.544 Mbit/s T1 mode is selected for all four quadrants.

E1/T1B is only defined for Register 000H. In Registers 100H, 200H, and 300H the bit is unused, and the Default value is ‘X’.

Register 001H, 101H, 201H, 301H: Clock Monitor

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	XCLKA	X
Bit 3	R	BTCLKA	X
Bit 2	R	CTCLKA	X
Bit 1	R	BRCLKA	X
Bit 0		Unused	

When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. This register should be read at periodic intervals to detect clock failures.

BTCLKA:

The BTCLK active (BTCLKA) bit detects low to high transitions on the BTCLK input. BTCLKA is set high on a rising edge of BTCLK, and is set low when this register is read.

CTCLKA:

The CTCLK active (CTCLKA) bit detects low to high transitions on the CTCLK input. CTCLKA is set high on a rising edge of CTCLK, and is set low when this register is read.

BRCLKA:

The BRCLK active (BRCLKA) bit detects low to high transitions on the BRCLK input. BRCLKA is set high on a rising edge of BRCLK, and is set low when this register is read.

XCLKA:

The XCLK active (XCLKA) bit detects for low to high transitions on the XCLK input. XCLKA is set high on a rising edge of XCLK, and is set low when this register is read.

XCLKA is only defined for register 301H, although it applies to the XCLK source used by four quadrants. In Registers 001H, 101H, and 201H, the bit is unused and the Default value is ‘X’.

Register 002H, 102H, 202H, 302H: Receive Options

Bit	Type	Function	Default
Bit 7	R/W	RJATBYP	1
Bit 6	R/W	UNF	0
Bit 5	R/W	RXELSTBYP	0
Bit 4	R/W	RSYNC_MEM	0
Bit 3	R/W	RSYNCSEL	0
Bit 2	R/W	WORDERR	0
Bit 1	R/W	CNTNFAS	0
Bit 0	R/W	CCOFA	0

This register allows software to configure the receive functions of each framer.

RJATBYP:

The RJATBYP bit disables jitter attenuation in the receive direction. When receive jitter attenuation is not being used, setting RJATBYP to logic 1 will reduce the latency through the receiver section by typically 40 bits. When RJATBYP is set to logic 0, the RSYNC output and the BRCLK output (if BRCLK is configured to be an output by setting the CMODE bit of the Receive Backplane Configuration register to logic 0), are jitter attenuated. When the RJAT is bypassed, RSYNC and BRCLK are not jitter attenuated.

UNF:

The UNF bit allows the framer to operate with unframed DS-1 or E1 data. When UNF is set to logic 1, the framer is disabled (both the T1-FRMR and E1-FRMR are held reset) and the recovered data passes through the receiver section of the framer without frame or channel alignment. While UNF is set to logic 1, the Alarm Integrator continues to operate and detects and integrates AIS alarm. When UNF is set to logic 0, the framer operates normally, searching for frame alignment on the incoming data.

When UNF is a logic 1, the BRFP pin (if configured as an output) is held low.

RXELSTBYP:

The RXELSTBYP bit allows the Receive Elastic Store (RX-ELST) to be bypassed, eliminating the one frame delay incurred through the RX-ELST. When set to logic 1, the received data and clock inputs to RX-ELST are internally routed directly to the RX-ELST output. If RXELSTBYP is logic 1, the CMODE bit of the Receive Backplane Configuration register must be logic 0 and the FPMODE bit of the Receive Backplane Frame Pulse Configuration register must be logic 0.

In Receive Clock Slave: H-MVIP mode, RXELSTBYP must be programmed to logic 0.

RSYNC_MEM:

The RSYNC_MEM bit controls the RSYNC output under a loss of signal condition (as determined by the RSYNC_ALOSB register bit). When RSYNC_MEM is a logic 1, the RSYNC output is held high during a loss of signal condition. When RSYNC_MEM is a logic 0, the RSYNC output is derived from XCLK during a loss of signal condition.RSYNCSEL:

The RSYNCSEL bit selects the frequency of the receive reference presented on the RSYNC output. If RSYNCSEL is a logic 1, RSYNC will be an 8 kHz clock. If RSYNCSEL is a logic 0, RSYNC will be an 1.544 MHz (T1) or 2.048 MHz (E1) clock.

WORDERR:

In E1 mode, the WORDERR bit determines how frame alignment signal (FAS) errors are reported. When WORDERR is logic 1, one or more errors in the seven bit FAS word results in a single framing error count. When WORDERR is logic 0, each error in a FAS word results in a single framing error count.

CNTNFAS:

In E1 mode, when the CNTNFAS bit is a logic 1, a zero in bit 2 of timeslot 0 of non-frame alignment signal (NFAS) frames results in an increment of the framing error count. If WORDERR is also a logic 1, the word is defined as the eight bits consisting of the seven-bit FAS pattern and bit 2 of timeslot 0 of the next NFAS frame. When the CNTNFAS bit is a logic 0, only errors in the FAS affect the framing error count.

CCOFA

The CCOFA bit determines whether the PMON counts Change-Of-Frame Alignment (COFA) events or out-of-frame (OOF) events. When CCOFA is set to logic 1, COFA events are counted by PMON. When CCOFA is set to logic 0, OOF events are counted by PMON. The CCOFA bit is only valid in T1 mode.

Register 003H, 103H, 203H, 303H: Receive Line Interface Configuration

Bit	Type	Function	Default
Bit 7	R/W	AUTOYELLOW	0
Bit 6	R/W	AUTORED	0
Bit 5	R/W	AUTOOOF	0
Bit 4	R/W	AUTOAIS	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	BPV	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	0

RESERVED:

These bits must be a logic 0 for correct operation.

AUTOYELLOW:

In T1 mode, when the AUTOYELLOW bit is set to logic 1, whenever the alarm integrator declares a Red alarm in the receive direction, Yellow alarm will be transmitted to the far end. When AUTOYELLOW is set to logic 0, Yellow alarm will only be transmitted when the XYEL bit is set in the T1-XBAS Alarm Transmit Register. Note that the Red alarm is not deasserted on detection of AIS.

In E1 mode, when the AUTOYELLOW bit is set to logic 1, The RAI bit in the transmit stream is set to a logic 1 for the duration of a loss of frame alignment or AIS. The G706ANNBRAI bit of the Transmit Framing and Bypass Options register optionally also allows for the transmission of RAI when CRC-to-non-CRC interworking has been established. When AUTOYELLOW is set to logic 0, RAI will only be transmitted when the RAI bit is set in the E1-TRAN Transmit Alarm/Diagnostic Control register.

AUTORED:

The AUTORED bit allows global trunk conditioning to be applied to the receive data and signaling streams, BRPCM and BRSIG, immediately upon declaration of Red carrier failure alarm. When AUTORED is set to logic 1, the data on BRPCM for each channel is replaced with the data contained in the Data Trunk Conditioning registers within RPSC and the data on BRSIG for each channel is replaced with the data contained in the Signaling Trunk Conditioning registers within the RPSC while Red CFA is declared. When AUTORED is set to logic 0, the receive data is not automatically conditioned when Red CFA is declared.

AUTOOOF:

The AUTOOOF bit allows global trunk conditioning to be applied to the receive data stream, BRPCM, immediately upon declaration of out of frame (OOF). When AUTOOOF is set to logic 1, while OOF is declared, the data on BRPCM for each channel is replaced with the data contained in the data trunk conditioning registers within RPSC. When AUTOOOF is set to logic 0, the backplane receive data is not automatically conditioned by RPSC when OOF is declared. However, if the RX-ELST is not bypassed, the RX-ELST trouble code will still be inserted in channel data while OOF is declared if the TRKEN register bit is logic 1. RPSC data and signaling trunk conditioning overwrites the RX-ELST trouble code.

AUTOAIS:

If the AUTOAIS bit is logic 1, AIS is inserted in the receive path and the signaling is frozen for the duration of a loss of signal condition. If AUTOAIS is logic 0, AIS may be inserted manually via the RAIS register bit.

BPV:

In T1 mode, the BPV bit enables only bipolar violations to indicate line code violations and be accumulated in the PMON LCV Count Registers. When BPV is set to logic 1, BPVs (which are not part of a valid B8ZS signature if B8ZS line coding is used) generate an LCV indication and increment the PMON LCV counter. When BPV is set to logic 0, both BPVs (which are not part of a valid B8ZS signature if B8ZS line coding is used) and excessive zeros (EXZ) generate an LCV indication and increment the PMON LCV counter. Excessive zeros is a sequence of zeros greater than fifteen bits long for an AMI-coded signal and greater than seven bits long for a B8ZS-coded signal.

In E1 mode, the BPV bit enables only bipolar violations to indicate line code violations and be accumulated in the PMON LCV Count Registers. (The O162 bit in the CDRC Configuration register provides two E1 LCV definitions.) When BPV is set to logic 1, BPVs (which are not part of a valid HDB3 signature if HDB3 line coding is used) generate an LCV indication and increment the PMON LCV counter. When BPV is set to logic 0, both BPVs (which are not part of a valid HDB3 signature if HDB3 line coding is used) and excessive zeros (EXZ) generate an LCV indication and increment the PMON LCV counter. Excessive zeros is a sequence of zeros greater than four bits long.

Register 004H, 104H, 204H, 304H: Transmit Line Interface Configuration

Bit	Type	Function	Default
Bit 7	R/W	TJATBYP	0
Bit 6	R/W	TAISEN	0
Bit 5	R/W	TAUXP	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2		Unused	X
Bit 1	R/W	Reserved	0
Bit 0		Unused	X

RESERVED:

These bits must be a logic 0 for correct operation.

TJATBYP:

The TJATBYP bit enables the transmit jitter attenuator's FIFO to be removed from the transmit data path. When transmit jitter attenuation is not being used, setting TJATBYP to logic 1 will reduce the latency through the transmitter section by typically 40 bits.

TAISEN:

The TAISEN bit enables the interface to generate an unframed all-ones AIS alarm on the TXTIP and TXRING. When TAISEN is set to logic 1, the bipolar TXTIP and TXRING outputs are forced to pulse alternately, creating an all-ones signal. The transition to transmitting AIS on the TXTIP and TXRING outputs is done in such a way as to not introduce any bipolar violations.

The diagnostic loopback point is upstream of this AIS insertion point.

TAUXP:

The TAUXP bit enables the interface to generate an unframed alternating zeros and ones (i.e. 010101...) auxiliary pattern (AUXP) on the TXTIP and TXRING. When TAUXP is set to logic 1, the bipolar TXTIP and TXRING outputs are forced to pulse alternately every other cycle. The transition to transmitting AUXP on the TXTIP and TXRING outputs is done in such a way as to not introduce any bipolar violations.

The diagnostic loopback point is upstream of this AUXP insertion point.

Register 005H, 105H, 205H, 305H : Transmit Framing and Bypass Options

Bit	Type	Function	Default
Bit 7	R/W	PATHCRC	0
Bit 6	R/W	G706ANNBRAI	0
Bit 5	R/W	SIGAEN	0
Bit 4	R/W	OOCMFE0	0
Bit 3	R/W	FDIS	0
Bit 2	R/W	FBITBYP	0
Bit 1	R/W	CRCBYP	0
Bit 0	R/W	FDLBYP	0

This register allows software to configure the bypass and framing options of the transmitter, the use of the Signaling Alignment block, and controls the global transmit framing disable.

PATHCRC:

This bit only has effect in E1 mode.

When in E1 mode, the PATHCRC bit allows upstream block errors to be preserved in the transmit CRC bits. If PATHCRC is a logic 1, the CRC-4 bits are modified to reflect any bit values in BTPCM which have changed prior to transmission. When PATHCRC is set to logic 0, a new CRC-4 value overwrites the incoming CRC-4 word. For the PATHCRC bit to be effective, the FPTYP bit of the Transmit Backplane Frame Pulse Configuration register must be a logic 1; otherwise, the identification of the incoming CRC-4 bits would be impossible. The PATHCRC bit only takes effect if the GENCRC bit of the E1-TRAN Configuration register is a logic 1 and either the INDIS or FDIS bit in the same register are set to logic 1.

G706ANNBRAI:

When in E1 mode, the G.706 Annex B RAI bit, G706ANNBRAI, selects between two modes of operation concerning the transmission of RAI when the COMET-Quad quadrant is out of CRC-4 multiframe. When G706ANNBRAI is logic 1, the behaviour of RAI follows Annex B of G.706, i.e., RAI is transmitted only when out of basic frame, not when CRC-4-to-non-CRC-4 interworking is declared, nor when the offline framer is out of frame. When G706ANNBRAI is logic 0, the behaviour of RAI follows ETSI standards, i.e., RAI is transmitted when out of basic frame, when CRC-4-to-non-CRC-4 interworking is declared, and when the offline framer is out of frame.

This bit only has effect in E1 mode.

SIGAEN:

The SIGAEN bit enables the operation of the signaling aligner (SIGA) to ensure superframe alignment of signaling bits between the backplane and the transmit DS-1 stream. When set to logic 1, the SIGA is inserted into the signaling bit data path before the T1-XBAS. When the signaling aligner is used, the backplane frame alignment indication must also be changed to indicate superframe alignment for the transmit backplane. When SIGAEN is set to logic 0, the SIGA is removed from the circuit.

This bit has no effect in E1 mode.

OOCMFE0:

When in E1 mode, the OOCMFE0 bit selects between two modes of operation concerning the transmission of E-bits when the COMET-Quad quadrant is out of CRC-4 multiframe. When OOCMFE0 is logic 0, the COMET-Quad quadrant transmits ones for the E-bits while out of CRC-4 multiframe. When OOCMFE0 is logic 1, the COMET-Quad quadrant transmits zeroes for the E-bits while out of CRC-4 multiframe. The option to transmit zeroes as E-bits while out of CRC-4 multiframe is provided to allow compliance with the CRC-4 to non-CRC-4 interworking procedure in Annex B of G.706.

This bit only has effect in E1 mode.

FDIS:

The FDIS bit allows the framing generation through the transmitter to be disabled and the transmit data to pass through the transmitter unchanged. When FDIS is set to logic 1, the transmitter is disabled from generating framing. When FDIS is set to logic 0, the transmitter is enabled to generate and insert the framing into the transmit data.

FBITBYP:

The FBITBYP bit allows the frame synchronization bit in the input data stream, BTPCM, to bypass the generation through the XBAS and be re-inserted into the appropriate position in the digital output stream. When FBITBYP is set to logic 1, the input frame synchronization bit is re-inserted into the output data stream. When FBITBYP is set to logic 0, the XBAS is allowed to generate the output frame synchronization bits.

This bit must be set to logic 0 when not in T1 ESF mode.

CRCBYP:

In T1 mode, when the CRCBYP bit is a logic 1, the framing bit corresponding to the CRC-6 bit position in the input data stream, BTPCM, passes transparently to the transmit output data stream. When CRCBYP is set to logic 0, the XBAS is allowed to generate the output CRC-6 bits.

This bit must be set to logic 0 when not in T1 ESF mode.

FDLBYP:

In T1 mode, when the FDLBYP bit is a logic 1, the framing bit corresponding to the facility data link bit position in the input data stream, BTPCM, passes transparently to the transmit output data stream. When FDLBYP is set to logic 0, the XBAS is allowed to generate the output facility data link.

This bit must be set to logic 0 when not in T1 ESF mode.

Register 006H, 106H, 206H, 306H: Transmit Timing Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	OCLKSEL1	0
Bit 4	R/W	OCLKSEL0	0
Bit 3	R/W	PLLREF1	0
Bit 2	R/W	PLLREF0	0
Bit 1		Unused	X
Bit 0	R/W	TXELSTBYP	1

This register allows software to configure the options of the transmit timing section.

TXELSTBYP:

The TXELSTBYP bit allows the Transmit Elastic Store (TX-ELST) to be bypassed, eliminating the one frame delay incurred through the TX-ELST. When set to logic 1, the received data and clock inputs to TX-ELST are internally routed directly to the TX-ELST outputs.

OCLKSEL1, OCLKSEL0:

The OCLKSEL[1:0] bits select the source of the Transmit Jitter Attenuator FIFO output clock signal.

Table 5 - TJAT FIFO Output Clock Source

OCLKSEL1	OCLKSEL0	Source of FIFO Output Clock
0	0	The TJAT FIFO output clock is driven with the internal jitter-attenuated 1.544 MHz or 2.048 MHz clock.
0	1	The TJAT FIFO output clock is driven with the CTCLK input clock.
1	X	The TJAT FIFO output clock is driven with the FIFO input clock. In this mode the jitter attenuation is disabled and the input clock must be jitter-free.

PLLREF1, PLLREF0:

The PLLREF[1:0] bits select the source of the Transmit Jitter Attenuator phase locked loop reference signal as follows:

Table 6 - TJAT PLL Source

PLLREF1	PLLREF0	Source of PLL Reference
0	0	TJAT FIFO input clock (either the conditioned BTCLK or the receive recovered clock, as selected by LINELB, assuming the TX-ELST is bypassed)
0	1	conditioned BTCLK input (assuming the TX-ELST is bypassed)
1	0	Receive recovered clock
1	1	CTCLK input

If the BTCLK is configured as an output (CMODE bit of the Transmit Backplane Configuration register is a logic 0), only the recovered clock or the CTCLK input should be selected, or else the timing becomes self-referential and unpredictable.

The following table illustrates the required bit settings for these various clock sources to affect the transmitted data:

Table 7 - Transmit Timing Options Summary

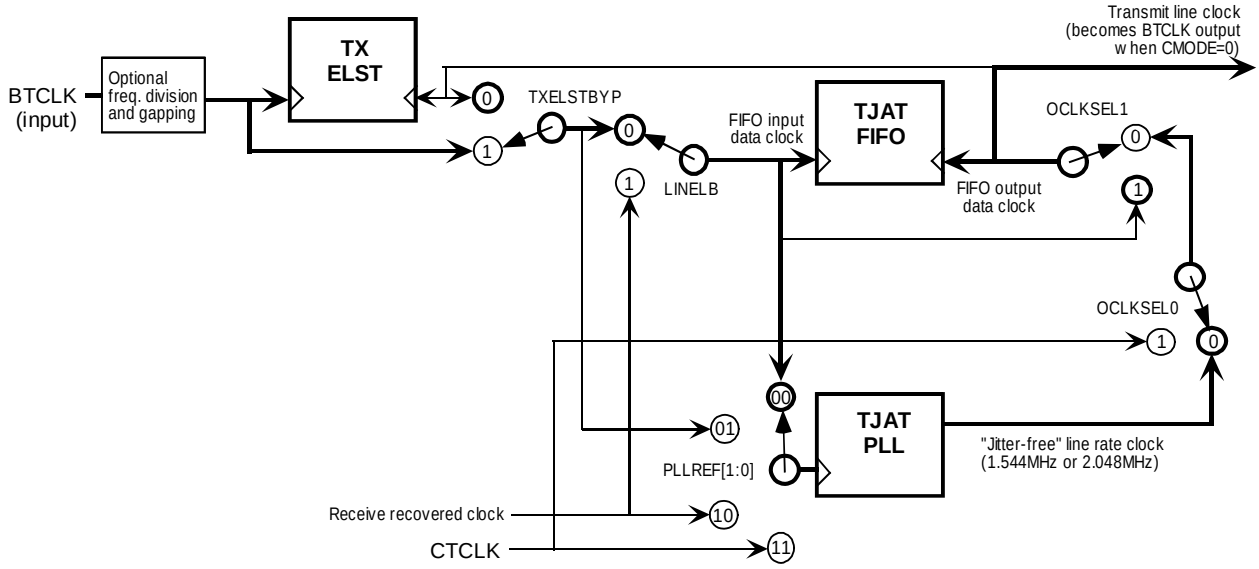
Input Transmit Data	Bit Settings	Effect on Output Transmit Data
Synchronous to BTCLK input. Transmit Backplane Configuration register CMODE =1.	OCLKSEL1=0 OCLKSEL0=0 PLLREF1=0 PLLREF0=X LINELB=0 TXELSTBYP=1	Jitter attenuated. Transmit clock is a smooth 1.544 MHz or 2.048 MHz. Transmit clock referenced to BTCLK input. TX-ELST bypassed.
Synchronous to BTCLK output. Transmit Backplane Configuration register CMODE =0.	OCLKSEL1=0 OCLKSEL0=0 PLLREF1=1 PLLREF0=0 LINELB=0 TXELSTBYP=1	Jitter attenuated looptiming. Transmit clock is a smooth 1.544 MHz or 2.048 MHz. Loop timed to the receive recovered clock. TX-ELST bypassed.
Synchronous to BTCLK input. Transmit Backplane Configuration register CMODE =1.	OCLKSEL1=0 OCLKSEL0=0 PLLREF1=1 PLLREF0=0 LINELB=0 TXELSTBYP=0	Jitter attenuated looptiming. Transmit clock is a smooth 1.544 MHz or 2.048 MHz. Loop timed to the receive recovered clock. TX-ELST allows BTCLK to be plesiochronous.

Input Transmit Data	Bit Settings	Effect on Output Transmit Data
Synchronous to BTCLK output. Transmit Backplane Configuration register CMODE =0.	OCLKSEL1=0 OCLKSEL0=0 PLLREF1=1 PLLREF0=1 LINELB=0 TXELSTBYP=1	Jitter attenuated. Transmit clock is a smooth 1.544 MHz or 2.048 MHz. Transmit clock and BTCLK referenced to CTCLK input. TX-ELST bypassed.
Synchronous to BTCLK input. Transmit Backplane Configuration register CMODE =1.	OCLKSEL1=0 OCLKSEL0=0 PLLREF1=1 PLLREF0=1 LINELB=0 TXELSTBYP=0	Jitter attenuated. Transmit clock is a smooth 1.544 MHz or 2.048 MHz. Transmit clock referenced to CTCLK input. TX-ELST allows BTCLK to be plesiochronous.
Synchronous to BTCLK input. Transmit Backplane Configuration register CMODE =1.	OCLKSEL1=1 OCLKSEL0=X PLLREF1=X PLLREF0=X LINELB=0 TXELSTBYP=1	No jitter attenuation. Transmit clock is equivalent to BTCLK. TX-ELST bypassed.
Synchronous to BTCLK output. Transmit Backplane Configuration register CMODE =0.	OCLKSEL1=0 OCLKSEL0=1 PLLREF1=1 PLLREF0=1 LINELB=0 TXELSTBYP=1	No jitter attenuation. Transmit clock is equal to CTCLK (useful for higher rate MUX applications). The BTCLK output referenced to CTCLK. TX-ELST bypassed.
Synchronous to BTCLK input. Transmit Backplane Configuration register CMODE =1.	OCLKSEL1=0 OCLKSEL0=1 PLLREF1=X PLLREF0=X LINELB=0 TXELSTBYP=0	No jitter attenuation. Transmit clock is equal to CTCLK (useful for higher rate MUX applications). TX-ELST allows BTCLK to be plesiochronous.

Input Transmit Data	Bit Settings	Effect on Output Transmit Data
Transmit data ignored. Receive data is looped back.	OCLKSEL1=0 OCLKSEL0=0 PLLREF1=X PLLREF0=0 LINELB=1 TXELSTBYP=X	Line loopback with jitter attenuation.

Upon reset of the COMET-QUAD, these bits are cleared to zero, selecting jitter attenuation with Transmit clock referenced to the backplane transmit clock, BTCLK. Figure 25 illustrates the various bit setting options, with the reset condition highlighted.

Figure 25 - Transmit Timing Options



Register 007H, 107, 207H, 307H: Interrupt Source #1

Bit	Type	Function	Default
Bit 7	R	PMON	X
Bit 6	R	PRBS	X
Bit 5	R	FRMR	X
Bit 4	R	SIGX	X
Bit 3	R	APRM	X
Bit 2	R	TJAT	X
Bit 1	R	RJAT	X
Bit 0	R	CDRC	X

This register allows software to determine the block which produced the interrupt on the INTB output pin. A logic 1 indicates an interrupt was produced from the block.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Register 008H, 108H, 208H, 308H: Interrupt Source #2

Bit	Type	Function	Default
Bit 7	R	RX-ELST	X
Bit 6	R	RX-ELST CCS	X
Bit 5	R	Unused	X
Bit 4	R	RDLC	X
Bit 3	R	TX-ELST	X
Bit 2	R	TX-ELST CCS	X
Bit 1	R	XBOC	X
Bit 0	R	TDPR	X

This register allows software to determine the block that produced the interrupt on the INTB output pin. A logic 1 indicates an interrupt was produced from the block.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Register 009H, 109H, 209H, 309H: Interrupt Source #3

Bit	Type	Function	Default
Bit 7	R	IBCD	X
Bit 6	R	PDVD	X
Bit 5	R	RBOC	X
Bit 4	R	XPDE	X
Bit 3	R	ALMI	X
Bit 2	R	TRAN	X
Bit 1	R	RLPS	X
Bit 0	R	BTIF	X

This register allows software to determine the block that produced the interrupt on the INTB output pin. A logic 1 indicates an interrupt was produced from the block.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Register 00AH, 10AH, 20AH, 30AH: Master Diagnostics

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PAYLB	0
Bit 4	R/W	LINELB	0
Bit 3	R/W	RAIS	0
Bit 2	R/W	DDLB	0
Bit 1	R/W	TXMFP	0
Bit 0		Reserved	0

RESERVED:

This bit must be a logic 0 for correct operation.

PAYLB:

The PAYLB bit selects the payload loopback mode, where the received data output from the RX-ELST is internally connected to the transmit data input of the transmitter. The data read out of RX-ELST is timed to the transmitter clock, and the transmit frame alignment is used to synchronize the output frame alignment of RX-ELST. The transmit frame alignment is either arbitrary (when the TX-ELST is used) or is specified by the BTFP input (when the TX-ELST is bypassed). During payload loopback, the data on BRPCM is only valid when the COMET-Quad quadrant is configured as a BRCLK master, BRFP master and the RX-ELST is bypassed. In all other modes, the BRPCM output is forced to all-ones. When PAYLB is set to logic 1, the payload loopback mode is enabled. When PAYLB is set to logic 0, the loopback mode is disabled. In T1 mode, if the TDPR is configured to send performance reports from the T1-APRM, this bit requires two updating cycles before being included in the performance report.

LINELB:

The LINELB bit selects the line loopback mode, where the recovered data are internally directed to the digital inputs of the transmit jitter attenuator. The data sent to the TJAT is the recovered data from the output of the CDRC block. When LINELB is set to logic 1, the line loopback mode is enabled. When LINELB is set to logic 0, the line loopback mode is disabled. Note that when line loopback is enabled, to correctly attenuate the jitter on the receive clock, the contents of the TJAT Reference Clock Divisor and Output Clock Divisor registers should be programmed to 2FH and the Transmit Timing Options register should be cleared to all zeros.

RAIS:

When a logic 1, the RAIS bit forces all ones into the BRPCM data stream. The BRSIG data stream will freeze at the current valid signaling. This capability is provided to indicate the unavailability of the line when line loopback is active.

DDLB:

The DDLB bit selects the diagnostic digital loopback mode, where the COMET-Quad quadrant is configured to internally direct the output of the TJAT to the inputs of the receiver section. The dual-rail RZ outputs of the TJAT are directed to the dual-rail inputs of the CDRC. When DDLB is set to logic 1, the diagnostic digital loopback mode is enabled. When DDLB is set to logic 0, the diagnostic digital loopback mode is disabled.

TXMFP:

In T1 mode, the TXMFP bit introduces a mimic framing pattern in the digital output of the basic transmitter by forcing a copy of the current framing bit into bit location 1 of the frame, thereby creating a mimic pattern in the bit position immediately following the correct framing bit. When TXMFP is set to logic 1, the mimic framing pattern is generated. When TXMFP is set to logic 0, no mimic pattern is generated.

Register 00BH: Master Test

Bit	Type	Function	Default
Bit 7	W	OVR	X
Bit 6	W	IDDQEN	X
Bit 5	W	PMCATST	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to select COMET-Quad test features. All bits, except for OVR, PMCTST, PMCATST and IDDQEN are reset to zero by a hardware reset of the COMET; a software reset of the COMET-Quad does not affect the state of the bits in this register. This register can be written via address 00BH, 10BH, 20BH, or 30BH, but can be read only via address 00BH. Refer to the Test Features Description section for more information.

OVR:

The OVR bit disables the QUAD_TM[1:0] bits of the Master Test Control register. When PMCTST is logic 1 and OVR is logic 1, the QUAD_TM[1:0] bits have no effect and A[9:8] select the quadrant for read and write accesses. The OVR bit cleared by setting CSB high or by writing OVR to logic 0.

This bit only has effect when PMCTST or IOTST is logic 1.

IDDQEN:

The IDDQEN bit is used to configure the COMET-Quad for IDDQ tests. IDDQEN is cleared when CSB is high and RSTB is low or when IDDQEN is written as logic 0. When the IDDQEN bit is set to logic 1, the HIGHZ bit in the XLPG Line Driver Configuration register must also be set to logic 1.

PMCATST:

The PMCATST bit is used to configure the analog portion of the COMET-Quad for PMC's manufacturing tests. PMCATST is cleared when CSB is high and RSTB is low or when PMCATST is written as logic 0.

PMCTST:

The PMCTST bit is used to configure the COMET-Quad for PMC's manufacturing tests. When PMCTST is set to logic 1, the COMET-Quad microprocessor port becomes the test

access port used to run the PMC manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and is cleared by setting CSB high.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the COMET-Quad to drive the data bus with the value last read from quadrant #1. Holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit only has effect when the IOTST bit is set to logic 1. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the COMET-Quad for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the Test Features Description section).

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the COMET-Quad. While the HIZIO bit is a logic 1, all output pins of the COMET-Quad except TDO and the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is held in a high-impedance state which inhibits microprocessor read cycles.

Register 00DH, 10DH, 20DH, 30DH: Revision/Chip ID/Quadrant PMON Update

Bit	Type	Function	Default
Bit 7	R	TYPE[2]	0
Bit 6	R	TYPE[1]	1
Bit 5	R	TYPE[0]	0
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	0

The version identification bits, ID[4:0], are set to a fixed value representing the version number of the COMET-Quad. The TYPE[2:0] and ID[4:0] bits are only defined for Register 00DH. In Registers 10DH, 20DH, and 30DH, the bits are undefined and the Default value is ‘X’.

The chip identification bits, TYPE[2:0], are set to “010” representing the COMET-Quad.

Writing any value to this register causes all performance monitor counters in the quadrant to be updated simultaneously.

Register 00EH: Reset

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	RESET	0

RESET:

The RESET bit implements a software reset. If the RESET bit is a logic 1, the COMET-Quad is held in reset. This bit is not self-clearing; therefore, a logic 0 must be written to bring the COMET-Quad out of reset. Holding the COMET-Quad in a reset state effectively puts it into a low-power, stand-by mode. A hardware reset clears the RESET bit, thus deasserting the software reset.

Register 00FH, 10FH, 20FH, 30FH: PRBS Positioning/Control and HDLC Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	HDLC_DIS	0
Bit 4	R/W	Nx56K_GEN	0
Bit 3	R/W	Nx56K_DET	0
Bit 2	R/W	RXPATGEN	0
Bit 1	R/W	UNF_GEN	0
Bit 0	R/W	UNF_DET	0

This register modifies the way in which the PRBS generator/checker is used by the TPSC and RPSC.

HDLC_DIS:

The HDLC_DIS bit, when set to logic 1, is used to disable the clock to the TDPR and RDLC, putting them into a low power, stand-by mode. When the HDLC_DIS bit is set to logic 0, the clock to the TDPR and RDLC is enabled.

Nx56K_GEN:

The Nx56K_GEN bit is active when the RPSC or TPSC is used to insert PRBS into selected channels of the transmit or receive stream. When the Nx56Kbit/s generation bit is set to logic 1, the pattern is only inserted in the first 7 bits of the selected channels, and gapped on the eighth bit. This is particularly useful when using the jammed-bit-8 zero code suppression in the transmit direction, for instance when sending a Nx56Kbit/s fractional T1/E1 loopback sequence. This bit has no effect when UNF_GEN is set to logic 1.

Nx56K_DET:

The Nx56K_DET bit is active when the RPSC or TPSC is used to detect PRBS in selected channels of the transmit or receive stream. When the Nx56Kbit/s detection bit is set to logic 1, the pattern generator only looks at the first 7 bits of the selected channels, and gaps out the eighth bit. This is particularly useful when searching for fractional T1 loopback codes in an Nx56Kbit/s fractional T1 signal. This bit has no effect when UNF_DET is set to logic 1.

RXPATGEN:

The Receive Pattern Generate, RXPATGEN, bit controls the location of the PRBS generator/detector. When RXPATGEN is set to logic 1, the PRBS generator is inserted in the receive path and the PRBS checker is inserted in the transmit path. Timeslots from the receive line may be overwritten with generated PRBS patterns before appearing on the

receive system interface, and timeslots from the transmit system interface may be checked for the generated pattern before appearing on the transmit line. When RXPATGEN is set to logic 0, the PRBS detector is inserted in the receive path and the PRBS generator is inserted in the transmit path. Timeslots from the transmit system interface may be overwritten with generated PRBS patterns before appearing on the transmit line, and timeslots from the receive line may be checked for the generated pattern before appearing on the receive system interface.

UNF_GEN

When the Unframed Pattern Generation bit, UNF_GEN, is set to logic 1, the PRBS Generator will overwrite all 193 bits/256 bits in every frame in the direction specified by the RXPATGEN bit. If the generator is enabled in the transmit path, unless signaling and/or framing is disabled, the transmitter will still overwrite the signaling bit positions and/or the framing bit position. Similarly, if pattern generation is enabled in the receive direction, the pattern will overwrite the framing bit positions. The UNF_GEN bit overrides any per-timeslot pattern generation specified in the TPSC or RPSC. When RXPATGEN = 0, UNF_GEN also overrides idle code insertion and data inversion in the transmit direction, just like the TEST bit in the TPSC.

UNF_DET

When the Unframed Pattern Detection bit, UNF_DET, is set to logic 1, the PRBS Checker will search for the pattern in all 193 bits/256 bits of the transmit or receive stream, depending on the setting of RXPATGEN. The UNF_DET bit overrides any per-timeslot pattern detection specified in the TPSC or RPSC.

Register 010H, 110H, 210H, 310H: CDRC Configuration

Bit	Type	Function	Default
Bit 7	R/W	AMI	0
Bit 6	R/W	LOS[1]	0
Bit 5	R/W	LOS[0]	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	ALGSEL	0
Bit 1	R/W	O162	0
Bit 0	R/W	Reserved	0

Reserved:

These bits must be a logic 0 for correct operation.

O162:

If the AMI bit is logic 0 in E1 mode, the Recommendation O.162 compatibility select bit (O162) allows selection between two line code violation definitions:

If O162 is a logic 0, a line code violation is indicated if the serial stream does not match the verbatim HDB3 definition given in Recommendation G.703. A bipolar violation that is not part of an HDB3 signature or a bipolar violation in an HDB3 signature that is the same polarity as the last bipolar violation results in a line code violation indication.

If O162 is a logic 1, a line code violation is indicated if a bipolar violation is of the same polarity as the last bipolar violation, as per Recommendation O.162.

The O162 bit has no effect in T1 mode.

ALGSEL:

The Algorithm Select (ALGSEL) bit specifies the algorithm used by the DPLL for clock and data recovery. The choice of algorithm determines the high frequency input jitter tolerance of the CDRC. When ALGSEL is set to logic 1, the CDRC jitter tolerance is increased to approach 0.5 UIpp for jitter frequencies above 20 kHz. When ALGSEL is set to logic 0, the jitter tolerance is increased for frequencies below 20 kHz (i.e. the tolerance is improved by 20% over that of ALGSEL=1 at these frequencies), but the tolerance approaches 0.4 UIpp at the higher frequencies.

AMI:

The alternate mark inversion (AMI) bit specifies the line coding of the incoming signal. A logic 1 selects AMI line coding by disabling HDB3 decoding if E1 mode and B8ZS in T1 mode. In E1 mode, a logic 0 selects HDB3 line decoding which entails substituting an HDB3 signature with four zeros. In T1 mode, a logic 0 selects B8ZS line decoding which entails substituting an B8ZS signature with eight zeros.

LOS[1:0]:

The loss of signal threshold is set by the operating mode and the state of the AMI, LOS[1] and LOS[0] bits:

Table 8 - Loss of Signal Thresholds

Mode	AMI	LOS[1]	LOS[0]	Threshold (PCM periods)
E1	0	0	0	10
T1	0	0	0	15
X	1	0	0	15
X	X	0	1	31
X	X	1	0	63
X	X	1	1	175

When the number of consecutive zeros on the incoming PCM line exceeds the programmed threshold, the LOSV status bit is set. For example, if the threshold is set to 10, the 11th zero causes the LOSV bit to be set.

Register 011H, 111H, 211H, 311H: CDRC Interrupt Control

Bit	Type	Function	Default
Bit 7	R/W	LCVE	0
Bit 6	R/W	LOSE	0
Bit 5	R/W	LCSDE	0
Bit 4	R/W	ZNDE	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The bit positions LCVE, LOSE, LCSDE and ZNDE (bits 7 to 4) of this register are interrupt enables to select which of the status events (Line Code Violation , Loss Of Signal, HDB3 signature, B8ZS signature or N Zeros), either singly or in combination, are enabled to generate an interrupt on the microprocessor INTB pin when they are detected. A logic 1 bit in the corresponding bit position enables the detection of these signals to generate an interrupt; a logic 0 bit in the corresponding bit position disables that signal from generating an interrupt.

When the COMET-Quad is reset, LCVE, LOSE, LCSDE and ZNDE are set to logic 0, disabling these events from generating an interrupt.

Register 012H, 112H, 212H, 312H: CDRC Interrupt Status

Bit	Type	Function	Default
Bit 7	R	LCVI	X
Bit 6	R	LOSI	X
Bit 5	R	LCSDI	X
Bit 4	R	ZNDI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	LOSV	X

The ZNDI, LCSDI, LOSI and LCVI (bits 4 to 7) of this register indicate which of the status events have occurred since the last time this register was read. A logic 1 in any of these bit positions indicates that the corresponding event was detected.

Bits ZNDI, LCSDI, LOSI and LCVI are cleared to logic 0 by reading this register.

LOSV:

The LOSV bit reflects the status of the LOS alarm.

ZNDI:

The consecutive zeros detection interrupt (ZNDI) indicates that N consecutive spaces have occurred, where N is four for E1 and eight for T1. This bit can be used to detect an AMI coded signal.

LCSDI:

The line code signature detection interrupt (LCSDI) indicates that a valid line code signature has occurred. In T1 mode, the B8ZS signature is defined as 000+-0-+ if the previous impulse is positive, or 000-+0+- if it is negative. In E1 mode, a valid HDB3 signature is defined as a bipolar violation preceded by two zeros. This bit can be used to detect an HDB3 coded signal in E1 mode and B8ZS coded signal in T1.

LOSI:

The LOSI bit is set to a logic 1 when the LOSV bit changes state.

LCVI:

The line code violation interrupt (LCVI) indicates a series of marks and spaces has occurred in contradiction to the defined line code (AMI, B8ZS or HDB3).

Register 013H, 113H, 213H, 313H: Alternate Loss of Signal Status

Bit	Type	Function	Default
Bit 7	R/W	ALTLOSE	0
Bit 6	R	ALTLOSI	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	ALTLOS	X

The alternate loss of signal status provides a more stringent criteria for the deassertion of the alarm than the LOS indication in the CDRC Interrupt Status register.

ALTLOSE:

If the ALTLOSE bit is a logic 1, the INTB output is asserted low when the ALTLOS status bit changes state.

ALTLOSI:

The ALTLOSI bit is set high when the ALTLOS status bit changes state. It is cleared when this register is read.

ALTLOS:

The ALTLOS bit is asserted upon the absence of marks for the threshold of bit periods specified by the LOS[1:0] register bits. The ALTLOS bit is deasserted only after pulse density requirements have been met. In T1 mode, there must be N ones in each and every time window of 8(N+1) data bits (where N can equal 1 through 23). In E1 mode, ALTLOS is deasserted only after 255 bit periods during which no sequence of four zeros has been received.

Register 014H, 114H, 214H, 314H: RJAT Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OVRI	X
Bit 0	R	UNDI	X

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the receive FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred. Reading this register will clear the UNDI bit to logic 0.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the receive FIFO when the FIFO is already full. When OVRI is a logic 1, an overrun event has occurred. Reading this register will clear the OVRI bit to logic 0.

Register 015H, 115H, 215H, 315H: RJAT Divider N1 Control

Bit	Type	Function	Default
Bit 7	R/W	N1[7]	0
Bit 6	R/W	N1[6]	0
Bit 5	R/W	N1[5]	1
Bit 4	R/W	N1[4]	0
Bit 3	R/W	N1[3]	1
Bit 2	R/W	N1[2]	1
Bit 1	R/W	N1[1]	1
Bit 0	R/W	N1[0]	1

This register contains an 8-bit binary number, N1, which is one less than the magnitude of the reference clock divisor. The reference divisor magnitude, (N1+1), is the ratio between the frequency of the recovered clock (or the transmit clock if a diagnostic loopback is enabled) and the frequency at the phase discriminator input.

Writing to this register will reset the PLL.

The default value of N1 after a device reset is 47 = 2FH.

Register 016H, 116H, 216H, 316H: RJAT Divider N2 Control

Bit	Type	Function	Default
Bit 7	R/W	N2[7]	0
Bit 6	R/W	N2[6]	0
Bit 5	R/W	N2[5]	1
Bit 4	R/W	N2[4]	0
Bit 3	R/W	N2[3]	1
Bit 2	R/W	N2[2]	1
Bit 1	R/W	N2[1]	1
Bit 0	R/W	N2[0]	1

This register contains an 8-bit binary number, N2, which is one less than the magnitude of the output clock divisor. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock, BRCLK, and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL.

The default value of N2 after a device reset is 47 = 2FH.

Register 017H, 117H, 217H, 317H: RJAT Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	CENT	0
Bit 3	R/W	UNDE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	FIFORST	0
Bit 0	R/W	LIMIT	1

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions.

UNDE:

Setting the UNDE bit to logic 1 enables an underrun event to assert the INTB output low.

OVRE:

Setting the OVRE bit to logic 1 enables an overrun event to assert the INT output low.

FIFORST:

Setting the FIFORST bit allows the FIFO to reset when the PLL is reset by software. When FIFORST is logic 1, writing to the PLL Divider Control Registers N1 and N2 will cause both the PLL and FIFO to reset. When FIFORST is logic 0, writing to the Divider Control Registers N1 and N2 will cause only the PLL to reset.

LIMIT:

Setting the LIMIT bit to logic 1 will limit the PLL jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one UI of overflowing or underflowing. This limiting of jitter ensures that no data is lost during

high phase shift conditions. When LIMIT is set to logic 0, underflows and overflows may occur.

It is recommended the LIMIT be left at its logic 1 default.

Register 018H, 118H, 218H, 318H: TJAT Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OVRI	X
Bit 0	R	UNDI	X

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the transmit FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred. Reading this register will clear the UNDI bit to logic 0.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the transmit FIFO when the FIFO is already full. When OVRI is a logic 1, an overrun event has occurred. Reading this register will clear the OVRI bit to logic 0.

Register 019H, 119H, 219H, 319H: TJAT Jitter Attenuator Divider N1 Control

Bit	Type	Function	Default
Bit 7	R/W	N1[7]	0
Bit 6	R/W	N1[6]	0
Bit 5	R/W	N1[5]	1
Bit 4	R/W	N1[4]	0
Bit 3	R/W	N1[3]	1
Bit 2	R/W	N1[2]	1
Bit 1	R/W	N1[1]	1
Bit 0	R/W	N1[0]	1

This register contains an 8-bit binary number, N1, which is one less than the magnitude of the reference clock divisor. The reference divisor magnitude, (N1+1), is the ratio between the frequency of the reference clock (as selected by the PLLREF1 and PLLREF0 bits of the Transmit Timing Options register) and the frequency at the phase discriminator input.

Writing to this register will reset the PLL.

The default value of N1 after a device reset is 47 = 2FH.

Register 01AH, 11AH, 21AH, 31AH: TJAT Divider N2 Control

Bit	Type	Function	Default
Bit 7	R/W	N2[7]	0
Bit 6	R/W	N2[6]	0
Bit 5	R/W	N2[5]	1
Bit 4	R/W	N2[4]	0
Bit 3	R/W	N2[3]	1
Bit 2	R/W	N2[2]	1
Bit 1	R/W	N2[1]	1
Bit 0	R/W	N2[0]	1

This register contains an 8-bit binary number, N2, which is one less than the magnitude of the output clock divisor. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL.

The default value of N2 after a device reset is 47 = 2FH.

Register 01BH, 11BH, 21BH, 31BH: TJAT Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	CENT	0
Bit 3	R/W	UNDE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	FIFORST	0
Bit 0	R/W	LIMIT	1

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions.

UNDE:

Setting the UNDE bit to logic 1 enables an underrun event to assert the INTB output low.

OVRE:

Setting the OVRE bit to logic 1 enables an overrun event to assert the INT output low.

FIFORST:

Setting the FIFORST bit allows the FIFO to reset when the PLL is reset by software. When FIFORST is logic 1, writing to the PLL Divider Control Registers N1 and N2 will cause both the PLL and FIFO to reset. When FIFORST is logic 0, writing to the Divider Control Registers N1 and N2 will cause only the PLL to reset.

LIMIT:

Setting the LIMIT bit to logic 1 will limit the PLL jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one UI of overflowing or underflowing. This limiting of jitter ensures that no data is lost during

high phase shift conditions. When LIMIT is set to logic 0, underflows and overflows may occur.

It is recommended the LIMIT be left at its logic 1 default.

Register 01CH, 11CH, 21CH, 31CH: RX-ELST Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IR	1
Bit 0	R/W	OR	1

Reserved:

This bit must be a logic 0 for correct operation.

IR:

The IR bit selects the input frame format. The IR bit must be set to logic 1 for E1 mode; it must be logic 0 for T1 mode.

OR:

The OR bit selects the output frame format. The OR bit must be set to logic 1 for E1 mode; it must be logic 0 for T1 mode.

Register 01DH, 11DH, 21DH, 31DH: RX-ELST Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	SLIPE	0
Bit 1	R	SLIPD	X
Bit 0	R	SLIPI	X

SLIPE:

The SLIPE bit position is an interrupt enable that when set, enables the INTB output to assert low when a slip occurs. When the block is reset the SLIPE bit position is cleared and interrupt generation is disabled.

SLIPD:

The SLIPD bit indicates the direction of the last slip. If the SLIPD bit is a logic 1 then the last slip was due to the frame buffer becoming full; a frame was deleted. If the SLIPD bit is a logic 0 then the last slip was due to the frame buffer becoming empty; a frame was duplicated.

SLIPI:

The SLIPI bit is set if a slip occurred since the last read of this register. The SLIPI bit is cleared upon reading this register.

Register 01EH, 11EH, 21EH, 31EH: RX-ELST Idle Code

Bit	Type	Function	Default
Bit 7	R/W	D7	1
Bit 6	R/W	D6	1
Bit 5	R/W	D5	1
Bit 4	R/W	D4	1
Bit 3	R/W	D3	1
Bit 2	R/W	D2	1
Bit 1	R/W	D1	1
Bit 0	R/W	D0	1

The contents of this register replace the timeslot data in the BRPCM serial data stream when the framer is out of frame and the TRKEN bit in the Receive Options register is a logic 1. Since the transmission of all ones timeslot data is a common requirement, this register is set to all ones on a reset condition. D7 is the first to be transmitted.

The writing of the idle code pattern is asynchronous with respect to the output data clock. One timeslot of idle code data will be corrupted if the register is written to when the framer is out of frame.

Register 020H, 120H, 220H, 320H: TX-ELST Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IR	1
Bit 0	R/W	OR	1

Reserved:

This bit must be logic 0 for correct operation.

IR:

The IR bit selects the input frame format. The IR bit must be set to logic 1 for E1 mode; it must be logic 0 for T1 mode.

OR:

The OR bit selects the output frame format. The OR bit must be set to logic 1 for E1 mode; it must be logic 0 for T1 mode.

Register 021H, 121H, 221H, 321H: TX-ELST Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	SLIPE	0
Bit 1	R	SLIPD	X
Bit 0	R	SLIPI	X

SLIPE:

The SLIPE bit position is an interrupt enable that when set, enables the INTB output to assert low when a slip occurs. When the block is reset the SLIPE bit position is cleared and interrupt generation is disabled.

SLIPD:

The SLIPD bit indicates the direction of the last slip. If the SLIPD bit is a logic 1 then the last slip was due to the frame buffer becoming full; a frame was deleted. If the SLIPD bit is a logic 0 then the last slip was due to the frame buffer becoming empty; a frame was duplicated.

SLIPI:

The SLIPI bit is set if a slip occurred since the last read of this register. The SLIPI bit is cleared upon reading this register.

Register 028H, 128H, 228H, 328H: RXCE Receive Data Link Control

Bit	Type	Function	Default
Bit 7	R/W	DL_EVEN	0
Bit 6	R/W	DL_ODD	0
Bit 5	R/W	T1_DL_EN	1
Bit 4	R/W	DL_TS[4]	0
Bit 3	R/W	DL_TS[3]	0
Bit 2	R/W	DL_TS[2]	0
Bit 1	R/W	DL_TS[1]	0
Bit 0	R/W	DL_TS[0]	0

This register, along with the RXCE Data Link Bit Select register, controls the extraction of the data link terminated by RDLC. Refer to the "Using the Internal HDLC Receivers" description in the Operation section for details on terminating HDLC frames.

DL_EVEN:

The data link even select (DL_EVEN) bit controls whether or not the first data link is extracted from the even frames of the receive data stream. If DL_EVEN is a logic 0, the data link is not extracted from the even frames. If DL_EVEN is a logic 1, the data link is extracted from the even frames. In E1 mode, the frames in an E1 CRC-4 multiframe are considered to be numbered from 0 to 15; in T1 mode, the frames in a superframe are considered to be numbered from 1 to 12 (or 1 to 24 in an extended superframe).

DL_ODD:

The data link odd select (DL_ODD) bit controls whether or not the first data link is extracted from the odd frames of the receive data stream. If DL_ODD is a logic 0, the data link is not extracted from the odd frames. If DL_ODD is a logic 1, the data link is extracted from the odd frames.

T1_DL_EN:

The T1 data link enable bit allows the termination of the ESF or T1DM data links when in T1 mode. If T1_DL_EN is a logic 1, the ESF, FMS1 and FMS0 bits of the T1-FRMR Configuration register determine the bit locations from which the data link is extracted. When the T1_DL_EN bit is a logic 1, the DL_EVEN and DL_ODD bits must both be set to logic 0. This bit must be set to logic 0 when in E1 mode.

DL_TS[4:0]:

The data link timeslot (DL_TS[4:0]) bits gives a binary representation of the timeslot/channel from which the data link is to be extracted. Note that T1 channels 1 to 24 are mapped to

values 0 to 23. The DL_TS[4:0] bits have no effect when DL_EVEN and DL_ODD are both a logic 0.

Register 029H, 129H, 229H, 329H: RXCE Receive Data Link Bit Select

Bit	Type	Function	Default
Bit 7	R/W	DL_BIT[7]	0
Bit 6	R/W	DL_BIT[6]	0
Bit 5	R/W	DL_BIT[5]	0
Bit 4	R/W	DL_BIT[4]	0
Bit 3	R/W	DL_BIT[3]	0
Bit 2	R/W	DL_BIT[2]	0
Bit 1	R/W	DL_BIT[1]	0
Bit 0	R/W	DL_BIT[0]	0

DL_BIT[7:0]:

The data link bit select (DL_BIT[7:0]) bits controls which bits of the timeslot/channel are to be extracted and passed to RDLC. If DL_BIT[x] is a logic 1, that bit is extracted as part of the data link. To extract the data link from the entire timeslot, all eight DL_BIT[x] bits must be set to a logic 1. DL_BIT[7] corresponds to the most significant bit (bit 1, the first bit received) of the timeslot and DL_BIT[0] corresponds to the least significant bit (bit 8, the last bit received) of the timeslot. The DL_BIT[7:0] bits have no effect when the DL_EVEN and DL_ODD bits of the RXCE Data Link Control register are both logic 0.

Register 030H, 130H, 230H, 330H: BRIF Configuration

Bit	Type	Function	Default
Bit 7	R/W	NX64KBIT/S[1]	0
Bit 6	R/W	NX64KBIT/S[0]	0
Bit 5	R/W	CMODE	1
Bit 4	R/W	DE	1
Bit 3	R/W	FE	1
Bit 2	R/W	CMS	0
Bit 1	R/W	RATE[1]	0
Bit 0	R/W	RATE[0]	0

NX64KBIT/S[1:0]:

The NX64KBIT/S[1:0] bits determine the mode of operation when BRCLK clock master mode is selected, as shown in the following table. Note that these bits are ignored when clock slave mode is selected.

Table 9 - Receive Backplane Nx64Kbit/s Mode Selection

NX64KBIT/S[1]	NX64KBIT/S[0]	Operation
0	0	Full Frame
0	1	Nx56Kbit/s
1	0	Nx64Kbit/s
1	1	Nx64Kbit/s with F-bit (only valid for E1 mode)

When in Full Frame mode, the entire frame (193 bits for T1 or 256 bits for E1) is presented and the BRCLK pulse train contains no gaps.

When in any of the Nx64Kbit/s modes (including the Nx56Kbit/s variant), only those timeslots with their DTRKC bit cleared (logic 0) are clocked out the backplane. BRCLK does not pulse during those timeslots with their DTRKC bit set (logic 1). The DTRKC bits are located in the RPSC Indirect Registers. When in T1 mode, the clock is always gapped during the framing bit position.

When the Nx56Kbit/s mode is selected, only the first 7 bits of the selected timeslots are presented to the backplane and the 8th bit is gapped out. When the Nx64Kbit/s mode is selected, all 8 bits of the selected timeslots are presented to the backplane.

The Nx64Kbit/s with F-bit mode is intended to support ITU recommendation G.802 where 1.544 Mbit/s data is carried within a 2.048 Mbit/s data stream. This mode is only valid when the

E1/T1B register bit is a logic 1 (E1 mode is selected). The operation is the same as the Nx64Kbit/s mode, except that the framing bit is presented during the first bit of timeslot 26. To properly extract a G.802 formatted T1, the DTRKC bits must be set to logic 0 for timeslots 1 through 15 and 17 through 26, and the DTRKC bits must be set to logic 1 for timeslots 27 through 31.

CMODE:

The clock mode (CMODE) bit determines whether the BRCLK pin is an input or output. When CMODE is a logic 0, clock master mode is selected and the BRCLK output is derived from the integral clock synthesizer. Depending on the mode of operation, BRCLK may have a burst frequency of up to 2.048 MHz and may be gapped to support sub-rate applications.

When CMODE is a logic 1, clock slave mode is selected and BRCLK is an input. A multiplexed backplane is only supported when CMODE is logic 1.

In Receive Clock Slave: H-MVIP mode, CMODE must be programmed to logic 1.

DE:

The data edge (DE) bit determines the edge of BRCLK on which BRPCM and BRSIG are generated. If DE is a logic 0, BRPCM and BRSIG are updated on the falling edge of BRCLK. If DE is a logic 1, BRPCM and BRSIG are updated on the rising edge of BRCLK.

In Receive Clock Slave: H-MVIP mode, DE must be programmed to logic 0.

FE:

The framing edge (FE) bit determines the edge of BRCLK on which the frame pulse (BRFP) pulse is sampled or updated. If FE is a logic 0, BRFP is sampled or updated on the falling edge of BRCLK. If FE is a logic 1, BRFP is sampled on the rising edge of BRCLK. In the case where FE is not equal to DE, BRFP is sampled or updated one clock edge before BRPCM and BRSIG.

In Receive Clock Slave: H-MVIP mode, FE must be programmed to logic 1.

CMS:

When in Receive Clock Slave mode, the clock mode select (CMS) bit determines the BRCLK frequency multiple. If CMS is a logic 0, BRCLK is at the backplane rate. If CMS is a logic 1, BRCLK is at twice the backplane rate.

In Receive Clock Slave: Full T1/E1 or Receive Clock Slave: Full T1/E1 with CCS H-MVIP mode, CMS must be programmed to logic 0. In Receive Clock Slave: H-MVIP mode, CMS must be programmed to logic 1. CMS has no effect when in Receive Clock Master mode.

RATE[1:0]:

The rate select (RATE[1:0]) bits determine the backplane rate according to the following table:

Table 10 - Receive Backplane Rate

RATE[1]	RATE[0]	Backplane Rate
0	0	1.544 Mbit/s
0	1	2.048 Mbit/s
1	0	Reserved
1	1	8.192 Mbit/s (H-MVIP)

When in Receive Clock Slave: H-MVIP mode and only in this mode, RATE[1:0] are to be programmed to “11”. When in a Receive Clock Slave with CCS H-MVIP mode, RATE[1:0] configure the backplane rate of BRPCM and BRSIG.

The RATE[1:0] bits can only be set once after reset.

Register 031H, 131H, 231H, 331H: BRIF Frame Pulse Configuration

Bit	Type	Function	Default
Bit 7	R/W	MAP	0
Bit 6	R/W	FPINV	0
Bit 5	R/W	FPMODE	1
Bit 4	R/W	ALTFDL	0
Bit 3	R/W	ROHM	0
Bit 2	R/W	BRXSMFP	0
Bit 1	R/W	BRXCMFP	0
Bit 0	R/W	ALTBRFP	0

MAP:

The MAP bit determines the mapping of a 2.048 MHz backplane onto a 1.544 MHz line. This bit is ignored when in E1 mode (E1/T1B register bit is logic 1), when the backplane rate is 1.544 Mbit/s (RATE[1:0] = 'b00), or when in clock master mode (CMODE = 'b0).

When MAP is a logic 0, every fourth timeslot is unused, starting with timeslot 0. The framing bit is presented during bit 0 of timeslot 0, so that only bits 1 to 7 of timeslot 0 are unused.

When MAP is a logic 1, the first 24 timeslots (0 to 23) are used. The framing bit is sampled during bit 7 of timeslot 31 and the rest of the frame (timeslots 24 to 30 and bits 0 to 6 of timeslot 31) does not contain valid data.

MAP must be programmed to logic 0 when the Receive H-MVIP interface is enabled.

FPINV:

The frame pulse inversion (FPINV) bit determines whether BRFP is inverted prior to sampling or presentation. If FPINV is a logic 0, BRFP is active high. If FPINV is a logic 1, BRFP is active low.

In Receive Clock Slave: H-MVIP mode, FPINV must be programmed to logic 0.

FPMODE:

The frame pulse mode (FPMODE) bit determines whether BRFP is an input or an output. When FPMODE is a logic 0, frame pulse master mode is selected, BRFP is an output and the ROHM, BRXSMFP, BRXCMFP and ALTBRFP bits determine what BRFP connotes.

When FPMODE is a logic 1, frame pulse slave mode is selected and BRFP is an input. When configured as an input, BRFP only has effect when the elastic store is in use

(RXELSTBYP is logic 0); otherwise, it is ignored.

In Receive Clock Slave: H-MVIP mode, FPMODE must be programmed to logic 1.

ALTFDL:

In T1 mode, the ALTFDL bit enables the framing bit position on the backplane PCM output to contain a copy of the FDL bit. When ALTFDL is set to logic 1, each M-bit value in the ESF-formatted stream is duplicated and replaces the subsequent CRC bit or F-bit in the output signal stream on BRPCM. When ALTFDL is set to logic 0, the output BRPCM stream contains the received M, CRC, or F bits in the framing bit position. Note that this function is only valid for ESF-formatted streams; ALTFDL should be set to logic 0 when other framing formats are being received.

This bit is ignored in E1 mode.

ALTBRFP:

The ALTBRFP bit suppresses every second output pulse on the backplane output BRFP. When ALTBRFP is set to logic 1 and BRXCMFP and BRXSMP bits are both logic 0, the output signal on BRFP pulses every 386 bits or 512 bits, indicating the first bit or every second frame. Under this condition, BRFP indicates the Signaling Alignment bits (S1-S6) for T1 SF, the data link bits for T1 ESF and the NFAS frames for E1. If the BRXCMFP or BRXSMFP bit is logic 1 when ALTBRFP is logic 1, the output signal on BRFP pulses every 24, 32 or 48 frames. In T1 mode, this latter setting (i.e. both ALTBRFP and BRXSMFP set to logic 1) is useful for converting SF formatted data to ESF formatted data between two COMET-Quad devices. When ALTBRFP is set to logic 0, the output signal on BRFP pulses in accordance to the ROHM, BRXCMFP and BRXSMP bit settings.

ALTBRFP has no effect if the FPMODE bit or the ROHM bit is a logic 1.

ROHM, BRXSMFP, BRXCMFP:

The ROHM, BRXSMFP and BRXCMFP bits select the output signal seen on the backplane output BRFP. These register bits only have effect if the FPMODE bit is a logic 0.

In T1 mode, only BRXSMFP has effect, the other two bits are ignored. When set to logic 1, the BRFP output pulses high during the first framing bit of the 12 frame SF or the 24 frame ESF (depending on the framing format selected in the T1-FRMR). When BRXSMFP is set to logic 0, the BRFP output pulses high during each framing bit (i.e. every 193 bits).

The following table summarizes the configurations for E1 mode:

Table 11 - E1 Receive Backplane Frame Pulse Configurations

ROHM	BRXSMFP	BRXCMFP	Result
0	0	0	Backplane receive frame pulse output: BRFP pulses high for 1 BRCLK cycle during bit 1 of each 256-bit frame, indicating the frame alignment of the BRPCM data stream.
0	0	1	Backplane receive CRC multiframe output: BRFP pulses high for 1 BRCLK cycle during bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the BRPCM data stream. (Even when CRC multiframing is disabled, the BRFP output continues to indicate the position of bit 1 of the FAS frame every 16th frame).
0	1	0	Backplane receive signaling multiframe output: BRFP pulses high for 1 BRCLK cycle during bit 1 of frame 1 of the 16 frame signaling multiframe, indicating the signaling multiframe alignment of the BRPCM data stream. (Even when signaling multiframing is disabled, the BRFP output continues to indicate the position of bit 1 of every 16th frame.)

ROHM	BRXSMFP	BRXCMFP	Result
0	1	1	Backplane receive composite multiframe output: BRFP goes high on the active BRCLK edge marking the beginning of bit 1 of frame 1 of every 16 frame signaling multiframe, indicating the signaling multiframe alignment of the BRPCM data stream, and returns low on the active BRCLK edge marking the end of bit 1 of frame 1 of every 16 frame CRC multiframe, indicating the CRC multiframe alignment of the BRPCM data stream. This mode allows both multiframe alignments to be decoded externally from the single BRFP signal. Note that if the signaling and CRC multiframe alignments are coincident, BRFP will pulse high for 1 BRCLK cycle every 16 frames.
1	X	X	Backplane receive overhead output: BRFP is high for timeslot 0 and timeslot 16 of each 256-bit frame, indicating the overhead of the BRPCM data stream.

Register 032H, 132H, 232H, 332H : BRIF Parity/F-bit Configuration

Bit	Type	Function	Default
Bit 7	R/W	RPTYP	0
Bit 6	R/W	RPTYE	0
Bit 5	R/W	FIXF	0
Bit 4	R/W	FIXPOL	0
Bit 3	R/W	PTY_EXTD	0
Bit 2		Unused	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	TRI	0

This register provides control of data integrity checking on the BRPCM and BRSIG signals of the receive backplane interface in T1 and E1 mode. A single parity bit in the first bit position of the frame (the F-bit if in T1 mode) represents parity over the previous frame (including the undefined bit positions). If a 2.048 Mbit/s backplane rate is selected, the parity calculation is performed over all bit positions, including the undefined positions. Signaling parity is similarly calculated over all bit positions. Parity checking and generation is not supported when the Nx64Kbit/s mode or when mapping a 1.544 Mbit/s signal onto a higher rate backplane in the format where the first 24 timeslots are used, i.e., the RATE[1:0] bits in the BRIF Configuration register are not set to “00” and the MAP bit in the BRIF Frame Pulse Configuration register is logic 1.

RPTYP:

The receive parity type (RPTYP) bit sets even or odd parity in the receive streams. If RPTYP is a logic 0, the expected parity value in the first bit position of the frame (the F-bit if in T1 mode) of BRPCM and BRSIG is even, thus it is a one if the number of ones in the previous frame is odd. If RPTYP is a logic 1, the expected parity value in the first bit position of the frame if BRPCM and BRSIG is odd, thus it is a one if the number of ones in the previous frame is even. RPTYP only has effect if RPRTYE is a logic one.

RPRTYE:

The RPRTYE bit enables receive parity insertion. When set a logic one, parity is inserted into the first bit position of the frame of the BRPCM and BRSIG streams. When set to logic zero, the first bit position of the frame passes through transparently.

FIXF:

If the RPRTYE bit is a logic 0, a logic 1 in the FIXF bit forces the first bit of the BRPCM frame to the polarity specified by the FIXPOL bit.

If RPRTYE is a logic 1, FIXF has no effect. If RPRTYE and FIXF are both logic 0, the first bit of the frame passes from the line transparently.

FIXPOL:

This bit determines the logic level of the first bit of the BRPCM frame when the FIXF bit is a logic 1 and the RPRTYE bit is a logic 0. If FIXPOL is a logic 1, BRPCM will be high in the first bit of the frame. If FIXPOL is a logic 0, BRPCM will be low in the first bit of the frame.

PTY_EXTD:

The parity extend (PRY_EXTD) bit causes the parity to be calculated over the previous frame plus the previous parity bit, instead of only the previous frame.

Reserved

This bit must be logic 0 for correct operation.

TRI:

This bit must be programmed to logic 1 when the Receive H-MVIP interface is active. This bit can be either a 1 or a 0 in other modes.

Register 033H, 133H, 233H, 333H: BRIF Timeslot Offset

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	TSOFF[6]	0
Bit 5	R/W	TSOFF[5]	0
Bit 4	R/W	TSOFF[4]	0
Bit 3	R/W	TSOFF[3]	0
Bit 2	R/W	TSOFF[2]	0
Bit 1	R/W	TSOFF[1]	0
Bit 0	R/W	TSOFF[0]	0

TSOFF[6:0]:

The timeslot offset (TSOFF[6:0]) bits give a binary representation of the fixed byte offset between the backplane receive frame pulse (BRFP) and the start of the next frame on the backplane receive data signal (BRPCM). The seven bits can give an offset from 0 - 127 bytes.

When in Receive Clock Slave: Full T1/E1 with CCS H-MVIP mode, TSOFF[6:0] must all be programmed to logic 0.

When in Receive Clock Slave: H-MVIP mode, the TSOFF[6:0] bits must be programmed as follows:
Quadrant 1 (Register 033H): TSOFF[6:0] = “0000000”.
Quadrant 2 (Register 133H): TSOFF[6:0] = “0000001”.
Quadrant 3 (Register 233H): TSOFF[6:0] = “0000010”.
Quadrant 4 (Register 333H): TSOFF[6:0] = “0000011”.

Register 034H, 134H, 234H, 334H: BRIF Bit Offset

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	BOFF_EN	0
Bit 2	R/W	BOFF[2]	0
Bit 1	R/W	BOFF[1]	0
Bit 0	R/W	BOFF[0]	0

BOFF_EN:

The bit offset enable (BOFF_EN) bit is used to enable the bit offset bits. If BOFF_EN is a logic 0, the bit offset is disabled and there is no bit offset between the frame pulse and the first bit of the first timeslot. In this case, the BOFF[2:0] bits are ignored. If BOFF_EN is a logic 1, the bit offset is enabled and the BOFF[2:0] bits operate as described below.

When the Receive H-MVIP interface is active, BOFF_EN must be programmed to logic 0.

BOFF[2:0]:

The bit offset (BOFF[2:0]) bits gives a binary representation of the fixed offset between the backplane receive frame pulse (BRFP) and the start of the first bit of the first timeslot. This binary representation is then used to determine the BRCLK edge, defined as CET (clock edge transmit) on which the first bit of the first timeslot is sampled. For example, if CET is 4, the data on BRPCM and BRSIG is sampled on the fourth clock edge after BRFP is sampled (see Figure 24). The following tables show the relationship between BOFF[2:0], FE, DE and CER.

Table 12 - Receive Backplane Bit Offset for CMS = 0

FE	DE	BOFF[2:0]								
		000	001	010	011	100	101	110	111	
0	0	4	6	8	10	12	14	16	18	
0	1	3	5	7	9	11	13	15	17	CET
1	0	3	5	7	9	11	13	15	17	
1	1	4	6	8	10	12	14	16	18	

Table 13 - Receive Backplane Bit Offset for CMS = 1

FE	DE	BOFF[2:0]								
		000	001	010	011	100	101	110	111	
0	0	4	8	12	16	20	24	28	32	
0	1	3	7	11	15	19	23	27	31	CET
1	0	3	7	11	15	19	23	27	31	
1	1	4	8	12	16	20	24	28	32	

The above tables are consistent with the convention established by the Concentration Highway Interface (CHI) specification.

Note that in the case where FE is logic 0, DE is logic 1 and BRFP is configured for a superframe/multiframe mode, the maximum offset is one frame less two bits, rather than one frame less one bit as in all other configurations. In this configuration, the maximum offset is 191 bits at 1.544 Mbit/s and 254 bits at 2.048 Mbit/s.

Register 038H, 138H, 238H, 338H: TXCI Transmit Data Link Control

Bit	Type	Function	Default
Bit 7	R/W	DL_EVEN	0
Bit 6	R/W	DL_ODD	0
Bit 5	R/W	T1_DL_EN	1
Bit 4	R/W	DL_TS[4]	0
Bit 3	R/W	DL_TS[3]	0
Bit 2	R/W	DL_TS[2]	0
Bit 1	R/W	DL_TS[1]	0
Bit 0	R/W	DL_TS[0]	0

This register, along with the TXCI Data Link Bit Select register, controls the insertion of the data link generated by TDPR. Refer to the "Using the Internal HDLC Transmitters" description in the Operation section for details on terminating HDLC frames.

DL_EVEN:

The data link even select (DL_EVEN) bit controls whether or not the first data link is inserted into the even frames of the receive data stream. If DL_EVEN is a logic 0, the data link is not inserted into the even frames. If DL_EVEN is a logic 1, the data link is inserted into the even frames. In E1 mode, the frames in an E1 CRC-4 multiframe are considered to be numbered from 0 to 15; in T1 mode, the frames in a superframe are considered to be numbered from 1 to 12 (or 1 to 24 in an extended superframe).

DL_ODD:

The data link odd select (DL_ODD) bit controls whether or not the first data link is inserted into the odd frames of the receive data stream. If DL_ODD is a logic 0, the data link is not inserted into the odd frames. If DL_ODD is a logic 1, the data link is inserted into the odd frames.

T1_DL_EN:

The T1 data link enable bit allows the generation of the ESF or T1DM data links when in T1 mode. If T1_DL_EN is a logic 1, the ESF, FMS1 and FMS0 bits of the T1-FRMR Configuration register determine the bit locations into which the data link is inserted. When the T1_DL_EN bit is a logic 1, the DL_EVEN and DL_ODD bits must both be set to logic 0. This bit must be set to logic 0 when in E1 mode.

DL_TS[4:0]:

The data link timeslot (DL_TS[4:0]) bits gives a binary representation of the timeslot/channel into which the data link is to be inserted. Note that T1 channels 1 to 24 are mapped to values 0 to 23. The DL_TS[4:0] bits have no effect when DL_EVEN and DL_ODD are both a logic 0.

Register 039H, 139H, 239H, 339H: TXCI Transmit Data Link Bit Select

Bit	Type	Function	Default
Bit 7	R/W	DL_BIT[7]	0
Bit 6	R/W	DL_BIT[6]	0
Bit 5	R/W	DL_BIT[5]	0
Bit 4	R/W	DL_BIT[4]	0
Bit 3	R/W	DL_BIT[3]	0
Bit 2	R/W	DL_BIT[2]	0
Bit 1	R/W	DL_BIT[1]	0
Bit 0	R/W	DL_BIT[0]	0

DL_BIT[7:0]:

The data link bit select (DL_BIT[7:0]) bits controls into which bits of the timeslot/channel data from TDPR are to be inserted. If DL_BIT[x] is a logic 1, the data link is inserted into that bit. To insert the data link into the entire timeslot, all eight DL_BIT[x] bits must be set to a logic 1. DL_BIT[7] corresponds to the most significant bit (bit 1, the first bit transmitted) of the timeslot and DL_BIT[0] corresponds to the least significant bit (bit 8, the last bit transmitted) of the timeslot. The DL_BIT[7:0] bits have no effect when the DL_EVEN and DL_ODD bits of the TXCI Data Link Control register are both logic 0.

Register 040H, 140H, 240H, 340H: BTIF Configuration

Bit	Type	Function	Default
Bit 7	R/W	NX64KBIT/S[1]	0
Bit 6	R/W	NX64KBIT/S[0]	0
Bit 5	R/W	CMODE	1
Bit 4	R/W	DE	1
Bit 3	R/W	FE	1
Bit 2	R/W	CMS	0
Bit 1	R/W	RATE[1]	0
Bit 0	R/W	RATE[0]	0

NX64KBIT/S[1:0]:

The NX64KBIT/S[1:0] bits determine the mode of operation when BTCLK clock master mode is selected (CMODE logic 0), as shown in the following table. Note that these bits are ignored when clock slave mode is selected (CMODE logic 1).

Table 14 - Transmit Backplane Nx64Kbit/s Mode Selection

NX64KBIT/S[1]	NX64KBIT/S[0]	Operation
0	0	Full Frame
0	1	Nx56Kbit/s
1	0	Nx64Kbit/s
1	1	Nx64Kbit/s with F-bit (only valid for E1 mode)

When in Full Frame mode, the entire frame (193 bits for T1 or 256 bits for E1) is sampled from the backplane.

When in any of the Nx64Kbit/s modes (including the Nx56Kbit/s variant), only those timeslots with their IDLE_CHAN bit cleared (logic 0) are sampled from the backplane. The other timeslots, with their IDLE_CHAN bit set (logic 1), do not contain valid data and will be overwritten with the per-DS0 idle code. The IDLE_CHAN bits are located in the TPSC Indirect registers. When in T1 mode, the clock is always gapped during the framing bit position.

When the Nx56Kbit/s mode is selected, only the first 7 bits of the selected timeslots are sampled from the backplane and the 8th bit is gapped out. When the Nx64Kbit/s mode is selected, all 8 bits of the selected timeslots are sampled from the backplane.

The Nx64Kbit/s with F-bit mode is intended to support ITU recommendation G.802. This mode is only valid when the E1/T1B register bit is a logic 1 (E1 mode is selected). The operation is the same as the Nx64Kbit/s mode, except that the framing bit is sampled. The F-bit is always sampled during the first bit of timeslot 26. The remaining seven bits of timeslot 26 are not sampled. To properly insert a G.802 formatted T1, the IDLE_CHAN bits must be set to logic 0 for timeslots 1 through 15 and 17 through 26, and the IDLE_CHAN bits must be set to logic 1 for timeslots 27 through 31.

CMODE:

The clock mode (CMODE) bit determines whether the BTCLK pin is an input or output. When CMODE is a logic 0, clock master mode is selected and the BTCLK output is derived from the integral clock synthesizer. Depending on the mode of operation, BTCLK may have a burst frequency of up to 2.048 MHz and may be gapped to support sub-rate applications.

When CMODE is a logic 1, clock slave mode is selected and BTCLK is an input.

In Transmit Clock Slave: H-MVIP mode, CMODE must be programmed to logic 1.

DE:

The data edge (DE) bit determines the edge of BTCLK on which BTPCM and BTSIG are sampled. If DE is a logic 0, BTPCM and BTSIG are sampled on the falling edge of BTCLK. If DE is a logic 1, BTPCM and BTSIG are sampled on the rising edge of BTCLK.

In Transmit Clock Slave: H-MVIP mode, DE must be programmed to logic 1.

FE:

The framing edge (FE) bit determines the edge of BTCLK on which the frame pulse (BTFP) pulse is sampled or updated. If FE is a logic 0, BTFP is sampled or updated on the falling edge of BTCLK. If FE is a logic 1, BTFP is sampled or updated on the rising edge of BTCLK. In the case where FE is not equal to DE, BTFP is sampled or updated one clock edge before BTPCM and BTSIG.

In Transmit Clock Slave: H-MVIP mode, FE must be programmed to logic 1.

CMS:

The clock mode select (CMS) bit determines the BTCLK frequency multiple. If CMS is a logic 0, BTCLK is at the backplane rate. If CMS is a logic 1, BTCLK is at twice the backplane rate.

In Transmit Clock Slave: H-MVIP mode, CMS must be programmed to logic 1.

RATE[1:0]:

The rate select (RATE[1:0]) bits determine the backplane rate according to the following table:

Table 15 - Transmit Backplane Rate

RATE[1]	RATE[0]	Backplane Rate
0	0	1.544 Mbit/s
0	1	2.048 Mbit/s
1	0	Reserved
1	1	8.192 Mbit/s (H-MVIP)

When in Transmit Clock Slave: H-MVIP mode and only in this mode, RATE[1:0] are to be programmed to “11”. When in a Transmit Clock Slave with CCS H-MVIP mode, RATE[1:0] configure the backplane rate of BTPCM and BTSIG.

The RATE[1:0] bits can only be set once after reset.

Register 041H, 141H, 241H, 341H: BTIF Frame Pulse Configuration

Bit	Type	Function	Default
Bit 7	R/W	MAP	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	FPINV	0
Bit 2	R/W	ESF_EN	0
Bit 1	R/W	FPTYP	0
Bit 0	R/W	FPMODE	1

MAP:

The MAP bit determines the mapping of a 2.048 MHz backplane onto a 1.544 MHz line. This bit is ignored when in E1 mode (E1/T1B register bit is logic 1), when the backplane rate is 1.544 Mbit/s (RATE[1:0] = 'b00), or when in clock master mode (CMODE = 'b0).

When MAP is a logic 0, every fourth timeslot is unused, starting with timeslot 0. The framing bit is sampled during bit 0 of timeslot 0, so that only bits 1 to 7 of timeslot 0 are ignored.

When MAP is a logic 1, the first 24 timeslots (0 to 23) are sampled. The framing bit is sampled during bit 7 of timeslot 31 and the rest of the frame (timeslots 24 to 30 and bits 0 to 6 of timeslot 31) are ignored.

MAP must be programmed to logic 0 when the Transmit H-MVIP interface is enabled.

FPINV:

The frame pulse inversion (FPINV) bit determines whether BTFP is inverted prior to sampling. If FPINV is a logic 0, BTFP is active high. If FPINV is a logic 1, BTFP is active low. Frame pulse inversion cannot be used when BTFP is configured as an output (FPMODE is a logic 0).

In Transmit Clock Slave: H-MVIP mode, FPINV must be programmed to logic 0.

ESF_EN:

The extended superframe enable (ESF_EN) bit determines which superframe alignment is used when in T1 mode and FPTYP is a logic 1. When ESF_EN is a logic 0, superframe alignment is chosen and BTFP pulses (FPMODE logic 0) or is expected (FPMODE logic 1) every 12 frames on the first frame bit of the superframe. When ESF_EN is a logic 1,

extended superframe alignment is chosen and pulses (FPMODE logic 0) or is expected (FPMODE logic 1) every 24 frames on the first frame bit of the extended superframe.

This bit is ignored when in E1 mode or in T1 mode when FPTYP is a logic 0.

FPTYP:

The frame pulse type (FPTYP) bit determines the type of frame pulse on BTFP. When FPTYP is a logic 0, basic frame alignment is chosen and frame pulses occur every frame. When FPTYP is a logic 1, multiframe alignment is chosen.

In T1 mode, with multiframe alignment pulses (FPMODE logic 0) or is expected (FRMODE logic 1) every 12 or 24 frames as determined by the ESF_EN bit. In E1 mode with multiframe alignment when FPMODE is a logic 0, BTFP is expected to transition high at the beginning of the first bit of the first frame of a 16 frame signaling multiframe and transitions low to at the end of the first bit of the first frame of every 16 frame CRC multiframe.

In E1 mode, with multiframe alignment when FPMODE is a logic 0, as an output BTFP pulses once every 16 frames to indicate both CRC and signaling multiframe alignment. When BTFP is configured as an input, it must be brought high to mark bit 1 of frame 1 of every 16 frame signaling multiframe and brought low following bit 1 of frame 1 of every 16 frame CRC multiframe.

To properly initialize the transmit HDLC controllers in basic frame alignment mode (FPTYP is logic 0), multiframe alignment (FPTYP is logic 1) must be configured for at least one frame (i.e., for at least one frame period in frame pulse master mode or for at least one input frame pulse in frame pulse slave mode). After this initialization, the FPTYP can be set to any desired value.

When operating at T1 in 2.048 MHz backplane mode, the framing pattern can be corrupted when FPTYP = 1. In order to avoid corruption, toggle FPTYP high then low and keep it held low. The transmitter will maintain the multiframe alignment provided on BTFP. If BTFP loses multiframe alignment, FPTYP will have to be toggled again.

In Transmit Clock Slave: H-MVIP mode, FPTYP must be programmed to logic 0.

FPMODE:

The frame pulse mode (FPMODE) bit determines whether BTFP is an input or an output. When FPMODE is a logic 0, frame pulse master mode is selected and BTFP is an output. When FPMODE is a logic 1, frame pulse slave mode is selected and BTFP is an input. Frame pulse master mode cannot be used with transmit backplane clock rates greater than 2.048 MHz.

In Transmit Clock Slave: H-MVIP mode, FPMODE must be programmed to logic 1.

Register 042H, 142H, 242H, 342H: BTIF Parity Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	TPTYP	0
Bit 6	R/W	TPTYE	0
Bit 5	R	BTPCMI	X
Bit 4	R	BTSIGI	X
Bit 3	R/W	PTY_EXTD	0
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

This register provides control and status reporting of data integrity checking on the BTPCM and BTSIG signals of the transmit backplane interface in T1 and E1 mode. A single parity bit in the first bit position of the frame (the F-bit if in T1 mode) represents parity over the previous frame (including the undefined bit positions). Parity checking and generation is not supported when the Nx64Kbit/s mode is active. Parity checking and generation is not supported when mapping a 1.544 Mbit/s signal onto a higher rate backplane in the format where the first 24 timeslots are used, i.e., the RATE[1:0] bits in the BTIF Configuration register are not set to “00” and the MAP bit in the BTIF Frame Pulse Configuration register is logic 1.

TPTYP:

The transmit parity type (TPTYP) bit sets even or odd parity in the transmit streams. If TPTYP is a logic 0, the expected parity value in the first bit position of the frame of BTPCM and BTSIG is even, thus it is a one if the number of ones in the previous frame is odd. If TPTYP is a logic 1, the expected parity value in the first bit position of the frame of BTPCM and BTSIG is odd, thus it is a one if the number of ones in the previous frame is even.

TPTYE:

The transmit parity enable (TPTYE) bit enables transmit parity interrupts. When TPTYE is a logic 1, parity errors on the inputs BTPCM and BTSIG are indicated by the BTPCMI and BTSIGI bits, respectively, and by the assertion low of the INTB output. When TPTYE is a logic 0, parity errors are indicated by the BTPCMI and BTSIGI bits but are not indicated on the INTB output.

BTPCMI:

The transmit PCM data interrupt (BTPCMI) bit indicates if a parity error has been detected on the BTPCM input. This bit is cleared when this register is read.

BTSIGI:

The transmit signaling interrupt (BTSIGI) bit indicated if a parity error has been detected on the BTSIG input. This bit is cleared when this register is read.

PTY_EXTD:

The parity extend (PRY_EXTD) bit causes the parity to be calculated over the previous frame plus the previous parity bit, instead of only the previous frame.

Register 043H, 143H, 243H, 343H: BTIF Timeslot Offset

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	TSOFF[6]	0
Bit 5	R/W	TSOFF[5]	0
Bit 4	R/W	TSOFF[4]	0
Bit 3	R/W	TSOFF[3]	0
Bit 2	R/W	TSOFF[2]	0
Bit 1	R/W	TSOFF[1]	0
Bit 0	R/W	TSOFF[0]	0

TSOFF[6:0]:

The timeslot offset (TSOFF[6:0]) bits give a binary representation of the fixed byte offset between the backplane transmit frame pulse (BTFP) and the start of the next frame on the backplane transmit data signal (BTPCM). The seven bits can give an offset from 0 - 127 bytes.

When in Transmit Clock Slave: Full T1/E1 with CCS H-MVIP mode, TSOFF[6:0] must all be programmed to logic 0.

When in Transmit Clock Slave: H-MVIP mode, the TSOFF[6:0] bits must be programmed as follows:
Quadrant 1 (Register 043H): TSOFF[6:0] = “0000000”.
Quadrant 2 (Register 143H): TSOFF[6:0] = “0000001”.
Quadrant 3 (Register 243H): TSOFF[6:0] = “0000010”.
Quadrant 4 (Register 343H): TSOFF[6:0] = “0000011”.

Register 044H, 144H, 244H, 344H: BTIF Bit Offset

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	BOFF_EN	0
Bit 2	R/W	BOFF[2]	0
Bit 1	R/W	BOFF[1]	0
Bit 0	R/W	BOFF[0]	0

BOFF_EN:

The bit offset enable (BOFF_EN) bit is used to enable the bit offset bits. If BOFF_EN is a logic 0, the bit offset is disabled and there is no bit offset between the frame pulse and the first bit of the first timeslot. In this case, the BOFF[2:0] bits are ignored. If BOFF_EN is a logic 1, the bit offset is enabled and the BOFF[2:0] bits operate as described below.

When the Transmit H-MVIP interface is active, BOFF_EN must be programmed to logic 0.

BOFF[2:0]:

The bit offset (BOFF[2:0]) bits gives a binary representation of the fixed offset between the backplane transmit frame pulse (BTFP) and the start of the first bit of the first timeslot. This binary representation is then used to determine the BTCLK edge, defined as CER (clock edge receive) on which the first bit of the first timeslot is sampled. For example, if CER is 4, the data on BTPCM and BTSIG is sampled on the fourth clock edge after BTFP is sampled (see Figure 24). The following tables show the relationship between BOFF[2:0], FE, DE and CER.

Table 16 - Transmit Backplane Bit Offset for CMS = 0

FE	DE	BOFF[2:0]								
		000	001	010	011	100	101	110	111	
0	0	4	6	8	10	12	14	16	18	
0	1	3	5	7	9	11	13	15	17	CER
1	0	3	5	7	9	11	13	15	17	
1	1	4	6	8	10	12	14	16	18	

Table 17 - Transmit Backplane Bit Offset for CMS = 1

FE	DE	BOFF[2:0]								
		000	001	010	011	100	101	110	111	
0	0	6	10	14	18	22	26	30	34	
0	1	7	11	15	19	23	27	31	35	CER
1	0	7	11	15	19	23	27	31	35	
1	1	6	10	14	18	22	26	30	34	

The above tables are consistent with the convention established by the Concentration Highway Interface (CHI) specification.

Register 048H, 148H, 248H, 348H: T1-FRMR Configuration

Bit	Type	Function	Default
Bit 7	R/W	M2O[1]	0
Bit 6	R/W	M2O[0]	0
Bit 5	R/W	ESFFA	0
Bit 4	R/W	ESF	0
Bit 3	R/W	FMS1	0
Bit 2	R/W	FMS0	0
Bit 1	R/W	JPN	0
Bit 0		Unused	X

When the E1/T1B bit of the Global Configuration register is a logic 1 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register selects the framing format and the frame loss criteria used by the T1-FRMR.

M2O[1:0]:

The M2O[1:0] bits select the ratio of errored to total framing bits before declaring out of frame in SF, SLC®96, and ESF framing formats. A logic 00 selects 2 of 4 framing bits in error; a logic 01 selects 2 of 5 bits in error; a logic 10 selects 2 of 6 bits in error. In T1DM framing format, the ratio of errored to total framing bits before declaring out of frame is always 4 out of 12. A logic 11 in the M2O[1:0] bits is reserved and should not be used.

ESFFA:

The ESFFA bit selects one of two framing algorithms for ESF frame search in the presence of mimic framing patterns in the incoming data. A logic 0 selects the ESF algorithm where the FRMR does not declare in-frame while more than one framing bit candidate is following the framing pattern in the incoming data. A logic 1 selects the ESF algorithm where a CRC-6 calculation is performed on each framing bit candidate, and is compared against the CRC bits associated with the framing bit candidate to determine the most likely framing bit position.

ESF:

The ESF bit selects either extended superframe format or enables the Frame Mode Select bits to select either standard superframe, T1DM, or SLC®96 framing formats. A logic 1 in the ESF bit position selects ESF; a logic 0 bit enables FMS1 and FMS0 to select SF, T1DM, or SLC®96.

FMS1,FMS0:

The FMS1 and FMS0 bits select standard superframe, T1DM, or SLC®96 framing formats. A logic 00 in these bits enable the SF framing format; a logic 01 or 11 in these bit positions enable the T1DM framing format; a logic 10 in these bit positions enable the SLC®96 framing format. When ESF is selected (ESF bit set to logic 1), the FMS1 and FMS0 bits select the data rate and the source channel for the facility data link data. A logic 00 in these bits enable the FRMR to receive FDL data at the full 4 kHz rate from every odd frame. When ESF is selected, FMS1 and FMS0 settings other than logic 00 are reserved and should not be used.

The valid combinations of the ESF, FMS1, and FMS0 bits are summarized in the table below:

Table 18 - T1 Framing Modes

ESF	FMS1	FMS0	Mode
0	0	0	Select SF framing format
0	0	1	Select T1DM framing format
0	1	0	Select SLC96 framing format
0	1	1	Select T1DM framing format
1	0	0	Select ESF framing format & 4 kHz FDL Data Rate
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

JPN:

The JPN bit enables Japanese variations of the standard framing formats. If the JPN bit is a logic 1 and the ESF format is selected (ESF bit is logic 1), the T1-FRMR complies to TTC JT-G704. If the JPN bit is a logic 1 and a non-ESF format is selected (ESF bit is logic 0), it is assumed the 12^{th} F-bit of the superframe carries a far end receive failure alarm. The alarm is extracted and the framing is modified to be robust when the alarm is active.

Register 049H, 149H, 249H, 349H: T1-FRMR Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	Reserved	0
Bit 5	R/W	COFAE	0
Bit 4	R/W	FERE	0
Bit 3	R/W	BEEE	0
Bit 2	R/W	SFEE	0
Bit 1	R/W	MFPE	0
Bit 0	R/W	INFRE	0

When the E1/T1B bit of the Global Configuration register is a logic 1 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register selects which of the MFP, COFA, FER, BEE, SFE or INFR events generates an interrupt on the microprocessor INTB pin when their state changes or their event condition is detected.

Reserved:

The Reserved bit is used for production test purposes only. The Reserved bit must be logic 0 for normal operation.

COFAE:

The COFAE bit enables the generation of an interrupt when the frame find circuitry determines that frame alignment has been achieved and that the new alignment differs from the previous alignment. When COFAE is set to logic 1, the declaration of a change of frame alignment is allowed to generate an interrupt. When COFAE is set to logic 0, a change in the frame alignment does not generate an interrupt on the INTB pin.

FERE:

The FERE bit enables the generation of an interrupt when a framing bit error has been detected. When FERE is set to logic 1, the detection of a framing bit error is allowed to generate an interrupt. When FERE is set to logic 0, any error in the framing bits does not generate an interrupt on the INTB pin.

BEEE:

The BEEE bit enables the generation of an interrupt when a bit error event has been detected. A bit error event is defined as framing bit errors for SF formatted data, CRC-6 mismatch errors for ESF formatted data, Ft bit errors for SLC®96 formatted data, and either

framing bit errors or sync word errors for T1DM formatted data. When BEEE is set to logic 1, the detection of a bit error event is allowed to generate an interrupt. When BEEE is set to logic 0, bit error events are disabled from generating an interrupt on the INTB pin.

SFEE:

The SFEE bit enables the generation of an interrupt when a severely errored framing event has been detected. A severely errored framing event is defined as 2 or more framing bit errors during the current superframe for SF, ESF, or SLC®96 formatted data, and 2 or more framing bit errors or sync word errors during the current superframe for T1DM formatted data. When SFEE is set to logic 1, the detection of a severely errored framing event is allowed to generate an interrupt. When SFEE is set to logic 0, severely errored framing events are disabled from generating an interrupt on the INTB pin.

MFPE:

The MFPE bit enables the generation of an interrupt when the frame find circuitry detects the presence of framing bit mimics. The occurrence of a mimic is defined as more than one framing bit candidate following the frame alignment pattern. When MFPE is set to logic 1, the assertion or deassertion of the detection of a mimic is allowed to generate an interrupt. When MFPE is set to logic 0, the detection of a mimic framing pattern is disabled from generating an interrupt on the INTB pin.

INFRE:

The INFRE bit enables the generation of an interrupt when the frame find circuitry determines that frame alignment has been achieved and that the framer is now "in-frame". When INFRE is set to logic 1, the assertion or deassertion of the "in-frame" state is allowed to generate an interrupt. When INFRE is set to logic 0, a change in the "in-frame" state is disabled from generating an interrupt on the INTB pin.

Upon reset of the COMET-QUAD, these bits are set to logic 0, disabling the generation of interrupts on the INTB pin.

Register 04AH, 14AH, 24AH, 34AH: T1-FRMR Interrupt Status

Bit	Type	Function	Default
Bit 7	R	COFAI	X
Bit 6	R	FERI	X
Bit 5	R	BEEI	X
Bit 4	R	SFEI	X
Bit 3	R	MFPI	X
Bit 2	R	INFRI	X
Bit 1	R	MFP	X
Bit 0	R	INFR	X

When the E1/T1B bit of the Global Configuration register is a logic 1 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register indicate whether a change of frame alignment, a framing bit error, a bit error event, or a severely errored framing event generated an interrupt. This register also indicates whether a mimic framing pattern was detected or whether there was a change in the "in-frame" state of the frame circuitry.

COFAI, FERI, BEEI, SFEI:

A logic 1 in the status bit positions COFAI, FERI, BEEI and SFEI indicate that the occurrence of the corresponding event generated an interrupt; a logic 0 in the status bit positions COFAI, FERI, BEEI, and SFEI indicate that the corresponding event did not generate an interrupt.

MFPI:

A logic 1 in the MFPI status bit position indicates that the assertion or deassertion of the mimic detection indication has generated an interrupt; a logic 0 in the MFPI bit position indicates that no change in the state of the mimic detection indication occurred.

INFRI:

A logic 1 in the INFRI status bit position indicates that a change in the "in-frame" state of the frame alignment circuitry generated an interrupt; a logic 0 in the INFRI status bit position indicates that no state change occurred.

MFP, INFR:

The bit position MFP and INFR indicate the current state of the mimic detection and of the frame alignment circuitry.

The interrupt and the status bit positions (COFAI, FERI, BEEI, SFEI, MFPI, and INFRI) are cleared to logic 0 when this register is read.

Register 04CH, 14CH, 24CH, 34CH: IBCD Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	DSEL1	0
Bit 2	R/W	DSEL0	0
Bit 1	R/W	ASEL1	0
Bit 0	R/W	ASEL0	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register provides the selection of the Activate and De-activate loopback code lengths (from 3 bits to 8 bits) as follows:

Table 19 - Loopback Code Configurations

DEACTIVATE Code		ACTIVATE Code		
DSEL1	**DSEL0**	**ASEL1**	**ASEL0**	**CODE LENGTH**
0	0	0	0	5 bits
0	1	0	1	6 (or 3*) bits
1	0	1	0	7 bits
1	1	1	1	8 (or 4*) bits

Note:

3-bit and 4-bit code sequences can be accommodated by configuring the IBCD for 6 or 8 bits and by programming two repetitions of the code sequence.

The Reserved bit is used for production test purposes only. The Reserved bit must be logic 0 for normal operation.

Register 04DH, 14DH, 24DH, 34DH: IBCD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R	LBACP	X
Bit 6	R	LBDCP	X
Bit 5	R/W	LBAE	0
Bit 4	R/W	LBDE	0
Bit 3	R	LBAI	X
Bit 2	R	LBDI	X
Bit 1	R	LBA	X
Bit 0	R	LBD	X

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

LBACP, LBDCP:

The LBACP and LBDCP bits indicate when the corresponding loopback code is present during a 39.8 ms interval.

LBAE:

The LBAE bit enables the assertion or deassertion of the inband Loopback Activate (LBA) detect indication to generate an interrupt on the microprocessor INTB pin. When LBAE is set to logic 1, any change in the state of the LBA detect indication generates an interrupt. When LBAE is set to logic 0, no interrupt is generated by changes in the LBA detect state.

LBDE:

The LBDE bit enables the assertion or deassertion of the inband Loopback Deactivate (LBD) detect indication to generate an interrupt on the microprocessor INTB pin. When LBDE is set to logic 1, any change in the state of the LBD detect indication generates an interrupt. When LBDE is set to logic 0, no interrupt is generated by changes in the LBD detect state.

LBAI, LBDI:

The LBAI and LBDI bits indicate which of the two expected loopback codes generated the interrupt when their state changed. A logic 1 in these bit positions indicate that a state change in that code has generated an interrupt; a logic 0 in these bit positions indicate that no state change has occurred.

LBA, LBD:

The LBA and LBD bits indicate the current state of the corresponding loopback code detect indication. A logic 1 in these bit positions indicate the presence of that code has been detected; a logic 0 in these bit positions indicate the absence of that code.

Register 04EH, 14EH, 24EH, 34EH: IBCD Activate Code

Bit	Type	Function	Default
Bit 7	R/W	ACT7	0
Bit 6	R/W	ACT6	0
Bit 5	R/W	ACT5	0
Bit 4	R/W	ACT4	0
Bit 3	R/W	ACT3	0
Bit 2	R/W	ACT2	0
Bit 1	R/W	ACT1	0
Bit 0	R/W	ACT0	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This 8-bit register selects the Activate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8-bit register. For example, if code sequence is a repeating 00001, the first 8 bits of two repetitions (0000100001) is programmed into the register, i.e.00001000. Note that bit ACT7 corresponds to the first code bit received.

Register 04FH, 14FH, 24FH, 34FH: IBCD Deactivate Code

Bit	Type	Function	Default
Bit 7	R/W	DACT7	0
Bit 6	R/W	DACT6	0
Bit 5	R/W	DACT5	0
Bit 4	R/W	DACT4	0
Bit 3	R/W	DACT3	0
Bit 2	R/W	DACT2	0
Bit 1	R/W	DACT1	0
Bit 0	R/W	DACT0	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This 8-bit register selects the Deactivate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8-bit register. For example, if code sequence is a repeating 001, the first 8 bits of three repetitions (001001001) is programmed into the register, i.e.00100100. Note that bit DACT7 corresponds to the first code bit received.

Register 050H, 150H, 250H, 350H: SIGX Configuration Register (COSS = 0)

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6	R/W	COSS	0
Bit 5	R/W	SIGE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	ESF	0
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

Reserved:

These bits must be a logic 0 for correct operation.

COSS:

The COSS bit allows the channels to be polled to determine in which channel(s) the signaling state has changed. When COSS is a logic 1, the SIGX register space is configured to allow the change of signaling state event bits to be read. When COSS is a logic 0, the SIGX register space is configured to allow indirect access to the configuration and signaling data for each of the 24 T1 or 30 E1 channels.

SIGE:

The SIGE bit enables a change of signaling state in any one of the 24 channels (T1 mode) or 30 channels for (E1 mode) to generate an interrupt on the INTB output.

When SIGE is set to logic 1, a change of signaling state in any channel generates an interrupt. When SIGE is set to logic 0, the interrupt is disabled.

ESF:

The framing format in T1 mode is controlled by the ESF bit. A logic 1 in the ESF bit position selects ESF; a logic 0 bit selects SF, SLC®96 or T1DM. When in E1 mode, this bit is ignored.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. IND must be logic 1 for proper operation.

PCCE:

The per-timeslot/per-channel configuration enable bit, PCCE, enables the configuration data in the per-timeslot/per-channel registers to affect the BRSIG and BRPCM data streams. A logic 1 in the PCCE bit position enables the Per-Timeslot/Per-Channel Configuration Register bits in the indirect registers 40H through 5FH; a logic 0 disables the Per-Timeslot/Per-Channel Configuration Register bits in those registers. Please refer to the Per-timeslot/Per-Channel Configuration descriptions for configuration bit details. When the TSB is reset, the PCCE bit is set to logic 0, disabling the Per-Timeslot/Per-Channel Configuration Register bits.

Register 050H, 150H, 250H, 350H: SIGX Change of Signaling State Register (COSS = 1)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	COSS	0
Bit 5	R	COSS[30]	X
Bit 4	R	COSS[29]	X
Bit 3	R	COSS[28]	X
Bit 2	R	COSS[27]	X
Bit 1	R	COSS[26]	X
Bit 0	R	COSS[25]	X

COSS[30:25]:

The COSS[30:25] bits will be set to logic 1 if a change of signaling state occurs on the corresponding E1 timeslot. COSS[30:25] are cleared after this register is read. COSS[30:25] are valid only if CEPT is a logic 1. The COSS bit allows the timeslot to be polled to determine in which timeslot(s) the signaling state has changed. When COSS is a logic 1, the SIGX register space is configured to allow the change of signaling state event bits to be read. When COSS is a logic 0, the SIGX register space is configured to allow indirect access to the configuration and signaling data for each of the 24 T1 or 30 E1 channels.

COSS[25] through COSS[30] correspond to timeslots 26 through 31.

Register 051H, 151H, 251H, 351H: SIGX Timeslot Indirect Status (COSS = 0)

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The Timeslot Indirect Status Register is provided at SIGX read/write address 1.

BUSY:

The BUSY bit is set to logic 1 while the timeslot data is being retrieved or while the configuration data is being written. The bit is set to logic 0 when the read or write cycle has been completed. The BUSY signal holds off a microprocessor read or write access until the SIGX has completed the previous request. This register should be polled until the BUSY bit is logic 0. The bits in this register are valid only when COSS = 0.

Register 051H, 151H, 251H, 351H: SIGX Change Of Signaling State Change (COSS=1)

Bit	Type	Function	Default
Bit 7	R	COSS[24]	X
Bit 6	R	COSS[23]	X
Bit 5	R	COSS[22]	X
Bit 4	R	COSS[21]	X
Bit 3	R	COSS[20]	X
Bit 2	R	COSS[19]	X
Bit 1	R	COSS[18]	X
Bit 0	R	COSS[17]	X

COSS[24:17]:

The COSS[24:17] bits will be set to logic 1 if a change of signaling state occurs on the corresponding E1 timeslot OR T1 channel. COSS[24:17] are cleared after this register is read.

In E1 mode, COSS[17] through COSS[24] correspond to timeslots 18 through 25.

For the purposes of signaling extraction, the T1 channels are indexed 1 through 24.

Register 052H, 152H, 252H, 352H: SIGX Timeslot Indirect Address/Control (COSS = 0)

Bit	Type	Function	Default
Bit 7	R/W	RWB	0
Bit 6	R/W	A[6]	0
Bit 5	R/W	A[5]	0
Bit 4	R/W	A[4]	0
Bit 3	R/W	A[3]	0
Bit 2	R/W	A[2]	0
Bit 1	R/W	A[1]	0
Bit 0	R/W	A[0]	0

If the SIGX is enabled for direct microprocessor access, writing to and reading from the Timeslot Indirect Address Register will not generate any additional accesses.

A[6:0]:

If the SIGX is enabled for indirect microprocessor access, writing to the Timeslot Indirect Address Register initiates a microprocessor access request to one of the registers in segments 2 and 3. The desired register is addressed using the value written to bits A[6:0].

RWB:

The RWB bit indicates which operation is requested. If RWB is set to logic 1, a read is requested. After the request has been issued, the Timeslot Indirect Status register should be monitored to verify completion of the read. The desired register contents can then be found in the Timeslot Indirect Data Register. If RWB is set to logic 0, a write is requested. Data to be written to the microprocessor should first be placed in the Timeslot Indirect Data Register. For both read and write operations, the BUSY bit in the Timeslot Indirect Status Register should be monitored to ensure that the previous access has been completed.

Note: If the value written to A[6:0] addresses a segment 1 register, an access is not initiated.

Register 052H, 152H, 252H, 352H: SIGX Change of Signaling State Register (COSS = 1)

Bit	Type	Function	Default
Bit 7	R	COSS[16]	X
Bit 6	R	COSS[15]	X
Bit 5	R	COSS[14]	X
Bit 4	R	COSS[13]	X
Bit 3	R	COSS[12]	X
Bit 2	R	COSS[11]	X
Bit 1	R	COSS[10]	X
Bit 0	R	COSS[9]	X

COSS[16:9]:

The COSS[16:9] bits will be set to logic 1 if a change of signaling state occurs on the corresponding E1 timeslot or T1 channel. COSS[16:9] are cleared after this register is read.

In E1 mode, COSS[9] through COSS[15] correspond to timeslots 9 through 15 and COSS[16] corresponds to timeslot 17.

For the purposes of signaling extraction, the T1 channels are indexed 1 through 24.

Register 053H, 153H, 253H, 353H: SIGX Timeslot Indirect Data Buffer (COSS = 0)

Bit	Type	Function	Default
Bit 7	R/W	D[7]	X
Bit 6	R/W	D[6]	X
Bit 5	R/W	D[5]	X
Bit 4	R/W	D[4]	X
Bit 3	R/W	D[3]	X
Bit 2	R/W	D[2]	X
Bit 1	R/W	D[1]	X
Bit 0	R/W	D[0]	X

In the case of an indirect write, the Indirect Data Register holds the value that will be written to the desired register when a write is initiated via the Timeslot Indirect Address Register. In the case of an indirect read, the Indirect Data Register will hold the contents of the indirectly addressed register, when the read has been completed. Please refer below to the per-timeslot register descriptions for the expected bit formats.

Register 053H, 153H, 253H, 353H: SIGX Change of Signaling State (COSS = 1)

Bit	Type	Function	Default
Bit 7	R	COSS[8]	X
Bit 6	R	COSS[7]	X
Bit 5	R	COSS[6]	X
Bit 4	R	COSS[5]	X
Bit 3	R	COSS[4]	X
Bit 2	R	COSS[3]	X
Bit 1	R	COSS[2]	X
Bit 0	R	COSS[1]	X

COSS[8:1]:

The COSS[8:1] bits will be set to logic 1 if a change of signaling state occurs on the corresponding E1 timeslot or T1 channel. COSS[8:1] are cleared after this register is read.

In E1 mode, COSS[1] through COSS[8] correspond to timeslots 1 through 8.

For the purposes of signaling extraction, the T1 channels are indexed 1 through 24.

SIGX Indirect Registers

The signaling and per-timeslot functions are allocated within the indirect registers as follows:

Table 20 - SIGX Indirect Register Map

Addr	Register
20H	Signaling Data Register for Ch 1
21H	Signaling Data Register for TS1/Ch 2
22H	Signaling Data Register for TS2/Ch 3
•	•
•	•
•	•
2FH	Signaling Data Register for TS15/Ch 16
30H	Signaling Data Register for Ch 17
31H	Signaling Data Register for TS17/Ch 18

Addr	Register
•	•
•	•
•	•
37H	Signaling Data Register for TS23/Ch 24
38H	Signaling Data Register for TS24
•	•
•	•
•	•
3EH	Signaling Data Register for TS30
3FH	Signaling Data Register for TS31
40H	TS0/Ch 1 Configuration Data
41H	TS1/Ch 2 Configuration Data
•	•
•	•
•	•
57H	TS23/Ch 24 Configuration Data
58H	TS24 Configuration Data
•	•
•	•
•	•
5EH	TS 30 Configuration Data
5FH	TS 31 Configuration Data

Table 21 - SIGX Indirect Registers 20H - 3FH: Timeslot/Channel Signaling Data

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	A TS/Ch ‘n’	X

Bit	Type	Function	Default
Bit 2	R	B TS/Ch ‘n’	X
Bit 1	R	C TS/Ch ‘n’	X
Bit 0	R	D TS/Ch ‘n’	X

Timeslot (E1 mode) and Channel (T1 mode) signaling data can be read from the Timeslot/Channel Signaling Data registers. Addresses 20H - 37H are valid in T1 mode. Addresses 20H-3FH correspond to TS 0 - TS31. In E1 mode, TS0 and TS16 do not contain valid data.

Signaling data is not available for one full signaling multi-frame after the COSS[x] indication is available. If the signaling data is needed in the same signaling multi-frame that the COSS[x] indication is available, the data can be read from the SIGX indirect registers shown in Table 22 and Table 23. Note that the signaling data is stored in nibble format.

Table 22 - SIGX Signaling Data Map (T1 Mode)

Channel	SIGX Addr	Bit Mask	Channel	SIGX Addr	Bit Mask
1	10H	F0H	17	10H	0FH
2	11H	F0H	18	11H	0FH
...	...	...	...	...	...
...	...	...	23	16H	0FH
...	...	...	24	17H	0FH
15	1EH	F0H			
16	1FH	F0H			

Table 23 - SIGX Signaling Data Map (E1 Mode)

Timeslot	SIGX Addr	Bit Mask	Timeslot	SIGX Addr	Bit Mask
0	N/A	N/A	16	N/A	N/A
1	11H	F0H	17	11H	0FH
2	12H	F0H	18	12H	0FH
...	...	...	...	...	...
14	1EH	F0H	30	1EH	0FH
15	1FH	F0H	31	1FH	0FH

Table 24 - Indirect Registers 40H - 5FH: Per-Timeslot Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	RINV[1]	X
Bit 2	R/W	RINV[0]/RFIX	X
Bit 1	R/W	RPOL	X
Bit 0	R/W	RDEBE	X

RINV[1:0] / RFIX:

In T1 mode, the RINV[1] and SIGNINV bit of the RPSC Data Control byte can be used to invert data as shown in Table 25:

Table 25 - SIGX Per-Channel T1 Data Conditioning

RINV[1]	SIGNINV	Effect on PCM Channel Data
0	0	PCM Channel data is unchanged
1	0	All 8 bits of the received PCM channel data are inverted
0	1	Only the MSB of the received PCM channel data is inverted (SIGN bit inversion)
1	1	All bits EXCEPT the MSB of the received PCM channel data is inverted (Magnitude inversion)

In E1 mode, the RINV[1:0] bits select bits within the timeslot are inverted. The bit mapping is as shown in Table 26.

Table 26 - SIGX Per-Channel E1 Data Conditioning

RINV[1]	RINV[0]	Effect on PCM Channel Data
0	0	do not invert
0	1	invert even bits (2,4,6,8)
1	0	invert odd bits (1,3,5,7)
1	1	invert all bits

Because of the distinct requirements for E1 and T1, the register bits have different definitions in the two modes. In E1 mode bit 2 is defined as RINV[0]; whereas in T1 it is RFIX. RINV[1] has a different effect for the two modes.

In T1 mode, RFIX controls whether the signaling bit (the least significant bit of the DS0 channel on BRPCM during signaling frames) is fixed to the polarity specified by the RPOL bit. A logic 1 in the RFIX position enables bit fixing; a logic 0 in the RFIX position disables bit fixing. Note that the RPSC functions (inversion, digital milliwatt code insertion, trunk conditioning, and PRBS detection or insertion) take place after bit fixing.

RPOL:

In T1 mode, the RPOL bit selects the logic level the signaling bit is fixed to when bit fixing is enabled. When RPOL is a logic 1, the signaling is fixed to logic 1. When RPOL is a logic 0, the signaling is fixed to logic 0.

RDEBE:

The RDEBE bit enables debouncing of timeslot/channel signaling bits. A logic 1 in this bit position enables signaling debouncing while a logic 0 disables it. When debouncing is selected, per-timeslot/per-channel signaling transitions are ignored until two consecutive, equal values are sampled. Debouncing is performed on a per signaling bit basis.

Data inversion, data trunk conditioning, and digital milliwatt insertion are performed independently of the received framing format. Digital milliwatt insertion takes precedence over data trunk conditioning which, in turn, takes precedence over the various data inversions.

To enable the RINV[1], RINV[0]/RFIX, RPOL, RDEBE bits, the PCCE bit in the SIGX Configuration Register must be set to logic 1.

Register 054H, 154H, 254H, 354H: T1 XBAS Configuration

Bit	Type	Function	Default
Bit 7	R/W	MTRK	0
Bit 6	R/W	JPN	0
Bit 5	R/W	B8ZS	0
Bit 4	R/W	ESF	0
Bit 3	R/W	FMS1	0
Bit 2	R/W	FMS0	0
Bit 1	R/W	ZCS1	0
Bit 0	R/W	ZCS0	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

MTRK:

The MTRK bit forces trunk conditioning, idle code substitution and signaling conditioning, on all channels when MTRK is a logic 1. This has the same effect as setting the IDLE_CHAN bit in the PCM Control byte and the SIG0 bit in the SIGNALING Control byte for all channels.

JPN:

The JPN bit enables Japanese variations of the standard framing formats. If the JPN bit is a logic 1 and the ESF format is selected (ESF bit is logic 1), the XBAS complies to TTC JT-G704. If the JPN bit is a logic 1 and the SF format is selected, the framing bit of frame 12 is forced to logic 1 when a Yellow alarm is declared. Otherwise, bit 2 in all of the channels is forced to logic 0 to indicate Yellow alarm. Framing insertion must be enabled in order to transmit the alternate SF Yellow alarm.

B8ZS:

The B8ZS bit enables B8ZS line coding when it is a logic 1.

ESF, FMS1, FMS0:

The ESF bit selects either Extended Superframe format or enables the Frame Mode Select bits (FMS) to select either regular superframe, T1DM or SLC®96 framing formats. The mode is encoded as follows:

Table 27 - T1 Framing Formats

ESF	FMS1	FMS0	MODE
0	0	0	SF framing format

ESF	FMS1	FMS0	MODE
0	0	1	T1DM framing format (R bit unaffected)
0	1	0	SLC®96
0	1	1	T1DM framing format (FDL data replaces R bit)
1	0	0	ESF framing format - 4 kbit/s data link
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

ZCS[1:0]:

The ZCS[1:0] bits select the Zero Code Suppression format to be used. These bits are logically ORed with the ZCS[1:0] bits in the TPSC per-channel PCM Control byte. The bits are encoded as follows:

Table 28 - T1 Zero Code Suppression Formats

ZCS1	ZCS0	Zero Code Suppression Format
0	0	None
0	1	GTE Zero Code Suppression (Bit 8 of an all zero channel byte is replaced by a one, except in signaling frames where bit 7 is forced to a one.)
1	0	DDS Zero Code Suppression (All zero data byte replaced with "10011000")
1	1	Bell Zero Code Suppression (Bit 7 of an all zero channel byte is replaced by a one.)

Register 055H, 155H, 255H, 355H: T1 XBAS Alarm Transmit

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	XYEL	0
Bit 0	R/W	XAIS	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register controls the transmission of Yellow or AIS alarm.

XYEL

The XYEL bit enables the XBAS to generate a Yellow alarm in the appropriate framing format. When XYEL is set to logic 1, XBAS is enabled to set bit 2 of each channel to logic 0 for SF and SLC®96 formats, the Y-bit to logic 0 for T1DM format, and XBAS is enabled to transmit repetitions of 1111111100000000 (the Yellow Alarm BOC) on the FDL for ESF format. If the JPN bit of the T1-XBAS Configuration register is a logic 1 and the SF format is selected, the framing bit of frame 12 is forced to logic 1 when a Yellow alarm is enabled. When XYEL is set to logic 0, XBAS is disabled from generating the Yellow alarm.

XAIS:

The XAIS bit enables the XBAS to generate an unframed all-ones AIS alarm. When XAIS is set to logic 1, the XBAS bipolar outputs are forced to pulse alternately, creating an all-ones signal. When XAIS is set to logic 0, the XBAS bipolar outputs operate normally.

Register 056H, 156H, 256H, 356H: T1 XIBC Control

Bit	Type	Function	Default
Bit 7	R/W	EN	0
Bit 6	R/W	UF	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	CL1	0
Bit 0	R/W	CL0	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

EN:

The EN bit controls whether the Inband Code is transmitted or not. A logic 1 in the EN bit position enables transmission of inband codes; a logic 0 in the EN bit position disables inband code transmission.

UF:

The UF bit controls whether the code is transmitted framed or unframed. A logic 1 in the UF bit position selects unframed inband code transmission; a logic 0 in the UF bit position selects framed inband code transmission. Note: the UF register bit controls the XBAS directly and is not qualified by the EN bit. When UF is set to logic 1, the XBAS is disabled and no framing is inserted regardless of the setting of EN. The UF bit should only be written to logic 1 when the EN bit is set, and should be cleared to logic 0 when the EN bit is cleared.

CL1, CL0:

The bit positions CL1 and CL0 of this register indicate the length of the inband loopback code sequence, as follows:

Table 29 - Transmit In-band Code Length

CL1	CL0	Code Length
0	0	5
0	1	6
1	0	7
1	1	8

Codes of 3 or 4 bits in length may be accommodated by treating them as half of a double-sized code (i.e., a 3-bit code would use the 6-bit code length setting).

Register 057H, 157H, 257H, 357H: T1 XIBC Loopback Code

Bit	Type	Function	Default
Bit 7	R/W	IBC7	X
Bit 6	R/W	IBC6	X
Bit 5	R/W	IBC5	X
Bit 4	R/W	IBC4	X
Bit 3	R/W	IBC3	X
Bit 2	R/W	IBC2	X
Bit 1	R/W	IBC1	X
Bit 0	R/W	IBC0	X

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register contains the inband loopback code pattern to be transmitted. The code is transmitted most significant bit (IBC7) first, followed by IBC6 and so on. The code, regardless of the length, must be aligned with the MSB always in the IBC7 position (e.g., a 5-bit code would occupy the IBC7 through IBC2 bit positions). To transmit a 3-bit or a 4-bit code pattern, the pattern must be paired to form a double-sized code (i.e., the 3-bit code '011' would be written as the 6-bit code '011011').

When the COMET-Quad is reset, the contents of this register are not affected.

Register 058H, 158H, 258H, 358H: PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	XFER	0
Bit 0	R	OVR	0

This register contains status information indicating when counter data has been transferred into the holding registers and indicating whether the holding registers have been overrun.

INTE:

The INTE bit controls the generation of a microprocessor interrupt when the transfer clock has caused the counter values to be stored in the holding registers. A logic 1 bit in the INTE position enables the generation of an interrupt via the INTB output; a logic 0 bit in the INTE position disables the generation of an interrupt.

XFER:

The XFER bit indicates that a transfer of counter data has occurred. A logic 1 in this bit position indicates that a latch request, initiated by writing to one of the counter register locations or the Quadrant PMON Update register, was received and a transfer of the counter values has occurred. A logic 0 indicates that no transfer has occurred. The XFER bit is cleared (acknowledged) by reading this register.

OVR:

The OVR bit is the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFER being logic 1) has not been acknowledged before the next transfer clock has been issued and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register.

Registers 059-05FH, 159-15FH, 259-25FH, 359-35FH: Latching Performance Data

The Performance Data registers for a single framer are updated as a group by writing to any of the PMON count registers (addresses 059H-05FH, 159-15FH, 259-25FH, 359-35FH). A write to one (and only one) of these locations loads performance data located in the PMON into the internal holding registers. Alternatively, the Performance Data registers are updated by writing to the Revision/Chip ID/Quadrant PMON Update register (address 00DH). The data contained in the holding registers can then be subsequently read by microprocessor accesses into the PMON count register address space. The latching of count data, and subsequent resetting of the counters, is synchronized to the internal event timing so that no events are missed.

The PMON is loaded with new performance data within 3.5 recovered clock periods of the latch performance data register write. With nominal line rates, the PMON registers should not be polled until 2.3 µsec have elapsed from the "latch performance data" register write.

When the COMET-Quad is reset, the contents of the PMON count registers are unknown until the first latching of performance data is performed.

Register 059H, 159H, 259H, 359H: PMON Framing Bit Error Count

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	FER[6]	X
Bit 5	R	FER[5]	X
Bit 4	R	FER[4]	X
Bit 3	R	FER[3]	X
Bit 2	R	FER[2]	X
Bit 1	R	FER[1]	X
Bit 0	R	FER[0]	X

FER[6:0]:

The FER[6:0] bits indicate the number of framing bit error events that occurred during the previous accumulation interval. The FER counts are suppressed when the framer has lost frame alignment (OOF in the E1-FRMR Framing Status register is logic 1 or INFR in the T1-FRMR Interrupt Status register is logic 0).

In T1 mode, a framing bit error is defined as an F_e-bit error in ESF, a framing bit error in SF, F_T-bit error in SLC®96, or an F-bit error in T1DM.

In E1 mode, the count is either the number of FAS (frame alignment signal) bits (default) or words in error. As an option, a zero in bit 2 of timeslot 0 of non-frame alignment signal (NFAS) frames results in an increment of the framing error count. Refer to the Receive Options register.

Register 05AH: , 15AH, 25AH, 35AH PMON OOF/COFA/Far End Block Error Count LSB

Bit	Type	Function	Default
Bit 7	R	OOF/FEBE[7]	X
Bit 6	R	OOF/FEBE[6]	X
Bit 5	R	OOF/FEBE[5]	X
Bit 4	R	OOF/FEBE[4]	X
Bit 3	R	OOF/FEBE[3]	X
Bit 2	R	OOF/FEBE[2]	X
Bit 1	R	OOF/FEBE[1]	X
Bit 0	R	OOF/FEBE[0]	X

Register 05BH, 15BH, 25BH, 35BH: PMON OOF/COFA/Far End Block Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OOF/FEBE[9]	X
Bit 0	R	OOF/FEBE[8]	X

OOF/FEBE[9:0]:

In T1 mode, the OOF[9:0] bits indicate the number Out Of Frame or Change Of Frame Alignment events that occurred during the previous accumulation interval, as specified by the CCOFA bit in the Receive Options register. If OOF's are being accumulated, the count is incremented each time a severely errored framing event forces a reframe. IF COFA's are being accumulated, the count is incremented if a new alignment differs from the previous alignment.

In E1 mode, the FEBE[9:0] bits indicate the number of far end block error events that occurred during the previous accumulation interval. The FEBE counts are suppressed when the E1-FRMR has lost frame alignment (OOF in the FRMR Framing Status register is set).

Register 05CH, 15CH, 25CH, 35CH: PMON Bit Error/CRC Error Count LSB

Bit	Type	Function	Default
Bit 7	R	BEE/CRCE[7]	X
Bit 6	R	BEE/CRCE[6]	X
Bit 5	R	BEE/CRCE[5]	X
Bit 4	R	BEE/CRCE[4]	X
Bit 3	R	BEE/CRCE[3]	X
Bit 2	R	BEE/CRCE[2]	X
Bit 1	R	BEE/CRCE[1]	X
Bit 0	R	BEE/CRCE[0]	X

Register 05DH, 15DH, 25DH, 35DH: PMON Bit Error/CRC Error Count MSB

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	BEE/CRCE[9]	X
Bit 0	R	BEE/CRCE[8]	X

BEE/CRCE[9:0]:

In T1 mode, the BEE[9:0] bits contain the number of bit error events that occurred during the previous accumulation interval. A bit error event is defined as a CRC-6 error in ESF, a framing bit error in SF, an F_T-bit error in SLC®96, and an F-bit or sync bit error (there can be up to 7 bits in error per frame) in T1DM.

In E1 mode, the CRCE[9:0] bits indicate the number of CRC error events that occurred during the previous accumulation interval. CRC error events are suppressed when the E1-FRMR is out of CRC-4 multiframe alignment (OOCMF bit in the FRMR Framing Status register is set).

Register 05EH, 15EH, 25EH, 35EH: PMON LCV Count (LSB)

Bit	Type	Function	Default
Bit 7	R	LCV[7]	X
Bit 6	R	LCV[6]	X
Bit 5	R	LCV[5]	X
Bit 4	R	LCV[4]	X
Bit 3	R	LCV[3]	X
Bit 2	R	LCV[2]	X
Bit 1	R	LCV[1]	X
Bit 0	R	LCV[0]	X

Register 05FH, 15FH, 25FH, 35FH: PMON LCV Count (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	LCV[12]	X
Bit 3	R	LCV[11]	X
Bit 2	R	LCV[10]	X
Bit 1	R	LCV[9]	X
Bit 0	R	LCV[8]	X

LCV[12:0]:

The LCV[12:0] bits indicate the number of LCV error events that occurred during the previous accumulation interval. An LCV event is defined as the occurrence of a Bipolar Violation or Excessive Zeros. The counting of Excessive Zeros can be disabled by the BPV bit of the Receive Interface Configuration register.

Register 060H, 160H, 260H, 360H: T1 ALMI Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	ESF	0
Bit 3	R/W	FMS1	0
Bit 2	R/W	FMS0	0
Bit 1		Unused	X
Bit 0		Unused	X

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register allows selection of the framing format and the data rate of the Facility Data Link in ESF to allow operation of the CFA detection algorithms.

ESF:

The ESF bit selects either extended superframe format or enables the frame mode select bits to select either regular superframe, T1DM, "alternate" T1DM, or SLC®96 framing formats. A logic 1 in the ESF bit position selects ESF; a logic 0 bit enables FMS1 and FMS0 to select SF, T1DM, "alternate" T1DM, or SLC®96.

FMS1,FMS0:

The FMS1 and FMS0 bits select standard superframe, T1DM, "alternate" T1DM, or SLC®96 framing formats. A logic 00 in these bits enable the SF framing format; a logic 01 in these bit positions enable the T1DM framing format; a logic 10 in these bit positions enable the SLC®96 framing format; and a logic 11 in these bit positions enable the "alternate" T1DM framing format. The "alternate" T1DM framing format configures the ALMI to process the Red alarm as if the SF, SLC®96, or ESF framing format were selected; the Yellow alarm is still processed as T1DM.

When ESF is selected (ESF bit set to logic 1), the FMS1 and FMS0 bits select the data rate and the source channel for the Facility Data Link (FDL) data. A logic 00 in these bits enables the ALMI to receive FDL data and validate the Yellow alarm at the full 4 kbit rate.

The valid combinations of the ESF, FMS1, and FMS0 bits are summarized in the table below:

Table 30 - T1 Framing Modes

ESF	FMS1	FMS0	Mode
0	0	0	Select Superframe framing format
0	0	1	Select T1DM framing format
0	1	0	Select SLC-96 framing format
0	1	1	Select "alternate" T1DM mode
1	0	0	Select ESF framing format & 4 kbit FDL Data Rate
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Register 061H, 161H, 261H, 361H: T1 ALMI Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	FASTD	0
Bit 3	R/W	ACCEL	0
Bit 2	R/W	YELE	0
Bit 1	R/W	REDE	0
Bit 0	R/W	AISE	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register selects which of the three CFA's can generate an interrupt when their logic state changes and enables the "fast" deassertion mode of operation.

FASTD:

The FASTD bit enables the "fast" deassertion of Red and AIS alarms. When FASTD is set to a logic 1, deassertion of Red alarm occurs within 120 ms of going in frame. Deassertion of AIS alarm occurs within 180 ms of either detecting a 60 ms interval containing 127 or more zeros, or going in frame. When FASTD is set to a logic 0, Red and AIS alarm deassertion times remain as defined in the ALMI description.

ACCEL:

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE LOGIC 0 FOR NORMAL OPERATION.

YELE, REDE, AISE:

A logic 1 in the enable bit positions (YELE, REDE, AISE) enables a state change in the corresponding CFA to generate an interrupt; a logic 0 in the enable bit positions disables any state changes to generate an interrupt. The enable bits are independent; any combination of Yellow, Red, and AIS CFA's can be enabled to generate an interrupt.

Register 062H, 162H, 262H, 362H: T1 ALMI Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	YELI	X
Bit 4	R	REDI	X
Bit 3	R	AISI	X
Bit 2	R	YEL	X
Bit 1	R	RED	X
Bit 0	R	AIS	X

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register indicates which of the three Carry Failure Alarms (CFA's) generated an interrupt when their logic state changed in bit positions 5 through 3, and indicate the current state of each CFA in bit positions 2 through 0. A logic 1 in the status positions (YELI, REDI, AISI) indicate that a state change in the corresponding CFA has generated an interrupt; a logic 0 in the status positions indicates that no state change has occurred. Both the status bit positions (bits 5 through 3) and the interrupt generated because of the change in CFA state are cleared to logic 0 when the register containing then is read.

Register 063H, 163H, 263H, 363H: T1 ALMI Alarm Detection Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	REDD	X
Bit 1	R	YELD	X
Bit 0	R	AISD	X

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register indicates the presence or absence of one or more OOF occurrences within the last 40 ms; the presence or absence of the Yellow alarm signal over the last 40 ms; and indicate the presence or absence of the AIS alarm signal over the last 60 ms.

REDD:

When REDD is a logic 1, one or more out of frame events have occurred during the last 40 ms interval. When REDD is a logic 0, no out of frame events have occurred within the last 40 ms interval.

YELD:

When YELD is logic 1, a valid Yellow signal was present during the last 40 ms interval. When YELD is logic 0, the Yellow signal was absent during the last 40 ms interval. For each framing format, a valid Yellow signal is deemed to be present if:

- bit 2 of each channel is not logic 0 for 16 or fewer times during the 40 ms interval for SF and SLC®96 framing formats;
- the Y-bit is not logic 0 for 4 or fewer times during the 40 ms interval for T1DM framing format;
- the 16-bit Yellow bit oriented code is received error-free 8 or more times during the interval for ESF framing format with a 4 kHz data link;
- In a Japanese T1 mode, the 12th F-bit toggles between 1 and 0 signifying a Japanese Yellow alarm

AISD:

When AISD is logic 1, a valid AIS signal was present during the last 60 ms interval. When AISD is logic 0, the AIS signal was absent during the last 60 ms interval. A valid AIS signal is deemed to be present during a 60 ms interval if the out of frame condition has persisted for the entire interval and the received PCM data stream is not logic 0 for 126 or fewer times.

Register 065H, 165H, 265H, 365H: T1 PDVD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	PDV	X
Bit 3	R	Z16DI	X
Bit 2	R	PDVI	X
Bit 1	R/W	Z16DE	0
Bit 0	R/W	PDVE	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

PDV:

The PDV bit indicates the current state of the pulse density violation indication. When PDV is a logic 1, a violation of the pulse density rule exists. When PDV is a logic 0, no violation of the pulse density rule exists. Note: the PDV indication persists for the duration of the pulse density violation. At its minimum, PDV may be asserted for only 1 bit time, therefore, reading this bit may not return a logic 1 even though a pulse density violation has occurred. When the XPDE is enabled for pulse stuffing, PDV remains logic 0.

PDVI, Z16DI:

The PDVI and Z16DI bits identify the source of a generated interrupt. PDVI is a logic 1 whenever a change in the pulse density violation indication generated an interrupt. PDVI is cleared to 0 when this register is read. Z16DI is a logic 1 whenever 16 consecutive zeros are detected. Z16DI is cleared to 0 when this register is read. Note that the PDVI and Z16DI interrupt indications operate regardless of whether interrupts are enabled or disabled.

Z16DE:

The Z16DE bit enables an interrupt to be generated on the microprocessor INTB pin when 16 consecutive zeros are detected. When Z16DE is set to logic 1, interrupt is generation is enabled. When Z16DE is set to logic 0, interrupt generation is disabled.

PDVE:

The PDVE bit enables an interrupt to be generated on the microprocessor INTB pin when a change in the pulse density is detected. When PDVE is set to logic 1, an interrupt is generated whenever a pulse density violation occurs or when the pulse density ceases to exist. When PDVE is set to logic 0, interrupt generation by pulse density violations is disabled.

Register 066H, 166H, 266H, 366H: T1 XBOC Control

Bit	Type	Function	Default
Bit 7	R	BOCSMPI	X
Bit 6	R/W	BOCSMPE	0
Bit 5	R	RDY	X
Bit 4		Unused	X
Bit 3	R/W	RPT[3]	0
Bit 2	R/W	RPT[2]	0
Bit 1	R/W	RPT[1]	0
Bit 0	R/W	RPT[0]	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

BOCSMPI:

The BOCSMPI bit is set high when the XBOC Code register and RPT[3:0] are sampled by the XBOC, indicating that the Code Register is ready to be updated with a new BOC. BOCSMPI will not change while a Control Register read is in process. Instead, BOCSMPI will hold its initial value – its value at the start of a Control Register read cycle, when RDB falls – until the Control Register read cycle is complete, when RDB rises. After RDB rises, BOCSMPI will be cleared to 0 if it was logic 1 during the read, otherwise BOCSMPI will not be cleared.

BOCSMPE:

Setting BOCSMPE to logic 1 enables a hardware interrupt on the INTB output pin when BOCSMPI is logic 1.

RDY:

The RDY bit is set high when the Code Register and RPT[3:0] are sampled by the XBOC, indicating that the XBOC is ready to be updated with a new BOC. Whenever a new BOC is written, RDY goes low, indicating that the BOC has not yet been accepted by the XBOC state machine. Note that if the XBOC code register is written with a new value, causing RDY to fall, and then written with its original value, RDY will rise immediately, indicating that the BOC has been sampled previously.

RPT[3:0]:

These bits contain the 4 bit repeat count used to determine the number (RPT[3:0] + 1) of consecutive, identical, 16-bit bit-oriented code patterns to be transmitted before sampling the XBOC Code Register, and XBOC Control Register again. In the event that the Code Register values do not change, the same bit oriented code pattern will be repeated continuously. The RPT[3:0] bits can be changed at any time, and are sampled at the same time as the bit

oriented code patterns. To obtain the maximum BOC modification rate, RPT[3:0] should be updated and stable within N*16 - 3 bit periods of the INTB interrupt pin going high, where N is the number of times the BOC code is to be repeated.

Register 067H, 167H, 267H, 367H: T1 XBOC Code

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	BOC[5]	1
Bit 4	R/W	BOC[4]	1
Bit 3	R/W	BOC[3]	1
Bit 2	R/W	BOC[2]	1
Bit 1	R/W	BOC[1]	1
Bit 0	R/W	BOC[0]	1

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

BOC[5:0]:

BOC[5:0] enables the XBOC to generate a bit oriented code and selects the 6-bit code to be transmitted.

When this register is written with any 6-bit code other than 111111, that code will be transmitted repeatedly in the ESF Facility Data Link with the format 111111110[BOC0][BOC1][BOC2][BOC3][BOC4][BOC5]0, overwriting any HDLC packets currently being transmitted. When the register is written with 111111, the XBOC is disabled. To obtain the maximum BOC modification rate, BOC[5:0] should be updated and stable within N*16 - 3 CLK cycles of the BOCSMPI bit going high, where N is the number of times the BOC code is to be transmitted.

Register 069H, 169H, 269H, 369H: T1 XPDE Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	STUFE	0
Bit 6	R/W	STUFF	0
Bit 5	R	STUFI	X
Bit 4	R	PDV	X
Bit 3	R	Z16DI	X
Bit 2	R	PDVI	X
Bit 1	R/W	Z16DE	0
Bit 0	R/W	PDVE	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

STUFE:

The STUFE bit enables the occurrence of pulse stuffing to generate an interrupt on INTB. When STUFE is set to logic 1, an interrupt is generated on the occurrence of a bit stuff. When STUFE is a logic 0, bit stuffing occurrences do not generate an interrupt on INTB.

STUFF:

The STUFF bit enables pulse stuffing to occur upon detection of a violation of the pulse density rule. Bit stuffing is performed in such a way that the resulting data stream no longer violates the pulse density rule. When STUFF is set to logic 1, bit stuffing is enabled and the STUFI bit indicates the occurrence of bit stuffs. When STUFF is a logic 0, bit stuffing is disabled and the PDVI bit indicates occurrences of pulse density violation. Also, when STUFF is a logic 0, PCM data passes through XPDE unaltered.

STUFI:

The STUFI bit is valid when pulse stuffing is active. This bit indicates when a bit stuff occurred to eliminate a pulse density violation and that an interrupt was generated due to the bit stuff (if STUFE is logic 1). When pulse stuffing is active, PDVI remains logic 0, indicating that the stuffing has removed the density violation. The STUFI bit is reset to logic 0 once this register is read. If the STUFE bit is also logic 1, the interrupt is also cleared once this register is read.

PDV:

The PDV bit indicates the current state of the pulse density violation indication. When PDV is a logic 1, a violation of the pulse density rule exists. When PDV is a logic 0, no violation of the pulse density rule exists. Note: the PDV indication persists for the duration of the pulse density violation. At its minimum, PDV may be asserted for only 1 bit time, therefore, reading

this bit may not return a logic 1 even though a pulse density violation has occurred. When the XPDE is enabled for pulse stuffing, PDV remains logic 0.

PDVI, Z16DI:

The PDVI and Z16DI bits identify the source of a generated interrupt. PDVI is a logic 1 whenever a change in the pulse density violation indication generated an interrupt. PDVI is cleared to 0 when this register is read. Z16DI is a logic 1 whenever 16 consecutive zeros are detected. Z16DI is cleared to 0 when this register is read. Note that the PDVI and Z16DI interrupt indications operate regardless of whether the corresponding interrupt enables are enabled or disabled. When STUFF is set to logic 1, the PDVI and Z16DI bits are forced to logic 0.

Z16DE:

The Z16DE bit enables an interrupt to be generated on the microprocessor INTB pin when 16 consecutive zeros are detected. When Z16DE is set to logic 1, interrupt is generation is enabled. When Z16DE is set to logic 0, interrupt generation is disabled.

PDVE:

The PDVE bit enables an interrupt to be generated on the microprocessor INTB pin when a change in the pulse density is detected. When PDVE is set to logic 1, an interrupt is generated whenever a pulse density violation occurs or when the pulse density ceases to exist (if STUFE is logic 0). When PDVE is set to logic 0, interrupt generation by pulse density violations is disabled.

Register 06AH, 16AH, 26AH, 36AH: T1 RBOC Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	BOCE	0

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

This register selects the validation criteria to be used in determining a valid bit oriented code (BOC) and enables generation of an interrupt on a change in code status.

IDLE:

The IDLE bit position enables or disables the generation of an interrupt when there is a transition from a validated BOC to idle code. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

AVC:

The AVC bit position selects the validation criteria used in determining a valid BOC. A logic 1 in the AVC bit position selects the "alternate" validation criterion of 4 out of 5 matching BOCs; a logic 0 selects the 8 out of 10 matching BOC criterion.

BOCE:

The BOCE bit position enables or disables the generation of an interrupt on the microprocessor INTB pin when a valid BOC is detected. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

Register 06BH, 16BH, 26BH, 36BH: T1 RBOC Code Status

Bit	Type	Function	Default
Bit 7	R	IDLEI	X
Bit 6	R	BOCI	X
Bit 5	R	BOC[5]	X
Bit 4	R	BOC[4]	X
Bit 3	R	BOC[3]	X
Bit 2	R	BOC[2]	X
Bit 1	R	BOC[1]	X
Bit 0	R	BOC[0]	X

When the E1/T1B bit of the Global Configuration register is a logic 1, this register is held reset.

BOC[5:0]:

The BOC[5:0] bits indicate the current state value of the received bit-oriented code.

IDLEI:

The IDLEI bit position indicates whether an interrupt was generated by the detection of the transition from a valid BOC to idle code. A logic 1 in the IDLEI bit position indicates that a transition from a valid BOC to idle code has generated an interrupt; a logic 0 in the IDLEI bit position indicates that no transition from a valid BOC to idle code has been detected. IDLEI is cleared to logic 0 when the register is read.

BOCI:

The BOCI bit position indicates whether an interrupt was generated by the detection of a valid BOC. A logic 1 in the BOCI bit position indicates that a validated BOC code has generated an interrupt; a logic 0 in the BOCI bit position indicates that no BOC has been detected. BOCI is cleared to logic 0 when the register is read.

Register 06CH, 16CH, 26CH, 36CH: TPSC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

This register allows selection of the microprocessor read access type and output enable control for the Transmit Per-channel Serial Controller.

Reserved:

The Reserved bit must be logic 0 for normal operation.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the COMET-Quad is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-channel functions. When the PCCE bit is set to a logic 1, each channel's PCM Control byte, IDLE Code byte, and SIGNALING Control byte are passed on to the XBAS. When the PCCE bit is set to logic 0, the per-channel functions are disabled.

Register 06DH, 16DH, 26DH, 36DH: TPSC µP Access Status

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

Register 06EH, 16EH, 26EH, 36EH: TPSC Channel Indirect Address/Control

Bit	Type	Function	Default
Bit 7	R/W	R/WB	0
Bit 6	R/W	A6	0
Bit 5	R/W	A5	0
Bit 4	R/W	A4	0
Bit 3	R/W	A3	0
Bit 2	R/W	A2	0
Bit 1	R/W	A1	0
Bit 0	R/W	A0	0

This register allows the µP to access the internal TPSC registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal TPSC register is requested; when R/WB is set to a logic 0, a write to the internal TPSC register is requested.

Register 06FH, 16FH, 26FH, 36FH: TPSC Channel Indirect Data Buffer

Bit	Type	Function	Default
Bit 7	R/W	D7	0
Bit 6	R/W	D6	0
Bit 5	R/W	D5	0
Bit 4	R/W	D4	0
Bit 3	R/W	D3	0
Bit 2	R/W	D2	0
Bit 1	R/W	D1	0
Bit 0	R/W	D0	0

This register contains either the data to be written into the internal TPSC registers when a write request is initiated or the data read from the internal TPSC registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

The internal TPSC registers control the per-channel functions on the Transmit PCM data, provide the per-channel Transmit IDLE Code, and provide the per-channel Transmit signaling control and the alternate signaling bits. The functions are allocated within the registers as follows:

Table 31 - TPSC Indirect Register Map

Addr	Register
20H	PCM Data Control byte for Timeslot 0
21H	PCM Data Control byte for Channel 1/Timeslot 1
22H	PCM Data Control byte for Channel 2/Timeslot 2
•	•
•	•
37H	PCM Data Control byte for Channel 23/Timeslot 23
38H	PCM Data Control byte for Channel 24/Timeslot 24
39H	PCM Data Control byte for Timeslot 25
•	•

Addr	Register
•	•
3EH	PCM Data Control byte for Timeslot 30
3FH	PCM Data Control byte for Timeslot 31
40H	IDLE Code byte for Timeslot 0
41H	IDLE Code byte for Channel 1/Timeslot 1
42H	IDLE Code byte for Channel 2/Timeslot 2
• •	• •
57H	IDLE Code byte for Channel 23/Timeslot 23
58H	IDLE Code byte for Channel 24/Timeslot 24
59H	IDLE Code byte for Timeslot 25
• •	• •
5EH	IDLE Code byte for Timeslot 30
5FH	IDLE Code byte for Timeslot 31
60H	E1 Control byte for Timeslot 0
61H	Signaling/E1 Control byte for Channel 1/Timeslot 1
62H	Signaling/E1 Control byte for Channel 2/Timeslot 2
• •	• •
77H	Signaling/E1 Control byte for Channel 23/Timeslot 23
78H	Signaling/E1 Control byte for Channel 24/Timeslot 24
79H	Signaling/E1 Control byte for Timeslot 25
• •	• •
7EH	Signaling/E1 Control byte for Timeslot 30
7FH	Signaling/E1 Control byte for Timeslot 31

The "Timeslot" designation refers to the E1 assignment. The "Channel" designation refers to the T1 assignment.

The bits within each control byte are allocated as follows:

Table 32 - TPSC Indirect Registers 20H-3FH: PCM Data Control byte

Bit	Type	Function	Default
Bit 7	R/W	INVERT	X
Bit 6	R/W	IDLE_CHAN	X
Bit 5	R/W	DMW	X
Bit 4	R/W	SIGNINV	X
Bit 3	R/W	TEST	X
Bit 2	R/W	LOOP	X
Bit 1	R/W	ZCS0	X
Bit 0	R/W	ZCS1	X

INVERT:

When the INVERT bit is set to a logic 1, data from the BTPCM input is inverted for the duration of that channel.

The INVERT bit only has effect in T1 mode.

IDLE_CHAN:

When the IDLE_CHAN bit is set to a logic 1, data from the IDLE Code Byte replaces the BTPCM input data for the duration of that channel. The IDLE_CHAN bit controls insertion of the IDLE Code Byte only in T1 mode.

When the Nx64Kbit/s mode is active, IDLE_CHAN also controls the generation of BTCLK. When IDLE_CHAN is a logic 0, data is inserted from the transmit backplane interface during that channel, and eight clock pulses are generated on BTCLK. When IDLE_CHAN is a logic 1, an IDLE code byte is inserted, and BTCLK is suppressed for the duration of that channel.

SIGNINV:

When the SIGNINV bit is set to a logic 1, the most significant bit from the BTPCM input is inverted for that channel.

The SIGNINV bit only has effect in T1 mode.

The INVERT and SIGNINV can be used to produce the following types of inversions:

Table 33 - TPSC Transmit Data Conditioning

INVERT	SIGNINV	Effect on PCM Channel Data
0	0	PCM Channel data is unchanged
1	0	All 8 bits of the PCM channel data are inverted
0	1	Only the MSB of the PCM channel data is inverted (SIGN bit inversion)
1	1	All bits EXCEPT the MSB of the PCM channel data is inverted (Magnitude inversion)

DMW:

When the DMW bit is set to a logic 1, the digital milliwatt pattern replaces the BTPCM input data for the duration of that channel.

The DMW bit only has effect in T1 mode.

TEST:

When the TEST bit is set to a logic 1, channel data from the BTPCM input is either overwritten with a test pattern from the PRBS generator block or is routed to the PRBS checker block and compared against an expected test pattern. The RXPATGEN bit in the T1/E1 PRBS Positioning and HDLC Control register determines whether the transmit data is overwritten or compared as shown in the following table:

Table 34 - Transmit Test Pattern Modes

TEST	RXPATGEN	Description
0	X	Channel data is not included in test pattern
1	1	Channel data is routed to PRBS Checker and compared against expected test pattern
1	0	Channel data is overwritten with PRBS test pattern

All the channels that are routed to the PRBS generator/checker are concatenated and treated as a continuous stream in which PRBS patterns are searched for. Similarly, all channels set to be overwritten with PRBS test pattern data are treated such that if the channels are subsequently extracted and concatenated, the PRBS appears in the concatenated stream. PRBS generation/detection can be enabled to work on only the first 7 bits of a channel (for Nx56Kbit/s fractional T1) using the Nx56K_DET and Nx56K_GEN bits in the T1/E1 PRBS Positioning and HDLC Control register. The PRBS generator/checker can also be enabled to work on the entire DS1, including framing bits, using the UNF_GEN and UNF_DET bits in the PRBS Positioning/Control and HDLC Control register.

LOOP:

The LOOP bit enables the DS0 loopback. When the LOOP bit is set to a logic 1, transmit data is overwritten with the corresponding channel data from the receive line. When the Clock Master receive mode is enabled, the receive elastic store is used to align the receive line data to the transmit frame. When the Clock Slave receive mode is enabled, however, the receive elastic store is unavailable to facilitate per-DS0 loopbacks.

Data inversion, idle, loopback and test pattern insertion/checking are performed independent of the transmit framing format. DS0 loopback takes precedence over digital milliwatt pattern insertion. Next in priority is test pattern insertion, which, in turn, takes precedence over idle code insertion. Data inversion has the lowest priority. When test pattern checking is enabled, the transmit data is compared before DS0 loopback, digital milliwatt pattern insertion, idle code insertion or data inversion is performed. None of this prioritizing has any effect on the gapping of BTCLK in Nx64Kbit/s mode. That is, if both DS0 loopback and idle code insertion are enabled for a given channel while in Nx64Kbit/s mode, the DS0 will be looped-back, will not be overwritten with idle code, and BTCLK will be gapped out for the duration of the channel. Similarly, none of the prioritizing has any effect on the generation of test patterns from the PRBS generator, only on the insertion of that pattern. Thus, if both DMW and TEST are set for a given DS0, and RXPATGEN = 0, the test pattern from the PRBS generator will be overwritten with the digital milliwatt code. This same rule also applies to test patterns inserted via the UNF_GEN bit in the PRBS Positioning/Control register.

ZCS0, ZCS1:

The ZCS0 and ZCS1 bits select the zero code suppression used as follows:

Table 35 - Transmit Zero Code Suppression Formats

ZCS0	ZCS1	Description
0	0	No Zero Code Suppression
0	1	“Jammed bit 8" - Every bit 8 is forced to a one. This may be used for 56 kbit/s data service. This is the only code that should be inserted in E1 mode.
1	0	GTE Zero Code Suppression (Bit 8 of an all zero channel byte is replaced by a one, except in signaling frames where bit 7 is forced to a one.)
1	1	Bell Zero Code Suppression (Bit 7 of an all zero channel byte is replaced by a one.)

Table 36 - TPSC Indirect Registers 40H-5FH: IDLE Code byte

Bit	Type	Function	Default
Bit 7	R/W	IDLE7	X

Bit	Type	Function	Default
Bit 6	R/W	IDLE6	X
Bit 5	R/W	IDLE5	X
Bit 4	R/W	IDLE4	X
Bit 3	R/W	IDLE3	X
Bit 2	R/W	IDLE2	X
Bit 1	R/W	IDLE1	X
Bit 0	R/W	IDLE0	X

The contents of the IDLE Code byte register is substituted for the channel data on BTPCM when the IDLE_CHAN bit in the PCM Control Byte is set to a logic 1 in T1 mode or when the SUBS bit of the E1 Control Byte is logic 1 and the DS[0] bit of the E1 Control Byte is logic 0 in E1 mode. The IDLE Code is transmitted from MSB (IDLE7) to LSB (IDLE0).

Table 37 - TPSC Indirect Registers 60H-7FH: Signaling/E1 Control byte

Bit	Type	Function	Default
Bit 7	R/W	SIGC[0]/SUBS	X
Bit 6	R/W	SIGC[1]/DS[0]	X
Bit 5	R/W	DS[1]	X
Bit 4	R/W	SIGSRC	X
Bit 3	R/W	A'	X
Bit 2	R/W	B'	X
Bit 1	R/W	C'	X
Bit 0	R/W	D'	X

The significance of the bits in these registers is dependent on whether the operating mode is T1 or E1.

E1 Mode

SUBS, DS[1], and DS[0]:

The SUBS, DS[1], and DS[0] bits select one of the following data manipulations to be performed on the timeslot:

Table 38 - Transmit Per-timeslot Data Manipulation

SUBS	DS[0]	DS[1]	Function
0	0	0	OFF - no change to PCM timeslot data
0	0	1	ADI - data inversion on timeslot bits 1, 3, 5, 7
0	1	0	ADI - data inversion on timeslot bits 2, 4, 6, 8
0	1	1	INV - data inversion on all timeslot bits
1	0	X	Data substitution on - IDLE code replaces BTPCM timeslot data
1	1	0	Data substitution on - A-Law digital pattern* replaces BTPCM timeslot data.
1	1	1	Data substitution on - µ-Law digital pattern* replaces BTPCM timeslot data.

*Note: The A-Law digital milliwatt pattern used is that defined in Recommendation G.711 for A-law:

Table 39 - A-Law Digital Milliwatt Pattern

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
0	0	1	1	0	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1
0	0	1	1	0	1	0	0
1	0	1	1	0	1	0	0
1	0	1	0	0	0	0	1
1	0	1	0	0	0	0	1
1	0	1	1	0	1	0	0

*Note: The µ-Law digital milliwatt pattern used is that defined in Recommendation G.711 for µ-law:

Table 40 - µ-Law Digital Milliwatt Pattern

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
0	0	0	1	1	1	1	0
0	0	0	0	1	0	1	1

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8
0	0	0	0	1	0	1	1
0	0	0	1	1	1	1	0
1	0	0	1	1	1	1	0
1	0	0	0	1	0	1	1
1	0	0	0	1	0	1	1
1	0	0	1	1	1	1	0

SIGSRC:

The SIGSRC bit is valid only if Channel Associated Signaling (CAS) is selected in the E1-TRAN Configuration Register; otherwise, it is ignored. When valid, the SIGSRC bit selects the source of the timeslot signaling bits: if SIGSRC is a logic 0, the signaling bits are taken from the incoming BTSIG stream in the format specified by the SIGEN and DLEN bits in the E1-TRAN Configuration Register; if SIGSRC is a logic 1, the signaling bits are taken from the A',B',C', and D' bit .

T1 Mode

Signaling insertion is controlled by the SIGC[1:0] bits. The source of the signaling bits is determined by SIGC0: when SIGC0 is set to a logic 1, signaling data is taken from the A', B', C', and D' bits; when SIGC0 is set to logic 0, signaling data is taken from the A,B,C, and D bit locations on the BTSIG input. Signaling insertion is controlled by SIGC1: when SIGC1 is set to a logic 1 and ESF, SF, or SLC®96 transmit format is selected, insertion of signaling bits is enabled; when SIGC1 is set to logic 0, the insertion of signaling bits is disabled. For SF and SLC®96 formats, the C' and D' or C and D bits from Signaling Control byte or BTSIG, respectively, are inserted into the A and B signaling bit positions of every second superframe that is transmitted. It is assumed that C=A and D=B.

Register 070H, 170H, 270H, 370H: RPSC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	Reserved	0
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

This register allows selection of the microprocessor read access type and output enable control for the Receive Per-channel Serial Controller.

Reserved:

The Reserved bit must be logic 0 for normal operation.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the COMET-Quad is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-channel functions. When the PCCE bit is set to a logic 1, the Data Trunk Conditioning Code byte and Signaling Trunk Conditioning Code byte are enabled to modify the received data and extracted signaling data streams (visible on BRPCM and BRSIG, if selected) under direction of each channel's PCM Control byte. When the PCCE bit is set to logic 0, the per-channel functions are disabled.

Register 071H, 171H, 271H, 371H: RPSC µP Access Status

Bit	Type	Function	Default
Bit 7	R	BUSY	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

Register 072H, 172H, 272H, 372H: RPSC Channel Indirect Address/Control

Bit	Type	Function	Default
Bit 7	R/W	R/WB	0
Bit 6	R/W	A6	0
Bit 5	R/W	A5	0
Bit 4	R/W	A4	0
Bit 3	R/W	A3	0
Bit 2	R/W	A2	0
Bit 1	R/W	A1	0
Bit 0	R/W	A0	0

This register allows the µP to access the internal RPSC registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal RPSC register is requested; when R/WB is set to a logic 0, an write to the internal RPSC register is requested.

Register 073H, 173H, 273H, 373H: RPSC Channel Indirect Data Buffer

Bit	Type	Function	Default
Bit 7	R/W	D7	0
Bit 6	R/W	D6	0
Bit 5	R/W	D5	0
Bit 4	R/W	D4	0
Bit 3	R/W	D3	0
Bit 2	R/W	D2	0
Bit 1	R/W	D1	0
Bit 0	R/W	D0	0

This register contains either the data to be written into the internal RPSC registers when a write request is initiated or the data read from the internal RPSC registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

The internal RPSC registers control the per-channel functions on the Receive PCM data, provide the per-channel Data Trunk Conditioning Code and provide the per-channel Signaling Trunk Conditioning Code. The functions are allocated within the registers shown in Table 41:

Table 41 - RPSC Indirect Register Map

Addr	Register
20H	PCM Data Control byte for Timeslot 0
21H	PCM Data Control byte for Channel 1/Timeslot 1
22H	PCM Data Control byte for Channel 2/Timeslot 2
•	•
•	•
37H	PCM Data Control byte for Channel 23/Timeslot 23
38H	PCM Data Control byte for Channel 24/Timeslot 24
39H	PCM Data Control byte for Timeslot 25

Addr	Register
•	•
•	•
3EH	PCM Data Control byte for Timeslot 30
3FH	PCM Data Control byte for Timeslot 31
40H	Data Trunk Conditioning byte for Timeslot 0
41H	Data Trunk Conditioning byte for Channel 1/Timeslot 1
42H	Data Trunk Conditioning byte for Channel 2/Timeslot 2
• •	• •
57H	Data Trunk Conditioning byte for Channel 23/Timeslot 23
58H	Data Trunk Conditioning byte for Channel 24/Timeslot 24
59H	Data Trunk Conditioning byte for Timeslot 25
• •	• •
5EH	Data Trunk Conditioning byte for Timeslot 30
5FH	Data Trunk Conditioning byte for Timeslot 31
61H	Signaling Trunk Conditioning byte for Channel 1/Timeslot 1
62H	Signaling Trunk Conditioning byte for Channel 2/Timeslot 2
• •	• •
77H	Signaling Trunk Conditioning byte for Channel 23/Timeslot 23
78H	Signaling Trunk Conditioning byte for Channel 24/Timeslot 24
79H	Signaling Trunk Conditioning byte for Timeslot 25
• •	• •
7EH	Signaling Trunk Conditioning byte for Timeslot 30
7FH	Signaling Trunk Conditioning byte for Timeslot 31

The "Timeslot" designation refers to the E1 assignment. The "Channel" designation refers to the T1 assignment.

The bits within each control byte are allocated as follows:

Table 42 - RPSC Indirect Registers 20H-3FH: PCM Data Control byte

Bit	Type	Function	Default
Bit 7	R/W	TEST	X
Bit 6	R/W	DTRKC	X
Bit 5	R/W	STRKC	X
Bit 4	R/W	DMW	X
Bit 3	R/W	DMWALAW	X
Bit 2	R/W	SIGNINV	X
Bit 1		Unused	X
Bit 0		Unused	X

TEST:

When the TEST bit is set to a logic 1, receive channel data is either overwritten with a test pattern from the PRBS generator block or is routed to the PRBS checker block and compared against an expected test pattern. The RXPATGEN bit in the Pattern Generator/Detector Positioning/Control register determines whether the transmit data is overwritten or compared as shown in the following table:

Table 43 - Receive Test Pattern Modes

TEST	RXPATGEN	Description
0	X	Channel data is not included in test pattern
1	0	Channel data is routed to the PRBS Checker and compared against expected test pattern
1	1	Channel data is overwritten with the PRBS test pattern

All the channels that are routed to the PRBS Checker are concatenated and treated as a continuous stream in which pseudorandom patterns are searched for. Similarly, all channels set to be overwritten with the PRBS test pattern data are treated such that if the channels are subsequently extracted and concatenated, the PRBS appears in the concatenated stream. PRBS generation/detection can be enabled to work on only the first 7 bits of a channel (for Nx56Kbit/s fractional T1) using the Nx56K_DET and Nx56K_GEN bits in the T1/E1 PRBS Positioning and HDLC Control register. The PRBS generator/checker can also be enabled to work on the entire DS1, including framing bits, using the UNF_GEN and UNF_DET bits in the Pattern Generator/Detector Positioning/Control register.

DTRKC:

When the DTRKC bit is set to a logic 1, data from the Data Trunk Conditioning Code Byte contained within the RPSC indirect registers replaces the BRPCM output data for the duration of that channel.

When the Receive Backplane Configuration register selects a Nx64Kbit/s mode, the DTRKC bit also controls BRCLK generation. If DTRKC is a logic 1, BRCLK is held low for the duration of the channel.

STRKC:

When the STRKC bit is set to a logic 1, data from the Signaling Trunk Conditioning Code Byte contained within the RPSC indirect registers replaces the BRSIG output data for the duration of that channel.

DMW:

When the DMW bit is set to a logic 1, a digital milliwatt pattern replaces the BRPCM output data for the duration of that channel. The particular digital milliwatt pattern used, A-law or u-law, is selected by the DMWALAW bit of this register.

DMWALAW:

When the DMWALAW bit is set to a logic 1, the digital milliwatt pattern replacing the BRPCM output data for the duration of that channel is the A-law pattern (see Table 39). When the DMWALAW bit is set to a logic 0, the digital milliwatt pattern replacing the BRPCM output data for the duration of that channel is the µ-law pattern (see Table 40).

SIGNINV:

When the SIGNINV bit is set to a logic 1, the most significant bit of the data output on the BRPCM pin is the inverse of the received data most significant bit for that channel.

In T1 mode, the RINV[1] of the and SIGNINV bits can be used to invert data as shown in Table 25:

Table 44 - RPSC Indirect Registers 40H-5FH: Data Trunk Conditioning Code byte

Bit	Type	Function	Default
Bit 7	R/W	DTRK7	X
Bit 6	R/W	DTRK6	X
Bit 5	R/W	DTRK5	X
Bit 4	R/W	DTRK4	X
Bit 3	R/W	DTRK3	X
Bit 2	R/W	DTRK2	X

Bit	Type	Function	Default
Bit 1	R/W	DTRK1	X
Bit 0	R/W	DTRK0	X

The contents of the Data Trunk Conditioning Code byte register is substituted for the channel data on BRPCM when the DTRKC bit in the PCM Control Byte is set to a logic 1. The Data Trunk Conditioning Code is transmitted from MSB (DTRK7) to LSB (DTRK0).

Table 45 - RPSC Indirect Registers 61H-7FH: Signaling Trunk Conditioning byte

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	A'	X
Bit 2	R/W	B'	X
Bit 1	R/W	C'	X
Bit 0	R/W	D'	X

The contents of the Signaling Trunk Conditioning Code byte register is substituted for the channel signaling data on BRSIG when the STRKC bit is set to a logic 1. The Signaling Trunk Conditioning Code is placed in least significant nibble of the channel byte.

Register 078H, 178H, 278H, 378H: T1 APRM Configuration/Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	Reserved	0
Bit 2	R/W	CONT_CRC	0
Bit 1	R/W	INTE	0
Bit 0	R/W	AUTOUPDATE	0

Reserved:

These bits must be a logic 0 for correct operation.

AUTOUPDATE:

The AUTOUPDATE bit controls the automatic updating of the performance report on a per second basis. If this bit is set to a logic 1, the Performance Report Messages are generated and updated once a second. When AUTOUPDATE is set to a logic 0, the performance report is not updated.

INTE:

The INTE bit enables the interrupt output pin. When INTE is set to a logic 1, a logic 1 in the INTR bit in the T1 APRM Interrupt Status register asserts the INTB output low. INTR is disabled from generating interrupts when INTE is set to a logic 0.

CONT_CRC:

The CONT_CRC is the Continuous CRC bit. When set to logic 1, the SE and G6 bits in the Performance Report are set to1 and G1, G2, G3, G4, G5 and FE are set to 0. When reset to logic 0, the Gn (n = [1..5]), FE and SE bits are set according to the received CRC errors.

Register 07AH, 17AH, 27AH, 37AH: T1 APRM Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	INTR	X

INTR:

The interrupt (INTR) bit is set to logic 1 on one second boundaries, to signal that the one second data is ready. If the INTE bit is a logic 1, the INTB output is asserted low when INTR is logic 1. INTR is cleared when this register is read.

Register 07BH, 17BH, 27BH, 37BH: T1 APRM One Second Content Octet 2

Bit	Type	Function	Default
Bit 7	R/W	SAPI[5]	0
Bit 6	R/W	SAPI[4]	0
Bit 5	R/W	SAPI[3]	1
Bit 4	R/W	SAPI[2]	1
Bit 3	R/W	SAPI[1]	1
Bit 2	R/W	SAPI[0]	0
Bit 1	R/W	C/R	0
Bit 0	R/W	EA	0

SAPI[5:0]:

The SAPI[5:0] represent the service access point identifier bits. The value of SAPI[5:0] in the performance report is constant i.e., SAPI = 14.

C/R:

The C/R bit is the Command/Response bit. The value of C/R from the CI is set to a logic 0 and the value of the C/R bit from the carrier is set to a logic 1.

EA:

The EA bit is the Extended Address bit in the second octet. The EA bit defaults to logic 0.

Register 07CH, 17CH, 27CH, 37CH: T1 APRM One Second Content Octet 3

Bit	Type	Function	Default
Bit 7	R/W	TEI[6]	0
Bit 6	R/W	TEI[5]	0
Bit 5	R/W	TEI[4]	0
Bit 4	R/W	TEI[3]	0
Bit 3	R/W	TEI[2]	0
Bit 2	R/W	TEI[1]	0
Bit 1	R/W	TEI[0]	0
Bit 0	R/W	EA	1

TEI[6:0]:

The TEI[6:0] bits represent the terminal endpoint identifier. The TEI[6:0] default to logic 0.

EA:

The EA bit is the Extended Address bit in the third octet. The EA bit defaults to logic 1.

Register 07DH, 17DH, 27DH, 37DH: T1 APRM One Second Content Octet 4

Bit	Type	Function	Default
Bit 7	R/W	CONTROL[7]	0
Bit 6	R/W	CONTROL[6]	0
Bit 5	R/W	CONTROL[5]	0
Bit 4	R/W	CONTROL[4]	0
Bit 3	R/W	CONTROL[3]	0
Bit 2	R/W	CONTROL[2]	0
Bit 1	R/W	CONTROL[1]	1
Bit 0	R/W	CONTROL[0]	1

CONTROL[7:0]:

This register set the value of the CONTROL field in the performance report and defaults to "00000011". It is inserted into the fourth octet of the performance report.

Register 07EH, 17EH, 27EH, 37EH: T1 APRM One Second Content MSB (Octet 5)

Bit	Type	Function	Default
Bit 7	R	G3	X
Bit 6	R	LV	X
Bit 5	R	G4	X
Bit 4	R	U1	X
Bit 3	R	U2	X
Bit 2	R	G5	X
Bit 1	R	SL	X
Bit 0	R	G6	X

The contents of this register represent the values encoded in the latest performance report transmitted. This register is updated coincident with the assertion of the INTR bit of the T1 APRM Interrupt Status register.

G3:

This bit is set to a logic-1, if the number of CRC error events in a one second interval is greater than 5 and less than or equal to 10 (i.e., 5 < CRC error events ≤ 10).

LV:

This bit is set to a logic 1, if the number of Line code violation events in a one second interval is greater than or equal to 1 (i.e., LCV ≥ 1).

G4:

This bit is set to a logic 1, if the number of CRC error events in a one second interval is greater than 10 and less than or equal to 100 (i.e., 10 <CRC error events ≤ 100).

U1,U2:

Under Study For Synchronization. The default value is set by the U1 and U2 bits in the T1 APRM configuration register (register 078H).

G5:

This bit is set to a logic 1 if, the number of CRC error events is greater than 100 and less than or equal to 319 (i.e., 100 < CRC error events ≤ 319).

SL:

This bit is set to a logic 1 if, one or more controlled slip events occur in a one second interval i.e. (SL ≥ 1).

G6:

This bit is set to a logic 1 if the number of CRC error events in a one second interval is greater than or equal to 320 (i.e., CRC error events ≥ 320).

Register 07FH, 17FH, 27FH, 37FH: T1 APRM One Second Content LSB (Octet 6)

Bit	Type	Function	Default
Bit 7	R	FE	X
Bit 6	R	SE	X
Bit 5	R	LB	X
Bit 4	R	G1	X
Bit 3	R	R	X
Bit 2	R	G2	X
Bit 1	R	Nm	X
Bit 0	R	NI	X

The contents of this register represent the values encoded in the latest performance report transmitted. This register is updated coincident with the assertion of the INTR bit of the T1 APRM Interrupt Status register.

FE:

This bit is set to a logic 1 if one or more Frame Synchronization Bit Error Event occurs in a 1 second window (SE =0). If more than one FE occurs in a 3 ms window, a SE is declared and the FE bit is set to 0.

SE:

This bit is set to a logic 1 if, Severely Errored Framing Event ≥ 1 (FE =0). If more than one FE occurs in a 3 ms window, a SE is declared and the FE bit is set to 0.

LB:

This bit is set to a logic 1 if the Payload Loopback is activated.

G1:

This bit is set to a logic 1 if the number of CRC error events in a one second interval is equal to 1 (i.e., CRC error events =1).

R:

Reserved. The default value is set by the R bit in the T1 APRM configuration register (register 078H).

G2:

This bit is set to a logic 1 if the number of CRC error events in a one second interval is greater than 1 and less than or equal to 5 (i.e., 1 <CRC error events ≤ 5).

NmNi:

One second Report Modulo 4 Counter. Every second, the value of NmNi is incremented by one for the most recent second. The values NmNi can take are shown in the table below:

Table 46 - NmNi Settings

NmNi	Time
00	t (most recent second)
11	t-1
10	t-2
01	t-3

Register 080H, 180H, 280H, 380H: E1 TRAN Configuration

Bit	Type	Function	Default
Bit 7	R/W	AMI	0
Bit 6	R/W	SIGEN	1
Bit 5	R/W	DLEN	1
Bit 4	R/W	GENCRC	0
Bit 3	R/W	FDIS	0
Bit 2	R/W	FEBEDIS	0
Bit 1	R/W	INDIS	0
Bit 0	R/W	XDIS	0

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

AMI:

The AMI bit enables AMI line coding when set to logic 1; when it is set to logic 0, the HDB3 line coding is enabled.

SIGEN, DLEN:

The SIGEN and DLEN bits select the signaling data source for Timeslot 16 (TS16) as follows:

Table 47 - E1 Signaling Insertion Mode

SIGEN	DLEN	MODE
0	0	Signaling insertion disabled. TS16 data is taken directly from the CCSBTD input when the TCCSEN bit of the Transmit H-MVIP/CCS Enable and Configuration register is logic 1. When TCCSEN is logic 0, TS16 is taken directly from BTPCM TS16.
0	1	HDLC CCS enabled. TS16 data is taken directly from the HDLC/LAPD transmitter.
1	0	Reserved.
1	1	CAS enabled. TS16 data is taken from either BTSIG stream or from the TPSC SIGNALING/E1 Control byte as selected on a per-timeslot basis via the SIGSRC bit. The format of the BTSIG input data stream is shown in the "Functional Timing" section.

When channel associated signaling (CAS) is enabled, the format of the input BTSIG stream is selected by the DLEN bit. A logic 1 in the DLEN bit position selects the PMC compatible

format in which the BTSIG stream contains the signaling data nibble in the lower four bits of the timeslot byte. A logic 0 in the DLEN bit position is reserved and should not be used.

GENCRC:

The GENCRC bit enables generation of the CRC multiframe when set to logic 1. When enabled, the E1-TRAN generates the CRC multiframe alignment signal, calculates and inserts the CRC bits, and if enabled by FEBEDIS, inserts the FEBE indication in the spare bit positions. The CRC bits transmitted during the first submultiframe (SMF) are indeterminate and should be ignored. The CRC bits calculated during the transmission of the n^{th} SMF (SMF n) are transmitted in the following SMF (SMF n+1). When GENCRC is set to logic 0, the CRC generation is disabled. The CRC bits are then set to the logic value contained in the Si[1] bit position in the International/National Bit Control Register and bit 1 of the NFAS frames are set to the value of Si[0] bit if enabled by INDIS, or, if not enabled by INDIS, are taken directly from BTPCM. When BTPCM or Si[1] are transmitted in lieu of the calculated CRC bits, there is no delay of one SMF (i.e., the BTPCM bits received in SMF n are transmitted in the same SMF). The same applies when substituting Si[1] in place of the calculated CRC bits.

FDIS:

The FDIS bit value controls the generation of the framing alignment signal. A logic 1 in the FDIS bit position disables the generation of the framing pattern in TS0 and allows the incoming data on BTPCM to pass through the E1-TRAN transparently. A logic 0 in FDIS enables the generation of the framing pattern, replacing TS0 of frames 0, 2, 4, 6, 8, 10, 12 and 14 with the frame alignment signal, and if enabled by INDIS, replacing TS0 of frames 1, 3, 5, 7, 9, 11, 13 and 15 with the contents of the International Bits Control Register. When FDIS is a logic 1, framing is globally disabled and the values in control bits GENCRC, FEBEDIS, INDIS, and XDIS are ignored.

Note that the above is true only if the AIS bit in the E1-TRAN Transmit Alarm/Diagnostic Control register is a logic 0. If AIS is logic 1, the output bit stream becomes all-ones unconditionally.

INDIS, GENCRC and FEBEDIS:

The INDIS bit controls the insertion of the International and National bits into TS0. When INDIS is set to logic 0, the contents of the E1-TRAN International Bits Control register and the National bits are inserted into TS0 (note that only the national bits that are enabled in the E1-TRAN National Bits Codeword registers are inserted into TS0); when INDIS is a logic 1, the contents of the E1-TRAN International Bits Control register and the E1-TRAN National bits are ignored and the values for those bit positions in the output stream are taken directly from the BTPCM stream. When INDIS and FDIS are logic 0, the bit values used for the International and National bits are dependent upon the values of the GENCRC and FEBEDIS configuration bits, as shown in the following table:

Table 48 - E1 Timeslot 0 Bit 1 Insertion Control Summary

GENCRC	FEBEDIS	Source of International Bits
0	X	Bit position Si[1] in the International Bits Control register is used for the International bit in the frame alignment signal (FAS) frames and the Si[0] bit in the non-frame alignment signal (NFAS) frames if INDIS is logic 0. BTPCM replaces Si[1:0] if INDIS is logic 1.
1	0	The calculated CRC bits are used for the International bit in the FAS frames and the generated CRC multiframe alignment signal and the FEBE bits are used for the International bit in the NFAS frames.
1	1	The calculated CRC bits are used for the International bit in the FAS frames and the generated CRC multiframe alignment signal is used for the International bit in the NFAS frames, with the Si[1:0] bits in the International Bits Control register used for the spare bits.

XDIS:

If FDIS is logic 0 and SIGEN is logic 1, the XDIS bit controls the insertion of the Extra bits in TS16 of frame 0 of the signaling multiframe as follows. When XDIS is set to a logic 0, the contents of the E1-TRAN Extra Bits Control Register are inserted into TS16, frame 0; when XDIS is a logic 1, the contents of the register are ignored and the values for those bits positions in the output stream are taken directly from the BTPCM stream. That is, when XDIS and FDIS are logic 0 and SIGEN is logic 1, the X1, X3 and X4 bit values from the E1-TRAN Extra Bits Control Register are used for the Extra bits in TS16 of frame 0 of the signaling multiframe.

Register 081H, 181H, 281H, 381H: E1 TRAN Transmit Alarm/Diagnostic Control

Bit	Type	Function	Default
Bit 7	R/W	MTRK	0
Bit 6	R/W	FPATINV	0
Bit 5	R/W	SPLRINV	0
Bit 4	R/W	SPATINV	0
Bit 3	R/W	RAI	0
Bit 2	R/W	YBIT	0
Bit 1	R/W	Reserved	0
Bit 0	R/W	AIS	0

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

MTRK:

The MTRK bit forces trunk conditioning (i.e., idle code substitution and signaling substitution) when MTRK is a logic 1. This has the same effect as setting data substitution to IDLE code on timeslots 1-15 and 17-31 (setting bits SUBS and DS[0] to binary 10 in timeslots 1-15 and 17-31) and sourcing the signaling data from the TPCS stream, if SIGEN is logic 1. When SIGEN is logic 0, TS16 will be treated the same as timeslots 1-15 and 17-31 and will contain data sourced from TIDL. TS0 data is determined by the control bits associated with it and is independent of the value of MTRK.

FPATINV:

The FPATINV bit is a diagnostic control bit. When set to logic 1, FPATINV forces the frame alignment signal (FAS) written into TS0 to be inverted (i.e., the correct FAS, 0011011, is substituted with 1100100); when set to logic 0, the FAS is unchanged.

SPLRINV:

The SPLRINV bit is a diagnostic control bit. When set to logic 1, SPLRINV forces the "spoiler bit" written into bit 2 of TS0 of NFAS frames to be inverted (i.e., the spoiler bit is forced to 0); when set to logic 0, the spoiler bit is unchanged.

SPATINV:

The SPATINV bit is a diagnostic control bit. When set to logic 1, SPATINV forces the signaling multiframe alignment signal written into bits 1-4 of TS16 of frame 0 of the signaling multiframe to be inverted (i.e., the correct signaling multiframe alignment signal, 0000, is substituted with 1111); when set to logic 0, the signaling multiframe alignment signal is unchanged.

RAI:

The RAI bit controls the transmission of the Remote Alarm Indication signal. A logic 1 in the RAI bit position causes bit 3 of NFAS frames to be forced to logic 1; otherwise, bit 3 of NFAS frames is a logic 0 unless the AUTOYELLOW register bit is set and a receive defect is present.

YBIT:

The YBIT bit controls the transmission of the signaling multiframe Alarm Indication Signal. A logic 1 in the YBIT bit position causes the Y-bit (bit 6) of TS16 of frame 0 of the signaling multiframe to be forced to logic 1; otherwise, the Y-bit is a logic 0.

Reserved:

This bit must be set to a logic 0 for correct operation.

AIS:

The AIS bit controls the transmission of the Alarm Indication Signal (unframed all-ones). A logic 1 in the AIS bit position forces the output streams to logic 1.

Register 082H, 182H, 282H, 382H: E1 TRAN International/National Control

Bit	Type	Function	Default
Bit 7	R/W	Si[1]	1
Bit 6	R/W	Si[0]	1
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

Si[1:0]:

The bits Si[1] and Si[0] correspond to the International bits. The Si[1] and Si[0] bits can be programmed to any value and will be inserted into bit 1 of each FAS frame and NFAS frame, respectively, when the block is configured for frame generation, INDIS is set to logic 0, and CRC multiframe generation is disabled. When CRC multiframe generation is enabled, both Si[1] and Si[0] are ignored if FEBE indication is enabled; if FEBEDIS is a logic 1 and INDIS = 0, the values programmed in the Si[1] and Si[0] bit positions are inserted into the spare bit locations of frame 13 and frame 15, respectively, of the CRC multiframe. If both FEBEDIS and INDIS are logic 1, data from BTPCM replaces the Si[0] and Si[1] bits in the CRC multiframe.

The Si[1] and Si[0] bits should be programmed to a logic 1 when not being used to carry information.

Register 083H, 183H, 283H, 383H: E1 TRAN Extra Bits Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	X[1]	1
Bit 2		Unused	X
Bit 1	R/W	X[3]	1
Bit 0	R/W	X[4]	1

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

X[4:3,1]:

The X[1], X[3], and X[4] bits control the value programmed in the X[1], X[3], and X[4] bit locations (bits 5,7, and 8) in TS16 of frame 0 of the signaling multiframe, when enabled by XDIS. The X[1], X[3], and X[4] bits should be programmed to a logic 1 when not being used to carry information.

Register 084H, 184H, 284H, 384H: E1 TRAN Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	SIGMFE	0
Bit 3	R/W	NFASE	0
Bit 2	R/W	MFE	0
Bit 1	R/W	SMFE	0
Bit 0	R/W	FRME	0

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

FRME:

When FRME is set to logic 1, the interrupt generated by the FRMI interrupt register is propagated to the INTB output pin. When FRME is set to logic 0, the FRMI interrupt bit is masked.

SMFE:

When SMFE is set to logic 1, the interrupt generated by the SMFI interrupt register is propagated to the INTB output pin. When SMFE is set to logic 0, the SMFI interrupt bit is masked.

MFE:

When MFE is set to logic 1, the interrupt generated by the MFI interrupt register is propagated to the INTB output pin. When MFE is set to logic 0, the MFI interrupt bit is masked.

NFASE:

When NFASE is set to logic 1, the interrupt generated by the NFASI interrupt register is propagated to the INTB output pin. When NFASE is set to logic 0, the NFASI interrupt bit is masked.

SIGMFE:

When SIGMFE is set to logic 1, the interrupt generated by the SIGMFI interrupt register is propagated to the INTB output pin. When SIGMFE is set to logic 0, the SIGMFI interrupt bit is masked.

Register 085H, 185H, 285H, 385H: E1 TRAN Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	SIGMFI	X
Bit 3	R	NFASI	X
Bit 2	R	MFI	X
Bit 1	R	SMFI	X
Bit 0	R	FRMI	X

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

FRMI:

The FRMI interrupt bit is set to logic 1 on frame boundaries, it is set on timeslot 30, bit 7 of every frame in the transmit data stream. The contents of this register are cleared to logic 0 after the register is read.

SMFI:

The SMFI interrupt bit is set to logic 1 on CRC-4 sub multiframe boundaries, it is set on timeslot 30, bit 7 of frame 0 of the CRC submultiframe in the transmit data stream. The contents of this register are cleared to logic 0 after the register is read.

MFI:

The MFI interrupt bit is set to logic 1 on CRC-4 multiframe boundaries, it is set on timeslot 30, bit 7 of frame 0 of the CRC multiframe in the transmit data stream. The contents of this register are cleared to logic 0 after the register is read.

NFASI:

The NFASI interrupt bit is set to logic 1 on NFAS frame boundaries, it is set on timeslot 30, bit 7 of the NFAS frame in the transmit data stream. The contents of this register are cleared to logic 0 after the register is read.

SIGMFI:

The SIGMFI interrupt bit is set to logic 1 on signaling multiframe boundaries, it is set on timeslot 14, bit 1 of frame 0 of the signaling multiframe in the transmit data stream. The contents of this register are cleared to logic 0 after the register is read.

Register 086H, 186H, 286H, 386H: E1 TRAN National Bits Codeword Select

Bit	Type	Function	Default
Bit 7	R/W	SaSEL[2]	X
Bit 6	R/W	SaSEL[1]	X
Bit 5	R/W	SaSEL[0]	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

SaSEL[2:0]:

The SaSEL[2:0] bits select which National Bit codeword appears in the SaX[1:4] bits of the E1-TRAN National Bits Codeword register. These bits map to the codeword selection as follows:

Table 49 - National Bits Codeword Select

SaSEL[2:0]	National Bit Codeword
000	Undefined
001	Undefined
010	Undefined
011	Sa4
100	Sa5
101	Sa6
110	Sa7
111	Sa8

Register 087H, 187H, 287H, 387H: E1 TRAN National Bits Codeword

Bit	Type	Function	Default
Bit 7	R/W	SaX_EN[1]	0
Bit 6	R/W	SaX_EN[2]	0
Bit 5	R/W	SaX_EN[3]	0
Bit 4	R/W	SaX_EN[4]	0
Bit 3	R/W	SaX[1]	1
Bit 2	R/W	SaX[2]	1
Bit 1	R/W	SaX[3]	1
Bit 0	R/W	SaX[4]	1

When the E1/T1B bit of the Global Configuration register is a logic 0, this register is held reset.

SaX[1:4]:

The code word SaX[1:4], (where X = 4, 5, 6, 7 or 8 as selected by the SaSEL[2:0] bits in the E1 TRAN National Bits Codeword Select register) appears in bit X (where X= 4, 5, 6, 7 or 8 as selected by the SaSEL[2:0] bits) of TS0 in frames 1, 3, 5 and 7 respectively (SMF I), or in frames 9, 11, 13 and 15 respectively (SMF II) of a G.704 CRC-4 multiframe. If X = 4, Sa4[1:4] bits appear in bit 4 of frames 1, 3, 5, and 7 respectively (SMF I) or in bit 4 of frames 9, 11, 13, and 15 (SMF II) of a G.704 CRC-4 multiframe. If X = 8, the codeword is inserted into bit 8 of TS 0 in frames 1, 3, 5 and 7 respectively (SMF I), or in frames 9, 11, 13 and 15 respectively (SMF II) of a G.704 CRC-4 multiframe.

The code word written in bits SaX[1:4] is latched internally and is updated every submultiframe. Therefore, If the code word is written into register 7 during SMF I of a G.704 CRC-4 multiframe, it will appear in the SaX[1:4] bits of SMF II of the same multiframe. If the code word is written into register 7 during SMF II of a multiframe, its contents will be latched internally and will appear in SMF I of the next multiframe.

Hence, a code written in SMF I of a multiframe is latched internally and appears in bit positions 4, 5, 6, 7, or 8 of TS0 in frames 9, 11, 13, and 15 of the CRC-4 multiframe. Also, a code word written during SMF II of a G.704 CRC-4 multiframe will appear in bit positions 4, 5, 6, 7, or 8 of TS0 in frames 1, 3, 5 and 7 of the subsequent CRC-4 multiframe.

Note that when Sa8[1:4] has been selected by the SaSEL[2:0] bits, the SaX[1:4] bits are mapped in this register in the reverse order as the SaX[1:4] bits, where X = 4, 5, 6 or 7. That is, Sa8[1] is mapped to bit 0 of this register, Sa8[2] is mapped to bit 1, Sa8[3] is mapped to bit 2, and Sa8[4] is mapped to bit 3.

SaX_EN[1:4]

Bits SaX_EN[1:4] enable the insertion of codeword bits SaX[1:4] (where X = 4, 5, 6, 7, or 8) respectively. If bits SaX_EN[1: 4] are set to logic 1, then the contents of bits SaX[1:4] are substituted into bit X of TS0 (where X = 4, 5, 6, 7, or 8) of NFAS frames 1, 3, 5, and 7 of SMF I, or into NFAS frames 9, 11, 13, and 15 of SMF II. If any one or more of the SaX_EN[1:4] bits are set to logic 0, the respective SaX[1:4] register bit is disabled and will not be written into the G.704 CRC multiframe (i.e. the SaX bit that has been disabled will pass through transparently). The SaX_EN bits are valid only when the INDIS bit in the E1-TRAN Configuration register is set to logic 0.

Register 090H, 190H, 290H, 390H: E1-FRMR Frame Alignment Options

Bit	Type	Function	Default
Bit 7	R/W	CRCEN	1
Bit 6	R/W	CASDIS	0
Bit 5	R/W	C2NCIWCK	0
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	REFR	0
Bit 1	R/W	REFCRCEN	1
Bit 0	R/W	REFRDIS	0

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register selects the various framing formats and framing algorithms supported by the FRMR block.

CRCEN:

The CRCEN bit enables the FRMR to frame to the CRC multiframe. When the CRCEN bit is logic 1, the FRMR searches for CRC multiframe alignment and monitors for errors in the alignment. A logic 0 in the CRCEN bit position disables searching for multiframe and suppresses the OOCMF, CRCE, CMFER, FEBE, CFEBE, RAICCRC, C2NCIW and ICMFPI FRMR status/interrupt bits, forcing them to logic 0.

CASDIS:

The CASDIS bit enables the FRMR to frame to the Channel Associated Signaling multiframe when set to a logic 0. When CAS is enabled, the FRMR searches for signaling multiframe alignment and monitors for errors in the alignment. A logic 1 in the CASDIS bit position disables searching for multiframe and suppresses the OOSMF and the SMFER FRMR outputs, forcing them to logic 0.

C2NCIWCK:

The C2NCIWCK bit enables the continuous checking for CRC multiframe in the CRC to non-CRC interworking mode of the E1-FRMR. If this bit is a logic 0, the E1-FRMR will cease searching for CRC multiframe alignment in CRC to non-CRC interworking mode. If this bit is a logic 1, the E1-FRMR will continue searching for CRC multiframe alignment, even if CRC to non-CRC interworking has been declared.

Reserved:

The Reserved bit must be logic 0 for normal operation.

REFR:

A transition from logic 0 to logic 1 in the REFR bit position forces the re-synchronization to a new frame alignment. The bit must be cleared to logic 0, then set to logic 1 again to generate subsequent re-synchronizations.

REFCRCEN:

The REFCRCEN bit enables excessive CRC errors (≥ 915 errors in one second) to force a re-synchronization to a new frame alignment. Setting the REFCRCEN bit position to logic 1 enables reframe due to excessive CRC errors; setting the REFCRCEN bit to logic 0 disables CRC errors from causing a reframe.

REFRDIS:

The REFRDIS bit disables reframing under any error condition once frame alignment has been found; reframing can be initiated by software via the REFR bit. A logic 1 in the REFRDIS bit position causes the FRMR to remain "locked in frame" once initial frame alignment has been found. A logic 0 allows reframing to occur based on the various error criteria (FER, excessive CRC errors, etc.). Note that while the FRMR remains locked in frame due to REFRDIS=1, a received AIS will not be detected since the FRMR must be out-of-frame to detect AIS.

Register 091H, 191H, 291H, 391H: E1-FRMR Maintenance Mode Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	BIT2C	1
Bit 5	R/W	SMFASC	0
Bit 4	R/W	TS16C	0
Bit 3	R/W	RAIC	0
Bit 2		Unused	X
Bit 1	R/W	AISC	0
Bit 0	R	EXCRCERR	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

BIT2C:

The BIT2C bit enables the additional criterion that loss of frame is declared when bit 2 in timeslot 0 of NFAS frames has been received in error on 3 consecutive occasions: a logic 1 in the BIT2C position enables declaration of loss of frame alignment when bit 2 is received in error; a logic 0 in BIT2C enables declaration of loss of frame alignment based on the absence of FAS frames only.

SMFASC:

The SMFASC bit selects the criterion used to declare loss of signaling multiframe alignment signal: a logic 0 in the SMFASC bit position enables declaration of loss of signaling multiframe alignment when 2 consecutive multiframe alignment patterns have been received in error; a logic 1 in the SMFASC bit position enables declaration of loss of signaling multiframe when 2 consecutive multiframe alignment patterns have been received in error or when timeslot 16 contains logic 0 in all bit positions for 1 or 2 multiframes based on the criterion selected by TS16C.

TS16C:

The TS16C bit selects the criterion used to declare loss of signaling multiframe alignment signal when enabled by the SMFASC: a logic 0 in the TS16C bit position enables declaration of loss of signaling multiframe alignment when timeslot 16 contains logic 0 in all bit positions for 1 multiframe; a logic 1 in the TS16C bit position enables declaration of loss of signaling multiframe when timeslot 16 contains logic 0 in all bit positions for 2 consecutive signaling multiframes.

RAIC:

The RAIC bit selects the criterion used to declare a Remote Alarm Indication (RAI). If RAIC is logic 0, the RAIV indication is asserted upon reception of any A=1 (bit 3 of NFAS frames) and is deasserted upon reception of any A=0. If RAIC is logic 1, the RAIV indication is asserted if A=1 is received on 4 or more consecutive occasions, and is cleared upon reception of any A=0.

AISC :

The AISC bit selects the criterion used for determining AIS alarm indication. If AISC is logic 0, AIS is declared if there is a loss of frame (LOF) indication and a 512-bit period is received with less than 3 zeros. If AISC is a logic 1, AIS is declared if less than 3 zeros are detected in each of 2 consecutive 512-bit periods and is cleared when 3 or more zeros are detected in each of 2 consecutive 512-bit intervals.

EXCRCERR:

The EXCRCERR bit is an active high status bit indicating that excessive CRC evaluation errors (i.e., ≥ 915 errors in one second) have occurred, thereby initiating a reframe if enabled by the REFCRCNE bit of the E1-FRMR Frame Alignment Options register. The EXCRCERR bit is reset to logic 0 after the register is read.

Register 092H, 1902H, 292H, 392H: E1-FRMR Framing Status Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	C2NCIWE	0
Bit 6	R/W	OOFE	0
Bit 5	R/W	OOSMFE	0
Bit 4	R/W	OOCMFE	0
Bit 3	R/W	COFAE	0
Bit 2	R/W	FERE	0
Bit 1	R/W	SMFERE	0
Bit 0	R/W	CMFERE	0

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

C2NCIWE, OOFE, OOSMFE and OOCMFE:

A logic one in bits C2NCIWE, OOFE, OOSMFE and OOCMFE enables the generation of an interrupt on a change of state of C2NCIWV, OOFV, OOSMFV and OOCMFV bits respectively of the E1-FRMR Framing Status register.

COFAE:

A logic one in the COFAE bit enables the generation of an interrupt when the position of the frame alignment has changed.

FERE:

A logic one in the FERE bit enables the generation of an interrupt when an error has been detected in the frame alignment signal.

SMFERE:

A logic one in the SMFERE bit enables the generation of an interrupt when an error has been detected in the signaling multiframe alignment signal.

CMFERE:

A logic one in the CMFERE bit enables the generation of an interrupt when an error has been detected in the CRC multiframe alignment signal.

Register 093H, 193H, 293H, 393H: E1-FRMR Maintenance/Alarm Status Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	RAIE	0
Bit 6	R/W	RMAIE	0
Bit 5	R/W	AISDE	0
Bit 4	R/W	Reserved	0
Bit 3	R/W	REDE	0
Bit 2	R/W	AISE	0
Bit 1	R/W	FEBEE	0
Bit 0	R/W	CRCEE	0

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

RAIE, RMAIE, AISDE, REDE and AISE:

A logic one in bits RAIE, RMAIE, AISDE, REDE or AISE enables the generation of an interrupt on a change of state of the RAIV, RMAIV, AISD, RED and AIS bits respectively of the E1-FRMR Maintenance/Alarm Status register.

Reserved:

This bit must be set to a logic 0 for correct operation.

FEBEE:

When the FEBEE bit is a logic one, an interrupt is generated when a logic zero is received in the Si bits of frames 13 or 15.

CRCEE:

When the CRCEE bit is a logic one, an interrupt is generated when calculated CRC differs from the received CRC remainder.

Register 094H, 194H, 294H, 394H: E1-FRMR Framing Status Interrupt Indication

Bit	Type	Function	Default
Bit 7	R	C2NCIWI	X
Bit 6	R	OOFI	X
Bit 5	R	OOSMFI	X
Bit 4	R	OOCMFI	X
Bit 3	R	COFAI	X
Bit 2	R	FERI	X
Bit 1	R	SMFERI	X
Bit 0	R	CMFERI	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

A logic 1 in any bit position of this register indicates which framing status generated an interrupt by changing state.

C2NCIWI, OOFI, OOSMFI, OOCMFI, and COFAI:

C2NCIWI, OOFI, OOSMFI, OOCMFI, and COFAI indicate when the corresponding status has changed state from logic 0 to logic 1 or vice-versa.

FERI, SMFERI, CMFERI:

FERI, SMFERI, CMFERI indicate when a framing error, signaling multiframe error or CRC multiframe error event has been detected; these bits will be set if one or more errors have occurred since the last register read.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The contents of this register are cleared to logic 0 after the register is read; the interrupt is also cleared if it was generated by any of the Framing Status outputs.

Register 095H, 195H, 295H, 395H: E1-FRMR Maintenance/Alarm Status Interrupt Indication

Bit	Type	Function	Default
Bit 7	R	RAII	X
Bit 6	R	RMAII	X
Bit 5	R	AISDI	X
Bit 4		Unused	X
Bit 3	R	REDI	X
Bit 2	R	AISI	X
Bit 1	R	FEBEI	X
Bit 0	R	CRCEI	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

A logic 1 in any bit position of this register indicates which maintenance or alarm status generated an interrupt by changing state.

RAII, RMAII, AISDI, REDI, and AISI:

RAII, RMAII, AISDI, REDI, and AISI indicate when the corresponding FRMR Maintenance/Alarm Status register bit has changed state from logic 0 to logic 1 or vice-versa.

FEBEI:

The FEBEI bit becomes a logic one when a logic zero is received in the Si bits of frames 13 or 15.

CRCEI:

The CRCEI bit becomes a logic one when a calculated CRC differs from the received CRC remainder.

The bits in this register are set by a single error event.

The interrupt indications within this register work independently from the interrupt enable bits, allowing the microprocessor to poll the register to determine the state of the framer. The contents of this register are cleared to logic 0 after the register is read; the interrupt is also cleared if it was generated by one of the Maintenance/Alarm Status events.

Register 096H, 196H, 296H, 396H: E1-FRMR Framing Status

Bit	Type	Function	Default
Bit 7	R	C2NCIWV	X
Bit 6	R	OOFV	X
Bit 5	R	OOSMFV	X
Bit 4	R	OOCMFV	X
Bit 3	R	OOOFV	X
Bit 2	R	RAICCRCV	X
Bit 1	R	CFEBEV	X
Bit 0	R	V52LINKV	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

Reading this register returns the current state value of the C2NCIW, OOF, OOSMF, OOCMF, OOOF and RAICCRC FRMR framing statuses.

C2NCIWV:

The C2NCIWV bit is set to logic one while the FRMR is operating in CRC to non-CRC interworking mode. The C2NCIWV bit goes to a logic zero once when the FRMR exits CRC to non-CRC interworking mode.

OOFV:

The OOFV bit is a logic one when basic frame alignment has been lost. The OOFV bit goes to a logic zero once frame alignment has been regained.

OOSMFV:

The OOSMFV bit is a logic one when the signaling multiframe alignment has been lost. The OOSMFV bit becomes a logic zero once signaling multiframe has been regained.

OOCMFV:

The OOCMFV bit is a logic one when the CRC multiframe alignment has been lost. The OOCMFV bit becomes a logic zero once CRC multiframe has been regained.

OOOFV:

This bit indicates the current state of the out of offline frame (OOOF) indicator. OOOFV is asserted when the offline framer in the CRC multiframe find procedure is searching for frame alignment.

RAICCRCV:

This bit indicates the current state of the RAI and continuous CRC (RAICCRC) indicator. RAICCRCV is asserted when the remote alarm (A bit) is set high and the CRC error (E bit) is set low for a period of 10 ms.

CFEBEV:

This bit indicates the current state of the continuous FEBE (CFEBE) indicator. CFEBEV is asserted when the CRC error (E bit) is set high on more than 990 occasions in each second (out of 1000 possible occasions) for the last 5 consecutive seconds.

V52LINKV:

This bit indicates the current state of the V5.2 link (V52LINK) identification signal indicator. V52LINKV is asserted if 2 out of the last 3 received Sa7 bits are a logic 0.

Register 097H, 197H, 297H, 397H: E1-FRMR Maintenance/Alarm Status

Bit	Type	Function	Default
Bit 7	R	RAIV	X
Bit 6	R	RMAIV	X
Bit 5	R	AISD	X
Bit 4		Unused	X
Bit 3	R	RED	X
Bit 2	R	AIS	X
Bit 1		Unused	X
Bit 0		Unused	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

Reading this register returns the current state value of the RAI, RMAI, AISD, RED, and AIS maintenance/alarm statuses.

RAIV:

The RAIV bit indicates the remote alarm indication (RAI) value. The RAIV bit is set to logic one when the "A" bit (bit 3 in timeslot 0 of the non-frame alignment signal frame) has been logic one for an interval specified by the RAIC bit in the E1-FRMR Maintenance Mode Options register. When RACI is logic 1, RAIV is set when A=1 for 4 or more consecutive intervals, and is cleared upon reception of any A=0. When RACI is logic 0, RAI is set upon reception of any A=1, and is cleared upon reception of any A=0. The RAIV output is updated every two frames.

RMAIV:

The RMAIV bit indicates the remote multiframe alarm indication (RMAI) value. The RMAIV bit is set to logic one when the "Y" bit (bit 6 in timeslot 16 in frame 0 of the signaling multiframes) has been a logic one for 3 consecutive signaling multiframes, and is cleared upon reception of any Y=0. The RMAIV bit is updated every 16 frames.

AISD:

The AISD bit indicates the alarm indication signal (AIS) detect value. The AISD bit is set to logic one when the incoming data stream has a low zero-bit density for an interval specified by the AISC bit in the E1-FRMR Maintenance Mode Options register. When AISC is logic 0, AISD is asserted when 512-bit periods have been received with 2 or fewer zeros. The indication is cleared when a 512-bit period is received with 3 or more zeros. When AISC is logic 1, AISD is asserted when two consecutive 512 bit periods have been received with 2 or

fewer zeros. The indication is cleared when 2 consecutive 512-bit periods are received, with each period containing 3 or more zeros. The AISD bit is updated once every 512-bit period.

RED:

The RED bit is a logic one if an out of frame condition has persisted for 100 ms. The RED bit returns to a logic zero when a out of frame condition has been absent for 100 ms.

AIS:

The AIS bit is a logic one when an out of frame all-ones condition has persisted for 100 ms. The AIS bit returns to a logic zero when the AIS condition has been absent for 100 ms.

Register 098H, 198H, 298H, 398H: E1-FRMR Timeslot 0 International/National Bits

Bit	Type	Function	Default
Bit 7	R	Si[1]	X
Bit 6	R	Si[0]	X
Bit 5	R	A	X
Bit 4	R	Sa[4]	X
Bit 3	R	Sa[5]	X
Bit 2	R	Sa[6]	X
Bit 1	R	Sa[7]	X
Bit 0	R	Sa[8]	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register returns the International and National bits from TS0 of incoming frames. The Si[1:0], A and Sa[4:8] bits map to TS0 frames as shown in Table 50.

Table 50 - Timeslot 0 Bit Position Allocation

Frame	1	2	3	4	5	6	7	8
FAS	Si[1]	0	0	1	1	0	1	1
NFAS	Si[0]	1	A	Sa[4]	Sa[5]	Sa[6]	Sa[7]	Sa[8]

Si [1]:

Reading the Si[1] bit returns the International bit in the last received FAS frame. This bit is updated upon generation of the BRFPI interrupt on FAS frames.

Si[0]:

Reading the Si[0] bit returns the International bit in the last received NFAS frame. This bit is updated upon generation of the BRFPI interrupt on NFAS frames.

A:

Reading the A bit position returns the Remote Alarm Indication (RAI) bit in the last received NFAS frame. This bit is updated upon generation of the BRFPI interrupt on NFAS frames.

Sa[4:8]:

Reading these bits returns the National bit values in the last received NFAS frame. This bit is updated upon generation of the BRFPI interrupt on NFAS frames.

Register 099H, 199H, 299H, 399H: E1-FRMR CRC Error Counter - LSB

Bit	Type	Function	Default
Bit 7	R	CRCERR[7]	X
Bit 6	R	CRCERR[6]	X
Bit 5	R	CRCERR [5]	X
Bit 4	R	CRCERR [4]	X
Bit 3	R	CRCERR [3]	X
Bit 2	R	CRCERR [2]	X
Bit 1	R	CRCERR [1]	X
Bit 0	R	CRCERR [0]	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

CRCERR[7:0]:

The CRCERR[7:0] register bits contain the least significant byte of the 10-bit CRC error counter value, which is updated every second.

Register 09AH, 19AH, 29AH, 39AH: E1-FRMR CRC Error Counter – MSB/Timeslot 16 Extra Bits

Bit	Type	Function	Default
Bit 7	R	OVR	X
Bit 6	R	NEWDATA	X
Bit 5	R	X[3]	X
Bit 4	R	Y	X
Bit 3	R	X[1]	X
Bit 2	R	X[0]	X
Bit 1	R	CRCERR [9]	X
Bit 0	R	CRCERR [8]	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

This register contains the most significant two bits of the 10-bit CRC error counter value, updated every second.

NEWDATA:

The NEWDATA flag bit indicates that the CRCERR counter register contents have been updated with a new count value accumulated over the last 1 second interval. It is set to logic 1 when the CRC error counter data is transferred into the counter registers, and is reset to logic 0 when this register is read. This bit can be polled to determine the 1 second timing boundary used by the FRMR.

OVR:

The OVR flag bit indicates that the CRCERR counter register contents have not been read within the last 1 second interval, and therefore have been over-written. It is set to logic 1 if CRC error counter data is transferred into the counter registers before the previous data has been read out, and is reset to logic 0 when this register is read.

X[3], Y, X[1], X[0]:

Reading these bits returns the value of the Extra bits (X[3] and X1:0]) and the Remote Signaling Multiframe Alarm bit (Y) in Frame 0, Timeslot 16 of the last received signaling multiframe. These bits are updated upon generation of the BRFPI interrupt on NFAS frames. They map to timeslot 16 as shown in Table 51. Note that the contents of this register are not updated while the E1-FRMR is out of frame.

Table 51 - Signaling Multiframe Timeslot 16, Frame 0 Bit Positions

Bit	1	2	3	4	5	6	7	8
	0	0	0	0	X[3]	Y	X[1]	X[0]

CRCERR[9:8]:

The CRCERR[9:8] register bits contain the two most significant bits of the 10-bit CRC error counter value, which is updated every second.

This CRC error count is distinct from that of PMON because it is guaranteed to be an accurate count of the number of CRC errors in one second; whereas, PMON relies on externally initiated transfers which may not be one second apart.

Register 09BH, 19BH, 29BH, 39BH: E1-FRMR National Bit Codeword Interrupt Enables

Bit	Type	Function	Default
Bit 7	R/W	SaSEL[2]	0
Bit 6	R/W	SaSEL[1]	0
Bit 5	R/W	SaSEL[0]	0
Bit 4	R/W	Sa4E	0
Bit 3	R/W	Sa5E	0
Bit 2	R/W	Sa6E	0
Bit 1	R/W	Sa7E	0
Bit 0	R/W	Sa8E	0

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

SaSEL[2:0]:

The SaSEL[2:0] bits selects which National Bit Codeword appears in the SaX[1:4] bits of the National Bit Codeword register. These bits map to the codeword selection as shown in Table 52:

Table 52 - E1-FRMR Codeword Select

SaSEL[2:0]	National Bit Codeword
001	Undefined
010	Undefined
011	Undefined
100	Sa4
101	Sa5
110	Sa6
111	Sa7
000	Sa8

Sa4E, Sa5E, Sa6E, Sa7E, Sa8E:

The National Use interrupt enables allow changes in Sa code word values to generate an interrupt. If SaXE is a logic 1, a logic 1 in the corresponding SaXI bit of the E1-FRMR National Bit Codeword Interrupts register will result in the assertion low of the INTB output.

The interrupt enable should be logic 0 for any bit receiving a HDLC datalink.

Register 09CH, 19CH, 29CH, 39CH: E1-FRMR National Bit Codeword Interrupts

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	Sa4I	X
Bit 3	R	Sa5I	X
Bit 2	R	Sa6I	X
Bit 1	R	Sa7I	X
Bit 0	R	Sa8I	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

Sa4I, Sa5I, Sa6I, Sa7I, Sa8I:

The National Use interrupt status bits indicate if the debounced version of the individual bits has changed since the last time this register has been read. A logic 1 in one of the bit positions indicates a new nibble codeword is available in the associated SaX[1:4] bits in the National Bit Codeword registers, where N is 4 through 8. If the associated SaXE bit in the E1-FRMR National Bit Interrupt Enables register is a logic 1, a logic 1 in the SaXI results in the assertion of the INTB output.

Register 09DH, 19DH, 29DH, 39DH: E1-FRMR National Bit Codeword

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	SaX[1]	X
Bit 2	R	SaX[2]	X
Bit 1	R	SaX[3]	X
Bit 0	R	SaX[4]	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

SaX[1:4]:

Reading these bits returns the SaX nibble code word extracted from the submultiframe, where 'X' corresponds to the National bit selected by the SaSEL[2:0] bits in the E1-FRMR National Bit Codeword Interrupt Enables register. SaX[1] is from the first SaX bit of the submultiframe; SaX[4] is from the last. A change in the codeword values sets the SaI[X] bit of the E1-FRMR National Bits Codeword Interrupts register.

Register 09EH, 19EH, 29EH, 39EH: E1-FRMR Frame Pulse/Alarm/V5.2 Link ID Interrupt Enables

Bit	Type	Function	Default
Bit 7	R/W	OOOFE	0
Bit 6	R/W	RAICCRCE	0
Bit 5	R/W	CFEBEE	0
Bit 4	R/W	V52LINKE	0
Bit 3	R/W	BRFPE	0
Bit 2	R/W	ICSMFPE	0
Bit 1	R/W	ICMFPE	0
Bit 0	R/W	ISMFPE	0

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

OOOFE:

A logic one in the OOOFE bit enables the generation of an interrupt when the out of offline frame interrupt (OOOFI) is asserted.

RAICCRCE:

A logic one in the RAICCRCE bit enables the generation of an interrupt when a RAI and Continuous CRC condition has been detected in the incoming data stream.

CFEBEE:

A logic one in the CFEBEE bit enables the generation of an interrupt when continuous FEBEs have been detected in the incoming data stream.

V52LINKE:

A logic one in the V52LINKE bit enables the generation of an interrupt when a V5.2 link identification has been detected in the Sa7 bits.

BRFPE:

The input frame pulse interrupt enable bit allows interrupts to be generated on each basic frame pulse. If BRFPE is a logic 1, a logic 1 in the BRFPI bit of the Frame Pulse Interrupts register will result in the assertion low of the INTB output.

ICSMFPE:

The input frame pulse interrupt enable bit allows interrupts to be generated on each CRC submultiframe pulse. If ICSMFPE is a logic 1, a logic 1 in the ICSMFPI bit of the Frame Pulse Interrupts register will result in the assertion low of the INTB output.

ICMFPE:

The input frame pulse interrupt enable bit allows interrupts to be generated on each CRC multiframe pulse. If ISMFPE is a logic 1, a logic 1 in the ISMFPI bit of the Frame Pulse Interrupts register will result in the assertion low of the INTB output.

ISMFPE:

The input frame pulse interrupt enable bit allows interrupts to be generated on each signalling multiframe pulse. If ISMFPE is a logic 1, a logic 1 in the ISMFPI bit of the Frame Pulse Interrupts register will result in the assertion low of the INTB output.

Register 09FH, 19FH, 29FH, 39FH: E1-FRMR Frame Pulse/Alarm Interrupts

Bit	Type	Function	Default
Bit 7	R	OOOFI	X
Bit 6	R	RAICCRCI	X
Bit 5	R	CFEBEI	X
Bit 4	R	V52LINKI	X
Bit 3	R	BRFPI	X
Bit 2	R	ICSMFPI	X
Bit 1	R	ICMFPI	X
Bit 0	R	ISMFPI	X

When the E1/T1B bit of the Global Configuration register is a logic 0 or the UNF bit of the Receive Options register is a logic 1, this register is held reset.

OOOFI:

The OOOFI bit indicates when the out of offline frame indicator (OOOFV) changes state.

RAICCRCI:

The RAICCRCI bit indicates when a RAI and Continuous CRC condition has been detected in the incoming data stream. This interrupt is triggered when the remote alarm (A bit) is set high and the CRC error (E bit) is set low for a period of 10 ms.

CFEBEI:

The CFEBEI bit indicates when continuous FEBEs have been detected in the incoming data stream. This interrupt is triggered when the CRC error (E bit) is set high on more than 990 occasions in each second (out of 1000 possible occasions) for 5 consecutive seconds.

V52LINKI:

V52LINKI indicates when a V5.2 link identification signal has been detected or lost in the Sa7 bits. This bit will toggle any time the V52LINKV bit changes state.

BRFPI:

The input frame pulse interrupt status bit is asserted at timeslot 1, bit position 1 of the frame in the incoming data stream.

ICSMFPI:

The input CRC submultiframe alignment frame pulse interrupt status bit is asserted at timeslot 1, bit position 1 of frame 0 of the CRC submultiframe in the incoming data stream.

ICMFPI:

The input CRC multiframe alignment frame pulse interrupt status bit is asserted at timeslot 1, bit position 1 of frame 0 of the CRC multiframe in the incoming data stream.

ISMFPI:

The input signaling multiframe alignment frame pulse interrupt status bit is asserted at timeslot 17, bit position 1 of frame 0 of the signaling multiframe in the incoming data stream.

Register 0A8H, 1A8H, 2A8H, 3A8H: TDPR Configuration

Bit	Type	Function	Default
Bit 7	R/W	FLGSHARE	1
Bit 6	R/W	FIFOCLR	0
Bit 5	R/W	PREN	0
Bit 4		Unused	X
Bit 3	R/W	EOM	0
Bit 2	R/W	ABT	0
Bit 1	R/W	CRC	1
Bit 0	R/W	EN	0

EN:

The EN bit enables the TDPR functions. When EN is set to logic 1, the TDPR is enabled and flag sequences are sent until data is written into the TDPR Transmit Data register and the E1-TRAN bit is set to logic 1. When the EN bit is set to logic 0, the TDPR is disabled; the incoming backplane data will not be overwritten.

CRC:

The CRC enable bit controls the generation of the CCITT_CRC frame check sequence (FCS). Setting the CRC bit to logic 1 enables the CCITT-CRC generator and appends the 16-bit FCS to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to the end of the message. The CRC type used is the CCITT-CRC with generator polynomial $x^{16} + x^{12} + x^5 + 1$. The high order bit of the FCS word is transmitted first. CRC FCS is also appended to the data transmitted via the Performance Report Interface if CRC is set to logic 1.

ABT:

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 11111110 code (the 0 is transmitted first) to be transmitted after the last byte from the TDPR FIFO is transmitted. The FIFO is then reset. All data in the FIFO will be lost. Aborts are continuously sent and the FIFO is held in reset until this bit is reset to a logic 0. At least one Abort sequence will be sent when the ABT bit transitions from logic 0 to logic 1. Note that PRI insertion takes precedence over the ABT register bit. When a PRI frame is available, the TDPR will transmit 2 flag sequences before, and 1 or 2 flag sequences (depending on the FLGSHARE bit setting) after the PRI frame. If the ABT bit is still set, the TDPR will then transmit the Abort sequence again.

EOM:

The EOM bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is cleared upon a write to the TDPR Transmit Data register.

PREN:

The PREN bit enables the performance reports from the PR interface to be transmitted. When PREN is a logic 1, the message arbitrator circuit will insert the PR reports as soon as it is finished any packet whose transmission is already in progress and the delimiting flags. When PREN is a logic 0, the message arbitrator circuit will ignore requests from the PR interface.

This bit has no effect for TDPR #2 and TDPR #3.

FIFOCLR:

The FIFOCLR bit resets the TDPR FIFO. When set to logic 1, FIFOCLR will cause the TDPR FIFO to be cleared. There is a maximum delay of one TCLK cycle between the setting of this register bit and the execution of the FIFO clear operation.

FLGSHARE:

The FLGSHARE bit configures the TDPR to share the opening and closing flags between successive frames. If FLGSHARE is logic 1, the opening and closing flags between successive frames are shared. If FLGSHARE is logic 0, separate closing and opening flags are inserted between successive frames.

Register 0A9H, 1A9H, 2A9H, 3A9H: TDPR Upper Transmit Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	UTHR[6]	1
Bit 5	R/W	UTHR[5]	0
Bit 4	R/W	UTHR[4]	0
Bit 3	R/W	UTHR[3]	0
Bit 2	R/W	UTHR[2]	0
Bit 1	R/W	UTHR[1]	0
Bit 0	R/W	UTHR[0]	0

UTHR[6:0]:

The UTHR[6:0] bits define the TDPR FIFO fill level which will automatically cause the bytes stored in the TDPR FIFO to be transmitted. Once the fill level exceeds the UTHR[6:0] value, transmission will begin. Transmission will not stop until the last complete packet is transmitted and the TDPR FIFO fill level is below UTHR[6:0] + 1.

The value of UTHR[6:0] must always be greater than the value of LINT[6:0] unless both values are equal to 00H.

Register 0AAH, 1AAH, 2AAH, 3AAH: TDPR Lower Interrupt Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	LINT[6]	0
Bit 5	R/W	LINT[5]	0
Bit 4	R/W	LINT[4]	0
Bit 3	R/W	LINT[3]	0
Bit 2	R/W	LINT[2]	1
Bit 1	R/W	LINT[1]	1
Bit 0	R/W	LINT[0]	1

LINT[6:0]:

The LINT[6:0] bits define the TDPR FIFO fill level which causes an internal interrupt (LFILLI) to be generated. Once the TDPR FIFO level decrements to empty or to a value less than LINT[6:0], LFILLI and BLFILL will be set to logic 1. LFILLI will cause an interrupt on INTB if LFILLE is set to logic 1.

The value of LINT[6:0] must always be less than the value of UTHR[6:0] unless both values are equal to 00H.

Register 0ABH, 1ABH, 2ABH, 3ABH: TDPR Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	PRINTE	0
Bit 3	R/W	FULLE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	UDRE	0
Bit 0	R/W	LFILLE	0

LFILLE:

If LFILLE is a logic 1, a transition to logic 1 on LFILLI will generate an interrupt on INTB.

UDRE:

If UDRE is a logic 1, a transition to logic 1 on UDRI will generate an interrupt on INTB.

OVRE:

If OVRE is a logic 1, a transition to logic 1 on OVRI will generate an interrupt on INTB.

FULLE:

If FULLE is a logic 1, a transition to logic 1 on FULLI will generate an interrupt on INTB.

PRINTE:

If PRINTE is a logic 1, a transition to logic 1 on PRINTI will generate an interrupt on INTB.

Register 0ACH, 1ACH, 2ACH, 3ACH: TDPR Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	FULL	X
Bit 5	R	BLFILL	X
Bit 4	R	PRINTI	X
Bit 3	R	FULLI	X
Bit 2	R	OVRI	X
Bit 1	R	UDRI	X
Bit 0	R	LFILLI	X

Writing to this register will clear the underrun condition if it has occurred.

Consecutive writes to the TDPR Configuration and TDPR Transmit Data register and reads of the TDPR Interrupt Status register should not occur at rates greater than that of Transmit clock.

LFILLI:

The LFILLI bit will transition to logic 1 when the TDPR FIFO level transitions to empty or falls below the value of LINT[6:0] programmed in the TDPR Lower Interrupt Threshold register. LFILLI will assert INTB if it is a logic 1 and LFILLE is programmed to logic 1. LFILLI is cleared when this register is read.

UDRI:

The UDRI bit will transition to 1 when the TDPR FIFO underruns. That is, the TDPR was in the process of transmitting a packet when it ran out of data to transmit. UDRI will assert INTB if it is a logic 1 and UDRE is programmed to logic 1. UDRI is cleared when this register is read.

OVRI:

The OVRI bit will transition to 1 when the TDPR FIFO overruns. That is, the TDPR FIFO was already full when another data byte was written to the TDPR Transmit Data register. OVRI will assert INTB if it is a logic 1 and OVRE is programmed to logic 1. OVRI is cleared when this register is read.

FULLI:

The FULLI bit will transition to logic 1 when the TDPR FIFO is full. FULLI will assert INTB if it is a logic 1 and FULLE is programmed to logic 1. FULLI is cleared when this register is read.

PRINTI:

The PRINTI bit will transition to logic 1 when the sampled PR_AVL signal makes a 0 to 1 transition, indicating that a performance report is ready to be transmitted on the Performance Report Interface. PRINTI will assert INTB if it is a logic 1 and PRINTE is programmed to logic 1. PRINTI is cleared when this register is read.

BLFILL:

The BLFILL bit is set to logic 1 if the current FIFO fill level is below the LINT[7:0] level or is empty.

FULL:

The FULL bit reflects the current condition of the TDPR FIFO. If FULL is a logic 1, the TDPR FIFO already contains 128-bytes of data and can accept no more.

Register 0ADH, 1ADH, 2ADH, 3ADH: TDPR Transmit Data

Bit	Type	Function	Default
Bit 7	R/W	TD[7]	X
Bit 6	R/W	TD[6]	X
Bit 5	R/W	TD[5]	X
Bit 4	R/W	TD[4]	X
Bit 3	R/W	TD[3]	X
Bit 2	R/W	TD[2]	X
Bit 1	R/W	TD[1]	X
Bit 0	R/W	TD[0]	X

Consecutive writes to the TDPR Configuration and TDPR Transmit Data register and reads of the TDPR Interrupt Status register should not occur at rates greater than that of Transmit clock

TD[7:0]:

The TD[7:0] bits contain the data to be transmitted on the data link. Data written to this register is serialized and transmitted (TD[0] is transmitted first).

Register 0B0H, 1B0H, 2B0H, 3B0H: RX-ELST CCS Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IR	1
Bit 0	R/W	OR	1

Reserved:

This bit must be logic 0 for correct operation.

IR:

This bit determines the input rate of the RX-ELST CCS. It must be programmed to the same value as the E1/T1B bit of the Global Configuration Register.

OR:

This bit must be logic 1 for correct operation.

Register 0B1H, 1B1H, 2B1H, 3B1H: RX-ELST CCS Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	SLIPE	0
Bit 1	R	SLIPD	X
Bit 0	R	SLIPI	X

SLIPE:

The SLIPE bit position is an interrupt enable that when set, enables the INTB output to assert low when a slip occurs. When the block is reset the SLIPE bit position is cleared and interrupt generation is disabled.

SLIPD:

The SLIPD bit indicates the direction of the last slip. If the SLIPD bit is a logic 1 then the last slip was due to the frame buffer becoming full; a frame was deleted. If the SLIPD bit is a logic 0 then the last slip was due to the frame buffer becoming empty; a frame was duplicated.

SLIPI:

The SLIPI bit is set if a slip occurred since the last read of this register. The SLIPI bit is cleared upon reading this register.

Register 0B2H, 1B2H, 2B2H, 3B2H: RX-ELST CCS Idle Code

Bit	Type	Function	Default
Bit 7	R/W	D7	1
Bit 6	R/W	D6	1
Bit 5	R/W	D5	1
Bit 4	R/W	D4	1
Bit 3	R/W	D3	1
Bit 2	R/W	D2	1
Bit 1	R/W	D1	1
Bit 0	R/W	D0	1

The contents of this register replace the timeslot data in the CCSBRD serial data stream for the associated COMET quadrant when the framer is out of frame and the RCCSTRKEN bit in the Receive H-MVIP/CCS Enable register is a logic 1. Since the transmission of all ones timeslot data is a common requirement, this register is set to all ones on a reset condition. D7 is the first to be transmitted.

The writing of the idle code pattern is asynchronous with respect to the output data clock. One timeslot of idle code data will be corrupted if the register is written to when the framer is out of frame.

Register 0B4H, 1B4H, 2B4H, 3B4H: TX-ELST CCS Configuration

Bit	Type	Function	Default
Bit 7	R/W	Reserved	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IR	1
Bit 0	R/W	OR	1

Reserved:

This bit must be logic 0 for correct operation.

IR:

This bit must be logic 1 for correct operation.

OR:

This bit determines the output rate of the TX-ELST CCS. It must be programmed to the same value as the E1/T1B bit of the Global Configuration Register.

Register 0B5H, 1B5H, 2B5H, 3B5H: TX-ELST CCS Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	SLIPE	0
Bit 1	R	SLIPD	X
Bit 0	R	SLIPI	X

SLIPE:

The SLIPE bit position is an interrupt enable that when set, enables the INTB output to assert low when a slip occurs. When the block is reset the SLIPE bit position is cleared and interrupt generation is disabled.

SLIPD:

The SLIPD bit indicates the direction of the last slip. If the SLIPD bit is a logic 1 then the last slip was due to the frame buffer becoming full; a frame was deleted. If the SLIPD bit is a logic 0 then the last slip was due to the frame buffer becoming empty; a frame was duplicated.

SLIPI:

The SLIPI bit is set if a slip occurred since the last read of this register. The SLIPI bit is cleared upon reading this register.

Register 0B8H: Receive H-MVIP/CCS Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	RCCSTRKEN	0
Bit 1	R/W	RCCSEN	0
Bit 0	R/W	RHMVIPEN	0

RHMVIPEN:

The Receive H-MVIP Enable bit, RHMVIPEN, configures the Receive stream for Clock Slave: H-MVIP mode. When RHMVIPEN is a logic 1, the Receive stream is configured for Clock Slave: H-MVIP mode and BRPCM[2:4] and BRSIG[1:4] are driven low. To enter Receive Clock Slave: Full T1/E1 with CCS H-MVIP mode, RHMVIPEN is to be programmed to logic 0 and RCCSEN is to be programmed to logic 1.

See the Operation section for more information configuring the COMET-Quad for the Receive Clock Slave: H-MVIP mode of operation.

RCCSEN:

The Receive Common Channel Signaling Enable bit, RCCSEN, configures the Receive stream for Common Channel Signaling (CCS) extraction. When RCCSEN is a logic 1, the extracted CCS is presented on the CCSBRD pin. This bit is ignored when RHMVIPEN is a logic 1. To enter Receive Clock Slave: Full T1/E1 with CCS H-MVIP mode, RCCSEN is to be programmed to logic 1.

RCCSTRKEN:

The Receive Common Channel Signaling Trunk Conditioning Enable bit enables trunk conditioning on the Receive Common Channel Signaling stream upon an out-of-frame condition. If RCCSTRKEN is a logic 1, the contents of the RX-ELST CCS Idle Code register are inserted into the CCSBRD timeslots corresponding to the COMET quadrant reporting out-of-basic frame (i.e., having its OOF status bit is logic 1). This bit only has an effect if RHMVIPEN is logic 0 and RCCSEN is logic 1.

Register 0B9H, 1B9H, 2B9H, 3B9H: Transmit H-MVIP/CCS Enable and Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	TCCS31	0
Bit 3	R/W	TCCS16	0
Bit 2	R/W	TCCS15	0
Bit 1	R/W	TCCSEN	0
Bit 0	R/W	THMVIPEN	0

THMVIPEN:

The Transmit H-MVIP Enable bit, THMVIPEN, enables the Transmit stream on all four quadrants for Clock Slave: H-MVIP mode. When THMVIPEN is a logic 1, the Transmit stream on all quadrants is configured for Clock Slave: H-MVIP mode. To enter Clock Slave: Full T1/E1 with CCS H-MVIP mode, THMVIPEN is to be programmed to logic 0 and TCCSEN is to be programmed to logic 1. THMVIPEN is only defined for Register 0B9H. In Registers 1B9H, 2B9H, and 3B9H, the bits is unused and the default value is ‘X’.

See the Operation section for more information on configuring the COMET-Quad for the Transmit Clock Slave: H-MVIP mode of operation.

TCCSEN:

The Transmit Common Channel Signaling Enable bit, TCCSEN, enables insertion of Common Channel Signaling (CCS) into the transmit frame. In T1 mode, CCS is inserted into either timeslot 23 or timeslot 31, as determined by the MAP bit of the BTIF Frame Pulse Configuration Register. When MAP is a logic 0, CCS is inserted into timeslot 31. When MAP is a logic 1, CCS is inserted into timeslot 23. In E1 mode, CCS is inserted into zero or more of timeslots 15, 16, and 31, as determined by the TCCS15, TCCS16, and TCCS31 register bits.

TCCSEN is to be programmed to logic 1 in Transmit Clock Slave: Full T1/E1 with CCS H-MVIP mode. TCCSEN can optionally be programmed to logic 1 in Transmit Clock Slave: H-MVIP mode.

TCCS15:

The Transmit Common Channel Signaling timeslot 15 bit enables the insertion of Common Channel Signaling into timeslot 15 of the transmit E1 frame. This bit is ignored when TCCSEN is a logic 0 or when in T1 mode.

TCCS16:

The Transmit Common Channel Signaling timeslot 16 bit enables the insertion of Common Channel Signaling into timeslot 16 of the transmit E1 frame. This bit is ignored when TCCSEN is a logic 0 or when in T1 mode.

Note: CCS is inserted upstream of the E1-TRAN. To avoid Timeslot 16 CCS from being overwritten, program both the SIGEN and DLEN bits of the E1 TRAN Configuration register to logic 0.

TCCS31:

The Transmit Common Channel Signaling timeslot 31 bit enables the insertion of Common Channel Signaling into timeslot 31 of the transmit E1 frame. This bit is ignored when TCCSEN is a logic 0 or when in T1 mode.

Register 0BBH: RSYNC Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	RSYNC_SEL[1]	0
Bit 0	R/W	RSYNC_SEL[0]	0

RSYNC_SEL[1:0]:

The RSYNC Select register bits, RSYNC_SEL[1:0], select the source of the RSYNC COMET-Quad output.
When RSYNC_SEL[1:0] = “00”, COMET quadrant #1 is selected as the source.
When RSYNC_SEL[1:0] = “01”, COMET quadrant #2 is selected as the source.
When RSYNC_SEL[1:0] = “10”, COMET quadrant #3 is selected as the source.
When RSYNC_SEL[1:0] = “11”, COMET quadrant #4 is selected as the source.

Register 0BCH: COMET-Quad Master Interrupt Source

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	QUAD[4]	X
Bit 2	R	QUAD[3]	X
Bit 1	R	QUAD[2]	X
Bit 0	R	QUAD[1]	X

QUAD[4:1]:

The QUAD[4:1] register bits allow software to determine the COMET quadrant that produced the interrupt on the INTB output pin. A logic 1 indicates an interrupt was produced from the quadrant.

Reading this register does not remove the interrupt indication; within the corresponding COMET quadrant, the corresponding block's interrupt status register must be read to remove the interrupt indication.

Registers 0C0H, 1C0H, 2C0H, 3C0H: RDLC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	Reserved	0
Bit 3	R/W	MEN	0
Bit 2	R/W	MM	0
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

EN:

The enable (EN) bit controls the overall operation of the RDLC. When EN is set to logic 1, RDLC is enabled; when set to logic 0, RDLC is disabled. When the RDLC is disabled, the FIFO buffer and interrupts are all cleared. When the RDLC is enabled, it will immediately begin looking for flags.

TR:

Setting the terminate reception (TR) bit to logic 1 forces the RDLC to immediately terminate the reception of the current data frame, empty the FIFO buffer, clear the interrupts, and begin searching for a new flag sequence. The RDLC handles a terminate reception event in the same manner as it would the toggling of the EN bit from logic 1 to logic 0 and back to logic 1. Thus, the RDLC state machine will begin searching for flags. An interrupt will be generated when the first flag is detected. The TR bit will reset itself to logic 0 after a rising and falling edge have occurred on the CLK input, once the write strobe (CBI[9]) goes high. If the Configuration Register is read after this time, the TR bit value returned will be logic 0.

MEN:

Setting the Match Enable (MEN) bit to logic 1 enables the detection and storage in the FIFO of only those packets whose first data byte matches either of the bytes written to the Primary or Secondary Match Address Registers, or the universal all ones address. When the MEN bit is logic 0, all packets received are written into the FIFO.

MM:

Setting the Match Mask (MM) bit to logic 1 ignores the PA[1:0] bits of the Primary Address Match Register, the SA[1:0] bits of the Secondary Address Match Register, and the two least significant bits of the universal all ones address when performing the address comparison.

Reserved:

This bit must be set to logic 0 for correct operation.

Registers 0C1H, 1C1H, 2C1H, 3C1H: RDLC Interrupt Control

Bit	Type	Function	Default
Bit 7	R/W	INTE	0
Bit 6	R/W	INTC[6]	0
Bit 5	R/W	INTC[5]	0
Bit 4	R/W	INTC[4]	0
Bit 3	R/W	INTC[3]	0
Bit 2	R/W	INTC[2]	0
Bit 1	R/W	INTC[1]	0
Bit 0	R/W	INTC[0]	0

The contents of the Interrupt Control Register should only be changed when the EN bit in the Configuration Register is logic 0. This prevents any erroneous interrupt generation.

INTC[6:0]:

These bits control the assertion of FIFO fill level set point interrupts. A value of 0 in INTC[6:0] is interpreted as decimal 128.

INTE:

The Interrupt Enable bit (INTE) must be set to logic 1 to allow the internal interrupt status to be propagated to the INTB output.

Registers 0C2H, 1C2H, 2C2H, 3C2H: RDLC Status

Bit	Type	Function	Default
Bit 7	R	FE	X
Bit 6	R	OVR	X
Bit 5	R	COLS	X
Bit 4	R	PKIN	X
Bit 3	R	PBS[2]	X
Bit 2	R	PBS[1]	X
Bit 1	R	PBS[0]	X
Bit 0	R	INTR	X

INTR:

The interrupt (INTR) bit reflects the status of the INTB output unless the INTE bit in the Interrupt Control Register is cleared to logic 0. In that case, the INTB output is forced low and the INTR bit of this register will reflect the state of the internal interrupt latch.

PBS[2:0]

The packet byte status (PBS[2:0]) bits indicate the status of the data last read from the FIFO. The bits are encoded as follows:

Table 53 - Receive Packet Byte Status

PBS[2:0]	Significance
000	Data byte read from the FIFO is not special
001	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the first HDLC flag sequence (01111110) was detected. This indicates that the data link became active.
010	The data byte read from the FIFO is the dummy byte that was written into the FIFO when the HDLC abort sequence (01111111) was detected. This indicates that the data link became inactive.
011	Reserved
100	The data byte read from the FIFO is the last byte of a normally terminated packet with no CRC error and the packet received had an integer number of bytes.
101	The data byte read from the FIFO must be discard because there was a non-integer number of bytes in the packet.

PBS[2:0]	Significance
110	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error. The packet was received in error.
111	The data byte read from the FIFO is the last byte of a normally terminated packet with a CRC error and a non-integer number of bytes. The packet was received in error.

PKIN:

The Packet In (PKIN) bit is logic 1 when the last byte of a non-aborted packet is written into the FIFO. The PKIN bit is cleared to logic 0 after the Status Register is read.

COLS:

The Change of Link Status (COLS) bit is set to logic 1 if the RDLC has detected the HDLC flag sequence (01111110) or HDLC abort sequence (01111111) in the data. This indicates that there has been a change in the data link status. The COLS bit is cleared to logic 0 by reading this register or by clearing the EN bit in the Configuration Register. For each change in link status, a byte is written into the FIFO. If the COLS bit is found to be logic 1 then the FIFO must be read until empty. The status of the data link is determined by the PBS bits associated with the data read from the FIFO.

OVR:

The overrun (OVR) bit is set to logic 1 when data is written over unread data in the FIFO buffer. This bit is not reset to logic 0 until after the Status Register is read. While the OVR bit is logic 1, the RDLC and FIFO buffer are held in the reset state, causing the COLS and PKIN bits to be reset to logic 0.

FE:

The FIFO buffer empty (FE) bit is set to logic 1 when the last FIFO buffer entry is read. The FE bit goes to logic 0 when the FIFO is loaded with new data.

Registers 0C3H, 1C3H, 2C3H, 3C3H: RDLC Data

Bit	Type	Function	Default
Bit 7	R	RD[7]	X
Bit 6	R	RD[6]	X
Bit 5	R	RD[5]	X
Bit 4	R	RD[4]	X
Bit 3	R	RD[3]	X
Bit 2	R	RD[2]	X
Bit 1	R	RD[1]	X
Bit 0	R	RD[0]	X

RD[0] corresponds to the first bit of the serial byte received on the DATA input.

This register is actually a 128-byte FIFO buffer. If data is available, the FE bit in the FIFO Input Status Register is logic 0.

When an overrun is detected, an interrupt is generated and the FIFO buffer is held cleared until the FIFO Input Status Register is read.

Registers 0C4H, 1C4H, 2C4H, 3C4H: RDLC Primary Address Match

Bit	Type	Function	Default
Bit 7	R/W	PA[7]	1
Bit 6	R/W	PA[6]	1
Bit 5	R/W	PA[5]	1
Bit 4	R/W	PA[4]	1
Bit 3	R/W	PA[3]	1
Bit 2	R/W	PA[2]	1
Bit 1	R/W	PA[1]	1
Bit 0	R/W	PA[0]	1

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. PA[0] corresponds to the first bit of the serial byte received on the DATA input. The MM bit in the Configuration Register is used mask off PA[1:0] during the address comparison.

Registers 0C5H, 1C5H, 2C5H, 3C5H: RDLC Secondary Address Match

Bit	Type	Function	Default
Bit 7	R/W	SA[7]	1
Bit 6	R/W	SA[6]	1
Bit 5	R/W	SA[5]	1
Bit 4	R/W	SA[4]	1
Bit 3	R/W	SA[3]	1
Bit 2	R/W	SA[2]	1
Bit 1	R/W	SA[1]	1
Bit 0	R/W	SA[0]	1

The first byte received after a flag character is compared against the contents of this register. If a match occurs, the packet data, including the matching first byte, is written into the FIFO. SA[0] corresponds to the first bit of the serial byte received on the DATA input. The MM bit in the Configuration Register is used mask off SA[1:0] during the address comparison.

Register 0D6H : CSU Configuration

Bit	Type	Function	Default
Bit 7	R/W	CSU_RESET	0
Bit 6	R/W	IDDQ_EN	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	CSU_LOCK	X
Bit 2	R/W	MODE[2]	0
Bit 1	R/W	MODE[1]	0
Bit 0	R/W	MODE[0]	0

MODE[2:0]:

The MODE[2:0] selects the mode of the CSU. Table 54 indicates the required XCLK frequency, and output frequencies for each mode.

Table 54 - Clock Synthesis

MODE[2:0]	XCLK frequency	Transmit clock frequency
000	2.048 MHz	2.048 MHz
001	1.544 MHz	1.544 MHz
01X	Reserved	Reserved
10X	Reserved	Reserved
110	Reserved	Reserved
111	2.048 MHz	1.544 MHz

CSU_LOCK:

The CSU_LOCK bit indicates whether or not the embedded clock synthesis unit (CSU) has achieved phase and frequency lock to XCLK. CSU_LOCK is a logic 1 if the divided down synthesized clock frequency is within 244 ppm of the XCLK frequency. A persistent logic 0 in this bit position may indicate a mismatch between the actual and expected XCLK frequency or a problem with the analog supplies (CAVS and CAVD).

IDDQ_EN:

The IDDQ enable bit (IDDQ_EN) is used to configure the embedded CSU for IDDQ tests. When IDDQ_EN is a logic 1, or the IDDQEN bit in the Master Test register (00BH) is a logic

1, the digital outputs of the CSU are pulled to ground. When either the IDDQ_EN bit or IDDQEN bit is set to logic 1, the HIGHZ bit in the XLPG Line Driver Configuration register must also be set to logic 1.

CSU_RESET:

Setting the CSU_RESET bit to logic 1 causes the embedded CSU to be forced to a frequency much lower than normal operation.

Register 0D8H, 1D8H, 2D8H, 3D8H: RLPS Equalization Indirect Data

Bit	Type	Function	Default
7	R/W	EQ_DATA[31]	0
6	R/W	EQ_DATA[30]	0
5	R/W	EQ_DATA[29]	0
4	R/W	EQ_DATA[28]	0
3	R/W	EQ_DATA[27]	0
2	R/W	EQ_DATA[26]	0
1	R/W	EQ_DATA[25]	0
0	R/W	EQ_DATA[24]	0

EQ_DATA[31:24]:

This register consists of 2-parts: read-only and write-only. Writing this register affects the most significant byte of the input-data to the equalization RAM. Reading it returns the MSB of the RAM location indexed by the RLPS Equalization Indirect Address register.

Register 0D9H, 1D9H, 2D9H, 3D9H: RLPS Equalization Indirect Data

Bit	Type	Function	Default
7	R/W	EQ_DATA[23]	0
6	R/W	EQ_DATA[22]	0
5	R/W	EQ_DATA[21]	0
4	R/W	EQ_DATA[20]	0
3	R/W	EQ_DATA[19]	0
2	R/W	EQ_DATA[18]	0
1	R/W	EQ_DATA[17]	0
0	R/W	EQ_DATA[16]	0

EQ_DATA[23:16]:

This register consists of 2-parts: read-only and write-only. Writing this register affects the second most significant byte of the input-data to the equalization RAM. Reading it returns the second MSB of the RAM location indexed by the RLPS Equalization Indirect Address register.

Register 0DAH, 1DAH, 2DAH, 3DAH: RLPS Equalization Indirect Data

Bit	Type	Function	Default
7	R/W	EQ_DATA[15]	0
6	R/W	EQ_DATA[14]	0
5	R/W	EQ_DATA[13]	0
4	R/W	EQ_DATA[12]	0
3	R/W	EQ_DATA[11]	0
2	R/W	EQ_DATA[10]	0
1	R/W	EQ_DATA[9]	0
0	R/W	EQ_DATA[8]	0

EQ_DATA[15:8]:

This register consists of 2-parts: read-only and write-only. Writing this register affects the second least significant byte of the input-data to the equalization RAM. Reading it returns the corresponding bits of the RAM location indexed by the RLPS Equalization Indirect Address register.

Register 0DBH, 1DBH, 2DBH, 3DBH: RLPS Equalization Indirect Data

Bit	Type	Function	Default
7	R/W	EQ_DATA[7]	0
6	R/W	EQ_DATA[6]	0
5	R/W	EQ_DATA[5]	0
4	R/W	EQ_DATA[4]	0
3	R/W	EQ_DATA[3]	0
2	R/W	EQ_DATA[2]	0
1	R/W	EQ_DATA[1]	0
0	R/W	EQ_DATA[0]	0

EQ_DATA[7:0]:

This register consists of 2-parts: read-only and write-only. Writing this register affects the least significant byte of the input-data to the equalization RAM. Reading it returns the LSB of the RAM location indexed by the RLPS Equalization Indirect Address register.

Register 0DCH, 1DCH, 2DCH, 3DCH: RLPS Equalizer Voltage Reference

Bit	Type	Function	Default
7		unused	X
6		unused	X
5	R/W	EQ_VREF[5]	0
4	R/W	EQ_VREF[4]	0
3	R/W	EQ_VREF[3]	0
2	R/W	EQ_VREF[2]	0
1	R/W	EQ_VREF[1]	0
0	R/W	EQ_VREF[0]	0

EQ_VREF[5:0]:

This register sets the voltage reference of the analog receiver's equalizer. The EQ_VREF[5:0] bits must be programmed to 2CH (101100B).

Register 0E0H, 1E0H, 2E0H, 3E0H: PRBS Generator/Checker Control

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	QRSS	0
Bit 4		Unused	X
Bit 3	R/W	TINV	0
Bit 2	R/W	RINV	0
Bit 1	R/W	AUTOSYNC	1
Bit 0	R/W	MANSYNC	0

QRSS:

The quasi-random signal source (QRSS) bit enables the zero suppression feature required when generating a QRSS sequence. When QRSS is a logic 1, a one is forced in the transmit stream when the following 14 bit positions are all zeros. When QRSS is a logic 0, the zero suppression feature is disabled.

TINV:

The TINV bit controls the logical inversion of the generated data stream. When TINV is a logic 1, the data is inverted. When TINV is a logic 0, the data is not inverted.

RINV:

The RINV bit controls the logical inversion of the received stream before processing. When RINV is a logic 1, the received data is inverted before being processed by the pattern detector. When RINV is a logic 0, the data is not inverted

AUTOSYNC:

The AUTOSYNC bit enables the automatic resynchronization of the pattern detector. The automatic resynchronization is activated when 10 or more bit errors are detected in a fixed 48-bit window. When AUTOSYNC is a logic 1, the auto resync feature is enabled. When AUTOSYNC is a logic 0, the auto sync feature is disabled, and pattern resynchronization is accomplished using the MANSYNC bit.

MANSYNC:

The MANSYNC bit is used to initiate a manual resynchronization of the pattern detector. A low to high transition on MANSYNC initiates the resynchronization.

Register 0E1H, 1E1H, 2E1H, 3E1H: PRBS Checker Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	SYNCE	0
Bit 6	R/W	BEE	0
Bit 5	R/W	XFERE	0
Bit 4	R	SYNCV	X
Bit 3	R	SYNCI	X
Bit 2	R	BEI	X
Bit 1	R	XFERI	X
Bit 0	R	OVR	X

SYNCE:

The SYNCE bit enables the generation of an interrupt when the PRBS checker changes synchronization state. When SYNCE is set to logic 1, the interrupt is enabled.

BEE:

The BEE bit enables the generation of an interrupt when a bit error is detected in the receive data. When BEE is set to logic 1, the interrupt is enabled.

XFERE:

The XFERE bit enables the generation of an interrupt when an accumulation interval is completed and new values are stored in the error counter holding registers. When XFERE is set to logic 1, the interrupt is enabled.

SYNCV:

The SYNCV bit indicates the synchronization state of the PRBS checker. When SYNCV is a logic 1 the PRBS checker is synchronized (the PRBS checker has observed at least 32 consecutive error free bit periods). When SYNCV is a logic 0, the PRBS checker is out of sync (the PRBS checker has detected 6 or more bit errors in a 64 bit period window).

SYNCI:

The SYNCI bit indicates that the detector has changed synchronization state since the last time this register was read. If SYNCI is logic 1, the pattern detector has gained or lost synchronization at least once. SYNCI is set to logic 0 when this register is read.

BEI:

The BEI bit indicates that one or more bit errors have been detected since the last time this register was read. When BEI is set to logic 1, at least one bit error has been detected. BEI is set to logic 0 when this register is read.

XFERI:

The XFERI bit indicates that a transfer of the error count has occurred. A logic 1 in this bit position indicates that the error counter holding registers has been updated. This update is initiated by writing to one of the PRBS Error Count register locations, or by writing to the Quadrant PMON Update register. XFERI is set to logic 0 when this register is read.

OVR:

The OVR bit is the overrun status of the Error Count registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFERI being logic 1) has not been acknowledged before the next accumulation interval has occurred and that the contents of the error counter holding registers have been overwritten. OVR is set to logic 0 when this register is read.

Register 0E2H, 1E2H, 2E2H, 3E2H: PRBS Pattern Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	PATSEL[1]	0
Bit 0	R/W	PATSEL[0]	0

PATSEL[1:0]:

PATSEL[1:0] determines which of the three PRBS patterns are generated and checked for errors.

PATSEL[1:0]	Pattern
00	2^{15}-1
01	2^{20}-1
10	2^{11}-1
11	Reserved

Register 0E4H, 1E4H, 2E4H, 3E4H: PRBS Error Count #1

Bit	Type	Function	Default
Bit 7	R	ERRCNT[7]	X
Bit 6	R	ERRCNT[6]	X
Bit 5	R	ERRCNT[5]	X
Bit 4	R	ERRCNT[4]	X
Bit 3	R	ERRCNT[3]	X
Bit 2	R	ERRCNT[2]	X
Bit 1	R	ERRCNT[1]	X
Bit 0	R	ERRCNT[0]	X

Register 0E5H, 1E5H, 2E5H, 3E5H: PRBS Error Count #2

Bit	Type	Function	Default
Bit 7	R	ERRCNT[15]	X
Bit 6	R	ERRCNT[14]	X
Bit 5	R	ERRCNT[13]	X
Bit 4	R	ERRCNT[12]	X
Bit 3	R	ERRCNT[11]	X
Bit 2	R	ERRCNT[10]	X
Bit 1	R	ERRCNT[9]	X
Bit 0	R	ERRCNT[8]	X

Register 0E6H, 1E6H, 2E6H, 3E6H: PRBS Error Count #3

Bit	Type	Function	Default
Bit 7	R	ERRCNT[23]	X
Bit 6	R	ERRCNT[22]	X
Bit 5	R	ERRCNT[21]	X
Bit 4	R	ERRCNT[20]	X
Bit 3	R	ERRCNT[19]	X
Bit 2	R	ERRCNT[18]	X
Bit 1	R	ERRCNT[17]	X
Bit 0	R	ERRCNT[16]	X

ERRCNT[23:0]:

ERRCNT[23:0] contain the error counter holding register. The value in this register represents the number of bit errors that have been accumulated since the last accumulation interval. Note that bit errors are not accumulated while the pattern detector is out of sync.

The Error Count registers for each individual PRBS generator/Checker are updated by writing to any one of the Error count registers. Alternatively, the Error Count registers are updated with all other quadrant counter registers by writing to the Revision/Chip ID/Quadrant PMON Update register.

Register 0F0H, 1F0H, 2F0H, 3F0H: XLPG Line Driver Configuration

Bit	Type	Function	Default
Bit 7	R/W	HIGHZ	1
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	SCALE[4]	0
Bit 3	R/W	SCALE[3]	0
Bit 2	R/W	SCALE[2]	0
Bit 1	R/W	SCALE[1]	0
Bit 0	R/W	SCALE[0]	0

HIGHZ:

The HIGHZ bit controls if the TXTIP and TXRING outputs are to be tri-stated or not. When the HIGHZ bit is set to a logic 0, the outputs are enabled. When the HIGHZ bit is set to a logic 1 then the outputs are put into high impedance. Setting HIGHZ to logic 1 has the same effect as setting SCALE[4:0] to 00H.

SCALE[4:0]:

The SCALE[4:0] bits control the amplitude of the D/A output waveform. The full scale output amplitude is increased by increments of 11.14 mA. A value of 0 (00H) tristates the output while the maximum value of 21 (15H) sets the full scale current to 234 mA.

Table 55 - Transmit Output Amplitude

SCALE[4:0]	Output Amplitude
0 00000	0 mA (tristate)
1-20 00001-10100	Increments of 11.14 mA for each D/A step
21 10101	234 mA total
>21 10110-11111	Reserved

Register 0F1H, 1F1H, 2F1H, 3F1H: XLPG Control/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	OVRFLW	X
Bit 1	R/W	Reserved	0
Bit 0	R/W	Reserved	1

OVRFLW:

The overflow detection value bit (OVRFLW) indicates the presence or absence of an overflow condition in the waveform computation pipeline. An overflow occurs when the sum of the five unit interval (UI) samples exceeds the maximum D/A value. The XLPG detects overflows and saturates the output value to minimize their impact on the output signal. Overflows can easily be eliminated by changing the waveform programming. This status bit is set to logic 1 when an overflow condition is detected and it is reset to logic 0 only when this register is read. It is suggested to read this register twice after the programming of a new waveform and transmission of data to ensure the maximum output amplitude is never exceeded.

Reserved:

The Reserved bits must remain in their default state for correct operation.

Register 0F2H, 1F2H, 2F2H, 3F2H: XLPG Pulse Waveform Storage Write Address

Bit	Type	Function	Default
Bit 7	R/W	SAMPLE[4]	0
Bit 6	R/W	SAMPLE[3]	0
Bit 5	R/W	SAMPLE[2]	0
Bit 4	R/W	SAMPLE[1]	0
Bit 3	R/W	SAMPLE[0]	0
Bit 2	R/W	UI[2]	0
Bit 1	R/W	UI[1]	0
Bit 0	R/W	UI[0]	0

UI[2:0]:

The pulse waveform write address is composed of a unit interval selector and a sample selector. The unit interval selector (UI[2:0]) selects which unit interval is being written for a given sample. There are 5 unit intervals, numbered from 0 to 4. UI[2:0] can take the values 0H, 1H, 2H, 3H and 4H. The values 5H, 6H and 7H are undefined.

SAMPLE[4:0]:

The pulse waveform write address is composed of a unit interval selector and a sample selector. The sample selector (SAMPLE[4:0]) selects which sample is being written for a given unit interval. There are 24 samples, numbered from 0 to 23. SAMPLE[4:0] can thus have any value from 00H to 17H. The values from 18H to 1FH are undefined.

See the Operation section for more details on setting up waveform templates.

Register 0F3H, 1F3H, 2F3H, 3F3H: XLPG Pulse Waveform Storage Data

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	W	WDAT[6]	X
Bit 5	W	WDAT[5]	X
Bit 4	W	WDAT[4]	X
Bit 3	W	WDAT[3]	X
Bit 2	W	WDAT[2]	X
Bit 1	W	WDAT[1]	X
Bit 0	W	WDAT[0]	X

WDAT[6:0]:

This register allows software to program the contents of any one of the 120 internal waveform template registers, addressed by the UI[2:0] and SAMPLE[4:0] bits in the Pulse Waveform Storage Write Address register. When accessing the internal waveform storage registers, the address of the desired register must first be written to the Indirect Address register (XLPG register 2). Then, by writing the Indirect Data register, the microprocessor can write to the data to the selected write address.

The value written to the internal pulse waveform storage registers is contained in the signed WDAT[6:0] bits. A signed representation is used (by opposition to a two's complement representation) to make the programming easier. WDAT[6] is the sign bit, WDAT[5] is the most significant data bit and WDAT[0] is the least significant data bit. The data value thus can range from -62 to +63 (-63 is not a valid value due to subsequent conversion into a two's complement representation).

See the Operation section for more details on setting up custom waveform templates.

Register 0F4H, 1F4H, 2F4H, 3F4H: XLPG Analog Test Positive Control

Bit	Type	Function	Default
Bit 7	R/W	TPC[7]	0
Bit 6	R/W	TPC[6]	0
Bit 5	R/W	TPC[5]	0
Bit 4	R/W	TPC[4]	0
Bit 3	R/W	TPC[3]	0
Bit 2	R/W	TPC[2]	0
Bit 1	R/W	TPC[1]	0
Bit 0		Unused	X

TPC[7:1]:

This register controls the pDAC absolute current for software override of the fuses of the analog transmit line interface unit. TPC[6:1] adjust the offset in steps of 0.78125%, TPC[7] controls the direction (0 is positive, 1 is negative). When the PACT bit of XLPG Fuse Data Select register is logic 0, TPC[7:1] override the fuse.

When the FDSB bit of the XLPG Fuse Data Select register is logic 1, a write to this register places the contents of the microprocessor data bus into TPC[7:1]. When the FDSB bit of the XLPG Fuse Data Select register is logic 0, a write to this register places the value burned into the pDAC fuses of the transmit line interface unit into TPC[7:1], and the the contents of the microprocessor data bus are ignored.

Register 0F5H, 1F5H, 2F5H, 3F5H: XLPG Analog Test Negative Control

Bit	Type	Function	Default
Bit 7	R/W	TNC[7]	0
Bit 6	R/W	TNC[6]	0
Bit 5	R/W	TNC[5]	0
Bit 4	R/W	TNC[4]	0
Bit 3	R/W	TNC[3]	0
Bit 2	R/W	TNC[2]	0
Bit 1	R/W	TNC[1]	0
Bit 0		Unused	X

TNC[7:1]:

This register controls the nDAC absolute current for software override of the fuses of the analog transmit line interface unit. TNC[6:1] adjust the offset in steps of 0.78125%, TNC[7] controls the direction (0 is positive, 1 is negative). When the NACT bit of XLPG Fuse Data Select register is logic 0, TNC[7:1] override the fuse values.

When the FDSB bit of the XLPG Fuse Data Select register is logic 1, a write to this register places the contents of the microprocessor data bus into TNC[7:1]. When the FDSB bit of the XLPG Fuse Data Select register is logic 0, a write to this register places the value burned into the nDAC fuses of the transmit line interface unit into TNC[7:1], and the the contents of the microprocessor data bus are ignored.

Register 0F6H, 1F6H, 2F6H, 3F6H: XLPG Fuse Data Select

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	NACT	0
Bit 1	R/W	PACT	0
Bit 0	R/W	FDSB	0

FDSB:

This register bit selects between microprocessor data (FDSB is logic 1) or the value burned into the fuses of the transmit line interface unit (FDSB is logic 0) as the inputs to the XLPG Analog Test Negative Control register and the XLPG Analog Test Positive Control register.

After each reset write the fuse data into the XLPG Analog Test Negative Control register and the XLPG Analog Test Positive Control register, by following the steps below (where X represents a don't care condition).

(1) Write "XXXXX110" to the XLPG Fuse Data Select register. (This programs FDSB to logic 0, selecting the value burned into the fuses. This also programs NACT and PACT to logic 1, activating the nDAC and pDAC fuses respectively.)
(2) Write "XXXXXXXX" to the XLPG Analog Test Negative Control register. This copies the nDAC fuse value.
(3) Write "XXXXXXXX" to the XLPG Analog Test Positive control register. This copies the pDAC fuse value.
(4) Write "XXXXX000" to the XLPG Fuse Data Select register. (This programs NACT and PACT to logic 0, deactivating the fuses to lower the likelihood of fuse re-growth.)

Register 0F8H, 1F8H, 2F8H, 3F8H: RLPS Configuration and Status

Bit	Type	Function	Default
Bit 7	R	ALOSI	X
Bit 6	R	ALOSV	X
Bit 5	R/W	ALOSE	0
Bit 4	R/W	SQUELCHE	0
Bit 3	R/W	IDDQ_EN	0
Bit 2	R/W	DB_VALID	X
Bit 1		Unused	X
Bit 0	R/W	Reserved	1

Reserved:

The Reserved bit must be logic 1 for correct operation.

DB_VALID:

The DB_VALID bit indicates if the adaptive equalizer has stabilized. This bit is set if the CABLELOSS signal has not changed by more than 2dB (or +/-8 steps in the RAM table) in more than a selectable count of sampling periods.

IDDQ_EN:

The IDDQ enable bit (IDDQ_EN) is used to configure the analog receiver for IDDQ tests. When IDDQ_EN is a logic 1, or the IDDQEN bit in the Master Test register (00BH) is a logic 1, the digital outputs of the analog receiver are pulled to ground.

SQUELCHE:

The output data squelch enable (SQUELCHE) allows control of data squelching in response to an analog LOS of signal condition. When SQUELCHE is set to logic 1, the recovered data are forced to all-zeros if the ALOS register bit is asserted. When SQUELCHE is set to logic 0, squelching is disabled.

ALOSE:

The loss of signal interrupt enable bit (ALOSE) enables the generation of device level interrupt on a change of Loss of Signal status. When ALOSE is a logic 1, an interrupt is generated by asserting INTB low when there is a change of the ALOSV status. When ALOSE is set to logic 0, interrupts are disabled.

ALOSV:

The loss of signal value bit (ALOSV) indicates the loss of signal alarm state. This status bit is available only in short haul mode of operation (LONGE set to logic 0), and it is otherwise forced to logic 0.

ALOSI:

The loss of signal interrupt bit (ALOSI) is a logic 1 whenever the Loss of Signal indicator state (ALOSV) changes. This bit is cleared when this register is read.

Register 0F9H, 1F9H, 2F9H, 3F9H: RLPS ALOS Detection/Clearance Threshold

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	CLR_THR[2]	0
Bit 5	R/W	CLR_THR[1]	0
Bit 4	R/W	CLR_THR[0]	0
Bit 3		Unused	X
Bit 2	R/W	DET_THR[2]	0
Bit 1	R/W	DET_THR[1]	0
Bit 0	R/W	DET_THR[0]	0

Table 56 - ALOS Detection/Clearance Thresholds

THR	Signal level (dB)	Applicable Standard	Detection/ Clearance
000	9	G.775(E1)	Clearance
001	14.5		
010	20	I.431 (E1) ETSI 300 233	Detection and Clearance
011	22		
100	25		
101	30	I.431 (T1)	Detection and Clearance
110	31		
111	35	G.775 (E1)	Detection

DET_THR[2:0]:

DET_THR[2:0] references one of the threshold settings in Table 56 as the ALOS detection criteria. If the incoming signal level is less than or equal to that threshold for N consecutive pulse period, (where N = 16 * the value stored in the RLPS ALOS Detection Period Register) ALOS is declared and interrupt set. The DET_THR[2:0] bits must be programmed to the same value as the CLR_THR[2:0] bits.

CLR_THR[2:0]:

CLR_THR[2:0] references one of the threshold settings listed in Table 56 as the ALOS clearance criteria. ALOS is cleared when the incoming signal level is greater than or equal to dB below nominal for N consecutive pulse intervals, where N = 16 * CLR_PER stored in the RLPS ALOS Clearance Period Register. The CLR_THR[2:0] bits must be programmed to the same value as the DET_THR[2:0] bits.

Register 0FAH, 1FAH, 2FAH, 3FAH: RLPS ALOS Detection Period

Bit	Type	Function	Default
Bit 7	R/W	DET_PER[7]	0
Bit 6	R/W	DET_PER[6]	0
Bit 5	R/W	DET_PER[5]	0
Bit 4	R/W	DET_PER[4]	0
Bit 3	R/W	DET_PER[3]	0
Bit 2	R/W	DET_PER[2]	0
Bit 1	R/W	DET_PER[1]	0
Bit 0	R/W	DET_PER[0]	1

DET_PER[7:0]:

This register specifies the time duration that the incoming signal level has to remain below the detection threshold in order for the ALOS to be issued. This duration is equal to DET_PER * 16 number of pulse intervals, the resulting range is from 16 to 4080 and thus compliant with all the presently available E1/T1 ALOS detection standards/ recommendations.

Register 0FBH, 1FBH, 2FBH, 3FBH: RLPS ALOS Clearance Period

Bit	Type	Function	Default
Bit 7	R/W	CLR_PER[7]	0
Bit 6	R/W	CLR_PER[6]	0
Bit 5	R/W	CLR_PER[5]	0
Bit 4	R/W	CLR_PER[4]	0
Bit 3	R/W	CLR_PER[3]	0
Bit 2	R/W	CLR_PER[2]	0
Bit 1	R/W	CLR_PER[1]	0
Bit 0	R/W	CLR_PER[0]	1

CLR_PER[7:0]:

This register specifies the time duration that the incoming signal level has to remain above the clearance threshold in order for the ALOS to be cleared. This duration is equal to CLR_PER * 16 number of pulse intervals resulting in a range from 16 to 4080 and thus compliant with all the presently available E1/T1 ALOS clearance standards/ recommendations.

Register 0FCH, 1FCH, 2FCH, 3FCH: RLPS Equalization Indirect Address

Bit	Type	Function	Default
Bit 7	R/W	EQ_ADDR[7]	0
Bit 6	R/W	EQ_ADDR[6]	0
Bit 5	R/W	EQ_ADDR[5]	0
Bit 4	R/W	EQ_ADDR[4]	0
Bit 3	R/W	EQ_ADDR[3]	0
Bit 2	R/W	EQ_ADDR[2]	0
Bit 1	R/W	EQ_ADDR[1]	0
Bit 0	R/W	EQ_ADDR[0]	0

EQ_ADDR [7:0]:

Writing to this register initiates an internal uP access request cycle to the RAM. Depending on the setting of the RWB bit inside register 0FDH, a read or a write will be performed.
During a write cycle, the indirect data bits located in registers 0D8H to 0DBH is written into the RAM. For a read request, the content of the addressed RAM location is written into registers 0D8H to 0DBH. This register should be the last register to be written for a uP access.
A waiting period of one line rate cycle before another access is required.

Register 0FDH, 1FDH, 2FDH, 3FDH: RLPS Equalization Read/WriteB Select

Bit	Type	Function	Default
Bit 7	R/W	RWB	1
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

RWB:

This bit selects the operation to be performed on the RAM: when RWB is '1', a read from the equalization RAM is requested; when RWB is set to '0', a write to the RAM is desired.

Register 0FEH, 1FEH, 2FEH, 3FEH: RLPS Equalizer Loop Status and Control

Bit	Type	Function	Default
Bit 7	R/W	LOCATION[7]	0
Bit 6	R/W	LOCATION[6]	0
Bit 5	R/W	LOCATION[5]	0
Bit 4	R/W	LOCATION[4]	0
Bit 3	R/W	LOCATION[3]	0
Bit 2	R/W	LOCATION[2]	0
Bit 1	R/W	LOCATION[1]	0
Bit 0	R/W	LOCATION[0]	0

LOCATION[7:0]:

Writing to this register overwrites a counter which serves as the read address to the equalization RAM. Reading this register returns the current value of the counter

Register 0FFH, 1FFH, 2FFH, 3FFH: RLPS Equalizer Configuration

Bit	Type	Function	Default
Bit 7	R/W	VALID_PER[1]	0
Bit 6	R/W	VALID_PER[0]	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	Reserved	0
Bit 2	R/W	EQ_FREQ2]	0
Bit 1	R/W	EQ_FREQ[1]	1
Bit 0	R/W	EQ_FREQ[0]	1

EQ_FREQ[2:0]:

The EQ_FREQ[2:0] field selects the frequency of the EQ feedback loop as indicated by Table 57.

Table 57 - Equalization Feedback Frequencies

EQ_FREQ[2:0]	EQ Feedback Frequency	
	T1 mode	E1 mode
000	24.125 kHz	32.000 kHz
001	12.063 kHz	16.000 kHz
010	8.0417 kHz	10.667 kHz
011	6.0313 kHz	8.0000 kHz
100	4.8250 kHz	6.40 kHz
101	4.0208 kHz	5.333 kHz
110	3.4464 kHz	4.5714 kHz
111	3.0156 kHz	4.0 kHz

Reserved:

The Reserved bit must be programmed to logic 1 for correct operation. Note that this bit defaults to logic 0.

VALID_PER[1:0]:

The VALID_PER[1:0] bits select the length of time that the dB loss counter must be stable before DB_VALID is asserted. The duration is measured in number of periods of the EQ feedback loop (specified by the EQ_FREQ bits) as indicated by Table 58.

Table 58 - Valid Period

VALID_PER	Number of periods
00	32
01	64
10	128
11	256

TEST FEATURES DESCRIPTION

The COMET-Quad contains test features for both production testing and board testing.

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the COMET-Quad. Test mode registers (as opposed to normal mode registers) are selected when TRS (A[13]) is high.

Test mode registers may also be used for board testing. When all of the constituent Telecom System Blocks within the COMET-Quad are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

Test Mode Register Memory Map

Address	Register

Notes on Register Bits:

1) Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic one or a logic zero; hence unused bits should be masked off by software when read.

2) Writeable register bits are not initialized upon reset unless otherwise noted.

1.36 JTAG Test Port

The COMET-Quad JTAG Test Access Port (TAP) allows access to the TAP controller and the 4 TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 59: - Instruction Register

Table 60: - Identification Register

Table 61: - Boundary Scan Register

OPERATION

1.37 Servicing Interrupts

The COMET-Quad will assert INTB to logic 0 when a condition that is configured to produce an interrupt occurs. To find which condition caused this interrupt to occur, the procedure outlined below should be followed:

1. Read the bits of the COMET-Quad Master Interrupt Source register (0BCH) to identify which COMET quadrants generated the interrupt. For example, a logic one read in bit 2 of the COMET-Quad Master Interrupt Source register indicates that COMET quadrant #2 produced the interrupt.

2. Read the bits of the second level Interrupt Source registers to identify the block generating the interrupt.
   The Interrupt Source registers for COMET quadrant #1 are 007H-009H.
   The Interrupt Source registers for COMET quadrant #2 are 107H-109H.
   The Interrupt Source registers for COMET quadrant #3 are 207H-209H.
   The Interrupt Source registers for COMET quadrant #4 are 307H-309H.

3. Read the third level Interrupt Source registers to identify the interrupt source.

4. Service the interrupt.

5. If the INTB pin is still logic 0, then there are still interrupts to be serviced. Otherwise, all interrupts have been serviced. Wait for the next assertion of INTB

1.38 Using the Performance Monitoring Features

The PMON blocks are provided for performance monitoring purposes. The PMON blocks within each T1/E1 Framer slice are used to monitor T1 or E1 performance primitives. The T1/E1 PMON event counters are of sufficient length so that the probability of counter saturation over a one second interval is very small (less than 0.001%).

An accumulation interval is initiated by writing to one of the PMON event counter register addresses or by writing to the Revision/Chip ID/Quadrant PMON Update register. After initiating an accumulation interval, 3.5 recovered clock periods must be allowed to elapse to permit the PMON counter values to be properly transferred before the PMON registers may be read.

The odds of any one of the T1/E1 counters saturating during a one second sampling interval go up as the bit error rate (BER) increases. At some point, the probability of counter saturation

reaches 50%. This point varies, depending upon the framing format and the type of event being counted. The BER at which the probability of counter saturation reaches 50% is shown for various counters in Table 62 for E1 mode, and in Table 63 for T1 mode.

Table 62: - PMON Counter Saturation Limits (E1 mode)

Counter	BER
FER	4.0×10^{-3}
CRCE	cannot saturate
FEBE	cannot saturate

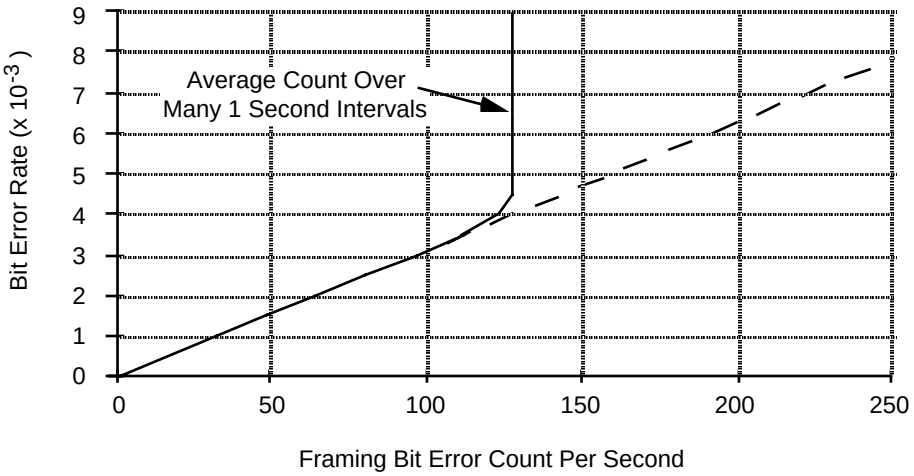
Table 63: - PMON Counter Saturation Limits (T1 mode)

Counter	Format	BER
FER	SF	1.6×10^{-3}
	ESF	6.4×10^{-2}
CRCE	SF	1.28×10^{-1}
	ESF	cannot saturate

Below these 50% points, the relationship between the BER and the counter event count (averaged over many one second samples) is essentially linear. Above the 50% point, the relationship between BER and the average counter event count is highly non-linear due to the likelihood of counter saturation. The following figures show this relationship for various counters and framing formats. These graphs can be used to determine the BER, given the average event count. In general, if the BER is above 10^{-3}, the average counter event count cannot be used to determine the BER without considering the statistical effect of occasional counter saturation.

Figure 26 illustrates the expected count values for a range of Bit Error Ratios in E1 mode.

Figure 26: - FER Count vs. BER (E1 mode)



Since the maximum number of CRC sub-multiframes that can occur in one second is 1000, the 10-bit FEBE and CRCE counters cannot saturate in one second. Despite this, there is not a linear relationship between BER and CRC-4 block errors due to the nature of the CRC-4 calculation. At BERs below 10^{-4}, there tends to be no more than one bit error per sub-multiframe, so the number of CRC-4 errors is generally equal to the number of bit errors, which is directly related to the BER. However, at BERs above 10^{-4}, each CRC-4 error is often due to more than one bit error. Thus, the relationship between BER and CRCE count becomes non-linear above a 10^{-4} BER. This must be taken into account when using CRC-4 counts to determine the BER. Since FEBEs are indications of CRCEs at the far end, and are accumulated identically to CRCEs, the same explanation holds for the FEBE event counter.

The bit error rate for E1 can be calculated from the one-second PMON CRCE count by the following equation:

Bit Error Rate = 1 - 10 $^{\left(\frac{\log\left(1-\frac{8}{8000}CRCE\right)}{8*256}\right)}$

Figure 27: - CRCE Count vs. BER (E1 mode)

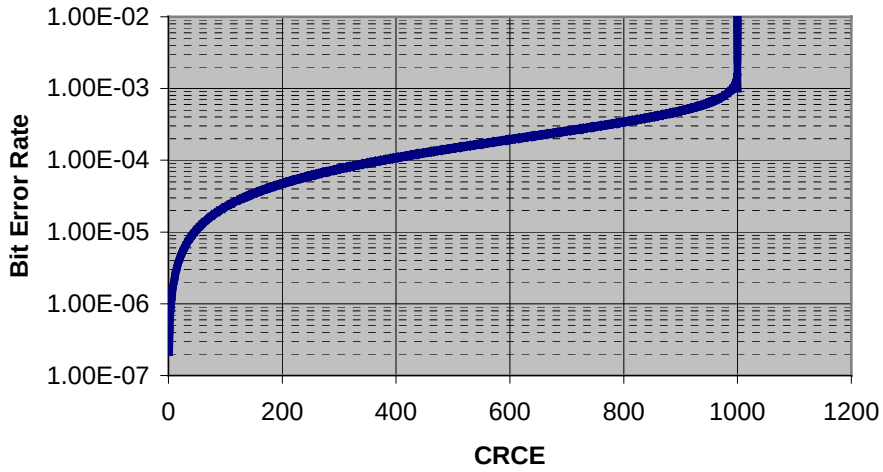
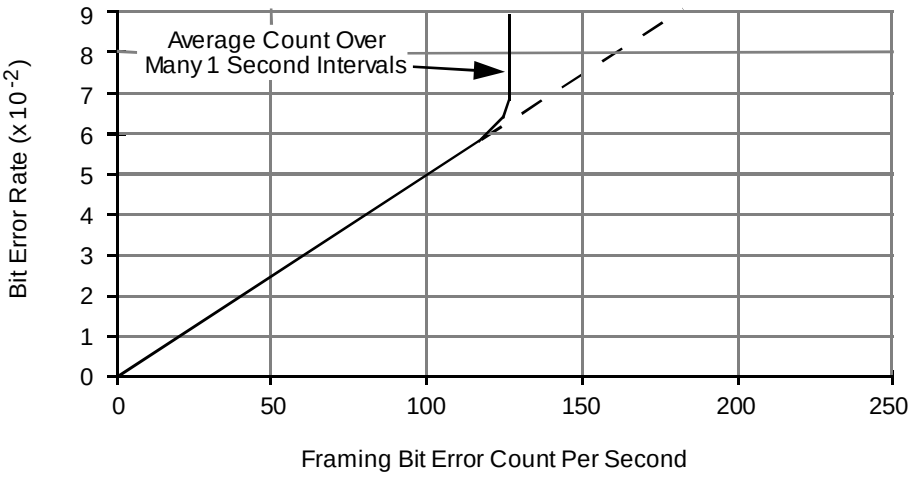


Figure 28 illustrates the expected count values for a range of Bit Error Ratios in T1 mode.

Figure 28: - FER Count vs. BER (T1 ESF mode)

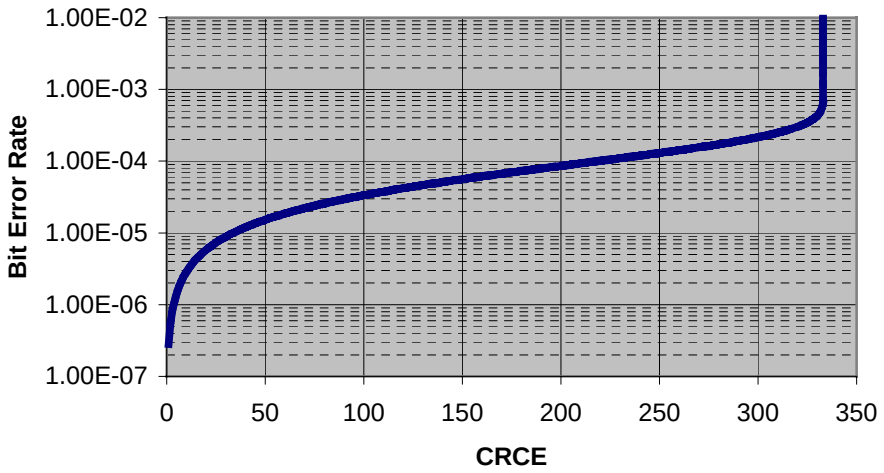


Since the maximum number of ESF superframes that can occur in one second is 333, the 9-bit BEE counter cannot saturate in one second in ESF framing format. Despite this, there is not a linear relationship between BER and BEE count, due to the nature of the CRC-6 calculation. At BERs below 10^{-4}, there tends to be no more than one bit error per superframe, so the number of CRC-6 errors is generally equal to the number of bit errors, which is directly related to the BER. However, at BERs above 10^{-4}, each CRC-6 error is often due to more than one bit error. Thus, the relationship between BER and BEE count becomes non-linear above a 10^{-4} BER. This must be taken into account when using ESF CRC-6 counts to determine the BER.

The bit error rate for T1 ESF can be calculated from the one-second PMON CRCE count by the following equation:

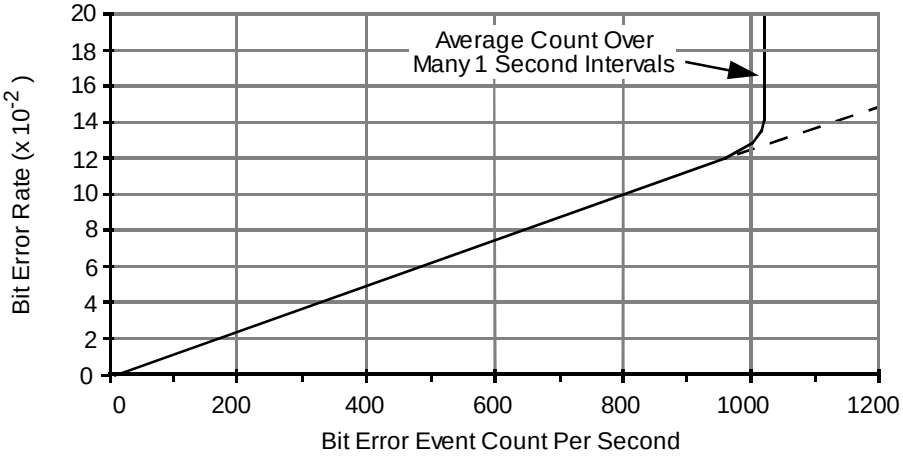
Bit Error Rate = 1 - 10 $^{\left(\frac{\log\left(1-\frac{24}{8000}BEE\right)}{24*193}\right)}$

Figure 29: - CRCE Count vs. BER (T1 ESF mode)



For T1 SF format, the CRCE and FER counts are identical, but the FER counter is smaller and should be ignored.

Figure 30: - CRCE Count vs. BER (T1 SF mode)



1.39 Using the Internal FDL Transmitter

It is important to note that access rate to the TDPR registers is limited by the rate of the internal high-speed system clock which is either the DS1 or E1 clock. Consecutive accesses to the TDPR Configuration, TDPR Interrupt Status/UDR Clear, and TDPR Transmit Data register should be accessed (with respect to WRB rising edge and RDB falling edge) at a rate no faster than 1/8 that of the selected TDPR high-speed system clock. This time is used by the high-speed system clock to sample the event, write the FIFO, and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the line clock) must be considered when determining the procedure used to read and write the TDPR registers.

Upon reset of the COMET-Quad, the TDPR should be disabled by setting the EN bit in the TDPR Configuration Register to logic 0 (default value). An HDLC all-ones idle signal will be sent while in this state. The TDPR is enabled by setting the EN bit to logic 1. The FIFOCLR bit should be set and then cleared to initialize the TDPR FIFO. The TDPR is now ready to transmit.

To initialize the TDPR, the TDPR Configuration Register must be properly set. If FCS generation is desired, the CRC bit should be set to logic 1. If the block is to be used in interrupt driven mode, then interrupts should be enabled by setting the FULLE, OVRE, UDRE, and LFILLE bits in the TDPR Interrupt Enable register to logic 1. The TDPR operating parameters in the TDPR Upper Transmit Threshold and TDPR Lower Interrupt Threshold registers should be set to the desired values. The TDPR Upper Transmit Threshold sets the value at which the TDPR automatically begins the transmission of HDLC packets, even if no complete packets are in the FIFO. Transmission will continue until the current packet is transmitted and the number of bytes in the TDPR FIFO falls to, or below, this threshold level. The TDPR will always transmit all complete HDLC packets (packets with EOM attached) in its FIFO. Finally, the TDPR can be enabled by setting the EN bit to logic 1. If no message is sent after the EN bit is set to logic 1, continuous flags will be sent.

The TDPR can be used in a polled or interrupt driven mode for the transfer of data. In the polled mode the processor controlling the TDPR must periodically read the TDPR Interrupt Status register to determine when to write to the TDPR Transmit Data register. In the interrupt driven mode, the processor controlling the TDPR uses the INTB output, the one of the COMET-Quad Master Interrupt Source registers, and the COMET-Quad TDPR Interrupt Status registers to identify TDPR interrupts which determine when writes can or must be done to the TDPR Transmit Data register.

Interrupt Driven Mode:

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 1 so an interrupt on INTB is generated upon detection of a FIFO full state, a

FIFO depth below the lower limit threshold, a FIFO overrun, or a FIFO underrun. The following procedure should be followed to transmit HDLC packets:

1. Wait for a complete packet to be transmitted. Once data is available to be transmitted, then go to step 2.
2. Write the data byte to the TDPR Transmit Data register.
3. If all bytes of the packet have been written to the Transmit Data register, then set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.
4. If there are more bytes in the packet to be sent, then go to step 2.

While performing steps 1 to 4, the processor should monitor for interrupts generated by the TDPR. When an interrupt is detected, the TDPR Interrupt Routine detailed in the following text should be followed immediately.

The TDPR will force transmission of the packet information when the FIFO depth exceeds the threshold programmed with the UTHR[6:0] bits in the TDPR Upper Transmit Threshold register. Unless an error condition occurs, transmission will not stop until the last byte of all complete packets is transmitted and the FIFO depth is at or below the threshold limit. The user should watch the FULLI and LFILLI interrupts to prevent overruns and underruns.

TDPR Interrupt Routine:

Upon assertion of INTB, the source of the interrupt must first be identified by reading the COMET-Quad Master Interrupt Source register (0020H) followed by reading one of the second level master interrupt source registers T1E1INT1, T1E1INT2, T1E1INT3, T1E1INT4. Once the source of the interrupt has been identified as the TDPR in use, then the following procedure should be carried out:

1. Read the TDPR Interrupt Status register.
2. If UDRI=1, then the FIFO has underrun and the last packet transmitted has been corrupted and needs to be retransmitted. When the UDRI bit transitions to logic 1, one Abort sequence and continuous flags will be transmitted. The TDPR FIFO is held in reset state. To re-enable the TDPR FIFO and to clear the underrun, the TDPR Interrupt Status/UDR Clear register should be written with any value.
3. If OVRI=1, then the FIFO has overflowed. The packet of which the last byte written into the FIFO belongs to, has been corrupted and must be retransmitted. Other packets in the FIFO are not affected. Either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

   If the FIFO overflows on the packet currently being transmitted (packet is greater than 128 bytes long), OVRI is set, an Abort signal is scheduled to be transmitted, the FIFO is emptied, and then flags are continuously sent until there is data to be transmitted. The FIFO is held in

reset until a write to the TDPR Transmit Data register occurs. This write contains the first byte of the next packet to be transmitted.

4. If FULLI=1 and FULL=1, then the TDPR FIFO is full and no further bytes can be written. When in this state, either a timer can be used to determine when sufficient bytes are available in the FIFO or the user can wait until the LFILLI interrupt is set, indicating that the FIFO depth is at the lower threshold limit.

   If FULLI=1 and FULL=0, then the TDPR FIFO had reached the FULL state earlier, but has since emptied out some of its data bytes and now has space available in its FIFO for more data.

5. If LFILLI=1 and BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. If there is more data to transmit, then it should be written to the TDPR Transmit Data register before an underrun occurs. If there is no more data to transmit, then an EOM should be set at the end of the last packet byte. Flags will then be transmitted once the last packet has been transmitted.

If LFILLI=1 and BLFILL=0, then the TDPR FIFO had fallen below the lower-threshold state earlier, but has since been refilled to a level above the lower-threshold level.

Polling Mode:

The TDPR automatically transmits a packet once it is completely written into the TDPR FIFO. The TDPR also begins transmission of bytes once the FIFO level exceeds the programmable Upper Transmit Threshold. The CRC bit can be set to logic 1 so that the FCS is generated and inserted at the end of a packet. The TDPR Lower Interrupt Threshold should be set to such a value that sufficient warning of an underrun is given. The FULLE, LFILLE, OVRE, and UDRE bits are all set to logic 0 since packet transmission is set to work with a periodic polling procedure. The following procedure should be followed to transmit HDLC packets:

1. Wait until data is available to be transmitted, then go to step 2.

2. Read the TDPR Interrupt Status register.

3. If FULL=1, then the TDPR FIFO is full and no further bytes can be written. Continue polling the TDPR Interrupt Status register until either FULL=0 or BLFILL=1. Then, go to either step 4 or 5 depending on implementation preference.

4. If BLFILL=1, then the TDPR FIFO depth is below its lower threshold limit. Write the data into the TDPR Transmit Data register. Go to step 6.

5. If FULL=0, then the TDPR FIFO has room for at least 1 more byte to be written. Write the data into the TDPR Transmit Data register. Go to step 6.

6. If more data bytes are to be transmitted in the packet, then go to step 2.

If all bytes in the packet have been sent, then set the EOM bit in the TDPR Configuration register to logic 1. Go to step 1.

1.40 Using the Internal Data Link Receiver

It is important to note that the access rate to the RDLC registers is limited by the rate of the internal high-speed system clock which is either the DS1 or E1 system clock. Consecutive accesses to the RDLC Status and RDLC Data registers should be accessed at a rate no faster than 1/10 that of the selected RDLC high-speed system clock. This time is used by the high-speed system clock to sample the event and update the FIFO status. Instantaneous variations in the high-speed reference clock frequencies (e.g. jitter in the receive line clock) must be considered when determining the procedure used to read RDLC registers.

On power up of the system, the RDLC should be disabled by setting the EN bit in the Configuration Register to logic 0 (default state). The RDLC Interrupt Control register should then be initialized to enable the INTB output and to select the FIFO buffer fill level at which an interrupt will be generated. If the INTE bit is not set to logic 1, the RDLC Status register must be continuously polled to check the interrupt status (INTR) bit.

After the RDLC Interrupt Control register has been written, the RDLC can be enabled at any time by setting the EN bit in the RDLC Configuration register to logic 1. When the RDLC is enabled, it will assume the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated, and a dummy byte will be written into the FIFO buffer. This is done to provide alignment of link up status with the data read from the FIFO. When an abort character is received, another dummy byte and link down status is written into the FIFO. This is done to provide alignment of link down status with the data read from the FIFO. It is up to the controlling processor to check the COLS bit in the RDLC Status register for a change in the link status. If the COLS bit is set to logic 1, the FIFO must be emptied to determine the current link status. The first flag and abort status encoded in the PBS bits is used to set and clear a Link Active software flag.

When the last byte of a properly terminated packet is received, an interrupt is generated. While the RDLC Status register is being read the PKIN bit will be logic 1. This can be a signal to the external processor to empty the bytes remaining in the FIFO or to just increment a number-of-packets-received count and wait for the FIFO to fill to a programmable level. Once the RDLC Status register is read, the PKIN bit is cleared to logic 0 . If the RDLC Status register is read immediately after the last packet byte is read from the FIFO, the PBS[2] bit will be logic 1 and the CRC and non-integer byte status can be checked by reading the PBS[1:0] bits.

When the FIFO fill level is exceeded, an interrupt is generated. The FIFO must be emptied to remove this source of interrupt.

The RDLC can be used in a polled or interrupt driven mode for the transfer of frame data. In the polled mode, the processor controlling the RDLC must periodically read the RDLC Status register to determine when to read the RDLC Data register. In the interrupt driven mode, the processor controlling the RDLC uses the COMET-Quad INTB output and the COMET-Quad Master Interrupt Source registers to determine when to read the RDLC Data register.

In the case of interrupt driven data transfer from the RDLC to the processor, the INTB output of the COMET-Quad is connected to the interrupt input of the processor. The processor interrupt

service routine verifies what block generated the interrupt by reading the COMET-Quad Master Interrupt Source register followed by one of the second level master interrupt source registers to identify one of the 29 HDLC receivers as the interrupt source. Once it has identified that the RDLC has generated the interrupt, it processes the data in the following order:

1. Read the RDLC Status register. The INTR bit should be logic 1.
2. If OVR = 1, then discard the last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.
3. If COLS = 1, then set the EMPTY FIFO software flag.
4. If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.
5. Read the RDLC Data register.
6. Read the RDLC Status register.
7. If OVR = 1, then discard last frame and go to step 1. Overrun causes a reset of FIFO pointers. Any packets that may have been in the FIFO are lost.
8. If COLS = 1, then set the EMPTY FIFO software flag.
9. If PKIN = 1, increment the PACKET COUNT. If the FIFO is desired to be emptied as soon as a complete packet is received, set the EMPTY FIFO software flag. If the EMPTY FIFO software flag is not set, FIFO emptying will delayed until the FIFO fill level is exceeded.
10. Start the processing of FIFO data. Use the PBS[2:0] packet byte status bits to decide what is to be done with the FIFO data.

    If PBS[2:0] = 001, discard data byte read in step 5 and set the LINK ACTIVE software flag.

    If PBS[2:0] = 010, discard the data byte read in step 5 and clear the LINK ACTIVE software flag.

    If PBS[2:0] = 1XX, store the last byte of the packet, decrement the PACKET COUNT, and check the PBS[1:0] bits for CRC or NVB errors before deciding whether or not to keep the packet.

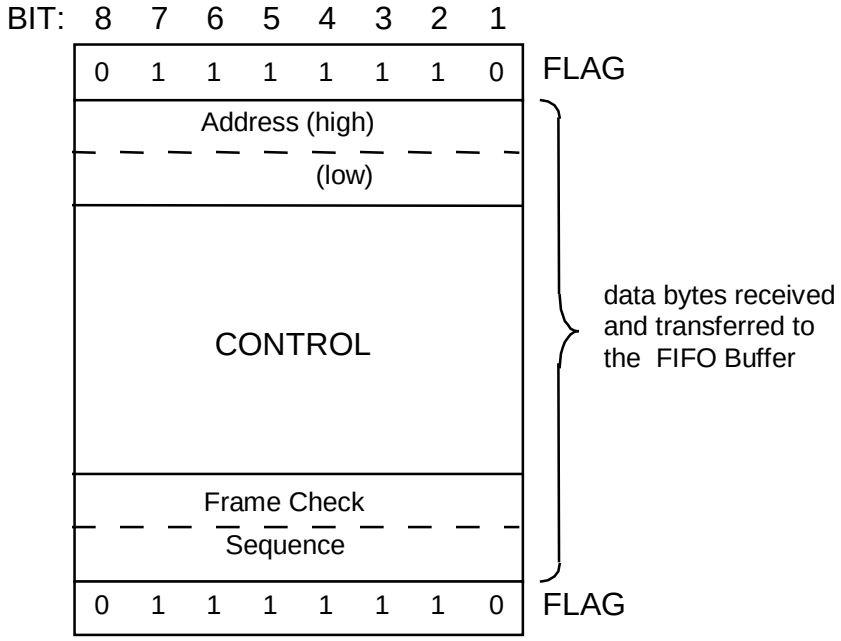
    If PBS[2:0] = 000, store the packet data.

11. If FE = 0 and INTR = 1 or FE = 0 and EMPTY FIFO = 1, go to step 5 else clear the EMPTY FIFO software flag and leave this interrupt service routine to wait for the next interrupt.

    The link state is typically a local software variable. The link state is inactive if the RDLC is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RDLC is receiving flags or data.

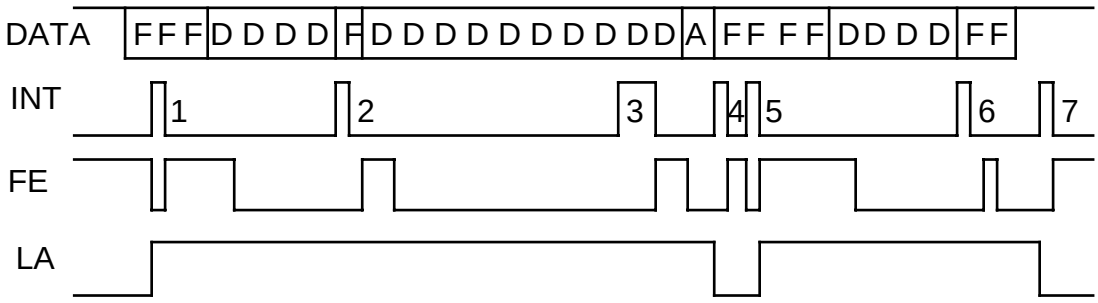
If the RDLC data transfer is operating in the polled mode, processor operation is exactly as shown above for the interrupt driven mode, except that the entry to the service routine is from a timer, rather than an interrupt.

Figure 31: - Typical Data Frame



Bit 1 is the first serial bit to be received. When enabled, the primary, secondary and universal addresses are compared with the high order packet address to determine a match.

Figure 32: - Example Multi-Packet Operational Sequence



F - flag sequence (01111110)
A - abort sequence (01111111)
D - packet data bytes

INT - active high interrupt output
FE - internal FIFO empty status
LA - state of the LINK ACTIVE software flag

Figure 32 shows the timing of interrupts, the state of the FIFO, and the state of the Data Link relative the input data sequence. The cause of each interrupt and the processing required at each point is described in the following paragraphs. The actual interrupt signal, INTB, is active low and will be the inverse of the INT signal shown in figure 16. Also in this example, the programmable fill level set point is set at 8 bytes by writing this value into the INTC[6:0] bits of the RDLC Interrupt Control register.

At points 1 and 5 the first flag after all ones or abort is detected. A dummy byte is written in the FIFO, FE goes low, and an interrupt goes active. When the interrupt is detected by the processor it reads the dummy byte, the FIFO becomes empty, and the interrupt is removed. The LINK ACTIVE (LA) software flag is set to logic 1.

At points 2 and 6 the last byte of a packet is detected and interrupt goes high. When the interrupt is detected by the processor, it reads the data and status registers until the FIFO becomes empty. The interrupt is removed as soon as the RDLC Status register is read, since the FIFO fill level of 8 bytes has not been exceeded. It is possible to store many packets in the FIFO and empty the FIFO when the FIFO fill level is exceeded. In either case the processor should use this interrupt to count the number of packets written into the FIFO. The packet count or a software time-out can be used as a signal to empty the FIFO.

At point 3 the FIFO fill level of 8 bytes is exceeded and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed.

At points 4 or 7 an abort character is detected, a dummy byte is written into the FIFO, and interrupt goes high. When the interrupt is detected by the processor it must read the data and status registers until the FIFO becomes empty and the interrupt is removed. The LINK ACTIVE software flag is cleared.

1.41 T1 Automatic Performance Report Format

Table 64: - Performance Report Message Structure and Contents

Octet No.	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
1	FLAG							
2	SAPI						C/R	EA
3	TEI							EA
4	CONTROL							
5	G3	LV	G4	U1	U2	G5	SL	G6
6	FE	SE	LB	G1	R	G2	Nm	NI
7	G3	LV	G4	U1	U2	G5	SL	G6
8	FE	SE	LB	G1	R	G2	Nm	NI
9	G3	LV	G4	U1	U2	G5	SL	G6
10	FE	SE	LB	G1	R	G2	Nm	NI

11	G3	LV	G4	U1	U2	G5	SL	G6
12	FE	SE	LB	G1	R	G2	Nm	NI
13	FCS							
14	FCS							
15	FLAG							

Notes:

1. The order of transmission of the bits is LSB (Bit 1) to MSB (Bit 8).

Table 65: - Performance Report Message Structure Notes

Octet No.	Octet Contents	Interpretation
1	01111110	Opening LAPD Flag
2	00111000 00111010	From CI: SAPI=14, C/R=0, EA=0 From carrier: SAPI=14,C/R=1,EA=0
3	00000001	TEI=0,EA=1
4	00000011	Unacknowledged Frame
5,6	Variable	Data for latest second (T')
7,8	Variable	Data for Previous Second(T'-1)
9,10	Variable	Data for earlier Second(T'-2)
11,12	Variable	Data for earlier Second(T'-3)
13,14	Variable	CRC16 Frame Check Sequence
15	01111110	Closing LAPD flag

Table 66: - Performance Report Message Contents

Bit Value	Interpretation
G1=1	CRC ERROR EVENT =1
G2=1	1<CRC ERROR EVENT ≤5
G3=1	5<CRC ERROR EVENT ≤10
G4=1	10<CRC ERROR EVENT ≤100
G5=1	100<CRC ERROR EVENT ≤319
G6=1	CRC ERROR EVENT ≤ 320

SE=1	Severely Errored Framing Event ≥ 1(FE shall =0)
FE=1	Frame Synchronization Bit Error Event ≥1 (SE shall=0)
LV=1	Line code violation event ≥ 1
SL=1	Slip Event ≥ 1
LB=1	Payload Loopback Activated
U1,U2=0	Under Study For Synchronization.
R=0	Reserved (Default Value =0)
NmNI=00,01,10,11	One second Report Modulo 4 Counter

1.42 Using the Per-Channel Serial Controllers

1.42.1 Initialization

Before the TPSC (RPSC) block can be used, a proper initialization of the internal registers must be performed to eliminate erroneous control data from being produced on the block outputs. The output control streams should be disabled by setting the PCCE bit in the TPSC (RPSC) Configuration Register to logic 0. Then, all 96 locations of the TPSC (RPSC) must be filled with valid data. Finally, the output streams can be enabled by setting the PCCE bit in the TPSC (RPSC) Configuration Register to logic 1.

1.42.2 Direct Access Mode

Direct access mode to the TPSC or RPSC is not used in the COMET-Quad. However, direct access mode is selected by default whenever the COMET-Quad is reset. The IND bit within the TPSC and RPSC Configuration Registers must be set to logic 1 after a reset is applied.

1.42.3 Indirect Access Mode

Indirect access mode is selected by setting the IND bit in the TPSC or RPSC Configuration Register to logic 1. When using the indirect access mode, the status of the BUSY indication bit should be polled to determine the status of the microprocessor access: when the BUSY bit is logic 1, the TPSC or RPSC is processing an access request; when the BUSY bit is logic 0, the TPSC or RPSC has completed the request.

The indirect write programming sequence for the TPSC (RPSC) is as follows:

1. Check that the BUSY bit in the TPSC (RPSC) µP Access Status Register is logic 0.
2. Write the channel data to the TPSC (RPSC) Channel Indirect Data Buffer register.

3. Write RWB=0 and the channel address to the TPSC (RPSC) Channel Indirect Address/Control Register.

4. Poll the BUSY bit until it goes to logic 0. The BUSY bit will go to logic 1 immediately after step 3 and remain at logic 1 until the request is complete.

5. If there is more data to be written, go back to step 1.

The indirect read programming sequence for the TPSC (RPSC) is as follows:

1. Check that the BUSY bit in the TPSC (RPSC) µP Access Status Register is logic 0.

2. Write RWB=1 and the channel address to the TPSC (RPSC) Channel Indirect Address/Control Register.

3. Poll the BUSY bit, waiting until it goes to a logic 0. The BUSY bit will go to logic 1 immediately after step 2 and remain at logic 1 until the request is complete.

4. Read the requested channel data from the TPSC (RPSC) Channel Indirect Data Buffer register.

5. If there is more data to be read, go back to step 1.

1.43 Using the Line Receiver

The line receiver must be properly initialized for correct operation. After each reset, several register bits must be programmed, and a RAM table must be initialized. Table 67 summarises the required settings for controlling the RLIU.

Note that several registers are not their default values. The RLPS Equalization Indirect Address must be set to 00H. The Reserved bit of the RLPS Equalizer Configuration register must be set to logic 1. The EQ_VREF[5:0] bits of the RLPS Equalizer Voltage Reference register must be programmed to 2CH (101100B).

Table 67 - Default Setup of the RLIU

Content		Register				
Bin	Hex					
XX000XX1	01H	0F8H	1F8H	2F8H	3F8H	RLPS Configuration and Status
X000X000	00H	0F9H	1F9H	2F9H	3F9H	RLPS ALOS Detection/ Clearance Threshold
00000001	01H	0FAH	1FAH	2FAH	3FAH	RLPS ALOS Detection Period
00000001	01H	0FBH	1FBH	2FBH	3FBH	RLPS ALOS Clearance Time
00000000	00H	0FCH	1FCH	2FCH	3FCH	RLPS Equalization Indirect Address
1XXXXXXX	80H	0FDH	1FDH	2FDH	3FDH	RLPS Equalization RAM Read/WriteB Select
00000000	00H	0FEH	1FEH	2FEH	3FEH	RLPS Equalizer Loop Status and Control

00001011	0BH	0FFH	1FFH	2FFH	3FFH	RLPS Equalizer Configuration
*	*	0D8H	1D8H	2D8H	3D8H	RLPS Equalization Indirect Data[31:24]
*	*	0D9H	1D9H	2D9H	3D9H	RLPS Equalization Indirect Data[23:16]
*	*	0DAH	1DAH	2DAH	3DAH	RLPS Equalization Indirect Data[15:8]
*	*	0DBH	1DBH	2DBH	3DBH	RLPS Equalization Indirect Data[7:0]
XX101100	2CH	0DCH	1DCH	2DCH	3DCH	RLPS Equalizer Voltage Reference

Since the line receiver supports both E1 and T1 standards over either short haul or long haul cables, the line receiver has two normal modes of operation, as selected by the T1/E1B bit of the Global Configuration register. Table 68 and Table 69 contain the values to be programmed into the equalizer RAM for T1 and E1 mode, respectively.

Table 68 - RLPS Equalizer RAM Table (T1 mode)

Table 69 - RLPS Equalizer RAM Table (E1 mode)

Access to the Equalizer RAM is provided by means of Registers xFCH, xFDH, xD8H, xD9H, xFAH, and xFBH, where ‘x’ refers to the COMET quadrant numbered 0 through 3. A typical programming sequence follows, this programming sequence is repeated for each of the 256 Equalizer RAM Addresses.

```
WRITE xD8H  <31 – 24 Bits of Data>

WRITE xD9H  <23 – 16 Bits of Data>

WRITE xDAH  <15 – 8 Bits of Data>

WRITE xDBH  <7 – 0 Bits of Data>

ACTION xFDH  <A=80H for “read”; A=00H for “write” action>

WRITE xFCH  <address register from 0 to 255>

PAUSE  <wait 3 line rate clock cycles>
```

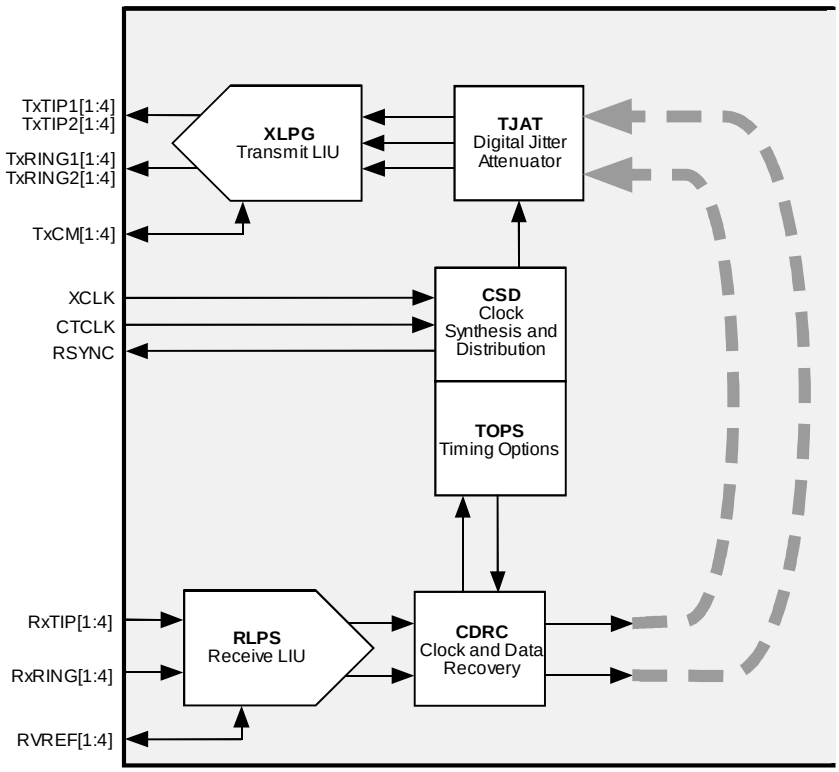
1.44 T1/E1 Framer Loopback Modes

The COMET-Quad provides four loopback modes to aid in network and system diagnostics. The network loopbacks (Payload and Line) can be initiated at any time via the µP interface, but are usually initiated once an inband loopback activate code is detected. The system Diagnostic Digital loopback can be initiated at any time by the system via the µP interface to check the path of system data through the framer. The Per-DS0 loopback permits the payload to be looped-back on a per-DS0 basis to allow network testing without taking an entire link off-line.

1.44.1 Line Loopback

When LINE loopback (LINELB) is initiated by setting the LINELB bit in the Master Diagnostics Register (00AH) to logic 1, the COMET-Quad is configured to internally connect the recovered data to the transmit jitter attenuator, TJAT. The data sent to the TJAT is the recovered data from the output of the CDRC block. Note that when line loopback is enabled, the contents of the TJAT Reference Clock Divisor and Output Clock Divisor registers should be programmed to 2FH to correctly attenuate the jitter on the receive clock. Conceptually, the data flow through a single quadrant of the COMET-Quad in this loopback mode is illustrated in Figure 33.

Figure 33: - Line Loopback

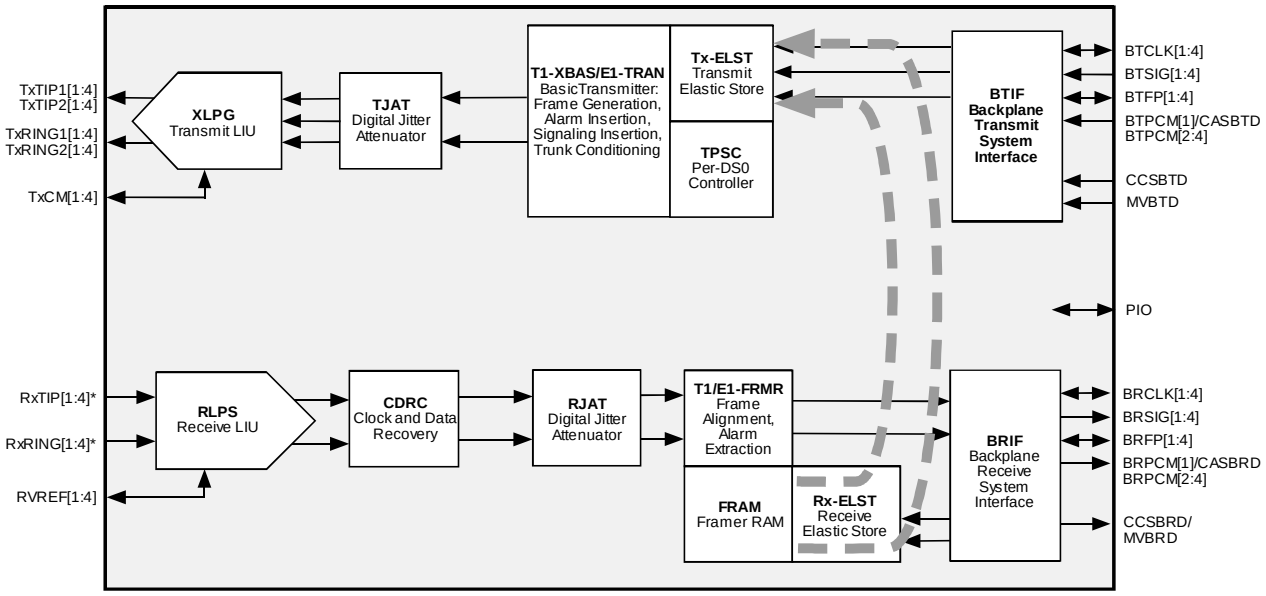


1.44.2 Payload Loopback

When PAYLOAD loopback (PAYLB) is initiated by setting the PAYLB bit in the Master Diagnostics Register (00AH) to logic 1, the COMET-Quad is configured to internally connect the output of its RX-ELST to the PCM input of its transmitter block. The data read out of RX-ELST is timed to the transmitter clock, and the transmit frame alignment indication is used to synchronize the output frame alignment of RX-ELST. Conceptually, the data flow through a single quadrant of the COMET-Quad in this loopback mode is illustrated in Figure 34. Note that because the transmit and receive streams are not superframe aligned, any robbed-bit signaling in the receive stream

will not fall in the correct frame once looped back and that transmit robbed-bit signaling will overwrite the looped back data if signaling insertion is enabled.

Figure 34: - Payload Loopback



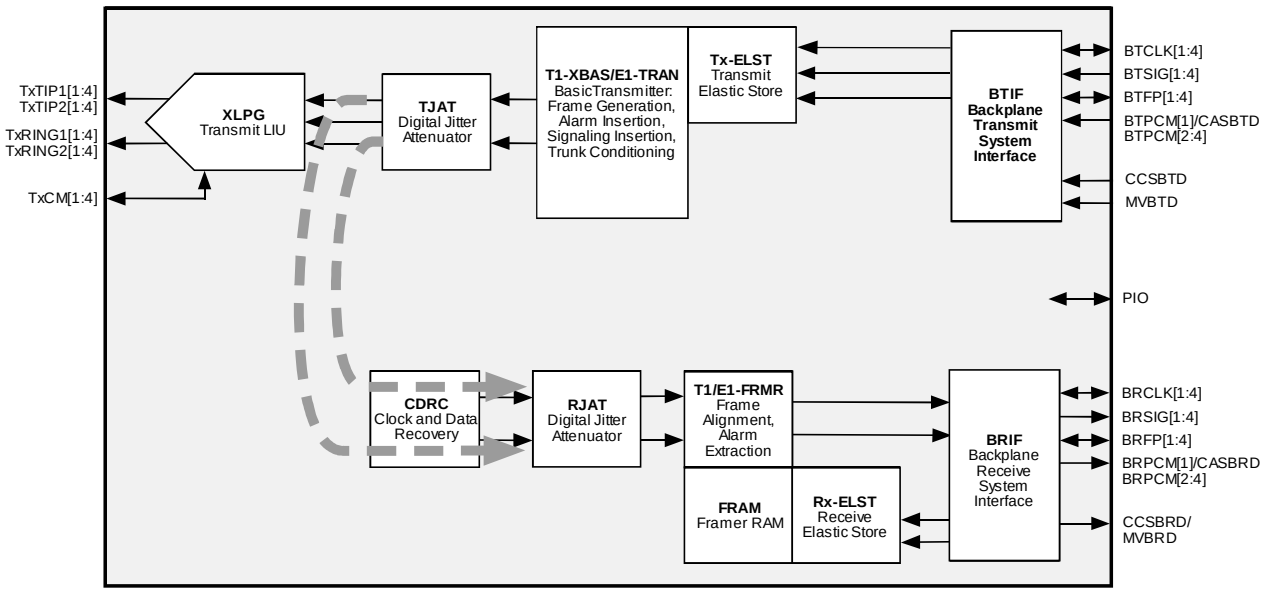
1.44.3 Per-Channel Loopback

The T1/E1 payload may be looped-back on a per-channel basis through the use of the TPSC. If all channels are looped-back, the result is very similar to Payload Loopback. In order for per-channel loopback to operate correctly, the Backplane Receive Interface must be in Clock Master mode, or else BRFP and BRCLK must be connected to BTFP and BTCLK, respectively. The LOOP bit must be set to logic 1 in the TPSC Internal Registers for each channel desired to be looped back, and the PCCE bit must be set to logic 1 in the TPSC Configuration register. When all these configurations have been made, the backplane receive DS0s or timeslots selected will overwrite their corresponding backplane transmit channels; the remaining backplane transmit channels will pass through intact. Conceptually, the data flow through a single quadrant of the COMET-Quad in this loopback mode is illustrated in Figure 34. Note that because the backplane transmit and backplane receive streams will not be superframe aligned, that any robbed-bit signaling in the backplane receive stream may not fall in the correct frame once looped-back, and that backplane transmit robbed-bit signaling will overwrite the looped-back channel data if signaling insertion is enabled.

1.44.4 Diagnostic Digital Loopback

When Diagnostic Digital loopback (DDLB) mode is initiated by setting the DDLB bit in the Master Diagnostics Register to logic 1, the COMET-Quad quadrant is configured to internally direct the output of the TJAT to the inputs of the receiver section. The dual-rail RZ outputs of the TJAT are directed to the dual-rail inputs of the CDRC. Conceptually, the data flow through a single quadrant of the COMET-Quad in this loopback condition is illustrated in Figure 35.

Figure 35: - Diagnostic Digital Loopback



1.45 Backplane Configuration

The following are example register settings that could be programmed for Backplane Interface modes. In some cases, variations from the example settings are possible. Example 1: in several of the modes, the active edge of BRCLK[x] and BTCLK[x] can be configured to be either the rising or falling edge via the BRIF Configuration and BTIF Configuration registers. Example 2: in several of the modes, several configuration of the Transmit Timing Options register are possible. Example 3: the Transmit and Receive Jitter Attenuators (JAT's) can be either enabled or disabled in several of the modes. The example settings in the below tables are to be used in conjunction with the register descriptions found in the Normal Mode Register: the below tables may not provide sufficient information for correct programming in all modes. Also note that in some modes, the registers are to be programmed differently between T1 and E1. These differences are outlined the register descriptions but may not indicated in the below tables.

1.45.1 Receive Clock Master: Full T1/E1

See Figure 9 and the Normal Mode Register Description section for details on this mode.

Register	Bit Name	Example Setting
Receive Options	RJATBYP	0
Receive Options	RXELSTBYP	1
BRIF Configuration	NX64KBIT/S[1]	0
BRIF Configuration	NX64KBIT/S[0]	0
BRIF Configuration	CMODE	0
BRIF Configuration	RATE[1]	0
BRIF Configuration	RATE[0]	0 or 1
BRIF Frame Pulse Configuration	FPMODE	0

1.45.2 Receive Clock Master: Nx64Kbit/s

See Figure 10 and the Normal Mode Register Description section for details on this mode.

Register	Bit Name	Example Setting
Receive Options	RJATBYP	0
Receive Options	RXELSTBYP	1
BRIF Configuration	NX64KBIT/S[1]	0 or 1
BRIF Configuration	NX64KBIT/S[0]	0 or 1
BRIF Configuration	CMODE	0
BRIF Configuration	RATE[1]	0
BRIF Configuration	RATE[0]	0 or 1
BRIF Frame Pulse Configuration	FPMODE	0

1.45.3 Receive Clock Master: Clear Channel

See Figure 11and the Normal Mode Register Description section for details on this mode.

Register	Bit Name	Example Setting
Receive Options	RJATBYP	0
Receive Options	UNF	1
Receive Options	RXELSTBYP	1
BRIF Configuration	CMODE	0
BRIF Configuration	RATE[1]	0
BRIF Configuration	RATE[0]	0 or 1

1.45.4 Receive Clock Slave: Full T1/E1

See Figure 12 and the Normal Mode Register Description section for details on this mode.

Register	Bit Name	Example Setting
Receive Options	RXELSTBYP	0
RX-ELST Configuration	IR, OR	0 or 1
BRIF Configuration	NX64KBIT/S[1]	0
BRIF Configuration	NX64KBIT/S[0]	0
BRIF Configuration	CMODE	1
BRIF Configuration	CMS	0
BRIF Configuration	RATE[1]	0
BRIF Configuration	RATE[0]	0 or 1
BRIF Frame Pulse Configuration	FPMODE	1

1.45.5 Receive Clock Slave: H-MVIP

See Figure 13 and the Normal Mode Register Description section for details on this mode.

Register	Bit Name	Example Setting
Receive Options	RXELSTBYP	0
RX-ELST Configuration	IR, OR	0 or 1
BRIF Configuration	CMODE	1
BRIF Configuration	DE	0
BRIF Configuration	FE	1
BRIF Configuration	CMS	1
BRIF Configuration	RATE[1]	1
BRIF Configuration	RATE[0]	1
BRIF Frame Pulse Configuration	MAP	0
BRIF Frame Pulse Configuration	FPINV	0

Register	Bit Name	Example Setting
BRIF Frame Pulse Configuration	FPMODE	1
BRIF Parity/F-bit Configuration	TRI	1
RX-ELST CCS Configuration	IR	0 or 1
Receive H-MVIP/CCS Enable	RHMVIPEN	1
Quadrant 1: BRIF Timeslot Offset	TSOFF[6:0]	0000000
Quadrant 2: BRIF Timeslot Offset	TSOFF[6:0]	0000001
Quadrant 3: BRIF Timeslot Offset	TSOFF[6:0]	0000010
Quadrant 4: BRIF Timeslot Offset	TSOFF[6:0]	0000011

1.45.6 Receive Clock Slave: Full T1/E1 with CCS H-MVIP

See Figure 14 and the Normal Mode Register Description section for details on this mode.

Register	Bit Name	Example Setting
Receive Options	RXELSTBYP	0
RX-ELST Configuration	IR, OR	0 or 1
BRIF Configuration	NX64KBIT/S[1]	0
BRIF Configuration	NX64KBIT/S[0]	0
BRIF Configuration	CMODE	1
BRIF Configuration	CMS	0
BRIF Configuration	RATE[1]	0
BRIF Configuration	RATE[0]	0 or 1
BRIF Frame Pulse Configuration	FPMODE	1
RX-ELST CCS Configuration	IR	0 or 1
Receive H-MVIP/CCS Enable	RCCSEN	1
Receive H-MVIP/CCS Enable	RHMVIPEN	0

1.45.7 Transmit Clock Master: Full T1/E1

See Figure 15 and the Normal Mode Register Description section for details on this mode.

Register	Bit Name	Example Setting
Transmit Line Interface Configuration	TJATBYP	0
Transmit Timing Options	TXELSTBYP	1
BTIF Configuration	NX64KBIT/S[1]	0
BTIF Configuration	NX64KBIT/S[0]	0
BTIF Configuration	CMODE	0
BTIF Configuration	RATE[1]	0
BTIF Configuration	RATE[0]	0 or 1
BTIF Frame Pulse Configuration	FPMODE	0

1.45.8 Transmit Clock Master: Nx64Kbit/s

See Figure 16 and the Normal Mode Register Description section for details on this mode.

Register	Bit Name	Example Setting
Transmit Line Interface Configuration	TJATBYP	0
Transmit Timing Options	TXELSTBYP	1
BTIF Configuration	NX64KBIT/S[1]	0 or 1
BTIF Configuration	NX64KBIT/S[0]	0 or 1
BTIF Configuration	CMODE	0
BTIF Configuration	RATE[1]	0
BTIF Configuration	RATE[0]	0 or 1
BTIF Frame Pulse Configuration	FPMODE	0

1.45.9 Transmit Clock Master: Clear Channel

See Figure 17 and the Normal Mode Register Description section for details on this mode.

Register	Bit Name	Example Setting
Transmit Line Interface Configuration	TJATBYP	0
Transmit Framing and Bypass Options	FDIS	1
Transmit Timing Options	TXELSTBYP	1
BTIF Configuration	CMODE	0
BTIF Configuration	RATE[1]	0
BTIF Configuration	RATE[0]	0 or 1

1.45.10 Transmit Clock Slave: Full T1/E1

See Figure 18 and the Normal Mode Register Description section for details on this mode.

Register	Bit Name	Example Setting
Transmit Timing Options	TXELSTBYP	0 or 1
TX-ELST Configuration	IR, OR	0 or 1
BTIF Configuration	NX64KBIT/S[1]	0
BTIF Configuration	NX64KBIT/S[0]	0
BTIF Configuration	CMODE	1
BTIF Configuration	CMS	0
BTIF Configuration	RATE[1]	0
BTIF Configuration	RATE[0]	0 or 1
BTIF Frame Pulse Configuration	FPMODE	1

1.45.11 Transmit Clock Slave: Clear Channel

See Figure 19 and the Normal Mode Register Description section for details on this mode.

Register	Bit Name	Example Setting
Transmit Line Interface Configuration	TJATBYP	0
Transmit Framing and Bypass Options	FDIS	1
Transmit Timing Options	TXELSTBYP	1
BTIF Configuration	CMODE	1
BTIF Configuration	RATE[1]	0
BTIF Configuration	RATE[0]	0 or 1

1.45.12 Transmit Clock Slave: H-MVIP

See Figure 20 and the Normal Mode Register Description section for details on this mode.

Register	Bit Name	Example Setting
Transmit Timing Options	TXELSTBYP	0 or 1
TX-ELST Configuration	IR, OR	0 or 1
BTIF Configuration	CMODE	1
BTIF Configuration	DE	1
BTIF Configuration	FE	1
BTIF Configuration	CMS	1
BTIF Configuration	RATE[1]	1
BTIF Configuration	RATE[0]	1
BTIF Frame Pulse Configuration	FPINV	1
BTIF Frame Pulse Configuration	FPTYP	0
BTIF Frame Pulse Configuration	FPMODE	1
TX-ELST CCS Configuration	OR	0 or 1
Transmit H-MVIP/CCS Enable and Configuration	THMVIPEN	1
Transmit H-MVIP/CCS Enable and Configuration	TCCSEN	0 or 1
Transmit H-MVIP/CCS Enable and Configuration	TCCS15, TCCS31	0 or 1
Transmit H-MVIP/CCS Enable and Configuration	TCCS16	0 or 1 Note: CCS is inserted upstream of the E1-TRAN. To avoid Timeslot 16 CCS from being overwritten, program both the SIGEN and DLEN bits of the E1 TRAN Configuration register to logic 0.
Quadrant 1: BTIF Timeslot Offset	TSOFF[6:0]	0000000

Register	Bit Name	Example Setting
Quadrant 2: BTIF Timeslot Offset	TSOFF[6:0]	0000001
Quadrant 3: BTIF Timeslot Offset	TSOFF[6:0]	0000010
Quadrant 4: BTIF Timeslot Offset	TSOFF[6:0]	0000011

1.45.13 Transmit Clock Slave: Full T1/E1 with CCS H-MVIP

See Figure 21 and the Normal Mode Register Description section for details on this mode.

Register	Bit Name	Example Setting
Transmit Timing Options	TXELSTBYP	0 or 1
TX-ELST Configuration	IR, OR	0 or 1
BTIF Configuration	NX64KBIT/S[1]	0
BTIF Configuration	NX64KBIT/S[0]	0
BTIF Configuration	CMODE	1
BTIF Configuration	CMS	0
BTIF Configuration	RATE[1]	0
BTIF Configuration	RATE[0]	0 or 1
BTIF Frame Pulse Configuration	FPMODE	1
Transmit H-MVIP/CCS Enable and Configuration	THMVIPEN	0
Transmit H-MVIP/CCS Enable and Configuration	TCCSEN	1
Transmit H-MVIP/CCS Enable and Configuration	TCCS15, TCCS16, TCCS31	0 or 1

1.46 H-MVIP Data Format

The H-MVIP data and Channel Associated Signaling streams on the COMET-Quad are able to carry all the DS0s for 4 T1s or all timeslots for 4 E1s. When Carrying timeslots from E1s the H-MVIP frame is completely filled with 128 timeslots from four E1s but when carrying DS0s from four T1s there are not enough DS0s to completely fill the 128 byte frame. Table 70 shows how the DS0s and CAS bits of four T1s are formatted in the 128 timeslot H-MVIP frame. Table 71 shows the timeslot and CAS bit H-MVIP format when in E1 mode.

Table 70: - Data and CAS T1 H-MVIP Format

Timeslot Number	First T1 DS0 Number	Second T1 DS0 Number	Third T1 DS0 Number	Fourth T1 DS0 Number
0-3	Undefined	Undefined	Undefined	Undefined
4-7	1	1	1	1
8-11	2	2	2	2
12-15	3	3	3	3
16-19	Undefined	Undefined	Undefined	Undefined
20-23	4	4	4	4
24-27	5	5	5	5
28-31	6	6	6	6
32-35	Undefined	Undefined	Undefined	Undefined
36-39	7	7	7	7
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
108-111	21	21	21	21
112-115	Undefined	Undefined	Undefined	Undefined
116-119	22	22	22	22
120-123	23	23	23	23
124-127	24	24	24	24

Table 71: - Data and CAS E1 H-MVIP Format

Timeslot Number	First E1 TS Number	Second E1 TS Number	Third E1 TS Number	Fourth E1 TS Number
0-3	1	1	1	1
4-7	2	2	2	2
8-11	3	3	3	3
12-15	4	4	4	4
16-19	5	5	5	5
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
120-123	31	31	31	31
124-127	32	32	32	32

The H-MVIP Common Channel Signaling interface on COMET-Quad carries at most 12 timeslots when in E1 mode: four instances of timeslot 16 for ISDN signaling, timeslot 15 and timeslot 31 for V5.2 interfaces. In T1 mode, the CCS H-MVIP stream carries at most 4 timeslots: four instances of timeslot 24. Table 72 shows the H-MVIP format for carrying 4 common channeling signaling channels when in T1 mode. Table 73 shows the H-MVIP format for carrying 12 common channeling signaling channels when in E1 mode. When a signaling or V5.2 channel is not in use the H-MVIP timeslot is undefined.

Table 72: - CCS T1 H-MVIP Format

H-MVIP Timeslot Number	T1 Designation
0	Undefined
1	Undefined
2	Undefined
•	•
•	•
123	Undefined
124	Quadrant 1 Timeslot 24
125	Quadrant 2 Timeslot 24
126	Quadrant 3 Timeslot 24

127	Quadrant 4 Timeslot 24

Table 73: - CCS E1 H-MVIP Format

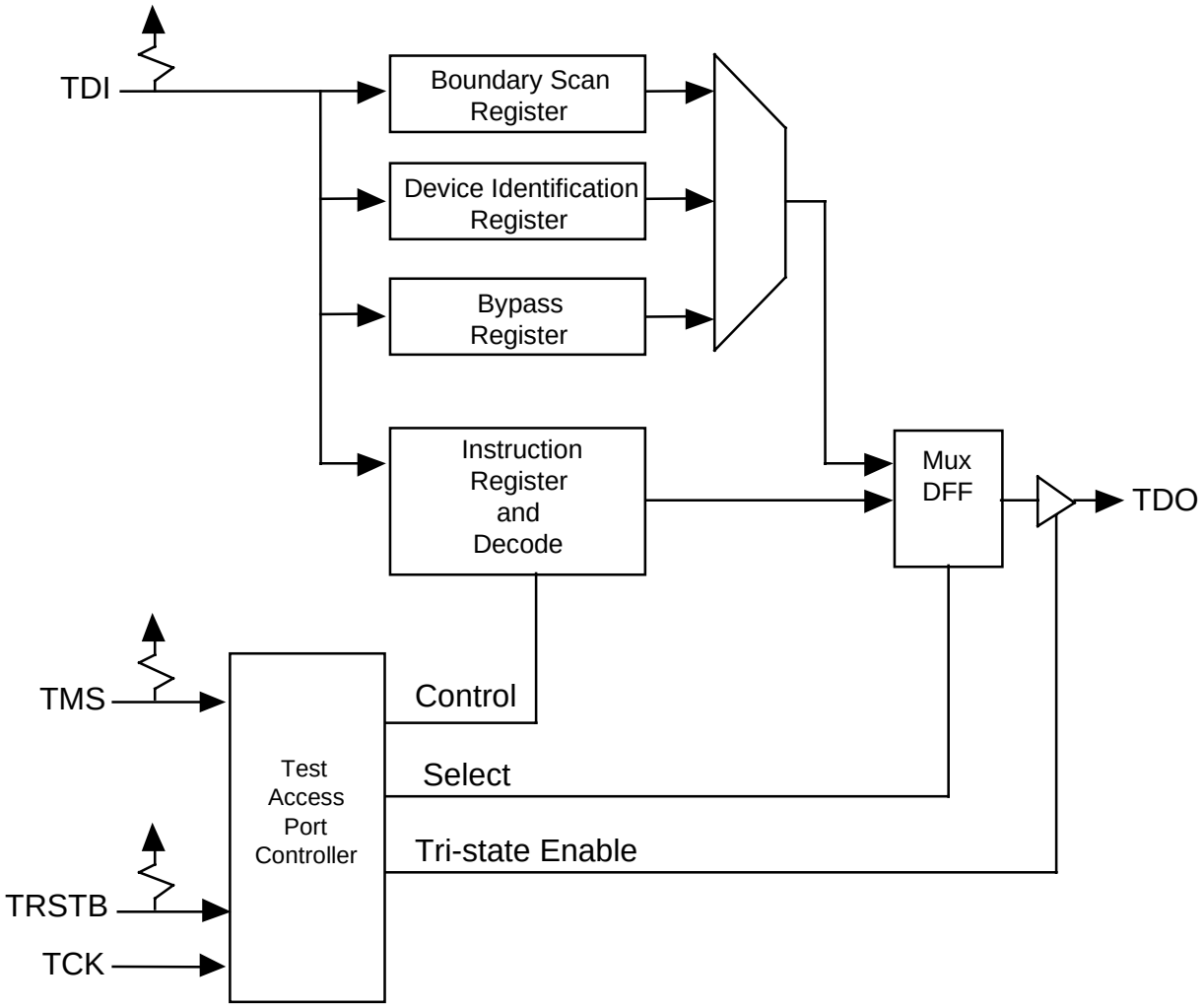
H-MVIP Timeslot Number	E1 Designation
0	Undefined
1	Undefined
•	•
•	•
•	•
59	Undefined
60	Quadrant 1 Timeslot 15
61	Quadrant 2 Timeslot 15
62	Quadrant 3 Timeslot 15
63	Quadrant 4 Timeslot 15
64	Quadrant 1 Timeslot 16
65	Quadrant 2 Timeslot 16
66	Quadrant 3 Timeslot 16
66	Quadrant 4 Timeslot 16
67	Undefined
•	•
•	•
•	•
123	Undefined
124	Quadrant 1 Timeslot 31
125	Quadrant 2 Timeslot 31
126	Quadrant 3 Timeslot 31
127	Quadrant 4 Timeslot 31

1.47 JTAG Support

The COMET-Quad supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The

TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 36: - Boundary Scan Architecture



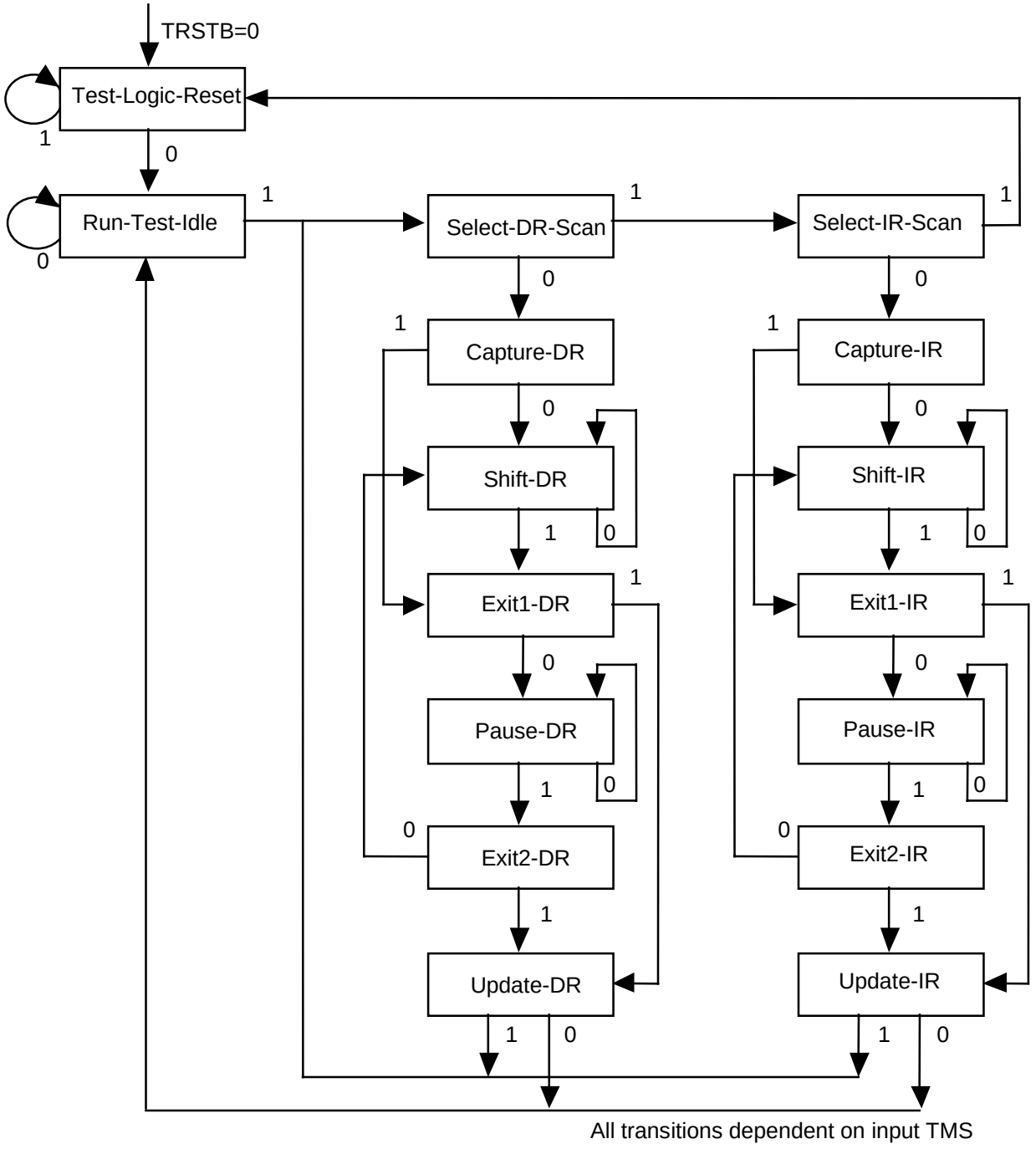
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register placed in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI, and forced onto all digital outputs.

1.47.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is described below.

Figure 37: - TAP Controller Finite State Machine



Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

Boundary Scan Instructions

The following is a description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state.

STCTEST

The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device

identification code is loaded into the boundary scan register. The code can then be shifted out of the output, TDO, using the Shift-DR state.

Boundary Scan Cells

In the following diagrams, CLOCK-DR is equal to TCK when the current controller state is SHIFT-DR or CAPTURE-DR, and unchanging otherwise. The multiplexer in the center of the diagram selects one of four inputs, depending on the status of select lines G1 and G2. The ID Code bit is as listed in the Boundary Scan Register table in the JTAG Test Port section 11.2.

Figure 38: - Input Observation Cell (IN_CELL)

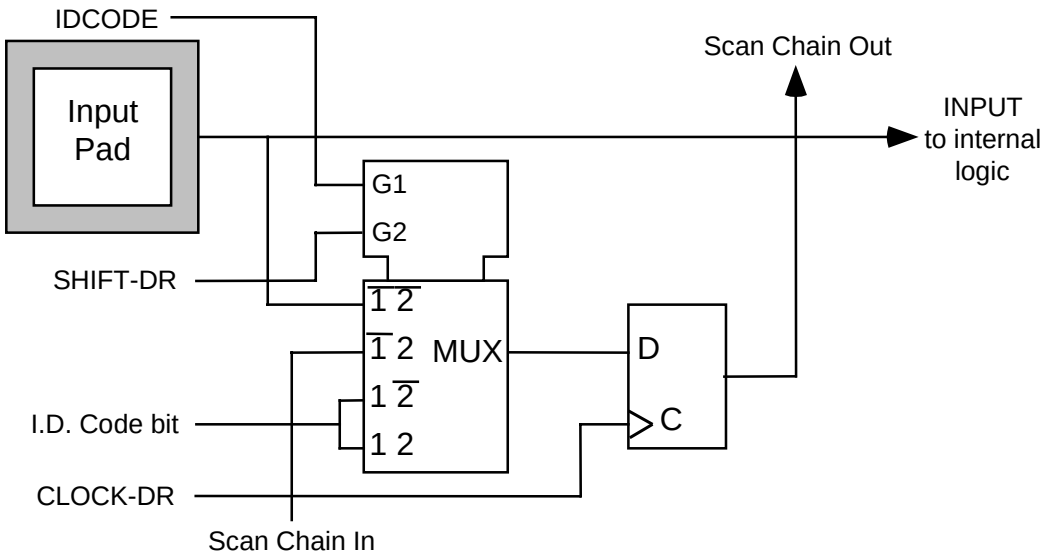


Figure 39: - Output Cell (OUT_CELL)

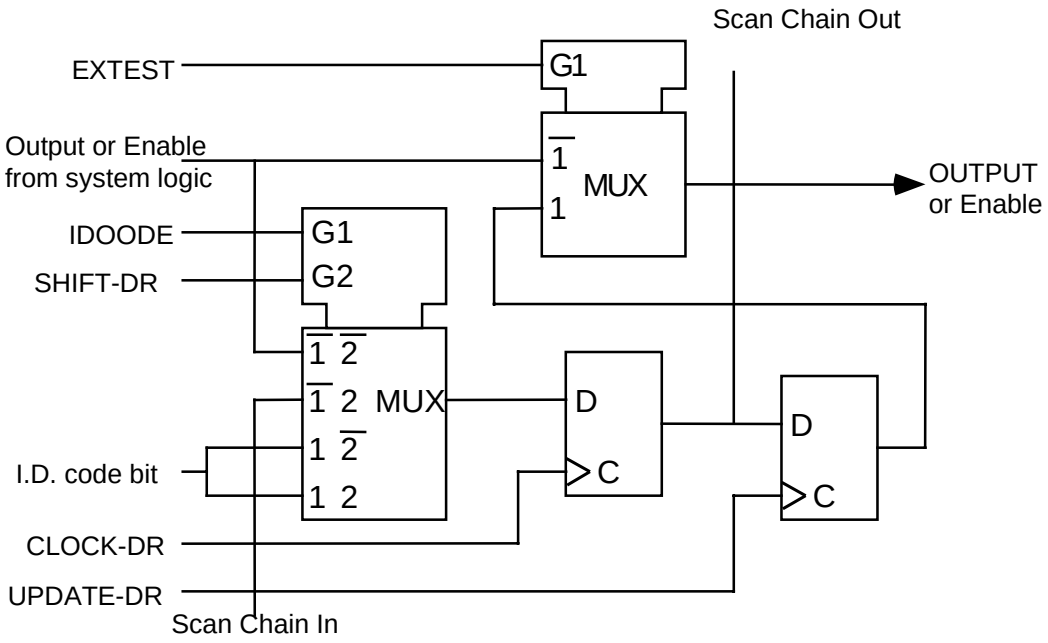


Figure 40: - Bidirectional Cell (IO_CELL)

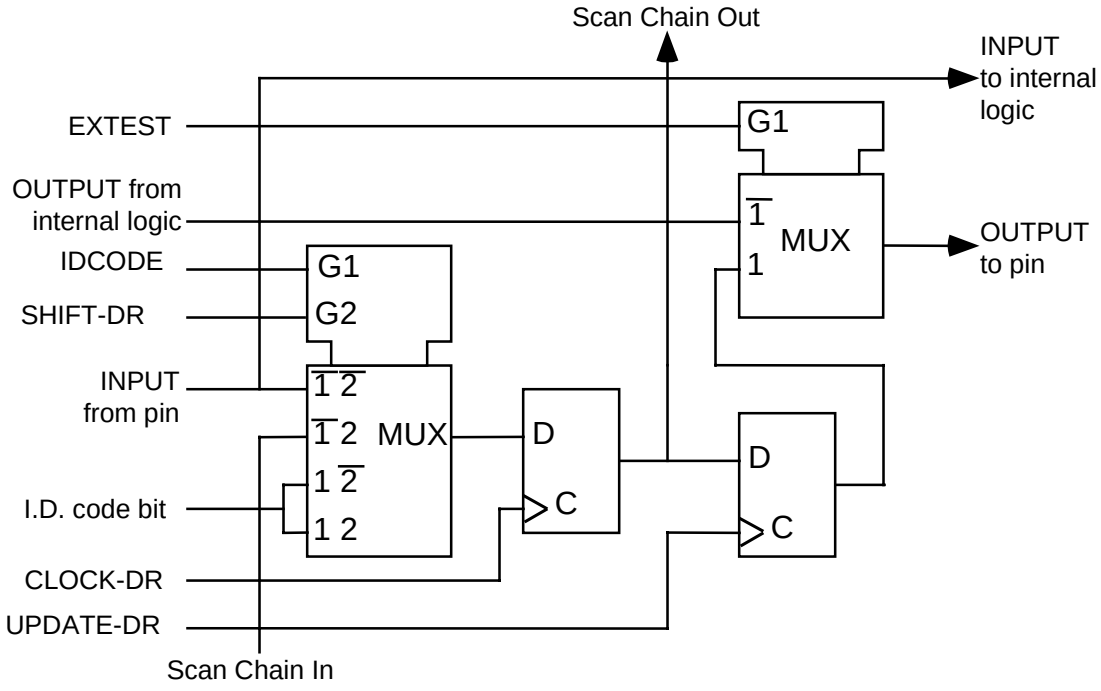
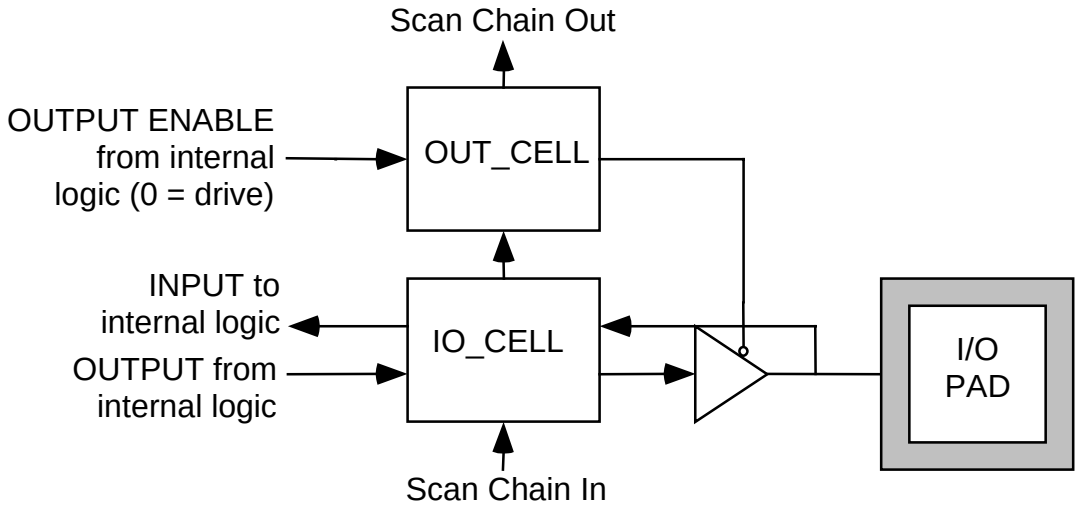


Figure 41: - Layout of Output Enable and Bidirectional Cells



1.48 Board Design Recommendations

FUNCTIONAL TIMING

1.49 Backplane Receive Serial Clock and Data Interface Timing

Figure 42: -T1 Receive Clock Master : Full T1/E1 Mode

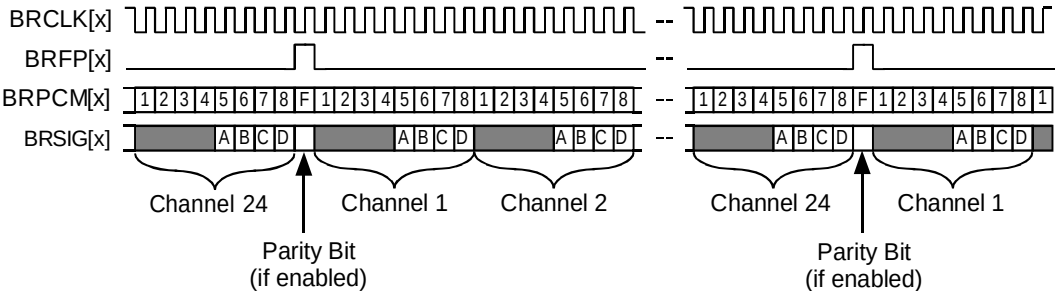
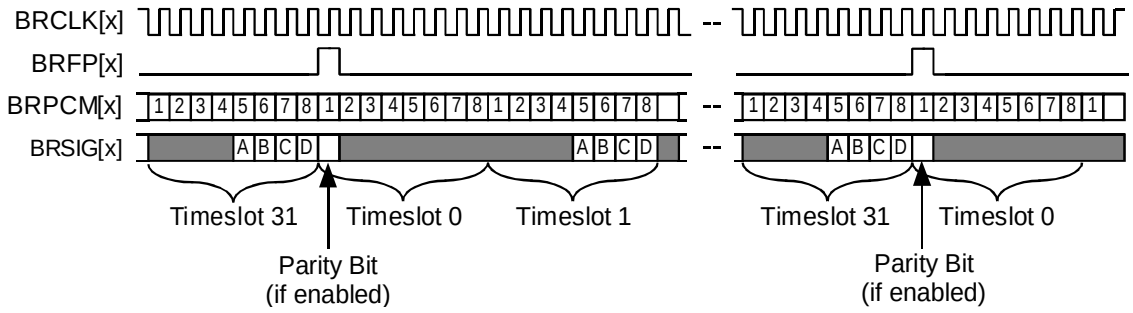


Figure 43: - E1 Receive Clock Master : Full T1/E1 Mode



The COMET-Quad has been programmed to select the Clock Master: Full T1/E1 mode. BRFP[x] is set high for one BRCLK[x] period every frame. If BRXSMFP=1 in T1 mode, BRFP[x] pulses on the superframe frame boundaries (i.e. once every 12 or 24 frame periods). If ROHM=0, BRXSMFP=0, and BRXCMFP=1 in E1 mode, BRFP[x] pulses once every CRC Multiframe. If ALTBRFP=1, BRFP[x] pulses on every second indication of either the frame or the superframe or multiframe boundary.

Figure 44: - T1 Receive Clock Master: Nx64Kbit/s Mode

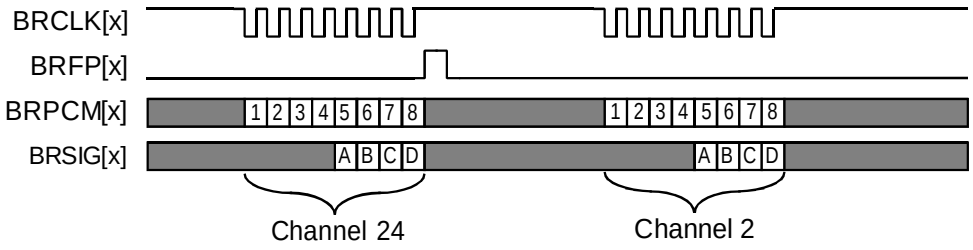
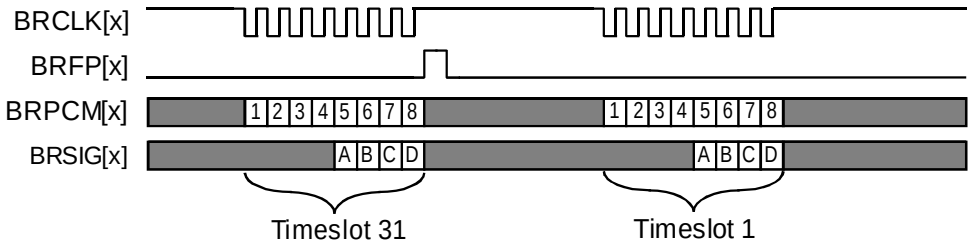


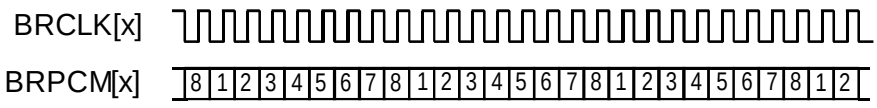
Figure 45: - E1 Receive Clock Master : Nx64Kbit/s Mode



The BRIF Configuration register is programmed to select Nx64Kbit/s mode. The DE and FE register bits are programmed to logic 0, configuring BRPCM[x], BRSIG[x], and BRFP[x] to update on the falling edge of BRCLK[x]. The RPSC backplane receive control bytes are programmed to extract the desired channels. In Figure 44, the backplane receive control bytes for T1 channels 2 and 24 are extracted. In Figure 45, the backplane receive control bytes for E1 channels 31 and 1 are extracted. BRCLK[x] is gapped so that it is only active for those channels whose associated

DTRKC bit is programmed to logic 0. If either BRXSMFP (ROHM, BRXCMFP, and BRXSMFP in E1 mode) or ALTBRFP is configured, then BRFP[x] will pulse only during the appropriate frames. When the DE register bit is set, BRPCM[x] and BRSIG[x] update on the rising edge of BRCLK[x]. When the FE register bit is set, BRFP[x] updates on the rising edge of BRCLK[x].

Figure 46: - T1/E1 Receive Clock Master : Clear Channel Mode



The Backplane Receive Interface is configured for the Clock Slave: Clear Channel mode by programming the UNF bit of the Receive Options register to logic 1, the RXELSTBYP bit to logic 1, the RJATBYP bit optionally to logic 0, and the CMODE bit of the BRIF Configuration register to logic 0. When the DE bit is programmed to logic 0, BRPCM[x] is clocked out on the falling edge of the BRCLK[x] output. When the DE bit is programmed to logic 1, BRPCM[x] is updated on the rising edge of BRCLK, and the functional timing is described by Figure 46 with the BRCLK signal inverted.

Figure 47: - T1 Receive Clock Slave: Full T1/E1 Mode

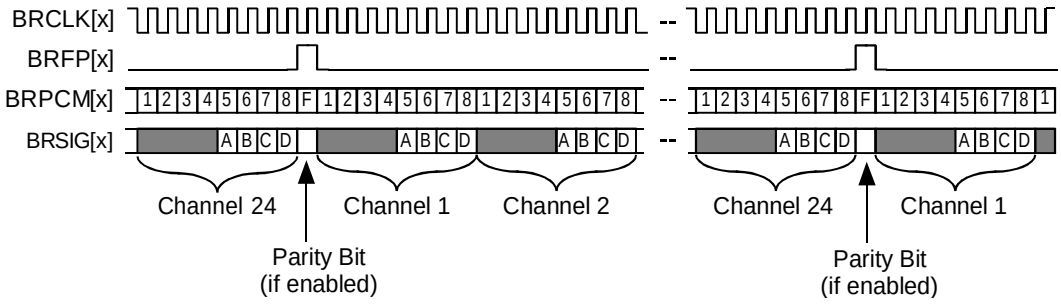
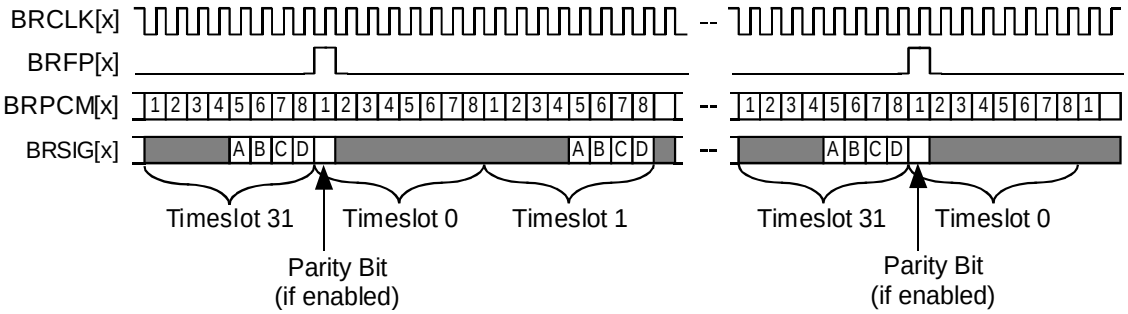


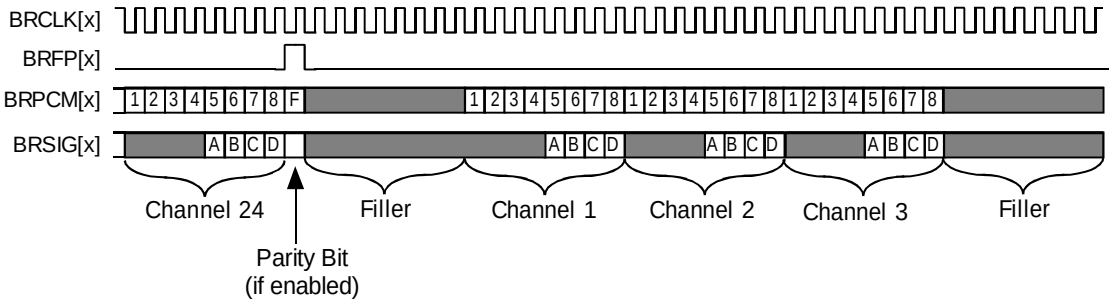
Figure 48: - E1 Receive Clock Slave: Full T1/E1 Mode



The Backplane Receive Interface is programmed for Clock Slave: Full T1/E1 mode by programming the RXELSTBYP bit of the Receive Options register to logic 0 and the CMODE and

FPMODE bits of the BRIF Configuration register to logic 1. BRPCM[x] and BRSIG[x] are timed to the active edge of BRCLK[x], and are frame-aligned to BRFP[x]; BRFP[x] need not be provided every frame. BRPCM[x] and BRSIG[x] may be configured to carry a parity bit during the first bit of each frame.

Figure 49: - T1 Receive 2.048 MHz Clock Slave: Full T1/E1 Mode

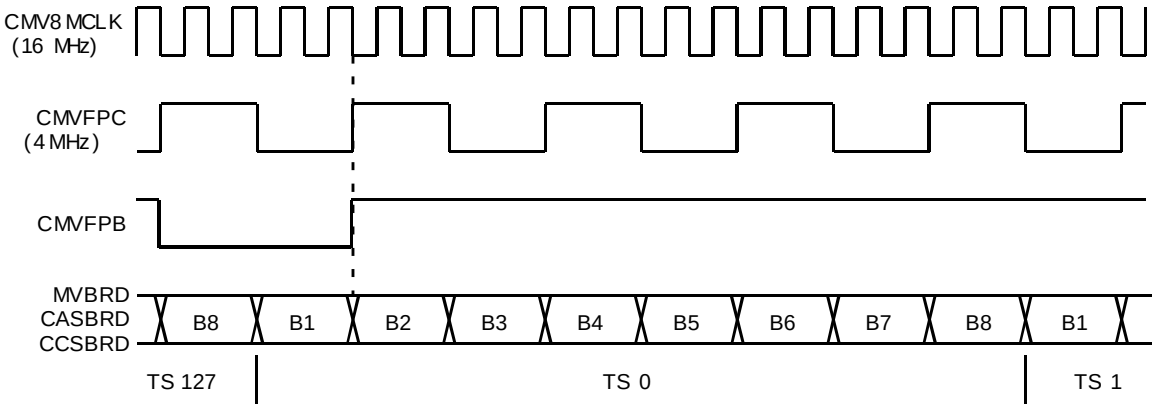


The Backplane Receive Interface is programmed for Clock Slave: Full T1/E1 mode by programming the RXELSTBYP bit of the Receive Options register to logic 0 and the CMODE and FPMODE bits of the BRIF Configuration register to logic 1. The 2.048 MHz internally-gapped clock mode is selected by programming the RATE[1:0] bits of the BRIF Configuration register to "01" (i.e., to the 2.048 Mbit/s mode). The above figure applies when the MAP bit of the BRIF Configuration register is programmed to logic 0. BRPCM[x] is timed to the active edge of BRCLK[x], and is frame-aligned to BRFP[x]; BRFP[x] need not be provided every frame. BRPCM[x] and BRSIG[x] may be configured to carry a parity bit during the first bit of each frame. The values of the filler bits will depend on the exact configuration of the COMET-Quad, and they will be included in the parity calculation.

1.50 Backplane Receive H-MVIP Link Timing

The timing relationship of the common 8M H-MVIP clock (CMV8MCLK), frame pulse clock (CMVFPC), data (MVBRD, CASBRD or CCSBRD) and frame pulse (CMVFPB) signals in 8.192 Mbit/s H-MVIP operation with a type 0 frame pulse is shown in Figure 50. The falling edges of each CMVFPC are aligned to a falling edge of the corresponding CMV8MCLK for 8.192 Mbit/s H-MVIP operation. The COMET-Quad samples CMVFPB low on the falling edge of CMVFPC and references this point as the start of the next frame. The COMET-Quad updates the data provided on MVBRD, CASBRD and CCSBRD on every second falling edge of CMV8MCLK as indicated for bit 2 (B2) of timeslot 0 (TS 0) in Figure 50. The first bit of the next frame is updated on MVBRD, CASBRD and CCSBRD on the falling CMV8MCLK clock edge for which CMVFPB is also sampled low. B1 is the most significant bit (first bit output on MVBRD, CASBRD, CCSBRD) and B8 is the least significant bit (last bit output on MVBRD, CASBRD, CCSBRD) of each octet.

Figure 50: - Receive 8.192 Mbit/s H-MVIP Link Timing



1.51 Backplane Transmit Serial Clock and Data Interface Timing

By convention in the following functional timing diagrams, the first bit transmitted in each channel shall be designated bit 1 and the last shall be designated bit 8. Each of the Backplane Receive and Backplane Transmit Master and Clock Modes apply to both T1 and E1 configurations with the exception of the 2.048MHz T1 Clock Slave Modes.

Figure 51: -T1 Transmit Clock Master : Full T1/E1 Mode

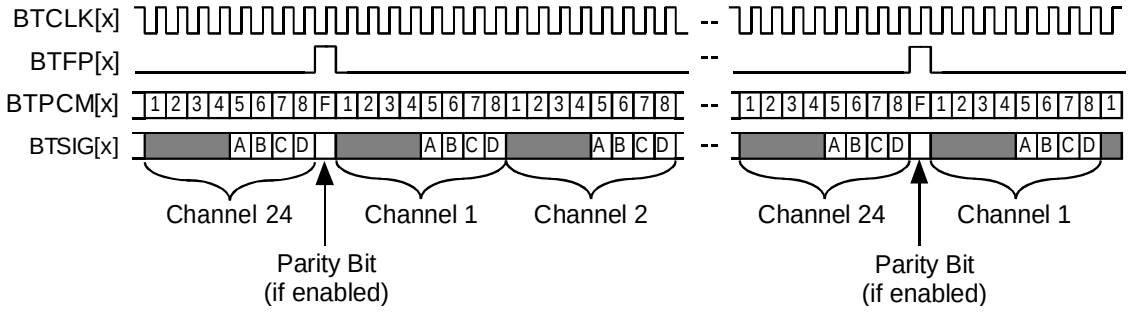
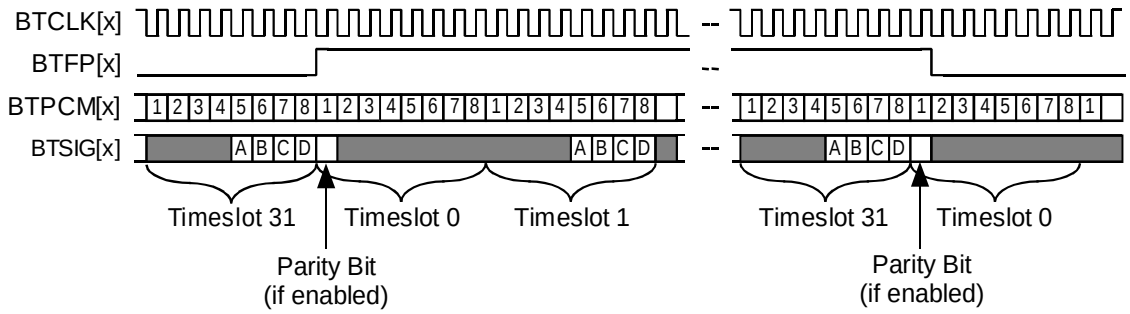


Figure 52: - E1 Transmit Clock Master : Full T1/E1 Mode



The Transmit Interface is programmed to select the Clock Master: Full T1/E1 mode by programming CMODE bit of the BTIF Configuration register to logic 0 and the FPMODE bit of the BTIF Frame Pulse Configuration register to logic 0. BTFP[x] is set high for one BTCLK[x] period every frame. If FPTYP=1, BTFP[x] pulses on the superframe frame boundaries. This means pulsing for one bit period every 12 or 24 frame periods when configured for T1 operation or toggling high to mark bit 1 of frame 1 of every 16 frame Signaling Multiframe and toggling low following bit 1 of every 16 frame CRC Multiframe when configured for E1 operation.

BTSIG[x] should carry the signaling bits for each channel in bits 5,6,7 and 8. These signaling bits will be inserted into the data stream by the T1 or E1 transmitter. If parity checking is enabled, a parity bit should be inserted on BTPCM[x] and BTSIG[x] in the first bit of each frame. The parity operates on all bits in the BTPCM[x] and BTSIG[x] streams, including the unused bits on BTSIG[x].

Figure 53: - T1 Transmit Clock Master: Nx64Kbit/s Mode

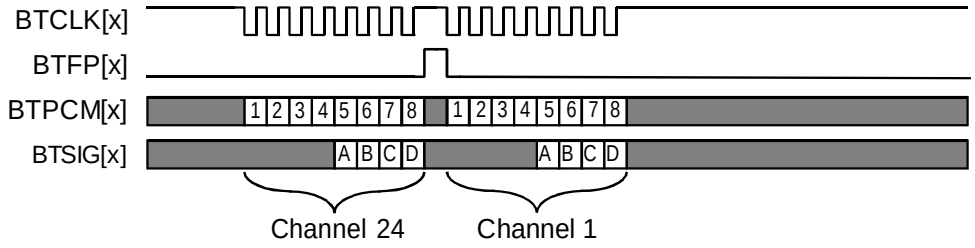
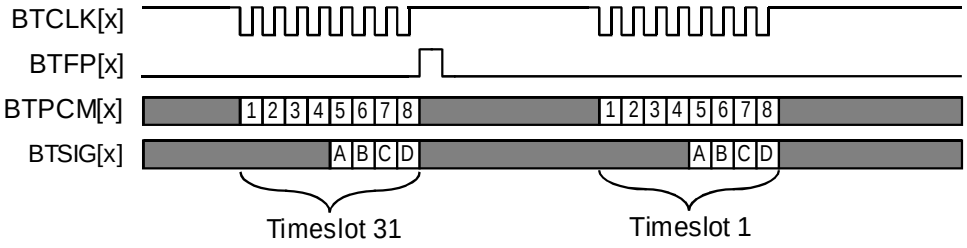
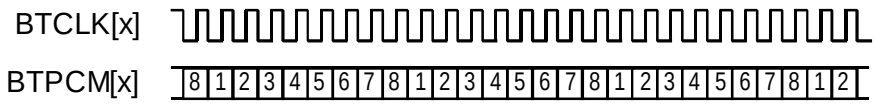


Figure 54: - E1 Transmit Clock Master : Nx64Kbit/s Mode



The BTIF Configuration register is programmed to select Nx64Kbit/s mode. The TPSC PCM Data Control bytes are programmed to insert the desired channels. In Figure 53, the PCM Data Control bytes for T1 channels 1 and 24 are configured to insert BTPCM[x] data into these channels. In Figure 54, the PCM Data Control bytes for E1 channels 1 and 31 are configured to insert BTPCM[x] data into these channels. BTCLK[x] is gapped so that it is only active for those channels with the associated IDLE_CHAN bit cleared (logic 0). The remaining channels (with IDLE_CHAN set) contain the per-channel idle code as defined in the associated Idle Code byte. When the DE bit is set to logic 0, then BTPCM[x] is sampled on the falling edge of BTCLK[x], and the functional timing is described by Figure 53 with the BTCLK[x] signal inverted during the active bytes.

Figure 55: - T1/E1 Transmit Clock Master : Clear Channel Mode



The Backplane Transmit Interface is configured for the Clock Master: Clear Channel mode by programming the CMODE bit of the BTIF Configuration register to logic 0 and the FDIS bit of the Transmit Framing and Bypass Options register to logic 1. BTPCM[x] is clocked in on the rising edge of the BTCLK[x] output. When the DE bit of the BTIF Configuration register is set to logic 0, then BTPCM[x] is sampled on the falling edge of BTCLK[x], and the functional timing is described with the BTCLK signal inverted.

Figure 56: - T1 Transmit Clock Slave: Full T1/E1 mode

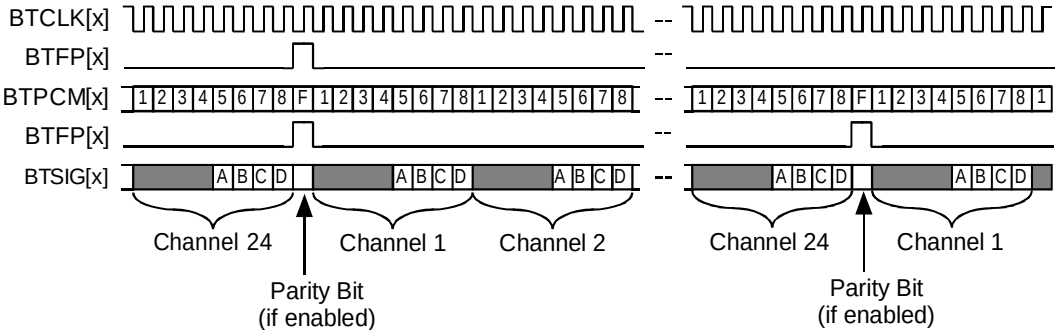
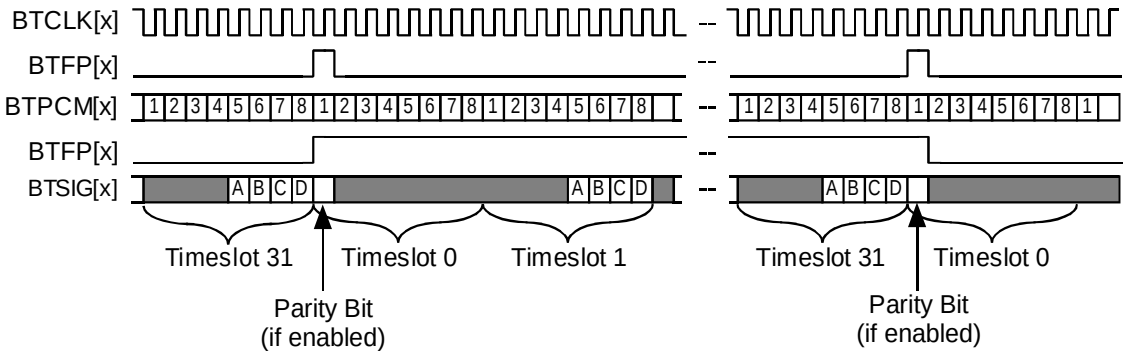


Figure 57: - E1 Transmit Clock Slave : Full T1/E1 Mode



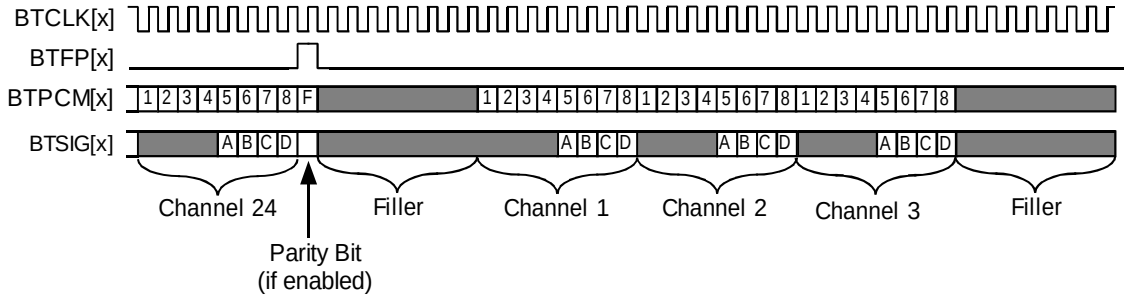
The Backplane Transmit Interface is configured for the Clock Slave: Full T1/E1 mode by programming the CMODE bit of the BTIF Configuration register to logic 1 and the FPMODE of the BTIF Frame Pulse Configuration register to logic 1. BTPCM[x] is clocked in on the active edge of BTCLK[x].

BTSIG[x] should carry the signaling bits for each channel in bits 5,6,7 and 8. These signaling bits will be inserted into the data stream by the T1 or E1 transmitter. If parity checking is enabled in T1 or E1 mode, a parity bit should be inserted on BTPCM[x] and BTSIG[x] in the first bit of each frame. The parity operates on all bits in the BTPCM[x] and BTSIG[x] streams, including the unused bits on BTSIG[x].

In T1 mode, Figure 56, the FPTYP bit is programmed to logic 1 in the BTIF Frame Pulse Configuration register, so that BTFP[x] must pulse once every 12 or 24 frames (for SF and ESF, respectively) on the first frame bit of the superframe. When the FPTYP bit is programmed to logic 0, the BTFP[x] input should pulse high to mark the F-bit of each frame.

In E1 mode, BTFP[x] may be chosen to indicate alignment of every frame or the composite CRC and Signaling multiframe alignment as shown in Figure 57, by programming the FPTYP bit in the BTIF Frame Pulse Configuration register.

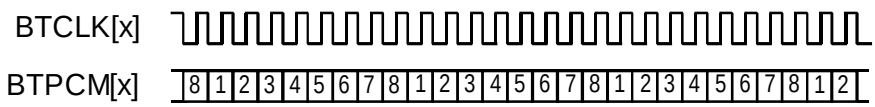
Figure 58: - T1 Transmit 2.048 MHz Clock Slave : Full T1/E1 Mode



The Backplane Transmit Interface is configured for the Clock Slave: Full T1/E1 Mode by programming the BTIF's CMODE and FPMODE register bits. The 2.048 MHz internally gapped clock mode is selected by programming RATE[1]=0 and RATE[0]=1 in the BTIF Configuration register. In Figure 58, BTFP[x] is configured for superframe alignment by writing FPTYP to logic 1 in the BTIF Frame Pulse Configuration register, so that the BTFP[x] input must pulse once every 12 or 24 frames (for SF and ESF, respectively) on the first F-bit of the multiframe to specify superframe alignment, instead of once every frame to specify frame alignment. If FPTYP is logic 0, the BTFP[x] input should pulse high to mark the F-bit of each frame.

BTSIG[x] should carry the signaling bits for each channel in bits 5,6,7 and 8; the signaling bits will be inserted into the data stream by the transmitter. If parity checking is enabled, a parity bit should be inserted on BTPCM[x] and BTSIG[x] in the first bit of each frame. The values of the BTPCM[x] and BTSIG[x] don't-care bits are not important, except that they will be used in the backplane parity check if it is enabled.

Figure 59: - T1/E1 Transmit Clock Slave : Clear Channel Mode

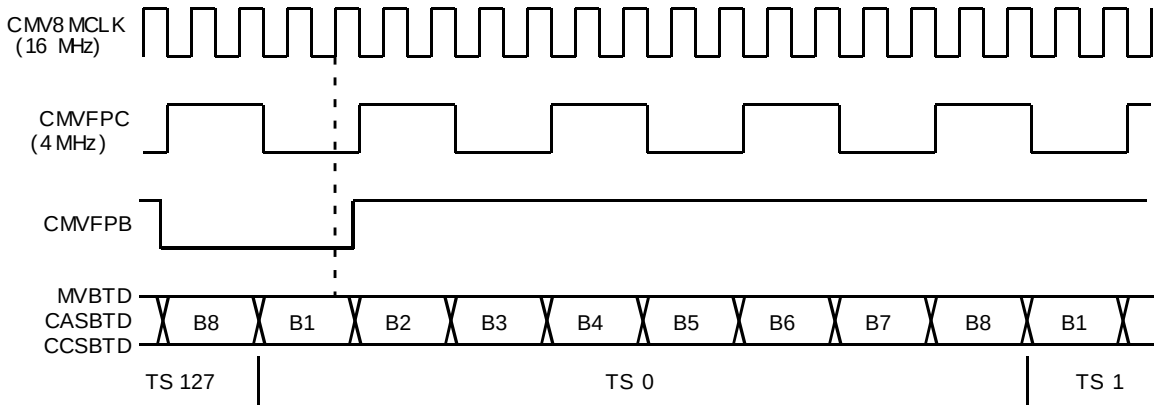


The Backplane Transmit Interface is configured for the Clock Slave: Clear Channel mode by programming FDIS=1 in the Transmit Framing and Bypass Options register. BTPCM[x] is clocked in on the rising edge of the BTCLK[x] input. When DE=0 in the BTIF Configuration register, BTPCM[x] is sampled on the falling edge of BTCLK[x], and the functional timing is described by Figure 59 with the BTCLK[x] signal inverted.

1.52 Backplane Transmit H-MVIP Link Timing

The timing relationship of the common 8M H-MVIP clock (CMV8MCLK), frame pulse clock (CMVFPC), data (MVBTD, CASBTD or CCSBTD) and frame pulse (CMVFPB) signals configured for 8.192 Mbit/s H-MVIP operation with a type 0 frame pulse is shown in Figure 60. The falling edges of each CMVFPC are aligned to a falling edge of the corresponding CMV8MCLK for 8.192 Mbit/s H-MVIP operation. The COMET-Quad samples CMVFPB low on the falling edge of CMVFPC and references this point as the start of the next frame. The COMET-Quad samples the data provided on MVBTD, CASBTD and CCSBTD at the ¾ point of the data bit using the rising edge of CMV8MCLK as indicated for bit 1 (B1) of timeslot 1 (TS 0) in Figure 60. B1 is the most significant bit and B8 is the least significant bit of each octet.

Figure 60: - Transmit 8.192 Mbit/s H-MVIP Link Timing



ABSOLUTE MAXIMUM RATINGS

Maximum ratings are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 74: - Absolute Maximum Ratings

Parameter	Symbol	Value	Units
Case Temperature under Bias		-40 to +85	°C
Storage Temperature	T_{ST}	-40 to +125	°C
Supply Voltage	V_{DD25}	-0.3 to + 3.5	V_{DC}

Parameter	Symbol	Value	Units
Case Temperature under Bias		-40 to +85	°C
Supply Voltage	All V_{DD} except V_{DD25}	-0.3 to + 4.6	V_{DC}
Voltage on Any Pin	V_{IN}		V_{DC}
Static Discharge Voltage		±1000	V
Latch-Up Current		±100	mA
DC Input Current	I_{IN}	±20	mA
Lead Temperature		+230	°C
Junction Temperature	T_J	+150	°C

D.C. CHARACTERISTICS

T_A = -40°C to +85°C, V_{DD33} = 3.3V ±5%, V_{DD25} = 2.5V ±0.2V
(Typical Conditions: T_A = 25°C, V_{DD33} = 3.3V, V_{DD25} = 2.5V)

Table 75: - D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VDD33	Power Supply	3.13	3.3	3.47	Volts	
VDD25	Power Supply	2.3	2.5	2.7	Volts	
VIL	Input Low Voltage	0		0.8	Volts	Guaranteed Input LOW Voltage
VIH	Input High Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
VOL	Output or Bidirectional Low Voltage	0	0.1	0.4	Volts	VDD = min, IOL = -4mA for D[7:0], BRCLK[1:4], BTCLK[1:4], and INTB and -2mA for others. Note 3
VOH	Output or Bidirectional High Voltage	2.4		VDD33	Volts	VDD = min, IOH = 4mA for D[7:0], BRCLK[1:4], BTCLK[1:4], and INTB and 2mA for others. Note 3
VT+	Reset Input High Voltage	2.0			Volts	TTL Schmidt
VT-	Reset Input Low Voltage			0.8	Volts	

Symbol	Parameter	Min	Typ	Max	Units	Conditions
VTH	Reset Input Hysteresis Voltage		TBD		Volts	
IILPU	Input Low Current	+10		+100	µA	VIL = GND. Notes 1, 3
IIHPU	Input High Current	-10		+10	µA	VIH = VDD. Notes 1, 3
IIL	Input Low Current	-10		+10	µA	VIL = GND. Notes 2, 3
IIH	Input High Current	-10		+10	µA	VIH = VDD. Notes 2, 3
CIN	Input Capacitance		5		pF	Excluding Package, Package Typically 2 pF
COUT	Output Capacitance		5		pF	Excluding Package, Package Typically 2 pF
CIO	Bidirectional Capacitance		5		pF	Excluding Package, Package Typically 2 pF
IDDOP1	Operating Current				mA	TBD
IDDOP2	Operating Current				mA	TBD

Notes on D.C. Characteristics:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
4. Typical values are given as a design aid. This product is not tested to the typical values given in the datasheet.

MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

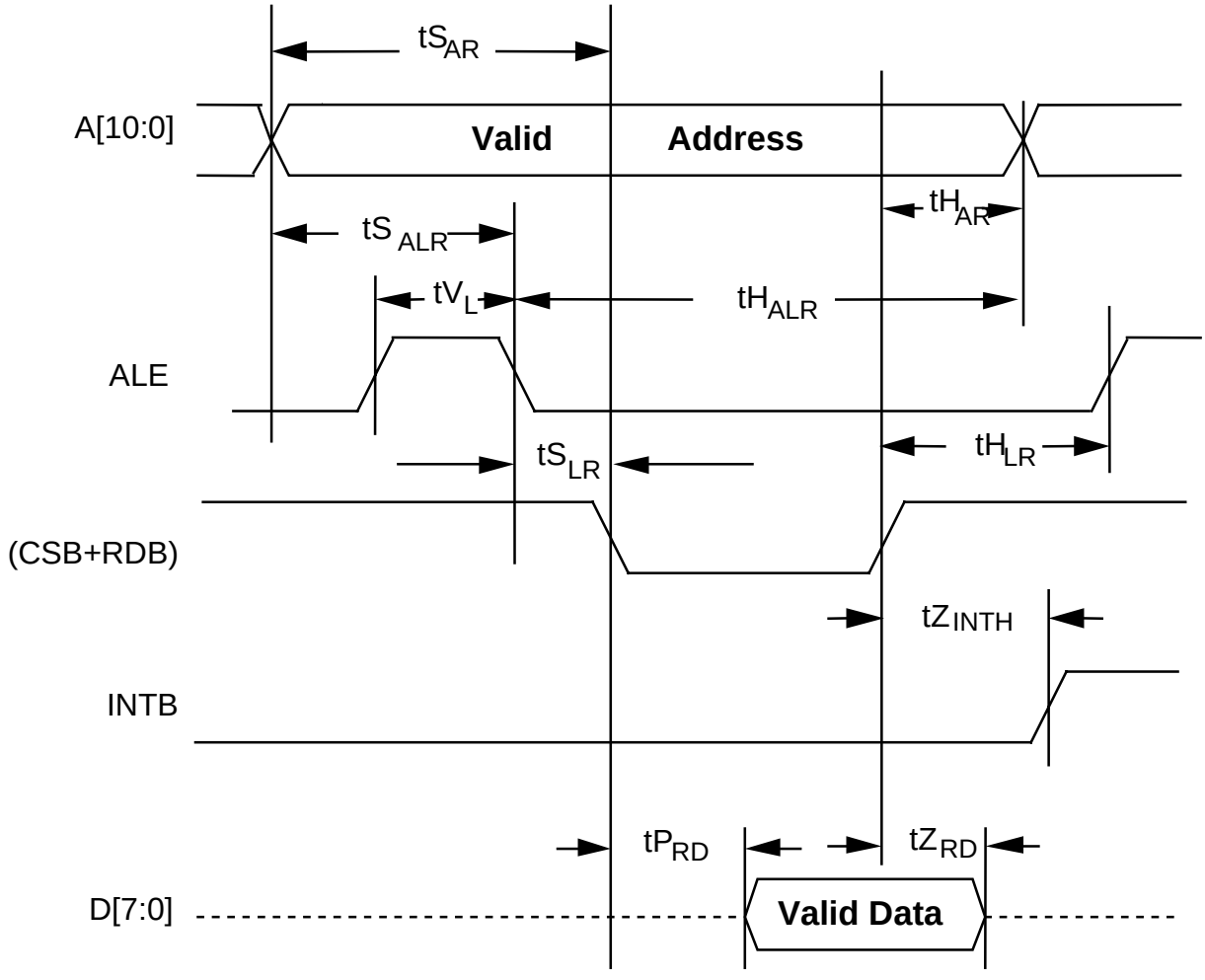
(T_A = -40°C to +85°C, V_{DD33} = 3.3V ±5%, V_{DD25} = 2.5V ±0.2V)

Table 76: - Microprocessor Interface Read Access

Symbol	Parameter	Min	Max	Units
tSAR	Address to Valid Read Set-up Time	10		ns
tHAR	Address to Valid Read Hold Time	5		ns
tSALR	Address to Latch Set-up Time	10		ns
tHALR	Address to Latch Hold Time	10		ns
tVL	Valid Latch Pulse Width	20		ns

Symbol	Parameter	Min	Max	Units
tSLR	Latch to Read Set-up	0		ns
tHLR	Latch to Read Hold	5		ns
tPRD	Valid Read to Valid Data Propagation Delay		70	ns
tZRD	Valid Read Negated to Output Tri-state		20	ns
tZINTH	Valid Read Negated to Output Tri-state		50	ns

Figure 61: - Microprocessor Interface Read Timing



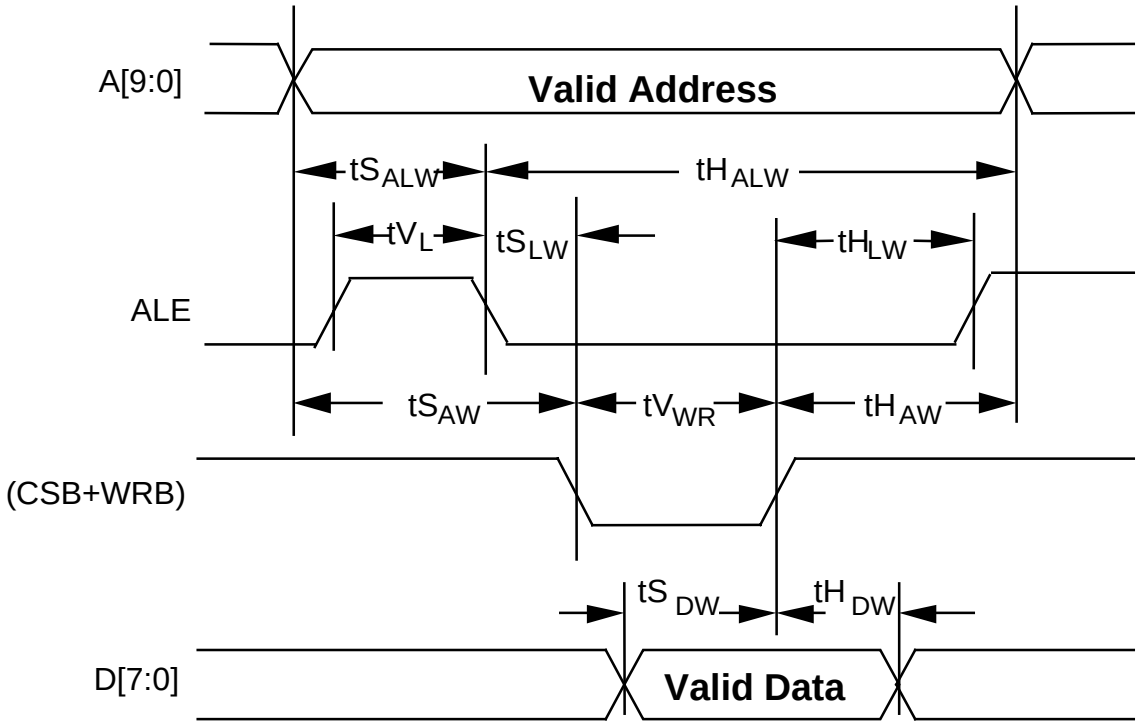
Notes on Microprocessor Interface Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 100 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALR, tHALR, tVL, and tSLR are not applicable.
5. Parameter tHAR is not applicable if address latching is used.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

Table 77: - Microprocessor Interface Write Access

Symbol	Parameter	Min	Max	Units
tSAW	Address to Valid Write Set-up Time	10		ns
tSDW	Data to Valid Write Set-up Time	20		ns
tSALW	Address to Latch Set-up Time	10		ns
tHALW	Address to Latch Hold Time	10		ns
tVL	Valid Latch Pulse Width	20		ns
tSLW	Latch to Write Set-up	0		ns
tHLW	Latch to Write Hold	5		ns
tHDW	Data to Valid Write Hold Time	5		ns
tHAW	Address to Valid Write Hold Time	5		ns
TVWR	Valid Write Pulse Width	40		ns

Figure 62: - Microprocessor Interface Write Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. In non-multiplexed address/data bus architectures, ALE should be held high so parameters tSALW, tHALW, tVL, tSLW and tHLW are not applicable.
3. Parameter tHAW is not applicable if address latching is used.
4. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.
5. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

COMET-Quad TIMING CHARACTERISTICS

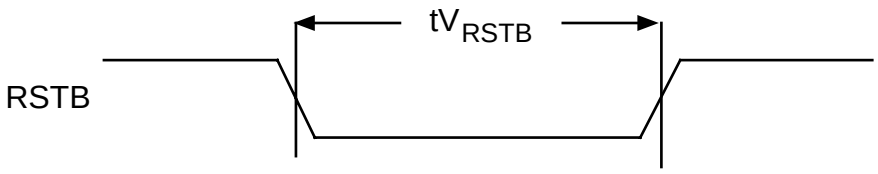
1.53 RSTB Timing

(T_A = -40°C to +85°C V_{DD33} = 3.3V ±5%, V_{DD25} = 2.5V ±0.2V)

Table 78: - RTSB Timing

Symbol	Description	Min	Max	Units
tVRSTB	RSTB Pulse Width	100		ns

Figure 63: - RSTB Timing

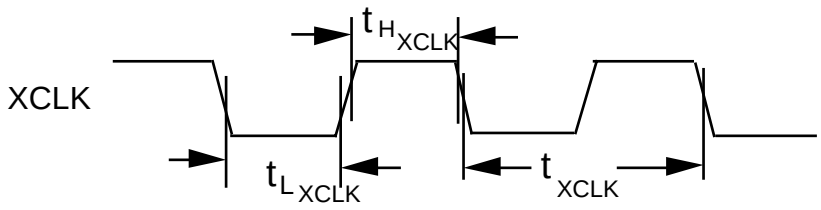


1.54 XCLK Input Timing

Table 79: - XCLK Input (Figure 64)

Symbol	Description	Min	Max	Units
t_{XCLK}	XCLK Frequency, typically 1.544MHz or 2.048 MHz ± 100ppm	1.543	2.049	MHz
tL_{XCLK}	XCLK Low Pulse Width[1]	160		ns
tH_{XCLK}	XCLK High Pulse Width[1]	160		ns

Figure 64: - XCLK Input Timing



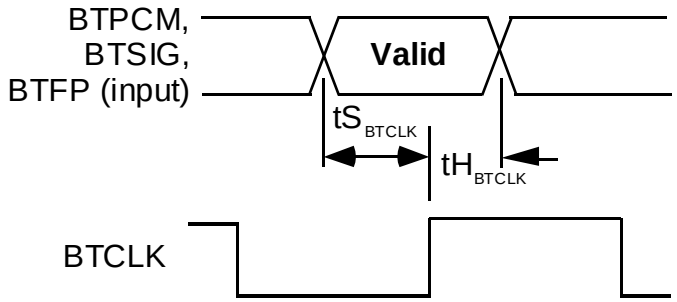
1.55 Transmit Backplane Interface (Figure 65, Figure 66)

(T_A = -40°C to +85°C, V_{DD33} = 3.3V ±5%, V_{DD25} = 2.5V ±0.2V)

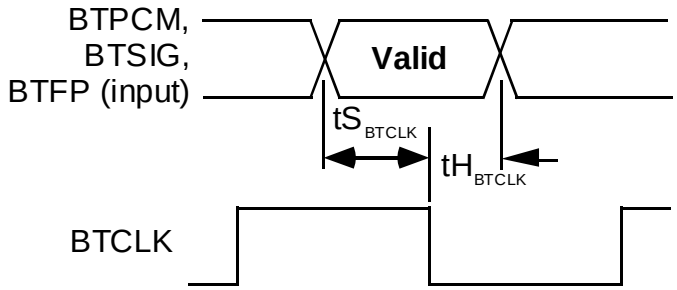
Table 80 - Transmit Backplane Interface

Symbol	Description	Min	Max	Units
	BTCLK Frequency (Nominally 1.544 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz or 16.384 MHz. Typically 1.544 MHz ± 130 ppm or 2.048 MHz ± 130 ppm)[2]	1.5	16.4	MHz
	BTCLK Duty Cycle[1]	35	65	%
t_{SBTCLK}	BTCLK to Backplane Input Set-up Time[3]	20		ns
t_{HBTCLK}	BTCLK to Backplane Input Hold Time[4]	20		ns
t_{PBTFP}	BTCLK to BTFP Output Propagation Delay[5, 6]	-20	50	ns

Figure 65 - Backplane Transmit Input Timing Diagram

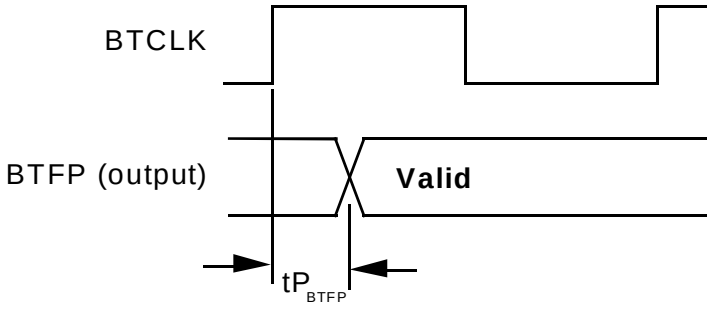


Inputs Sampled on Rising Edge

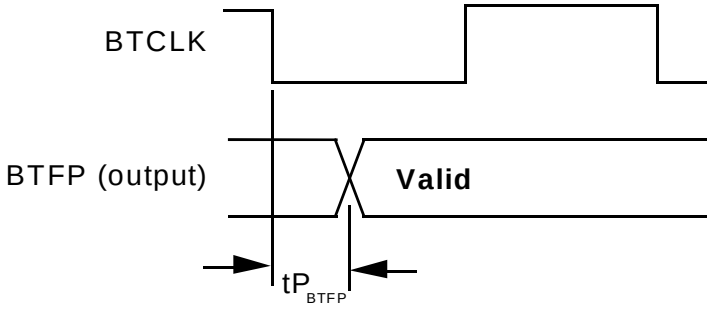


Inputs Sampled on Falling Edge

Figure 66 - Backplane Transmit Output Timing Diagram



Frame Pulse Output on Rising Edge



Frame Pulse Output on Falling Edge

1.56 Receive Backplane Interface (Figure 67, Figure 68)

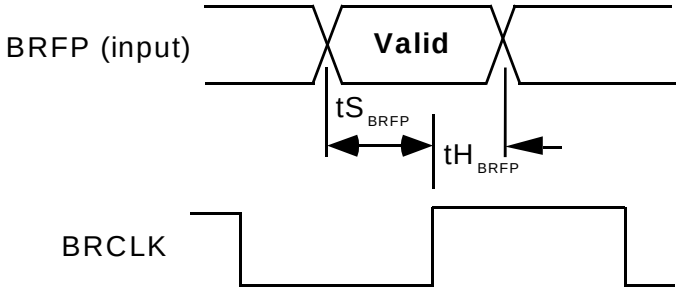
(T_A = -40°C to +85°C, V_{DD33} = 3.3V ±5%, V_{DD25} = 2.5V ±0.2V)

Table 81 - Receive Backplane Interface

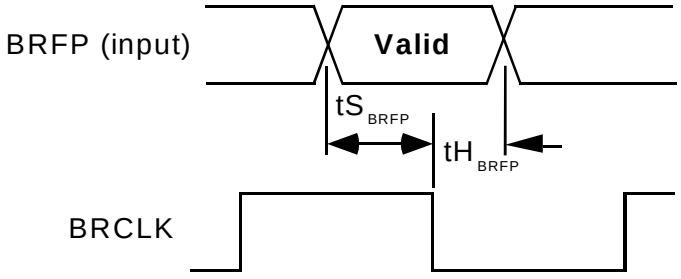
Symbol	Description	Min	Max	Units
	BRCLK Frequency (Nominally 1.544 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz or 16.384 MHz. Typically 1.544 MHz ± 130 ppm or 2.048 MHz ± 130 ppm)[2]	1.5	16.4	MHz
	BRCLK Duty Cycle[1]	35	65	%
$^tS_{BRFP}$	BRFP to BRCLK Input Set-up Time[3]	20		ns

Symbol	Description	Min	Max	Units
$^{t}H_{BRFP}$	BRFP to BRCLK Input Hold Time[4]	20		ns
$^{t}P_{BRCLK}$	BRCLK to Backplane Output Signals Propagation Delay[5,6]	-20	50	ns

Figure 67 - Backplane Receive Input Timing Diagram

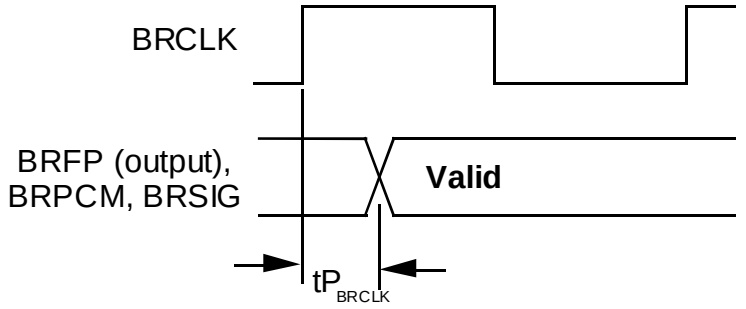


Frame Pulse Sampled on Rising Edge

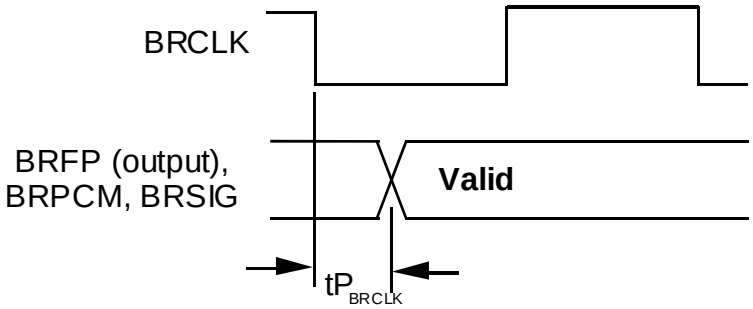


Frame Pulse Sampled on Falling Edge

Figure 68 - Backplane Receive Output Timing Diagram



Output on Rising Edge



Output on Falling Edge

Table 82: - H-MVIP Transmit Timing (Figure 69)

Symbol	Description	Min	Max	Units
	CMV8MCLK Frequency[8]	16.368	16.400	MHz
	CMV8MCLK Duty Cycle[1]	40	60	%
	CMVFPC Frequency[9]	4.092	4.100	MHz
	CMVFPC Duty Cycle[1]	40	60	%
tP_{MVC}	CMV8MCLK to CMVFPC skew	-10	10	ns
TS_{HMVED}	MVBTD, CASBTD, CCSBTD Set-Up Time[3]	5		ns
tH_{HMVED}	MVBTD, CASBTD, CCSBTD Hold Time[4]	5		ns

Symbol	Description	Min	Max	Units
TS_{MVFPB}	CMVFPB Set-Up Time[3]	5		ns
TH_{MVFPB}	CMVFPB Hold Time[4]	5		ns

Figure 69: - H-MVIP Transmit Data & Frame Pulse Timing

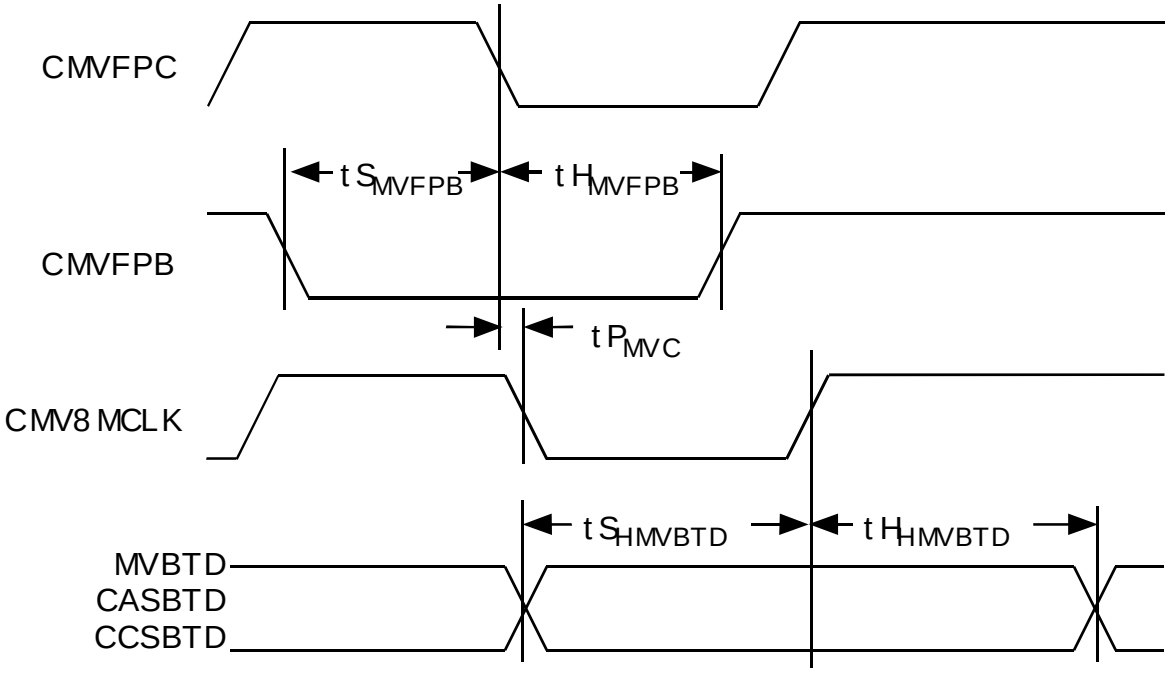


Table 83: - H-MVIP Receive Timing (Figure 70)

Symbol	Description	Min	Max	Units
tP_{HMVBRD}	CMV8MCLK Low to MVBRD, CASBRD, CCSBRD Valid[5,6]	5	25	ns

Figure 70: - H-MVIP Receive Data Timing

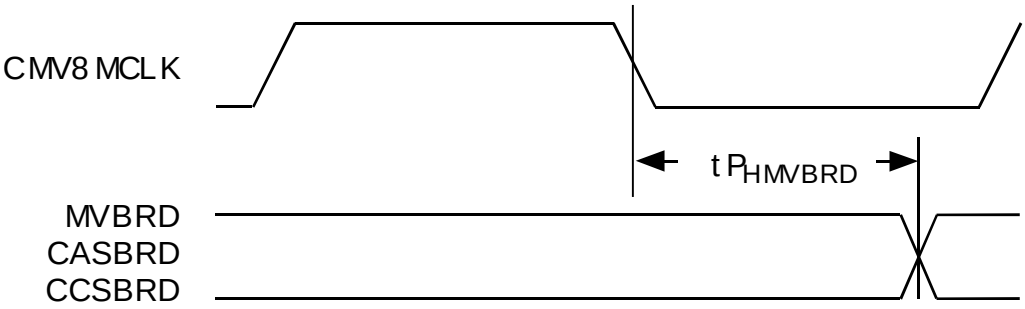


Table 84: - Transmit Line Interface Timing (Figure 71)

Symbol	Description	Min	Max	Units
	CTCLK Frequency (when used for TJAT Reference), typically 1.544 MHz ±130 ppm for T1 operation or 2.048 MHz ±50 ppm for E1 operation[2,10]	1.5	2.1	MHz
t_{HCTCLK}	CTCLK High Duration[1,10] (when used for TJAT Reference)	160		ns
t_{LCTCLK}	CTCLK Low Duration[1,10] (when used for TJAT Reference)	160		ns

Figure 71: - Transmit Line Interface Timing

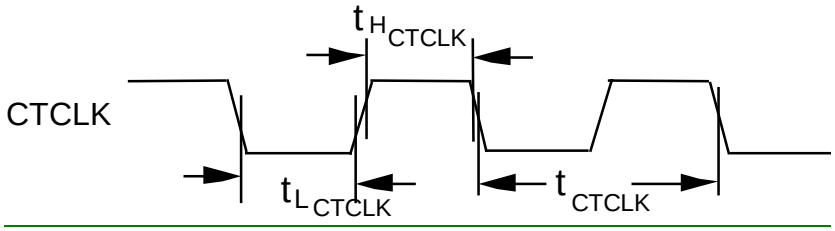
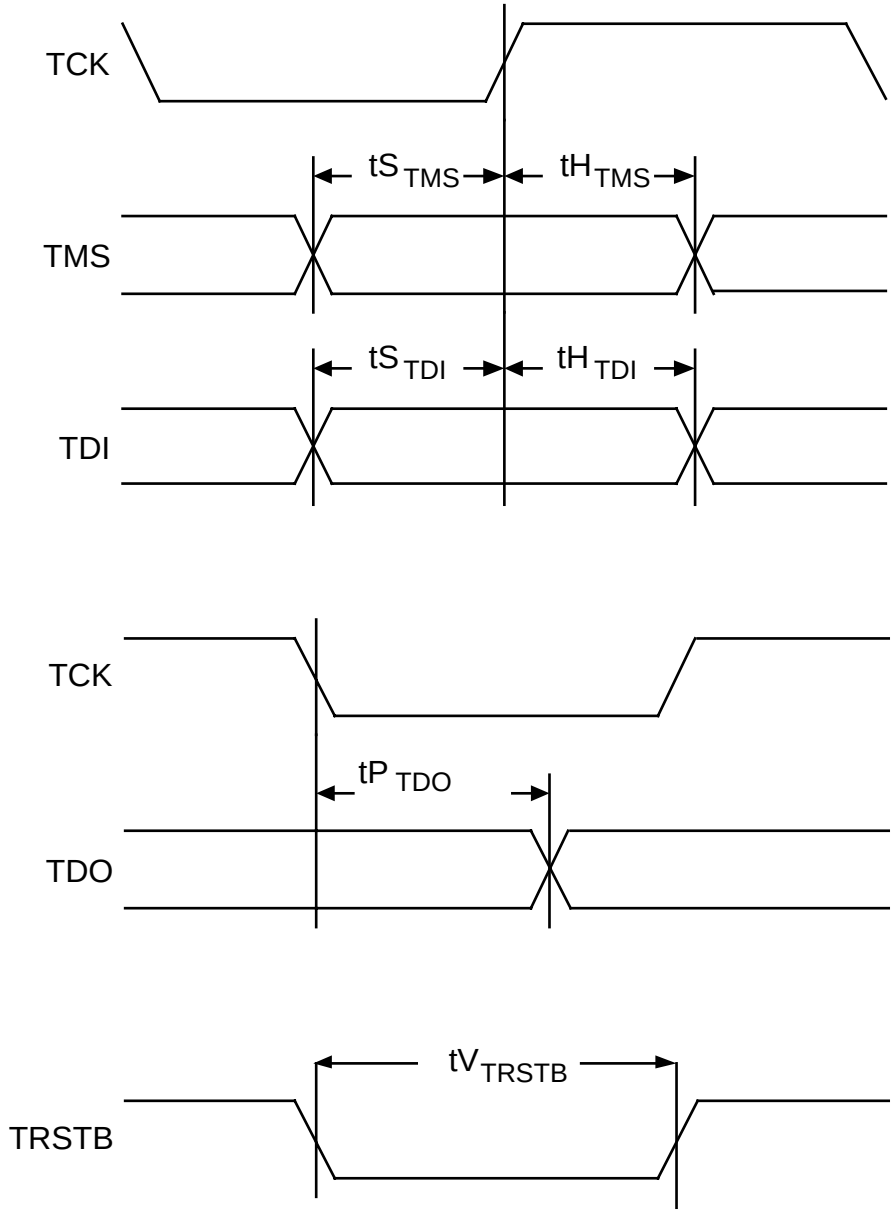


Table 85: - JTAG Port Interface

Symbol	Description	Min	Max	Units
	TCK Frequency		1	MHz
	TCK Duty Cycle	40	60	%
t_{STMS}	TMS Set-up time to TCK	50		ns

Symbol	Description	Min	Max	Units
t_{HTMS}	TMS Hold time to TCK	50		ns
t_{STDI}	TDI Set-up time to TCK	50		ns
t_{HTDI}	TDI Hold time to TCK	50		ns
t_{PTDO}	TCK Low to TDO Valid	2	50	ns
t_{VTRSTB}	TRSTB Pulse Width	100		ns

Figure 72: - JTAG Port Interface Timing



Notes on COMET-Quad Timing:

1. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

2. BTCLK and BRCLK can be a jittered clock signal subject to the minimum and maximum instantaneous frequencies and duty cycles shown. These specifications correspond to nominal XCLK input frequencies.

3. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

4. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

6. Maximum output propagation delays are measured with a 50 pF load on the output.

7. XCLK accuracy is ± 100 ppm.

8. Measured between any two CMV8MCLK falling edges.

9. Measured between any two CMVFPC falling edges.

10. CTCLK[x] can be a jittered clock signal subject to the minimum high and low durations tH_{CTCLK}, tL_{CTCLK}. These durations correspond to nominal XCLK input frequency.

ORDERING AND THERMAL INFORMATION

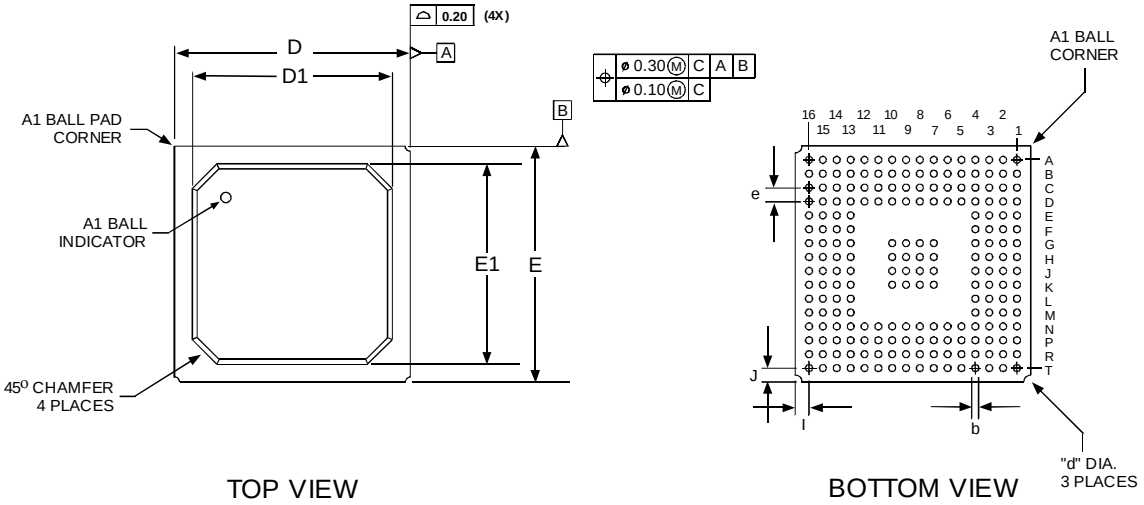
Table 86: - Ordering and Thermal Information

Part No.	Description
PM4354-PI	208 Plastic Ball Grid Array (PBGA)

Table 87: - Thermal Information

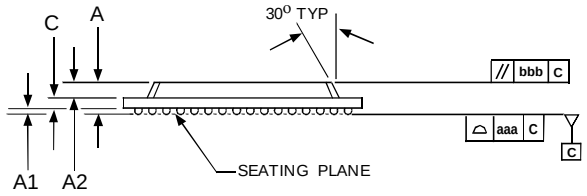
Part No.	Case Temperature	Theta J-A	Theta J-C
PM4354-PI	-40°C to 85°C		

MECHANICAL INFORMATION



TOP VIEW

BOTTOM VIEW



SIDE VIEW

NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES COPLANARITY.
3) DIMENSION bbb DENOTES PARALLEL.

PACKAGE TYPE : 208 PLASTIC BALL GRID ARRAY - PBGA																	
BODY SIZE : 17 x 17 x 1.76 MM (4 layer)																	
Dim.	A (2 layer)	A (4 layer)	A1	A2	D	D1	C (2 layer)	C (4 layer)	E	E1	l	J	b	d	e	aaa	bbb
Min	1.35	1.55	0.30	0.75	-	14.50	0.30	0.50	-	14.50	-	-	0.40	-	-	-	-
Nom.	1.56	1.76	0.40	0.80	17.00	15.00	0.36	0.56	17.00	15.00	1.00	1.00	0.50	1.00	1.00	-	-
Max.	1.75	1.97	0.50	0.85	-	15.70	0.40	0.62	-	15.70	-	-	0.60	-	-	0.15	0.35

NOTES

NOTES

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