

IS61C512

64K x 8 HIGH-SPEED CMOS STATIC RAM

FEATURES

- Pin compatible with 128K x 8 devices
- High-speed access time: 15, 20, 25, 35 ns
- Low active power: 500 mW (typical)
- Low standby power
 - 250 μ W (typical) CMOS standby
- Output Enable (\overline{OE}) and two Chip Enable ($\overline{CE1}$ and CE2) inputs for ease in applications
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V ($\pm 10\%$) power supply

DESCRIPTION

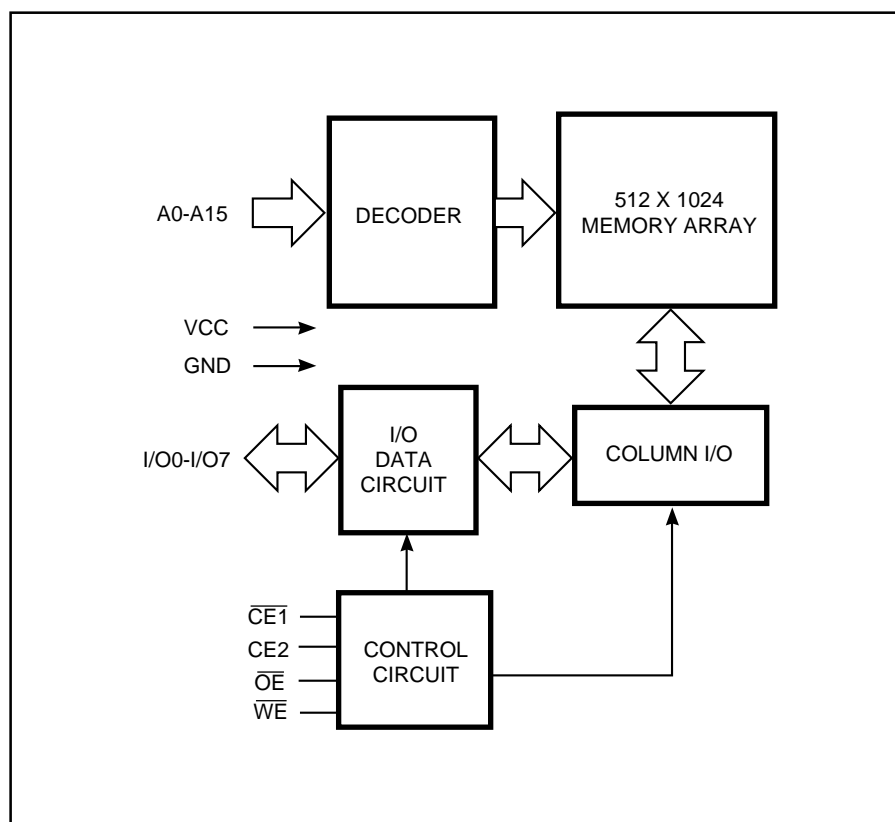
The ICSI IS61C512 is a very high-speed, low power, 65,536 word by 8-bit CMOS static RAMs. They are fabricated using ICSI's high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE1}$ is HIGH or CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 1 mW (typical) with CMOS input levels.

Easy memory expansion is provided by using two Chip Enable inputs, $\overline{CE1}$ and CE2. The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory.

The IS61C512 is available in 32-pin 300mil DIP, SOJ and 8*20mm TSOP-1 packages.

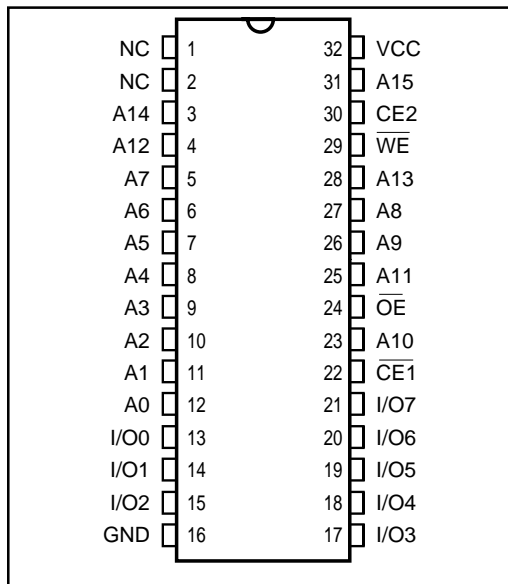
FUNCTIONAL BLOCK DIAGRAM



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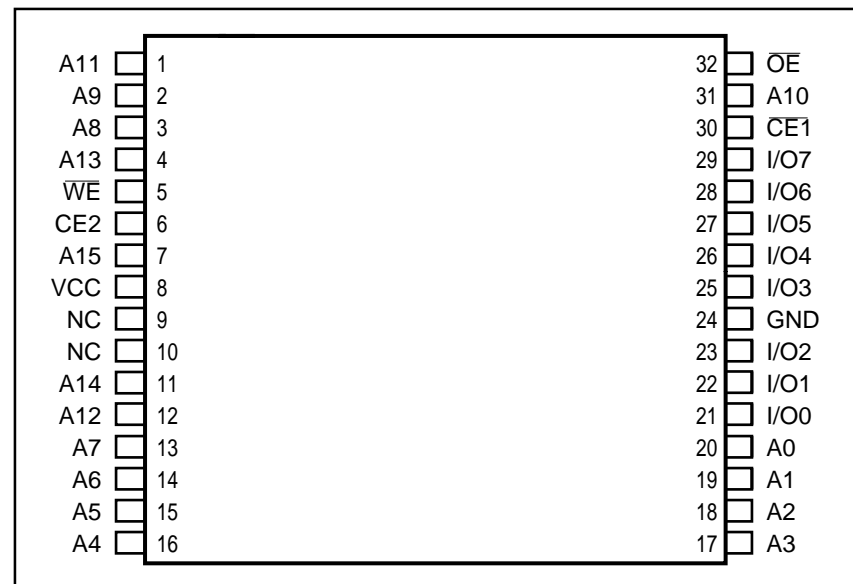
PIN CONFIGURATION

32-Pin DIP and SOJ



PIN CONFIGURATION

32-Pin TSOP-1



PIN DESCRIPTIONS

| | |
|-----------|---------------------|
| A0-A15 | Address Inputs |
| CE1 | Chip Enable 1 Input |
| CE2 | Chip Enable 2 Input |
| OE | Output Enable Input |
| WE | Write Enable Input |
| I/O0-I/O7 | Input/Output |
| Vcc | Power |
| GND | Ground |

TRUTH TABLE

| Mode | WE | CE1 | CE2 | OE | I/O Operation | Vcc Current |
|-----------------|----|-----|-----|----|---------------|-------------|
| Not Selected | X | H | X | X | High-Z | Isb1, Isb2 |
| (Power-down) | X | X | L | X | High-Z | Isb1, Isb2 |
| Output Disabled | H | L | H | H | High-Z | Icc1, Icc2 |
| Read | H | L | H | L | DOUT | Icc1, Icc2 |
| Write | L | L | H | X | DIN | Icc1, Icc2 |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|--------|--------------------------------------|--------------|------|
| VTERM | Terminal Voltage with Respect to GND | -0.5 to +7.0 | V |
| TBIAS | Temperature Under Bias | -10 to +85 | °C |
| TSTG | Storage Temperature | -65 to +150 | °C |
| PT | Power Dissipation | 1.5 | W |
| IOUT | DC Output Current (LOW) | 20 | mA |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Industrial | -40°C to +85°C | 5V ± 10% |

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|-----------------|----------------------------------|---|------|-----------------------|------|
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -4.0 mA | 2.4 | — | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 8.0 mA | — | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.2 | V _{CC} + 0.5 | V |
| V _{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{CC} | -2 | 2 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{CC} , Outputs Disabled | -2 | 2 | μA |

Notes:

1. V_{IL} = -3.0V for pulse width less than 10 ns.

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | -15 ns | | -20 ns | | -25 ns | | -35 ns | | Unit | |
|------------------|--|---|--------|------|--------|------|--------|------|--------|------|------|----|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| I _{CC1} | V _{CC} Operating Supply Current | V _{CC} = Max., | Com. | — | 70 | — | 70 | — | 70 | — | 70 | mA |
| | | I _{OUT} = 0 mA, f = 0 | Ind. | — | — | — | 90 | — | 90 | — | 90 | |
| I _{CC2} | V _{CC} Dynamic Operating Supply Current | V _{CC} = Max., | Com. | — | 125 | — | 115 | — | 105 | — | 90 | mA |
| | | I _{OUT} = 0 mA, f = f _{MAX} | Ind. | — | — | — | 135 | — | 125 | — | 115 | |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{CC} = Max., | Com. | — | 25 | — | 25 | — | 25 | — | 25 | mA |
| | | V _{IN} = V _{IH} or V _{IL} CE1 ≥ V _{IH} or CE2 ≤ V _{IL} , f = 0 | Ind. | — | — | — | 30 | — | 30 | — | 30 | |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{CC} = Max., | Com. | — | 750 | — | 750 | — | 750 | — | 750 | μA |
| | | CE1 ≥ V _{CC} - 0.2V, CE2 ≤ 0.2V, V _{IN} ≥ V _{CC} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Ind. | — | — | — | 1 | — | 1 | — | 1 | |

Notes:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE^(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 5 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 7 | pF |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

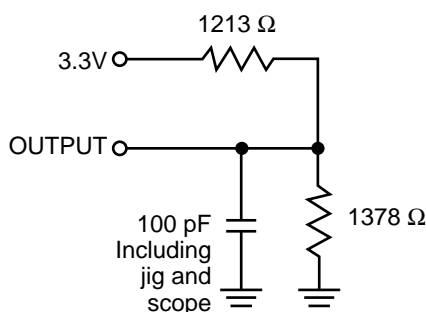
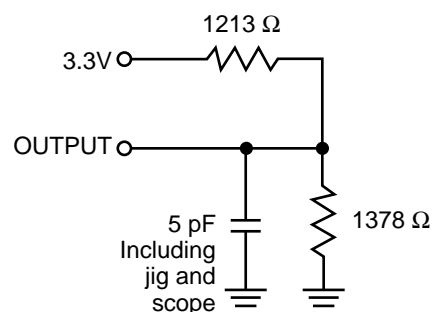
| Symbol | Parameter | -15 ns | | -20 ns | | -25 ns | | -35 ns | | Unit |
|-------------------|--|--------|------|--------|------|--------|------|--------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{RC} | Read Cycle Time | 15 | — | 20 | — | 25 | — | 35 | — | ns |
| t_{AA} | Address Access Time | — | 15 | — | 20 | — | 25 | — | 35 | ns |
| t_{OHA} | Output Hold Time | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| t_{ACE1} | $\overline{CE1}$ Access Time | — | 15 | — | 20 | — | 25 | — | 35 | ns |
| t_{ACE2} | CE2 Access Time | — | 15 | — | 20 | — | 25 | — | 35 | ns |
| t_{DOE} | \overline{OE} Access Time | — | 7 | — | 8 | — | 9 | — | 12 | ns |
| $t_{LZOE}^{(2)}$ | \overline{OE} to Low-Z Output | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{HZOE}^{(2)}$ | \overline{OE} to High-Z Output | 0 | 6 | 0 | 9 | 0 | 10 | 0 | 12 | ns |
| $t_{LZCE1}^{(2)}$ | $\overline{CE1}$ to Low-Z Output | 2 | — | 3 | — | 3 | — | 3 | — | ns |
| $t_{LZCE2}^{(2)}$ | CE2 to Low-Z Output | 2 | — | 3 | — | 3 | — | 3 | — | ns |
| $t_{HZCE}^{(2)}$ | $\overline{CE1}$ or CE2 to High-Z Output | 0 | 8 | 0 | 9 | 0 | 10 | 0 | 12 | ns |
| $t_{PU}^{(3)}$ | $\overline{CE1}$ or CE2 to Power-Up | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{PD}^{(3)}$ | $\overline{CE1}$ or CE2 to Power-Down | — | 12 | — | 18 | — | 20 | — | 20 | ns |

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

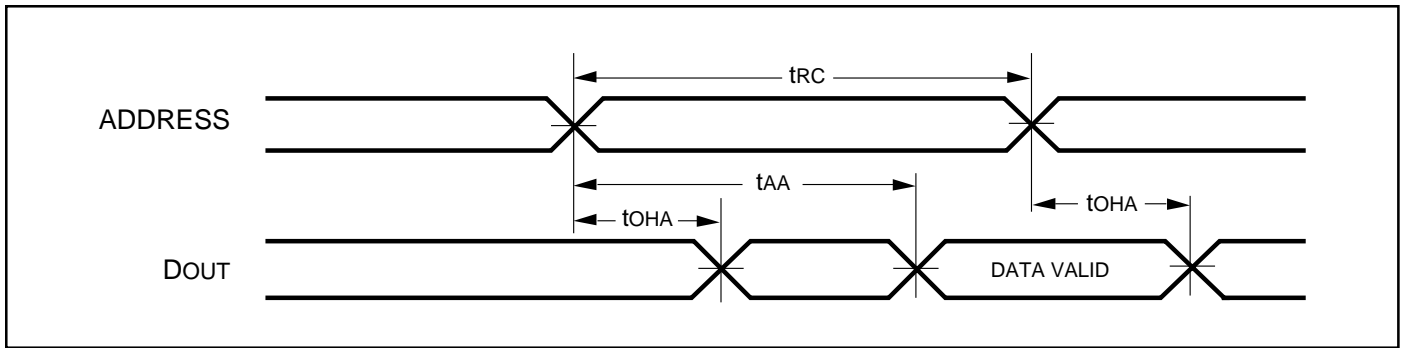
AC TEST CONDITIONS

| Parameter | Unit |
|---|-----------------------|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 3 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1a and 1b |

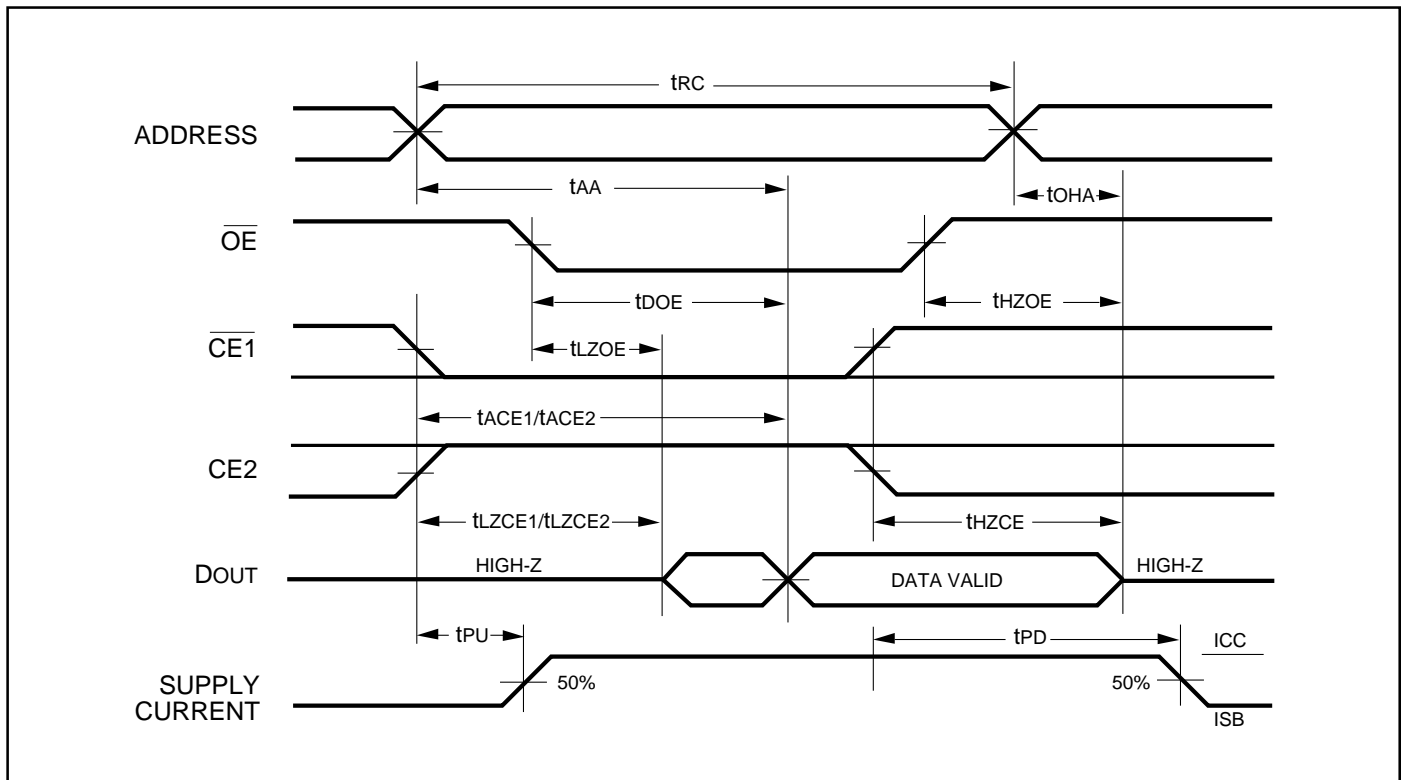
AC TEST LOADS

Figure 1a.

Figure 1b.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2)



READ CYCLE NO. 2^(1,3)



Notes:

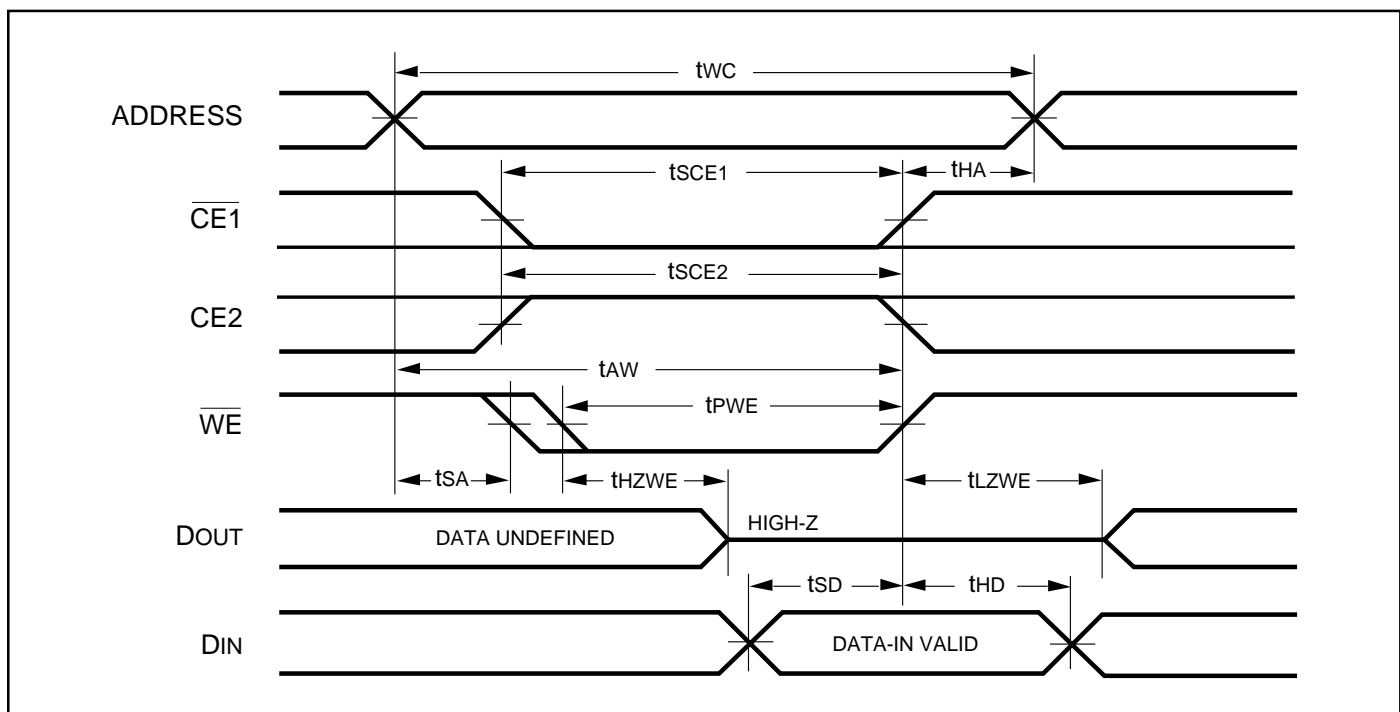
1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , $\overline{CE1} = V_{IL}$, $CE2 = V_{IH}$.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and $CE2$ HIGH transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

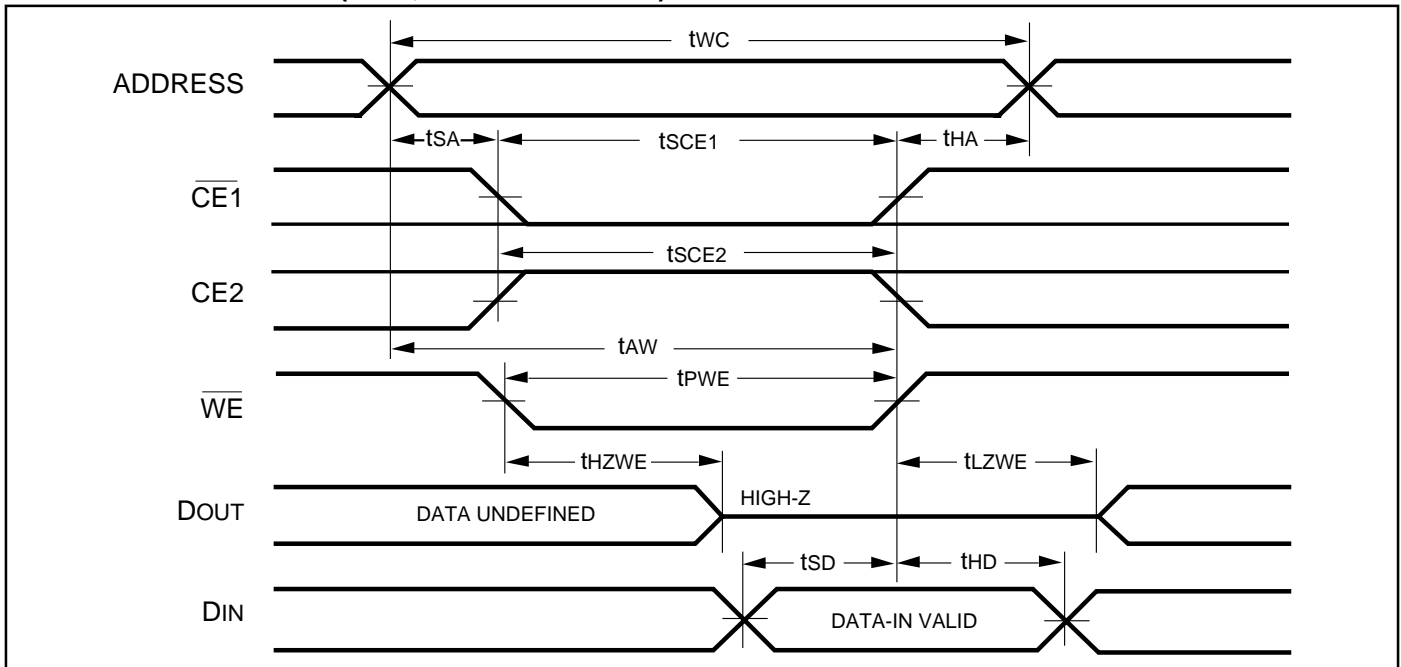
| Symbol | Parameter | -15 ns | | -20 ns | | -25 ns | | -35 ns | | Unit |
|------------------|--------------------------------------|--------|------|--------|------|--------|------|--------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{WC} | Write Cycle Time | 15 | — | 20 | — | 25 | — | 35 | — | ns |
| t_{SCE1} | $\overline{CE1}$ to Write End | 12 | — | 15 | — | 20 | — | 30 | — | ns |
| t_{SCE2} | CE2 to Write End | 12 | — | 15 | — | 20 | — | 30 | — | ns |
| t_{AW} | Address Setup Time to Write End | 12 | — | 15 | — | 20 | — | 30 | — | ns |
| t_{HA} | Address Hold from Write End | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t_{SA} | Address Setup Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{PWE}^{(4)}$ | \overline{WE} Pulse Width | 10 | — | 12 | — | 15 | — | 20 | — | ns |
| t_{SD} | Data Setup to Write End | 8 | — | 10 | — | 12 | — | 15 | — | ns |
| t_{HD} | Data Hold from Write End | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{HZWE}^{(2)}$ | \overline{WE} LOW to High-Z Output | — | 7 | — | 10 | — | 12 | — | 8 | ns |
| $t_{LZWE}^{(2)}$ | \overline{WE} HIGH to Low-Z Output | 2 | — | 2 | — | 2 | — | 2 | — | ns |

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1a.
2. Tested with the load in Figure 1b. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. Tested with \overline{OE} HIGH.

AC WAVEFORMS
WRITE CYCLE NO. 1 (\overline{WE} Controlled)^(1,2)


WRITE CYCLE NO. 2 ($\overline{CE1}$, CE2 Controlled)^(1,2)



Notes:

1. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
2. I/O will assume the High-Z state if \overline{OE} = HIGH.

ORDERING INFORMATION: IS61C512**Commercial Range: 0°C to + 70°C**

| Speed (ns) | Order Part No. | Package |
|------------|----------------|---------------|
| 15 | IS61C512-15J | 300mil SOJ |
| 15 | IS61C512-15N | 300mil DIP |
| 15 | IS61C512-15T | 8*20mm TSOP-1 |
| 20 | IS61C512-20J | 300mil SOJ |
| 20 | IS61C512-20N | 300mil DIP |
| 20 | IS61C512-20T | 8*20mm TSOP-1 |
| 25 | IS61C512-25J | 300mil SOJ |
| 25 | IS61C512-25N | 300mil DIP |
| 25 | IS61C512-25T | 8*20mm TSOP-1 |
| 35 | IS61C512-35J | 300mil SOJ |
| 35 | IS61C512-35N | 300mil DIP |
| 35 | IS61C512-35T | 8*20mm TSOP-1 |

ORDERING INFORMATION: IS61C512**Industrial Range: -40°C to + 85°C**

| Speed (ns) | Order Part No. | Package |
|------------|----------------|---------------|
| 15 | IS61C512-15JI | 300mil SOJ |
| 15 | IS61C512-15NI | 300mil DIP |
| 15 | IS61C512-15TI | 8*20mm TSOP-1 |
| 20 | IS61C512-20JI | 300mil SOJ |
| 20 | IS61C512-20NI | 300mil DIP |
| 20 | IS61C512-20TI | 8*20mm TSOP-1 |
| 25 | IS61C512-25JI | 300mil SOJ |
| 25 | IS61C512-25NI | 300mil DIP |
| 25 | IS61C512-25TI | 8*20mm TSOP-1 |
| 35 | IS61C512-35JI | 300mil SOJ |
| 35 | IS61C512-35NI | 300mil DIP |
| 35 | IS61C512-35TI | 8*20mm TSOP-1 |

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