Dual Ultra-Low V_{os} Matched Operational Amplifier

OP207

1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein.

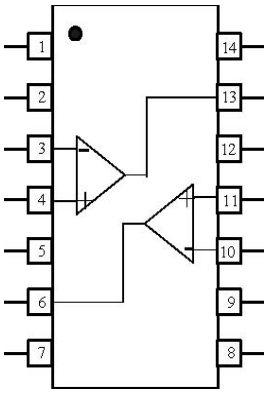
The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification http://www.analog.com/aerospace

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at www.analog.com/OP207

2.0 Part Number. The complete part number(s) of this specification follow:

Part Number	Description
OP207-903Y	Dual Ultra-Low Vos Matched Operational Amplifier

Letter	Descriptive designator	Case Outline (Lead Finish per MIL-PRF-38535)
Y	GDIP1-T14	14-Lead ceramic dual-in-line package (CERDIP)



14	V+ (A)
13	OUT (A)
12	V- (A)
11	+IN (B)
10	-IN (B)
9	NULL (B)
8	NULL (B)
7	V+ (B)
6	OUT (B)
5	V- (B)
4	+IN (A)
3	-IN (A)
2	NULL (A)
1	NULL (A)

NOTES:

1. Device may be operated even if insertion is reversed; this is due to inherent symmetry of pin locations of amplifiers A and B
2. V-(A) and V-(B) are internally connected via substrate resistance

Figure 1 - Terminal connections.

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3.0 Absolute Maximum Ratings. (T_A = 25°C, unless otherwise noted)

Supply Voltage.....±22V
Power Dissipation 500mW
Differential Input Voltage .....±30V
Input Voltage (Note 1) .....±22V
Output Short-Circuit Duration .....Indefinite
Operating Temperature Range .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (Soldering, 60 sec.) .....+300°C

NOTES:
For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltages.

3.1 Thermal Characteristics:

Thermal Resistance, CERDIP (Y) Package
Junction-to-Case (ΘJC) = 29°C/W Max
Junction-to-Ambient (ΘJA) = 91°C/W Max

4.0 Electrical Table:

Table I

Parameter See notes at end of table	Symbol	Conditions Note 1	Sub-group	Limit Min	Limit Max	Units
Input Offset Voltage	V_{OS}		1		100	µV
			2, 3		230	
		M, D, L, R 3/	1		500	
Average Input Offset Voltage Drift 4/	TCV_{OS}	TA = -55°C, +25°C, +125°C	1, 2, 3		1.3	µV/°C
Input Offset Current	I_{OS}		1		2.8	nA
			2, 3		5.6	
		M, D, L, R 3/	1		25	
Input Bias Current	I_B		1		±3.0	
			2, 3		±5.6	
		M, D, L, R 3/	1		±125	
Input Voltage Range 4/	IVR	Note 2	1, 2, 3	±13		V
Common-Mode Rejection Ratio 4/	CMRR	VCM = ±13V	1	106		dB
			2, 3	103		
Power Supply Rejection Ratio 4/	PSRR	VS = ±3V to ±18V	1		20	µV/V
			2, 3		32	
Output Voltage Swing 4/	V_O	RL = 10KΩ	4	±12.5		V
		RL = 2KΩ	4, 5, 6	±12		
		RL = 1KΩ	4	±10		
Large Signal Voltage Gain	A_{VO}	VO = ± 10V, RL = 2KΩ	4	200		V/mV
			5, 6	150		
		M, D, L, R 3/	4	100		
Power Supply Current	I_{SY}	No Load, Both Amplifiers	1		8	mA
		M, D, L, R 3/	1		8	
Input Noise Voltage 4/	e_n	f_O = 1Hz to 100 Hz	7		150	nV_{RMS}
Input Noise Current 4/	i_n	f_O = 1Hz to 100 Hz	7		8	pA_{RMS}
Offset Adjustment Range 4/	V_{OS}adj+	Rp = 20KΩ	1	0.5		mV
	V_{OS}adj-	Rp = 20KΩ	1		-0.5	
Input Offset Voltage Match 4/	ΔVOS		1		90	µV
			2, 3		180	
Average Non- Inverting Bias Current 4/	ΔIB+		1		±3.5	nA
			2, 3		±6.0	
Non-Inverting Offset Current 4/	ΔIOS+		1		±3.5	
			2, 3		±6.5	
Inverting Offset Current 4/	ΔIOS-		1		±3.5	
			2, 3		±6.5	
Common Mode Rejection Ratio Match 4/	ΔCMRR		1	103		dB
			2, 3	100		
Power Supply Rejection Ratio Match 4/	ΔPSRR	V_S = ±3V to ±18V	1		32	µV/V
			2, 3		51	
Output Short Circuit Current 4/	I_{SC}+		1	5	58	mA
	I_{SC}-		1	-55	-5	
Channel Separation 4/	CS		4	126		dB

TABLE I NOTES:

1/ V_S = ±15V, R_S = 50 ohm, unless otherwise specified

2/ I_{VR} is defined as the V_{CM} range used for the CMRR test.

3/ Post irradiation limit. Subgroup 1 parameters without limit are read and recorded but not guaranteed.

4/ Not tested post irradiation.

4.1 Electrical Test Requirements:

Table II	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1
Final Electrical Parameters	1, 2, 3, 4, 5, 6, 7 1/ 2/
Group A Test Requirements	1, 2, 3, 4, 5, 6
Group C end-point electrical parameters	1 2/
Group D end-point electrical parameters	1
Group E end-point electrical parameters	1

Notes:
1/ PDA applies to subgroup 1. VOS and delta's excluded from PDA.
2/ See table III for delta limits.

4.2 Table III. Burn-in test delta limits.

Table III				
TEST TITLE	BURN-IN ENDPOINT	LIFETEST ENDPOINT	DELTA LIMIT	UNITS
V_{OS}	±100	±175	±75	µV
$\pm I_B$	±3	±4	±1	nA

5.0 Life Test/Burn-In Circuit:

5.1 HTRB is not applicable for this drawing.
5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B (see figure 2).
5.3 Steady state life test is per MIL-STD-883 Method 1005, test condition B.

Rev	Description of Change	Date
A	Initiate	Mar. 28, 2000
B	Update web address. Correct PSRR units from V/μV to μV/V. Table I: reference to note 4 deleted, note 4 not in datasheet. Symbol for Inverting offset current should be Δ IOS-. Table II, note 1 add "VOS and delta's excluded from PDA". Update Table III with Life test end-point = datasheet + delta.	Mar. 19, 2002
C	Update web address. Add note 4 to indicate parameters not tested post irradiation	May 13, 2003
D	Delete burn-in and radiation bias circuits	Aug. 5, 2003
E	Updated header/footer & added to scope description, and deleted OP207R903Y – part is no longer offered.	Feb. 14, 2008