19-2413; Rev 6; 8/06

2-Wire-Interfaced, 2.5V to 5.5V, 20-Port or 28-Port I/O Expander

General Description

The MAX7300 compact, serial-interfaced, I/O expansion peripheral provides microprocessors with up to 28 ports. Each port is individually user configurable to either a logic input or logic output.

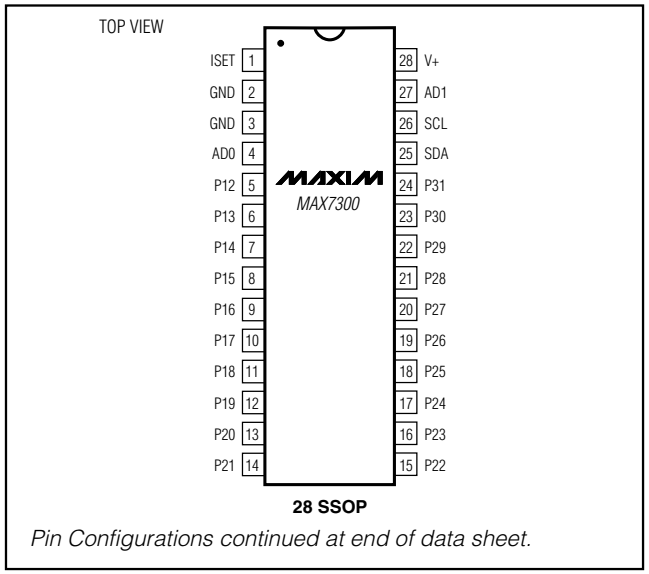
Each port can be configured as either a push-pull logic output capable of sinking 10mA and sourcing 4.5mA, or a Schmitt logic input with optional internal pullup. Seven ports feature configurable transition detection logic, which generates an interrupt upon change of port logic level. The MAX7300 is controlled through an I²C*-compatible 2-wire serial interface, and uses four-level logic to allow 16 I²C addresses from only two select pins.

The MAX7300AAX and MAX7300ATL have 28 ports and are available in 36-pin SSOP and 40-pin thin QFN packages, respectively. The MAX7300AAI and MAX7300ATI have 20 ports and are available in 28-pin SSOP and thin QFN packages. For an SPI-interfaced version, refer to the MAX7301 data sheet. For a pin-compatible port expander with additional 24mA constant-current LED drive capability, refer to the MAX6956 data sheet.

Applications

White Goods
Automotive
Industrial Controllers
System Monitoring

Pin Configurations



28 SSOP

Pin Configurations continued at end of data sheet.

*Purchase of I²C components from Maxim Integrated Products, Inc., or one of its sublicensed Associated Companies, conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

Features

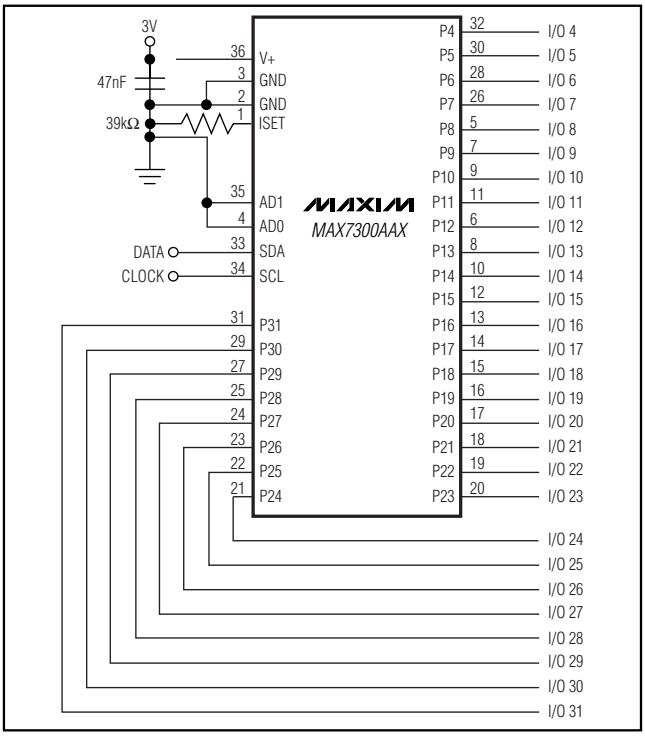
- **400kbps I²C-Compatible Serial Interface**
- **2.5V to 5.5V Operation**
- **-40°C to +125°C Temperature Range**
- **20 or 28 I/O Ports, Each Configurable as**
  - **Push-Pull Logic Output**
  - **Schmitt Logic Input**
  - **Schmitt Logic Input with Internal Pullup**
- **11µA (max) Shutdown Current**
- **Logic Transition Detection for Seven I/O Ports**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX7300AAI	-40°C to +125°C	28 SSOP	A28-1
MAX7300ATI**	-40°C to +125°C	28 Thin QFN	T2855-6
MAX7300AAX	-40°C to +125°C	36 SSOP	A36-4
MAX7300ATL**	-40°C to +125°C	40 Thin QFN	T4066-5

***Use package outline 21-0140 for MAX7300ATI, 21-0141 for MAX7300ATL at the end of the data sheet.*

Typical Operating Circuit



2-Wire-Interfaced, 2.5V to 5.5V, 20-Port or 28-Port I/O Expander

ABSOLUTE MAXIMUM RATINGS

Voltage (with respect to GND)
V+ .....-0.3V to +6V
SCL, SDA, AD0, AD1.....-0.3V to +6V
All Other Pins.....-0.3V to (V+ + 0.3V)
P4–P31 Current .....±30mA
GND Current 800mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin SSOP (derate 9.1mW/°C above +70°C) 727mW
28-Pin TQFN (derate 21.3mW/°C above +70°C) 1702mW
36-Pin SSOP (derate 11.8mW/°C above +70°C) 941mW
40-Pin TQFN (derate 26.3mW/°C above T_A = +70°C).2105mW
Operating Temperature Range
(T_{MIN} to T_{MAX}) .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(*Typical Operating Circuit*, V+ = 2.5V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+			2.5		5.5	V
Shutdown Supply Current	I_{SHDN}	All digital inputs at V+ or GND	T_A = +25°C		5.5	8	µA
			T_A = -40°C to +85°C			10	
			T_{MIN} to T_{MAX}			11	
Operating Supply Current	I_{GPOH}	All ports programmed as outputs high, no load, all other inputs at V+ or GND	T_A = +25°C		180	240	µA
			T_A = -40°C to +85°C			260	
			T_{MIN} to T_{MAX}			280	
Operating Supply Current	I_{GPOL}	All ports programmed as outputs low, no load, all other inputs at V+ or GND	T_A = +25°C		170	210	µA
			T_A = -40°C to +85°C			230	
			T_{MIN} to T_{MAX}			240	
Operating Supply Current	I_{GPI}	All ports programmed as inputs without pullup, ports, and all other inputs at V+ or GND	T_A = +25°C		110	135	µA
			T_A = -40°C to +85°C			140	
			T_{MIN} to T_{MAX}			145	
INPUTS AND OUTPUTS							
Logic High Input Voltage Port Inputs	V_{IH}			0.7 x V+			V
Logic Low Input Voltage Port Inputs	V_{IL}					0.3 x V+	V
Input Leakage Current	I_{IH}, I_{IL}	GPIO inputs without pullup, V_{PORT} = V+ to GND		-100	±1	+100	nA
GPIO Input Internal Pullup to V+	I_{PU}	V+ = 2.5V		12	19	30	µA
		V+ = 5.5V		80	120	180	
Hysteresis Voltage GPIO Inputs	ΔV_I				0.3		V

ELECTRICAL CHARACTERISTICS (continued)

(*Typical Operating Circuit*, V+ = 2.5V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}	GPIO outputs, I_{SOURCE} = 2mA, T_A = -40°C to +85°C	V+ - 0.7			V
		GPIO outputs, I_{SOURCE} = 1mA, $T_A = T_{MIN}$ to T_{MAX} (Note 2)	V+ - 0.7			
Port Sink Current	I_{OL}	V_{PORT} = 0.6V	2	10	18	mA
Output Short-Circuit Current	I_{OLSC}	Port configured output low, shorted to V+	2.75	11	20	mA
Input High-Voltage SDA, SCL, AD0, AD1	V_{IH}		0.7 x V+			V
Input Low-Voltage SDA, SCL, AD0, AD1	V_{IL}				0.3 x V+	V
Input Leakage Current SDA, SCL	I_{IH}, I_{IL}		-50		+50	nA
Input Capacitance		(Note 2)			10	pF
Output Low-Voltage SDA	V_{OL}	I_{SINK} = 6mA			0.4	V

TIMING CHARACTERISTICS (Figure 2)

(V+ = 2.5V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD, STA}$		0.6			µs
Repeated START Condition Setup Time	$t_{SU, STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU, STO}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	(Note 3)	15		900	ns
Data Setup Time	$t_{SU, DAT}$		100			ns
SCL Clock Low Period	t_{LOW}		1.3			µs
SCL Clock High Period	t_{HIGH}		0.7			µs
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Notes 2, 4)		20 + $0.1C_b$	300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Notes 2, 4)		20 + $0.1C_b$	300	ns
Fall Time of SDA Transmitting	$t_{F,TX}$	(Notes 2, 5)		20 + $0.1C_b$	250	ns
Pulse Width of Spike Suppressed	t_{SP}	(Notes 2, 6)	0		50	ns
Capacitive Load for Each Bus Line	C_b	(Note 2)			400	pF

2-Wire-Interfaced, 2.5V to 5.5V, 20-Port or 28-Port I/O Expander

TIMING CHARACTERISTICS (Figure 2) (continued)

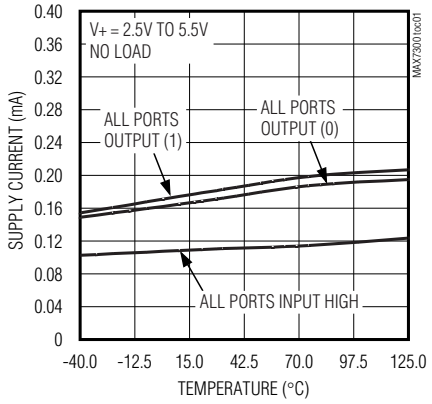
(V+ = 2.5V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

Note 1: All parameters tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Guaranteed by design.
Note 3: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
Note 4: C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.3V+ and 0.7V+.
Note 5: $I_{SINK} \le 6mA$. C_b = total capacitance of one bus line in pF. t_R and t_F measured between 0.3V+ and 0.7V+.
Note 6: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

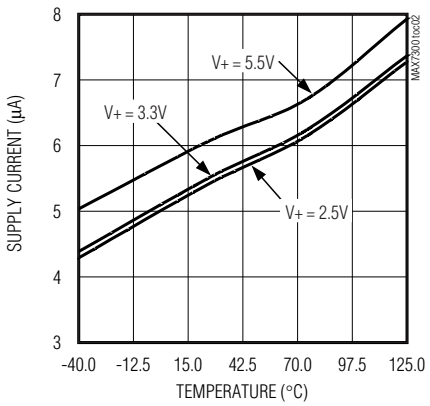
Typical Operating Characteristics

(R_{ISET} = 39kΩ, T_A = +25°C, unless otherwise noted.)

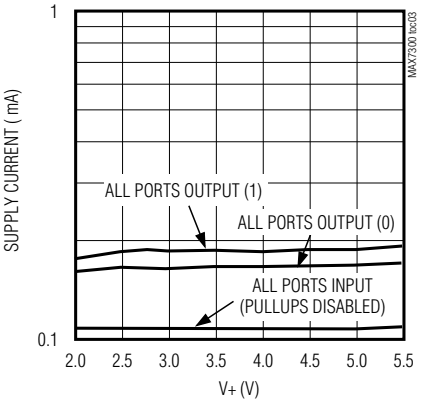
OPERATING SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



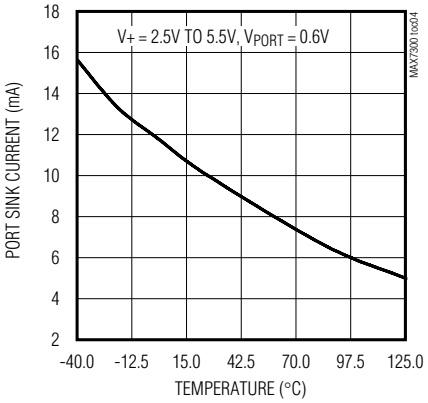
OPERATING SUPPLY CURRENT vs. V+ (OUTPUTS UNLOADED)



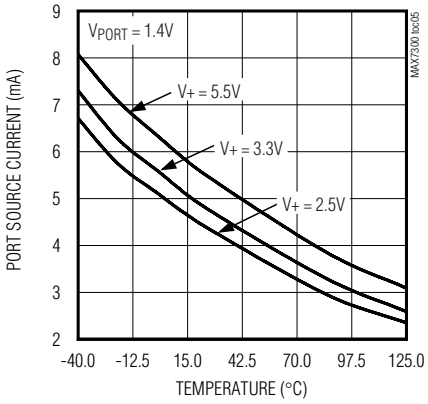
Typical Operating Characteristics (continued)

(R_{ISET} = 39kΩ, T_A = +25°C, unless otherwise noted.)

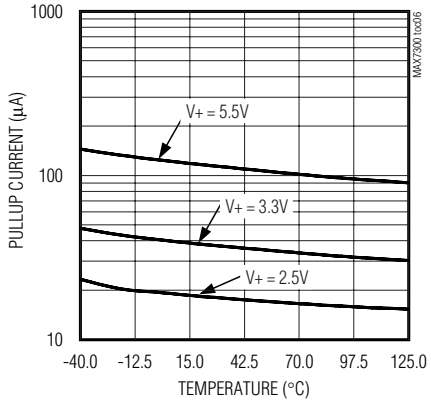
GPO SINK CURRENT vs. TEMPERATURE (OUTPUT = 0)



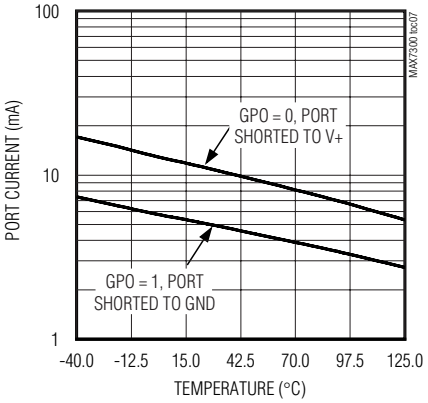
GPO SOURCE CURRENT vs. TEMPERATURE (OUTPUT = 1)



GPI PULLUP CURRENT vs. TEMPERATURE



GPO SHORT-CIRCUIT CURRENT vs. TEMPERATURE



2-Wire-Interfaced, 2.5V to 5.5V, 20-Port or 28-Port I/O Expander

Pin Description

PIN				NAME	FUNCTION
28 SSOP	28 TQFN	36 SSOP	40 TQFN		
1	26	1	36	ISET	Bias Current Setting. Connect ISET to GND through a resistor (R_{ISET}) value of 39kΩ to 120kΩ.
2, 3	27, 28	2, 3	37, 38, 39	GND	Ground
4	1	4	40	AD0	Address Input 0. Sets device slave address. Connect to either GND, V+, SCL, SDA to give four logic combinations. See Table 3.
5–24	2–21	—	—	P12–P31	I/O Ports. P12 to P31 can be configured as push-pull outputs, CMOS-logic inputs, or CMOS-logic inputs with weak pullup resistor.
—	—	5–32	1–10, 12–19, 21–30	P4–P31	I/O Ports. P4 to P31 can be configured as push-pull outputs, CMOS-logic inputs, or CMOS-logic inputs with weak pullup resistor.
—	—	—	11, 20, 31	N.C.	Not Connected.
25	22	33	32	SDA	I^2C-Compatible Serial-Data I/O
26	23	34	33	SCL	I^2C-Compatible Serial-Clock Input
27	24	35	34	AD1	Address Input 1. Sets device slave address. Connect to either GND, V+, SCL, SDA to give four logic combinations. See Table 3.
28	25	36	35	V+	Positive Supply Voltage. Bypass V+ to GND with minimum 0.047µF capacitor.
—	PAD	—	PAD	EXPOSED PAD	Exposed Pad on Package Underside. Connect to GND.

Detailed Description

The MAX7300 general-purpose input/output (GPIO) peripheral provides up to 28 I/O ports, P4 to P31, controlled through an I^2C-compatible serial interface. The ports can be configured to any combination of logic inputs and logic outputs, and default to logic inputs on power-up.

Figure 1 is the MAX7300 functional diagram. Any I/O port can be configured as a push-pull output (sinking 10mA, sourcing 4.5mA), or a Schmitt-trigger logic input. Each input has an individually selectable internal pullup resistor. Additionally, transition detection allows seven ports (P24 to P30) to be monitored in any maskable combination for changes in their logic status. A detected transition is flagged through a status register bit, as well as an interrupt pin (port P31), if desired.

The port configuration registers individually set the 28 ports, P4 to P31, as GPIO. A pair of bits in registers 0x09 through 0x0F sets each port's configuration (Tables 1 and 2).

The 36-pin MAX7300AAX and 40-pin MAX7300ATL have 28 ports, P4 to P31. The 28-pin MAX7300ANI, MAX7300AAI, and MAX7300ATI have only 20 ports available, P12 to P31. The eight unused ports should be configured as outputs on power-up by writing 0x55 to registers 0x09 and 0x0A. If this is not done, the eight unused ports remain as floating inputs and quiescent supply current rises, although there is no damage to the part.

Register Control of I/O Ports Across Multiple Drivers

The MAX7300 offers 20 or 28 I/O ports, depending on package choice. Two addressing methods are available. Any single port (bit) can be written (set/cleared) at once; or, any sequence of eight ports can be written (set/cleared) in any combination at once. There are no boundaries; it is equally acceptable to write P0 to P7, P1 to P8, or P31 to P38 (P32 to P38 are nonexistent, so the instructions to these bits are ignored).

Shutdown

When the MAX7300 is in shutdown mode, all ports are forced to inputs, and the pullup current sources are turned off. Data in the port and control registers remain unaltered, so port configuration and output levels are restored when the MAX7300 is taken out of shutdown. The MAX7300 can still be programmed while in shutdown mode. For minimum supply current in shutdown mode, logic inputs should be at GND or V+ potential. Shutdown mode is exited by setting the S bit in the configuration register (Table 8).

Table 1. Port Configuration Map

REGISTER	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Port Configuration for P7, P6, P5, P4	0x09	P7		P6		P5		P4	
Port Configuration for P11, P10, P9, P8	0x0A	P11		P10		P9		P8	
Port Configuration for P15, P14, P13, P12	0x0B	P15		P14		P13		P12	
Port Configuration for P19, P18, P17, P16	0x0C	P19		P18		P17		P16	
Port Configuration for P23, P22, P21, P20	0x0D	P23		P22		P21		P20	
Port Configuration for P27, P26, P25, P24	0x0E	P27		P26		P25		P24	
Port Configuration for P31, P30, P29, P28	0x0F	P31		P30		P29		P28	

Table 2. Port Configuration Matrix

MODE	FUNCTION	PORT REGISTER (0x20–0x5F)	PIN BEHAVIOR	ADDRESS CODE (HEX)	PORT CONFIGURATION BIT PAIR	
					UPPER	LOWER
DO NOT USE THIS SETTING				0x09 to 0x0F	0	0
Output	GPIO Output	Register bit = 0	Active-low logic output	0x09 to 0x0F	0	1
		Register bit = 1	Active-high logic output			
Input	GPIO Input without Pullup	Register bit = input logic level	Schmitt logic output	0x09 to 0x0F	1	0
Input	GPIO Input with Pullup		Schmitt logic input with pullup	0x09 to 0x0F	1	1

Serial Interface

Serial Addressing

The MAX7300 operates as a slave that sends and receives data through an I^2C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX7300, and generates the SCL clock that synchronizes the data transfer (Figure 2).

The MAX7300 SDA line operates as both an input and an open-drain output. A pullup resistor, typically 4.7kΩ, is required on SDA. The MAX7300 SCL line operates only as an input. A pullup resistor, typically 4.7kΩ, is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START condition (Figure 3) sent by a master, followed by the MAX7300 7-bit slave address plus R/$\overline{W}$ bit (Figure 6), a register address byte, one or more data bytes, and finally a STOP condition (Figure 3).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 3).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 4).

Acknowledge

The acknowledge bit is a clocked 9th bit, which the recipient uses to handshake receipt of each byte of data (Figure 5). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7300, the MAX7300 generates the acknowledge bit since the

2-Wire-Interfaced, 2.5V to 5.5V, 20-Port or 28-Port I/O Expander

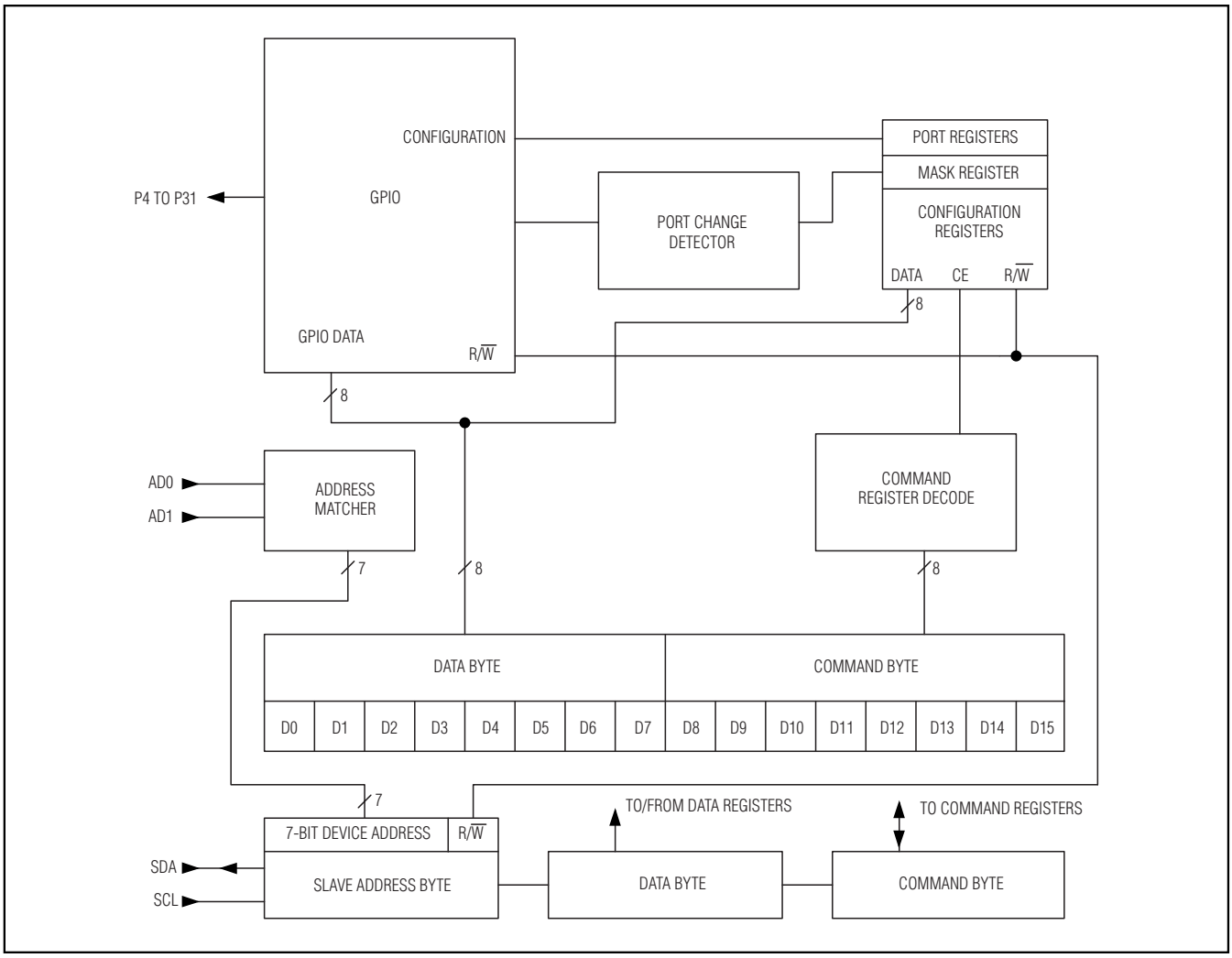


Figure 1. MAX7300 Functional Diagram

MAX7300 is the recipient. When the MAX7300 is transmitting to the master, the master generates the acknowledge bit since the master is the recipient.

Slave Address

The MAX7300 has a 7-bit-long slave address (Figure 6). The eighth bit following the 7-bit slave address is the R/$\overline{W}$ bit. It is low for a write command and high for a read command.

The first 3 bits (MSBs) of the MAX7300 slave address are always 100. Slave address bits A3, A2, A1, and A0 are selected by the address inputs, AD1 and AD0. These two input pins can be connected to GND, V+, SDA, or SCL. The MAX7300 has 16 possible slave addresses (Table 3), and therefore a maximum of 16 MAX7300 devices can share the same interface.

Message Format for Writing the MAX7300

A write to the MAX7300 comprises the transmission of the MAX7300's slave address with the R/$\overline{W}$ bit set to zero, followed by at least 1 byte of information. The first byte of information is the command byte. The command byte determines which register of the MAX7300 is to be written by the next byte, if received. If a STOP condition is detected after the command byte is received, then the MAX7300 takes no further action (Figure 7) beyond storing the command byte.

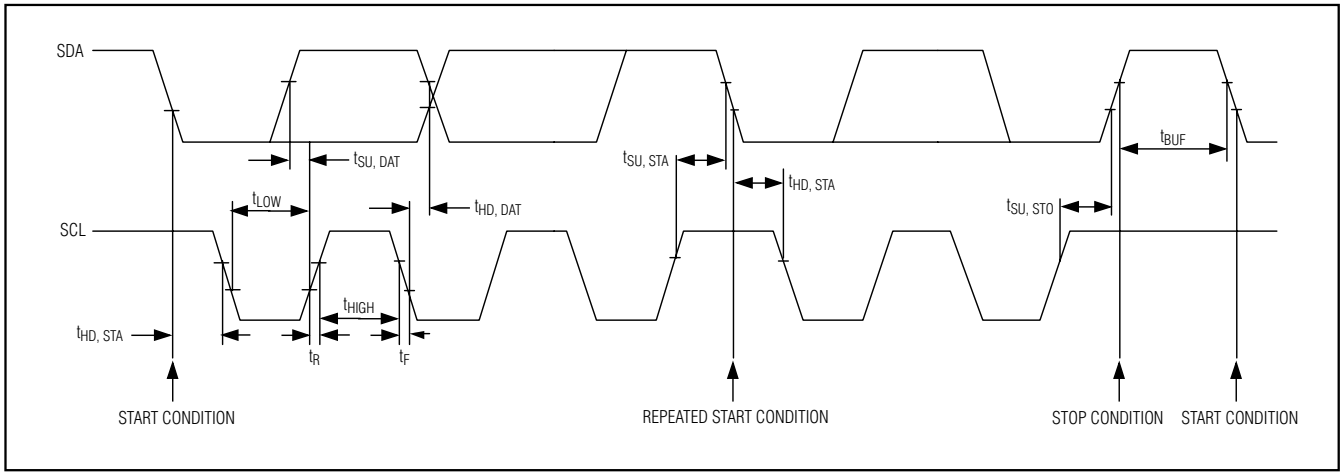


Figure 2. 2-Wire Serial Interface Timing Details

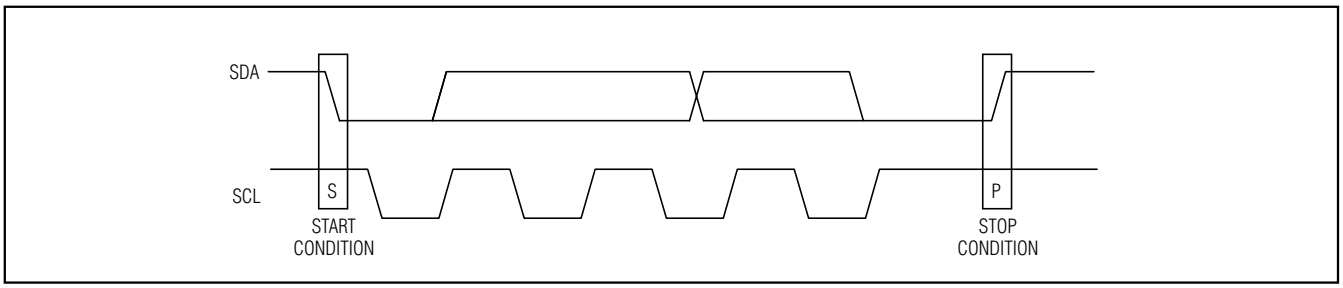


Figure 3. Start and Stop Conditions

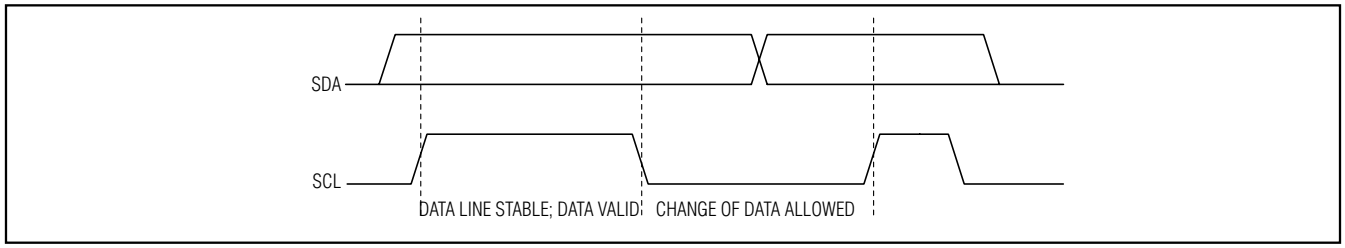


Figure 4. Bit Transfer

Any bytes received after the command byte are considered data bytes. The first data byte goes into the internal register of the MAX7300 selected by the command byte (Figure 8). If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent MAX7300 internal registers because the command byte address generally autoincrements (Table 4).

Message Format for Reading

The MAX7300 is read using the MAX7300's internally stored command byte as address pointer, the same way the stored command byte is used as address pointer for a write. The pointer generally autoincrements after each data byte is read using the same rules as for a write (Table 4). Thus, a read is initiated by first configuring the MAX7300's command byte by performing a write (Figure 7). The master can now read 'n' consecutive bytes from the MAX7300, with the first data byte being read from the register addressed by the initialized command byte (Figure 9). When performing read-after-write verification, remember to reset the command byte's address because the stored control byte address generally has been autoincremented after the write (Table 4). Table 5 is the register address map.

2-Wire-Interfaced, 2.5V to 5.5V, 20-Port or 28-Port I/O Expander

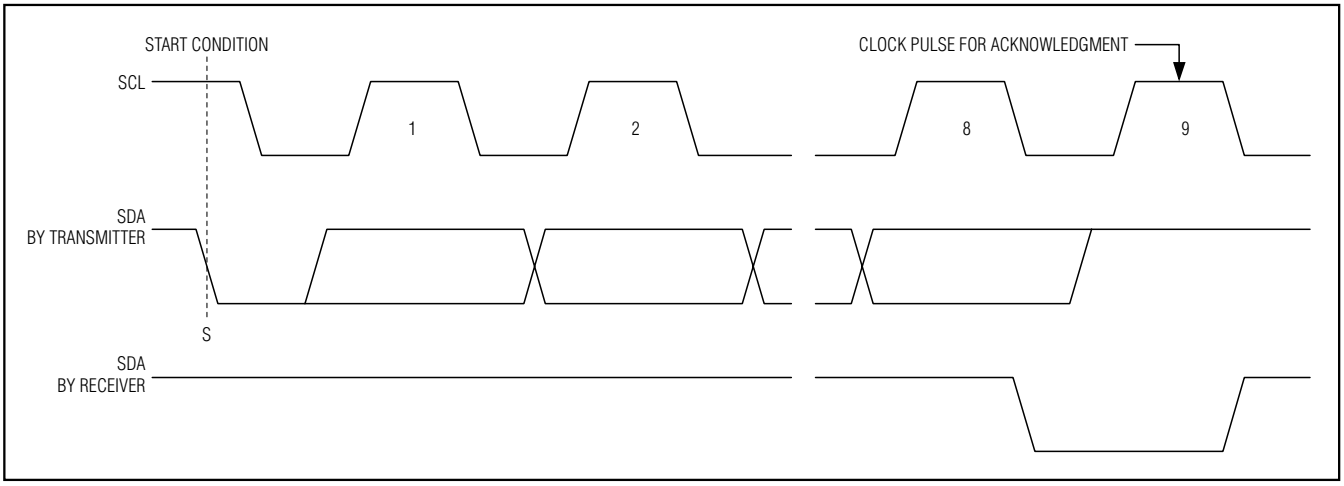


Figure 5. Acknowledge

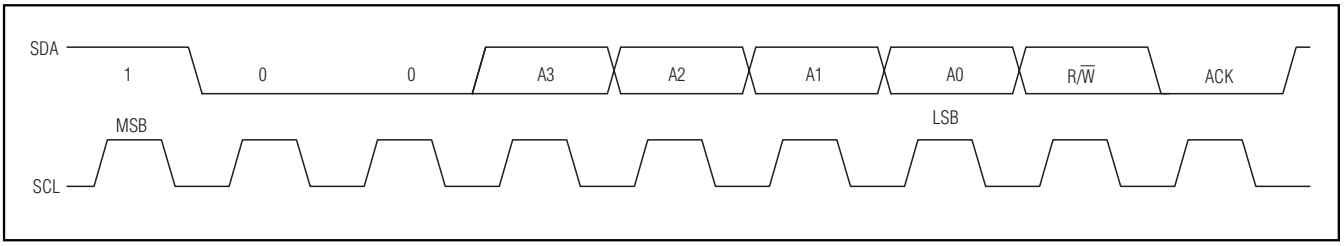


Figure 6. Slave Address

Operation with Multiple Masters

If the MAX7300 is operated on a 2-wire interface with multiple masters, a master reading the MAX7300 should use a repeated start between the write, which sets the MAX7300's address pointer, and the read(s) that takes the data from the location(s). This is because it is possible for master 2 to take over the bus after master 1 has set up the MAX7300's address pointer, but before master 1 has read the data. If master 2 subsequently changes, the MAX7300's address pointer, then master 1's delayed read can be from an unexpected location.

Command Address Autoincrementing

Address autoincrementing allows the MAX7300 to be configured with the shortest number of transmissions by minimizing the number of times the command address needs to be sent. The command address stored in the MAX7300 generally increments after each data byte is written or read (Table 4).

Initial Power-Up

On initial power-up, all control registers are reset and the MAX7300 enters shutdown mode (Table 6).

Transition (Port Data Change) Detection

Port transition detection allows any combination of the seven ports P24–P30 to be continuously monitored for changes in their logic status (Figure 10). A detected change is flagged on the transition detection mask register INT status bit, D7 (Table 10). If port P31 is configured as an output (Tables 1 and 2), then P31 also automatically becomes an active-high interrupt output (INT), which follows the condition of the INT status bit. Port P31 is set as output by writing bit D7 = 0 and bit D6 = 1 to the port configuration register (Table 1). Note that the MAX7300 does not identify which specific port(s) caused the interrupt, but provides an alert that one or more port levels have changed.

The mask register contains 7 mask bits that select which of the seven ports P24–P30 are to be monitored (Table 10). Set the appropriate mask bit to enable that port for transition detect. Clear the mask bit if transi-

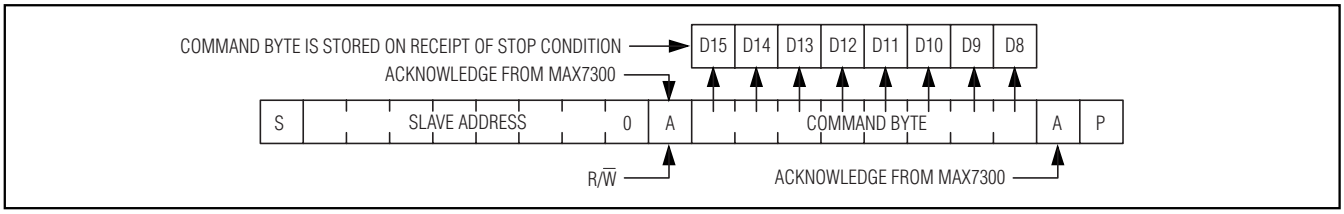


Figure 7. Command Byte Received

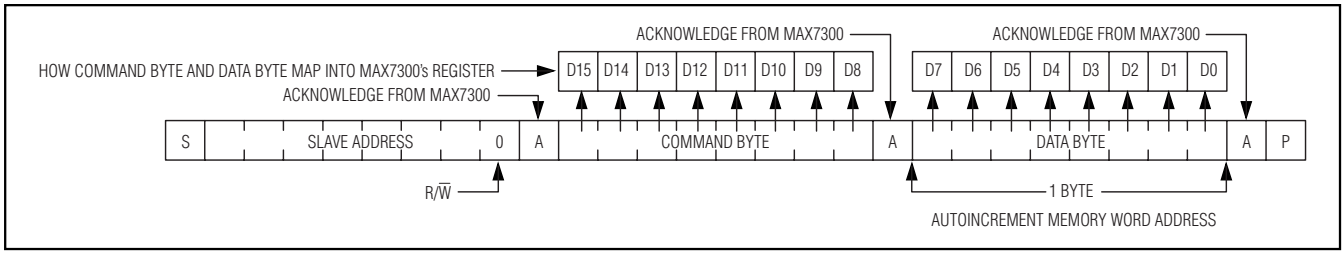


Figure 8. Command and Single Data Byte Received

tions on that port are to be ignored. Transition detection works regardless of whether the port being monitored is set to input or output, but generally, it is not particularly useful to enable transition detection for outputs.

To use transition detection, first set up the mask register and configure port P31 as an output, as described above. Then enable transition detection by setting the M bit in the configuration register (Table 9). Whenever the configuration register is written with the M bit set, the MAX7300 updates an internal 7-bit snapshot register, which holds the comparison copy of the logic states of ports P24 through P30. The update action occurs regardless of the previous state of the M bit, so that it is not necessary to clear the M bit and then set it again to update the snapshot register.

When the configuration register is written with the M bit set, transition detection is enabled and remains enabled until either the configuration register is written with the M bit clear, or a transition is detected. The INT status bit (transition detection mask register bit D7) goes low. Port P31 (if enabled as INT output) also goes low, if it was not already low.

Once transition detection is enabled, the MAX7300 continuously compares the snapshot register against the changing states of P24 through P31. If a change on any of the monitored ports is detected, even for a short time (like a pulse), the INT status bit (transition detection mask register bit D7) is set. Port P31 (if enabled as INT output) also goes high. The INT output and INT status bit are not cleared if more changes occur or if the data pattern returns to its original snapshot condition. The only way to clear INT is to access (read or write) the transition detection mask register (Table 10). So if the transition detection mask register is read twice in succession after a transition event, the first time reads with bit D7 set (identifying the event), and the second time reads with bit D7 clear.

Transition detection is a one-shot event. When INT has been cleared after responding to a transition event, transition detection is automatically disabled, even though the M bit in the configuration register remains set (unless cleared by the user). Reenable transition detection by writing the configuration register with the M bit set to take a new snapshot of the seven ports P24 to P30.

External Component R_{ISET}

The MAX7300 uses an external resistor, R_{ISET}, to set internal biasing. Use a resistor value of 39kΩ.

Applications Information

Low-Voltage Operation

The MAX7300 operates down to 2V supply voltage (although the sourcing and sinking currents are not guaranteed), providing that the MAX7300 is powered up initially to at least 2.5V to trigger the device's internal reset.

Serial Interface Latency

When a MAX7300 register is written through the I^2C interface, the register is updated on the rising edge of SCL during the data byte's acknowledge bit (Figure 5). The delay from the rising edge of SCL to the internal register being updated can range from 50ns to 350ns.

2-Wire-Interfaced, 2.5V to 5.5V, 20-Port or 28-Port I/O Expander

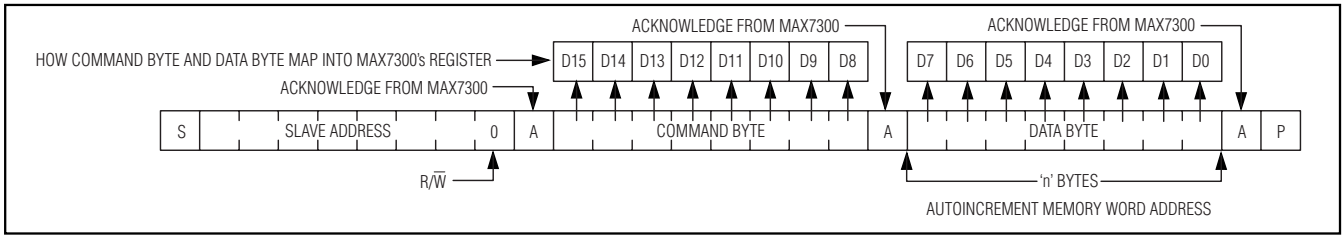


Figure 9. 'n' Data Bytes Received

Table 3. MAX7300 Address Map

PIN CONNECTION		DEVICE ADDRESS						
AD1	**AD0**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
GND	GND	1	0	0	0	0	0	0
GND	V+	1	0	0	0	0	0	1
GND	SDA	1	0	0	0	0	1	0
GND	SCL	1	0	0	0	0	1	1
V+	GND	1	0	0	0	1	0	0
V+	V+	1	0	0	0	1	0	1
V+	SDA	1	0	0	0	1	1	0
V+	SCL	1	0	0	0	1	1	1
SDA	GND	1	0	0	1	0	0	0
SDA	V+	1	0	0	1	0	0	1
SDA	SDA	1	0	0	1	0	1	0
SDA	SCL	1	0	0	1	0	1	1
SCL	GND	1	0	0	1	1	0	0
SCL	V+	1	0	0	1	1	0	1
SCL	SDA	1	0	0	1	1	1	0
SCL	SCL	1	0	0	1	1	1	1

Table 4. Autoincrement Rules

COMMAND BYTE ADDRESS RANGE	AUTOINCREMENT BEHAVIOR
x0000000 to x1111110	Command address autoincrements after byte read or written
x1111111	Command address remains at x1111111 after byte written or read

PC Board Layout Considerations

Ensure that all the MAX7300 GND connections are used. For QFN versions, connect the underside exposed pad to GND. A ground plane is not necessary, but may be useful to reduce supply impedance if the MAX7300 outputs are to be heavily loaded. Keep the track length from the ISET pin to the R_{ISET} resistor as short as possible, and take the GND end of the register either to the ground plane or directly to the GND pins.

Power-Supply Considerations

The MAX7300 operates with power-supply voltages of 2.5V to 5.5V. Bypass the power supply to GND with a 0.047µF capacitor as close to the device as possible. Add a 1µF capacitor if the MAX7300 is far away from the board's input bulk decoupling capacitor.

Table 5. Register Address Map

REGISTER	COMMAND ADDRESS								HEX CODE
	D15	D14	D13	D12	D11	D10	D9	D8	
No-Op	X	0	0	0	0	0	0	0	0x00
Configuration	X	0	0	0	0	1	0	0	0x04
Transition Detect Mask	X	0	0	0	0	1	1	0	0x06
Factory Reserved; do not write to this port	X	0	0	0	0	1	1	1	0x07
Port Configuration P7, P6, P5, P4	X	0	0	0	1	0	0	1	0x09
Port Configuration P11, P10, P9, P8	X	0	0	0	1	0	1	0	0x0A
Port Configuration P15, P14, P13, P12	X	0	0	0	1	0	1	1	0x0B
Port Configuration P19, P18, P17, P16	X	0	0	0	1	1	0	0	0x0C
Port Configuration P23, P22, P21, P20	X	0	0	0	1	1	0	1	0x0D
Port Configuration P27, P26, P25, P24	X	0	0	0	1	1	1	0	0x0E
Port Configuration P31, P30, P29, P28	X	0	0	0	1	1	1	1	0x0F
Port 0 only (virtual port, no action)	X	0	1	0	0	0	0	0	0x20
Port 1 only (virtual port, no action)	X	0	1	0	0	0	0	1	0x21
Port 2 only (virtual port, no action)	X	0	1	0	0	0	1	0	0x22
Port 3 only (virtual port, no action)	X	0	1	0	0	0	1	1	0x23
Port 4 only (data bit D0. D7-D1 read as 0)	X	0	1	0	0	1	0	0	0x24
Port 5 only (data bit D0. D7-D1 read as 0)	X	0	1	0	0	1	0	1	0x25
Port 6 only (data bit D0. D7-D1 read as 0)	X	0	1	0	0	1	1	0	0x26
Port 7 only (data bit D0. D7-D1 read as 0)	X	0	1	0	0	1	1	1	0x27
Port 8 only (data bit D0. D7-D1 read as 0)	X	0	1	0	1	0	0	0	0x28
Port 9 only (data bit D0. D7-D1 read as 0)	X	0	1	0	1	0	0	1	0x29
Port 10 only (data bit D0. D7-D1 read as 0)	X	0	1	0	1	0	1	0	0x2A
Port 11 only (data bit D0. D7-D1 read as 0)	X	0	1	0	1	0	1	1	0x2B
Port 12 only (data bit D0. D7-D1 read as 0)	X	0	1	0	1	1	0	0	0x2C
Port 13 only (data bit D0. D7-D1 read as 0)	X	0	1	0	1	1	0	1	0x2D
Port 14 only (data bit D0. D7-D1 read as 0)	X	0	1	0	1	1	1	0	0x2E
Port 15 only (data bit D0. D7-D1 read as 0)	X	0	1	0	1	1	1	1	0x2F
Port 16 only (data bit D0. D7-D1 read as 0)	X	0	1	1	0	0	0	0	0x30
Port 17 only (data bit D0. D7-D1 read as 0)	X	0	1	1	0	0	0	1	0x31
Port 18 only (data bit D0. D7-D1 read as 0)	X	0	1	1	0	0	1	0	0x32
Port 19 only (data bit D0. D7-D1 read as 0)	X	0	1	1	0	0	1	1	0x33
Port 20 only (data bit D0. D7-D1 read as 0)	X	0	1	1	0	1	0	0	0x34
Port 21 only (data bit D0. D7-D1 read as 0)	X	0	1	1	0	1	0	1	0x35
Port 22 only (data bit D0. D7-D1 read as 0)	X	0	1	1	0	1	1	0	0x36
Port 23 only (data bit D0. D7-D1 read as 0)	X	0	1	1	0	1	1	1	0x37
Port 24 only (data bit D0. D7-D1 read as 0)	X	0	1	1	1	0	0	0	0x38
Port 25 only (data bit D0. D7-D1 read as 0)	X	0	1	1	1	0	0	1	0x39

2-Wire-Interfaced, 2.5V to 5.5V, 20-Port or 28-Port I/O Expander

Table 5. Register Address Map (continued)

REGISTER	COMMAND ADDRESS								HEX CODE
	D15	D14	D13	D12	D11	D10	D9	D8	
Port 26 only (data bit D0. D7-D1 read as 0)	X	0	1	1	1	0	1	0	0x3A
Port 27 only (data bit D0. D7-D1 read as 0)	X	0	1	1	1	0	1	1	0x3B
Port 28 only (data bit D0. D7-D1 read as 0)	X	0	1	1	1	1	0	0	0x3C
Port 29 only (data bit D0. D7-D1 read as 0)	X	0	1	1	1	1	0	1	0x3D
Port 30 only (data bit D0. D7-D1 read as 0)	X	0	1	1	1	1	1	0	0x3E
Port 31 only (data bit D0. D7-D1 read as 0)	X	0	1	1	1	1	1	1	0x3F
4 ports 4–7 (data bits D0–D3. D4–D7 read as 0)	X	1	0	0	0	0	0	0	0x40
5 ports 4–8 (data bits D0–D4. D5–D7 read as 0)	X	1	0	0	0	0	0	1	0x41
6 ports 4–9 (data bits D0–D5. D6–D7 read as 0)	X	1	0	0	0	0	1	0	0x42
7 ports 4–10 (data bits D0–D6. D7 reads as 0)	X	1	0	0	0	0	1	1	0x43
8 ports 4–11 (data bits D0–D7)	X	1	0	0	0	1	0	0	0x44
8 ports 5–12 (data bits D0–D7)	X	1	0	0	0	1	0	1	0x45
8 ports 6–13 (data bits D0–D7)	X	1	0	0	0	1	1	0	0x46
8 ports 7–14 (data bits D0–D7)	X	1	0	0	0	1	1	1	0x47
8 ports 8–15 (data bits D0–D7)	X	1	0	0	1	0	0	0	0x48
8 ports 9–16 (data bits D0–D7)	X	1	0	0	1	0	0	1	0x49
8 ports 10–17 (data bits D0–D7)	X	1	0	0	1	0	1	0	0x4A
8 ports 11–18 (data bits D0–D7)	X	1	0	0	1	0	1	1	0x4B
8 ports 12–19 (data bits D0–D7)	X	1	0	0	1	1	0	0	0x4C
8 ports 13–20 (data bits D0–D7)	X	1	0	0	1	1	0	1	0x4D
8 ports 14–21 (data bits D0–D7)	X	1	0	0	1	1	1	0	0x4E
8 ports 15–22 (data bits D0–D7)	X	1	0	0	1	1	1	1	0x4F
8 ports 16–23 (data bits D0–D7)	X	1	0	1	0	0	0	0	0x50
8 ports 17–24 (data bits D0–D7)	X	1	0	1	0	0	0	1	0x51
8 ports 18–25 (data bits D0–D7)	X	1	0	1	0	0	1	0	0x52
8 ports 19–26 (data bits D0–D7)	X	1	0	1	0	0	1	1	0x53
8 ports 20–27 (data bits D0–D7)	X	1	0	1	0	1	0	0	0x54
8 ports 21–28 (data bits D0–D7)	X	1	0	1	0	1	0	1	0x55
8 ports 22–29 (data bits D0–D7)	X	1	0	1	0	1	1	0	0x56
8 ports 23–30 (data bits D0–D7)	X	1	0	1	0	1	1	1	0x57
8 ports 24–31 (data bits D0–D7)	X	1	0	1	1	0	0	0	0x58
7 ports 25–31 (data bits D0–D6. D7 reads as 0)	X	1	0	1	1	0	0	1	0x59
6 ports 26–31 (data bits D0–D5. D6–D7 read as 0)	X	1	0	1	1	0	1	0	0x5A
5 ports 27–31 (data bits D0–D4. D5–D7 read as 0)	X	1	0	1	1	0	1	1	0x5B
4 ports 28–31 (data bits D0–D3. D4–D7 read as 0)	X	1	0	1	1	1	0	0	0x5C
3 ports 29–31 (data bits D0–D2. D3–D7 read as 0)	X	1	0	1	1	1	0	1	0x5D
2 ports 30–31 (data bits D0–D1. D2–D7 read as 0)	X	1	0	1	1	1	1	0	0x5E
1 port 31 only (data bits D0. D1–D7 read as 0)	X	1	0	1	1	1	1	1	0x5F

Note: *Unused bits read as zero.*

Table 6. Power-Up Configuration

REGISTER FUNCTION	POWER-UP CONDITION	ADDRESS CODE (HEX)	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Port Register Bits 4 to 31	GPIO Output Low	0x24 to 0x3F	X	X	X	X	X	X	X	0
Configuration Register	Shutdown Enabled Transition Detection Disabled	0x04	0	0	X	X	X	X	X	0
Input Mask Register	All Clear (Masked Off)	0x06	X	0	0	0	0	0	0	0
Port Configuration	P7, P6, P5, P4: GPIO Inputs without Pullup	0x09	1	0	1	0	1	0	1	0
Port Configuration	P11, P10, P9, P8: GPIO Inputs without Pullup	0x0A	1	0	1	0	1	0	1	0
Port Configuration	P15, P14, P13, P12: GPIO Inputs without Pullup	0x0B	1	0	1	0	1	0	1	0
Port Configuration	P19, P18, P17, P16: GPIO Inputs without Pullup	0x0C	1	0	1	0	1	0	1	0
Port Configuration	P23, P22, P21, P20: GPIO Inputs without Pullup	0x0D	1	0	1	0	1	0	1	0
Port Configuration	P27, P26, P25, P24: GPIO Inputs without Pullup	0x0E	1	0	1	0	1	0	1	0
Port Configuration	P31, P30, P29, P28: GPIO Inputs without Pullup	0x0F	1	0	1	0	1	0	1	0

X = unused bits; if read, zero results.

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Table 7. Configuration Register Format

FUNCTION	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Configuration Register	0x04	M	0	X	X	X	X	X	S

Table 8. Shutdown Control (S Data Bit D0) Format

FUNCTION	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Shutdown	0x04	M	0	X	X	X	X	X	0
Normal Operation	0x04	M	0	X	X	X	X	X	1

Table 9. Transition Detection Control (M Data Bit D7) Format

FUNCTION	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Disabled	0x04	0	0	X	X	X	X	X	S
Enabled	0x04	1	0	X	X	X	X	X	S

Table 10. Transition Detection Mask Register

FUNCTION	REGISTER ADDRESS (HEX)	READ/ WRITE	REGISTER DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
Mask Register	0x06	Read	INT Status*	Port 30 mask	Port 29 mask	Port 28 mask	Port 27 mask	Port 26 mask	Port 25 mask	Port 24 mask
		Write	Unchanged							

**INT is automatically cleared after it is read.*

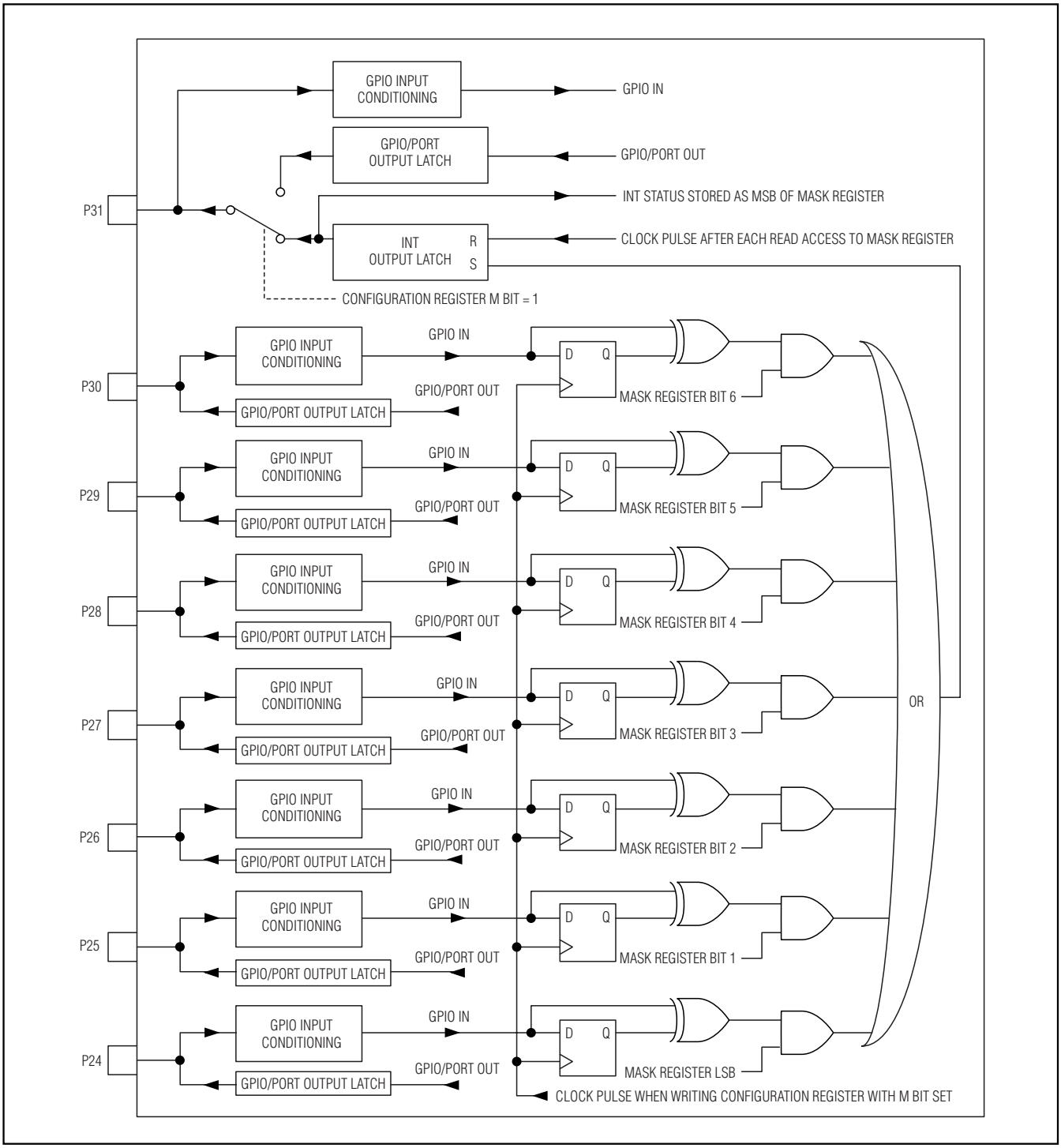
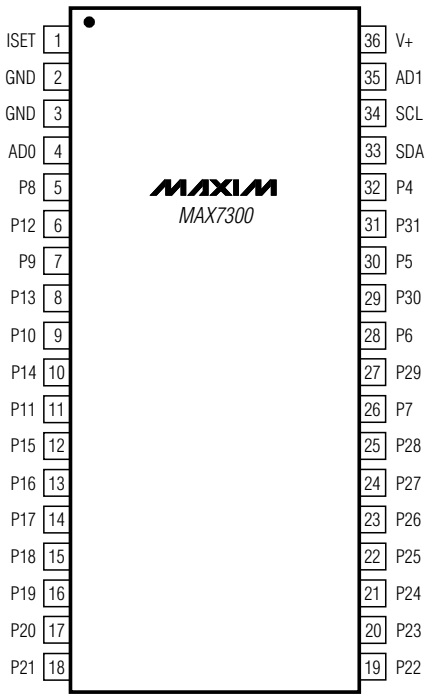


Figure 10. Maskable GPIO Ports P24 to P31

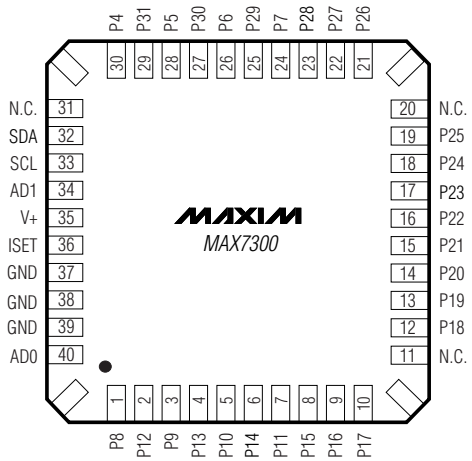
2-Wire-Interfaced, 2.5V to 5.5V, 20-Port or 28-Port I/O Expander

Pin Configurations (continued)

TOP VIEW

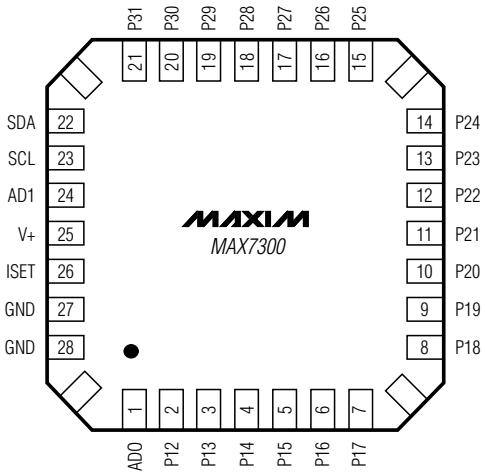


36 SSOP



40 TQFN

TOP VIEW



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Chip Information

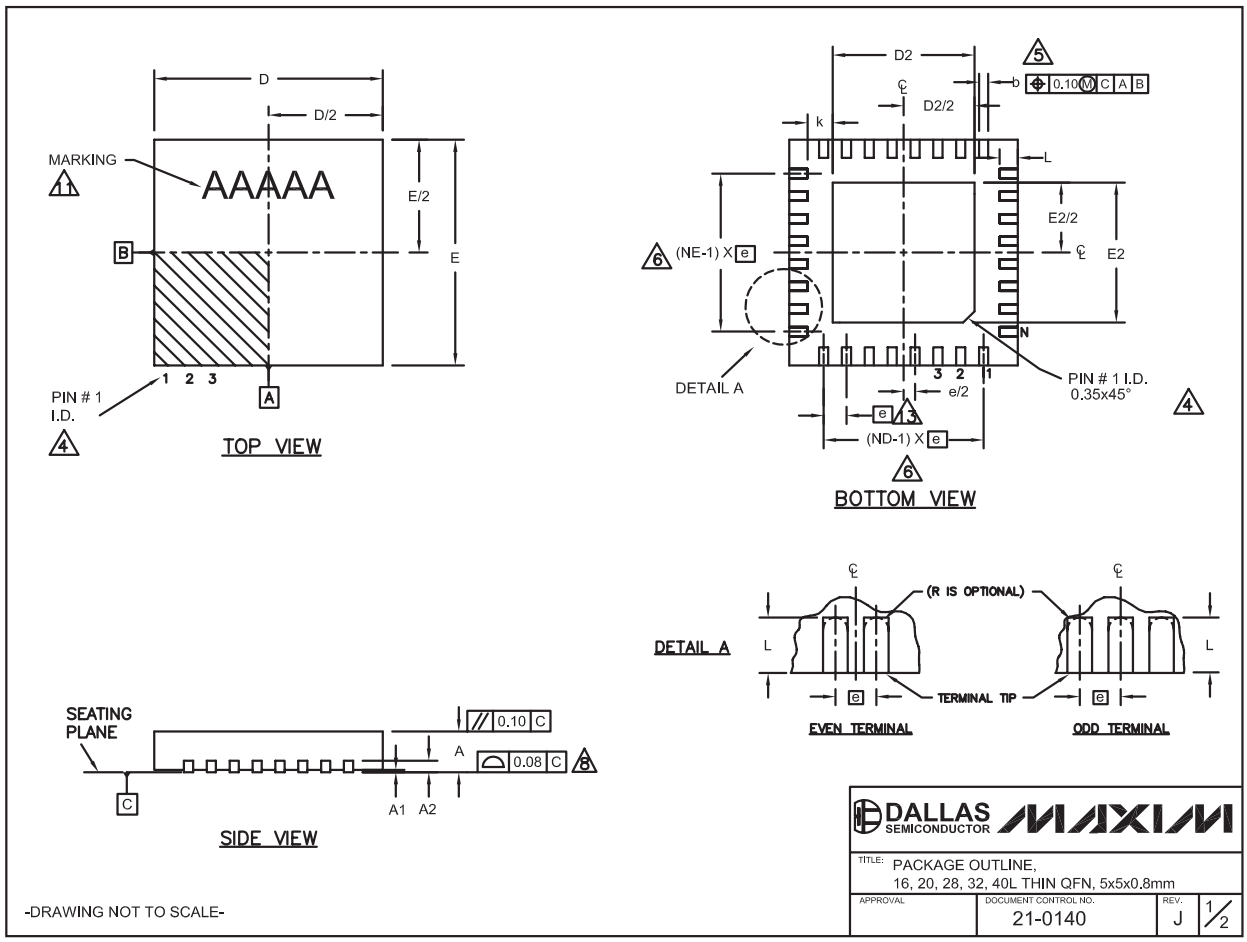
TRANSISTOR COUNT: 33,559

PROCESS: CMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



2-Wire-Interfaced, 2.5V to 5.5V, 20-Port or 28-Port I/O Expander

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			——		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60

**SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3 AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

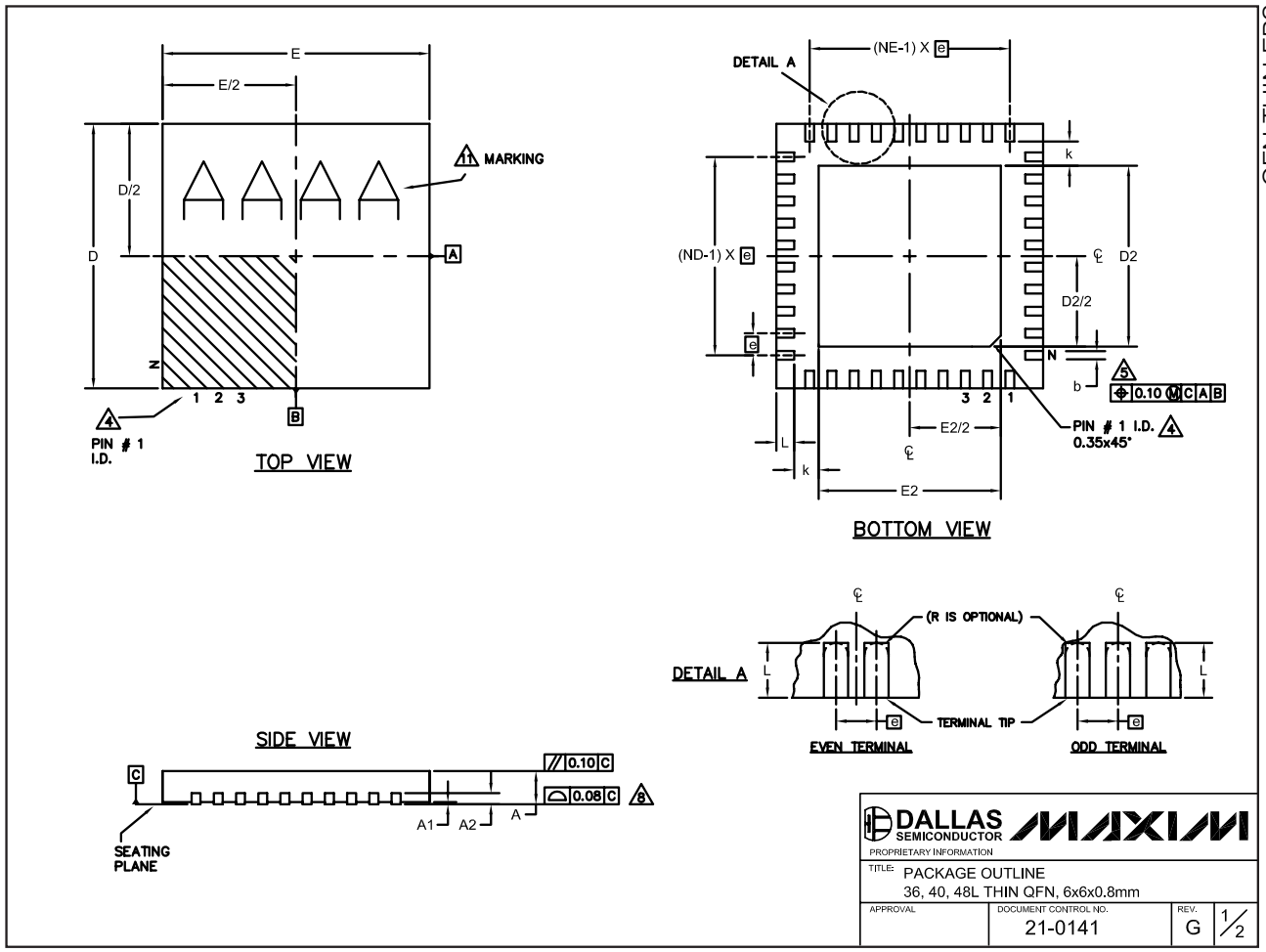
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	J	2/2

2-Wire-Interfaced, 2.5V to 5.5V, 20-Port or 28-Port I/O Expander

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



2-Wire-Interfaced, 2.5V to 5.5V, 20-Port or 28-Port I/O Expander

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80
T3666N-1	3.60	3.70	3.80	3.60	3.70	3.80
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20
T4866-1	4.40	4.50	4.60	4.40	4.50	4.60
T4866-2	4.40	4.50	4.60	4.40	4.50	4.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

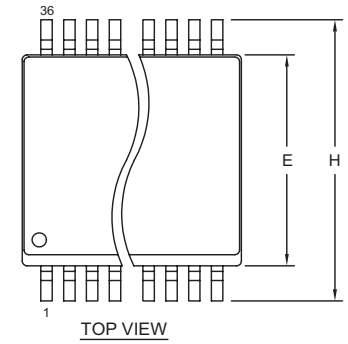
TITLE: PACKAGE OUTLINE
36, 40, 48L THIN QFN, 6x6x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0141	G	2/2

Package Information (continued)

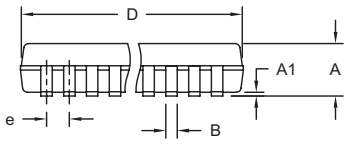
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SSOP.EPS

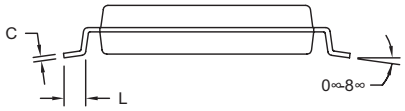


TOP VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.096	0.104	2.44	2.65
A1	0.004	0.011	0.10	0.29
B	0.012	0.017	0.30	0.44
C	0.009	0.013	0.23	0.32
e	0.0315 BSC		0.80 BSC	
E	0.291	0.299	7.40	7.60
H	0.398	0.414	10.11	10.51
L	0.020	0.040	0.51	1.02
D	0.598	0.612	15.20	15.55



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, 36L SSOP, 0.80 MM PITCH

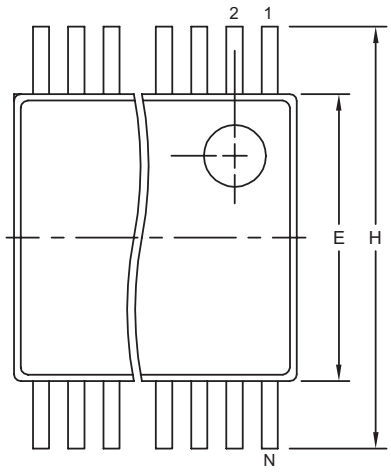
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0040	E	1/1

2-Wire-Interfaced, 2.5V to 5.5V, 20-Port or 28-Port I/O Expander

Package Information (continued)

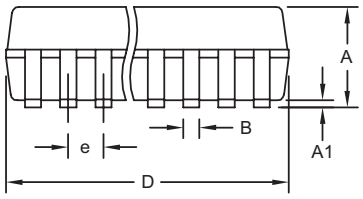
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

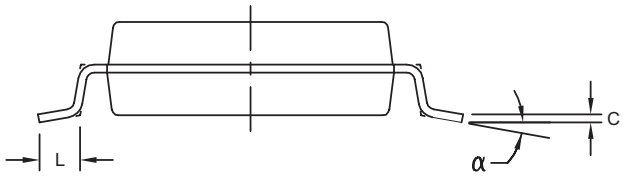
SSOP.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.212	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0∞	8∞	0∞	8∞

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L





NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO150.
5. LEADS TO BE COPLANAR WITHIN 0.10 MM.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, SSOP, 5.3 MM

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0056	C	1/1