

2.5V to 5.5V Micropower CMOS Op Amps

Features

- Low Input Offset Voltage: 250 μ V (max.)
- Rail-to-Rail Output
- Low Input Bias Current: 80 pA (max. at 85°C)
- Low Quiescent Current: 25 μ A (max.)
- Power Supply Voltage: 2.5V to 5.5V
- Unity-Gain Stable
- Chip Select ($\overline{\text{CS}}$) Capability: **MCP608**
- Industrial Temperature Range: -40°C to +85°C
- No Phase Reversal
- Available in Single, Dual and Quad Packages

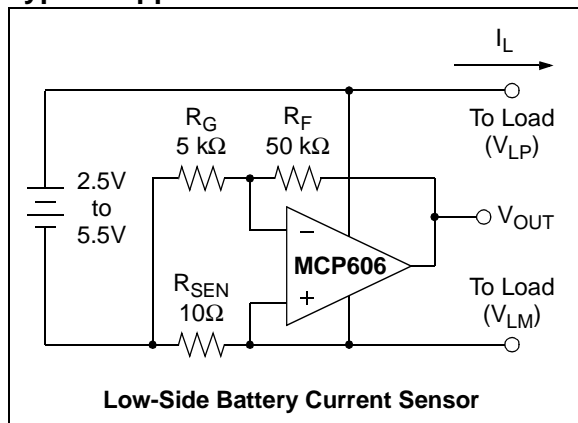
Typical Applications

- Battery Power Instruments
- High-Impedance Applications
 - Photodiode Amplifier
 - pH Probe Buffer Amplifier
 - Infrared Detectors
 - Precision Integrators
 - Charge Amplifier for Piezoelectric Transducers
- Strain Gauges
- Medical Instruments
- Test Equipment

Available Tools

- SPICE Macro Models (at www.microchip.com)
- FilterLab[®] Software (at www.microchip.com)

Typical Application

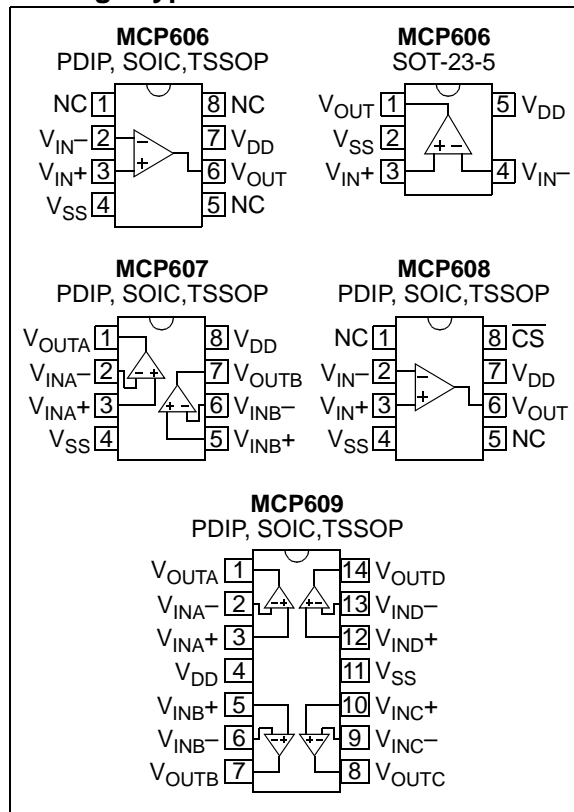


Description

The MCP606/7/8/9 family of operational amplifiers (op amps) from Microchip Technology Inc. are unity-gain stable with low offset voltage (250 μ V, max.). Performance characteristics include rail-to-rail output swing capability and low input bias current (80 pA at +85°C, max.). These features make this family of op amps well suited for single-supply, precision, high-impedance, battery-powered applications.

The single MCP606 is available in standard 8-lead PDIP, SOIC and TSSOP packages, as well as in a SOT-23-5 package. The single MCP608 with Chip Select ($\overline{\text{CS}}$) is offered in standard 8-lead PDIP, SOIC and TSSOP packages. The dual MCP607 is offered in standard 8-lead PDIP, SOIC and TSSOP packages. Finally, the quad MCP609 is offered in standard 14-lead PDIP, SOIC and TSSOP packages. All devices are fully specified from -40°C to +85°C, with power supplies from 2.5V to 5.5V.

Package Types



MCP606/7/8/9

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$V_{DD} - V_{SS}$	7.0V
All Inputs and Outputs	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input Voltage	$ V_{DD} - V_{SS} $
Output Short Circuit Current	continuous
Current at Input Pins	± 2 mA
Current at Output and Supply Pins	± 30 mA
Storage temperature	-65°C to $+150^{\circ}\text{C}$
Maximum Junction Temperature (T_J)	$+150^{\circ}\text{C}$
ESD protection on all pins (HBM;MM)	2 kV; 200V

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, $V_{DD} = +2.5V$ to $+5.5V$, $V_{SS} = \text{GND}$, $T_A = +25^{\circ}\text{C}$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$ and $R_L = 100$ k Ω to $V_{DD}/2$.						
Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-250	—	+250	μV	
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	± 1.8	—	$\mu\text{V}/^{\circ}\text{C}$	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
Power Supply Rejection Ratio	PSRR	80	93	—	dB	
Input Bias Current and Impedance						
Input Bias Current	I_B	—	1	—	pA	
At Temperature	I_B	—	—	80	pA	$T_A = +85^{\circ}\text{C}$
Input Offset Bias Current	I_{OS}	—	1	—	pA	
Common Mode Input Impedance	Z_{CM}	—	$10^{13} 6$	—	ΩpF	
Differential Input Impedance	Z_{DIFF}	—	$10^{13} 6$	—	ΩpF	
Common Mode						
Common Mode Input Range	V_{CMR}	$V_{SS} - 0.3$		$V_{DD} - 1.1$	V	CMRR ≥ 75 dB
Common Mode Rejection Ratio	CMRR	75	91	—	dB	$V_{DD} = 5V$, $V_{CM} = -0.3V$ to $3.9V$
Open-Loop Gain						
DC Open-Loop Gain (Large-signal)	A_{OL}	105	121	—	dB	$R_L = 25$ k Ω to $V_{DD}/2$, $V_{OUT} = 50$ mV to $V_{DD} - 50$ mV
DC Open-Loop Gain (Large-signal)	A_{OL}	100	118	—	dB	$R_L = 5$ k Ω to $V_{DD}/2$, $V_{OUT} = 0.1V$ to $V_{DD} - 0.1V$
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	$V_{SS} + 15$	—	$V_{DD} - 20$	mV	$R_L = 25$ k Ω to $V_{DD}/2$, 0.5V output overdrive
	V_{OL}, V_{OH}	$V_{SS} + 45$	—	$V_{DD} - 60$	mV	$R_L = 5$ k Ω to $V_{DD}/2$, 0.5V output overdrive
Linear Output Voltage Range	V_{OUT}	$V_{SS} + 50$	—	$V_{DD} - 50$	mV	$R_L = 25$ k Ω to $V_{DD}/2$, $A_{OL} \geq 105$ dB
	V_{OUT}	$V_{SS} + 100$	—	$V_{DD} - 100$	mV	$R_L = 5$ k Ω to $V_{DD}/2$, $A_{OL} \geq 100$ dB
Output Short Circuit Current	I_{SC}	—	7	—	mA	$V_{DD} = 2.5V$
	I_{SC}	—	17	—	mA	$V_{DD} = 5.5V$
Power Supply						
Supply Voltage	V_{DD}	2.5	—	5.5	V	
Quiescent Current per Amplifier	I_Q	—	18.7	25	μA	$I_O = 0$

AC CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, $V_{DD} = +2.5V$ to $+5.5V$, $V_{SS} = GND$, $T_A = 25^\circ C$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 60\text{ pF}$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	155	—	kHz	
Phase Margin	PM	—	62	—	°	$G = +1$
Slew Rate	SR	—	0.08	—	V/ μs	$G = 1$
Noise						
Input Noise Voltage	E_{ni}	—	2.8	—	μV_{P-P}	$f = 0.1\text{ Hz to }10\text{ Hz}$
Input Noise Voltage Density	e_{ni}	—	38	—	nV/ \sqrt{Hz}	$f = 1\text{ kHz}$
Input Noise Current Density	i_{ni}	—	3	—	fA/ \sqrt{Hz}	$f = 1\text{ kHz}$

MCP608 CHIP SELECT (\overline{CS}) CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, $V_{DD} = +2.5V$ to $+5.5V$, $V_{SS} = GND$, $T_A = 25^\circ C$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 60\text{ pF}$.

Parameters	Sym	Min	Typ	Max	Units	Conditions
\overline{CS} Low Specifications						
\overline{CS} Logic Threshold, Low	V_{IL}	V_{SS}	—	$0.2 V_{DD}$	V	
\overline{CS} Input Current, Low	I_{CSL}	-0.1	0.01	—	μA	$\overline{CS} = 0.2V_{DD}$
\overline{CS} High Specifications						
\overline{CS} Logic Threshold, High	V_{IH}	$0.8 V_{DD}$	—	V_{DD}	V	
\overline{CS} Input Current, High	I_{CSH}	—	0.01	0.1	μA	$\overline{CS} = V_{DD}$
\overline{CS} Input High, GND Current	I_{SS}	-2	-0.05	—	μA	$\overline{CS} = V_{DD}$
Amplifier Output Leakage, \overline{CS} High	$I_{O(LEAK)}$	—	10	—	nA	$\overline{CS} = V_{DD}$
\overline{CS} Dynamic Specifications						
\overline{CS} Low to Amplifier Output Turn-on Time	t_{ON}	—	9	100	μs	$\overline{CS} = 0.2V_{DD}$ to $V_{OUT} = 0.9(V_{DD}/2)$, $G = +1\text{ V/V}$, $R_L = 1\text{ k}\Omega$ to V_{SS}
\overline{CS} High to Amplifier Output Hi-Z	t_{OFF}	—	0.1	—	μs	$\overline{CS} = 0.8V_{DD}$ to $V_{OUT} = 0.1(V_{DD}/2)$, $G = +1\text{ V/V}$, $R_L = 1\text{ k}\Omega$ to V_{SS}
\overline{CS} Hysteresis	V_{HYST}	—	0.6	—	V	$V_{DD} = 5.0V$

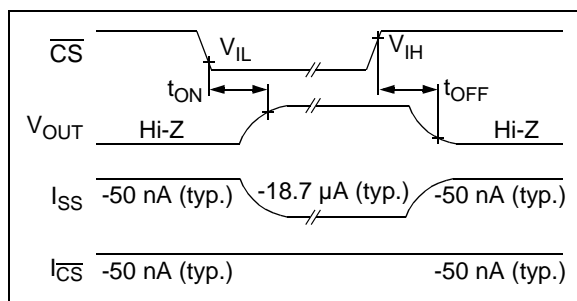


FIGURE 1-1: Timing Diagram for the \overline{CS} Pin on the MCP608.

MCP606/7/8/9

TEMPERATURE CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, $V_{DD} = +2.5V$ to $+5.5V$ and $V_{SS} = GND$.						
Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+85	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	Note 1
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-TSSOP	θ_{JA}	—	124	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note 1: The MCP606/7/8/9 operate over this extended temperature range, but with reduced performance. In any case, the Junction Temperature (T_J) must not exceed the Absolute Maximum specification of $+150^\circ\text{C}$.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, $V_{DD} = +2.5V$ to $+5.5V$, $V_{SS} = GND$, $T_A = 25^\circ C$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 60\text{ pF}$.

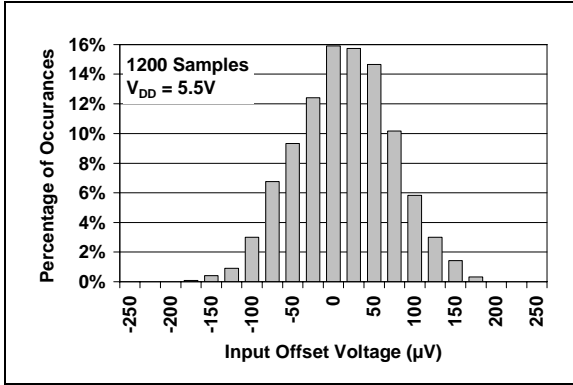


FIGURE 2-1: Input Offset Voltage at $V_{DD} = 5.5V$.

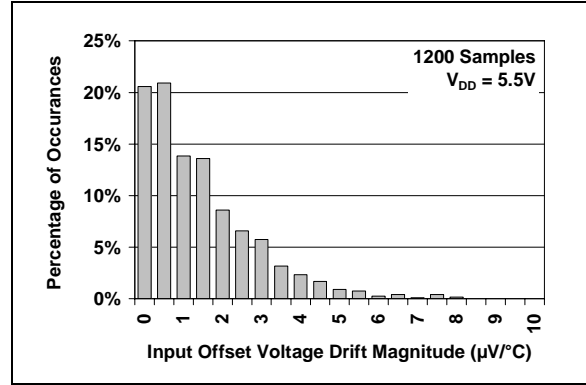


FIGURE 2-4: Input Offset Voltage Drift Magnitude at $V_{DD} = 5.5V$.

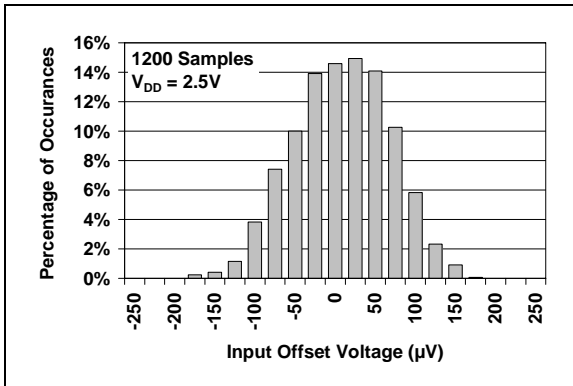


FIGURE 2-2: Input Offset Voltage at $V_{DD} = 2.5V$.

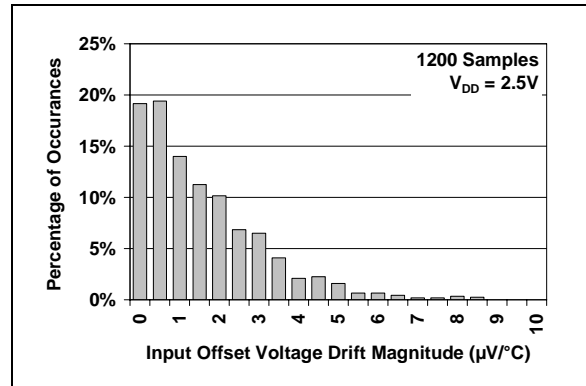


FIGURE 2-5: Input Offset Voltage Drift Magnitude at $V_{DD} = 2.5V$.

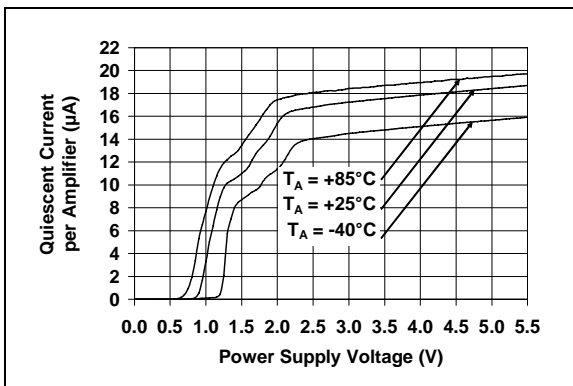


FIGURE 2-3: Quiescent Current vs. Power Supply Voltage.

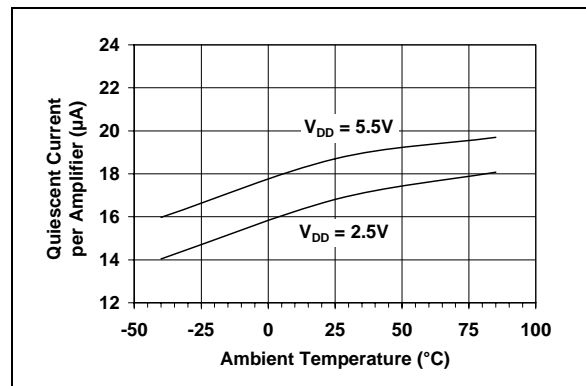


FIGURE 2-6: Quiescent Current vs. Ambient Temperature.

MCP606/7/8/9

Note: Unless otherwise indicated, $V_{DD} = +2.5V$ to $+5.5V$, $V_{SS} = GND$, $T_A = 25^\circ C$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 60\text{ pF}$.

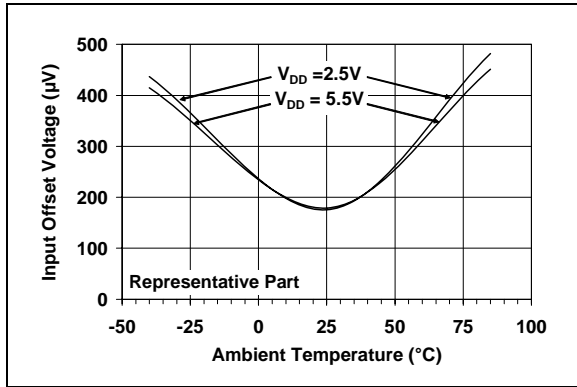


FIGURE 2-7: Input Offset Voltage vs. Ambient Temperature.

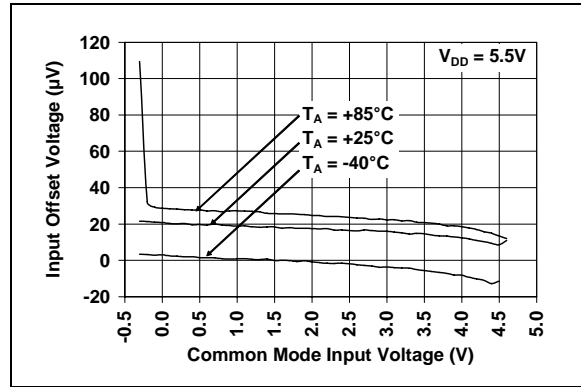


FIGURE 2-10: Input Offset Voltage vs. Common Mode Input Voltage.

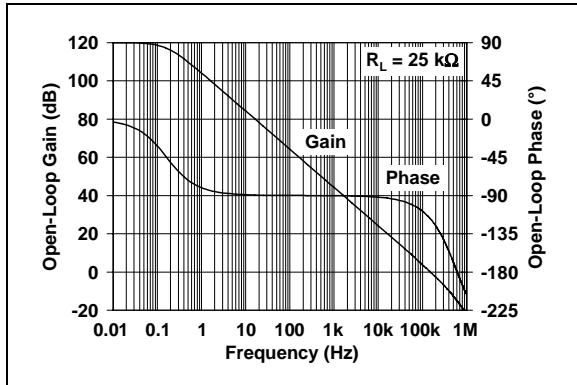


FIGURE 2-8: Open-Loop Gain and Phase vs. Frequency.

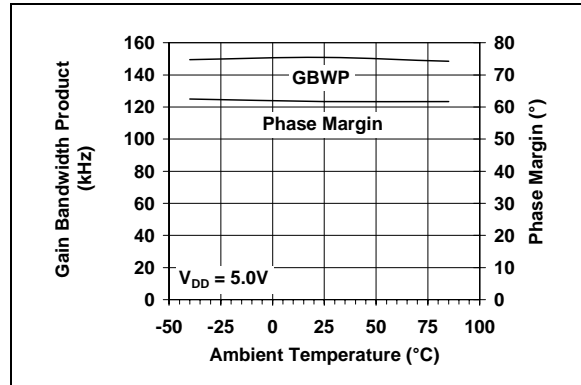


FIGURE 2-11: Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.

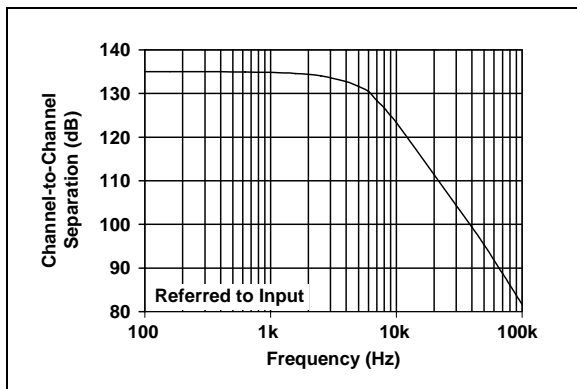


FIGURE 2-9: Channel-to-Channel Separation (MCP607 and MCP609 only).

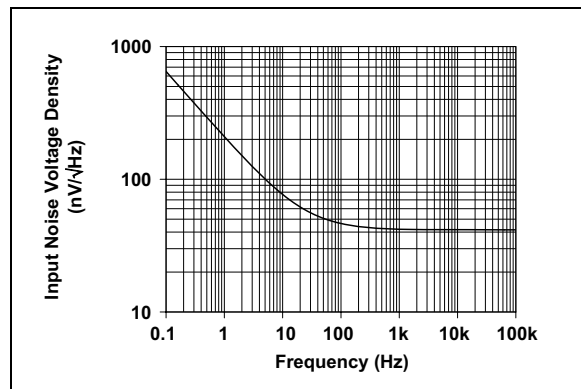


FIGURE 2-12: Input Noise Voltage Density vs. Frequency.

Note: Unless otherwise indicated, $V_{DD} = +2.5V$ to $+5.5V$, $V_{SS} = GND$, $T_A = 25^\circ C$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 60\text{ pF}$.

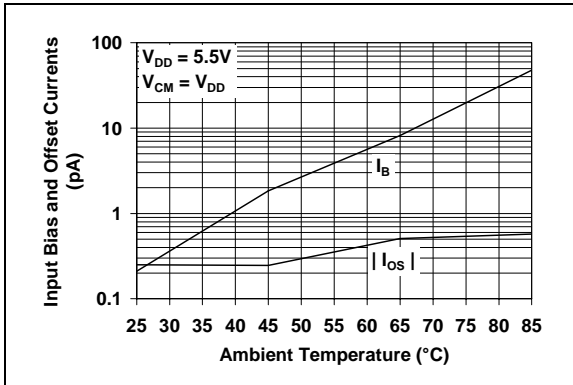


FIGURE 2-13: Input Bias Current, Input Offset Current vs. Ambient Temperature.

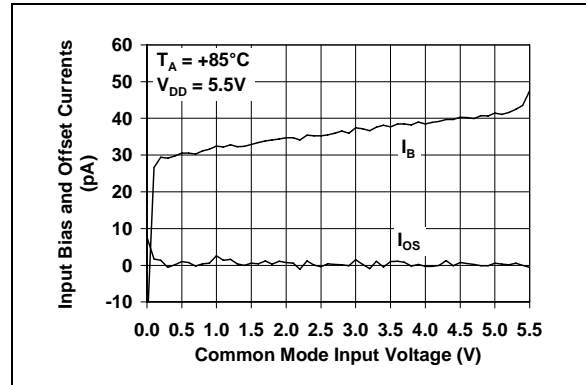


FIGURE 2-16: Input Bias Current, Input Offset Current vs. Common Mode Input Voltage.

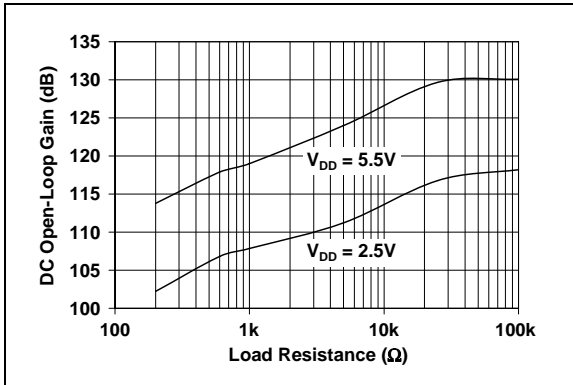


FIGURE 2-14: DC Open-Loop Gain vs. Load Resistance.

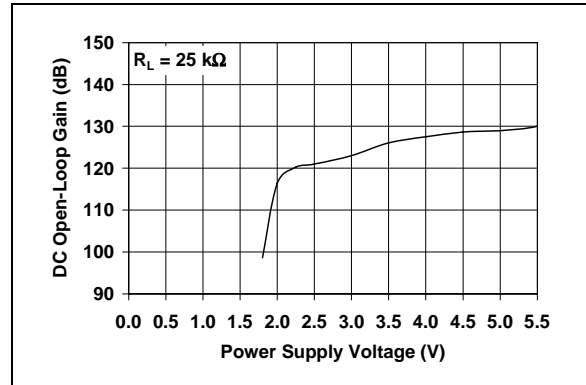


FIGURE 2-17: DC Open-Loop Gain vs. Power Supply Voltage.

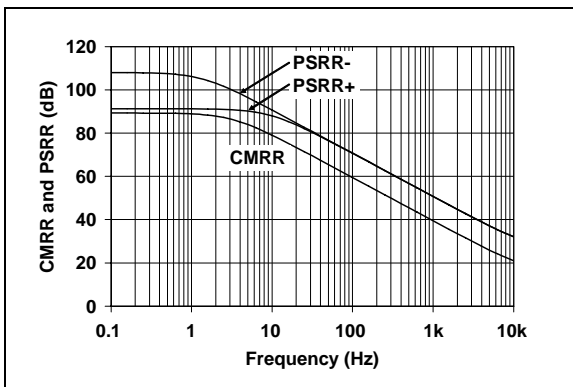


FIGURE 2-15: CMRR, PSRR vs. Frequency.

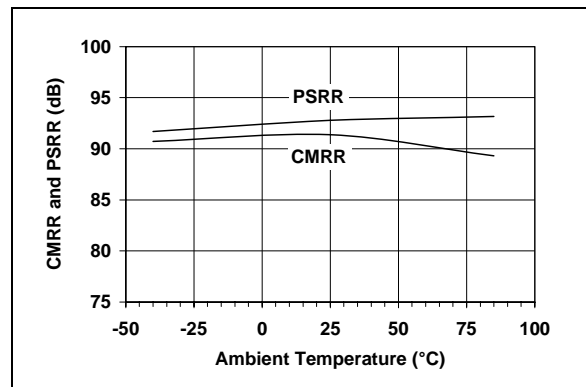


FIGURE 2-18: CMRR, PSRR vs. Ambient Temperature.

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Note: Unless otherwise indicated, $V_{DD} = +2.5V$ to $+5.5V$, $V_{SS} = GND$, $T_A = 25^\circ C$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 60\text{ pF}$.

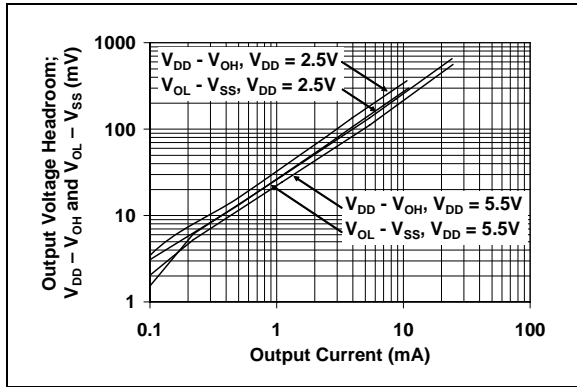


FIGURE 2-19: Output Voltage Headroom vs. Output Current Magnitude.

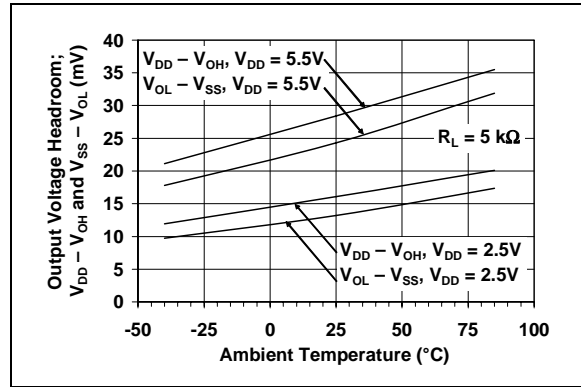


FIGURE 2-22: Output Voltage Headroom vs. Ambient Temperature at $R_L = 5\text{ k}\Omega$.

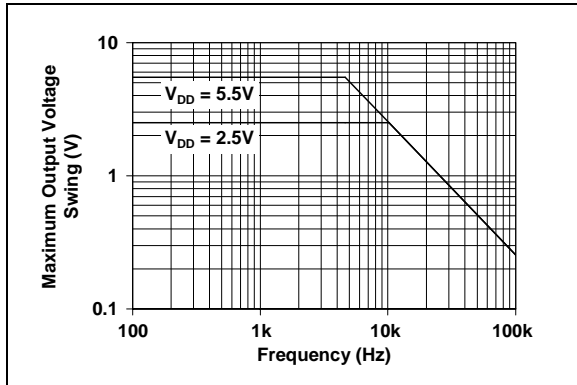


FIGURE 2-20: Maximum Output Voltage Swing vs. Frequency.

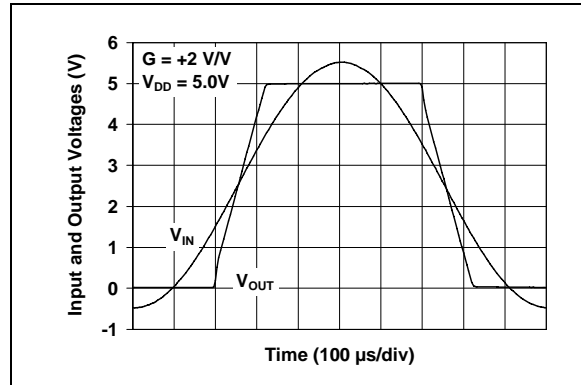


FIGURE 2-23: The MCP606/7/8/9 Show No Phase Reversal.

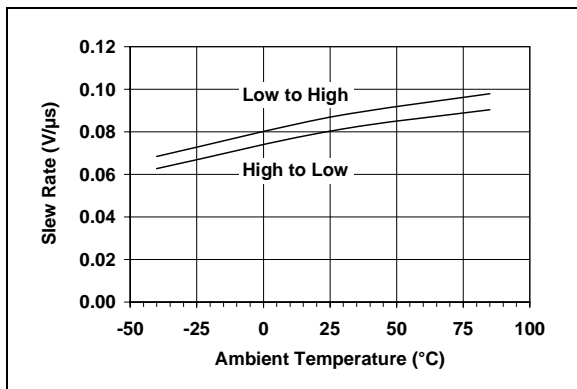


FIGURE 2-21: Slew Rate vs. Ambient Temperature.

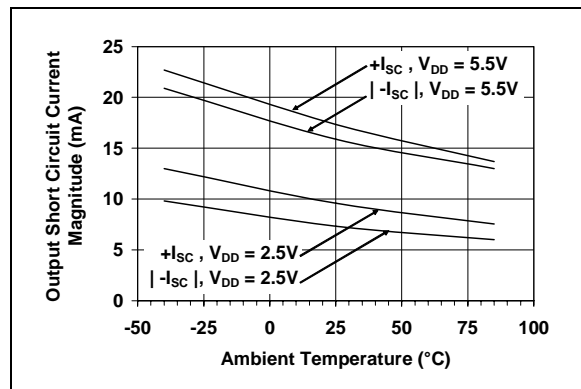


FIGURE 2-24: Output Short Circuit Current Magnitude vs. Ambient Temperature.

Note: Unless otherwise indicated, $V_{DD} = +2.5V$ to $+5.5V$, $V_{SS} = GND$, $T_A = 25^\circ C$, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, $R_L = 100\text{ k}\Omega$ to $V_{DD}/2$ and $C_L = 60\text{ pF}$.

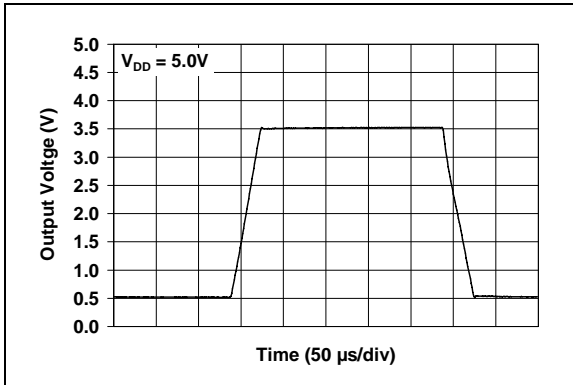


FIGURE 2-25: Large-signal, Non-inverting Pulse Response.

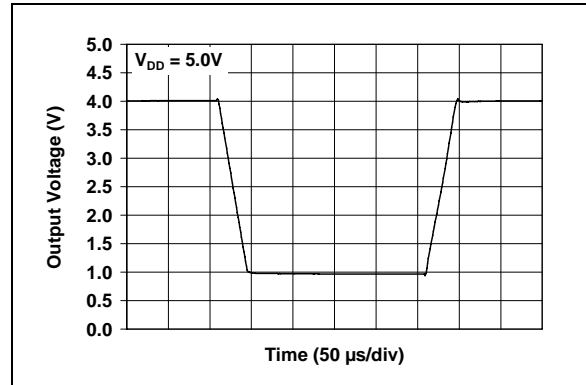


FIGURE 2-28: Large-signal, Inverting Pulse Response.

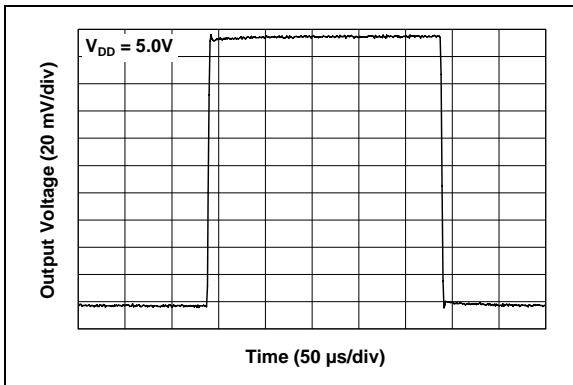


FIGURE 2-26: Small-signal, Non-inverting Pulse Response.

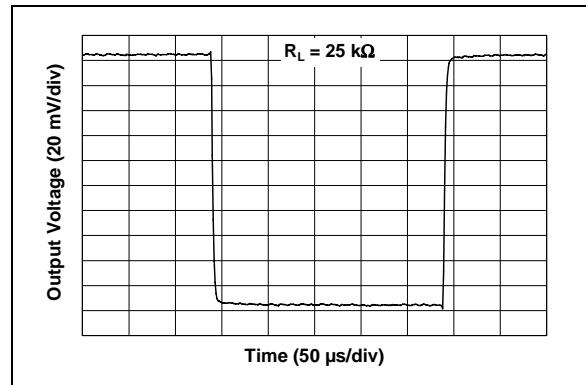


FIGURE 2-29: Small-signal, Inverting Pulse Response.

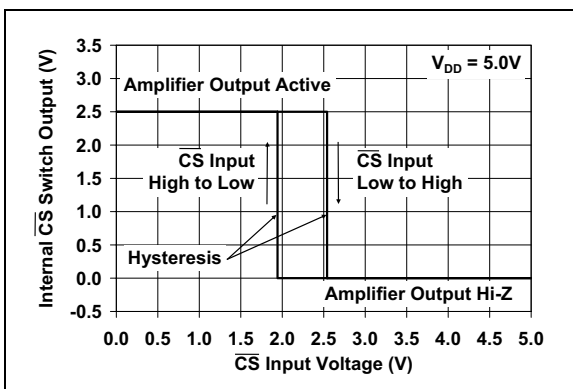


FIGURE 2-27: Chip Select (\overline{CS}) Hysteresis (MCP608 only).

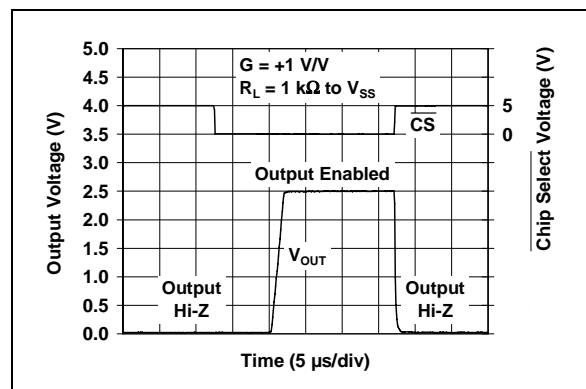


FIGURE 2-30: Amplifier Output Response Times vs. Chip Select (\overline{CS}) Pulse (MCP608 only).

MCP606/7/8/9

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE.

MCP606 (PDIP, SOIC, TSSOP)	MCP606 (SOT-23-5)	MCP607	MCP608	MCP609	Symbol	Description
6	1	1	6	1	V_{OUT}, V_{OUTA}	Output (op amp A)
2	4	2	2	2	V_{IN}^-, V_{INA}^-	Inverting Input (op amp A)
3	3	3	3	3	V_{IN}^+, V_{INA}^+	Non-inverting Input (op amp A)
7	5	4	7	4	V_{DD}	Positive Power Supply
—	—	5	—	5	V_{INB}^+	Non-inverting Input (op amp B)
—	—	6	—	6	V_{INB}^-	Inverting Input (op amp B)
—	—	7	—	7	V_{OUTB}	Output (op amp B)
—	—	—	—	8	V_{OUTC}	Output (op amp B)
—	—	—	—	9	V_{INC}^-	Inverting Input (op amp C)
—	—	—	—	10	V_{INC}^+	Non-inverting Input (op amp C)
4	2	8	4	11	V_{SS}	Negative Power Supply
—	—	—	—	12	V_{IND}^+	Non-inverting Input (op amp D)
—	—	—	—	13	V_{IND}^-	Inverting Input (op amp D)
—	—	—	—	14	V_{OUTD}	Output (op amp D)
—	—	—	8	—	\overline{CS}	Chip Select
1, 5, 8	—	—	1, 5	—	NC	No Internal Connection

3.1 Analog Outputs

The output pins are low-impedance voltage sources.

3.2 Analog Inputs

The non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.3 Power Supply (V_{SS} and V_{DD})

The positive power supply pin (V_{DD}) is 2.5V to 5.5V higher than the negative power supply pin (V_{SS}). For normal operation, the output pins are at voltages between V_{SS} and V_{DD} ; while the input pins are at voltages between $V_{SS} - 0.3V$ and $V_{DD} + 0.3V$.

Typically, these parts are used in a single-supply (positive) configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need a local bypass capacitor (typically 0.01 μF to 0.1 μF) within 2 mm of the V_{DD} pin. These parts can share a bulk capacitor with nearby analog parts (typically 1 μF or larger) within 100 mm of the V_{DD} pin.

3.4 Digital Input

The \overline{CS} (Chip Select) pin is a Schmitt-triggered, CMOS logic input. It is used to place the MCP608 op amp in a Low-power mode, with the output(s) in a Hi-Z state.

4.0 APPLICATIONS INFORMATION

The MCP606/7/8/9 family of op amps is manufactured using Microchip's state-of-the-art CMOS process. These op amps are unity-gain stable and suitable for a wide range of general purpose applications.

4.1 Inputs

The MCP606/7/8/9 op amps are designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 2-23 shows the input voltage exceeding the supply voltage without any phase reversal.

The inputs of the MCP606/7/8/9 op amps connect to a differential PMOS input stage. The Common Mode Input Voltage Range (V_{CMR}) includes ground in single-supply systems (V_{SS}), but does not include V_{DD} . This means that the amplifier input behaves linearly as long as the Common Mode Input Voltage (V_{CM}) is kept within the specified V_{CMR} limits ($V_{SS} - 0.3V$ to $V_{DD} - 1.1V$ at $+25^\circ C$).

Input voltages that exceed the Absolute Maximum Voltage Range ($V_{SS} - 0.3V$ to $V_{DD} + 0.3V$) can cause excessive current to flow into or out of the input pins. Current beyond ± 2 mA can cause reliability problems. Applications that exceed this rating must be externally limited with a resistor, as shown in Figure 4-1.

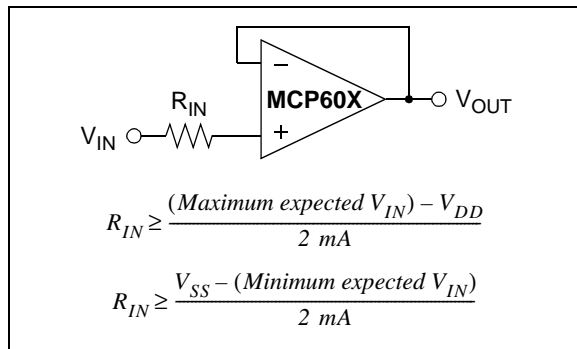


FIGURE 4-1: Input Current-Limiting Resistor (R_{IN}).

4.2 Rail-to-Rail Output

There are two specifications that describe the output-swing capability of the MCP606/7/8/9 family of op amps. The first specification (Maximum Output Voltage Swing) defines the absolute maximum swing that can be achieved under the specified load conditions. For instance, the output voltage swings to within 15 mV of the negative rail with a 25 k Ω load to $V_{DD}/2$. Figure 2-23 shows how the output voltage is limited when the input goes beyond the linear region of operation.

The second specification that describes the output-swing capability of these amplifiers (Linear Output Voltage Range) defines the maximum output swing that can be achieved while the amplifier still operates in its

linear region. To verify linear operation in this range, the large-signal DC Open-Loop Gain (A_{OL}) is measured at points inside the supply rails. The measurement must meet the specified A_{OL} conditions in the specification table.

4.3 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage-feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain-peaking in the frequency response, with overshoot and ringing in the step response. A unity-gain buffer ($G = +1$) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 60 pF when $G = +1$), a small series resistor at the output (R_{ISO} in Figure 4-2) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

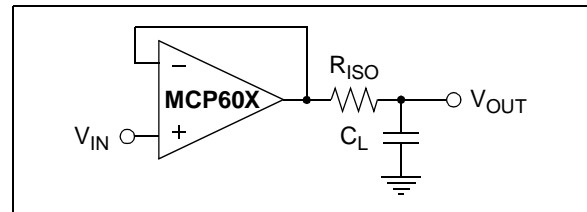


FIGURE 4-2: Output Resistor, R_{ISO} stabilizes large capacitive loads.

Figure 4-3 gives recommended R_{ISO} values for different capacitive loads and gains. The x-axis is the normalized load capacitance (C_L/G_N), where G_N is the circuit's noise gain. For non-inverting gains, G_N and the Signal Gain are equal. For inverting gains, G_N is $1 + |\text{Signal Gain}|$ (e.g., -1 V/V gives $G_N = +2$ V/V).

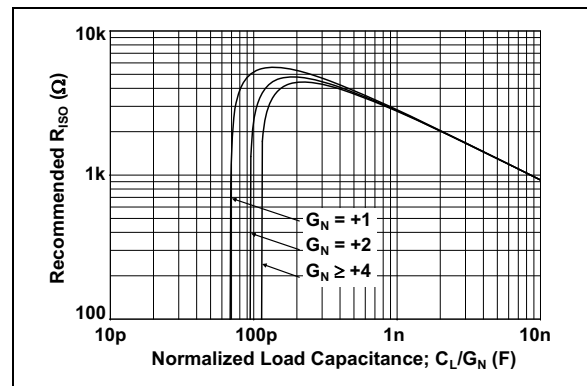


FIGURE 4-3: Recommended R_{ISO} Values for Capacitive Loads.

MCP606/7/8/9

After selecting R_{ISO} for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify R_{ISO} 's value until the response is reasonable. Bench evaluation and simulations with the MCP606/7/8/9 SPICE macro model are helpful.

4.4 MCP608 Chip Select (\overline{CS})

The MCP608 is a single op amp with Chip Select (\overline{CS}). When \overline{CS} is pulled high, the supply current drops to 50 nA (typ.) and flows through the \overline{CS} pin to V_{SS} . When this happens, the amplifier output is put into a high-impedance state. By pulling \overline{CS} low, the amplifier is enabled. If the \overline{CS} pin is left floating, the amplifier may not operate properly. Figure 1-1 shows the output voltage and supply current response to a \overline{CS} pulse.

4.5 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single-supply) should have a local bypass capacitor (i.e., 0.01 μ F to 0.1 μ F) within 2 mm for good high-frequency performance. It also needs a bulk capacitor (i.e., 1 μ F or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other nearby analog parts.

4.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface-leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow, which is greater than the MCP606/7/8/9 family's bias current at 25°C (1 pA, typ.).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-4.

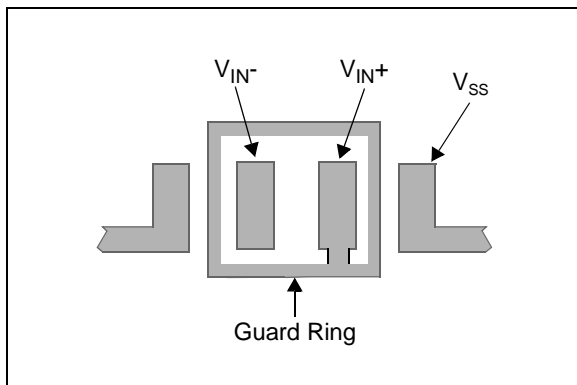


FIGURE 4-4: Example Guard Ring Layout for Inverting Gain.

1. Non-inverting Gain and Unity-gain Buffer:
 - a) Connect the non-inverting pin (V_{IN+}) to the input with a wire that does not touch the PCB surface.
 - b) Connect the guard ring to the inverting input pin (V_{IN-}). This biases the guard ring to the common mode input voltage.
2. Inverting Gain and Transimpedance Gain (convert current to voltage, such as photo detectors) amplifiers:
 - a) Connect the guard ring to the non-inverting input pin (V_{IN+}). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
 - b) Connect the inverting pin (V_{IN-}) to the input with a wire that does not touch the PCB surface.

4.7 Application Circuits

4.7.1 LOW-SIDE BATTERY CURRENT SENSOR

The MCP606/7/8/9 op amps can be used to sense the load current on the low-side of a battery using the circuit in Figure 4-5. In this circuit, the current from the power supply (minus the current required to power the MCP606) flows through a sense resistor (R_{SEN}), which converts it to voltage. This is gained by the the amplifier and resistors, R_G and R_F . Since the non-inverting input of the amplifier is at the load's negative supply (V_{LM}), the gain from R_{SEN} to V_{OUT} is R_F/R_G .

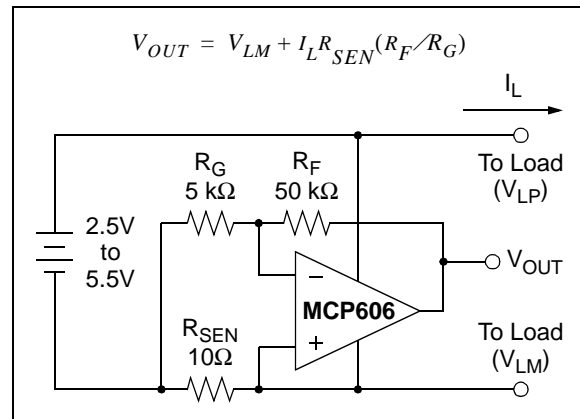


FIGURE 4-5: Low Side Battery Current Sensor.

Since the input bias current and input offset voltage of the MCP606 are low, and the input is capable of swinging below ground, there is very little error generated by the amplifier. The quiescent current is very low, which helps conserve battery power. The rail-to-rail output makes it possible to read very low currents.

4.7.2 PHOTODIODE AMPLIFIERS

Sensors that produce an output current and have high output impedance can be connected to a transimpedance amplifier. The transimpedance amplifier converts the current into voltage. Photodiodes are one sensor that produce an output current.

The key op amp characteristics that are needed for these circuits are: low input offset voltage, low input bias current, high input impedance and an input common mode range that includes ground. The low input offset voltage and low input bias current support a very low voltage drop across the photodiode; this gives the best photodiode linearity. Since the photodiode is biased at ground, the op amp's input needs to function well both above and below ground.

4.7.2.1 Photo-Voltaic Mode

Figure 4-6 shows a transimpedance amplifier with a photodiode (D_1) biased in the Photo-voltaic mode (0V across D_1), which is used for precision photodiode sensing.

As light impinges on D_1 , charge is generated, causing a current to flow in the reverse bias direction of D_1 . The op amp's negative feedback forces the voltage across the D_1 to be nearly 0V. Resistor R_2 converts the current into voltage. Capacitor C_2 limits the bandwidth and helps stabilize the circuit when D_1 's junction capacitance is large.

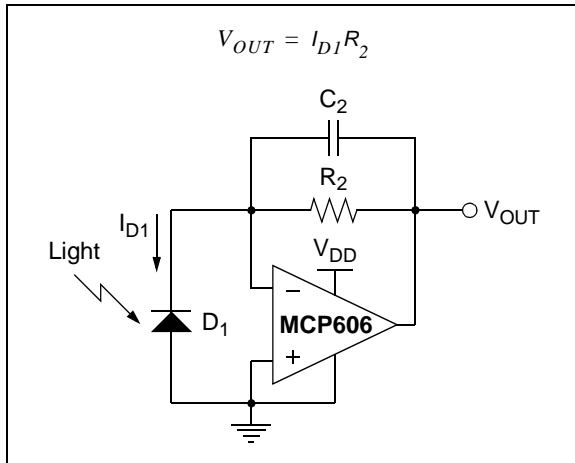


FIGURE 4-6: Photodiode (in Photo-voltaic mode) and Transimpedance Amplifier.

4.7.2.2 Photo-Conductive Mode

Figure 4-6 shows a transimpedance amplifier with a photodiode (D_1) biased in the Photo-conductive mode (D_1 is reverse biased), which is used for high-speed applications.

As light impinges on D_1 , charge is generated, causing a current to flow in the reverse bias direction of D_1 . Placing a negative bias on D_1 significantly reduces its junction capacitance, which allows the circuit to

operate at a much higher speed. This reverse bias also increases the dark current and current noise, however. Resistor R_2 converts the current into voltage. Capacitor C_2 limits the bandwidth and helps stabilize the circuit when D_1 's junction capacitance is large.

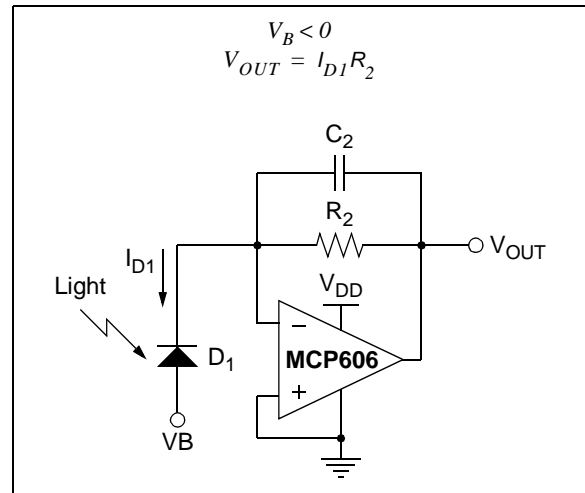


FIGURE 4-7: Photodiode (in Photo-conductive mode) and Transimpedance Amplifier.

4.7.3 TWO OP AMP INSTRUMENTATION AMPLIFIER

The two op amp instrumentation amplifier shown in Figure 4-8 serves the function of taking the difference of two input voltages, level-shifting it and gaining it to the output. This configuration is best suited for higher gains (i.e., gain > 3 V/V). The reference voltage (V_{REF}) is typically at mid-supply ($V_{DD}/2$) in a single-supply environment.

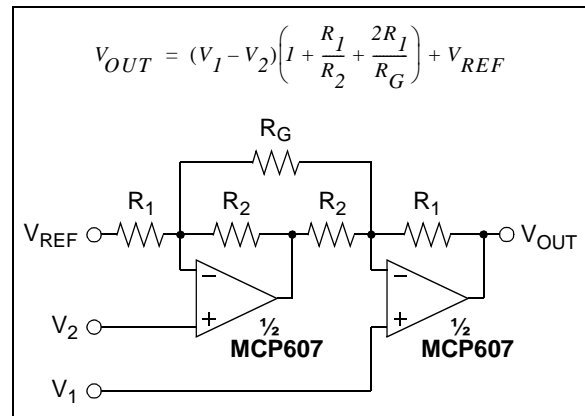


FIGURE 4-8: Two op amp Instrumentation Amplifier.

The key specifications that make the MCP606/7/8/9 family appropriate for this application circuit are low input bias current, low offset voltage and high common-mode rejection.

MCP606/7/8/9

4.7.4 THREE OP AMP INSTRUMENTATION AMPLIFIER

A classic, three op amp instrumentation amplifier is illustrated in Figure 4-9. The two input op amps provide differential signal gain and a common mode gain of +1. The output op amp is a difference amplifier, which converts its input signal from differential to a single ended output; it rejects common mode signals at its input. The gain of this circuit is simply adjusted with one resistor (R_G). The reference voltage (V_{REF}) is typically referenced to mid-supply ($V_{DD}/2$) in single-supply applications.

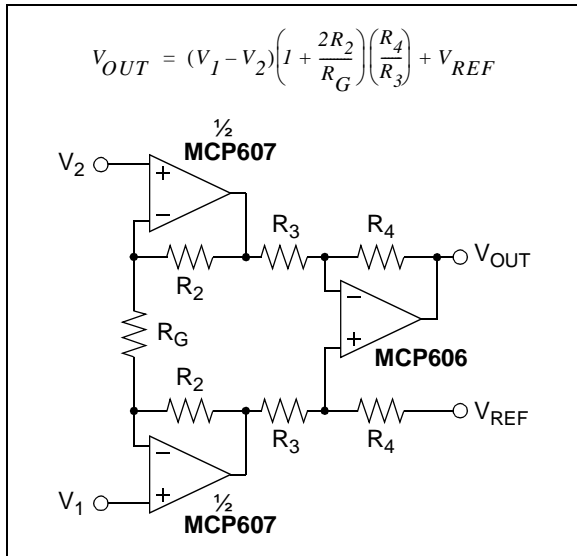


FIGURE 4-9: Three op amp Instrumentation Amplifier.

4.7.5 PRECISION GAIN WITH GOOD LOAD ISOLATION

In Figure 4-10, the MCP606 op amps, R_1 and R_2 provide a high gain to the input signal (V_{IN}). The MCP606's low offset voltage makes this an accurate circuit.

The MCP601 is configured as a unity-gain buffer. It isolates the MCP606's output from the load, increasing the high-gain stage's precision. Since the MCP601 has a higher output current, with the two amplifiers being housed in separate packages, there is minimal change in the MCP606's offset voltage due to loading effect.

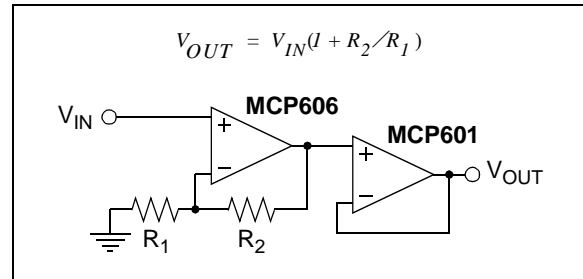


FIGURE 4-10: Precision Gain with Good Load Isolation.

5.0 DESIGN TOOLS

Microchip provides the basic design tools needed for the MCP606/7/8/9 family of op amps.

5.1 SPICE Macro Model

The latest SPICE macro model for the MCP606/7/8/9 op amps is available on our web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation at room temperature. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

5.2 FilterLab[®] Software

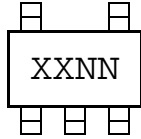
The FilterLab software is an innovative tool that simplifies analog active-filter (using op amps) design. It is available free of charge from our web site at www.microchip.com. The FilterLab software tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

MCP606/7/8/9

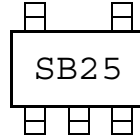
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

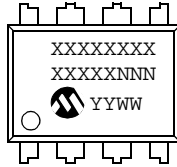
5-Lead SOT-23-5



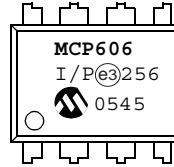
Example:



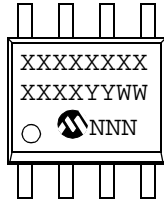
8-Lead PDIP (300 mil)



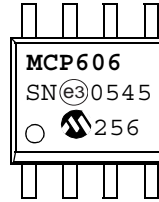
Example:



8-Lead SOIC (150 mil)



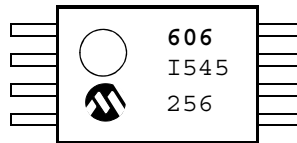
Example:



8-Lead TSSOP



Example:

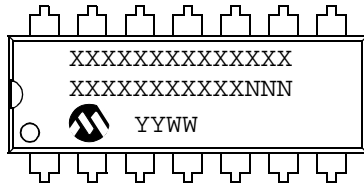


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

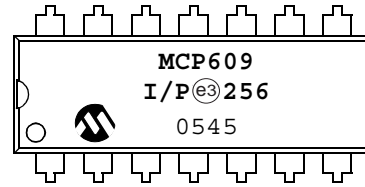
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

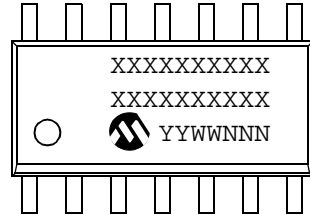
14-Lead PDIP (300 mil) (MCP609)



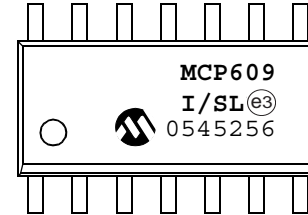
Example:



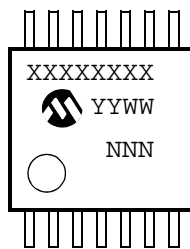
14-Lead SOIC (150 mil) (MCP609)



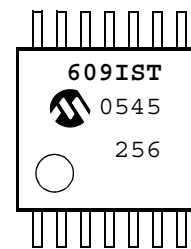
Example:



14-Lead TSSOP (MCP609)

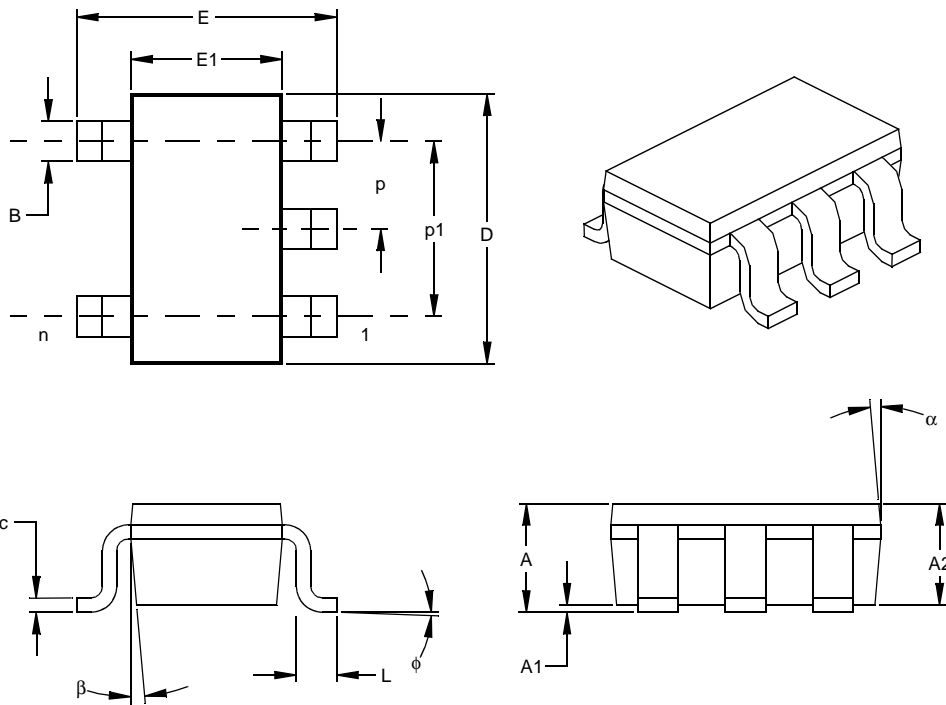


Example:



MCP606/7/8/9

5-Lead Plastic Small Outline Transistor (OT) (SOT23)



Dimension Limits		INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		5			5	
Pitch	p		.038			0.95	
Outside lead pitch (basic)	p1		.075			1.90	
Overall Height	A	.035	.046	.057	0.90	1.18	1.45
Molded Package Thickness	A2	.035	.043	.051	0.90	1.10	1.30
Standoff §	A1	.000	.003	.006	0.00	0.08	0.15
Overall Width	E	.102	.110	.118	2.60	2.80	3.00
Molded Package Width	E1	.059	.064	.069	1.50	1.63	1.75
Overall Length	D	.110	.116	.122	2.80	2.95	3.10
Foot Length	L	.014	.018	.022	0.35	0.45	0.55
Foot Angle	φ	0	5	10	0	5	10
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.014	.017	.020	0.35	0.43	0.50
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter

§ Significant Characteristic

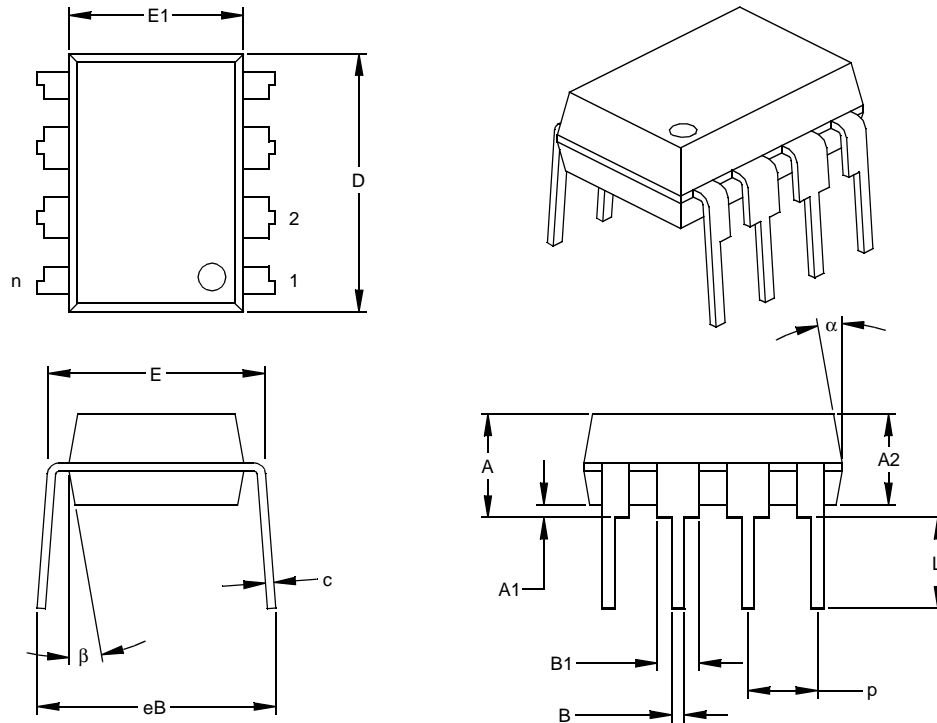
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-178

Drawing No. C04-091

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



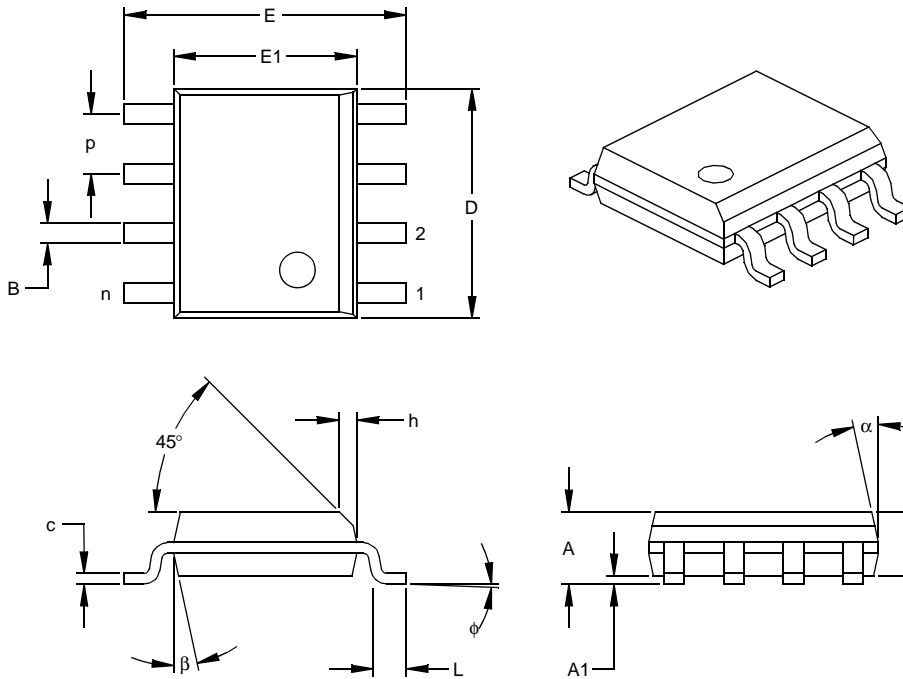
Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
 § Significant Characteristic

Notes:
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
 JEDEC Equivalent: MS-001
 Drawing No. C04-018

MCP606/7/8/9

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter

§ Significant Characteristic

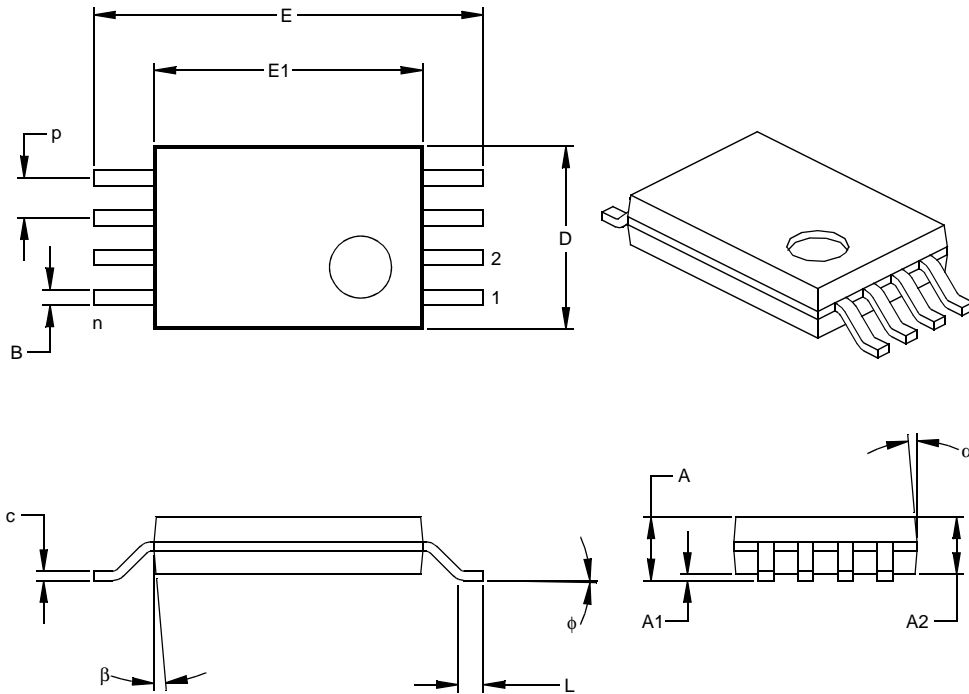
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



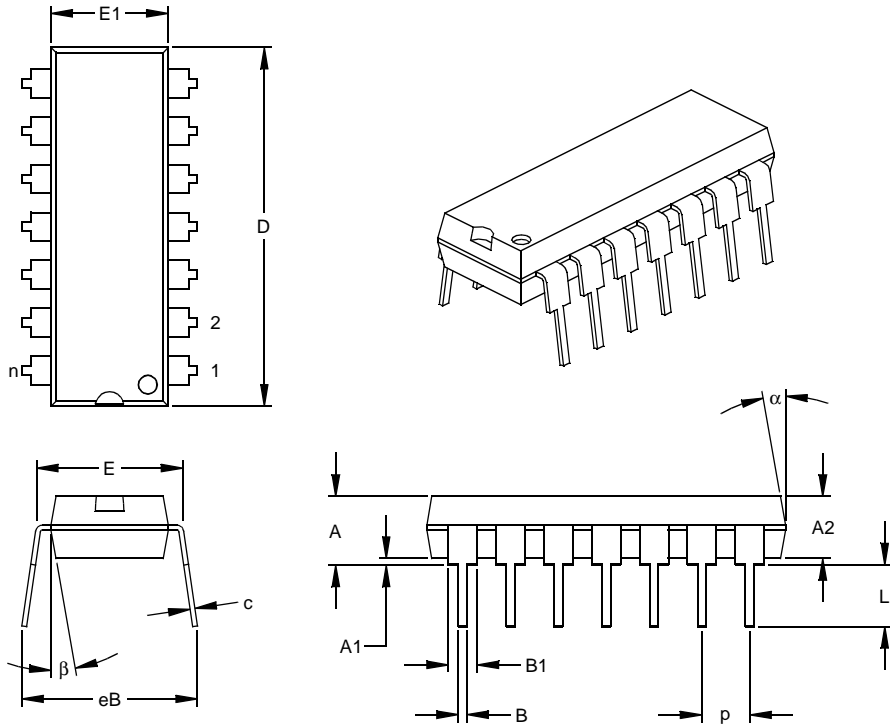
Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.114	.118	.122	2.90	3.00	3.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
 § Significant Characteristic

Notes:
 Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.
 JEDEC Equivalent: MO-153
 Drawing No. C04-086

MCP606/7/8/9

14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Dimension Limits	Units	INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

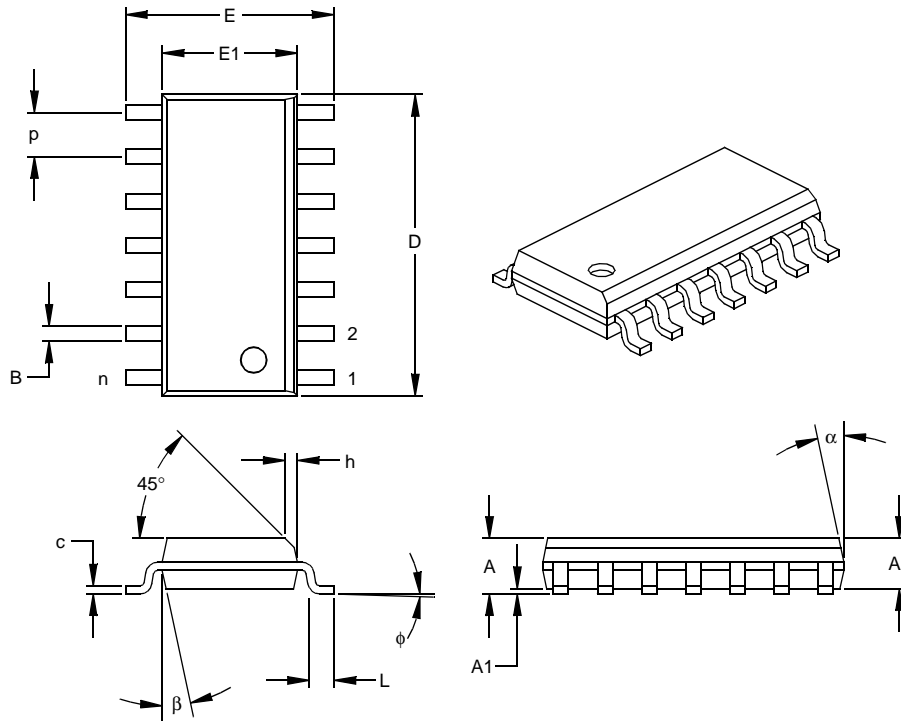
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-005

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter

§ Significant Characteristic

Notes:

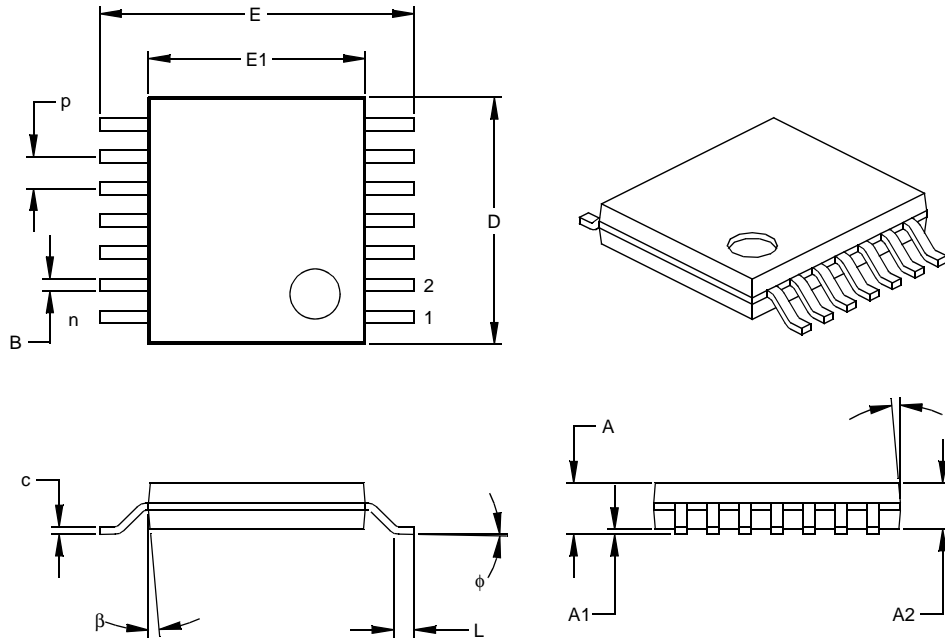
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-065

MCP606/7/8/9

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
 § Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" (0.127mm) per side.

JEDEC Equivalent: MO-153

Drawing No. C04-087

APPENDIX A: REVISION HISTORY

Revision D (February 2005)

The following is the list of modifications:

1. Added **Section 3.0 “Pin Descriptions”**.
2. Updated **Section 4.0 “Applications Information”**.
3. Added **Section 4.3 “Capacitive Loads”**
4. Updated **Section 5.0 “Design Tools”** to include FilterLab[®] and to point to the latest SPICE macro model.
5. Corrected and updated **Section 6.0 “Packaging Information”**.
6. Added **Section Appendix A: “Revision History”**.

Revision C (January 2001)

Revision B (May 2000)

Revision A (January 2000)

- Original Release of this Document.

MCP606/7/8/9

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	
Device	Temperature Range	Package	
Device			MCP606 = Single Op Amp MCP606T = Single Op Amp Tape and Reel (SOIC, TSSOP) MCP607 = Dual Op Amp MCP607T = Dual Op Amp Tape and Reel (SOIC, TSSOP) MCP608 = Single Op Amp with \overline{CS} MCP608T = Single Op Amp with \overline{CS} Tape and Reel (SOIC, TSSOP) MCP609 = Quad Op Amp MCP609T = Quad Op Amp Tape and Reel (SOIC, TSSOP)
Temperature Range	I	=	-40°C to +85°C
Package			OT = Plastic SOT-23, 5-lead P = Plastic DIP (300 mil Body), 8-lead & 14-lead SN = Plastic SOIC (150 mil Body), 8-lead SL = Plastic SOIC (150 mil Body), 14-lead ST = Plastic TSSOP, 8-lead & 14-lead

Examples:

- a) MCP606-I/P: Industrial Temperature, 8LD PDIP package.
- b) MCP606-I/SN: Industrial Temperature, 8LD SOIC package.
- c) MCP606T-I/SN: Tape and Reel, Industrial Temperature, 8LD SOIC package.
- d) MCP606-I/ST: Industrial Temperature, 8LD TSSOP package.
- e) MCP606-I/OT: Industrial Temperature, 5LD SOT-23 package.
- f) MCP606T-I/OT: Tape and Reel, Industrial Temperature, 5LD SOT-23 package.

- a) MCP607-I/P: Industrial Temperature, 8LD PDIP package.
- b) MCP607T-I/P: Industrial Temperature, 8LD PDIP package.

- a) MCP608-I/SN: Industrial Temperature, 8LD SOIC package.
- b) MCP608T-I/SN: Tape and Reel, Industrial Temperature, 8LD SOIC package.

- a) MCP609-I/P: Industrial Temperature, 14LD PDIP package.
- b) MCP609T-I/P: Industrial Temperature, 14LD PDIP package.

MCP606/7/8/9

NOTES:

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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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