MICROCHIP

MCP6271/2/3/4

170 µA, 2 MHz Bandwidth, Rail-to-Rail Op Amp

Features

- 2 MHz Gain Bandwidth Product (typ.)
- Supply Current: I_Q = 170 µA (typ.)
- Supply Voltage: 2.0V to 5.5V
- Rail-to-Rail Input/Output
- Extended Temperature Range: -40°C to +125°C
- Available in Single, Dual and Quad Packages
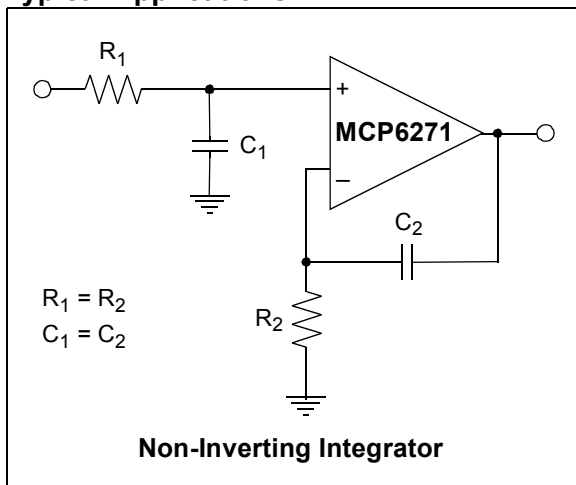- Single with Chip Select ($\overline{CS}$) (MCP6273)

Applications

- Automotive
- Portable Equipment
- Photodiode Pre-amps
- Analog Filters
- Notebooks and PDAs
- Battery-Powered Systems

Available Tools

- SPICE Macro Model (at www.microchip.com)
- FilterLab® Software (at www.microchip.com)

Typical Applications

$R_1 = R_2$
$C_1 = C_2$

Non-Inverting Integrator

Description

The Microchip Technology Inc. MCP6271/2/3/4 family of operational amplifiers (op amps) provide wide bandwidth for the current. This family has a 2 MHz gain bandwidth product and 65° phase margin. This family also operates from a single supply voltage as low as 2.0V, while drawing 170 µA (typ.) quiescent current. Additionally, the MCP6271/2/3/4 supports rail-to-rail input and output swing, with a common mode input voltage range of V_{DD} + 300 mV to V_{SS} - 300 mV. This family of operational amplifiers is designed with Microchip's advanced CMOS process.

The MCP6271/2/3/4 family operates in the Extended Temperature Range of -40°C to +125°C. It also has a power supply range of 2.0V to 5.5V.

Package Types
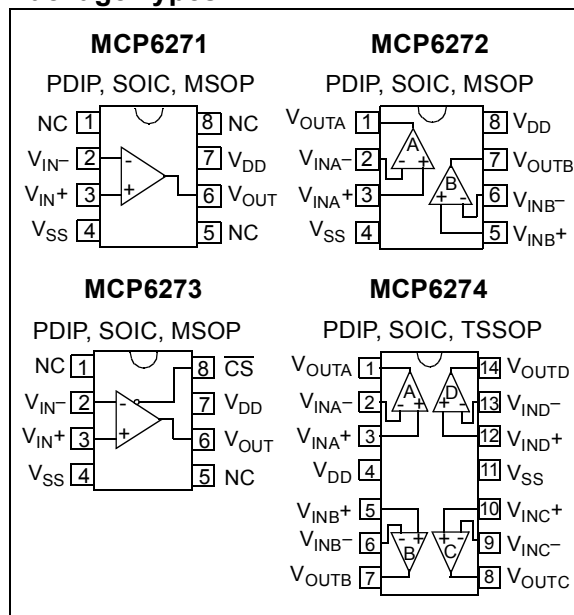
MCP6271/2/3/4

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{DD} - V_{SS} 7.0V

All Inputs and Outputs .... V_{SS} -0.3V to V_{DD} +0.3V

Difference Input Voltage .... |V_{DD} - V_{SS}|

Output Short Circuit Current ....continuous

Current at Input Pins ....±2 mA

Current at Output and Supply Pins ....±30 mA

Storage Temperature ....-65°C to +150°C

Junction Temperature (T_J) ....+150°C

ESD Protection On All Pins (HBM/MM) .... ≥ 4 kV/200V

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
$V_{IN}+$, $V_{INA}+$, $V_{INB}+$, $V_{INC}+$, $V_{IND}+$	Non-inverting Inputs
$V_{IN}-$, $V_{INA}-$, $V_{INB}-$, $V_{INC}-$, $V_{IND}-$	Inverting Inputs
V_{DD}	Positive Power Supply
V_{SS}	Negative Power Supply
V_{OUT}, V_{OUTA}, V_{OUTB}, V_{OUTC}, V_{OUTD}	Outputs
NC	No Internal Connection
$\overline{CS}$	Chip Select

DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, R_L = 10 kΩ to V_{DD}/2, and V_{OUT} ≈ V_{DD}/2.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input Offset						
Input Offset Voltage	V_{OS}	-3.0	—	+3.0	mV	V_{CM} = V_{SS}
Input Offset Voltage (Extended Temperature)	V_{OS}	-5.0	—	+5.0	mV	T_A= -40°C to +125°C, V_{CM} = V_{SS}
Input Offset Temperature Drift	$\Delta V_{OS}/\Delta T_A$	—	±1.5	—	µV/°C	T_A= -40°C to +125°C
Power Supply Rejection	PSRR	70	90	—	dB	V_{CM} = V_{SS}
Input Bias Current and Impedance						
Input Bias Current	I_B	—	±1.0	—	pA	
Overtemperature	I_B	—	50	200	pA	T_A= +85°C
Overtemperature	I_B	—	2	5	nA	T_A= +125°C
Input Offset Current	I_{OS}	—	±1.0	—	pA	
Common Mode Input Impedance	Z_{CM}	—	10^{13}||6	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||3	—	Ω||pF	
Common Mode						
Common Mode Input Range	V_{CMR}	$V_{SS} - 0.3$	—	$V_{DD} + 0.3$	V	
Common Mode Rejection Ratio	CMRR	70	85	—	dB	V_{CM} = -0.3V to 2.5V, V_{DD} = 5V
Common Mode Rejection Ratio	CMRR	65	80	—	dB	V_{CM} = -0.3V to 5.3V, V_{DD} = 5V
Open-Loop Gain						
DC Open-Loop Gain (large signal)	A_{OL}	90	110	—	dB	V_{OUT} = 0.2V to V_{DD} - 0.2V, V_{CM} = V_{SS}
Output						
Maximum Output Voltage Swing	V_{OL}, V_{OH}	V_{SS} + 15	—	V_{DD} – 15	mV	
Output Short-Circuit Current	I_{SC}	—	±25	—	mA	
Power Supply						
Supply Voltage	V_{DD}	2.0	—	5.5	V	
Quiescent Current per Amplifier	I_Q	100	170	240	µA	I_O = 0

AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2, and C_L = 60 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
AC Response						
Gain Bandwidth Product	GBWP	—	2.0	—	MHz	
Phase Margin at Unity Gain	PM	—	65	—	°	
Slew Rate	SR	—	0.9	—	V/µs	
Noise						
Input Noise Voltage	E_{ni}	—	3.5	—	µVp-p	f = 0.1 Hz to 10 Hz
Input Noise Voltage Density	e_{ni}	—	20	—	nV/√Hz	f = 1 kHz
Input Noise Current Density	i_{ni}	—	3	—	fA/√Hz	f = 1 kHz

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{DD} = +2.0V to +5.5V, and V_{SS} = GND.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	**(Note)**
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 5L-SOT-23	θ_{JA}	—	256	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	85	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	163	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	—	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	120	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

Note: The Junction Temperature (T_J) must not exceed the Absolute Maximum specification of +150°C.

MCP6271/2/3/4

MCP6273 CHIP SELECT ($\overline{\text{CS}}$) SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, $V_{CM} = V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 10 kΩ to $V_{DD}/2$, and C_L = 60 pF.

Parameters	Sym	Min	Typ	Max	Units	Conditions
$\overline{\text{CS}}$ Low Specifications						
$\overline{\text{CS}}$ Logic Threshold, Low	V_{IL}	V_{SS}	—	0.2 V_{DD}	V	
$\overline{\text{CS}}$ Input Current, Low	I_{CSL}	—	0.01	—	µA	$\overline{\text{CS}} = V_{SS}$
$\overline{\text{CS}}$ High Specifications						
$\overline{\text{CS}}$ Logic Threshold, High	V_{IH}	0.8 V_{DD}	—	V_{DD}	V	
$\overline{\text{CS}}$ Input Current, High	I_{CSH}	—	0.7	2	µA	$\overline{\text{CS}} = V_{DD}$
$\overline{\text{CS}}$ Input High, GND Current	I_Q	—	-0.7	—	µA	$\overline{\text{CS}} = V_{DD}$
Amplifier Output Leakage, $\overline{\text{CS}}$ High	—	—	0.01	—	µA	$\overline{\text{CS}} = V_{DD}$
Dynamic Specifications						
$\overline{\text{CS}}$ Low to Valid Amplifier Output, Turn-on Time	t_{ON}	—	4	10	µs	$\overline{\text{CS}}$ Low ≤ 0.2 V_{DD}, G = +1 V/V, $V_{IN} = V_{DD}/2$, V_{OUT} = 0.9 $V_{DD}/2$, V_{DD} = 5.0V
$\overline{\text{CS}}$ High to Amplifier Output High-Z	t_{OFF}	—	0.01	—	µs	$\overline{\text{CS}}$ High ≥ 0.8 V_{DD}, G = +1 V/V, $V_{IN} = V_{DD}/2$, V_{OUT} = 0.1 $V_{DD}/2$
Hysteresis	V_{HYST}	—	0.6	—	V	V_{DD} = 5V

2.0   TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 10 kΩ to $V_{DD}/2$ and C_L = 60 pF.
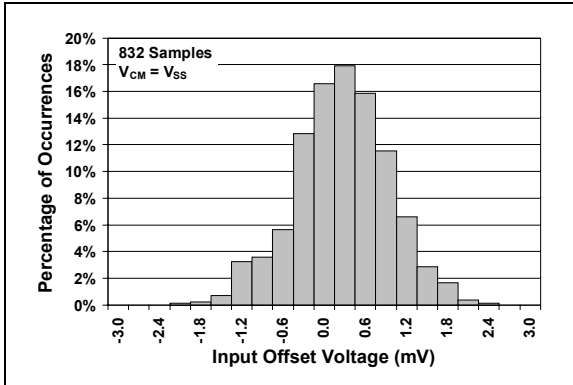
FIGURE 2-1:   *Histogram of Input Offset Voltage.*

FIGURE 2-2:   *Histogram of Input Bias Current with T_A = +85°C.*

FIGURE 2-3:   *Input Offset Voltage vs. Common Mode Input Voltage with V_{DD} = 2.0V.*
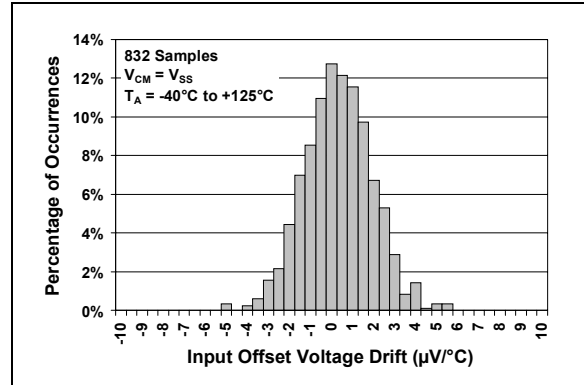
FIGURE 2-4:   *Histogram of Input Offset Voltage Drift.*
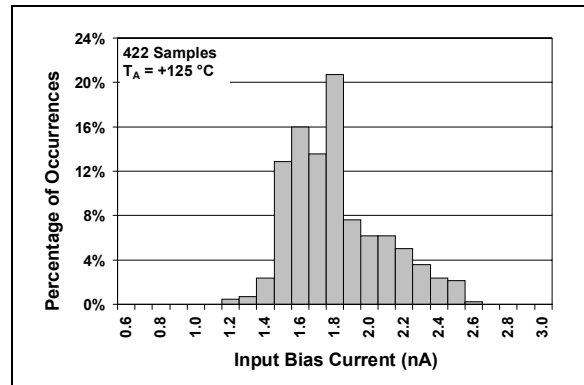
FIGURE 2-5:   *Histogram of Input Bias Current with T_A = +125°C.*
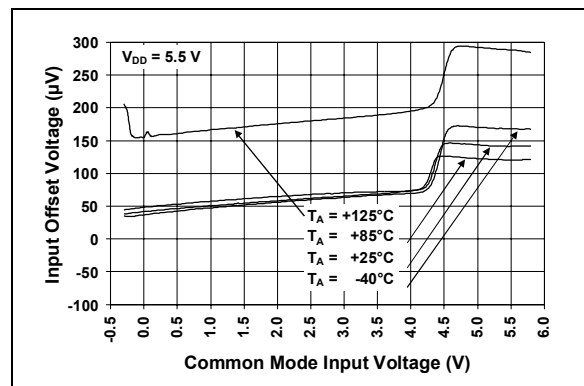
FIGURE 2-6:   *Input Offset Voltage vs. Common Mode Input Voltage with V_{DD} = 5.5V.*

MCP6271/2/3/4

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.
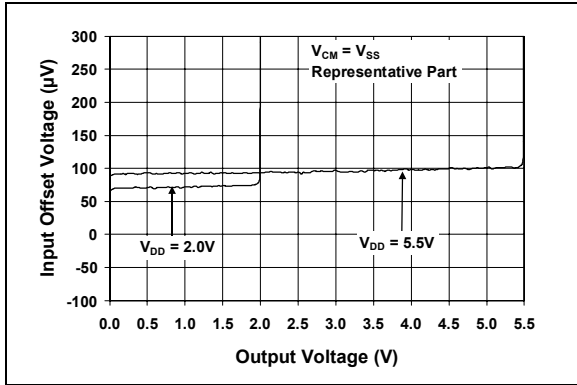
FIGURE 2-7: *Input Offset Voltage vs. Output Voltage.*

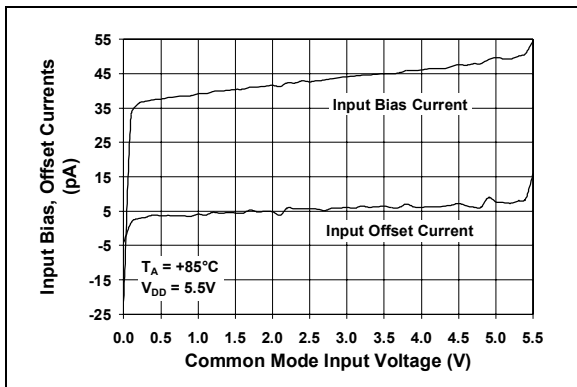**FIGURE 2-8:** *CMRR, PSRR vs. Frequency with V_{DD} = 5.0V.*

FIGURE 2-9: *Input Bias, Input Offset Currents vs. Common Mode Input Voltage with T_A = +85°C.*

FIGURE 2-10: *Input Bias, Input Offset Currents vs. Ambient Temperature.*

FIGURE 2-11: *CMRR, PSRR vs. Ambient Temperature.*
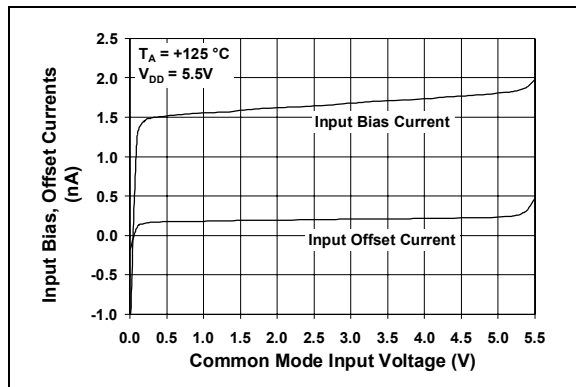
FIGURE 2-12: *Input Bias, Input Offset Currents vs. Common Mode Input Voltage with T_A = +125°C.*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = V_{DD}/2, V_{OUT} ≈ V_{DD}/2, R_L = 10 kΩ to V_{DD}/2 and C_L = 60 pF.
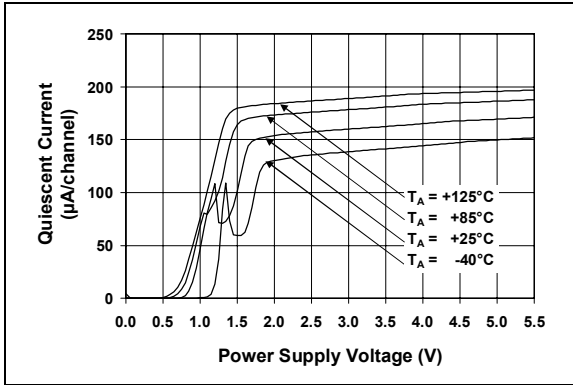
FIGURE 2-13: *Quiescent Current vs. Power Supply Voltage.*

FIGURE 2-14: *Open-Loop Gain, Phase vs. Frequency.*

FIGURE 2-15: *Maximum Output Voltage Swing vs. Frequency.*

FIGURE 2-16: *Output Voltage Headroom vs. Output Current Magnitude.*

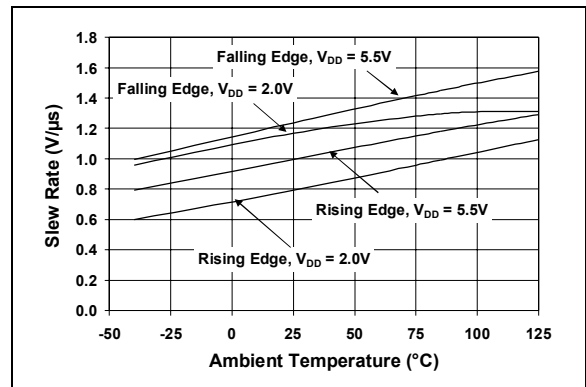**FIGURE 2-17:** *Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.*

FIGURE 2-18: *Slew Rate vs. Ambient Temperature.*

MCP6271/2/3/4

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 10 kΩ to $V_{DD}/2$ and C_L = 60 pF.

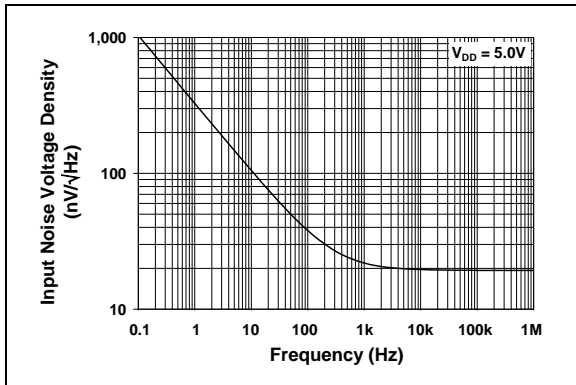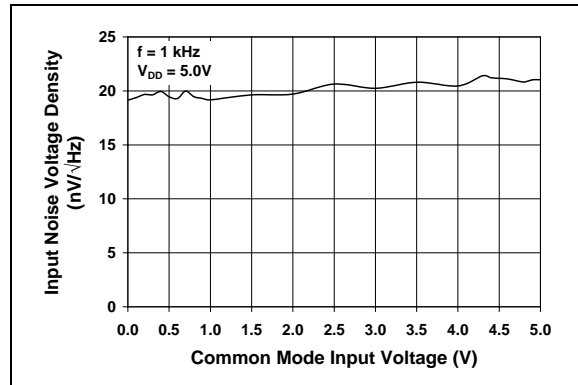**FIGURE 2-19:** *Input Noise Voltage Density vs. Frequency.*

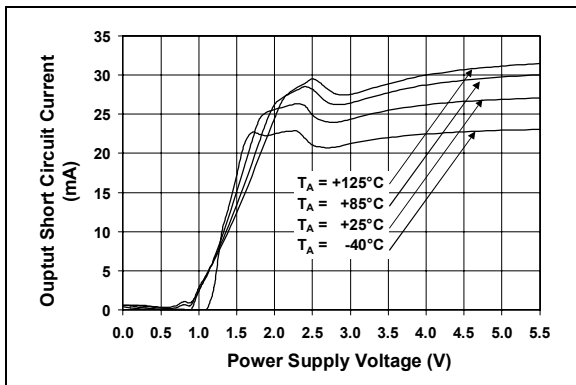**FIGURE 2-22:** *Input Noise Voltage Density vs. Common Mode Input Voltage at 1 kHz.*

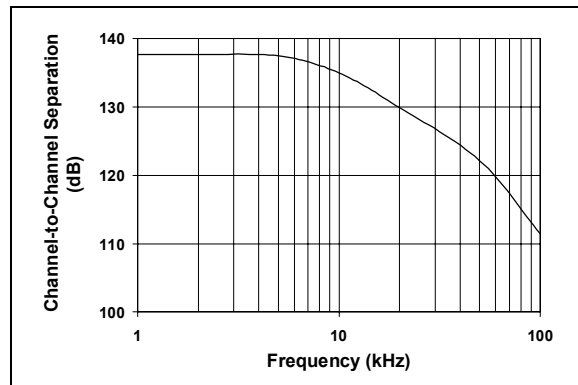**FIGURE 2-20:** *Output Short-Circuit Current vs. Power Supply Voltage.*

FIGURE 2-23: *Channel-to-Channel Separation vs. Frequency (MCP6272 and MCP6274).*
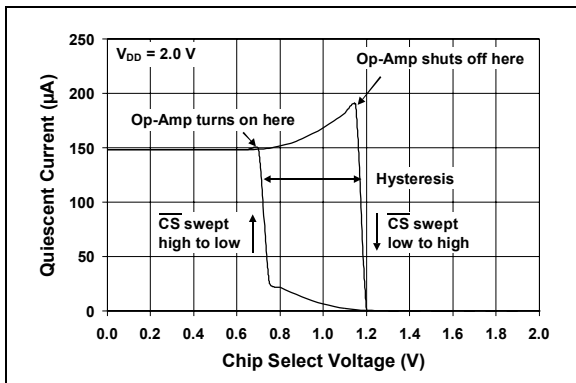

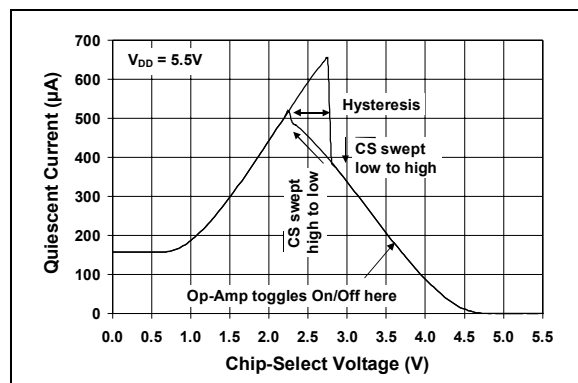**FIGURE 2-21:** *Quiescent Current vs. Chip Select ($\overline{CS}$) Voltage with V_{DD} = 2.0V (MCP6273 only).*

FIGURE 2-24: *Quiescent Current vs. Chip Select ($\overline{CS}$) Voltage with V_{DD} = 5.5V (MCP6273 only).*

Note: Unless otherwise indicated, T_A = +25°C, V_{DD} = +2.0V to +5.5V, V_{SS} = GND, V_{CM} = $V_{DD}/2$, $V_{OUT} \approx V_{DD}/2$, R_L = 10 kΩ to $V_{DD}/2$ and C_L = 60 pF.
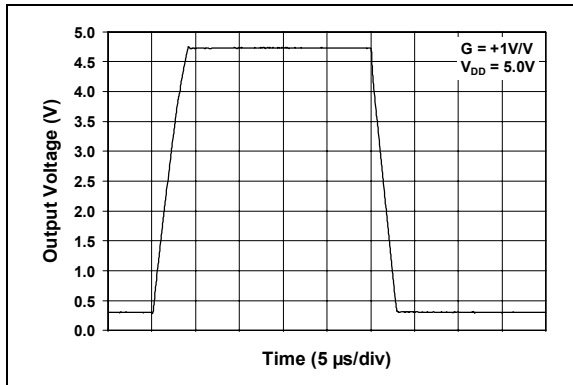
FIGURE 2-25: *Large Signal Non-inverting Pulse Response.*

FIGURE 2-28: *Large Signal Inverting Pulse Response.*
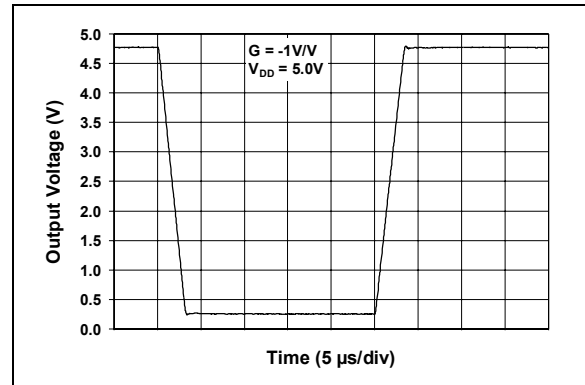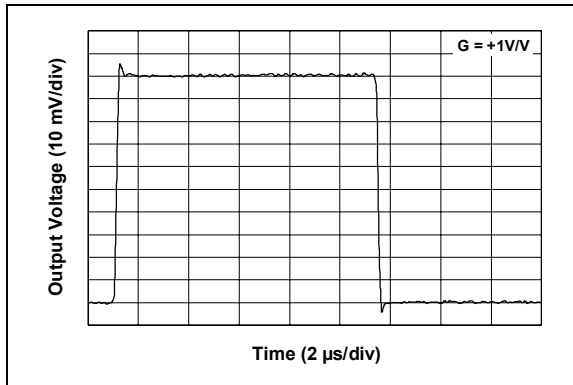

FIGURE 2-26: *Small Signal Non-inverting Pulse Response.*
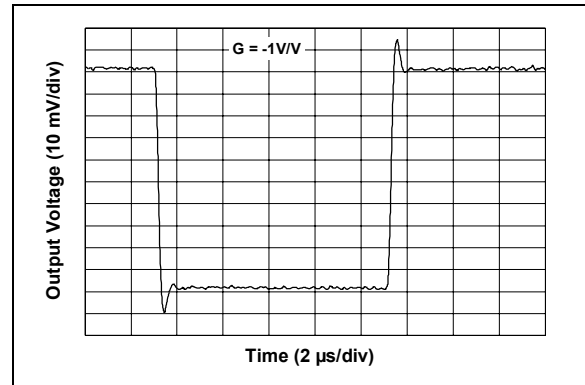

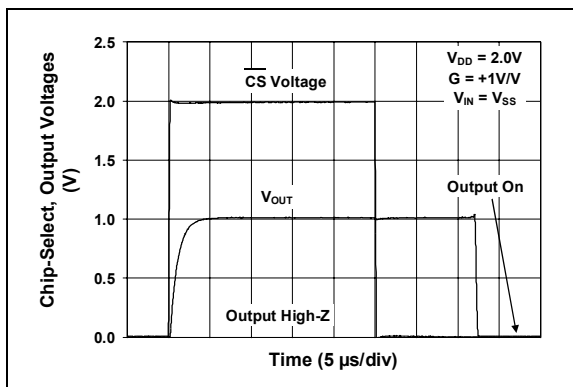**FIGURE 2-29:** *Small Signal Inverting Pulse Response.*

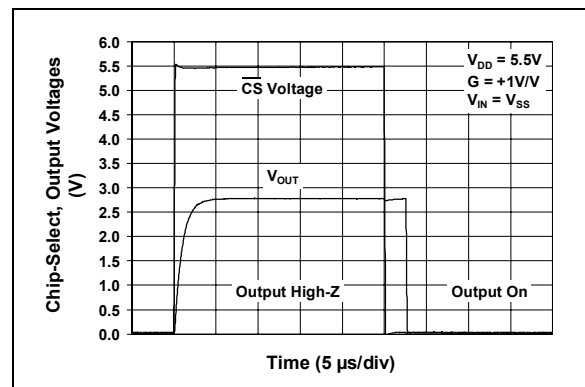**FIGURE 2-27:** *Chip Select ($\overline{CS}$) to Amplifier Output Response Time with V_{DD} = 2.0V (MCP6273 only).*

FIGURE 2-30: *Chip Select ($\overline{CS}$) to Amplifier Output Response Time with V_{DD} = 5.5V (MCP6273 only).*

3.0 APPLICATION INFORMATION

The MCP6271/2/3/4 family of op amps is manufactured using Microchip's state-of-the-art CMOS process, specifically designed for low cost, low power and general-purpose applications. The low supply voltage, low quiescent current and wide bandwidth makes the MCP6271/2/3/4 ideal for battery-powered applications.

3.1 Rail-to-Rail Input

The MCP6271/2/3/4 op amps are designed to prevent phase reversal when the input pins exceed the supply voltages. Figure 3-1 shows the input voltage exceeding the supply voltage without any phase reversal.
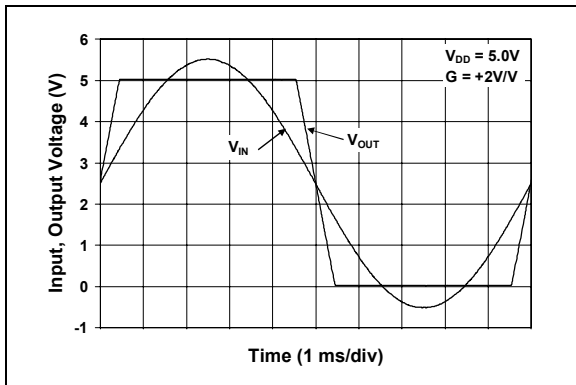

FIGURE 3-1: *The MCP6271/2/3/4 Show No Phase Reversal.*

The input stage of the MCP6271/2/3/4 op amp uses two differential input stages in parallel. One operates at low common mode input voltage (V_{CM}) and the other at high V_{CM}. With this topology, the device operates with V_{CM} up to 300 mV above V_{DD} and 300 mV below V_{SS}. The Input Offset Voltage is measured at $V_{CM} = V_{SS} - 300$ mV and $V_{DD} + 300$ mV to ensure proper operation.

Input voltages that exceed the input voltage range ($V_{SS} - 0.3V$ to $V_{DD} + 0.3V$ at 25°C) can cause excessive current to flow into or out of the input pins. Current beyond ±2 mA can cause reliability problems. Applications that exceed this rating must be externally limited with a resistor, as shown in Figure 3-2.

$$R_{IN} \geq \frac{(\text{Maximum expected } V_{IN}) - V_{DD}}{2 \; mA}$$

$$R_{IN} \geq \frac{V_{SS} - (\text{Minimum expected } V_{IN})}{2 \; mA}$$
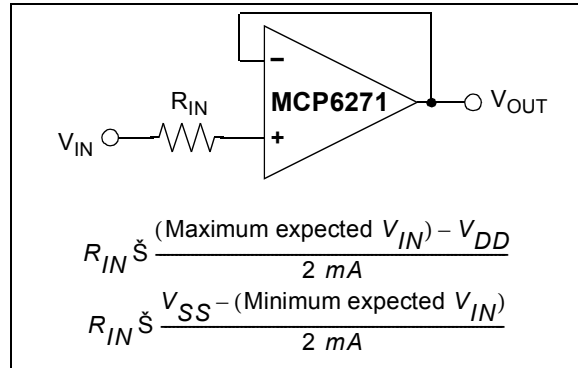
FIGURE 3-2: *Input Current Limiting Resistor (R_{IN}).*

3.2 Rail-to-Rail Output

The output voltage range of the MCP6271/2/3/4 op amp is $V_{DD} - 15$ mV (min.) and $V_{SS} + 15$ mV (max.) when $R_L = 10$ kΩ is connected to $V_{DD}/2$ and $V_{DD} = 5.5V$. Refer to Figure 2-16 for more information.

3.3 MCP6273 Chip Select ($\overline{CS}$)

The MCP6273 is a single amplifier with chip select ($\overline{CS}$). When $\overline{CS}$ is pulled high, the supply current drops to 0.7 µA (typ) and flows through the $\overline{CS}$ pin to V_{SS}. When this happens, the amplifier output is put into a high-impedance state. By pulling $\overline{CS}$ low, the amplifier is enabled. If the $\overline{CS}$ pin is left floating, the amplifier may not operate properly. Figure 3-3 shows the output voltage and supply current response to a $\overline{CS}$ pulse.

FIGURE 3-3: *Timing Diagram for the Chip Select ($\overline{CS}$) pin on the MCP6273.*

3.4 Capacitive Loads

Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot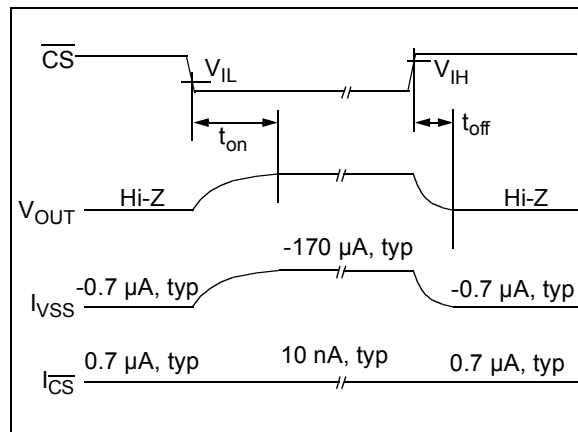 and ringing in the step response. A unity-gain buffer (G = +1) is the most sensitive to capacitive loads, though all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g., > 100 pF when G = +1), a small series resistor at the output (R_{ISO} in Figure 3-4) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. It does not, however, improve the bandwidth.
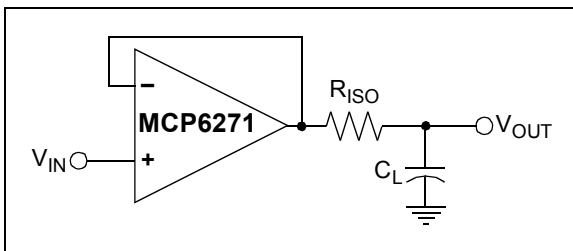

FIGURE 3-4: Output resistor, R_{ISO} stabilizes large capacitive loads.

To select R_{ISO}, check the frequency response peaking (or step response overshoot) on the bench (or with the MCP6271/2/3/4 SPICE Macro Model). If the response is reasonable, you do not need R_{ISO}. Otherwise, start R_{ISO} at 500Ω and modify its value until the response is reasonable.

3.5 Supply Bypass

With this family of operational amplifiers, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good, high-frequency performance. It also needs a bulk capacitor (i.e., 1 µF or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other parts.

3.6 PCB Surface Leakage

In applications where low input bias current is critical, PCB (printer circuit board) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA, if current-to-flow. This is greater than the MCP6271/2/3/4 family's bias current at 25°C (1 pA, typ.).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 3-5.
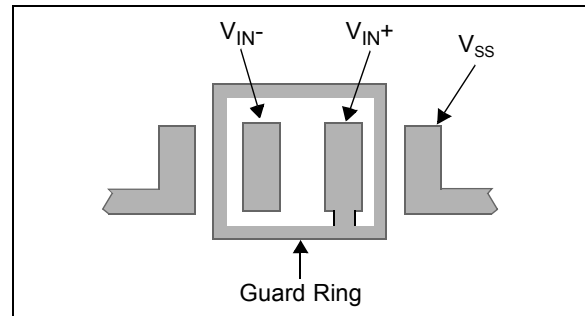
FIGURE 3-5: Example Guard Ring Layout for Inverting Gain.

1. For Inverting (Figure 3-5) and Transimpedance Amplifiers (convert current to voltage, such as photo detectors):
   a. Connect the guard ring to the non-inverting input pin ($V_{IN}+$). This biases the guard ring to the same reference voltage as the op amp (e.g., $V_{DD}/2$ or ground).
   b. Connect the inverting pin ($V_{IN}-$) to the input with a wire that does not touch the pcb surface.

2. Non-inverting Gain and Unity-Gain Buffer:
   a. Connect the non-inverting pin ($V_{IN}+$) to the input with a wire that does not touch the pcb surface.
   b. Connect the guard ring to the inverting input pin ($V_{IN}-$). This biases the guard ring to the common mode input voltage.

3.7 Application Circuits

3.7.1 ACTIVE FULL-WAVE RECTIFIER

The MCP6271/2/3/4 family of amplifiers can be used in applications such as an Active Full-Wave Rectifier or an Absolute Value circuit, as shown in Figure 3-6. The amplifier and the feedback loops in this active voltage rectifier circuit eliminate the diode drop problem that exists in a passive voltage rectifier. This circuit behaves as a follower (the output follows the input) as long as the input signal is more positive than the reference voltage. If the input signal is more negative than the reference voltage, however, the circuit behaves as an inverting amplifier. Therefore, the output voltage will always be above the reference voltage, regardless of the input signal.

$$R_1 = R_2 = R_3 = R_4$$

$$R_5 = \frac{R_1}{R_2}$$

FIGURE 3-6: Active Full-wave Rectifier.
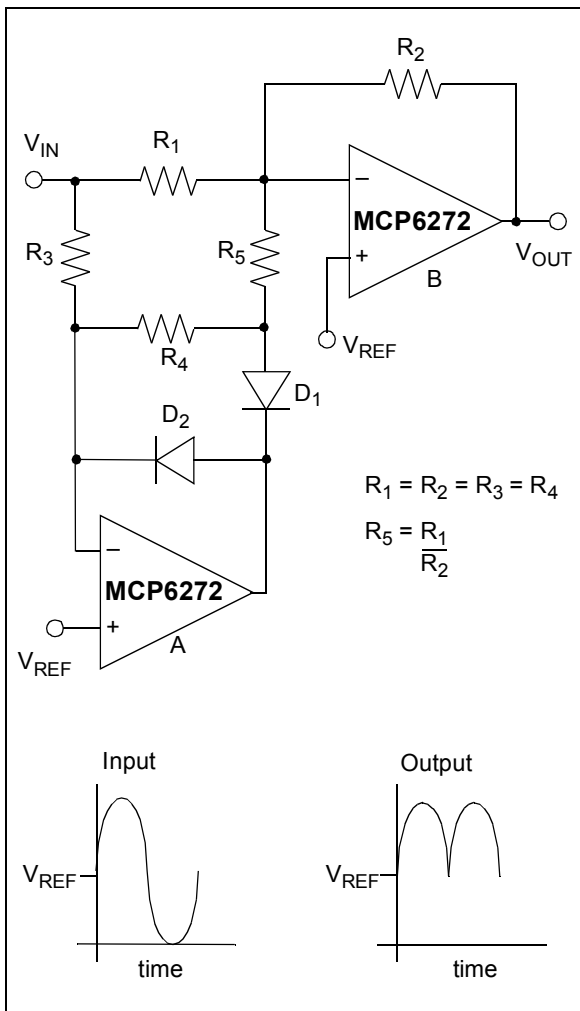
3.7.2 NON-INVERTING INTEGRATOR

The non-inverting integrator shown in Figure 3-7 is easy to build. It saves one op amp over the typical Miller Integrator plus inverting amplifier configuration. The phase accuracy of this integrator depends on the matching of the input and the feedback resistors and capacitors time constants.
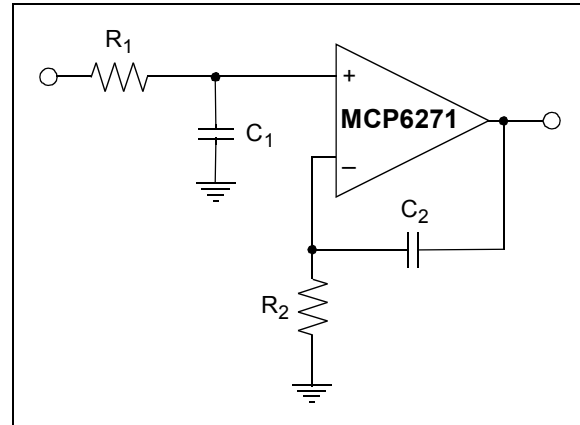

FIGURE 3-7: Non-Inverting Integrator.

4.0 DESIGN TOOLS

Microchip provides the basic design tools needed for the MCP6271/2/3/4 family of op amps.

4.1 SPICE Macro Model

The latest SPICE Macro Model for the MCP6271/2/3/4 op amp is available on our web site at www.microchip.com. This model is intended to be an initial design tool that works well in the op amp's linear region of operation at room temperature. See the model file for information on its capabilities.

Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

4.2 FilterLab® Software

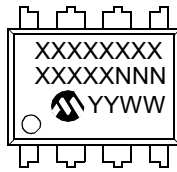The FilterLab software is an innovative tool that simplifies analog active-filter (using op amps) design. Available at no cost from our web site (www.microchip.com), the FilterLab active-filter software design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

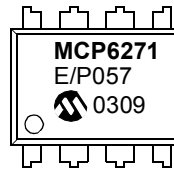## 5.0 PACKAGING INFORMATION

5.1 Package Marking Information

8-Lead PDIP (300 mil)

```
XXXXXXXX
XXXXXNNN
   Ⓜ YYWW
○
```

Example:

```
MCP6271
E/P057
   Ⓜ 0309
○
```

8-Lead SOIC (150 mil)

```
XXXXXXXX
XXXXYYWW
 ○  Ⓜ NNN
```

Example:

```
MCP6271
E/SN0309
 ○  Ⓜ 057
```

8-Lead MSOP

```
    XXXXXX
    YWWNNN
       Ⓜ    ⬡
```

Example:

```
     6271
    309057
       Ⓜ    ⬡
```
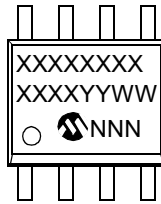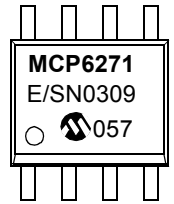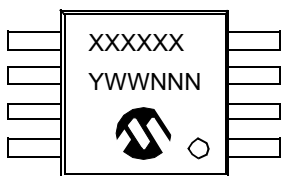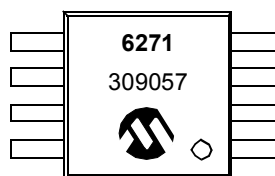
Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

Package Marking Information (Continued)

14-Lead PDIP (300 mil) **(MCP6274)**

```
┌─────────────────────────┐
│  XXXXXXXXXXXXX          │
│  XXXXXXXXXXXXX          │
│  ○   Ⓜ  YYWWNNN        │
└─────────────────────────┘
```

Example:

```
┌─────────────────────────┐
│  MCP6274-E/P           │
│      Ⓜ  0309057        │
│  ○                     │
└─────────────────────────┘
```
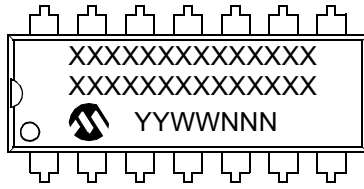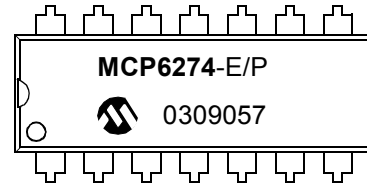
14-Lead SOIC (150 mil) **(MCP6274)**

```
┌─────────────────────────┐
│     XXXXXXXXX          │
│     XXXXXXXXX          │
│  ○  Ⓜ YYWWNNN          │
└─────────────────────────┘
```

Example:

```
┌─────────────────────────┐
│     MCP6274ESL         │
│  ○  Ⓜ  0309057         │
└─────────────────────────┘
```

14-Lead TSSOP **(MCP6274)**

```
┌─────────────────┐
│   XXXXXX        │
│   Ⓜ YYWW        │
│  ○   NNN        │
└─────────────────┘
```

Example:

```
┌─────────────────┐
│  6274ST         │
│   Ⓜ 0309        │
│  ○   057        │
└─────────────────┘
```
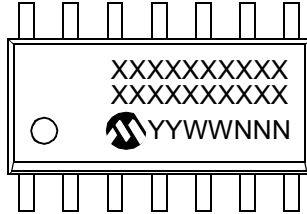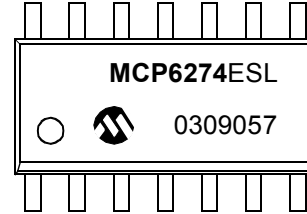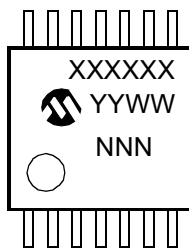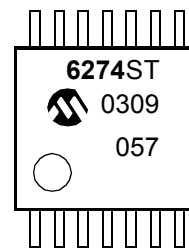
MCP6271/2/3/4

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)
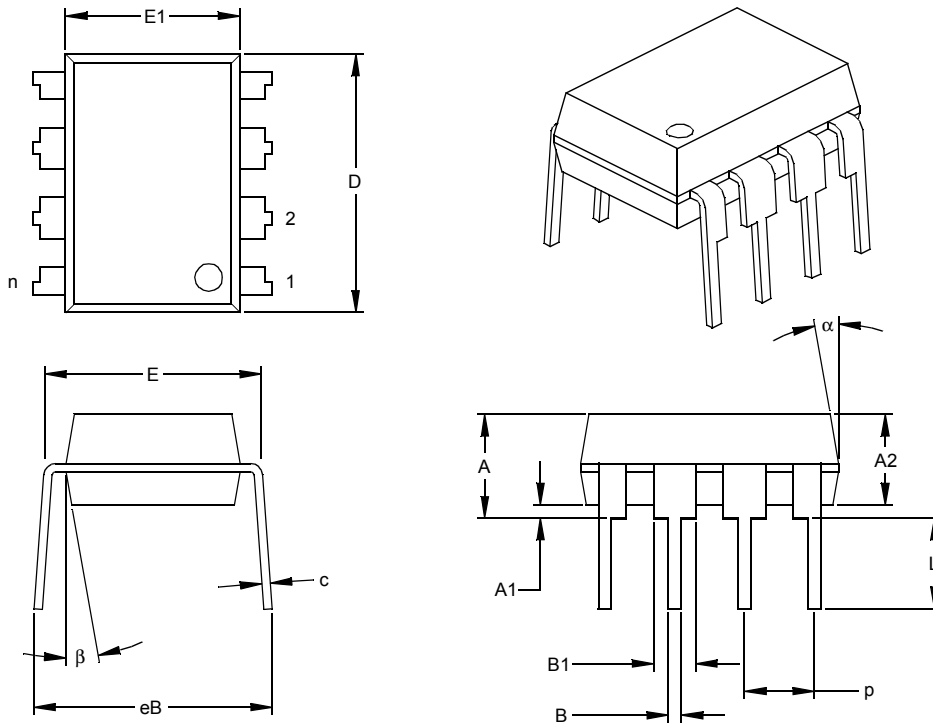
	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

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8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)
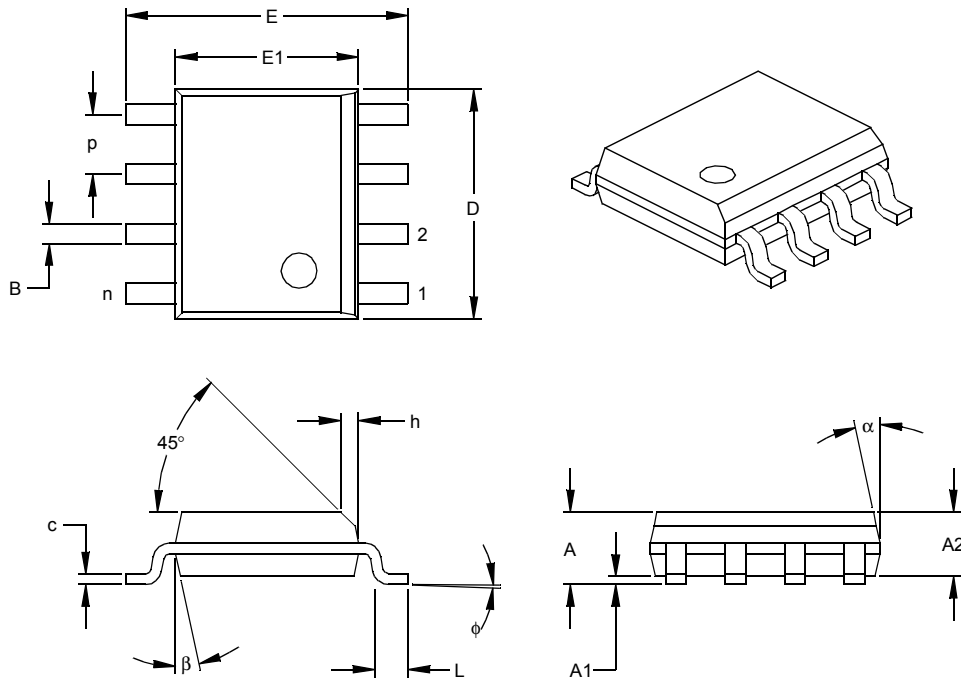
	Units	INCHES*			MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
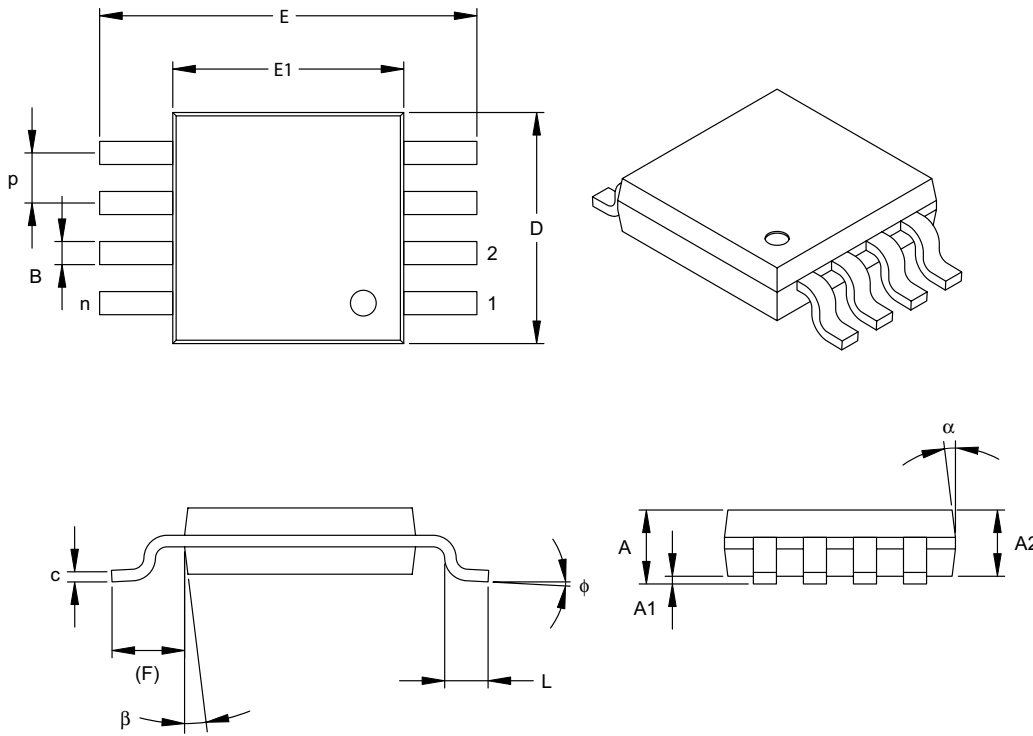Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)

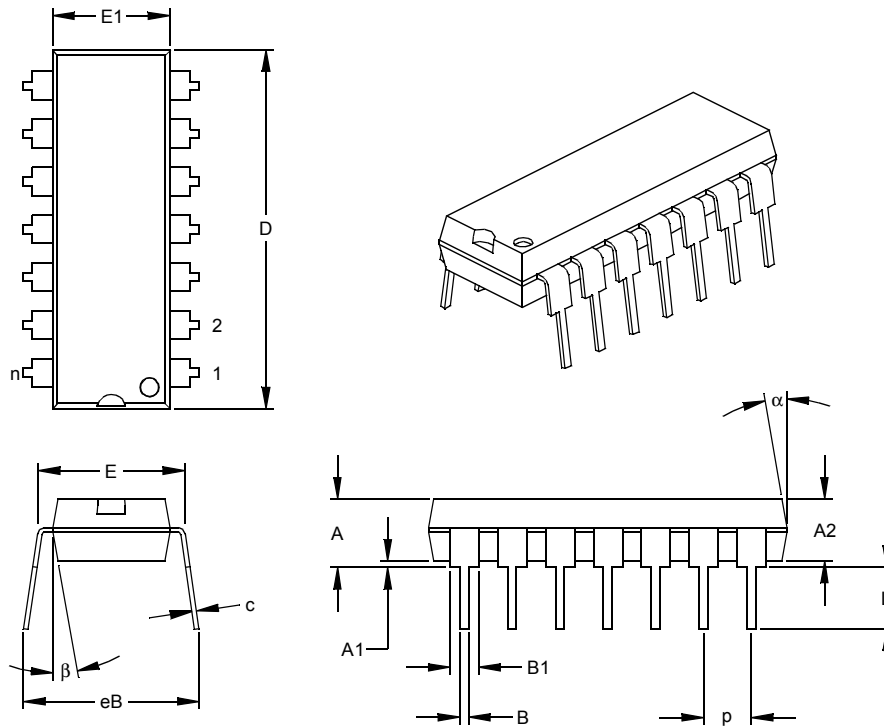|	Units	INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	φ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

	Units	INCHES*			MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.740	.750	.760	18.80	19.05	19.30
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
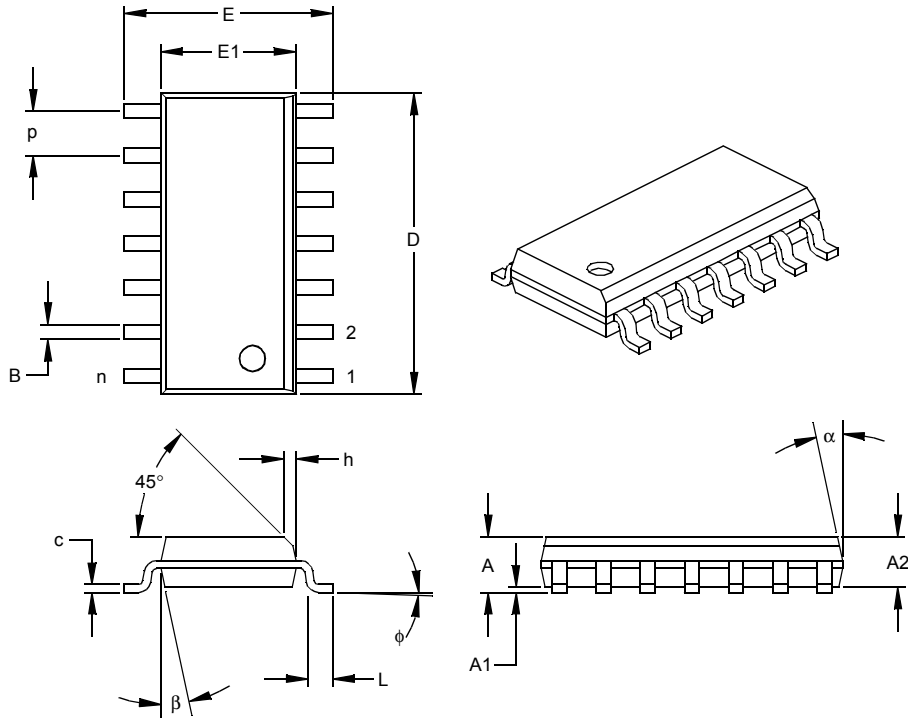§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed
.010" (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

MCP6271/2/3/4

14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)

	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.236	.244	5.79	5.99	6.20
Molded Package Width	E1	.150	.154	.157	3.81	3.90	3.99
Overall Length	D	.337	.342	.347	8.56	8.69	8.81
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
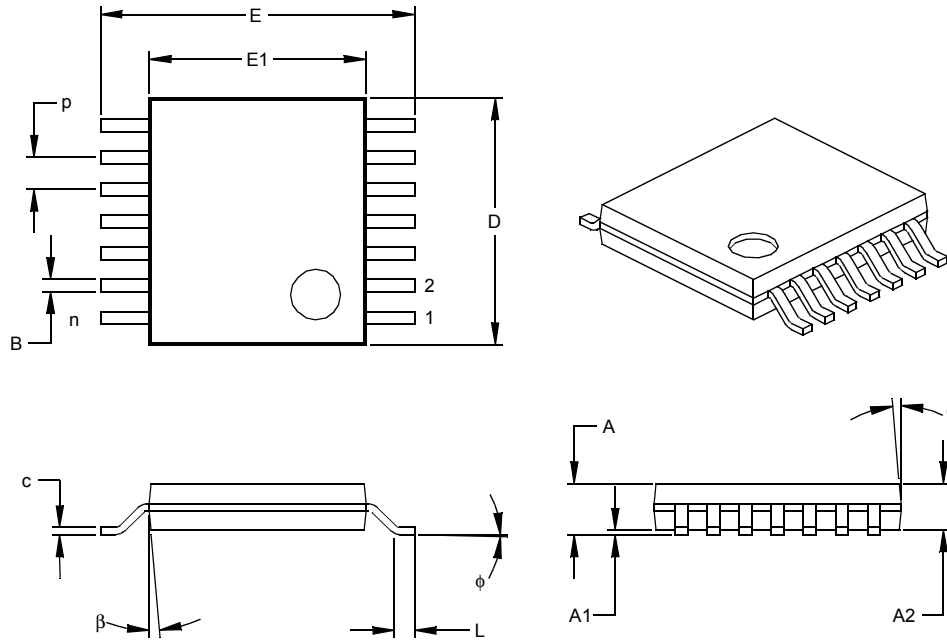§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed
.010" (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)

	Units		INCHES			MILLIMETERS*	
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		14			14	
Pitch	p		.026			0.65	
Overall Height	A			.043			1.10
Molded Package Thickness	A2	.033	.035	.037	0.85	0.90	0.95
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Overall Width	E	.246	.251	.256	6.25	6.38	6.50
Molded Package Width	E1	.169	.173	.177	4.30	4.40	4.50
Molded Package Length	D	.193	.197	.201	4.90	5.00	5.10
Foot Length	L	.020	.024	.028	0.50	0.60	0.70
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B1	.007	.010	.012	0.19	0.25	0.30
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed
.005" (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:
MCP6271: Single Operational Amplifier
MCP6271T: Single Operational Amplifier (Tape and Reel) (SOIC, MSOP)
MCP6272: Dual Operational Amplifiers
MCP6272T: Dual Operational Amplifiers (Tape and Reel) (SOIC, MSOP)
MCP6273: Single Operational Amplifier with Chip Select
MCP6273T: Single Operational Amplifier with Chip Select (Tape and Reel) (SOIC, MSOP)
MCP6274: Quad Operational Amplifiers
MCP6274T: Quad Operational Amplifiers (Tape and Reel) (SOIC, TSSOP)

Temperature Range: E = -40°C to +125°C

Package:
MS = Plastic MSOP, 8-lead
P = Plastic DIP (300 mil Body), 8-lead, 14-lead
SN = Plastic SOIC, (150 mil Body), 8-lead
SL = Plastic SOIC (150 mil Body), 14-lead
ST = Plastic TSSOP (4.4mm Body), 14-lead

Examples:

a) MCP6271-E/SN: Extended Temperature, 8LD SOIC package.
b) MCP6271-E/MS: Extended Temperature, 8LD MSOP package.
c) MCP6271-E/P: Extended Temperature, 8LD PDIP package.
d) MCP6271T-E/SN: Tape and Reel, Extended Temperature, 8LD SOIC package.
e) MCP6271T-E/MS: Tape and Reel, Extended Temperature, 8LD MSOP package.

a) MCP6272-E/SN: Extended Temperature, 8LD SOIC package.
b) MCP6272-E/MS: Extended Temperature, 8LD MSOP package.
c) MCP6272-E/P: Extended Temperature, 8LD PDIP package.
d) MCP6272T-E/SN: Tape and Reel, Extended Temperature, 8LD SOIC package.
e) MCP6272T-E/MS: Tape and Reel, Extended Temperature, 8LD MSOP package.

a) MCP6273-E/SN: Extended Temperature, 8LD SOIC package.
b) MCP6273-E/MS: Extended Temperature, 8LD MSOP package.
c) MCP6273-E/P: Extended Temperature, 8LD PDIP package.
d) MCP6273T-E/SN: Tape and Reel, Extended Temperature, 8LD SOIC package.
e) MCP6273T-E/MS: Tape and Reel, Extended Temperature, 8LD MSOP package.

a) MCP6274-E/P: Extended Temperature, 14LD PDIP package.
b) MCP6274T-E/SL: Tape and Reel, Extended Temperature, 14LD SOIC package.
c) MCP6274-E/SL: Extended Temperature, 14LD SOIC package.
d) MCP6274-E/ST: Extended Temperature, 14LD TSSOP package.
e) MCP6274T-E/ST: Tape and Reel, Extended Temperature, 14LD TSSOP package.

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

Customer Notification System
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NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.

- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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