DS05-20860-6E

FLASH MEMORY

CMOS

8M (1M × 8 / 512K × 16) BIT

MBM29DL800TA-70/90/MBM29DL800BA-70/90

■ FEATURES

- **Single 3.0 V read, program, and erase**
  Minimizes system level power requirements
- **Simultaneous operations**
  Read-while-Erase or Read-while-Program
- **Compatible with JEDEC-standard commands**
  Uses same software commands as E^2PROMs
- **Compatible with JEDEC-standard worldwide pinouts (Pin compatible with MBM29LV800TA/BA)**
  48-pin TSOP(1) (Package suffix: PFTN – Normal Bend Type, PFTR – Reversed Bend Type)
  48-ball FBGA (Package suffix: PBT)
- **Minimum 100,000 program/erase cycles**
- **High performance**
  70 ns maximum access time
- **Sector erase architecture**
  Two 16 K byte, four 8 K bytes, two 32 K byte, and fourteen 64 K bytes.
  Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Boot Code Sector Architecture**
  T = Top sector
  B = Bottom sector
- **Embedded Erase™ Algorithms**
  Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/Busy output (RY/$\overline{\text{BY}}$)**
  Hardware method for detection of program or erase cycle completion
- **Automatic sleep mode**
  When addresses remain stable, automatically switch themselves to low power mode.
- **Low V_{CC} write inhibit ≤ 2.5 V**
- **Erase Suspend/Resume**
  Suspends the erase operation to allow a read in another sector within the same device

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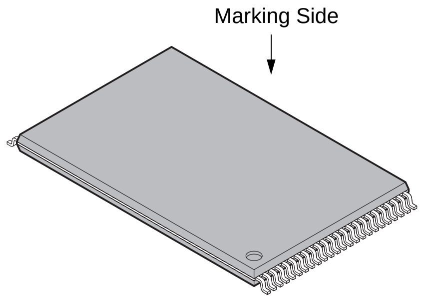
- **Sector protection**
  Hardware method disables any combination of sectors from program or erase operations
- **Sector Protection Set function by Extended sector protection command**
- **Fast Programming Function by Extended Command**
- **Temporary sector unprotection**
  Temporary sector unprotection via the $\overline{\text{RESET}}$ pin.

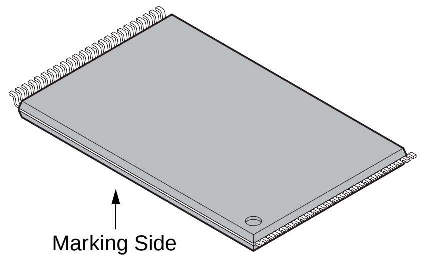
■ PACKAGES

48-pin plastic TSOP (I)



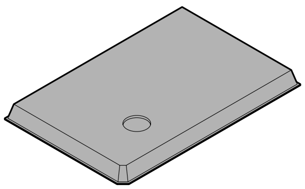
(FPT-48P-M19)

48-pin plastic TSOP (I)



(FPT-48P-M20)

48-pin plastic FBGA



(BGA-48P-M12)

■ GENERAL DESCRIPTION

The MBM29DL800TA/BA are a 8M-bit, 3.0 V-only Flash memory organized as 1 M bytes of 8 bits each or 512 K words of 16 bits each. The MBM29DL800TA/BA are offered in a 48-pin TSOP(1) and 48-ball FBGA packages. These devices are designed to be programmed in-system with the standard system 3.0 V V_{CC} supply. 12.0 V V_{PP} and 5.0 V V_{CC} are not required for write or erase operations. The devices can also be reprogrammed in standard EPROM programmers.

MBM29DL800TA/BA provide simultaneous operation which can read a data during program/erase. The simultaneous operation architecture provides simultaneous operation by dividing the memory space into two banks. The device can allow a host system to program or erase in one bank, then immediately and simultaneously read from the other bank.

The standard MBM29DL800TA/BA offer access times 70 ns and 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the devices have separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$), and output enable ($\overline{OE}$) controls.

The MBM29DL800TA/BA are pin and command set compatible with JEDEC standard E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the devices is similar to reading from 5.0 V and 12.0 V Flash or EPROM devices.

The MBM29DL800TA/BA are programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in about 0.5 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the devices automatically time the erase pulse widths and verify proper cell margin.

A sector is typically erased and verified in 1.0 second. (If already completely preprogrammed.)

The devices also feature a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors. The MBM29DL800TA/BA are erased when shipped from the factory.

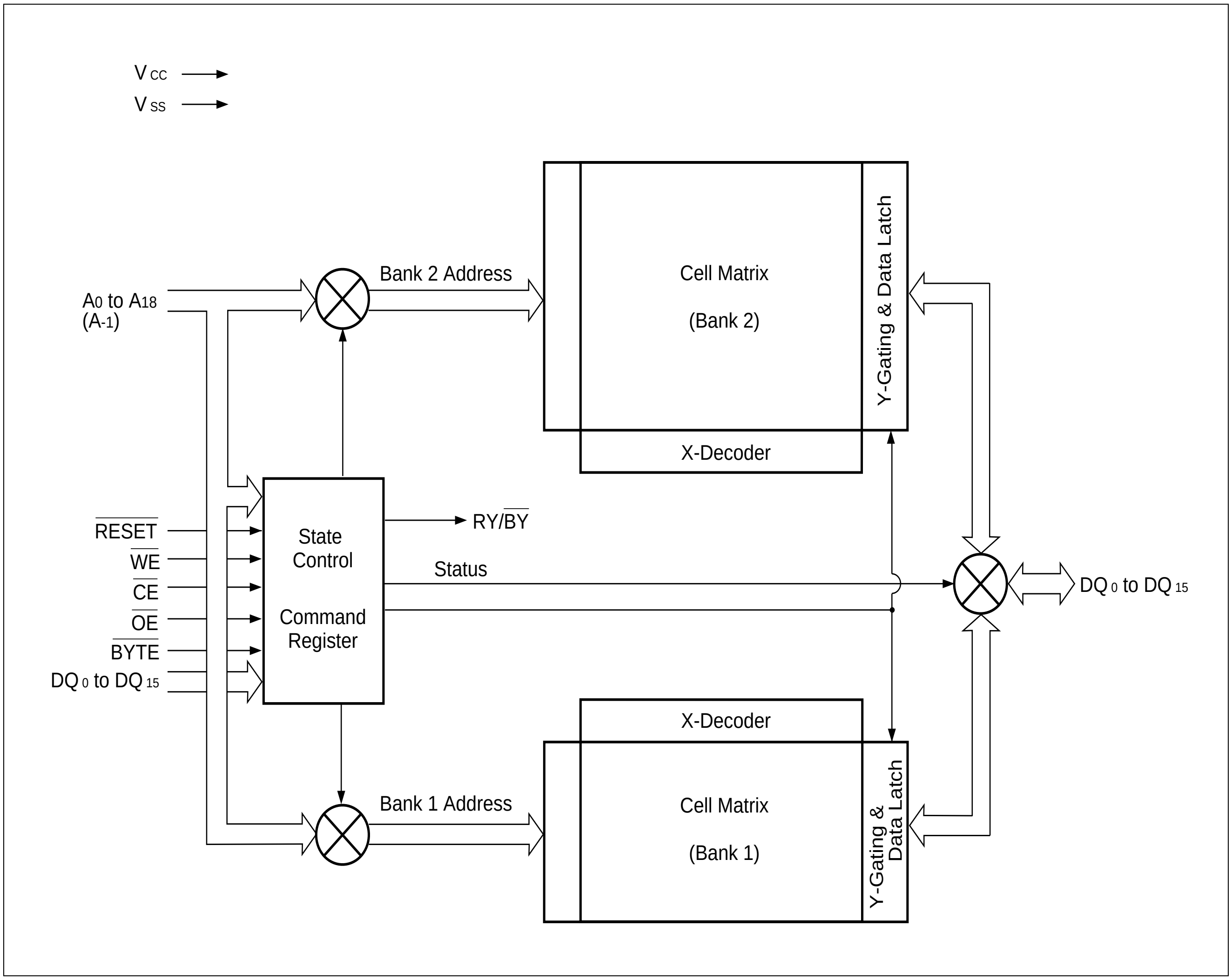
The devices feature single 3.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ_7, by the Toggle Bit feature on DQ_6, or the RY/$\overline{BY}$ output pin. Once the end of a program or erase cycle has been completed, the devices internally reset to the read mode.

Fujitsu's Flash technology combines years of EPROM and E2PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MBM29DL800TA/BA memories electrically erase the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

■ PRODUCT LINE UP

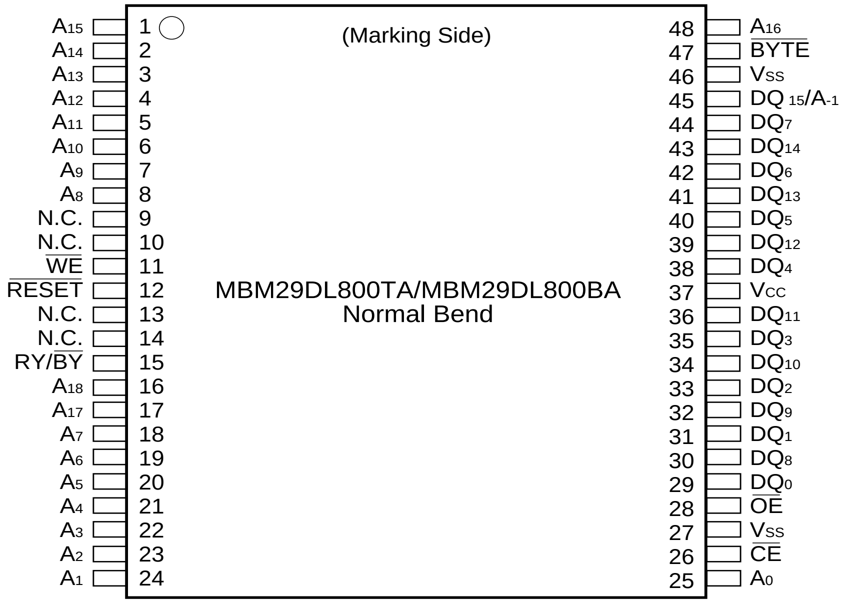
Part No.		MBM29DL800TA/MBM29DL800BA	
Ordering Part No.	$V_{CC} = 3.3\ V^{+0.3\ V}_{-0.3\ V}$	-70	—
	$V_{CC} = 3.0\ V^{+0.6\ V}_{-0.3\ V}$	—	-90
Max Address Access Time (ns)		70	90
Max $\overline{CE}$ Access Time (ns)		70	90
Max $\overline{OE}$ Access Time (ns)		30	35

■ BLOCK DIAGRAM

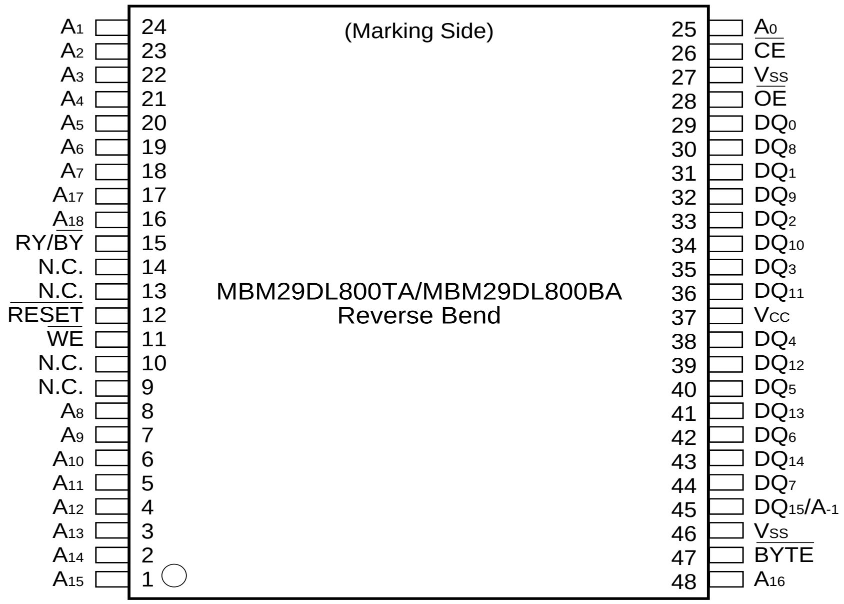


■ PIN ASSIGNMENTS

TSOP(1)



(FPT-48P-M19)



(FPT-48P-M20)

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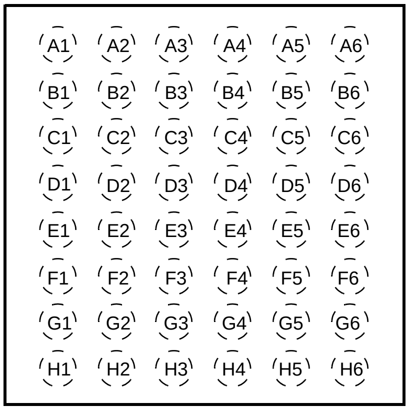
FBGA
(Top View)
Marking side



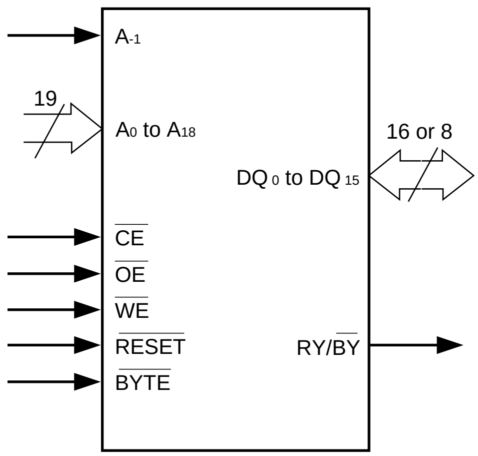
(BGA-48P-M12)

A1	A_3	A2	A_7	A3	RY/$\overline{BY}$	A4	$\overline{WE}$	A5	A_9	A6	A_{13}
B1	A_4	B2	A_{17}	B3	N.C.	B4	$\overline{RESET}$	B5	A_8	B6	A_{12}
C1	A_2	C2	A_6	C3	A_{18}	C4	N.C.	C5	A_{10}	C6	A_{14}
D1	A_1	D2	A_5	D3	N.C.	D4	N.C.	D5	A_{11}	D6	A_{15}
E1	A_0	E2	DQ_0	E3	DQ_2	E4	DQ_5	E5	DQ_7	E6	A_{16}
F1	$\overline{CE}$	F2	DQ_8	F3	DQ_{10}	F4	DQ_{12}	F5	DQ_{14}	F6	$\overline{BYTE}$
G1	$\overline{OE}$	G2	DQ_9	G3	DQ_{11}	G4	V_{CC}	G5	DQ_{13}	G6	DQ_{15}/A_{-1}
H1	V_{SS}	H2	DQ_1	H3	DQ_3	H4	DQ_4	H5	DQ_6	H6	V_{SS}

■ PIN DESCRIPTION

Pin Name	Function
A_{-1}, A_0 to A_{18}	Address Inputs
DQ_0 to DQ_{15}	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RY/$\overline{BY}$	Ready/Busy Output
$\overline{RESET}$	Hardware Reset Pin/Temporary Sector Unprotection
$\overline{BYTE}$	Selects 8-bit or 16-bit mode
N.C.	No Internal Connection
V_{SS}	Device Ground
V_{CC}	Device Power Supply

■ LOGIC SYMBOL



■ DEVICE BUS OPERATION

MBM29DL800TA/BA User Bus Operations Table ($\overline{BYTE}$ = V_{IH})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A_0	A_1	A_6	A_9	DQ_0 to DQ_{15}	$\overline{RESET}$
Auto-Select Manufacturer Code*1	L	L	H	L	L	L	V_{ID}	Code	H
Auto-Select Device Code*1	L	L	H	H	L	L	V_{ID}	Code	H
Read*3	L	L	H	A_0	A_1	A_6	A_9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	High-Z	H
Output Disable	L	H	H	X	X	X	X	High-Z	H
Write (Program/Erase)	L	H	L	A_0	A_1	A_6	A_9	D_{IN}	H
Enable Sector Protection*2, *4	L	V_{ID}	⊔	L	H	L	V_{ID}	X	H
Verify Sector Protection *2, *4	L	L	H	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotection*5	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware)/Standby	X	X	X	X	X	X	X	High-Z	L

MBM29DL800TA/BA User Bus Operations Table ($\overline{BYTE}$ = V_{IL})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ_{15}/A_{-1}	A_0	A_1	A_6	A_9	DQ_0 to DQ_7	$\overline{RESET}$
Auto-Select Manufacturer Code*1	L	L	H	L	L	L	L	V_{ID}	Code	H
Auto-Select Device Code*1	L	L	H	L	H	L	L	V_{ID}	Code	H
Read*3	L	L	H	A_{-1}	A_0	A_1	A_6	A_9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	X	High-Z	H
Output Disable	L	H	H	X	X	X	X	X	High-Z	H
Write (Program/Erase)	L	H	L	A_{-1}	A_0	A_1	A_6	A_9	D_{IN}	H
Enable Sector Protection*2, *4	L	V_{ID}	⊔	L	L	H	L	V_{ID}	X	H
Verify Sector Protection *2, *4	L	L	H	L	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotection *5	X	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware)/Standby	X	X	X	X	X	X	X	X	High-Z	L

Legend: L = V_{IL}, H = V_{IH}, X = V_{IL} or V_{IH}, ⊔ = Pulse input. See "■ DC CHARACTERISTICS" for voltage levels.

*1 : Manufacturer and device codes may also be accessed via a command register write sequence. See "MBM29DL800TA/BA Command Definitions Table".

*2 : Refer to the section on Sector Protection.

*3 : $\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.

*4 : V_{CC} = 3.0 V ± 10%

*5 : It is also used for the extended sector protection.

MBM29DL800TA/BA Command Definitions Table

Command Sequence		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	Word	1	XXXh	F0h	—	—	—	—	—	—	—	—	—	—
	Byte													
Read/Reset	Word	3	555h	AAh	2AAh	55h	555h	F0h	RA	RD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Autoselect	Word	3	555h	AAh	2AAh	55h	(BA) 555h	90h	—	—	—	—	—	—
	Byte		AAAh		555h		(BA) AAAh							
Program	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	—	—	—	—
	Byte		AAAh		555h		AAAh							
Chip Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
	Byte		AAAh		555h		AAAh		AAAh		555h		AAAh	
Sector Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	SA	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
Erase Suspend		1	BA	B0h	—	—	—	—	—	—	—	—	—	—
Erase Resume		1	BA	30h	—	—	—	—	—	—	—	—	—	—
Set to Fast Mode	Word	3	555h	AAh	2AAh	55h	555h	20h	—	—	—	—	—	—
	Byte		AAAh		555h		AAAh							
Fast Program *1	Word	2	XXXh	A0h	PA	PD	—	—	—	—	—	—	—	—
	Byte		XXXh											
Reset from Fast Mode *1	Word	2	BA	90h	XXXh	F0h *3	—	—	—	—	—	—	—	—
	Byte		BA		XXXh									
Extended Sector Protect*2	Word	4	XXXh	60h	SPA	60h	SPA	40h	SPA	SD	—	—	—	—
	Byte													

*1 : This command is valid during Fast Mode.

*2 : This command is valid while $\overline{RESET}=V_{ID}$.

*3 : This data "00h" is also acceptable.

Notes : • Address bits A_{12} to A_{18} = X = "H" or "L" for all address commands except or Program Address (PA), Sector Address (SA), and Bank Address (BA).

- Bus operations are defined in "MBM29DL800TA/BA User Bus Operations Tables ($\overline{BYTE}$ = V_{IH} and $\overline{BYTE}$ = V_{IL})".
- RA =Address of the memory location to be read
  PA =Address of the memory location to be programmed
  Addresses are latched on the falling edge of the write pulse.
  SA =Address of the sector to be erased. The combination of A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12} will uniquely select any sector.
  BA =Bank Address (A_{16} to A_{18})
- RD =Data read from location RA during read operation.
  PD =Data to be programmed at location PA. Data is latched on the rising edge of write pulse.
- SPA =Sector address to be protected. Set sector address (SA) and (A_6, A_1, A_0) = (0, 1, 0).
  SD =Sector protection verify data. Output 01h at protected sector addresses and output 00h at unprotected sector addresses.
- The system should generate the following address patterns:
  Word Mode: 555h or 2AAh to addresses A_0 to A_{11}
  Byte Mode: AAAh or 555h to addresses A_{-1} and A_0 to A_{11}
- Both Read/Reset commands are functionally equivalent, resetting the device to the read mode.
- The command combinations not described in "MBM29DL800TA/BA Command Definitions Table" are illegal.

MBM29DL800TA/BA Sector Protection Verify Autoselect Codes Table

Type			A_{12} to A_{18}	A_6	A_1	A_0	A_{-1}*1	Code (HEX)
Manufacture's Code			X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	04h
Device Code	MBM29DL800TA	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	4Ah
		Word					X	224Ah
	MBM29DL800BA	Byte	X	V_{IL}	V_{IL}	V_{IH}	V_{IL}	CBh
		Word					X	22CBh
Sector Protection			Sector Addresses	V_{IL}	V_{IH}	V_{IL}	V_{IL}	01h*2

*1 : A_{-1} is for Byte mode. At Byte mode, DQ_8 to DQ_{14} are High-Z and DQ_{15} is A_{-1}, the lowest address.

*2 : Outputs 01h at protected sector addresses and outputs 00h at unprotected sector addresses.

Extended Autoselect Code Table

Type			Code	DQ_{15}	DQ_{14}	DQ_{13}	DQ_{12}	DQ_{11}	DQ_{10}	DQ_9	DQ_8	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer's Code			04h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Device Code	MBM29DL800TA	(B)*	4Ah	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	0	1	0	0	1	0	1	0
		(W)	224Ah	0	0	1	0	0	0	1	0	0	1	0	0	1	0	1	0
	MBM29DL800BA	(B)*	CBh	A_{-1}	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	1	1	0	0	1	0	1	1
		(W)	22CBh	0	0	1	0	0	0	1	0	1	1	0	0	1	0	1	1
Sector Protection			01h	A_{-1}/0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(B): Byte mode
(W): Word mode

HI-Z: High-Z

* : At Byte mode, DQ_8 to DQ_{14} are High-Z and DQ_{15} is A_{-1}, the lowest address.

■ FLEXIBLE SECTOR-ERASE ARCHITECTURE

- Two 16 K bytes, four 8 K bytes, two 32 K bytes, and fourteen 64 K bytes
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable.

Bank	Sector	(×8)	(×16)
Bank 1	16 K byte	FFFFFh	7FFFFh
Bank 1	32 K byte	FBFFFh	7DFFFh
Bank 1	8 K byte	F3FFFh	79FFFh
Bank 1	8 K byte	F1FFFh	78FFFh
Bank 1	8 K byte	EFFFFh	77FFFh
Bank 1	8 K byte	EDFFFh	76FFFh
Bank 1	32 K byte	EBFFFh	75FFFh
Bank 1	16 K byte	E3FFFh	71FFFh
Bank 2	64 K byte	DFFFFh	6FFFFh
Bank 2	64 K byte	CFFFFh	67FFFh
Bank 2	64 K byte	BFFFFh	5FFFFh
Bank 2	64 K byte	AFFFFh	57FFFh
Bank 2	64 K byte	9FFFFh	4FFFFh
Bank 2	64 K byte	8FFFFh	47FFFh
Bank 2	64 K byte	7FFFFh	3FFFFh
Bank 2	64 K byte	6FFFFh	37FFFh
Bank 2	64 K byte	5FFFFh	2FFFFh
Bank 2	64 K byte	4FFFFh	27FFFh
Bank 2	64 K byte	3FFFFh	1FFFFh
Bank 2	64 K byte	2FFFFh	17FFFh
Bank 2	64 K byte	1FFFFh	0FFFFh
Bank 2	64 K byte	0FFFFh	07FFFh
		00000h	00000h

MBM29DL800TA Sector Architecture

Bank	Sector	(×8)	(×16)
Bank 2	64 K byte	FFFFFh	7FFFFh
Bank 2	64 K byte	EFFFFh	77FFFh
Bank 2	64 K byte	DFFFFh	6FFFFh
Bank 2	64 K byte	CFFFFh	67FFFh
Bank 2	64 K byte	BFFFFh	5FFFFh
Bank 2	64 K byte	AFFFFh	57FFFh
Bank 2	64 K byte	9FFFFh	4FFFFh
Bank 2	64 K byte	8FFFFh	47FFFh
Bank 2	64 K byte	7FFFFh	3FFFFh
Bank 2	64 K byte	6FFFFh	37FFFh
Bank 2	64 K byte	5FFFFh	2FFFFh
Bank 2	64 K byte	4FFFFh	27FFFh
Bank 2	64 K byte	3FFFFh	1FFFFh
Bank 2	64 K byte	2FFFFh	17FFFh
Bank 1	16 K byte	1FFFFh	0FFFFh
Bank 1	32 K byte	1BFFFh	0DFFFh
Bank 1	8 K byte	13FFFh	09FFFh
Bank 1	8 K byte	11FFFh	08FFFh
Bank 1	8 K byte	0FFFFh	07FFFh
Bank 1	8 K byte	0DFFFh	06FFFh
Bank 1	32 K byte	0BFFFh	05FFFh
Bank 1	16 K byte	03FFFh	01FFFh
		00000h	00000h

MBM29DL800BA Sector Architecture

Sector Address Table (MBM29DL800BA)

Bank	Sector	Sector Address: Bank Address							Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
		A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}			
Bank 2	SA21	1	1	1	1	X	X	X	64/32	F0000h to FFFFFh	78000h to 7FFFFh
	SA20	1	1	1	0	X	X	X	64/32	E0000h to EFFFFh	70000h to 77FFFh
	SA19	1	1	0	1	X	X	X	64/32	D0000h to DFFFFh	68000h to 6FFFFh
	SA18	1	1	0	0	X	X	X	64/32	C0000h to CFFFFh	60000h to 67FFFh
	SA17	1	0	1	1	X	X	X	64/32	B0000h to BFFFFh	58000h to 5FFFFh
	SA16	1	0	1	0	X	X	X	64/32	A0000h to AFFFFh	50000h to 57FFFh
	SA15	1	0	0	1	X	X	X	64/32	90000h to 9FFFFh	48000h to 4FFFFh
	SA14	1	0	0	0	X	X	X	64/32	80000h to 8FFFFh	40000h to 47FFFh
	SA13	0	1	1	1	X	X	X	64/32	70000h to 7FFFFh	38000h to 3FFFFh
	SA12	0	1	1	0	X	X	X	64/32	60000h to 6FFFFh	30000h to 37FFFh
	SA11	0	1	0	1	X	X	X	64/32	50000h to 5FFFFh	28000h to 2FFFFh
	SA10	0	1	0	0	X	X	X	64/32	40000h to 4FFFFh	20000h to 27FFFh
	SA9	0	0	1	1	X	X	X	64/32	30000h to 3FFFFh	18000h to 1FFFFh
	SA8	0	0	1	0	X	X	X	64/32	20000h to 2FFFFh	10000h to 17FFFh
Bank 1	SA7	0	0	0	1	1	1	X	16/8	1C000h to 1FFFFh	0E000h to 0FFFFh
	SA6	0	0	0	1	1	0	X	32/16	18000h to 1BFFFh, 14000h to 17FFFh	0C000h to 0DFFFh, 0A000h to 0BFFFh
						0	1	X			
	SA5	0	0	0	1	0	0	1	8/4	12000h to 13FFFh	09000h to 09FFFh
	SA4	0	0	0	1	0	0	0	8/4	10000h to 11FFFh	08000h to 08FFFh
	SA3	0	0	0	0	1	1	1	8/4	0E000h to 0FFFFh	07000h to 07FFFh
	SA2	0	0	0	0	1	1	0	8/4	0C000h to 0DFFFh	06000h to 06FFFh
	SA1	0	0	0	0	1	0	X	32/16	08000h to 0BFFFh, 04000h to 07FFFh	04000h to 05FFFh, 02000h to 03FFFh
						0	1	X			
	SA0	0	0	0	0	0	0	X	16/8	00000h to 03FFFh	00000h to 01FFFh

Note : The address range is A_{18}: A_{-1} if in byte mode ($\overline{BYTE}$ = V_{IL}).
The address range is A_{18}: A_0 if in word mode ($\overline{BYTE}$ = V_{IH}).

Sector Address Table (MBM29DL800TA)

Bank	Sector	Sector Address: Bank Address A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	Sector Size (Kbytes/ Kwords)	(×8) Address Range	(×16) Address Range
Bank 2	SA0	0	0	0	0	X	X	X	64/32	00000h to 0FFFFh	00000h to 07FFFh
	SA1	0	0	0	1	X	X	X	64/32	10000h to 1FFFFh	08000h to 0FFFFh
	SA2	0	0	1	0	X	X	X	64/32	20000h to 2FFFFh	10000h to 17FFFh
	SA3	0	0	1	1	X	X	X	64/32	30000h to 3FFFFh	18000h to 1FFFFh
	SA4	0	1	0	0	X	X	X	64/32	40000h to 4FFFFh	20000h to 27FFFh
	SA5	0	1	0	1	X	X	X	64/32	50000h to 5FFFFh	28000h to 2FFFFh
	SA6	0	1	1	0	X	X	X	64/32	60000h to 6FFFFh	30000h to 37FFFh
	SA7	0	1	1	1	X	X	X	64/32	70000h to 7FFFFh	38000h to 3FFFFh
	SA8	1	0	0	0	X	X	X	64/32	80000h to 8FFFFh	40000h to 47FFFh
	SA9	1	0	0	1	X	X	X	64/32	90000h to 9FFFFh	48000h to 4FFFFh
	SA10	1	0	1	0	X	X	X	64/32	A0000h to AFFFFh	50000h to 57FFFh
	SA11	1	0	1	1	X	X	X	64/32	B0000h to BFFFFh	58000h to 5FFFFh
	SA12	1	1	0	0	X	X	X	64/32	C0000h to CFFFFh	60000h to 67FFFh
	SA13	1	1	0	1	X	X	X	64/32	D0000h to DFFFFh	68000h to 6FFFFh
Bank 1	SA14	1	1	1	0	0	0	X	16/8	E0000h to E3FFFh	70000h to 71FFFh
	SA15	1	1	1	0	0 1	1 0	X X	32/16	E4000h to E7FFFh, E8000h to EBFFFh	72000h to 73FFFh, 74000h to 75FFFh
	SA16	1	1	1	0	1	1	0	8/4	EC000h to EDFFFh	76000h to 76FFFh
	SA17	1	1	1	0	1	1	1	8/4	EE000h to EFFFFh	77000h to 77FFFh
	SA18	1	1	1	1	0	0	0	8/4	F0000h to F1FFFh	78000h to 78FFFh
	SA19	1	1	1	1	0	0	1	8/4	F2000h to F3FFFh	79000h to 79FFFh
	SA20	1	1	1	1	0 1	1 0	X X	32/16	F4000h to F7FFFh, F8000h to FBFFFh	7A000h to 7BFFFh, 7C000h to 7DFFFh
	SA21	1	1	1	1	1	1	X	16/8	FC000h to FFFFFh	7E000h to 7FFFFh

Note : The address range is A_{18}: A_{-1} if in byte mode ($\overline{BYTE}$ = V_{IL}).
The address range is A_{18}: A_0 if in word mode ($\overline{BYTE}$ = V_{IH}).

■ FUNCTIONAL DESCRIPTION

Simultaneous Operation

MBM29DL800TA/BA have feature, which is capability of reading data from one bank of memory while a program or erase operation is in progress in the other bank of memory (simultaneous operation), in addition to the conventional features (read, program, erase, erase-suspend read, and erase-suspend program). The bank selection can be selected by bank address (A_{16} to A_{18}) with zero latency.

The MBM29DL800TA/BA have two banks which contain Bank 1 (16 KB, 32 KB, 8 KB, 8 KB, 8 KB, 8 KB, 32 KB, and 16 KB) and Bank 2 (64 KB × fourteen sectors).

The simultaneous operation can not execute multi-function mode in the same bank. “Simultaneous Operation Table” shows combination to be possible for simultaneous operation.

Simultaneous Operation Table

Case	Bank 1 Status	Bank 2 Status
1	Read mode	Read mode
2	Read mode	Autoselect mode
3	Read mode	Program mode
4	Read mode	Erase mode *
5	Autoselect mode	Read mode
6	Program mode	Read mode
7	Erase mode *	Read mode

*: An erase operation may also be supended to read from or program to a sector not being erased.

Read Mode

The MBM29DL800TA/BA have two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for a device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins. (Assuming the addresses have been stable for at least t_{ACC}-t_{OE} time.) When reading out a data without changing addresses after power-up, it is necessary to input hardware reset or to change $\overline{CE}$ pin from “H” or “L”

Standby Mode

There are two ways to implement the standby mode on the MBM29DL800TA/BA devices, one using both the $\overline{CE}$ and $\overline{RESET}$ pins; the other via the $\overline{RESET}$ pin only.

When using both pins, a CMOS standby mode is achieved with $\overline{CE}$ and $\overline{RESET}$ inputs both held at V_{CC} ± 0.3 V. Under this condition the current consumed is less than 5 µA Max During Embedded Algorithm operation, V_{CC} active current (I_{CC2}) is required even $\overline{CE}$ = “H”. The device can be read with standard access time (t_{CE}) from either of these standby modes.

When using the $\overline{RESET}$ pin only, a CMOS standby mode is achieved with $\overline{RESET}$ input held at V_{SS} ± 0.3 V ($\overline{CE}$ = “H” or “L”). Under this condition the current is consumed is less than 5 µA Max Once the $\overline{RESET}$ pin is taken high, the device requires t_{RH} of wake up time before outputs are valid for read access.

In the standby mode the outputs are in the high impedance state, independent of the $\overline{OE}$ input.

Automatic Sleep Mode

There is a function called automatic sleep mode to restrain power consumption during read-out of MBM29DL800TA/BA data. This mode can be used effectively with an application requested low power consumption such as handy terminals.

To activate this mode, MBM29DL800TA/BA automatically switch themselves to low power mode when MBM29DL800TA/BA addresses remain stably during access fine of 150 ns. It is not necessary to control $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ on the mode. Under the mode, the current consumed is typically 1 µA (CMOS Level).

During simultaneous operation, V_{CC} active current (I_{CC2}) is required.

Since the data are latched during this mode, the data are read-out continuously. If the addresses are changed, the mode is canceled automatically and MBM29DL800TA/BA read-out the data for changed addresses.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the devices are disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the devices and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the devices to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the devices.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A_9. Two identifier bytes may then be sequenced from the devices outputs by toggling address A_0 from V_{IL} to V_{IH}. All addresses are DON'T CARES except A_0, A_1, and A_6 (A_{-1}). (See "MBM29DL800TA/BA User Bus Operations Tables ($\overline{BYTE}$ = V_{IH} and $\overline{BYTE}$ = V_{IL})" in ■DEVICE BUS OPERATION.)

The manufacturer and device codes may also be read via the command register, for instances when the MBM29DL800TA/BA are erased or programmed in a system without access to high voltage on the A_9 pin. The command sequence is illustrated in "MBM29DL800TA/BA Command Definitions Table" (in ■DEVICE BUS OPERATION). (Refer to Autoselect Command section.)

Word 0 (A_0 = V_{IL}) represents the manufacturer's code (Fujitsu = 04h) and word 1 (A_0 = V_{IH}) represents the device identifier code (MBM29DL800TA = 4Ah and MBM29DL800BA = CBh for ×8 mode; MBM29DL800TA = 224Ah and MBM29DL800BA = 22CBh for ×16 mode). These two bytes/words are given in "MBM29DL800TA/BA Sector Protection Verify Autoselect Codes Table" and "Extended Autoselect Code Table" (in ■DEVICE BUS OPERATION). All identifiers for manufactures and device will exhibit odd parity with DQ_7 defined as the parity bit. In order to read the proper device codes when executing the autoselect, A_1 must be V_{IL}. (See "MBM29DL800TA/BA Sector Protection Verify Autoselect Codes Table" and "Extended Autoselect Code Table" in ■DEVICE BUS OPERATION.)

In case of applying V_{ID} on A_9, since both Bank 1 and Bank 2 enters Autoselect mode, the simultenous operation can not be executed.

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Protection

The MBM29DL800TA/BA feature hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 21). The sector protection feature is enabled using programming equipment at the user's site. The devices are shipped with all sectors unprotected. Alternatively, Fujitsu may program and protect sectors in the factory prior to shiping the device.

To activate this mode, the programming equipment must force V_{ID} on address pin A_9 and control pin $\overline{OE}$, (suggest V_{ID} = 11.5 V), $\overline{CE}$ = V_{IL}, and A_0 = A_6 = V_{IL}, A_1 = V_{IH}. The sector addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) should be set to the sector to be protected. "Sector Address Tables (MBM29DL800TA/BA)" in ■FLEXIBLE SECTOR-ERASE ARCHITECTURE define the sector address for each of the twenty two (22) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. See "(13) AC Waveforms for Sector Protection" in ■TIMING DIAGRAM and "(5) Sector Protection Algorithm" in ■FLOW CHART for sector protection waveforms and algorithm.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A_9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical "1" code at device output DQ_0 for a protected sector. Otherwise the devices will read 00h for unprotected sector. In this mode, the lower order addresses, except for A_0, A_1, and A_6 are DON'T CARES. Address locations with A_1 = V_{IL} are reserved for Autoselect manufacturer and device codes. A_{-1} requires to apply to V_{IL} on byte mode.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02h, where the higher order addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) are the desired sector address will produce a logical "1" at DQ_0 for a protected sector. See "MBM29DL800TA/BA Sector Protection Verify Autoselect Codes Table" and "Extended Autoselect Code Table" in ■DEVICE BUS OPERATION for Autoselect codes.

Temporary Sector Unprotection

This feature allows temporary unprotection of previously protected sectors of the MBM29DL800TA/BA devices in order to change data. The Sector Unprotection mode is activated by setting the $\overline{RESET}$ pin to high voltage (12 V). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once the 12 V is taken away from the $\overline{RESET}$ pin, all the previously protected sectors will be protected again. See "(14) Temporary Sector Unprotection Timing Diagram" in ■TIMING DIAGRAM and "(6) Temporary Sector Unprotection Algorithm" in ■FLOW CHART.

RESET

Hardware Reset

The MBM29DL800TA/BA devices may be reset by driving the $\overline{RESET}$ pin to V_{IL}. The $\overline{RESET}$ pin has a pulse requirement and has to be kept low (V_{IL}) for at least 500 ns in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset to the read mode 20 µs after the $\overline{RESET}$ pin is driven low. Furthermore, once the $\overline{RESET}$ pin goes high, the devices require an additional t_{RH} before it will allow read access. When the $\overline{RESET}$ pin is low, the devices will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted. Please note that the RY/$\overline{BY}$ output signal should be ignored during the $\overline{RESET}$ pulse. See "(9) $\overline{RESET}$/RY/$\overline{BY}$ Timing Diagram" in ■TIMING DIAGRAM for the timing diagram. Refer to Temporary Sector Unprotection for additional functionality.

■ COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the devices to the read mode. Some commands are required Bank Address (BA) input. When command sequences are inputed to bank being read, the commands have priority than reading. "MBM29DL800TA/BA Command Definitions Table" in ■DEVICE BUS OPERATION defines the valid register command sequences. Note that the Erase Suspend (B0h) and Erase Resume (30h) commands are valid only while the Sector Erase operation is in progress. Moreover both Read/Reset commands are functionally equivalent, resetting the device to the read mode. Please note that commands are always written at DQ_0 to DQ_7 and DQ_8 to DQ_{15} bits are ignored.

Read/Reset Command

In order to return from Autoselect mode or Exceeded Timing Limits (DQ_5 = 1) to Read/Reset mode, the Read/Reset operation is initiated by writing the Read/Reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The devices remain enabled for reads until the command register contents are altered.

The devices will automatically power-up in the Read/Reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the devices reside in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an Autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the Autoselect command sequence into the command register.

The Autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address (BA) and the Autoselect command. Then the manufacture and device codes can be read from the bank, and an actual data of memory cell can be read from the another bank.

Following the command write, a read cycle from address (BA)00h retrieves the manufacture code of 04h. A read cycle from address (BA)01h for ×16((BA)02h for ×8) returns the device code (MBM29DL800TA = 4Ah and MBM29DL800BA = CBh for ×8 mode; MBM29DL800TA = 224Ah and MBM29DL800BA = 22CBh for ×16 mode). (See "MBM29DL800TA/BA Sector Protection Verify Autoselect Codes Table" and "Extended Autoselect Code Table" in ■DEVICE BUS OPERATION.)

All manufacturer and device codes will exhibit odd parity with DQ_7 defined as the parity bit. Sector state (protection or unprotection) will be informed by address (BA)02h for ×16 ((BA)04h for ×8). Scanning the sector addresses (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13}, and A_{12}) while (A_6, A_1, A_0) = (0, 1, 0) will produce a logical "1" at device output DQ_0 for a protected sector. The programming verification should be performed by verify sector protection on the protected sector. (See "MBM29DL800TA/BA User Bus Operations Tables ($\overline{BYTE}$ = V_{IH} and $\overline{BYTE}$ = V_{IL})" in ■DEVICE BUS OPERATION.)

The manufacture and device codes can be allowed reading from selected bank. To read the manufacture and device codes and sector protection status from non-selected bank, it is necessary to write Read/Reset command sequence into the register and then Autoselect command should be written into the bank to be read.

If the software (program code) for Autoselect command is stored into the Frash memory, the device and manufacture codes should be read from the other bank where is not contain the software.

To terminate the operation, it is necessary to write the Read/Reset command sequence into the register, and also to write the Autoselect command during the operation, execute it after writing Read/Reset command sequence.

Byte/Word Programming

The devices are programmed on a byte-by-byte (or word-by-word) basis. Programming is a four bus cycle operation. There are two “unlock” write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence, the system is not required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The system can determine the status of the program operation by using DQ_7 ($\overline{Data}$ Polling), DQ_6 (Toggle Bit), or RY/$\overline{BY}$. The $\overline{Data}$ Polling and Toggle Bit must be performed at the memory location which is being programmed.

The automatic programming operation is completed when the data on DQ_7 is equivalent to data written to this bit at which time the devices return to the read mode and addresses are no longer latched. (See “Hardware Sequence Flags Table”.) Therefore, the devices require that a valid address to the devices be supplied by the system at this particular instance of time. Hence, $\overline{Data}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored. If hardware reset occurs during the programming operation, it is impossible to guarantee the data are being written.

Programming is allowed in any sequence and across sector boundaries. Beware that a data “0” cannot be programmed back to a “1”. Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from Read/Reset mode will show that the data is still “0”. Only erase operations can convert “0”s to “1”s.

“(1) Embedded Program™ Algorithm” in ■FLOW CHART illustrates the Embedded Program™ Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the chip erase command.

Chip erase does not require the user to program the device prior to erase. Upon executing the Embedded Erase Algorithm command sequence the devices will automatically program and verify the entire memory for an all zero data pattern prior to electrical erase (Preprogram function). The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{Data}$ Polling), DQ_6 (Toggle Bit), or RY/$\overline{BY}$. The chip erase begins on the rising edge of the last $\overline{CE}$ or $\overline{WE}$, whichever happens first in the command sequence and terminates when the data on DQ_7 is “1” (See Write Operation Status section.) at which time the device returns to read the mode.

Chip Erase Time; Sector Erase Time $\times$ All sectors + Chip Program Time (Preprogramming)

“(2) Embedded Erase™ Algorithm” in ■FLOW CHART illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two “unlock” write cycles. These are followed by writing the “set-up” command. Two more “unlock” write cycles are then followed by the Sector Erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ whichever happens later, while the command (Data=30h) is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$ which happens first. After time-out of 50 µs from the rising edge of the last sector erase command, the sector erase operation will begin.

Multiple sectors may be erased concurrently by writing the six bus cycle operations on “MBM29DL800TA/BA Command Definitions Table” in ■DEVICE BUS OPERATION. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 50 µs otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 50 µs from the rising edge of last $\overline{CE}$ or $\overline{WE}$ whichever happens first will initiate the execution of the Sector Erase command(s). If another falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first occurs within the 50 µs time-out window the timer is reset. (Monitor DQ_3 to determine if the sector erase timer window is still open, see section DQ_3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this time-out period will reset the devices to the read mode, ignoring the previous command string. Resetting the devices once execution has begun will corrupt the data in the sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 21).

Sector erase does not require the user to program the devices prior to erase. The devices automatically program all memory locations in the sector(s) to be erased prior to electrical erase (Preprogram function). When erasing a sector or sectors the remaining unselected sectors are not affected. The system is not required to provide any controls or timings during these operations.

The system can determine the status of the erase operation by using DQ_7 ($\overline{\text{Data}}$ Polling), DQ_6 (Toggle Bit), or RY/$\overline{BY}$.

The sector erase begins after the 50 µs time out from the rising edge of $\overline{CE}$ or $\overline{WE}$ whichever happens first for the last sector erase command pulse and terminates when the data on DQ_7 is “1” (See Write Operation Status section.) at which time the devices return to the read mode. $\overline{\text{Data}}$ polling and Toggle Bit must be performed at an address within any of the sectors being erased.

Multiple Sector Erase Time; [Sector Erase Time + Sector Program Time (Preprogramming)] × Number of Sector Erase

In case of multiple sector erase across bank boundaries, a read from bank (read-while-erase) can not performe.

“(2) Embedded Erase™ Algorithm” in ■FLOW CHART illustrates the Embedded Erase™ Algorithm using typical command strings and bus operations.

Erase Suspend/Resume

The Erase Suspend command allows the user to interrupt a Sector Erase operation and then perform data reads from or programs to a sector not being erased. This command is applicable ONLY during the Sector Erase operation which includes the time-out period for sector erase. The Erase Suspend command will be ignored if written during the Chip Erase operation or Embedded Program Algorithm. Writting the Erase Suspend command (B0h) during the Sector Erase time-out results in immediate termination of the time-out period and suspension of the erase operation.

Writing the Erase Resume command (30h) resumes the erase operation. The bank addresses of sector being erasing or suspending should be set when writting the Erase Suspend or Erase Resume command.

When the Erase Suspend command is written during the Sector Erase operation, the device will take a maximum of 20 µs to suspend the erase operation. When the devices have entered the erase-suspended mode, the RY/$\overline{BY}$ output pin will be at Hi-Z and the DQ_7 bit will be at logic “1”, and DQ_6 will stop toggling. The user must use the address of the erasing sector for reading DQ_6 and DQ_7 to determine if the erase operation has been suspended. Further writes of the Erase Suspend command are ignored.

When the erase operation has been suspended, the devices default to the erase-suspend-read mode. Reading data in this mode is the same as reading from the standard read mode except that the data must be read from sectors that have not been erase-suspended. Successively reading from the erase-suspended sector while the device is in the erase-suspend-read mode will cause DQ_2 to toggle. (See the section on DQ_2.)

After entering the erase-suspend-read mode, the user can program the device by writing the appropriate command sequence for Program. This program mode is known as the erase-suspend-program mode. Again, programming in this mode is the same as programming in the regular Program mode except that the data must be programmed to sectors that are not erase-suspended. Successively reading from the erase-suspended sector while the devices are in the erase-suspend-program mode will cause DQ_2 to toggle. The end of the erase-suspended Program operation is detected by the RY/$\overline{BY}$ output pin, $\overline{Data}$ polling of DQ_7 or by the Toggle Bit I (DQ_6) which is the same as the regular Program operation. Note that DQ_7 must be read from the Program address while DQ_6 can be read from any address within bank being erase-suspended.

To resume the operation of Sector Erase, the Resume command (30h) should be written to the bank being erase suspended. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Extended Command

(1) Fast Mode

MBM29DL800TA/BA has Fast Mode function. This mode dispenses with the initial two unclock cycles required in the standard program command sequence by writing Fast Mode command into the command register. In this mode, the required bus cycle for programming is two cycles instead of four bus cycles in standard program command. (Do not write erase command in this mode.) The read operation is also executed after exiting this mode. To exit this mode, it is necessary to write Fast Mode Reset command into the command register. The first cycle must contain the bank address. (Refer to “(8) Embedded Program™ Algorithm for Fast Mode” in ■FLOW CHART Extended algorithm.) The V_{CC} active current is required even $\overline{CE}$ = V_{IH} during Fast Mode.

(2) Fast Programming

During Fast Mode, the programming can be executed with two bus cycles operation. The Embedded Program Algorithm is executed by writing program set-up command (A0h) and data write cycles (PA/PD). (Refer to “(8) Embedded Program™ Algorithm for Fast Mode” in ■FLOW CHART Extended algorithm.)

(3) Extended Sector Protection

In addition to normal sector protection, the MBM29DL800TA/BA has Extended Sector Protection as extended function. This function enable to protect sector by forcing V_{ID} on $\overline{RESET}$ pin and write a commnad sequence. Unlike conventional procedure, it is not necessary to force V_{ID} and control timing for control pins. The only $\overline{RESET}$ pin requires V_{ID} for sector protection in this mode. The extended sector protect requires V_{ID} on $\overline{RESET}$ pin. With this condition, the operation is initiated by writing the set-up command (60h) into the command register. Then, the sector addresses pins (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set to the sector to be protected (recommend to set V_{IL} for the other addresses pins), and write extended sector protect command (60h). A sector is typically protected in 250 µs. To verify programming of the protection circuitry, the sector addresses pins (A_{18}, A_{17}, A_{16}, A_{15}, A_{14}, A_{13} and A_{12}) and (A_6, A_1, A_0) = (0, 1, 0) should be set and write a command (40h). Following the command write, a logical “1” at device output DQ_0 will produce for protected sector in the read operation. If the output data is logical “0”, please repeat to write extended sector protect command (60h) again. To terminate the operation, it is necessary to set $\overline{RESET}$ pin to V_{IH}.

Write Operation Status

Detailed in “Hardware Sequence Flags Table” are all the status flags that can determine the status of the bank for the current mode operation. The read operation from the bank where is not operate Embedded Algorithm returns a data of memory cell. These bits offer a method for determining whether a Embedded Algorithm is completed properly. The information on DQ_2 is address sensitive. This means that if an address from an erasing sector is consectively read, then the DQ_2 bit will toggle. However, DQ_2 will not toggle if an address from a non-erasing sector is consectively read. This allows the user to determine which sectors are erasing and which are not.

The status flag is not output from bank (non-busy bank) not executing Embedded Algorithm. For example, there is bank (busy bank) which is now executing Embedded Algorithm. When the read sequence is [1] <busy bank>, [2] <non-busy bank>, [3] <busy bank>, the DQ_6 is toggling in the case of [1] and [3]. In case of [2], the data of memory cell is outputted. In the erase-suspend read mode with the same read sequence, DQ_6 will not be toggled in the [1] and [3].

In the erase suspend read mode, DQ_2 is toggled in the [1] and [3]. In case of [2], the data of memory cell is outputted.

Hardware Sequence Flags Table

Status			DQ_7	DQ_6	DQ_5	DQ_3	DQ_2
In Progress	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	0	0	1
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle*1
	Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	1	0	0	Toggle
		Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data
		Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	0	0	1*2
Exceeded Time Limits	Embedded Program Algorithm		$\overline{DQ_7}$	Toggle	1	0	1
	Embedded Erase Algorithm		0	Toggle	1	1	N/A
	Erase Suspended Mode	Erase Suspend Program (Non-Erase Suspended Sector)	$\overline{DQ_7}$	Toggle	1	0	N/A

*1 : Successive reads from the erasing or erase-suspend sector cause DQ_2 to toggle.

*2 : Reading from non-erase suspend sector address indicates logic “1” at the DQ_2 bit.

DQ_7

Data Polling

The MBM29DL800TA/BA devices feature Data Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the devices will produce the complement of the data last written to DQ_7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ_7. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ_7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a "1" at the DQ_7 output. The flowchart for Data Polling (DQ_7) is shown in "(3) Data Polling Algorithm" in ■FLOW CHART.

For programming, the Data Polling is valid after the rising edge of fourth write pulse in the four write pulse sequence.

For chip erase and sector erase, the Data Polling is valid after the rising edge of the sixth write pulse in the six write pulse sequence. Data Polling must be performed at sector address within any of the sectors being erased and not a protected sector. Otherwise, the status may not be valid.

If a program address falls within a protected sector, Data Polling on DQ_7 is active for approximately 1 µs, then that bank returns to the read mode. After an erase command sequence is written, if all sectors selected for erasing are protected, Data Polling on DQ_7 is active for approximately 100 µs, then the bank returns to read mode.

Once the Embedded Algorithm operation is close to being completed, the MBM29DL800TA/BA data pins (DQ_7) may change asynchronously while the output enable ($\overline{OE}$) is asserted low. This means that the devices are driving status information on DQ_7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ_7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ_7 has a valid data, the data outputs on DQ_0 to DQ_6 may be still invalid. The valid data on DQ_0 to DQ_7 will be read on the successive read attempts.

The Data Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm or sector erase time-out. (See "Hardware Sequence Flags Table".)

See "(6) AC Waveforms for Data Polling during Embedded Algorithm Operations" in ■TIMING DIAGRAM for the Data Polling timing specifications and diagrams.

DQ_6

Toggle Bit I

The MBM29DL800TA/BA also feature the "Toggle Bit I" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{OE}$ toggling) data from the devices will result in DQ_6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ_6 will stop toggling and valid data will be read on the next successive attempts. During programming, the Toggle Bit I is valid after the rising edge of the fourth write pulse in the four write pulse sequence. For chip erase and sector erase, the Toggle Bit I is valid after the rising edge of the sixth write pulse in the six write pulse sequence. The Toggle Bit I is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 2 µs and then stop toggling without the data having changed. In erase, the devices will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 100 µs and then drop back into read mode, having changed none of the data.

Either $\overline{CE}$ or $\overline{OE}$ toggling will cause the DQ_6 to toggle. In addition, an Erase Suspend/Resume command will cause the DQ_6 to toggle.

The system can use DQ_6 to determine whether a sector is actively erasing or is erase-suspended. When a bank is actively erasing (that is, the Embedded Erase Algorithm is in progress), DQ_6 toggles. When a bank enters the Erase Suspend mode, DQ_6 stops toggling. Successive read cycles during the erase-suspend-program cause DQ_6 to toggle.

To operate toggle bit function properly, $\overline{CE}$ or $\overline{OE}$ must be high when bank address is changed.

See "(7) AC Waveforms for Toggle Bit I during Embedded Algorithm Operations" in ■TIMING DIAGRAM for the Toggle Bit I timing specifications and diagrams.

DQ_5

Exceeded Timing Limits

DQ_5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ_5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{Data}$ Polling is the only operating function of the devices under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in "MBM29DL800TA/BA User Bus Operations Tables ($\overline{BYTE}$ = V_{IH} and $\overline{BYTE}$ = V_{IL})" (in ■DEVICE BUS OPERATION).

The DQ_5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the devices lock out and never complete the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ_7 bit and DQ_6 never stops toggling. Once the devices have exceeded timing limits, the DQ_5 bit will indicate a "1." Please note that this is not a device failure condition since the devices were incorrectly used. If this occurs, reset the device with command sequence.

DQ_3

Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ_3 will remain low until the time-out is complete. $\overline{Data}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{Data}$ Polling or the Toggle Bit I indicates the device has been written with a valid erase command, DQ_3 may be used to determine if the sector erase timer window is still open. If DQ_3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{Data}$ Polling or Toggle Bit I. If DQ_3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ_3 prior to and following each subsequent Sector Erase command. If DQ_3 were high on the second status check, the command may not have been accepted.

See "Hardware Sequence Flags Table".

DQ_2

Toggle Bit II

This toggle bit II, along with DQ_6, can be used to determine whether the devices are in the Embedded Erase Algorithm or in Erase Suspend.

Successive reads from the erasing sector will cause DQ_2 to toggle during the Embedded Erase Algorithm. If the devices are in the erase-suspended-read mode, successive reads from the erase-suspended sector will cause DQ_2 to toggle. When the devices are in the erase-suspended-program mode, successive reads from the byte address of the non-erase suspended sector will indicate a logic "1" at the DQ_2 bit.

DQ_6 is different from DQ_2 in that DQ_6 toggles only when the standard program or Erase, or Erase Suspend Program operation is in progress. The behavior of these two status bits, along with that of DQ_7, is summarized as follows:

For example, DQ_2 and DQ_6 can be used together to determine if the erase-suspend-read mode is in progress. (DQ_2 toggles while DQ_6 does not.) See also "Hardware Sequence Flags Table" and "(16) DQ_2 vs. DQ_6" in ■TIMING DIAGRAM.

Furthermore, DQ_2 can also be used to determine which sector is being erased. When the device is in the erase mode, DQ_2 toggles if this bit is read from an erasing sector.

To operate toggle bit function properly, $\overline{CE}$ or $\overline{OE}$ must be high when bank address is changed.

Reading Toggle Bits DQ_6/DQ_2

Whenever the system initially begins reading toggle bit status, it must read DQ_7 to DQ_0 at least twice in a row to determine whether a toggle bit is toggling. Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, this indicates that the device has completed the program or erase operation. The system can read array data on DQ_7 to DQ_0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ_5 is high (see "the section on DQ_5") . If it is the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ_5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ_5 has not gone high. The system may continue to monitor the toggle bit and DQ_5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (See "(4) Toggle bit algorithm" in ■FLOW CHART) .

Toggle Bit Status Table

Mode	DQ_7	DQ_6	DQ_2
Program	$\overline{DQ_7}$	Toggle	1
Erase	0	Toggle	Toggle*1
Erase-Suspend Read (Erase-Suspended Sector)	1	1	Toggle
Erase-Suspend Program	$\overline{DQ_7}$	Toggle	1*2

*1 : Successive reads from the erasing or erase-suspend sector cause DQ_2 to toggle.

*2 : Reading from non-erase suspend sector address indicates logic "1" at the DQ_2 bit.

RY/$\overline{BY}$

Ready/Busy

The MBM29DL800TA/BA provide a RY/$\overline{BY}$ open-drain output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or has been completed. If the output is low, the devices are busy with either a program or erase operation. If the output is high, the devices are ready to accept any read/ write or erase operation. When the RY/$\overline{BY}$ pin is low, the devices will not accept any additional program or erase commands. If the MBM29DL800TA/BA are placed in an Erase Suspend mode, the RY/$\overline{BY}$ output will be high.

During programming, the RY/$\overline{BY}$ pin is driven low after the rising edge of the fourth write pulse. During an erase operation, the RY/$\overline{BY}$ pin is driven low after the rising edge of the sixth write pulse. The RY/$\overline{BY}$ pin will indicate a busy condition during the $\overline{RESET}$ pulse. Refer to "(8) RY/$\overline{BY}$ Timing Diagram during Program/Erase Operations" and "(9) $\overline{RESET}$/RY/$\overline{BY}$ Timing Diagram" in ■TIMING DIAGRAM for a detailed timing diagram. The RY/$\overline{BY}$ pin is pulled high in standby mode.

Since this is an open-drain output, the pull-up resistor needs to be connected to V_{CC}; multiples of devices may be connected to the host system via more than one RY/$\overline{BY}$ pin in parallel.

Byte/Word Configuration

The $\overline{BYTE}$ pin selects the byte (8-bit) mode or word (16-bit) mode for the MBM29DL800TA/BA devices. When this pin is driven high, the devices operate in the word (16-bit) mode. The data is read and programmed at DQ_0

to DQ_{15}. When this pin is driven low, the devices operate in byte (8-bit) mode. Under this mode, the DQ_{15}/A_{-1} pin becomes the lowest address bit and DQ_8 to DQ_{14} bits are tri-stated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ_0 to DQ_7 and the DQ_8 to DQ_{15} bits are ignored. Refer to “(10) Timing Diagram for Word Mode Configuration” and “(11) Timing Diagram for Byte Mode Configuration” and “(12) $\overline{\text{BYTE}}$ Timing Diagram for Write Operations” in ■TIMING DIAGRAM for the timing diagram.

Data Protection

The MBM29DL800TA/BA are designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the devices automatically reset the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The devices also incorporate several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 2.3 V (typically 2.4 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 2.3 V.

If Embedded Erase Algorithm is interrupted, there is possibility that the erasing sector(s) cannot be used.

Write Pulse “Glitch” Protection

Noise pulses of less than 3 ns (typical) on $\overline{\text{OE}}$, $\overline{\text{CE}}$, or $\overline{\text{WE}}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{\text{OE}} = V_{IL}$, $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{WE}} = V_{IH}$. To initiate a write cycle $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be a logical zero while $\overline{\text{OE}}$ is a logical one.

Power-Up Write Inhibit

Power-up of the devices with $\overline{\text{WE}} = \overline{\text{CE}} = V_{IL}$ and $\overline{\text{OE}} = V_{IH}$ will not accept commands on the rising edge of $\overline{\text{WE}}$. The internal state machine is automatically reset to the read mode on power-up.

Sector Protection

Device user is able to protect each sector individually to store and protect data. Protection circuit voids both program and erase commands that are addressed to protected sectors.

Any commands to program or erase addressed to protected sector are ignored (see “Sector Protection” in ■ FUNCTIONAL DESCRIPTION)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Storage Temperature	Tstg	–55	+125	°C
Ambient Temperature with Power Applied	T_A	–40	+85	°C
Voltage with respect to Ground All pins except A_9, $\overline{\text{OE}}$, $\overline{\text{RESET}}$ *2	V_{IN}, V_{OUT}	–0.5	V_{CC}+0.5	V
A_9, $\overline{\text{OE}}$, and $\overline{\text{RESET}}$ *1, *3	V_{IN}	–0.5	+13.0	V
Power Supply Voltage*1	V_{CC}	–0.5	+5.5	V

*1 : Voltage is defined on the basis of V_{SS} = GND = 0 V.

*2 : Minimum DC voltage on input or I/O pins are –0.5 V. During voltage transitions, input or I/O pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods of up to 20 ns.

*3 : Minimum DC input voltage on A_9, $\overline{\text{OE}}$ and $\overline{\text{RESET}}$ pins is –0.5 V. During voltage transitions, A_9, $\overline{\text{OE}}$ and $\overline{\text{RESET}}$ pins may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Voltage difference between input and supply voltage (V_{IN}–V_{CC}) does not exceed +9.0 V. Maximum DC input voltage on A_9, $\overline{\text{OE}}$ and $\overline{\text{RESET}}$ pins is +13.0 V which may overshoot to +14.0 V for periods of up to 20 ns.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Part No.	Value		Unit
			Min	Max	
Ambient Temperature	T_A	—	–40	+85	°C
Power Supply Voltages*	V_{CC}	-70	+3.0	+3.6	V
		-90	+2.7	+3.6	V

* : Voltage is defined on the basis of V_{SS} = GND = 0 V.

Note: Operating ranges define those limits between which the functionality of the devices are guaranteed.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ MAXIMUM OVERSHOOT/MAXIMUM UNDERSHOOT

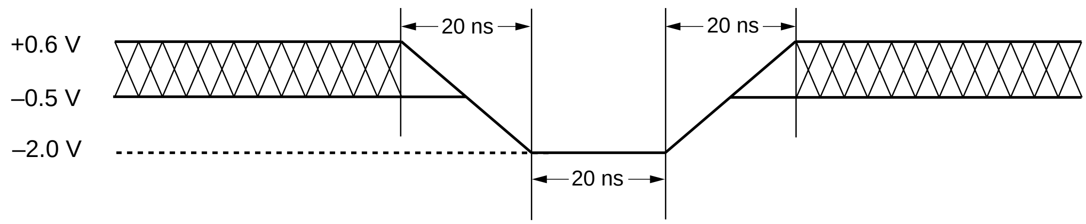


Figure 1 Maximum Undershoot Waveform

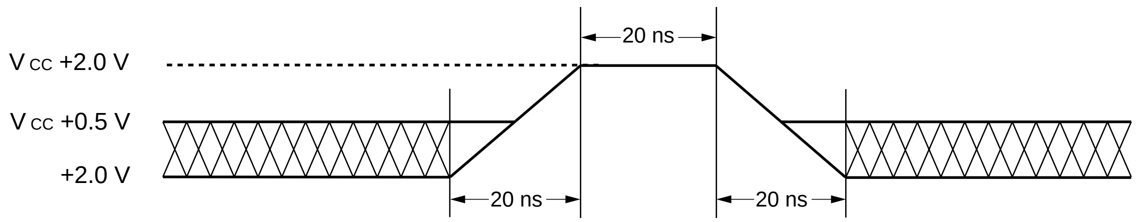
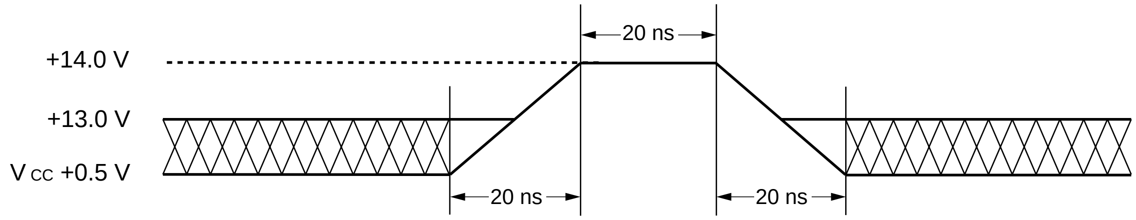


Figure 2 Maximum Overshoot Waveform 1



Note : This waveform is applied for A_9, $\overline{OE}$, and $\overline{RESET}$.

Figure 3 Maximum Overshoot Waveform 2

■ DC CHARACTERISTICS

Parameter	Symbol	Conditions		Value			Unit
				Min	Typ	Max	
Input Leakage Current	I_{LI}	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		–1.0	—	+1.0	µA
Output Leakage Current	I_{LO}	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		–1.0	—	+1.0	µA
A_9, $\overline{OE}$, $\overline{RESET}$ Inputs Leakage Current	I_{LIT}	$V_{CC} = V_{CC}$ Max A_9, $\overline{OE}$, $\overline{RESET}$ = 12.5 V		—	—	35	µA
V_{CC} Active Current *1	I_{CC1}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f=10 MHz	Byte	—	—	18	mA
			Word		—	20	
		$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f=5 MHz	Byte	—	—	8	mA
			Word		—	10	
V_{CC} Active Current *2	I_{CC2}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		—	—	35	mA
V_{CC} Current (Standby)	I_{CC3}	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{CC} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V		—	1	5	µA
V_{CC} Current (Standby, Reset)	I_{CC4}	$V_{CC} = V_{CC}$ Max, $\overline{RESET} = V_{SS} \pm 0.3$ V		—	1	5	µA
V_{CC} Current (Automatic Sleep Mode) *5	I_{CC5}	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{SS} \pm 0.3$ V, $\overline{RESET} = V_{CC} \pm 0.3$ V $V_{IN} = V_{CC} \pm 0.3$ V or $V_{SS} \pm 0.3$ V		—	1	5	µA
V_{CC} Active Current *6 (Read-While-Program)	I_{CC6}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	Byte	—	—	45	mA
			Word	—	—	45	
V_{CC} Active Current *6 (Read-While-Erase)	I_{CC7}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	Byte	—	—	45	mA
			Word	—	—	45	
V_{CC} Active Current (Erase-Suspend-Program)	I_{CC8}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		—	—	35	mA
Input Low Voltage	V_{IL}	—		–0.5	—	0.6	V
Input High Voltage	V_{IH}	—		2.0	—	V_{CC}+0.3	V
Voltage for Autoselect and Sector Protection (A_9, $\overline{OE}$, $\overline{RESET}$) *3, *4	V_{ID}	—		11.5	12	12.5	V
Output Low Voltage	V_{OL}	I_{OL} = 4.0 mA, $V_{CC} = V_{CC}$ Min		—	—	0.45	V
Output High Voltage	V_{OH1}	I_{OH} = –2.0 mA, $V_{CC} = V_{CC}$ Min		2.4	—	—	V
	V_{OH2}	I_{OH} = –100 µA		V_{CC}–0.4	—	—	V
Low V_{CC} Lock-Out Voltage	V_{LKO}	—		2.3	2.4	2.5	V

*1 : The I_{CC} current listed includes both the DC operating current and the frequency dependent component.

*2 : I_{CC} active while Embedded Algorithm (program or erase) is in progress.

*3 : This timing is only for Sector Protection operation and Autoselect mode.

*4 : Applicable for only V_{CC} applying.

*5 : Automatic sleep mode enables the low power mode when address remain stable for 150 ns.

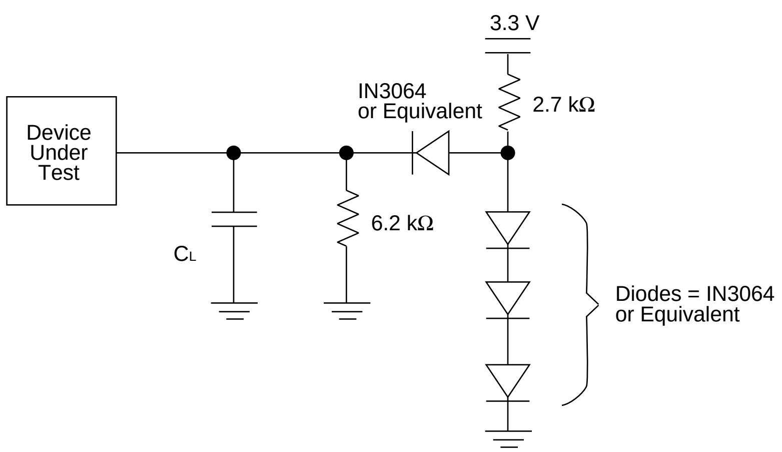
*6 : Embedded Algorithm (program or erase) is in progress. (@5 MHz)

■ AC CHARACTERISTICS

• **Read Only Operations Characteristics**

Parameter	Symbols		Test Setup	Value (Note)				Unit
				-70		-90		
	JEDEC	Standard		Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	—	70	—	90	—	ns
Address to Output Delay	t_{AVQV}	t_{ACC}	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	—	70	—	90	ns
Chip Enable to Output Delay	t_{ELQV}	t_{CE}	$\overline{OE} = V_{IL}$	—	90	—	90	ns
Output Enable to Output Delay	t_{GLQV}	t_{OE}	—	—	30	—	35	ns
Chip Enable to Output High-Z	t_{EHQZ}	t_{DF}	—	—	25	—	30	ns
Output Enable to Output High-Z	t_{GHQZ}	t_{DF}	—	—	25	—	30	ns
Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First	t_{AXQX}	t_{OH}	—	0	—	0	—	ns
$\overline{RESET}$ Pin Low to Read Mode	—	t_{READY}	—	—	20	—	20	µs
$\overline{CE}$ to $\overline{BYTE}$ Switching Low or High	—	t_{ELFL} t_{ELFH}	—	—	5	—	5	ns

Note: Test Conditions:
Output Load: 1TTL gate and 30 pF (MBM29DL800TA/BA-70)
1TTL gate and 100 pF (MBM29DL800TA/BA-90
Input rise and fall times: 5 ns
Input pulse levels: 0.0 V or 3.0 V
Timing measurement reference level
Input: 1.5 V
Output:1.5 V



Notes: C_L = 30 pF including jig capacitance (MBM29DL800TA/BA-70)
C_L = 100 pF including jig capacitance (MBM29DL800TA/BA-90)

Figure 4 Test Conditions

• **Write/Erase/Program Operations**

Parameter	Symbol JEDEC	Symbol Standard	-70 Min	-70 Typ	-70 Max	-90 Min	-90 Typ	-90 Max	Unit
Write Cycle Time	t_{AVAV}	t_{WC}	70	—	—	90	—	—	ns
Address Setup Time	t_{AVWL}	t_{AS}	0	—	—	0	—	—	ns
Address Setup Time to $\overline{OE}$ Low During Toggle Bit Polling	—	t_{ASO}	15	—	—	15	—	—	ns
Address Hold Time	t_{WLAX}	t_{AH}	45	—	—	45	—	—	ns
Address Hold Time from $\overline{CE}$ or $\overline{OE}$ High During Toggle Bit Polling	—	t_{AHT}	0	—	—	0	—	—	ns
Data Setup Time	t_{DVWH}	t_{DS}	35	—	—	45	—	—	ns
Data Hold Time	t_{WHDX}	t_{DH}	0	—	—	0	—	—	ns
Output Enable Hold Time – Read	—	t_{OEH}	0	—	—	0	—	—	ns
Output Enable Hold Time – Toggle and $\overline{Data}$ Polling	—	t_{OEH}	10	—	—	10	—	—	ns
$\overline{CE}$ High During Toggle Bit Polling	—	t_{CEPH}	20	—	—	20	—	—	ns
$\overline{OE}$ High During Toggle Bit Polling	—	t_{OEPH}	20	—	—	20	—	—	ns
Read Recover Time Before Write	t_{GHWL}	t_{GHWL}	0	—	—	0	—	—	ns
Read Recover Time Before Write	t_{GHEL}	t_{GHEL}	0	—	—	0	—	—	ns
$\overline{CE}$ Setup Time	t_{ELWL}	t_{CS}	0	—	—	0	—	—	ns
$\overline{WE}$ Setup Time	t_{WLEL}	t_{WS}	0	—	—	0	—	—	ns
$\overline{CE}$ Hold Time	t_{WHEH}	t_{CH}	0	—	—	0	—	—	ns
$\overline{WE}$ Hold Time	t_{EHWH}	t_{WH}	0	—	—	0	—	—	ns
Write Pulse Width	t_{WLWH}	t_{WP}	35	—	—	45	—	—	ns
$\overline{CE}$ Pulse Width	t_{ELEH}	t_{CP}	35	—	—	45	—	—	ns
Write Pulse Width High	t_{WHWL}	t_{WPH}	25	—	—	25	—	—	ns
$\overline{CE}$ Pulse Width High	t_{EHEL}	t_{CPH}	25	—	—	25	—	—	ns
Programming Operation – Byte	t_{WHWH1}	t_{WHWH1}	—	8	—	—	8	—	μs
Programming Operation – Word	t_{WHWH1}	t_{WHWH1}	—	16	—	—	16	—	μs
Sector Erase Operation *1	t_{WHWH2}	t_{WHWH2}	—	1	—	—	1	—	s
V_{CC} Setup Time	—	t_{VCS}	50	—	—	50	—	—	μs
Rise Time to V_{ID} *2	—	t_{VIDR}	500	—	—	500	—	—	ns
Voltage Transition Time *2	—	t_{VLHT}	4	—	—	4	—	—	μs
Write Pulse Width *2	—	t_{WPP}	100	—	—	100	—	—	μs
$\overline{OE}$ Setup Time to $\overline{WE}$ Active *2	—	t_{OESP}	4	—	—	4	—	—	μs

(Continued)

(Continued)

Parameter	Symbol		Value						Unit
			-70			-90			
	JEDEC	Standard	Min	Typ	Max	Min	Typ	Max	
$\overline{CE}$ Setup Time to $\overline{WE}$ Active *2	—	t_{CSP}	4	—	—	4	—	—	µs
Recover Time From RY/$\overline{BY}$	—	t_{RB}	0	—	—	0	—	—	ns
$\overline{RESET}$ Pulse Width	—	t_{RP}	500	—	—	500	—	—	ns
$\overline{RESET}$ Hold Time Before Read	—	t_{RH}	200	—	—	200	—	—	ns
$\overline{BYTE}$ Switching Low to Output High-Z	—	t_{FLQZ}	—	—	25	—	—	30	ns
$\overline{BYTE}$ Switching High to Output Active	—	t_{FHQV}	—	—	70	—	—	90	ns
Program/Erase Valid to RY/$\overline{BY}$ Delay	—	t_{BUSY}	—	—	90	—	—	90	ns
Delay Time from Embedded Output Enable	—	t_{EOE}	—	—	70	—	—	90	ns

*1 : This does not include the preprogramming time.

*2 : This timing is for Sector Protection operation.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Sector Erase Time	—	1	10	s	Excludes programming time prior to erasure
Word Programming Time	—	16	360	µs	Excludes system-level overhead
Byte Programming Time	—	8	300	µs	
Chip Programming Time	—	8.4	25	s	Excludes system-level overhead
Program/Erase Cycle	100,000	—	—	cycle	—

■ TSOP(1) PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C_{IN}	$V_{IN} = 0$	6	7.5	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$	8.5	12	pF
Control Pin Capacitance	C_{IN2}	$V_{IN} = 0$	8	10	pF

Notes : • Test conditions T_A = +25°C, f = 1.0 MHz
• DQ_{15}/A_{-1} pin capacitance is stipulated by output capacitance.

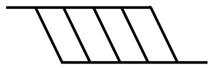
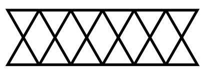
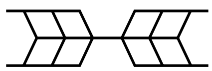
■ FBGA PIN CAPACITANCE

Parameter	Symbol	Test Setup	Value		Unit
			Typ	Max	
Input Capacitance	C_{IN}	$V_{IN} = 0$	6	7.5	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$	8.5	12	pF
Control Pin Capacitance	C_{IN2}	$V_{IN} = 0$	8	10	pF

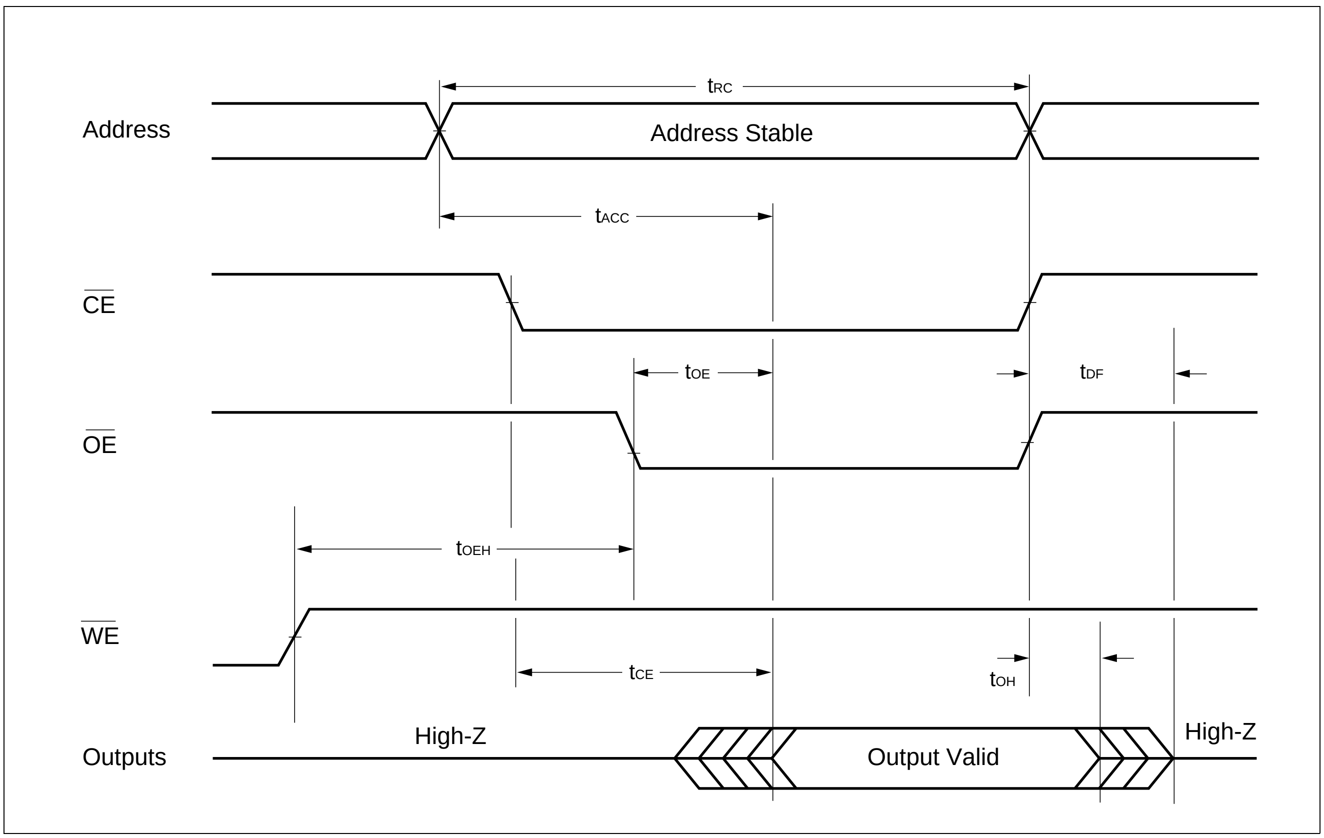
Notes : • Test conditions T_A = +25°C, f = 1.0 MHz
• DQ_{15}/A_{-1} pin capacitance is stipulated by output capacitance.

■ TIMING DIAGRAM

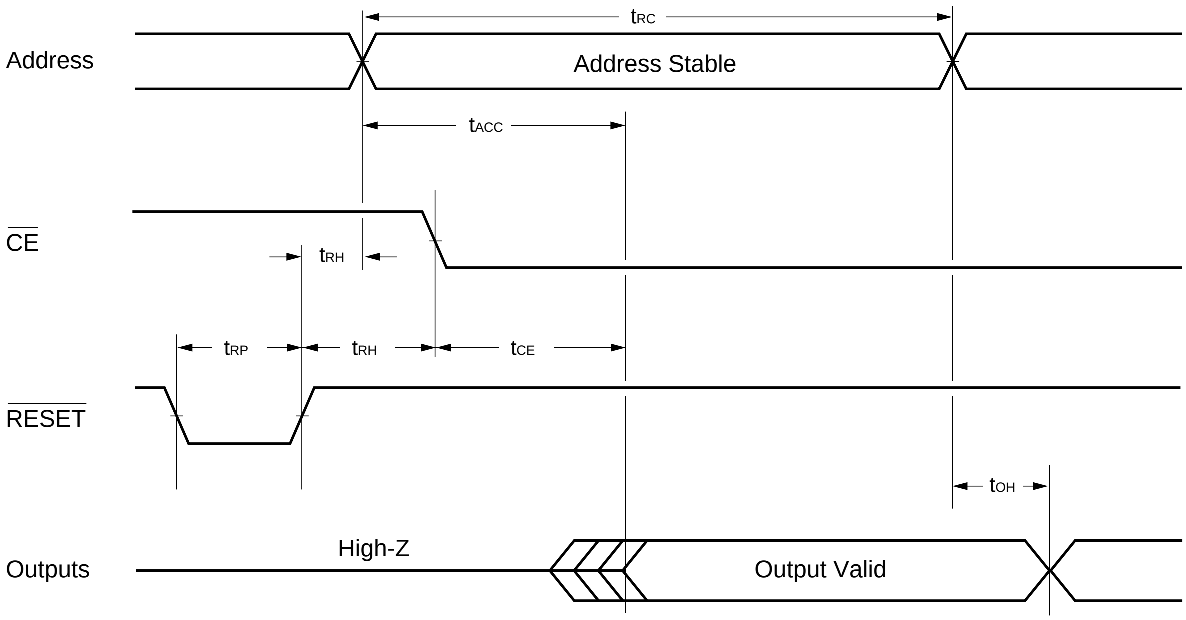
• **Key to Switching Waveforms**

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	"H" or "L" Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

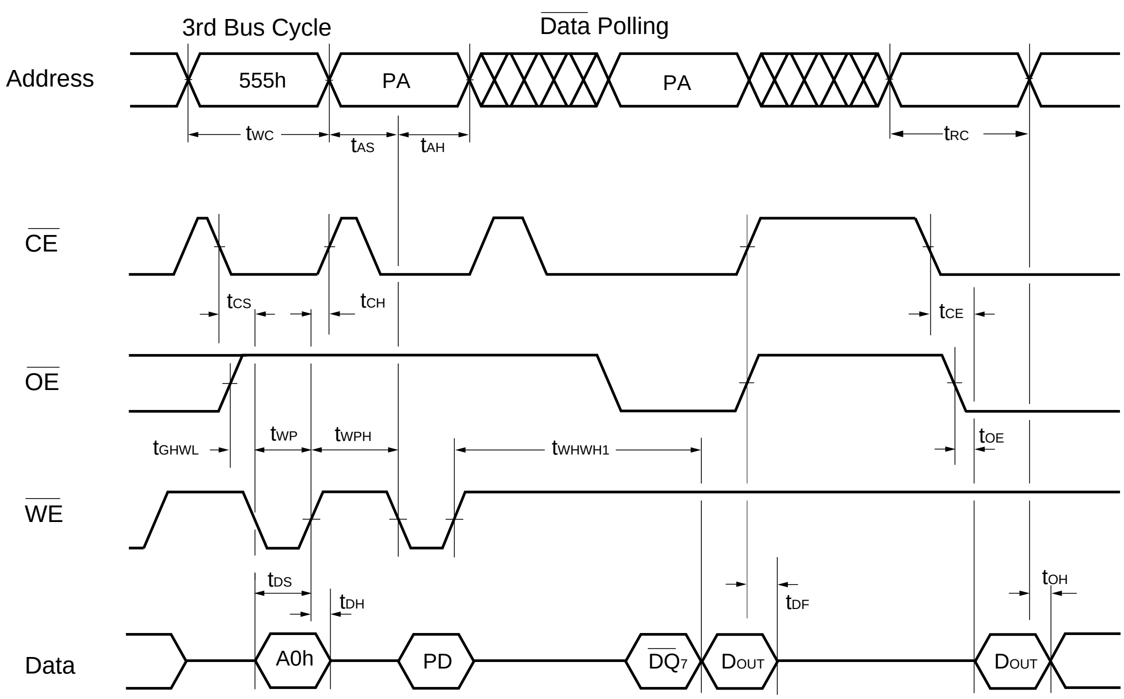
(1) AC Waveforms for Read Operations



(2) AC Waveforms for Hardware Reset/Read Operations

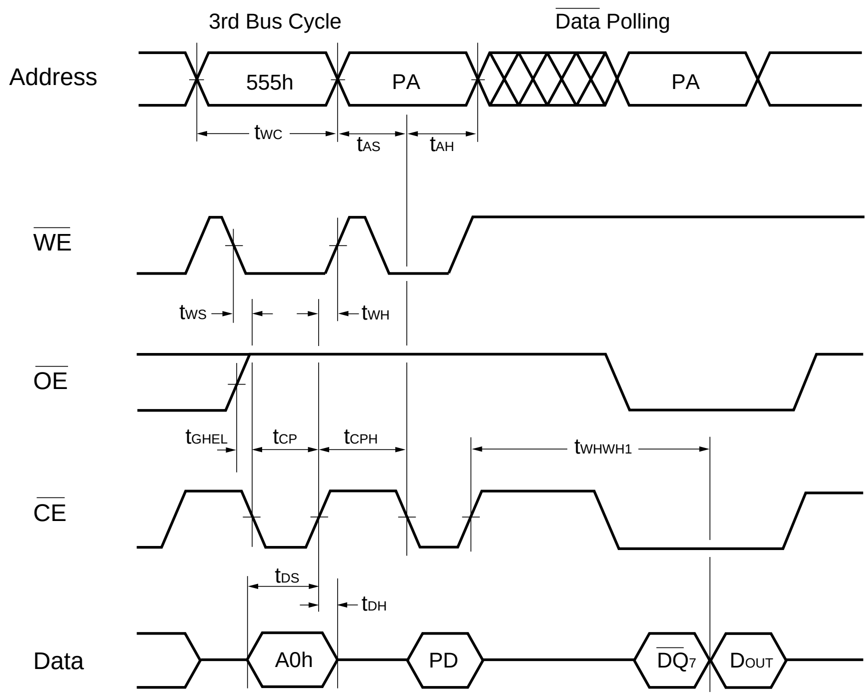


(3) Alternate WE Controlled Program Operations



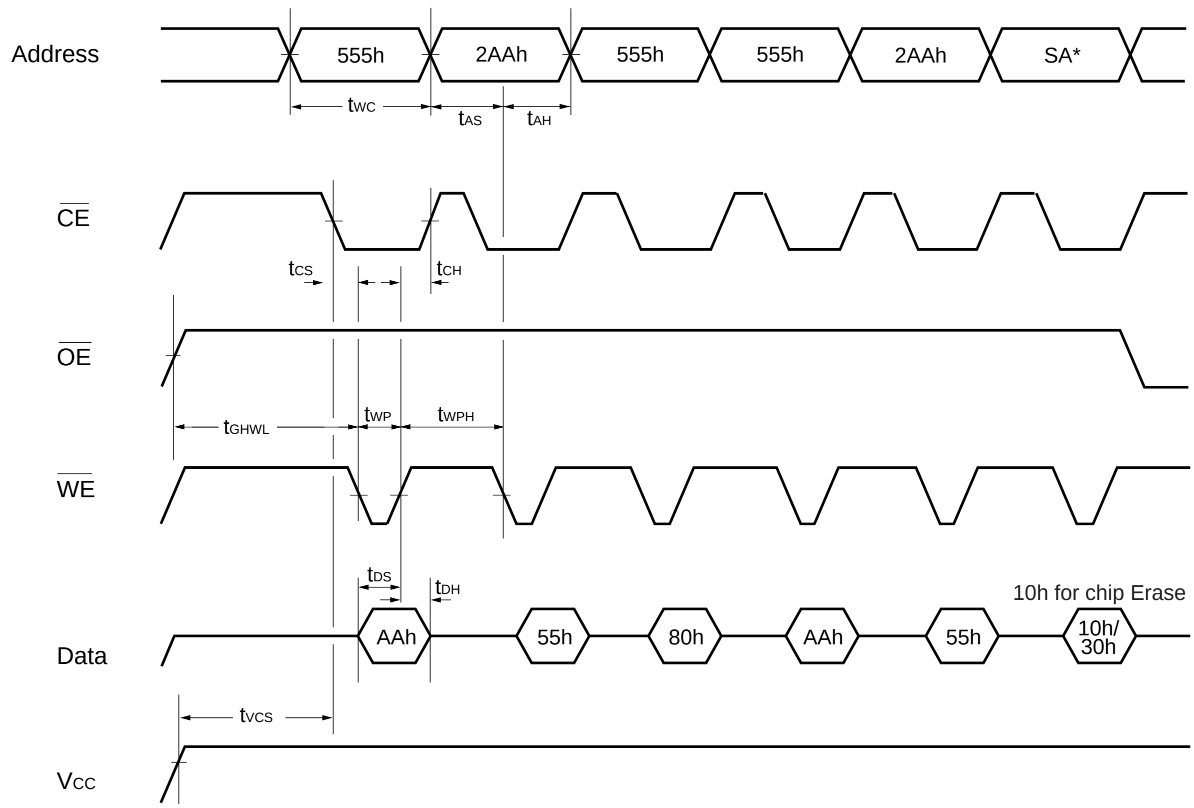
Notes:
- PA is address of the memory location to be programmed.
- PD is data to be programmed at byte address.
- $\overline{DQ_7}$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.
- These waveforms are for the ×16 mode. The addresses differ from ×8 mode.

(4) Alternate $\overline{CE}$ Controlled Program Operations



Notes:
- PA is address of the memory location to be programmed.
- PD is data to be programmed at byte address.
- $\overline{DQ_7}$ is the output of the complement of the data written to the device.
- D_{OUT} is the output of the data written to the device.
- Figure indicates last two bus cycles out of four bus cycle sequence.
- These waveforms are for the ×16 mode. (The addresses differ from ×8 mode.)

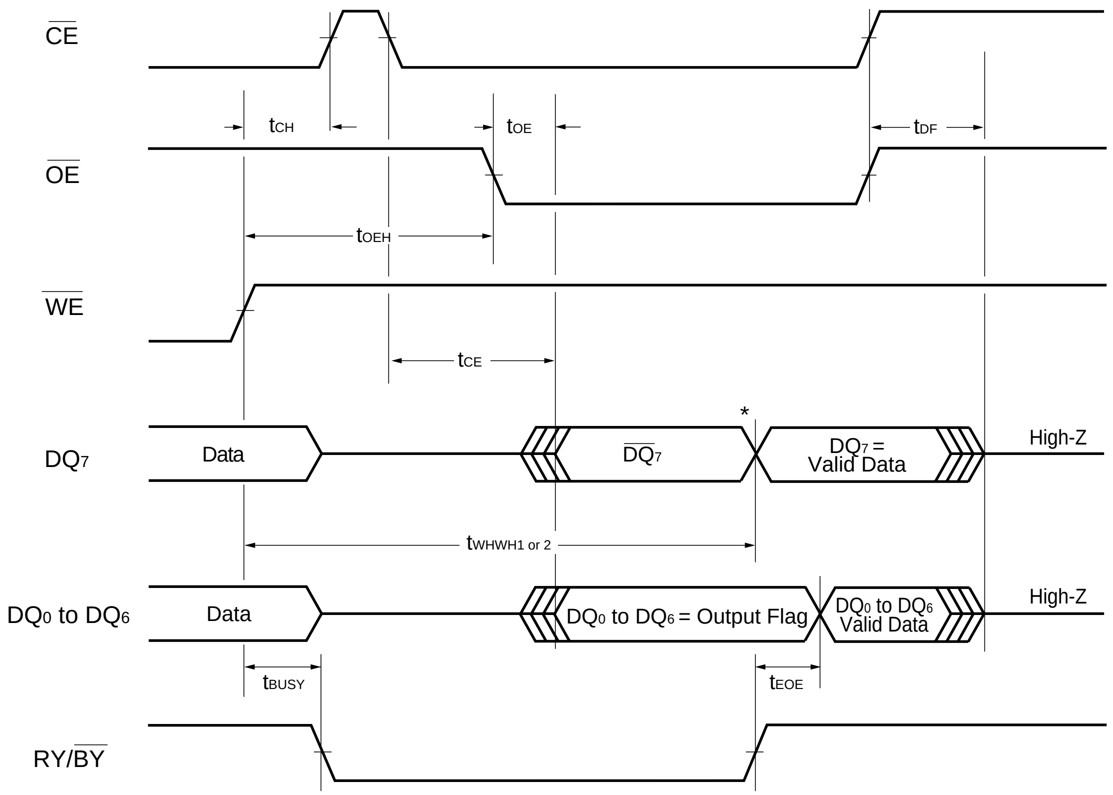
(5) AC Waveforms Chip/Sector Erase Operations



* : SA is the sector address for Sector Erase. Addresses = 555h (Word) for Chip Erase.

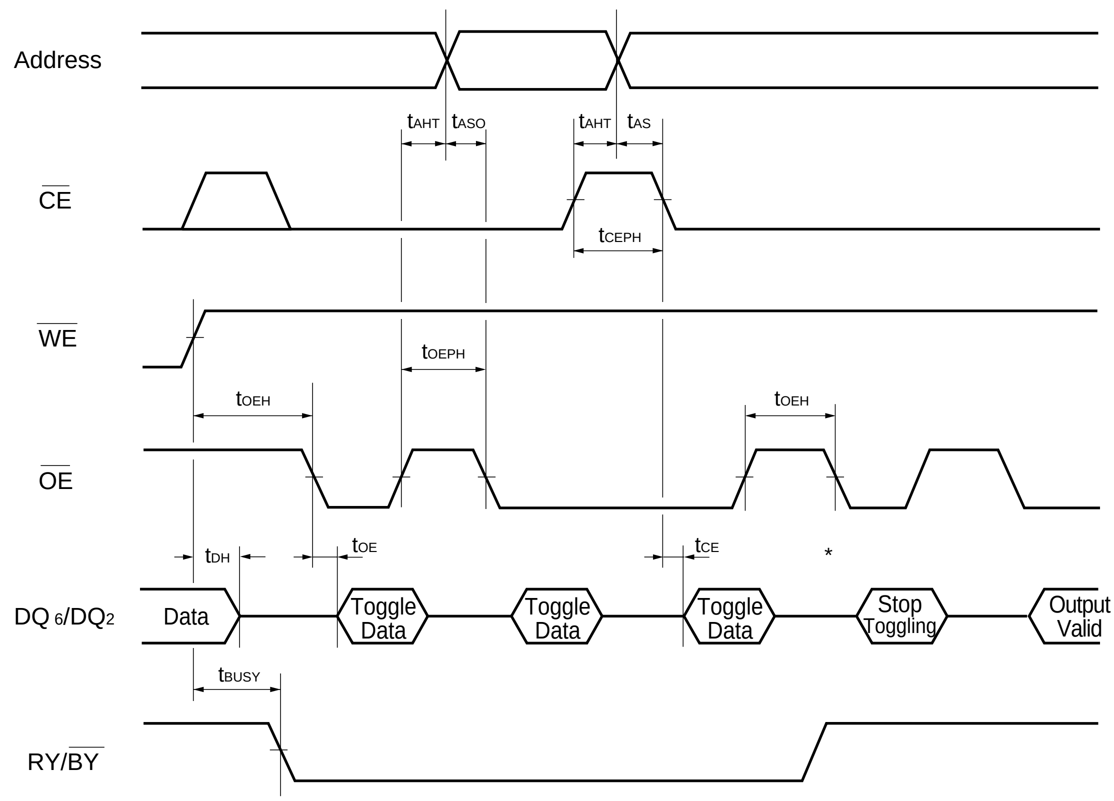
Note : These waveforms are for the ×16 mode. The addresses differ from ×8 mode.

(6) AC Waveforms for $\overline{\text{Data}}$ Polling during Embedded Algorithm Operations



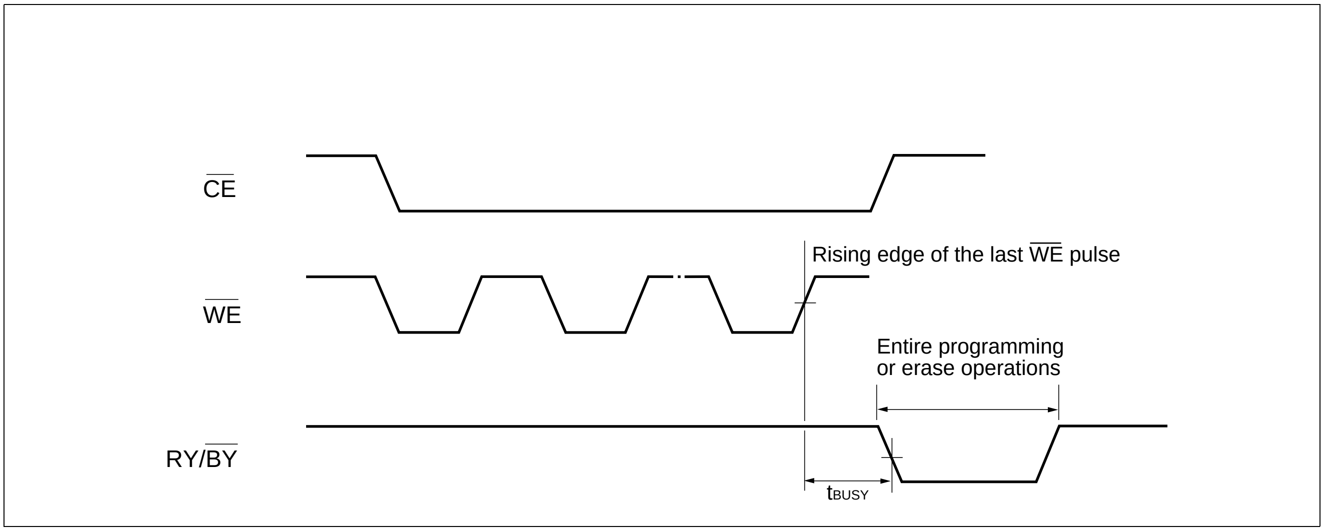
* : DQ_7 = Valid Data (The device has completed the Embedded operation).

(7) AC Waveforms for Toggle Bit I during Embedded Algorithm Operations

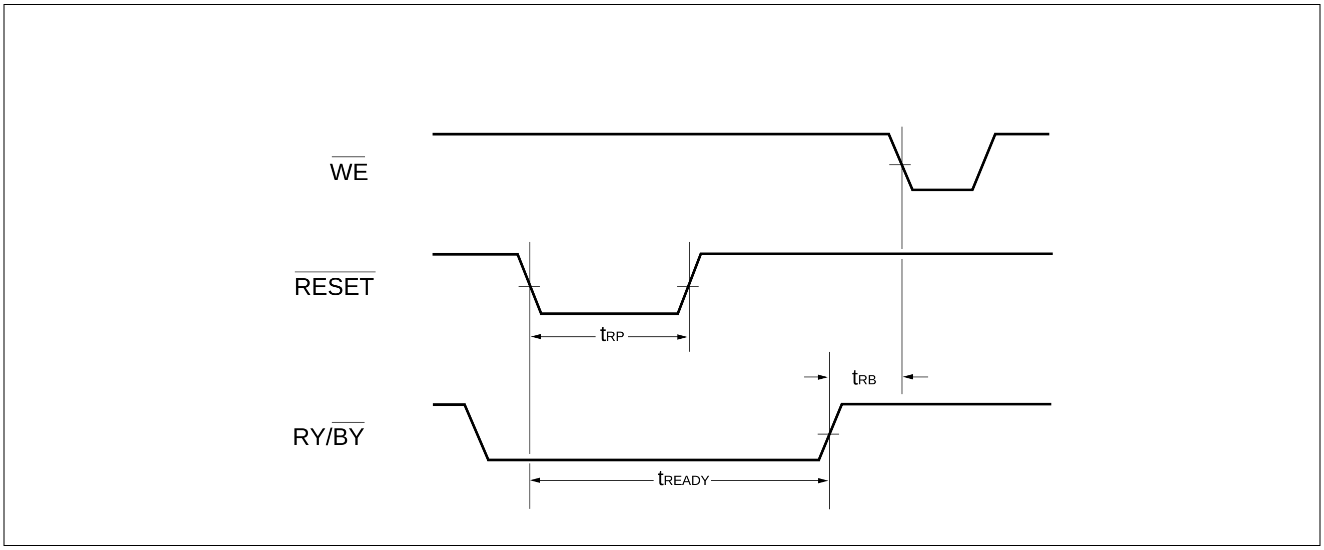


* : DQ_6 stops toggling (The device has completed the Embedded operation).

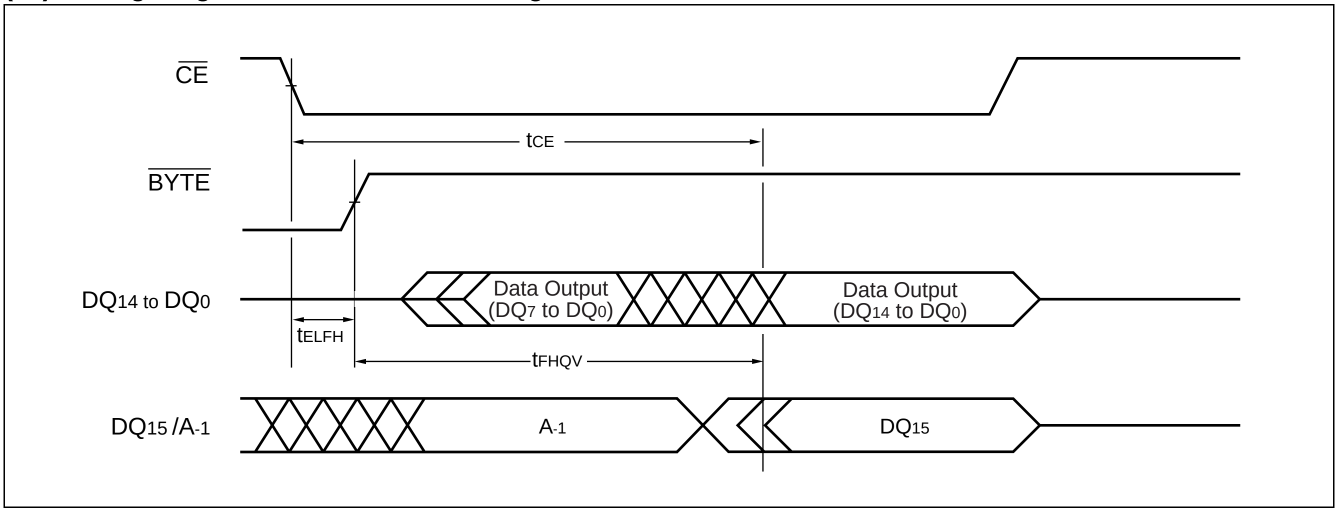
(8) RY/$\overline{\text{BY}}$ Timing Diagram during Program/Erase Operations



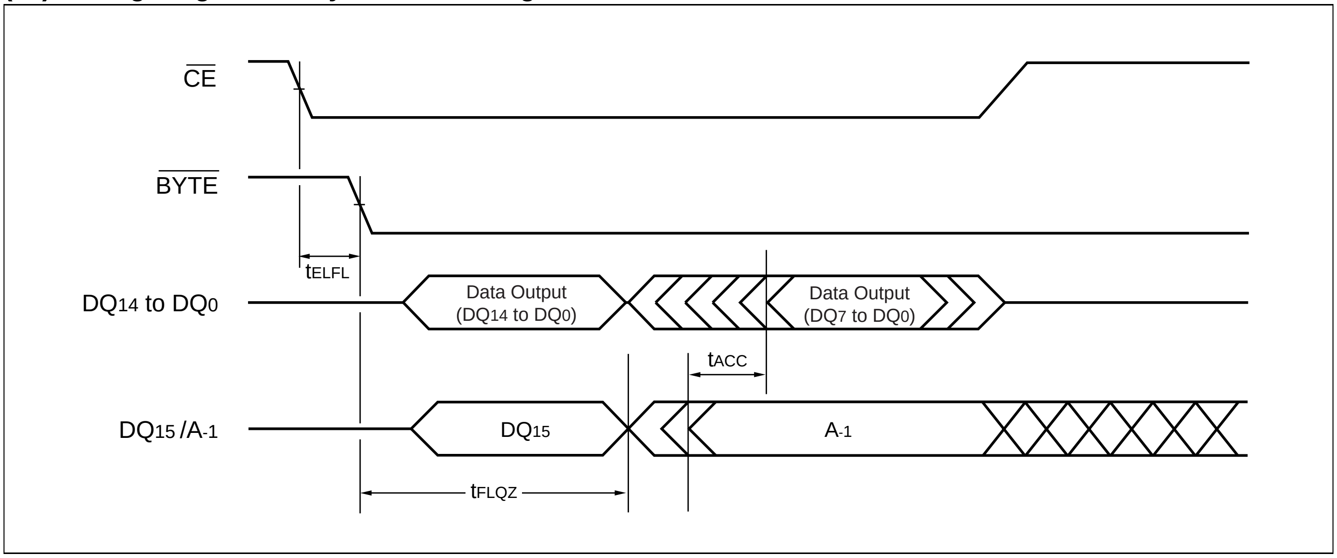
(9) $\overline{\text{RESET}}$/RY/$\overline{\text{BY}}$ Timing Diagram



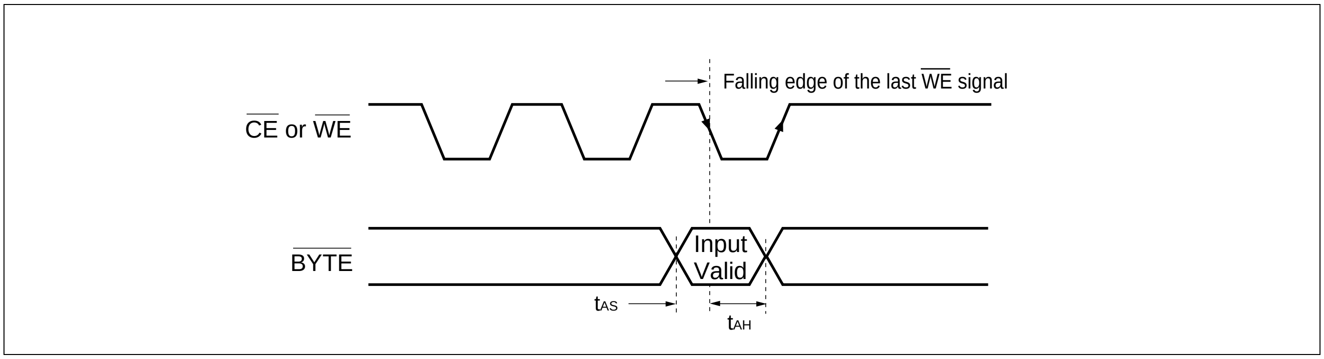
(10) Timing Diagram for Word Mode Configuration



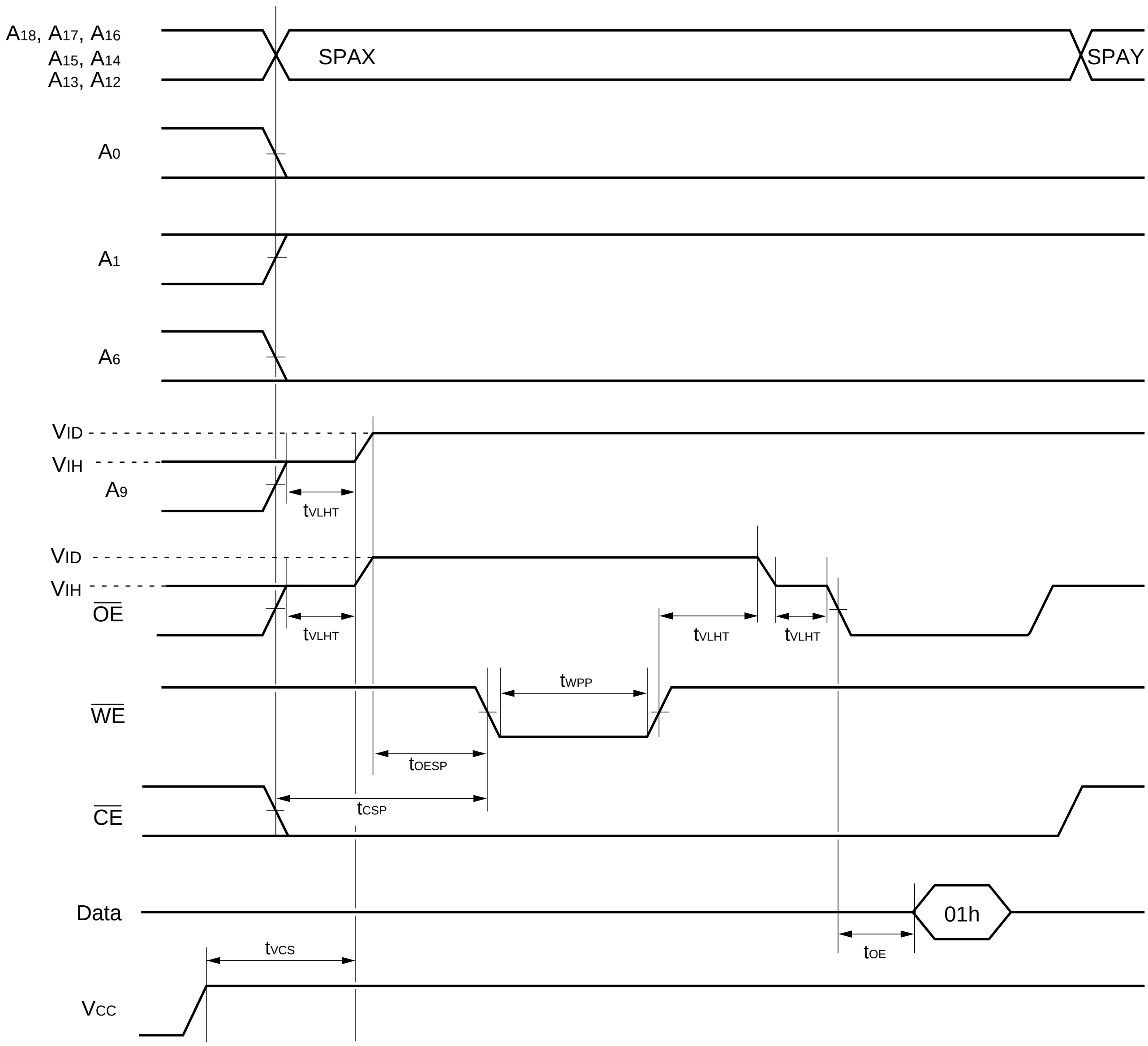
(11) Timing Diagram for Byte Mode Configuration



(12) BYTE Timing Diagram for Write Operations

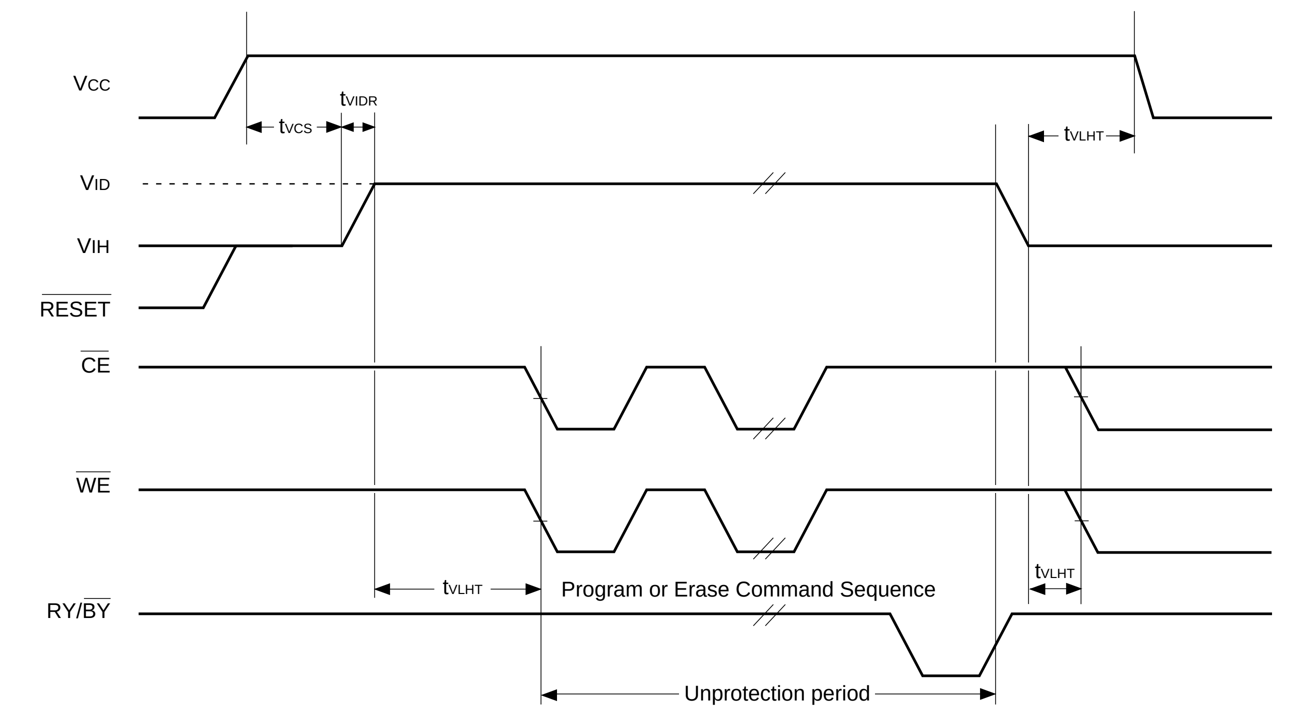


(13) AC Waveforms for Sector Protection

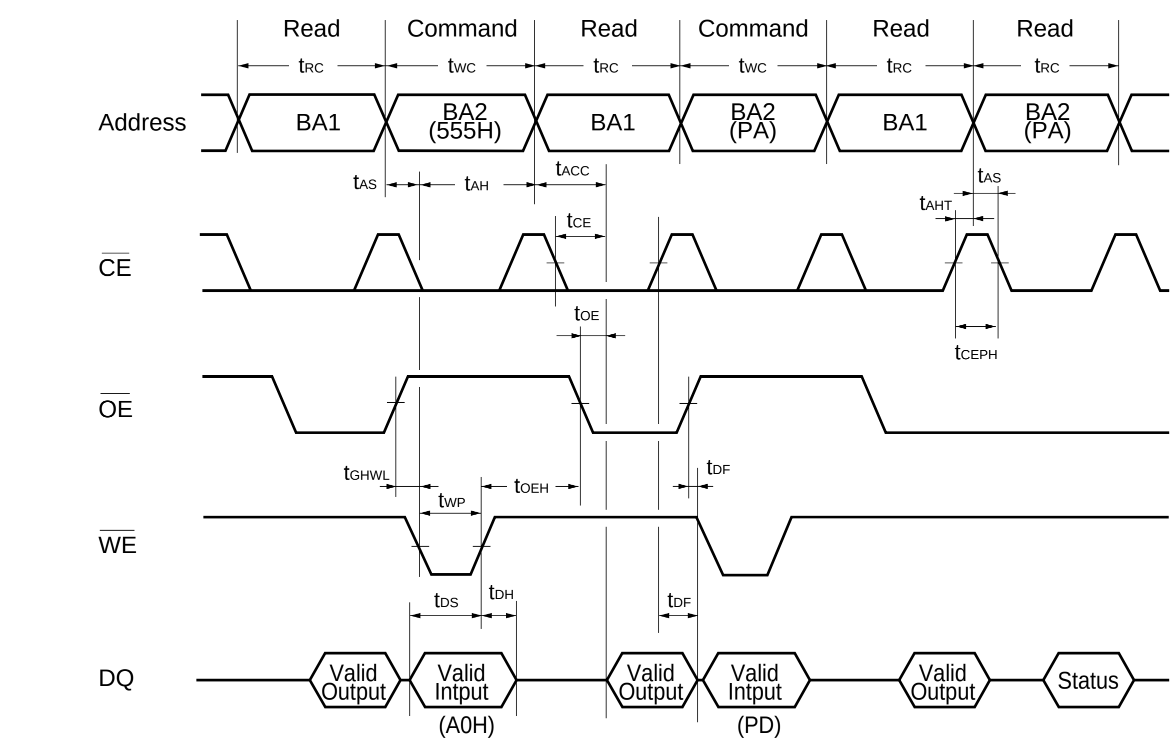


SPAX: Sector Address for initial sector
SPAY: Sector Address for next sector
Note : A_{-1} is V_{IL} on byte mode.

(14) Temporary Sector Unprotection Timing Diagram

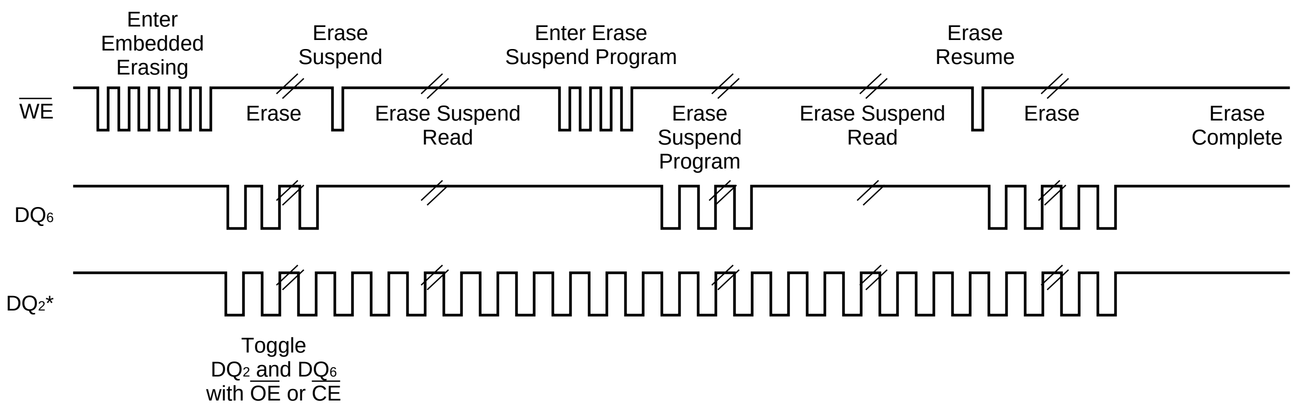


(15) Bank-to-bank Read/Write Timing Diagram



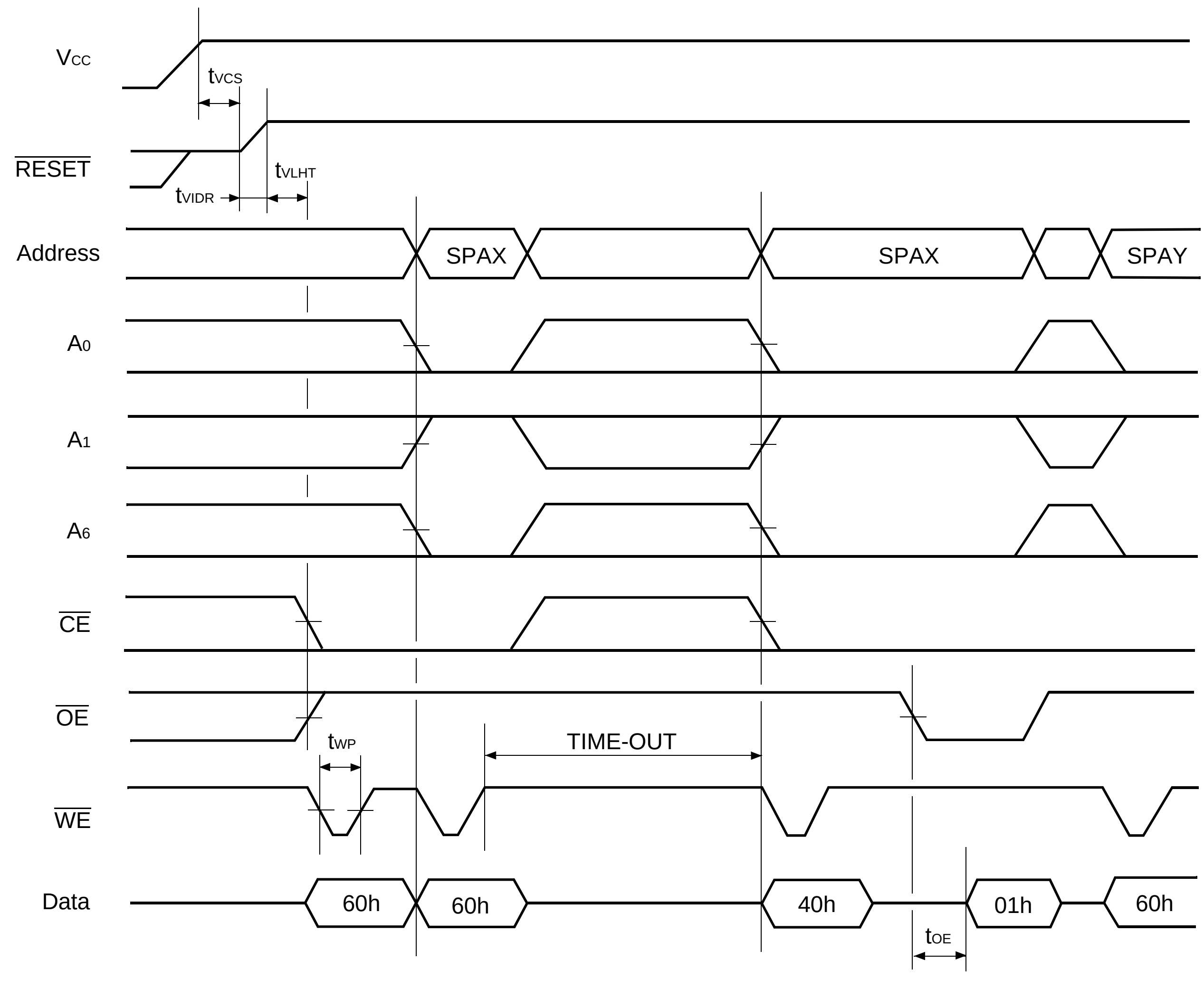
Note : This is example of Read for Bank 1 and Embedded Algorithm (program) for Bank 2.
BA1: Address corresponding of Bank 1.
BA2: Address corresponding of Bank 2.

(16) DQ_2 vs. DQ_6



* : DQ_2 is read from the erase-suspended sector.

(17) Extended Sector Protection Timing Diagram

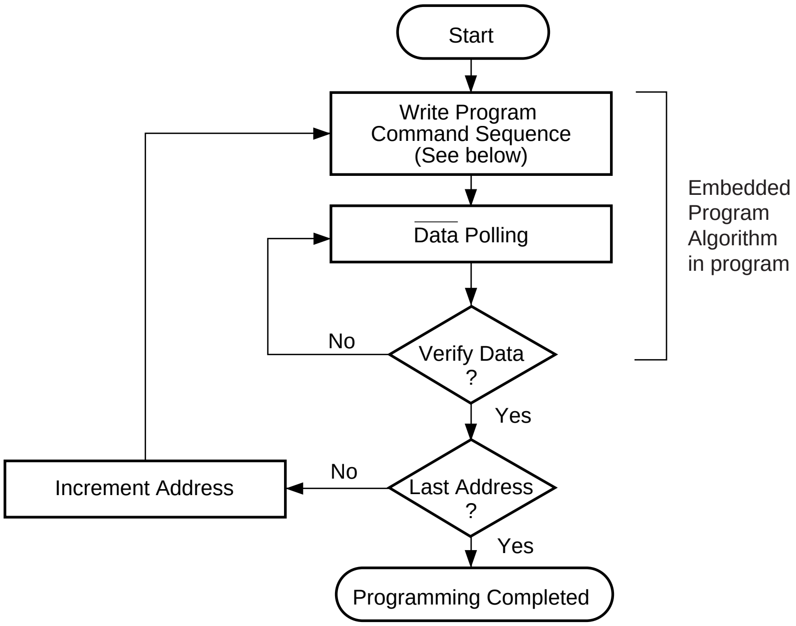


SPAX : Sector Address to be protected
SPAY : Next Sector Address to be protected
TIME-OUT : Time-Out window = 250 µs (Min)

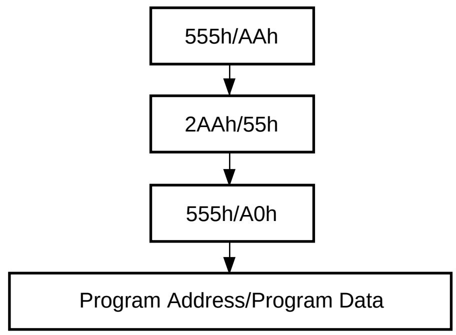
■ FLOW CHART

(1) Embedded Program™ Algorithm

EMBEDDED ALGORITHM



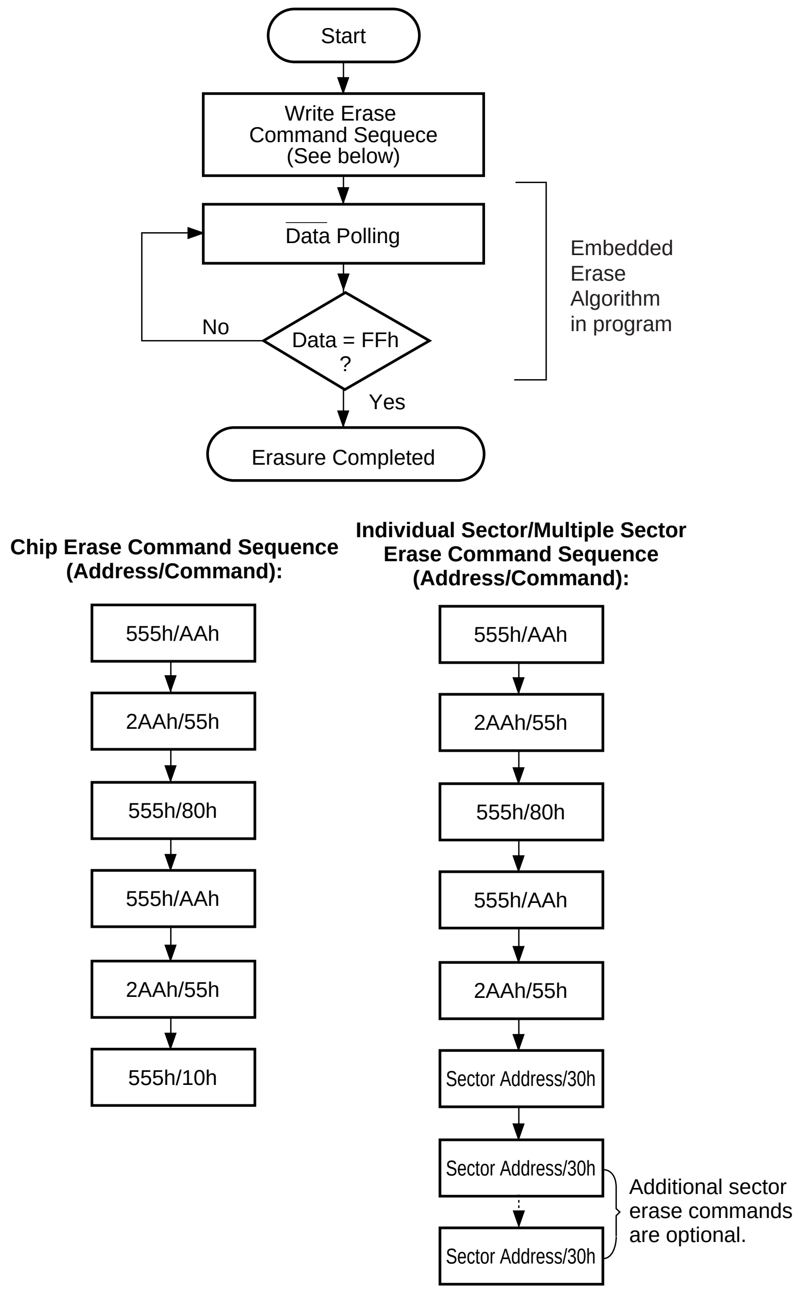
Program Command Sequence (Address/Command):



Notes : • The sequence is applied for × 16 mode.
• The addresses differ from × 8 mode.

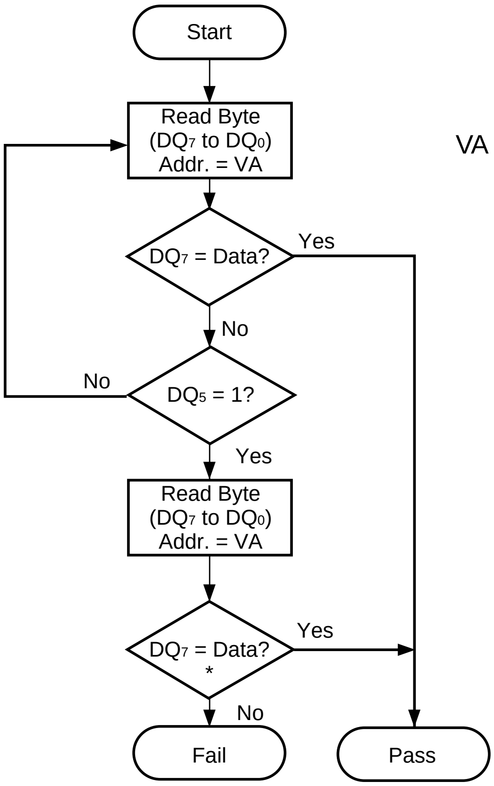
(2) Embedded Erase™ Algorithm

EMBEDDED ALGORITHM



Notes :
- The sequence is applied for × 16 mode.
- The addresses differ from × 8 mode.

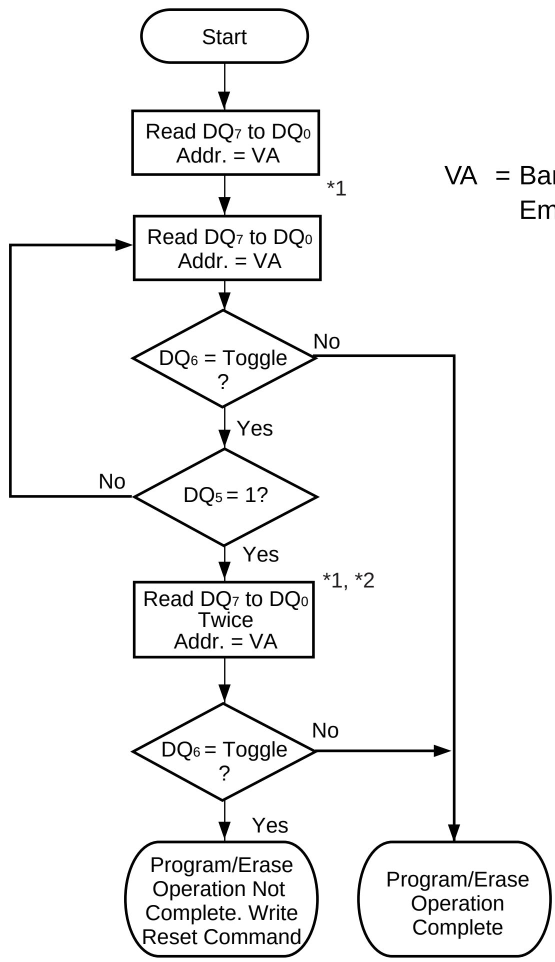
(3) $\overline{\text{Data}}$ Polling Algorithm



VA = Byte address for programming
= Any of the sector addresses within the sector being erased during sector erase or multiple sector erases operation
= Any of the sector addresses within the sector not being protected during chip erase operation

* : DQ_7 is rechecked even if DQ_5 = "1" because DQ_7 may change simultaneously with DQ_5.

(4) Toggle Bit Algorithm

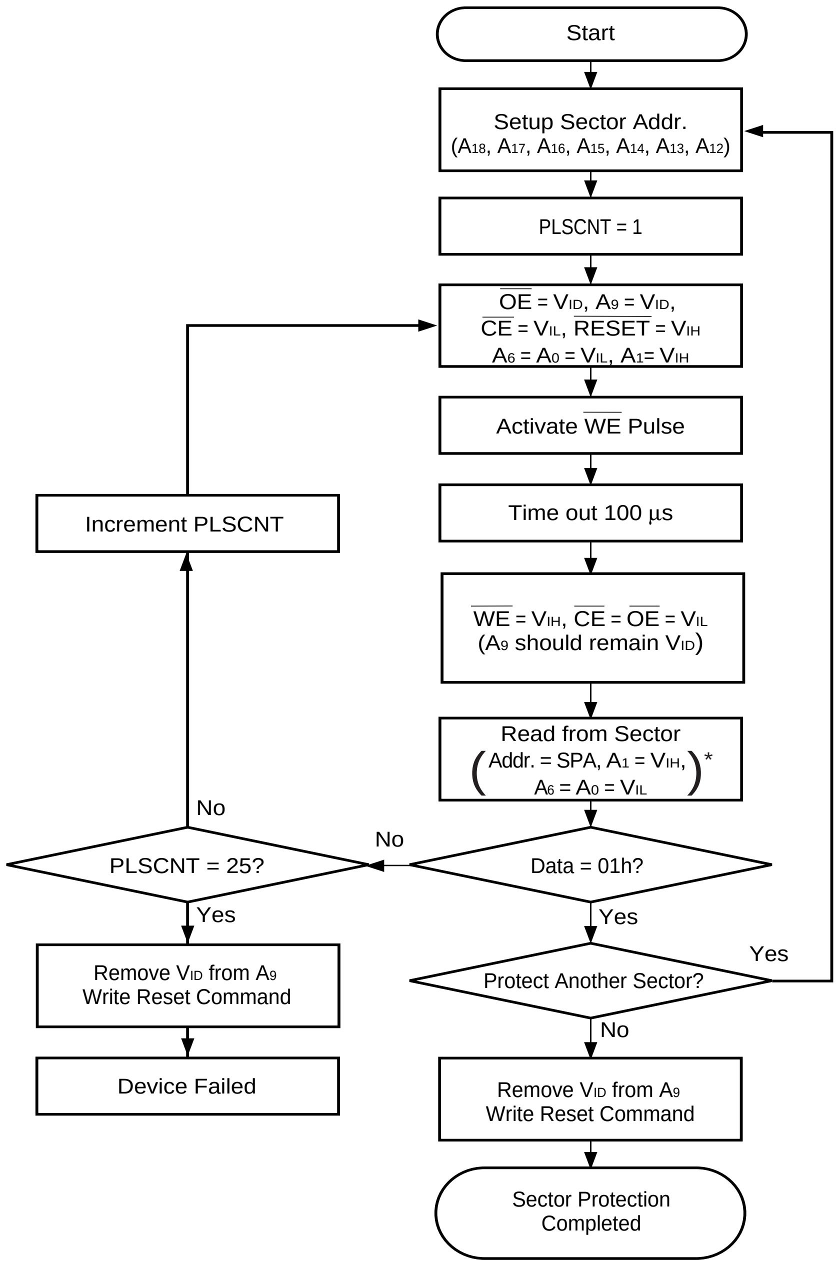


VA = Bank address being executed Embedded Algorithm.

*1 : Read toggle bit twice to determine whether it is toggling.

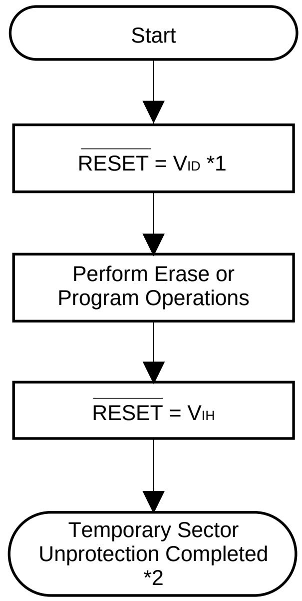
*2 : Recheck toggle bit because it may stop toggling as DQ_5 changes to “1”.

(5) Sector Protection Algorithm



* : A_{-1} is V_{IL} on byte mode.

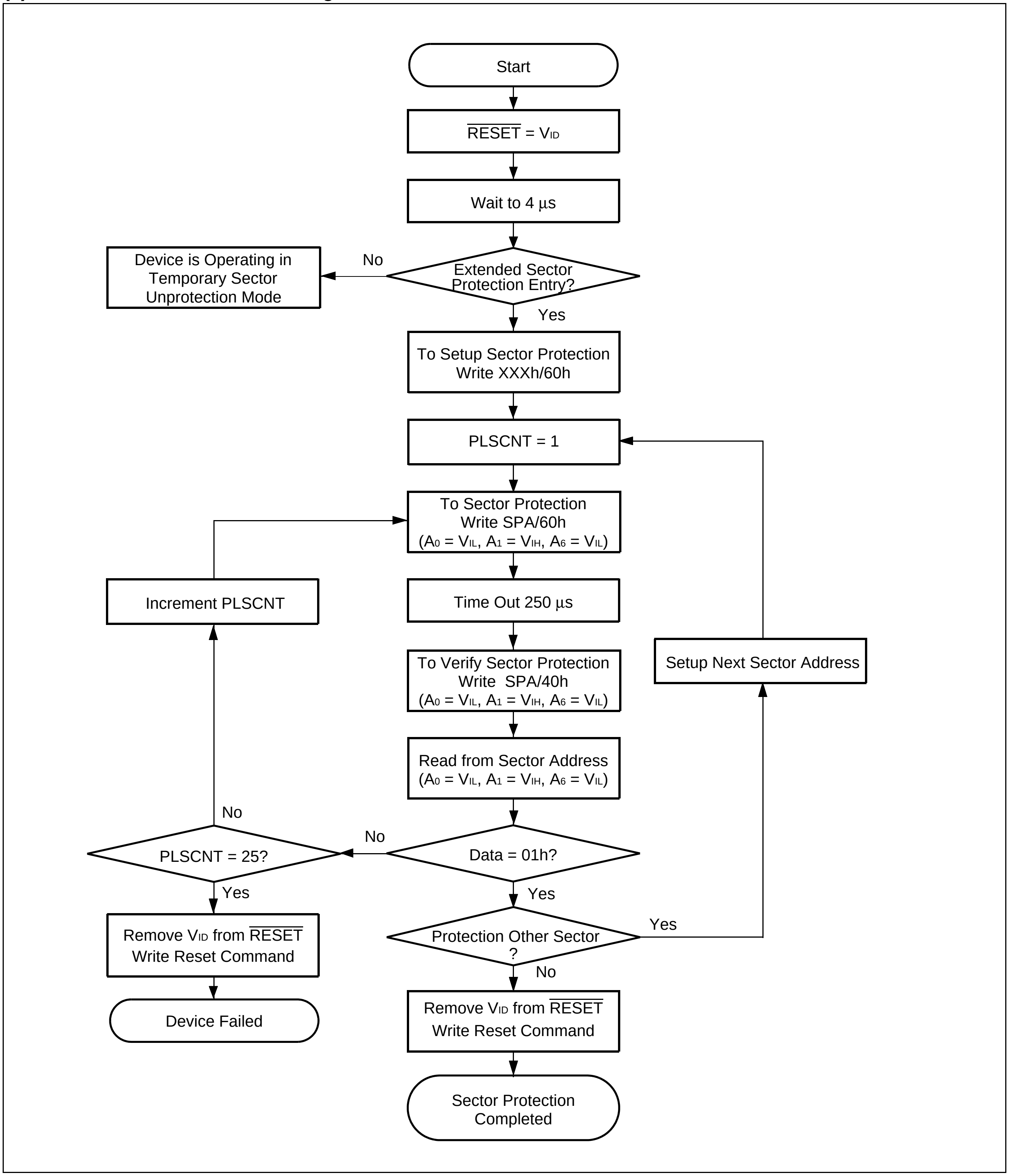
(6) Temporary Sector Unprotection Algorithm



*1 : All protected sectors are unprotected.

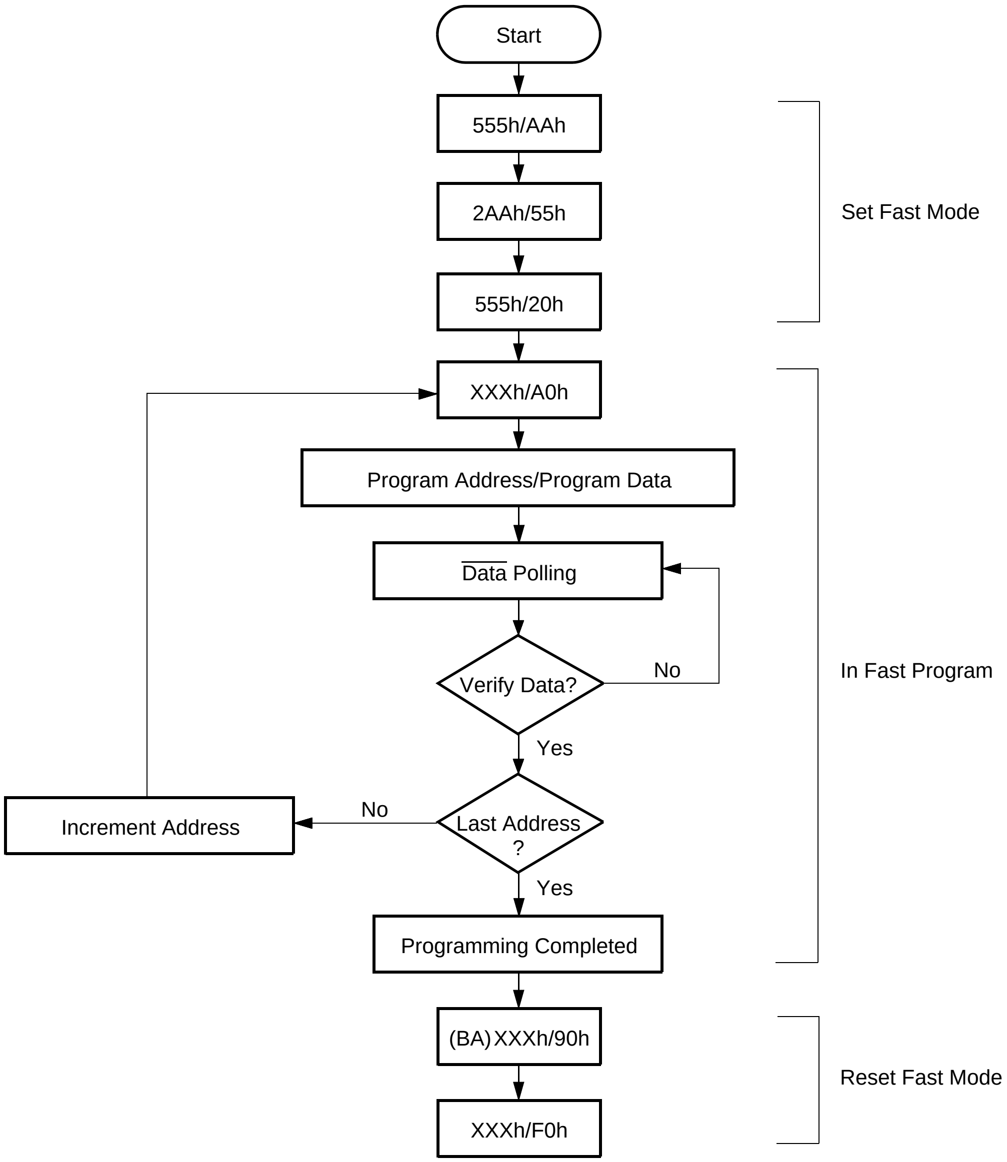
*2 : All previously protected sectors are protected once again.

(7) Extended Sector Protection Algorithm



(8) Embedded Program™ Algorithm for Fast Mode

FAST MODE ALGORITHM



Notes : • The sequence is applied for × 16 mode.
• The addresses differ from × 8 mode.

■ ORDERING INFORMATION

Part No.	Package	Access Time	Sector Architecture
MBM29DL800TA-70PFTN MBM29DL800TA-90PFTN	48-pin plastic TSOP (1) (FPT-48P-M19) (Normal Bend)	70 90	Top Sector
MBM29DL800TA-70PFTR MBM29DL800TA-90PFTR	48-pin plastic TSOP (1) (FPT-48P-M20) (Reverse Bend)	70 90	
MBM29DL800TA-70PBT MBM29DL800TA-90PBT	48-pin plastic FBGA (BGA-48P-M12)	70 90	
MBM29DL800BA-70PFTN MBM29DL800BA-90PFTN	48-pin plastic TSOP (1) (FPT-48P-M19) (Normal Bend)	70 90	Bottom Sector
MBM29DL800BA-70PFTR MBM29DL800BA-90PFTR	48-pin plastic TSOP (1) (FPT-48P-M20) (Reverse Bend)	70 90	
MBM29DL800BA-70PBT MBM29DL800BA-90PBT	48-pin plastic FBGA (BGA-48P-M12)	70 90	

MBM29DL800 T A -70 PFTN

PACKAGE TYPE
PFTN = 48-Pin Thin Small Outline Package (TSOP) Normal Bend
PFTR = 48-Pin Thin Small Outline Package (TSOP) Reverse Bend
PBT-SF2 =48-Ball Fine Pitch Ball Grid Array Package (FBGA:BGA-48P-M12)

SPEED OPTION
See Product Selector Guide.

Device Revision

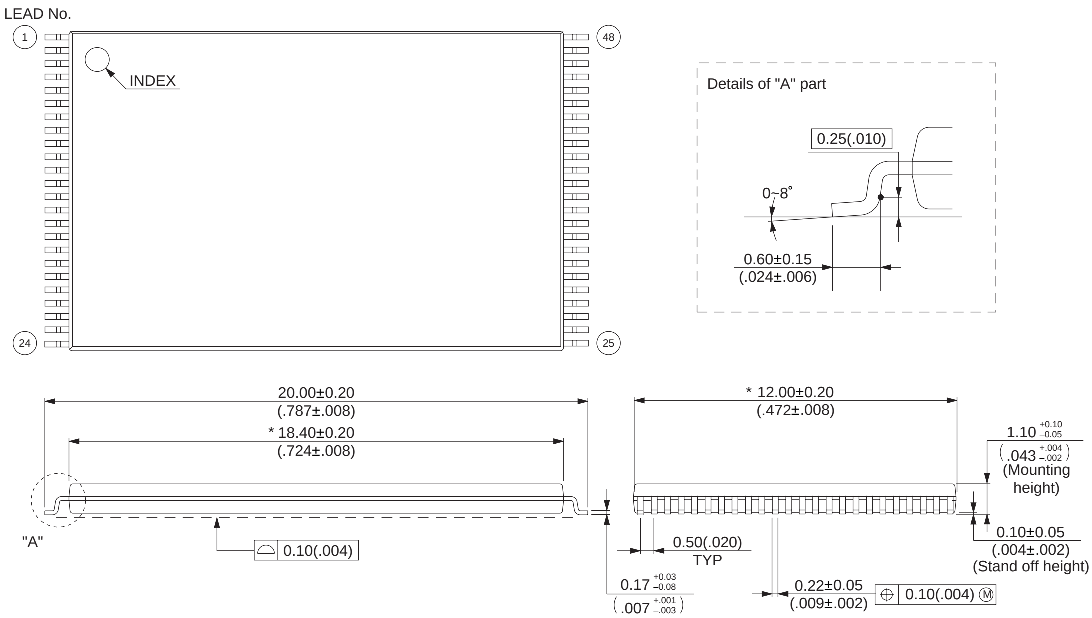
BOOT CODE SECTOR ARCHITECTURE
T = Top sector
B = Bottom sector

DEVICE NUMBER/DESCRIPTION
MBM29DL800
8Mega-bit (1M × 8-Bit or 512 K × 16-Bit) CMOS Flash Memory
3.0 V-only Read, Program, and Erase

■ PACKAGE DIMENSIONS

48-pin plastic TSOP (1)
(FPT-48P-M19)

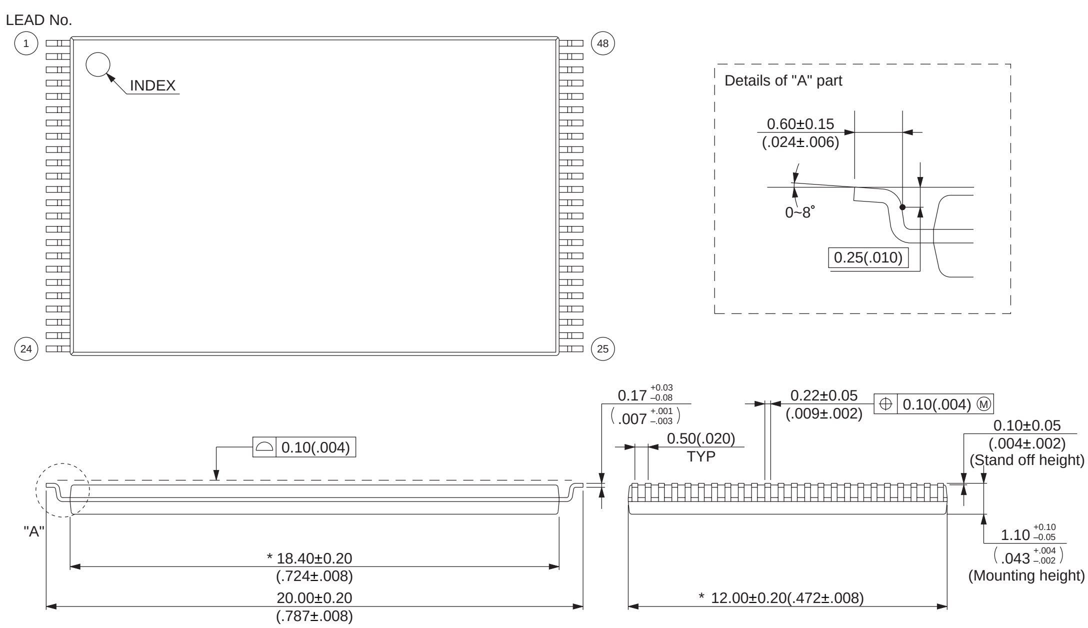
Note1 : * : Values do not include resin protrusion.
Resin protrusion and gate protrusion are +0.15 (.006) Max (each side) .
Note2 : Pins width and pins thickness include plating thickness.



Dimensions in mm (inches)

48-pin plastic TSOP (1)
(FPT-48P-M20)

Note1 : * : Values do not include resin protrusion.
Resin protrusion and gate protrusion are +0.15 (.006) Max (each side) .
Note2 : Pins width and pins thickness include plating thickness.

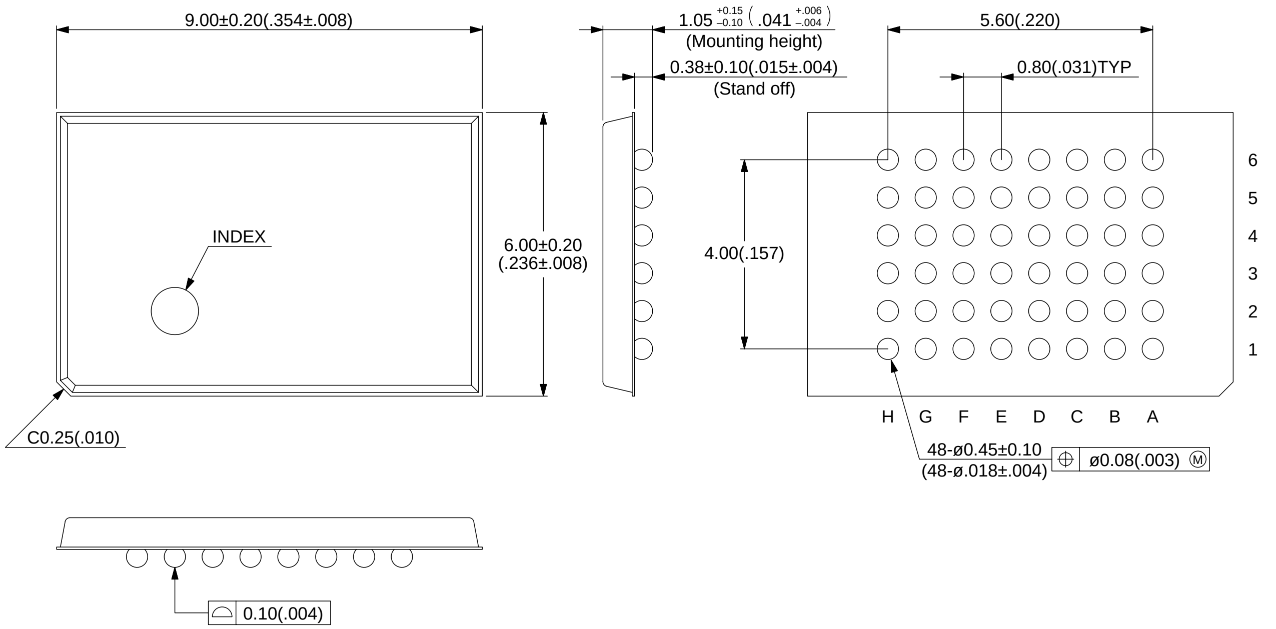


Dimensions in mm (inches)

(Continued)

(Continued)

48-pin plastic FBGA
(BGA-48P-M12)



Dimensions in mm (inches)

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