

16-Bit Stereo Audio Codec

Features

- CMOS Stereo Audio Input/Output System
 - Delta-Sigma A/D Converters
 - Delta-Sigma D/A Converters
 - Input Anti-Aliasing and Output Smoothing Filters
 - Programmable Input Gain and Output Attenuation
- Sample Frequencies of 4 kHz to 50 kHz
- CD Quality Noise and Distortion < 0.01 %THD
- Internal 64X Oversampling
- Low Power Dissipation: 80 mA
1 mA Power-Down Mode

General Description



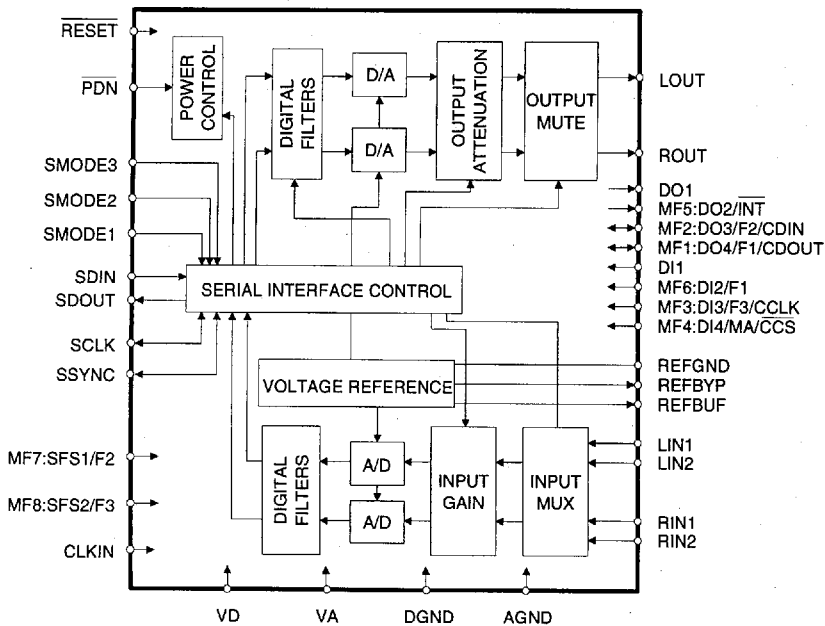
The CS4216 is an Mwave™ audio codec.

The CS4216 Stereo Audio Codec is a monolithic CMOS device for computer multimedia, automotive, and portable audio applications. It performs A/D and D/A conversion, filtering, and level setting, creating 4 audio inputs and 2 audio outputs for a digital computer system. The digital interfaces of left and right channels are multiplexed into a single serial data bus with word rates up to 50 kHz per channel. Up to 4 CS4216 devices can be attached to a single hardware bus.

Both the ADCs and the DACs use delta-sigma modulation with 64X oversampling. The ADCs include a digital decimation filter which eliminates the need for external anti-aliasing filters. The DACs include output smoothing filters on-chip.

Ordering Information:

CS4216-KL	0° to 70°C	44-pin PLCC
CS4216-KQ	0° to 70°C	44-pin TQFP
CDB4216		Evaluation Board



RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter	Symbol	Min	Typ	Max	Units	
Power Supplies:	Digital	VD	4.75	5.0	5.25	V
	Analog	VA	4.75	5.0	5.25	V
Operating Ambient Temperature	TA	0	25	70	°C	

ANALOG CHARACTERISTICS (TA = 25°C; VA, VD = +5V; Input Levels: Logic 0 = 0V, Logic 1 = VD; 1 kHz Input Sine Wave; CLKIN = 24.576 MHz; SM1; Conversion Rate = 48 kHz; SCLK = 12.288 MHz; Measurement Bandwidth is 10 Hz to 20 kHz; Unless otherwise specified.)

Parameter *	Symbol	Min	Typ	Max	Units
Analog Input Characteristics - Minimum gain setting (0 dB); unless otherwise specified.					
ADC Resolution		16	-	-	Bits
ADC Differential Nonlinearity (Note 1)		-	-	±0.9	LSB
Instantaneous Dynamic Range	IDR	80	85	-	dB
Total Harmonic Distortion	THD	-	-	0.01	%
Interchannel Isolation		-	80	-	dB
Interchannel Gain Mismatch		-	-	±0.5	dB
Frequency Response (Note 1)		-0.5	-	+0.2	dB
Programmable Input Gain Span		21	22.5	24	dB
Gain Step Size		-	1.5	-	dB
Absolute Gain Step Error		-	-	0.75	dB
Gain Drift		-	100	-	ppm/°C
Offset Error	DC Coupled Inputs	-	±10	±100	LSB
	AC Coupled Inputs	-	±150	±400	LSB
Full Scale Input Voltage		2.5	2.8	3.1	V _{pp}
Input Resistance (Notes 1,2)		20	-	-	kΩ
Input Capacitance (Note 1)		-	-	15	pF

- Notes: 1. This specification is guaranteed by characterization, not production testing.
 2. Input resistance is for the input selected. Non-selected inputs have a very high (>1MΩ) input resistance.

* Parameter definitions are given at the end of this data sheet.

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Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter *	Symbol	Min	Typ	Max	Units
Analog Output Characteristics - Minimum Attenuation; Unless Otherwise Specified.					
DAC Resolution		16	-	-	Bits
DAC Differential Nonlinearity (Note 1)		-	-	±0.9	LSB
Total Dynamic Range	TDR	-	93	-	dB
Instantaneous Dynamic Range	IDR	80	83	-	dB
Total Harmonic Distortion (Note 4)	THD	-	-	0.02	%
Interchannel Isolation (Note 4)		-	80	-	dB
Interchannel Gain Mismatch		-	-	±0.5	dB
Frequency Response (Note 1)		-0.5	-	+0.2	dB
Programmable Output Attenuation Span (Note 3)		-45	-46.5	-	dB
Attenuation Step Size (Note 3)		-	1.5	-	dB
Absolute Attenuation Step Error (Note 3)		-	-	0.75	dB
Gain Drift		-	100	-	ppm/°C
REFBUF Output Voltage (Note 5) Maximum output current= 400 µA		1.9	2.2	2.5	V
Offset Voltage		-	10	-	mV
Full Scale Output Voltage (Note 4)		2.5	2.8	3.1	V _{pp}
Deviation from Linear Phase (Note 1)		-	-	1	Degree
Out of Band Energy (22 kHz to 100 kHz)		-	-60	-	dB
Power Supply					
Power Supply Current (Note 6)	Operating	-	80	100	mA
	Power Down	-	-	1	mA
Power Supply Rejection (1 kHz)		-	40	-	dB

Notes: 3. Tested in SM3, Slave sub-mode, 128 BPF.

4. 10 kΩ, 100 pF load.

5. REFBUF load current must be DC. To drive dynamic loads, REFBUF must be buffered. AC variations in REFBUF current may degrade ADC and DAC performance.

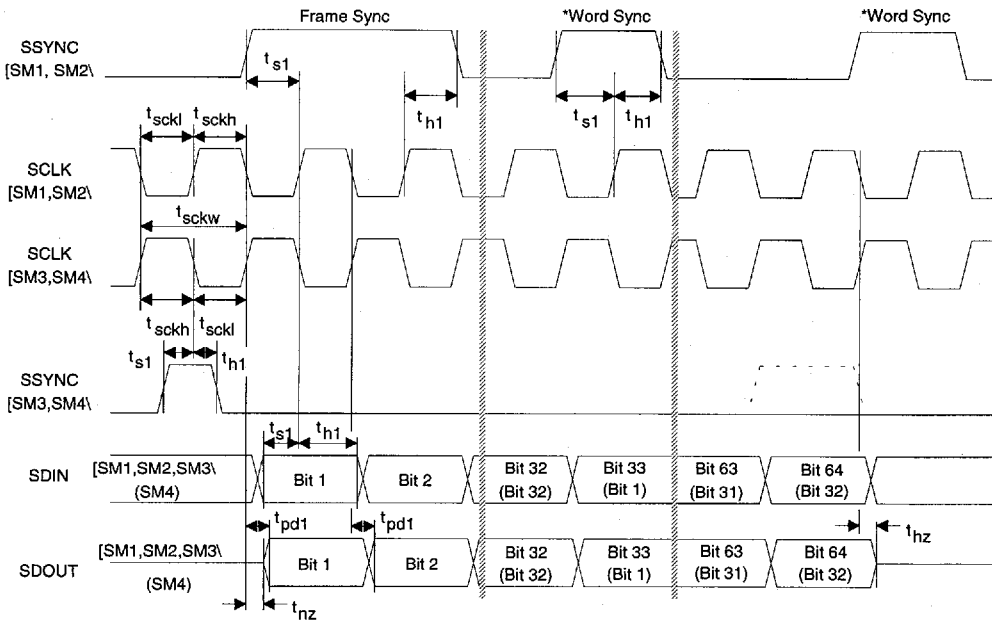
6. Typically current: VA = 30mA, VD = 50mA. Power supply current does not include output loading.

* Parameter definitions are given at the end of this data sheet.

SWITCHING CHARACTERISTICS ($T_A = 25^\circ\text{C}$; $V_A, V_D = +5\text{V}$, outputs loaded with 30 pF; Input Levels: Logic 0 = 0V, Logic 1 = VD)

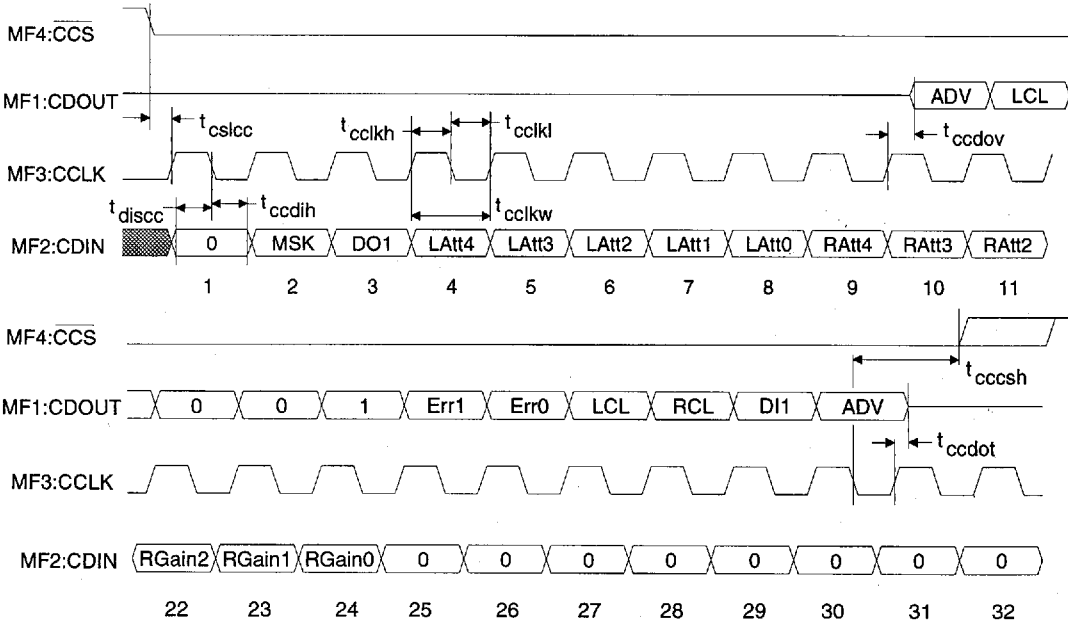
Parameter	Symbol	Min	Typ	Max	Units
Input clock (CLKIN) frequency	SM1: CLKIN	2.048	24.576	25.6	MHz
	SM2, SM3, SM4: CLKIN	1.024	12.288	12.8	MHz
CLKIN low time	t _{ckl}	15	-	-	ns
CLKIN high time	t _{ckh}	15	-	-	ns
Sample Rate	(Note 1) F _s	4	-	50	kHz
DI pins setup time to SCLK edge	(Note 1) t _{s2}	10	-	-	ns
DI pins hold time from SCLK edge	(Note 1) t _{h2}	8	-	-	ns
DO pins delay from SCLK edge	t _{pd2}	30	-	-	ns
SCLK and SSYNC output delay from CLKIN rising	Master Mode (Note 1) t _{pd3}	-	-	50	ns
SCLK period	Master Mode (Note 7) t _{sckw}	-	1/(F _s *bpf)	-	s
	Slave Mode	75	-	-	ns
SCLK high time	Slave Mode t _{sckh}	30	-	-	ns
SCLK low time	Slave Mode t _{sckl}	30	-	-	ns
SDIN, SSYNC setup time to SCLK edge	Slave Mode t _{s1}	15	-	-	ns
SDIN, SSYNC hold time from SCLK edge	Slave Mode t _{h1}	10	-	-	ns
SDOUT delay from SCLK edge	t _{pd1}	-	-	28	ns
Output to Hi-Z state	bit 64 (Note 1) t _{hz}	-	-	12	ns
Output to non-Hi-Z	bit 1 (Note 1) t _{nz}	15	-	-	ns
RESET pulse width low		500	-	-	ns
CCS low to CCLK rising	SM4 (Note 1) t _{cslcc}	25	-	-	ns
CDIN setup to CCLK falling	SM4 (Note 1) t _{disc}	15	-	-	ns
CCLK low to CDIN invalid (hold time)	SM4 (Note 1) t _{ccdi}	10	-	-	ns
CCLK high time	SM4 (Note 1) t _{cchh}	25	-	-	ns
CCLK low time	SM4 (Note 1) t _{cchl}	25	-	-	ns
CCLK Period	SM4 (Note 1) t _{cclk}	75	-	-	ns
CCLK rising to CDOOUT data valid	SM4 (Note 1) t _{ccdov}	-	-	30	ns
CCLK rising to CDOOUT Hi-Z	SM4 (Note 1) t _{ccdot}	-	-	30	ns
CCLK falling to CCS high	SM4 (Note 1) t _{ccsh}	0	-	-	ns

Notes: 7. When the CS4216 is in master mode (SSYNC and SCLK outputs), the SCLK duty cycle is 50%.
The equation is based on the selected sample frequency (F_s) and the number of bits per frame (bpf).

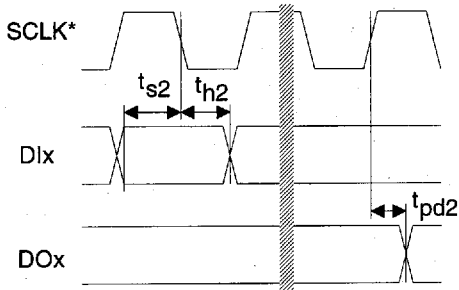


* Optional

Serial Audio Port Timing

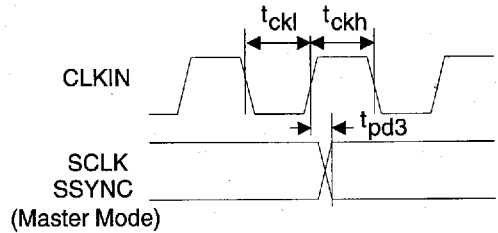


Serial Mode 4. Control Data Serial Port Timing



* SCLK is inverted for SM1 and SM2

DI/DO Timing



(Master Mode)

SCLK & SSYNC Output Timing (Master Mode)

DIGITAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$; $V_A, V_D = 5\text{V}$)

Parameter	Symbol	Min	Typ	Max	Units
High-level Input Voltage	V_{IH}	VD-1.0	-	-	V
Low-level Input Voltage	V_{IL}	-	-	1.0	V
High-level Output Voltage at $I_O = -2.0\text{ mA}$	V_{OH}	VD-0.3	-	-	V
Low-level Output Voltage at $I_O = +2.0\text{ mA}$	V_{OL}	-	-	0.1	V
Input Leakage Current (Digital Inputs)		-	-	10	μA
Output Leakage Current (High-Z Digital Outputs)		-	-	10	μA
Output Capacitance	C_{OUT}	-	-	15	pF
Input Capacitance	C_{IN}	-	-	15	pF

A/D Decimation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.2	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		80	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.0	µs

4

D/A Interpolation Filter Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Passband (Fs is conversion freq.)		0	-	0.45Fs	Hz
Frequency Response		-0.5	-	+0.2	dB
Passband Ripple		-	-	±0.1	dB
Transition Band		0.45Fs	-	0.55Fs	Hz
Stop Band		≥ 0.55Fs	-	-	Hz
Stop Band Rejection		74	-	-	dB
Group Delay		-	16/Fs	-	s
Group Delay Variation vs. Frequency		-	-	0.1/Fs	µs

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to 0V.)

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies: Digital	VD	-0.3	-	6.0	V
Power Supplies: Analog	VA	-0.3	-	6.0	V
Input Current (Except Supply Pins)		-	-	±10.0	mA
Analog Input Voltage		-0.3	-	VA+0.3	V
Digital Input Voltage		-0.3	-	VD+0.3	V
Ambient Temperature (Power Applied)		-55	-	+125	°C
Storage Temperature		-65	-	+150	°C

Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

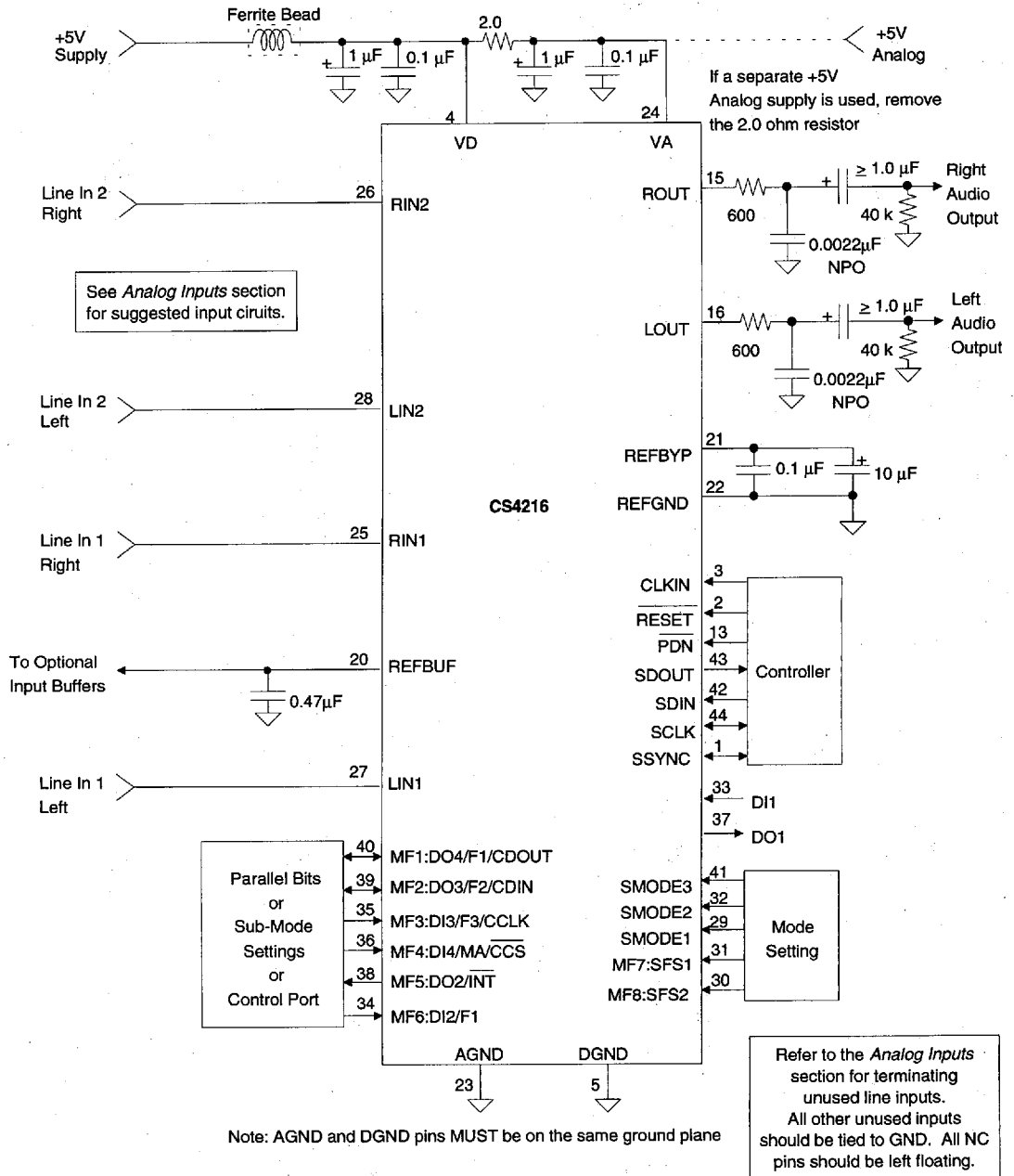


Figure 1. Typical Connection Diagram

OVERVIEW

The CS4216 contains two analog-to-digital converters, two digital-to-analog converters, adjustable input gain, and adjustable output level control. Since the converters contain all the required filters in digital or sampled analog form, the filters' frequency responses track the sample rate of the CS4216. Only a single-pole RC filter is required on the analog inputs and outputs. The RC filter acts as a charge reserve for the switched-capacitor input and buffers op-amps from a switched-capacitor load. Communication with the CS4216 is via a serial port, with separate pins for data into the device, and data from the device. The filters and converters operate over a sample rate range of 4 kHz to 50 kHz.

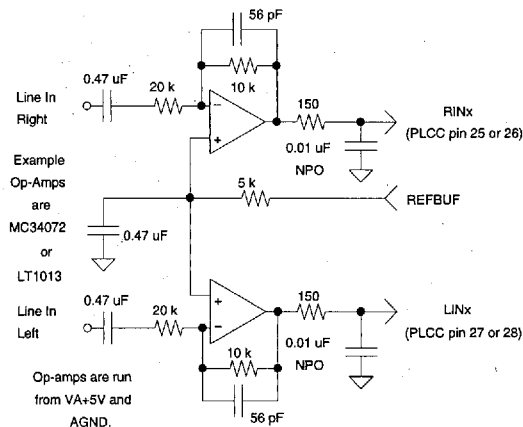


Figure 2. DC Coupled Input.

FUNCTIONAL SPECIFICATIONS

Analog Inputs and Outputs

Figure 1 illustrates the suggested connection diagram to obtain full performance from the CS4216. The line level inputs, LIN1 or LIN2 and RIN1 or RIN2, are selected by an internal input multiplexer. This multiplexer is a source selector and is not designed for switching between inputs at the sample rate.

Unused analog inputs that are not selected have a very high input impedance, so they may be tied to AGND directly. Unused analog inputs that are selected should be tied to AGND through a 0.1 μ F capacitor. This prevents any DC current flow.

The analog inputs are single-ended and internally biased to the REFBUF voltage (nominally 2.2 V). The REFBUF output pin can be used to level shift an input signal centered around 0 Volts as shown in Figure 2. The input buffers shown have a gain of 0.5, yielding a full scale input sensitivity of 2 V_{rms} with the CS4216 pro-

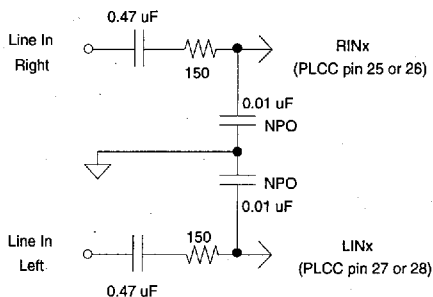


Figure 3. AC Coupled Input

grammable gain set to 0. If the source impedance is very low, then the inputs can be AC coupled with a series 0.47 μ F capacitor, eliminating the need for external op-amps (see Figure 3). However, the use of AC coupling capacitors will increase DC offset at 0dB gain (see Analog Characteristics Table).

The analog outputs are also single-ended and centered around the REFBUF pin. AC coupling capacitors of $>1 \mu$ F are recommended.

Offset Calibration

Both input and output offset voltages are minimized by internal calibration. Offset calibration occurs after exiting a reset or power down condition. During calibration, which takes 194 frames, output data from the ADCs will be all zeros, and will be flagged as invalid. Also, the DAC outputs will be muted. After power down mode or power up, **RESET** should be held low for a minimum of 50 ms to allow the voltage reference to settle.

Input Gain and Output Level Setting

Input gain is adjustable from 0 dB to +22.5 dB in 1.5 dB steps. In serial modes SM1 and SM2, the output level attenuation is adjustable from 0 dB to -22.5 dB. In serial modes SM3 and SM4, the output level attenuation is adjustable from 0 dB to -46.5 dB. Both input and output gain adjustments are internally made on zero-crossings of the analog signal, to minimize "zipper" noise. The gain change automatically takes effect if a zero crossing does not occur within 512 frames.

Muting and the ADC Valid Counter

The mute function allows the output channels to be silenced. It is the controlling processor's responsibility to reduce the signal level to a low value before muting, to avoid an audible click. The outputs should be muted before changing the sample frequency.

The serial data stream contains a "Valid Data" indicator for the A/D converters which is false until enough clocks have passed since reset, or low-power (power down mode) operation to have valid A/D data from the filters, i.e., until calibration time plus the full latency of the digital filters has passed.

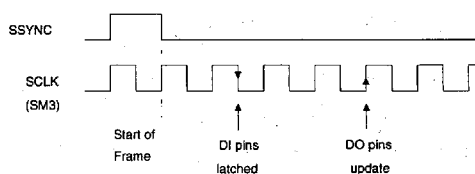


Figure 4. Digital Input/Output Timing

Parallel Digital Input/Output Pins

Parallel digital inputs are general purpose pins whose value is reflected in the serial data output stream to the processor. Parallel digital outputs provide a way to control external devices using bits in the serial data input stream. All parallel digital pins, with the exception of DI1 and DO1, are multifunction and are defined by the serial mode selected. Serial modes 1 and 2 define all multifunction pins as general purpose digital inputs and outputs. In Serial mode 3 only two digital inputs and two digital outputs are available. In serial mode 4 only one digital input and digital output exists. Figure 4 shows when the DI pins are latched, and when the DO pins are updated in SM3 and SM4.

Reset and Power Down Modes

Reset places the CS4216 into a known state and must be held low for at least 50 ms after power-up or a hard power down. Reset must also occur when the codec is in master mode and a change in sample frequency is desired. In reset, the digital outputs are driven low. Reset sets all control data register bits to zero.

Hard power down mode may be initiated by bringing the PDN pin low. All analog outputs will be driven to the REFBUF voltage which will then decay to zero. All digital outputs will be driven low and then will go to a high impedance state. Minimum power consumption will occur if CLKIN is held low. After leaving the power down state, **RESET** should be held low for 50 ms to allow the analog voltage reference to settle before calibration is started.

Alternatively, soft power down may be initiated, in slave mode, by reducing the SCLK frequency below the minimum CLKIN/12. In soft power down the analog outputs are muted and the serial data from the codec will indicate invalid data and the appropriate error code. The parallel bit I/O is still functional in soft power down mode. This is, in effect, a low power mode with only the parallel bit I/O unit functioning.

Audio Serial Interface

In serial modes 1, 2, and 3, the audio serial port uses 4 pins: SDOUT, SDIN, SCLK and SSYNC. SDIN carries the D/A converters' input data and control bits. Input data is ignored for frames not allocated to the selected CS4216. SDOUT carries the A/D converters' output data and status bits. SDOUT goes to a high-impedance state during frames not allocated to the selected CS4216. SCLK clocks data in to and out of the CS4216. The rising edge of SCLK clocks data out on SDOUT. The falling edge latches data on SDIN into the port (SCLK polarity is inverted in Serial Modes 1&2). SSYNC indicates the start of a frame and/or sub-frame. SCLK and SSYNC must be synchronous to the master clock.

Serial mode 4 is similar to serial mode 3 with the exception of the control information. In serial mode 4 the control information is entered through a separate asynchronous control port. Therefore, the audio serial port only contains

audio data which reduces the number of bits on the audio port from 64 to 32 per codec.

The serial port protocol is based on frames consisting of 1, 2, or 4 sub-frames. The frame rate is the system sample rate. Each sub-frame is used by one CS4216 device. Up to 4 CS4216s may be attached to the same serial control lines. SFS1 and SFS2 are tied low or high to indicate to each CS4216 which sub-frame is allocated for it to use.

Serial Data Format

In serial modes 1, 2, and 3, a sub-frame is 64 bits in length and consists of two 16-bit audio values and two 16-bit control fields. In serial mode 4 a sub-frame is 32 bits in length and only contains the two 16-bit audio values; the control data is loaded through a separate port. The audio data is MSB first, 2's complement format. The sub-frame bit assignments for serial modes 1, 2, and 3, are numbered 1 through 64 and are shown in Figures 5 and 6. Control data bits all reset to zero.

CS4216 SERIAL INTERFACE MODES

The CS4216 has 4 serial port modes, selected by the SMODE1, SMODE2 and SMODE3 pins. In all modes, CLKIN, SCLK and SSYNC must be derived from the same clock source. SM1 is an easy interface to ASICs that use a change in the SCLK-to-CLKIN ratio to determine the sample

SMODE PINS			Serial Mode	SCLK Bit Center	Sub-frame Width	Bits per Frame (BPF)	SCLK & SSYNC	Master Frequency
3	2	1						
0	0	0	SM1	Rising	64 bits	256	Slave	CLKIN = 512×Fs
0	0	1	SM2	Rising	64 bits	256	Slave	SCLK = 256×Fs
0	1	0	SM3	Falling	64 bits	64/128/256	Master/Slave	CLKIN/SCLK = 256×Fs
0	1	1	Factory Test mode					
1	x	x	SM4	Falling	32 bits [†]	32/64/128 [†]	Master/Slave	CLKIN = 256×Fs

[†]Contains audio data only. Control information is entered through a separate serial port.

Table 1. Serial Port Modes

INPUT DATA BIT DEFINITIONS

Sub-frame bits 1 to 16

Left DAC Audio Data, MSB first, 2's complement coded.

Sub-frame Bits 17 to 24

17	18	19	20	21	22	23	24
0	0	0	0	EXP	MUTE	ISL	ISR

EXP Expand bit
Reserved. Must be set to zero.

MUTE Mute D/A Outputs
0 - Normal Outputs
1 - Mute Outputs

ISL Select Left Input Mux
0 - Select LIN1
1 - Select LIN2

ISR Select Right Input Mux
0 - Select RIN1
1 - Select RIN2

Sub-frame Bits 25 to 32

25	26	27	28	29	30	31	32
LG3	LG2	LG1	LG0	RG3	RG2	RG1	RG0

LG3-LG0 Sets left input gain.
LG3 is the MSB. LG0 represents 1.5 dB.
0000 = no gain.
1111 = +22.5 dB gain

RG3-RG0 Sets right input gain.
RG3 is the MSB. RGO represents 1.5 dB.
0000 = no gain

Sub-frame Bits 33 to 48

Right DAC audio data MSB first, 2's complement coded.

Sub-frame Bits 49 to 50

Must be zero.

Sub-frame Bits 51 to 60

51	52	53	54	55	56	57	58	59	60	
*LA4	LA3	LA2	LA1	LA0	RA4	RA3	RA2	RA1	RA0	
†	0	0	LA3	LA2	LA1	LA0	RA3	RA2	RA1	RA0

LA4-LA0 Sets left output attenuation

†SM1, 2	*SM3, 4
LA3 is the MSB. 0000 = no attenuation 1111 = -22.5 dB	LA4 is the MSB. 00000 = no attenuation 11111 = -46.5 dB
LA0 represents 1.5 dB.	

RA4-RA0 Sets right output attenuation

†SM1, 2	*SM3, 4
RA3 is the MSB. 0000 = no attenuation 1111 = -22.5 dB	RA4 is the MSB. 00000 = no attenuation 11111 = -46.5 dB
RA0 represents 1.5 dB.	

Sub-frame Bits 61 to 64

61	62	63	64
DO1	DO2	DO3	DO4

DO1-DO4 Set the logic level on the 4 digital output pins. In SM3 DO2 and DO4 are not available. In SM4 DO2, DO3, & DO4 are not available.

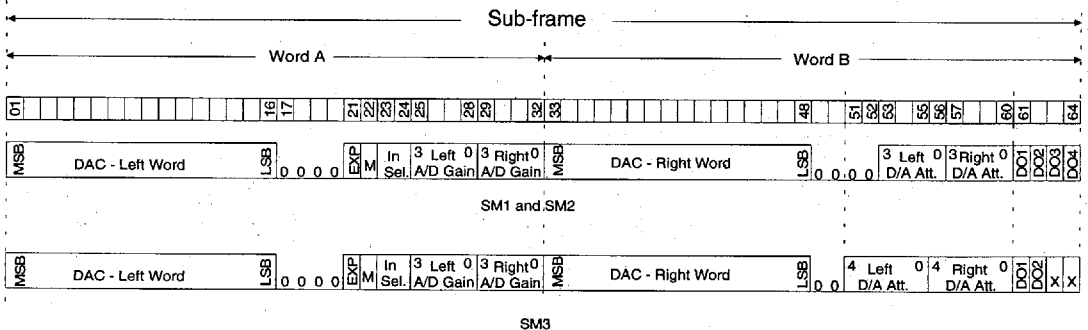


Figure 5. Serial Data Input Format - SM1, SM2, and SM3.

OUTPUT DATA BIT DEFINITIONS

Sub-frame Bits 1 to 16

Left ADC Audio Data, MSB first, 2's complement coded.

Sub-frame Bits 17 to 24

17	18	19	20	21	22	23	24
RESERVED				0	ADV	LCL	RCL

ADV ADC Valid data bit.
 0 - Invalid ADC data
 1 - Valid ADC data
 Indicates ADC has completed initialization after power-up, low power mode, or mute.

LCL Left ADC clipping indicator
 0 - Normal
 1 - Clipping

RCL Right ADC clipping indicator
 0 - Normal
 1 - Clipping

RESERVED bits can be 0 or 1

Sub-frame Bits 25 to 32

25	26	27	28	29	30	31	32
ER3	ER2	ER1	ER0	Ver3	Ver2	Ver1	Ver0

ER3-ER0 Error Word
 0000 - Normal - No errors.
 0001 - Input Sub-frame Bit 21 is set. Control data will not be loaded
 0010 - Sync Pulse is incorrect. Causes the analog output to mute.
 0011 - SCLK is outside the allowable range. Analog output mutes.

Ver3-Ver0 CS4216 Version Number
 0000 = "A" (see Appendix A)
 0001 = "B", "C", . . . (This data sheet)

Sub-frame Bits 33 to 48

Right ADC Audio Data, MSB first, 2's complement coded.

Sub-frame Bits 49 to 60

These bits are reserved, and can be 0 or 1.

Sub-frame Bits 61 to 64

61	62	63	64
DI1	DI2	DI3	DI4

DI1-DI4 These bits follow the state of the Digital Input pins. In SM3 DI3 and DI4 are used and unavailable. In SM4 DI2, DI3, & DI4 are not available as input bits.

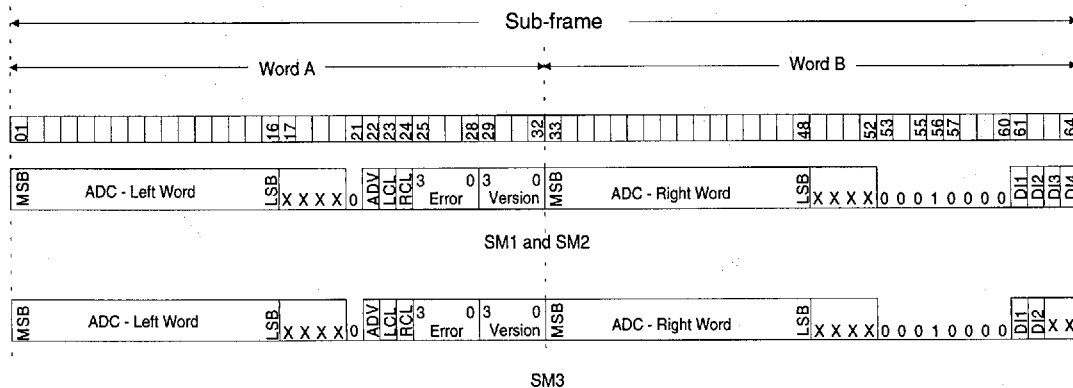


Figure 6. Serial Data Output Format - SM1, SM2, and SM3.

frequency. SM2 is similar to SM1 except that CLKIN is not used and SCLK becomes the master clock and is fixed at $256 \times F_s$. SM3 was designed as an easy interface to general purpose DSPs and provides extra features such as one more bit of attenuation, a master mode, and variable frame sizes. SM4 is similar to SM3 but splits the audio data from the control data thereby reducing the audio serial bus bandwidth by half. The control data is transmitted through a control serial port in SM4.

Table 1 lists the serial port modes available, along with some of the differences between modes. The first three columns in Table 1 select the serial mode. The "SCLK Bit Center" column indicates whether SCLK is rising or falling in the center of a bit period. The "Sub-frame Width" column indicates how many bits are in an individual codec's sub-frame. SM4 differs from all other modes by separating the control data from the audio data. In both SM1 and SM2, there are 256 bits per frame which allows up to four codecs to occupy the same bus. In SM3 and SM4, the number of bits per frame is programmable. In SM1 and SM2, SCLK and SSYNC must be generated externally; whereas, in SM3 and SM4 the CS4216 can optionally generate those signals. In all modes, SCLK and SSYNC must be synchronous to the master clock. The last column in Table 1 lists the master frequency used by the codec. In SM1, the master frequency, input on CLKIN, is 512 times the highest sample frequency available. In SM2, the master frequency is fixed at 256 times the sample frequency and, in this mode, SCLK is the master clock. In SM3, the master frequency is 256 times the highest frequency available and is input on CLKIN or SCLK, based on the sub-mode used. In SM4, the master frequency is also 256 times the highest frequency available and is input on CLKIN.

SERIAL MODE 1, SM1

Serial Mode 1 is a slave mode selected by setting $SMODE3 = SMODE2 = SMODE1 = 0$. SCLK and SYNC must be synchronous the master clock. SM1 uses a two bit wide (minimum) frame sync with an optional word sync. In this mode, SSYNC low for one SCLK period followed by SSYNC high for a minimum of two SCLK periods indicates the beginning of a frame. The first bit of the frame starts with the rising edge of SSYNC. An optional word sync, being one SCLK period high, may be used to indicate the start of a new 32-bit word. Figures 5 and 6 contain the serial data format for SM1. In this serial mode, the ratio of two clocks are used to select sample frequency. These are the master clock CLKIN and the serial clock SCLK. CLKIN should be set to $512 \times F_{smax}$, where F_{smax} is the maximum required sample rate. SCLK must be externally set to a value of $CLKIN/N$, such that SCLK equals 256 times the desired sample rate. The codec uses the ratio between CLKIN and SCLK to set the internal sample frequency and causes the CS4216 to go into soft power down mode if the SCLK frequency drops to $< CLKIN/12$. Even if only 1 CS4216 is used, the timing for 4 devices must be maintained. Table 2 shows some example sample rates for SM1.

Sample Rate kHz	SCLK MHz	CLKIN MHz	N
48	12.288	24.576	2
32	8.192	24.576	3
24	6.144	24.576	4
19.2	4.9152	24.576	5
16	4.096	24.576	6
12	3.072	24.576	8
9.6	2.4576	24.576	10
8	2.048	24.576	12
7.2	1.843	22.116	12
44.1	11.2896	22.5792	2

Table 2. SM1 - Example Clock Frequencies

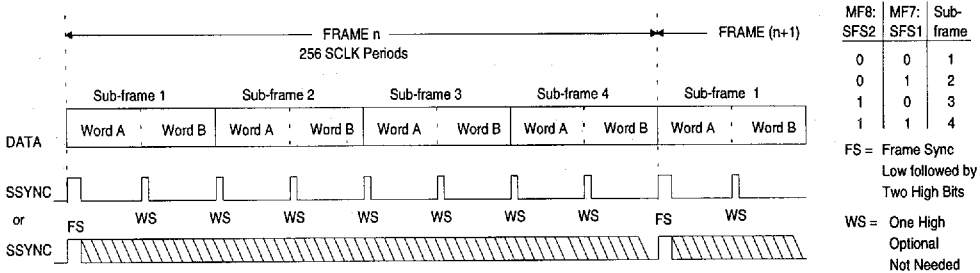


Figure 7. SM1, SM2 - 256 Bits per Frame.

SERIAL MODE 2, SM2

Serial Mode 2 is enabled by setting $SMODE3 = 0$, and $SMODE1 = 1$. SM2 is similar to SM1 except that SCLK is fixed at $256 \times F_s$ and is the master clock instead of CLKIN. The CLKIN pin is ignored in this mode and should be tied low. In SM2, the sample frequency will scale linearly with the frequency of SCLK. Up to four codecs may occupy the serial bus since each codec requires only 64 bit periods and a frame is fixed at 256 bit periods. The serial data format is the same as SM1 and is illustrated in Figures 5 and 6.

The multifunction pins in SM2 are defined identically to SM1. See *Serial Mode 1, SM1* section for more details.

SERIAL MODE 3, SM3

Serial Mode 3 is enabled by setting $SMODE3 = 0$, $SMODE2 = 1$ and $SMODE1 = 0$. This mode is designed to interface easily to DSPs and has the added versatility of a programmable number of bits per frame, a master mode, and one extra bit of D/A attenuation. In SM3, two of the parallel digital input bits and two of the parallel digital output bits are available.

Master Clock Frequency

In SM3, the master clock, CLKIN, must be $256 \times F_{smax}$. For example, given a 48 kHz maximum sample frequency, the master clock frequency must be 12.288 MHz. SCLK and SSYNC must be synchronous to CLKIN.

D/A Attenuation

SM3 has one more bit per channel allocated for D/A attenuation which doubles the attenuation range. Figure 5 illustrates the serial data in, SDIN, sub-frame for all SM3 sub-modes. The upper portion of this figure shows modes SM1 and SM2 where the D/A attenuation is located in Word B, bits 53 through 60. Four bits allow attenuation on each channel from 0 dB down to -22.5 dB using 1.5 dB steps. In SM3 the attenuation bits are still located in Word B, but start at bit 51 of the sub-frame. This allows five bits of attenuation per channel instead of four, producing an attenuation range for each channel from 0 dB down to -46.5 dB.

In SM3 MF5:DO2 is a general purpose output and MF6:DI2 is a general purpose input. The other six multifunction pins are used to select sub-modes under SM3.

SM3 is divided into two sub-modes, Master and Slave. In Master sub-mode, the CS4216 generates SSYNC and SCLK, while in Slave sub-mode SSYNC and SCLK must be generated

externally. In Master sub-mode, the serial port signal transitions are controlled with respect to the internal analog sampling clock to minimize the amount of digital noise coupled into the analog section. Since SSYNC and SCLK are externally derived in Slave sub-mode, optimum noise management cannot be obtained; therefore, Master sub-modes should be used whenever possible.

Master Sub-Mode (SM3)

Master sub-mode is selected by setting MF4:MA = 1, which configures SSYNC and SCLK as outputs from the CS4216. During power down, SSYNC and SCLK are driven high impedance, and during reset they both are driven low. In Master sub-mode the number of bits per frame determines how many codecs can occupy the serial bus and is illustrated in Figure 8.

Bits Per Frame (Master Sub-Mode)

MF8:SFS2 selects the number of bits per frame. The two options are MF8:SFS2 = 1 which selects 128 bits per frame, and MF8:SFS2 = 0 which selects 64 bits per frame.

Selecting 128 bits per frame (MF8:SFS2 = 1) allows two CS4216s to operate from the same serial bus since each codec requires 64 bit periods. The sub-frame used by an individual codec is selected using MF7:SFS1. MF7:SFS1 = 0 selects sub-frame 1 which is the first 64 bits following the SSYNC pulse. MF7:SFS1 = 1 selects sub-frame 2 which is the last 64 bits of the frame.

Selecting 64 bits per frame (MF8:SFS2 = 0) allows only one CS4216 to occupy the serial port. Since there is only one sub-frame (which is equal to one frame), MF7:SFS1 is defined differently in this mode. MF7:SFS1 selects the format of SSYNC. MF7:SFS1 = 0 selects an SSYNC pulse one SCLK period high, directly preceding the data as shown in the center portion of Fig-

ure 8. This format is used for all other Master and Slave sub-modes in SM3. If MF7:SFS1 = 1, an alternate SSYNC format is chosen in which SSYNC is high during the entire Word A (32 bits), which includes the left sample, and low for the entire Word B (32 bits), which includes the right sample. This alternate format for SSYNC is illustrated in the bottom portion of Figure 8 and is only available in Master sub-mode with 64 bits per frame. A more detailed timing diagram for the 64 bits-per-frame Master sub-mode is shown in Figure 9.

Sample Frequency Selection (Master Sub-Mode)

In SM3, Master sub-mode, the multifunction pins MF1:F1, MF2:F2, and MF3:F3 are used to select the sample frequency divider. Table 3 lists the decoding for the sample frequency select pins where the sample frequency selected is CLKIN/N. Also shown are the sample frequencies obtained by using one of two example master clocks: either 12.288 MHz or 11.2896 MHz. The codec must be reset when changing sample frequencies to allow the codec to calibrate to the new sample frequency.

Slave Sub-Mode (SM3)

In SM3, Slave sub-mode is selected by setting MF4:MA = 0 which configures SSYNC and SCLK as inputs to the CS4216. These two signals must be externally derived from CLKIN. In Slave sub-mode, the phase relationship between SCLK/SSYNC and CLKIN cannot be controlled since SCLK and SSYNC are externally derived. Therefore, the noise performance may be slightly worse than when using the master sub-mode.

The number of sub-frames on the serial port is selected using MF1:F1 and MF2:F2. In Slave sub-mode MF3:F3 works as a general purpose input. Figures 10 through 12 illustrate the Slave sub-mode formats.

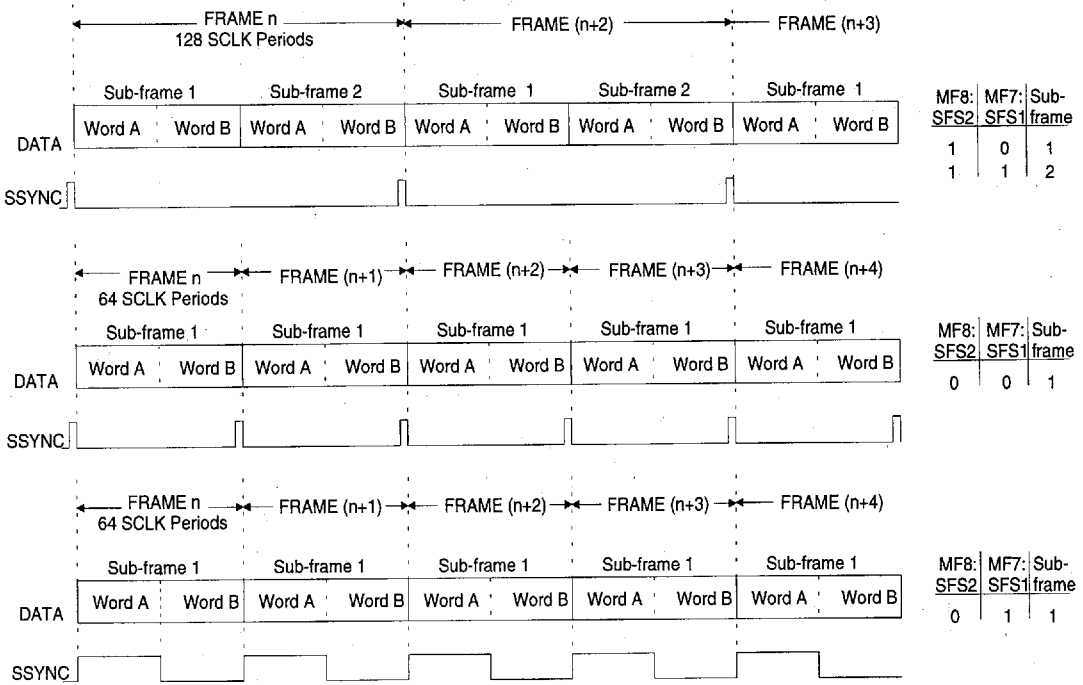


Figure 8. SM3, Master Sub-Mode.

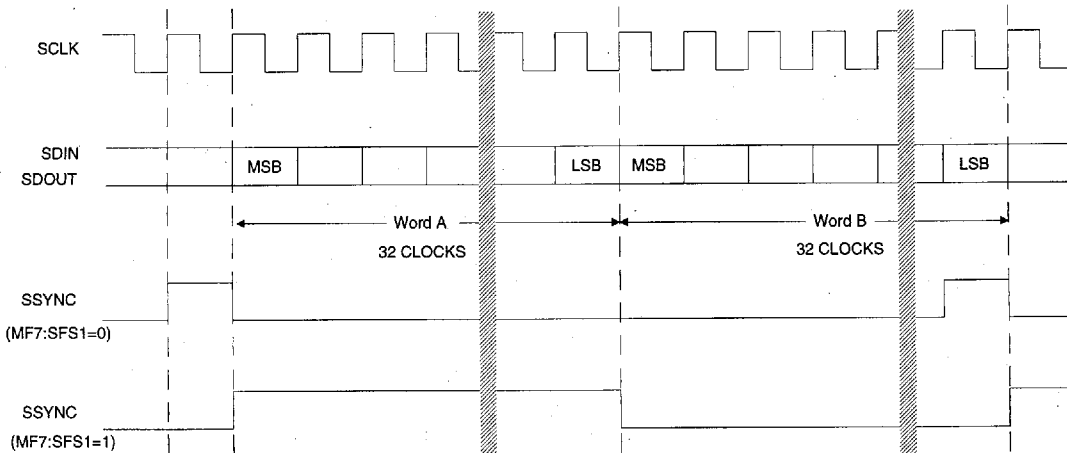


Figure 9. Detailed Master Sub-Mode, 64 BPF.

Bits per Frame (Slave Sub-Mode)

In Slave sub-mode, MF1:F1 and MF2:F2 select the number of bits per frame which determines how many CS4216's can occupy one serial port. Table 4 lists the decoding for MF1:F1 and MF2:F2.

When set for 64 SCLKs per frame, one device occupies the entire frame; therefore, a sub-frame is equivalent to a frame. MF7:SFS1 and MF8:SFS2 must be set to zero. See Figure 10.

When set for 128 SCLKs per frame, two devices can occupy the serial port, with MF7:SFS1 selecting the particular sub-frame. MF8:SFS2 must be set to zero. See Figure 11.

When set for 256 SCLKs per frame (MF1:F1, MF2:F2 = 10), four devices can occupy the serial port. In this format both MF8:SFS2 and MF7:SFS1 are used to select the particular sub-frame. See Figure 12.

In all three of the above Slave sub-mode formats, the frequency of the incoming SCLK signal, in relation to the master clock provided on the CLKIN pin, determines the sample frequency. The CS4216 determines the ratio of SCLK to CLKIN and sets the internal operating

frequency accordingly. Table 5 lists the SCLK to CLKIN frequency ratio used to determine the codec's sample frequency. To obtain a given sample frequency, SCLK must equal CLKIN divided by the number in the table, based on the number of bits per frame. As an example, assuming 64 BPF (bits per frame) and CLKIN = 12.288 MHz, if a sample frequency of 24 kHz is desired, SCLK must equal CLKIN divided by 8 or 1.536 MHz.

When MF1:F1 = MF2:F2 = 1, SCLK is used as the master clock and is assumed to be 256 times the sample frequency. In this mode, CLKIN is ignored and the sample frequency is linearly scaled with SCLK. (The CLKIN pin must be tied low.) This mode also fixes SCLK at 256 bits per frame with MF7:SFS1 and MF8:SFS2 selecting the particular sub-frame.

MF1: F1	MF2: F2	Bits per Frame	Sample Frequency/ SCLK
0	0	64	ratio to CLKIN sensed
0	1	128	ratio to CLKIN sensed
1	0	256	ratio to CLKIN sensed
1	1	256	fixed [†] = 256×Fs

[†] SCLK is master clock. CLKIN is not used.

Table 4. SM3-Slave, Bits per Frame.

MF1: F1	MF2: F2	MF3: F3	N	Fs (kHz) with CLKIN	
				12.288 MHz	11.2896 MHz
0	0	0	256	48.00	44.10
0	0	1	384	32.00	29.40
0	1	0	512	24.00	22.05
0	1	1	640	19.20	17.64
1	0	0	768	16.00	14.70
1	0	1	1024	12.00	11.025
1	1	0	1280	9.60	8.82
1	1	1	1536	8.00	7.35

Table 3. SM3-Master, Fs Select

SCLK to CLKIN Ratio			Fs (kHz) with CLKIN	Fs (kHz) with CLKIN
BPF 256	BPF 128	BPF 64	12.288 MHz	11.2896 MHz
1	2	4	48.00	44.10
1.5	3	6	32.00	29.40
2	4	8	24.00	22.05
2.5	5	10	19.20	17.64
3	6	12	16.00	14.70
4	8	16	12.00	11.025
5	10	20	9.60	8.82
6	12	24	8.00	7.35

Table 5. SM3-Slave, Fs Select.

SERIAL MODE 4, SM4

Serial mode 4 is enabled by setting $SMODE3 = 1$. Both Master and Slave sub-modes are available and are selected by setting the $SMODE2$ and $SMODE1$ pins as shown in Table 6. In Master sub-mode, the phase relationship between $SCLK/SSYNC$ and $CLKIN$ is controlled to minimize digital noise coupling into the analog section. Therefore, Master sub-mode may yield slightly better noise performance than Slave sub-mode. In Slave sub-mode, $SCLK$ and $SSYNC$ must be synchronous to the master clock.

In serial mode 4, SM4, the $CLKIN$ frequency must be 256 times the highest sample frequency needed. Also, SM4 has five attenuation bits for

each D/A output channel. SM4 differs from SM3 in that SM4 splits the audio data from the control data with the control data input on an independent serial port. This reduces the audio serial bus bandwidth in half, providing an easier interface to low-cost DSPs. The audio serial port sub-frame is illustrated in Figure 13 for SM4.

Interrupt Pin - MF5:INT

Serial Mode 4 also defines the multifunction pin $MF5:INT$ as an open-collector interrupt pin. In SM4, this pin requires a pullup resistor and will go low when the ADV bit or $DI1$ pin change, or a rising edge on the LCL or RCL bits, or by exiting an $SCLK$ out of range condition ($Error = 3$). The interrupt may be masked by setting the MSK bit in the control serial data port.

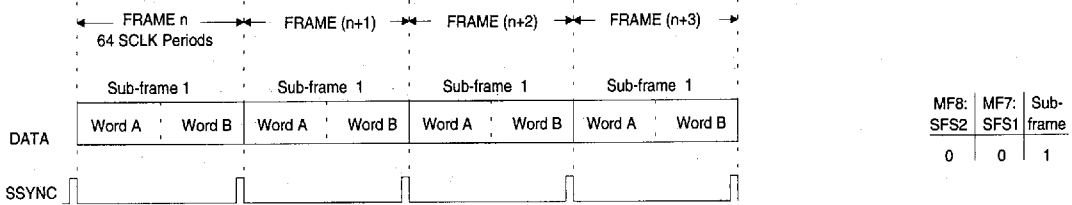


Figure 10. SM3-Slave - 64 BPF; MF1:F1, MF2:F2 = 00

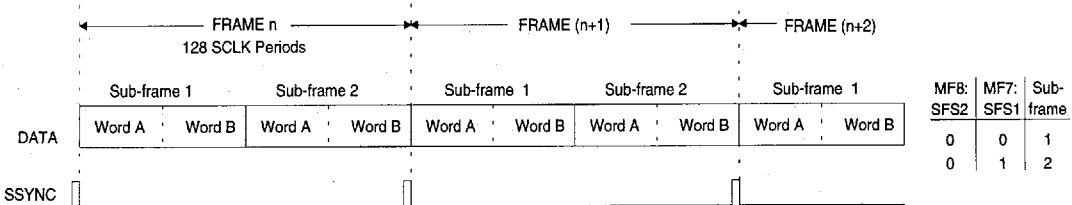


Figure 11. SM3-Slave - 128 BPF; MF1:F1, MF2:F2 = 01

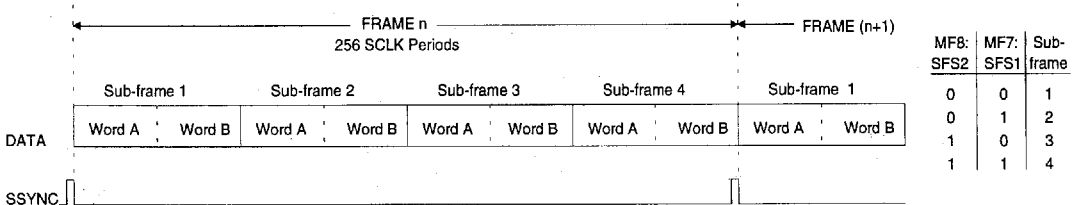


Figure 12. SM3-Slave - 256 BPF; MF1:F1, MF2:F2 = 10

MF5:INT is reset by reading the control serial port.

Master Sub-Mode (SM4)

Master sub-mode configures SSYNC and SCLK as outputs from the CS4216. During power down, SSYNC and SCLK are driven high impedance, and during reset they both are driven low. There are two SM4 Master sub-modes. One allows 32 bits per frame and the other allows 64 bits per frame. As shown in Table 6, the SMODE1 and SMODE2 pins select the particular Master sub-mode (as well as the Slave sub-mode). When SMODE1 is set to zero, SMODE2 selects either Master sub-mode with 32-bit frames, or Slave sub-mode.

SMODE1,SMODE2 = 00 selects Master sub-mode where a frame = sub-frame = 32 bits. This sub-mode allows only one codec on the audio serial bus, with the first 16 bits being the left channel and the second 16 bits being the right

channel. The *Applications of SM4* section contains more information on low-cost implementations of this sub-mode.

SMODE1 = 1 selects Master sub-mode with a frame width of 64 bits. This sub-mode allows up to two codecs to occupy the same bus. SMODE2 is now used to select the particular time slot. If SMODE2 = 0 the codec selects time slot 1, which is the first 32 bits. If SMODE2 = 1 the codec selects time slot 2, which is the second 32 bits.

In Master sub-mode, multifunction pins MF6:F1, MF7:F2, and MF8:F3 select the sample frequency as shown in Table 7. This table indicates how to obtain standard audio sample frequencies given one of two CLKIN frequencies: 12.288 MHz or 11.2896 MHz. Other CLKIN frequencies may be used with the corresponding sample frequencies being CLKIN/N. The codec must be reset when changing sample frequencies to allow a new calibration to occur.

SMODE1	SMODE2	SM4, Sub-Mode
0	0	Master, 32 BPF
0	1	Slave, 128/64/32 BPF
1	0	Master, 64 BPF, TS1
1	1	Master, 64 BPF, TS2

Table 6. SM4 Sub-Modes.

Slave Sub-Mode (SM4)

In SM4, Slave sub-mode is selected by setting SMODE1,SMODE2 = 01. This mode configures SSYNC and SCLK as inputs to the CS4216. These two signals must be externally derived from CLKIN. Since the CS4216 has no control over the phase relationship of SSYNC and

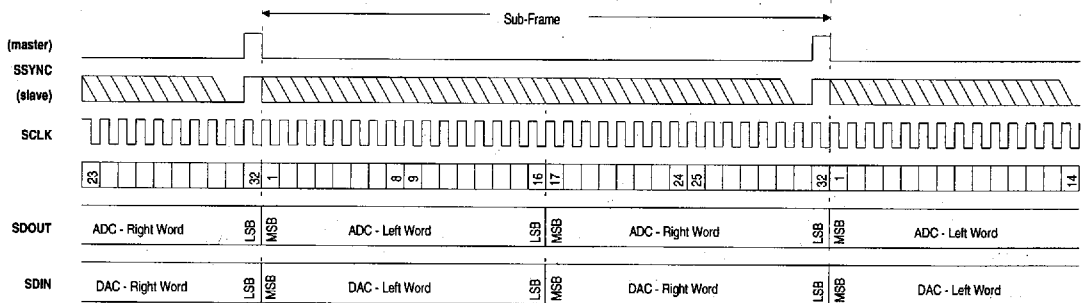


Figure 13. SM4-Audio Serial Port, 32 BPF

SCLK to CLKIN, the noise performance in Slave sub-mode may be slightly worse than when using Master sub-mode. The CS4216 internally sets the sample frequency by sensing the ratio of SCLK to CLKIN; therefore, for a given CLKIN frequency, the sample frequency is selected by changing the SCLK frequency.

SM4-Slave allows up to four codecs to occupy the same audio serial port. Table 8 lists the pin configurations required to set the serial audio port up for 32, 64, or 128 bits-per-frame (BPF). Since each codec requires one sub-frame of 32 bits, 64 bits-per-frame allows up to two codecs to occupy the same audio serial port, and 128 bits-per-frame allows up to four codecs to occupy the same audio serial port. When set up for more than one codec on the bus, other pins are needed to select the particular time slot (TS) associated with each codec. MF8:SFS2 selects the time slot when in 64 BPF mode, and MF8:SFS2 and MF7:SFS1 select one of four time slots when in 128 bits-per-frame mode. Table 8 lists the decoding for time slot selection.

In SM4-Slave, the frequency of the incoming SCLK signal, in relation to CLKIN, determines the sample frequency on the CS4216. The CS4216 determines the ratio of SCLK to CLKIN and sets the internal sample frequency accord-

ingly. Table 9 lists the SCLK to CLKIN frequency ratio used to determine the codec's sample frequency. SCLK must equal CLKIN divided by the number in the table, based on the selected bits per frame. As an example, assuming 32 BPF and CLKIN = 11.2896 MHz, if a sample frequency of 11.025 kHz is desired, SCLK must equal CLKIN divided by 32 or 352.8 kHz.

Serial Control Port (SM4)

Serial Mode 4 separates the audio data from the control data. Since control data such as gain and attenuation do not change often, this mode reduces the bandwidth needed to support the audio serial port.

The control information is entered through a separate port that can be asynchronous to the audio port and only needs to be updated when changes in the control data are needed. After a reset or power down, the control port must be written once to initialize it if the port will be accessed to read or write control bits. This initial write is considered a "dummy" write since the data is ignored by the codec. A second write is needed to configure the codec as desired. Then, the control port only needs to be written to when a change is desired, or to obtain the status information. The control port does not function if the master clock is not operating. When the control

MF6: F1	MF7: F2	MF8: F3	N	Fs (kHz) with CLKIN	
				12.288 MHz	11.2896 MHz
0	0	0	256	48.00	44.10
0	0	1	384	32.00	29.40
0	1	0	512	24.00	22.05
0	1	1	640	19.20	17.64
1	0	0	768	16.00	14.70
1	0	1	1024	12.00	11.025
1	1	0	1280	9.60	8.82
1	1	1	1536	8.00	7.35

Table 7. SM4-Master, Fs Select

MF6: F1	MF7: SFS1	MF8: SFS2	Bits Per Frame (BPF)	Time Slot (TS)
0	0	0	32	1
0	0	1	Reserved	
0	1	0	64	1
0	1	1	64	2
1	0	0	128	1
1	1	0	128	2
1	0	1	128	3
1	1	1	128	4

Table 8. SM4-Slave, Audio Port BPF & TS Select

port is used asynchronously to the audio port, the noise performance may be slightly degraded due to this asynchronous digital noise.

Since control data does not need to be accessed each audio frame, an interrupt pin, MF5:INT, is included in this mode and will go low when status has changed. The control port serial data format is illustrated in Figure 14. The control port uses one of the multifunction pins as a chip select line, MF4:CCS, that must be low for entering control data. Although only 23 bits contain useful data on MF2:CDIN, a minimum of 31 bits must be written. If more than 31 bits are written without toggling MF4:CCS, only the first 31 are recognized. MF1:CDOUT contains

status information that is output on the rising edge of MF3:CCLK. Status information is repeated at the end of the frame, bits 25 through 30, to allow a simple 8-bit shift and latch register to store the most important status information using the rising edge of MF4:CCS at the latch control (see Figure 17).

Applications of SM4

Figure 15 illustrates one method of using serial mode 4 wherein a DSP controls the audio serial port and a microcontroller controls the control port. Each controller is run independently and the micro updates the control information only when needed, or when an interrupt from the CS4216 occurs.

Figure 16 illustrates the minimum interface to the CS4216. In this application, the DSP sends and receives stereo DAC and ADC information. The CS4216 is configured for 32 bits per frame, Master sub-mode. The control data resets to all zeros, which configures the CS4216 as a simple stereo codec: no gain, no attenuation, line inputs #1, and not muted.

Figure 17 illustrates how to use all the CS4216 features with a low cost DSP that cannot support the interrupt rate of SM3. Using SM4 (32 bits

SCLK to CLKIN Ratio			Fs (kHz)	Fs (kHz)
BPF	BPF	BPF	with CLKIN	with CLKIN
128	64	32	12.288 MHz	11.2896 MHz
2	4	8	48.00	44.10
3	6	12	32.00	29.40
4	8	16	24.00	22.05
5	10	20	19.20	17.64
6	12	24	16.00	14.70
8	16	32	12.00	11.025
10	20	40	9.60	8.82
12	24	48	8.00	7.35

Table 9. SM4-Slave, Fs Select.

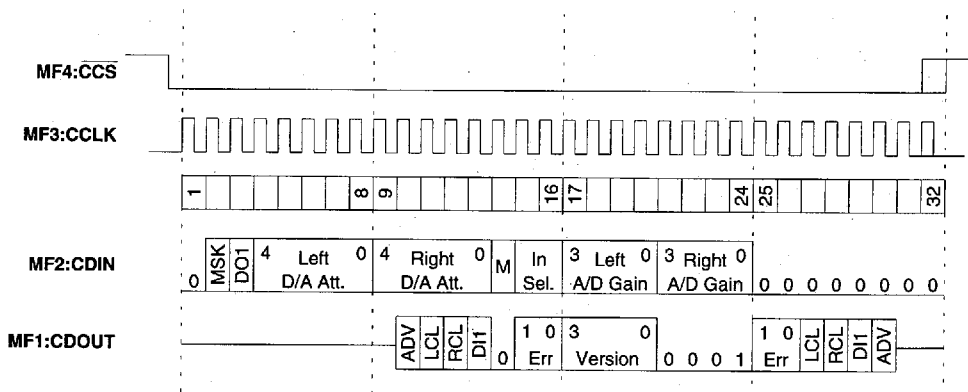


Figure 14. SM4 - Control Serial Port

per frame, Master sub-mode) reduces the DSP interrupts in half since the control data is split from the audio data. This circuit is comprised of three independent sections which may individually be eliminated if not needed.

To load control data into the codec, three HC597's are utilized. These are both latches that store the DSP-sent control data, and shift registers that shift the data into the codec. The codec uses an inverted SSYNC signal to copy the latches to the shift registers every frame. In this diagram the DSP is assumed to have a data bus bandwidth of at least 24 bits. If the DSP has less than 24 bits, the three HC597s must be split into two addresses. Since the HC597 internal latches are copied to the shift registers, the latches continually hold the DSP-sent data; therefore, the

DSP only needs to write data to the latches when a change is desired.

The second section is comprised of an HC595 shift register and latch that is clocked by an inverted SCLK. The data shifted into the HC595 is transferred to the HC595's latch by the SSYNC signal. This HC595 captures the 8 bits prior to the SSYNC signal (which is also MF4:CCS) going high. As shown in Figure 14, and assuming the MF4:CCS (SSYNC) signal rises at bit 32, the 8-bits prior to MF4:CCS rising are a copy of all the important status bits. This allows one shift register to capture all the important information. The interrupt pin cannot reliably be used in this configuration since the interrupt pin is cleared by reading the control port which occurs asynchro-

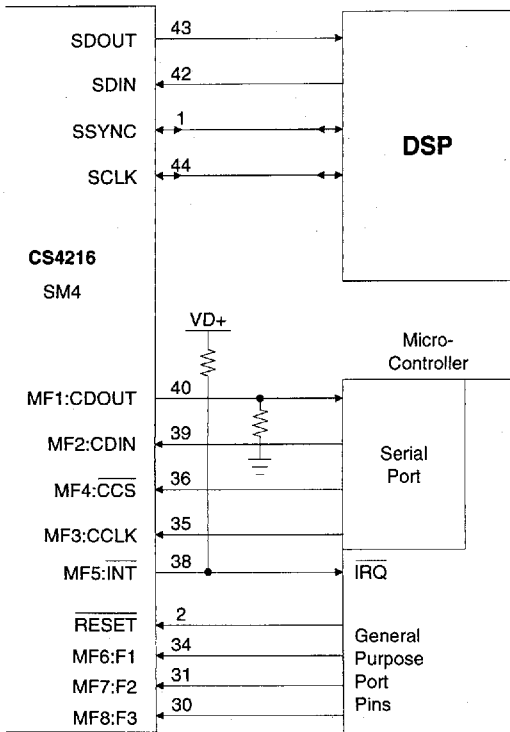


Figure 15. SM4 - Microcontroller Interface

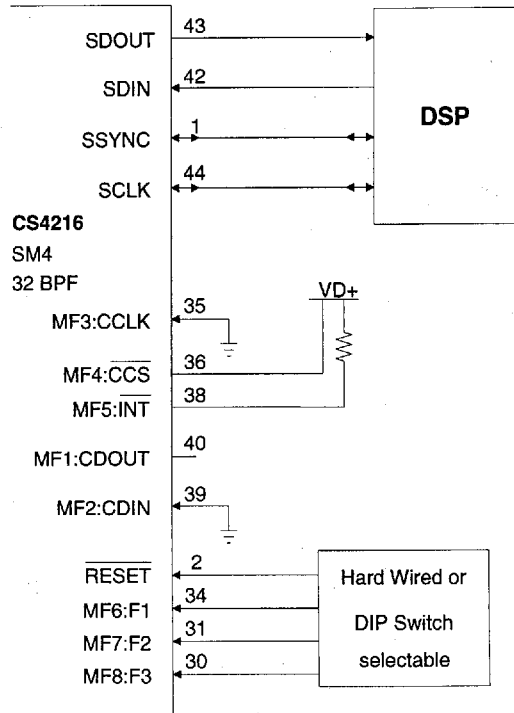


Figure 16. SM4 - Minimum DSP Interface

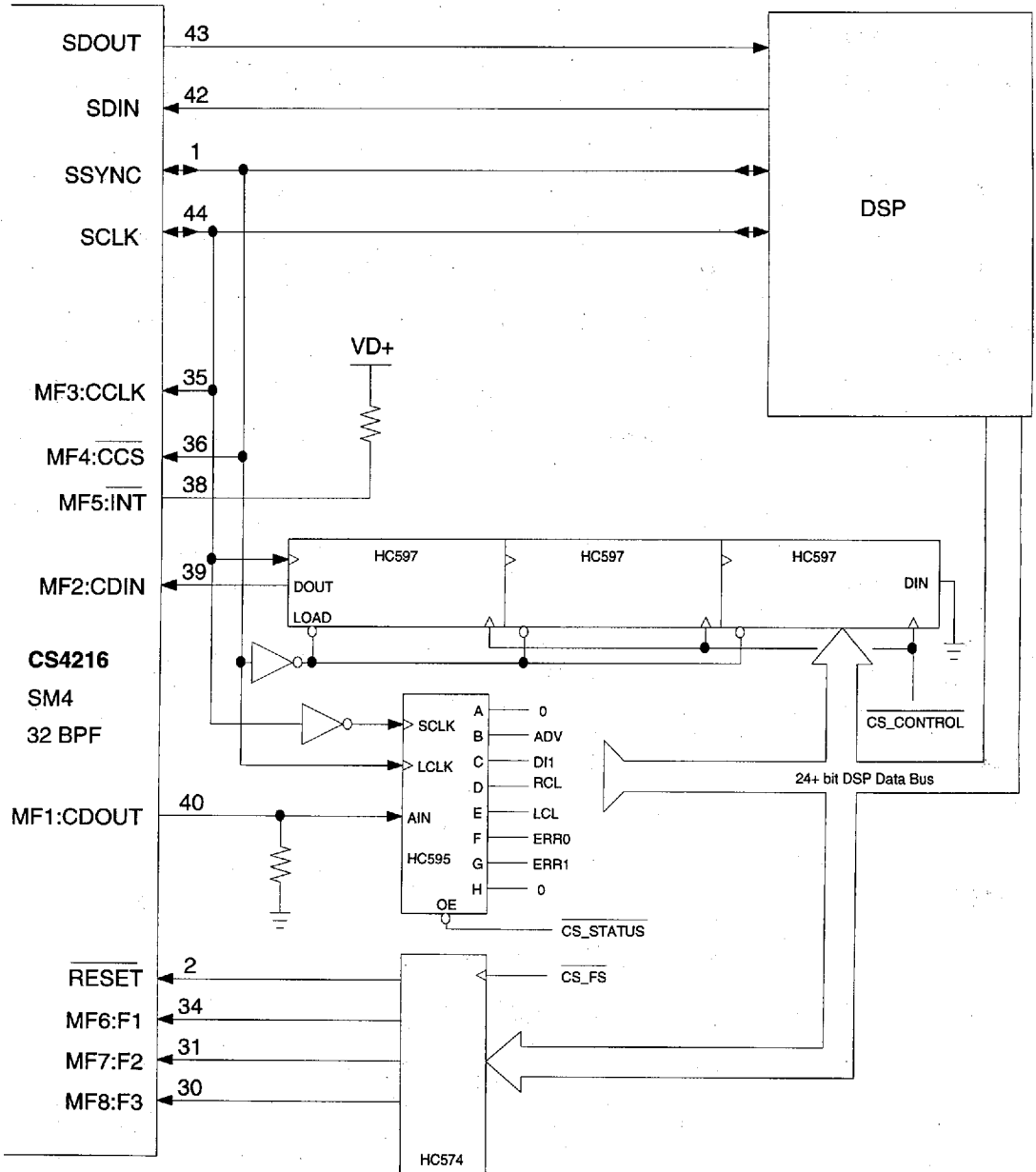


Figure 17. SM4 - Enhanced DSP Interface

nously (every audio frame) with respect to the interrupt occurrence.

The third section is only needed if sample frequencies need to be changed. This section is comprised of an HC574 octal latch that can be replaced by general purpose port pins if available. This section controls the sample frequency selection bits: MF6:F1, MF7:F2, MF8:F3 and the **RESET** pin. The codec must be reset when changing sample frequencies.

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Power Supply and Grounding

The CS4216, along with associated analog circuitry, should be positioned in an isolated section of the circuit board, and have its own, separate, ground plane. On the CS4216, the analog and digital grounds are internally connected; therefore, the AGND and DGND pins must be externally connected with no impedance between them. The best solution is to place the entire chip on a solid ground plane as shown in Figure 18. Preferably, it should also have its own power plane. The +5V supply must be connected to the CS4216 via a ferrite bead, positioned closer than 1" to the device. The VA supply can be derived from VD, as shown in Figure 1. Alternatively, a separate +5V analog supply may be used for VA, in which case, the 2.0 Ω resistor between VA and VD should be removed. A single connection between the CS4216 ground

(analog ground) and the board digital ground should be positioned as shown in Figure 18.

Figure 19 illustrates the optimum ground and decoupling layout for the CS4216 assuming a surface-mount socket and leaded decoupling capacitors. Surface-mount sockets are useful since the pad locations are identical to the chip pads; therefore, assuming space for the socket is left on the board, the socket can be optional for production. Figure 19 depicts the top layer, containing signal traces, and assumes the bottom or inter-layer contains a fairly solid ground plane. The important points are that there is solid ground plane under the codec on the same layer as the codec and it connects all ground pins with thick traces providing the absolute lowest impedance between ground pins. The decoupling capacitors are placed as close as possible to the device which, in this case, is the socket boundary. The lowest value capacitor is placed closest to the codec. Vias are placed near the AGND and DGND pins, under the IC, and should attach to the solid ground plane on another layer. The negative side of the decoupling capacitors should also attach to the same solid ground plane. Traces and vias bringing power to the codec should be large, which minimizes the impedance.

Although not shown in the figures, the trace layers (top layer in the figures) should have ground plane fill in-between the traces to minimize coupling into the analog section. See the CDB4216 evaluation board as an example.

If using all surface-mount components, the decoupling capacitors should be placed on the same layer as the codec and in the positions shown in Figure 20. The vias shown are assumed to attach to the appropriate power and ground layers. Traces and vias bringing power to the codec should be as large as possible to minimize the impedance.

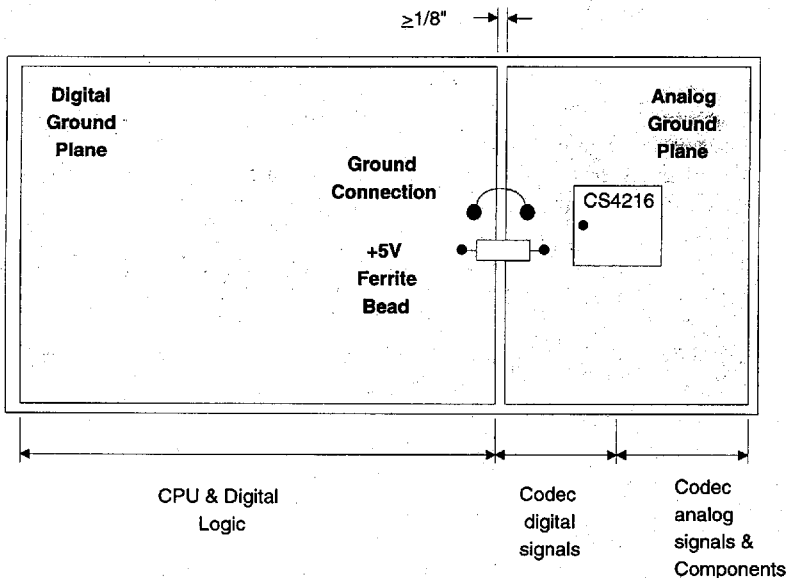
If using a through-hole socket, effort should be made to find a socket with minimum height,

which will minimize the socket impedance. When using a through hole socket, the vias under the codec in Figure 19 are not needed since the pins serve the same function.

ADC and DAC Filter Response Plots

Figures 21 - 26 shows the overall frequency response, passband ripple and transition band for the CS4216 ADCs and DACs. Figure 27 shows the DACs' deviation from linear phase.

Fs is defined as the selected sample frequency and is also the SSYNC frequency. Since the sample frequency is programmable, the filters will adjust to the selected sample frequency.



Note that the CS4216 is oriented with its digital pins towards the digital end of the board.

Figure 18. CS4216 Board Layout Guideline

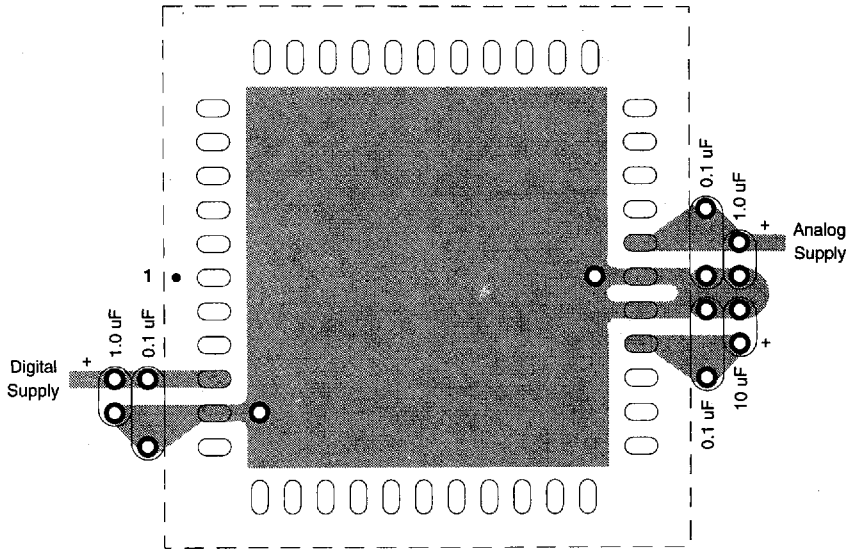


Figure 19. CS4216 Decoupling Layout Guideline

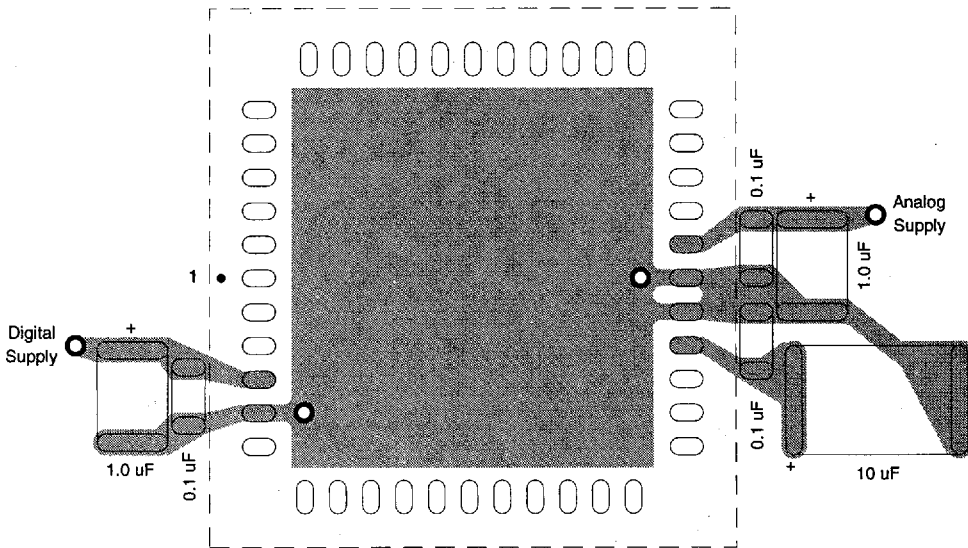


Figure 20. CS4216 Surface Mount Decoupling Layout

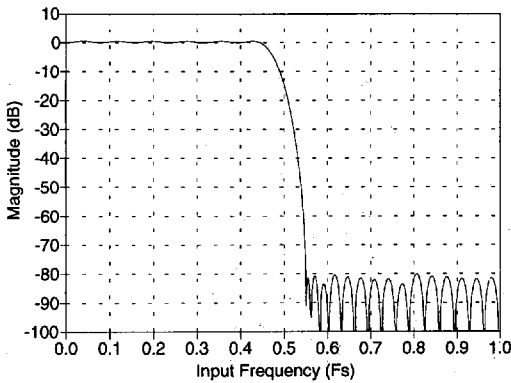


Figure 21. CS4216 ADC Frequency Response

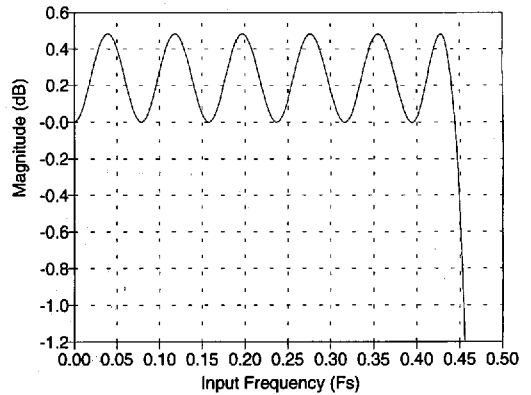


Figure 22. CS4216 ADC Passband Ripple

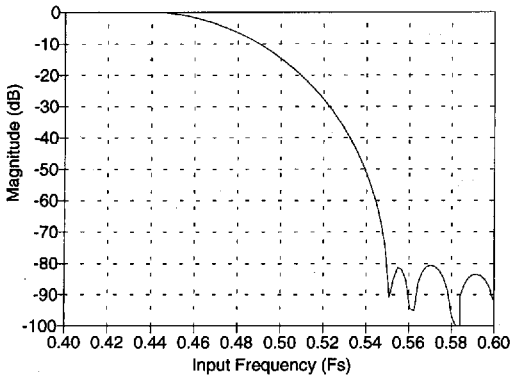


Figure 23. CS4216 ADC Transition Band

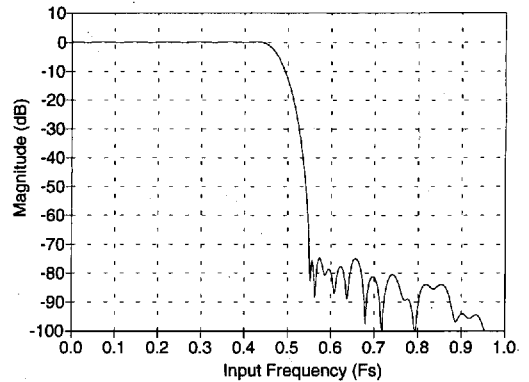


Figure 24. CS4216 DAC Frequency Response

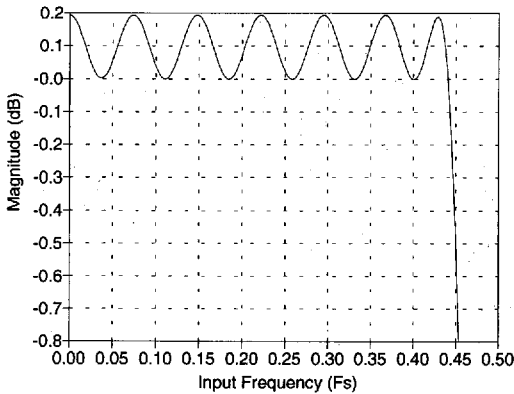


Figure 25. CS4216 DAC Passband Ripple

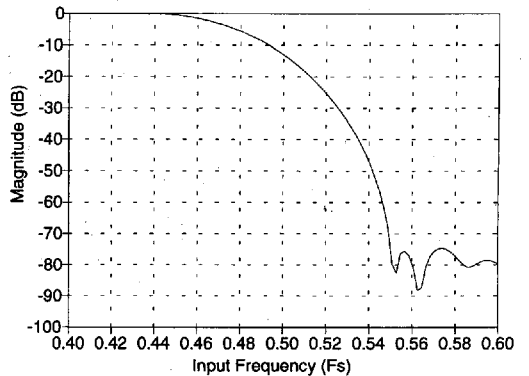


Figure 26. CS4216 DAC Transition Band

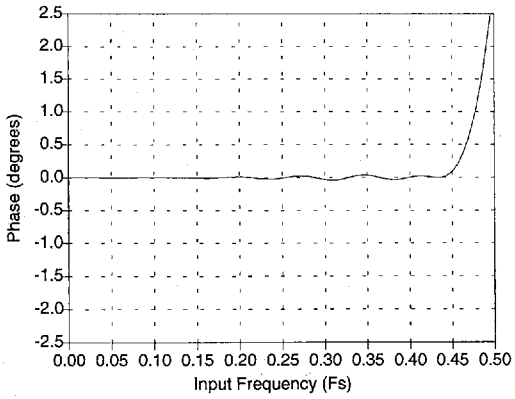
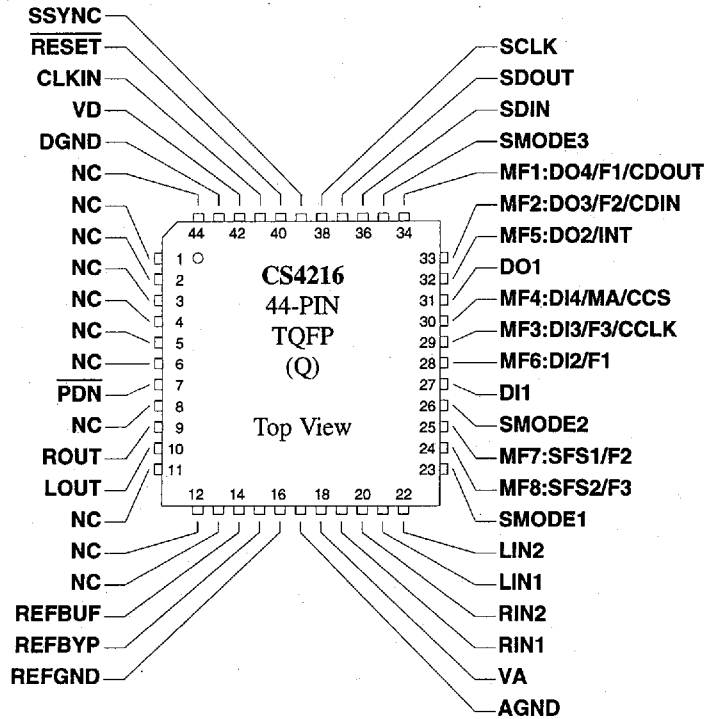
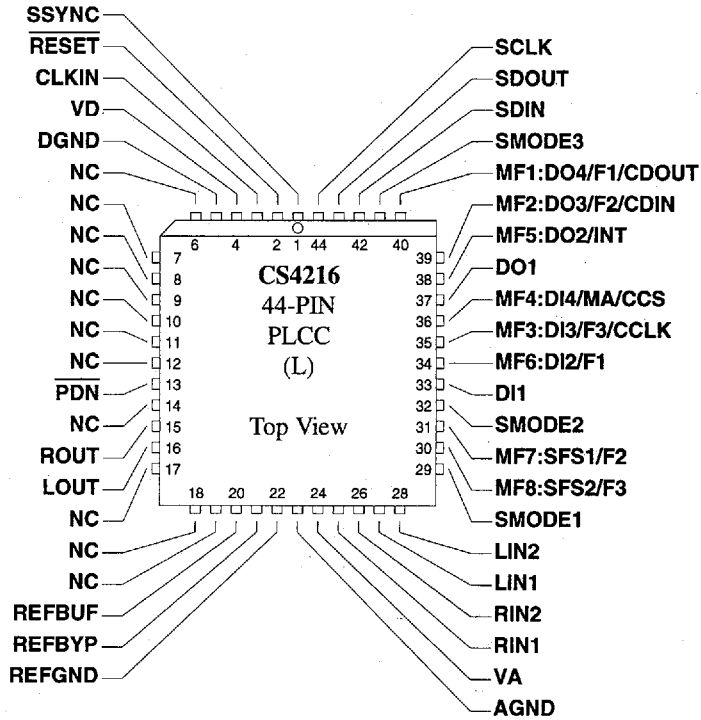


Figure 27. CS4216 DAC Deviation from Linear Phase

PIN DESCRIPTIONS



SM	MF1	MF2	MF3	MF4	MF5	MF6	MF7	MF8
1	DO4	DO3	DI3	DI4	DO2	DI2	SFS1	SFS2
2	DO4	DO3	DI3	DI4	DO2	DI2	SFS1	SFS2
3	F1	F2	F3	MA	DO2	DI2	SFS1	SFS2
4-SL	CDOUT	CDIN	CCLK	CCS	INT	F1	SFS1	SFS2
4-MA	CDOUT	CDIN	CCLK	CCS	INT	F1	F2	F3



SM	MF1	MF2	MF3	MF4	MF5	MF6	MF7	MF8
1	DO4	DO3	DI3	DI4	DO2	DI2	SFS1	SFS2
2	DO4	DO3	DI3	DI4	DO2	DI2	SFS1	SFS2
3	F1	F2	F3	MA	DO2	DI2	SFS1	SFS2
4-SL	CDOUT	CDIN	CCLK	CCS	INT	F1	SFS1	SFS2
4-MA	CDOUT	CDIN	CCLK	CCS	INT	F1	F2	F3

Power Supply

VD - Digital +5V Supply, PIN 4(L), 42(Q).
+5V digital supply.

VA - Analog +5V Supply, PIN 24(L), 18(Q).
+5V analog supply.

DGND - Digital Ground, PIN 5(L), 43(Q).
Digital ground. Must be connected to AGND with zero impedance.

AGND - Analog Ground, PIN 23(L), 17(Q).

Analog ground. Must be connected to DGND with zero impedance.

Analog Inputs**RIN1 - Right Input #1, PIN 25(L), 19(Q).**

Right analog input #1. Full scale input, with no gain, is 1 Vrms, centered at REFBUF.

RIN2 - Right Input #2, PIN 26(L), 20(Q).

Right analog input #2. Full scale input, with no gain, is 1 Vrms, centered at REFBUF.

LIN1 - Left Input #1, PIN 27(L), 21(Q).

Left analog input #1. Full scale input, with no gain, is 1 Vrms, centered at REFBUF.

LIN2 - Left Input #2, PIN 28(L), 22(Q).

Left analog input #2. Full scale input, with no gain, is 1 Vrms, centered at REFBUF.

Analog Outputs**ROUT - Right Channel Output, PIN 15(L), 9(Q).**

Right channel analog output. Maximum signal is 1 Vrms centered at REFBUF.

LOUT - Left Channel Output, PIN 16(L), 10(Q).

Left channel analog output. Maximum signal is 1 Vrms centered at REFBUF.

REFBYP - Analog Reference Decoupling, PIN 21(L), 15(Q).

A 10 μ F and 0.1 μ F capacitor must be attached between REFBYP and REFGND.

REFGND - Analog Reference Ground Connection, PIN 22(L), 16(Q).

Connect to AGND.

REFBUF - Buffered Reference Out, PIN 20(L), 14(Q).

A nominal +2.2 V output for setting the bias level for external analog circuits.

Serial Digital Audio Interface Signals**SDIN - Serial Port Data In, PIN 42(L), 36(Q).**

Digital audio data to the DACs and level control information is received by the CS4216 via SDIN.

SDOUT - Serial Port Data Out, PIN 43(L), 37(Q).

Digital audio data from the ADCs and status information is output from the CS4216 via SDOUT.

SCLK - Serial Port Bit Clock, PIN 44(L), 38(Q).

SCLK controls the digital audio data on SDOUT and latches the data on SDIN.

SSYNC - Serial Port Sync Signal, PIN 1(L), 39(Q).

Indicates the start of a digital audio frame in SM3 and SM4, and also the start of a word in SM1 & SM2.

SMODE1 - Serial Mode Select, PIN 29(L), 23(Q).

One of three pins that select the serial mode and function of the multifunction pins.

SMODE2 - Serial Mode Select, PIN 32(L), 26(Q).

One of three pins that select the serial mode and function of the multifunction pins.

SMODE3 - Serial Mode Select, PIN 41(L), 35(Q).

One of three pins that select the serial mode and function of the multifunction pins. This pin has an internal pull-down making this revision backwards compatible with a previous version (Revision A or Version3-Version0 bits = 0000).

Multifunction Digital Pins**MF1:DO4 - Parallel Digital Bit Output #4 in SM1/SM2, PIN 40(L), 34(Q).**

In serial modes 1 and 2 this pin reflects the value of the DO4 bit in the sub-frame.

MF1:F1 - Format bit 1 in SM3, PIN 40(L), 34(Q).

In serial mode 3 this pin is a format bit and is used as one of three sample frequency select pins when in master mode, or as one of two bits-per-frame select pins when in slave mode.

MF1:CDOOUT - Control Data Output in SM4, PIN 40(L), 34(Q).

In serial mode 4 this pin is the data output for the control port which contains status information.

MF2:DO3 - Parallel Digital Bit Output #3 in SM1/SM2, PIN 39(L), 33(Q).

In serial modes 1 and 2 this pin reflects the value of the DO3 bit in the sub-frame.

MF2:F2 - Format bit 2 in SM3, PIN 39(L), 33(Q).

In serial mode 3 this pin is a format bit and is used as one of three sample frequency select pins when in master mode, or as one of two bits-per-frame select pins when in slave mode.

MF2:CDIN - Control Data Input in SM4, PIN 39(L), 33(Q).

In serial mode 4 this pin is the control port data input which contains data such as gain and attenuation settings as well as input select, mute, and digital output bits.

MF3:DI3 - Parallel Digital Bit Input #3 in SM1/SM2/SM3 (Slave), PIN 35(L), 29(Q).

In serial modes 1 and 2 this pin value is reflected in the DI3 bit in the sub-frame.

MF3:F3 - Format bit 3 in SM3 (Master), PIN 35(L), 29(Q).

In serial mode 3 this pin is a format bit and is used as one of three sample frequency select pins when in master mode. In slave mode, the pin reverts to being a general purpose input.

MF3:CCLK - Control Data Clock in SM4, PIN 35(L), 29(Q).

In serial mode 4 this pin is the control port serial bit clock which latches data from CDIN on the falling edge, and outputs data onto CDOOUT on the rising edge.

MF4:DI4 - Parallel Digital Bit Input #4 in SM1/SM2, PIN 36(L), 30(Q).

In serial modes 1 and 2 this pin value is reflected in the DI4 bit in the sub-frame.

MF4:MA - Master Sub-Mode in SM3, PIN 36(L), 30(Q).

In serial mode 3 this pin selects either master or slave mode. When MF4:MA = 1, the codec is in master mode and outputs SSYNC and SCLK. When MF4:MA = 0, the codec is in slave mode and receives SSYNC and SCLK from an external source that must be frequency locked to CLKIN.

MF4:CCS - Control Data Chip Select in SM4, PIN 36(L), 30(Q).

In serial mode 4 this pin is the control port chip select signal. When low, the control port data is clocked in CDIN and status data is output on CDOU. When CCS goes high, control data is latched internally. This data remains active until new data is clocked in. The control port may also be asynchronous to the audio data port.

MF5:DO2 - Parallel Digital Bit Output #2 in SM1/SM2/SM3, PIN 38(L), 32(Q).

In serial modes 1, 2, and 3 this pin reflects the value of the DO2 bit in the sub-frame.

MF5:INT - Interrupt in SM4, PIN 38(L), 32(Q).

In serial mode 4 this pin is an active low interrupt signal that is maskable using the MSK bit in the control port serial data stream. INT is an open-collector output and requires an external pull-up resistor. Assuming the mask bit is not set, and interrupt is triggered by a change in ADV or DI1, or a rising edge on LCL or RCL, or a exiting an SCLK out of range condition (Error = 3)

MF6:DI2 - Parallel Digital Bit Input #2 in SM1/SM2/SM3, PIN 34(L), 28(Q).

In serial modes 1, 2, and 3 this pin value is reflected in the DI2 bit of the sub-frame.

MF6:F1 - Format Bit 1 in SM4, PIN 34(L), 28(Q).

In serial mode 4 this pin is a format bit and is used as one of three sample frequency select pins when in master mode. In slave mode, MF6:F1 helps determine the number of sub-frames within a frame.

MF7:SFS1 - Sub-Frame Select 1 in SM1/SM2/SM3/SM4-SL, PIN 31(L), 25(Q).

In serial modes 1, 2, and 3, MF7:SFS1 helps select the sub-frame that this particular CS4216 is allocated. In slave sub-mode of serial mode 4, this pin is one of two pins used as a sub-frame select when MF6:F1 = 1 (128-bit frames). When MF6:F1 = 0, this pin is used to select the frame sizes of 32 or 64 bits.

MF7:F2 - Format Bit 2 in SM4-MA, PIN 31(L), 25(Q).

In master sub-mode of serial mode 4, this pin is used as one of three sample frequency select pins.

MF8:SFS2 - Sub-Frame Select 2 in SM1/SM2/SM3/SM4-SL, PIN 30(L), 24(Q).

In serial modes 1, 2, 3, and slave sub-mode of 4, MF8:SFS2 helps select the sub-frame that this particular CS4216 is allocated.

MF8:F3 - Format Bit 3 in SM4-MA, PIN 30(L), 24(Q).

In master sub-mode of serial mode 4, this pin is a format bit and is one of three sample frequency select pins.

Miscellaneous**RESET - Reset Input, PIN 2(L), 40(Q).**

Resets the CS4216 into a known state, and must be initiated after power-up or power-down mode. Releasing RESET caused the CS4216 to initiate a calibration sequence. RESET should also be initiated when changing sample frequencies in any master sub-mode.

CLKIN - Master Clock, PIN 3(L), 41(Q).

CLKIN is the master clock that operates the internal logic. In serial mode 1, $CLKIN = 512 \times hFs$, where hFs is the highest sample frequency needed. Different sample frequencies are obtained by changing the ratio of SCLK to CLKIN. In serial mode 2, CLKIN is not used and must be tied low. In serial modes 3 and 4, CLKIN is $256 \times hFs$, where different sample frequencies are obtained by either changing the ratio of SCLK to CLKIN in slave mode, or changing the format pin values (F2-F0) in master mode.

4**PDN - Power Down, PIN 13(L), 7(Q).**

This pin, when low, causes the CS4216 to go into a power down state. RESET should be held low for 50 ms when exiting the power down state to allow time for the voltage reference to settle.

DII - Parallel Digital Bit Input #1, PIN 33(L), 27(Q).

This pin value is reflected in the DII bit in the sub-frame.

DO1 - Parallel Digital Bit Output #1, PIN 37(L), 31(Q).

This pin reflects the value of the DO1 bit in the sub-frame.

**NC - No Connection, PINS 6, 7, 8, 9, 10, 11, 12, 14, 17, 18, 19(L)
PINS 44, 1, 2, 3, 4, 5, 6, 8, 11, 12, 13(Q).**

These pins should be left floating with no trace attached to allow backwards compatibility with future revisions. They should not be used as a convenient path for signal traces.

PARAMETER DEFINITIONS**Resolution**

The number of bits in the input words to the DACs, and in the output words from the ADCs.

Differential Nonlinearity

The worst case deviation from the ideal codewidth. Units in LSB.

Total Dynamic Range

TDR is the ratio of the rms value of a full scale signal to the lowest obtainable noise floor. It is measured by comparing a full scale signal to the lowest noise floor possible in the codec (i.e. attenuation bits for the DACs at full attenuation). Units in dB.

Instantaneous Dynamic Range

IDR is the ratio of a full-scale rms signal to the rms noise available at any instant in time, without changing the input gain or output attenuation settings. It is measured using $S/(N+D)$ with a 1 kHz, -60 dB input signal, with 60 dB added to compensate for the small input signal. Use of a small input signal reduces the harmonic distortion components to insignificance when compared to the noise. Units in dB.

Total Harmonic Distortion

THD is the ratio of the rms value of a signal's first five harmonic components to the rms value of the signals fundamental component. THD is calculated using an input signal which is 3dB below typical full-scale, and is referenced to typical full-scale.

Interchannel Isolation

The amount of 1 kHz signal present on the output of the grounded input channel, with 1 kHz 0 dB signal present on the other channel. Units in dB.

Interchannel Gain Mismatch

For the ADCs, the difference in input voltage that generates the full scale code for each channel. For the DACs, the difference in output voltages for each channel with a full scale digital input. Units in dB.

Frequency Response

Worst case variation in output signal level versus frequency over the passband. Tested over the frequency band of 10 Hz to 20 kHz, with the sample frequency of 48 kHz. Units in dB.

Step Size

Typical delta between two adjacent gain or attenuation values. Units in dB.

Absolute Gain/Attenuation Step Error

The deviation of a gain or attenuation step from a straight line passing through the no-gain/attenuation value and the full-gain/attenuation value (i.e. end points). Units in dB.

Offset Error

For the ADCs, the deviation of the output code from the mid-scale with the selected input at REFBUF. For the DACs, the deviation of the output from REFBUF with mid-scale input code. Units in LSB's for the ADCs and volts for the DACs.

Out of Band Energy

The ratio of the rms sum of the energy from $0.46 \times F_s$ to $2.1 \times F_s$ compared to the rms full-scale signal value. Tested with 48 kHz F_s giving a out-of-band energy range of 22 kHz to 100 kHz.

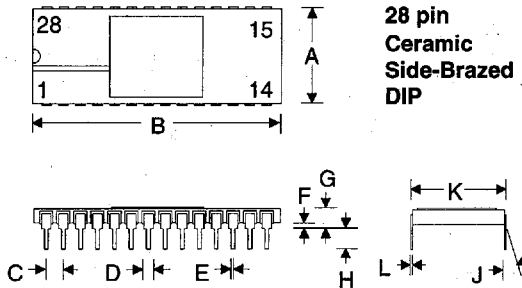
APPENDIX A

This data sheet describes version 1 of the CS4216. Therefore, this appendix is included to describe the differences between version 0 and version 1. This information is only useful for users that still have version 0 since version 1 devices will supplant the earlier version. The version number is contained in the serial data line, bits 29 - 32 on SDOUT in SM1-SM3 and, bits 17 - 20 on CDOUT in SM4. The version number can also be identified by the revision letter stamped on the top of the actual chip. The revision letter immediately precedes the data code on the second line of the package marking (See *General Information* section of the Crystal Data Book). Version 0 corresponds to chip revision A, and version 1 corresponds to chip revisions B, and C. The functionally and performance of revisions B and C are identical. Likewise, future chip revisions (i.e. D, E, F, . . .) may still be version 1 since the version number only changes if there is a software change to the part.

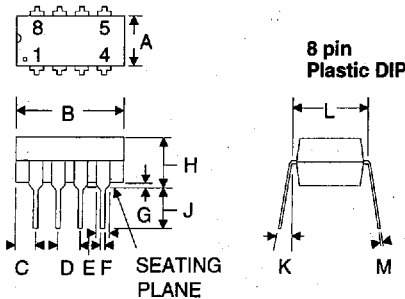
Functional Differences Between Version 0 (Rev. A) and Version 1 (Revs. B, C)

1. In version 0, serial mode 4 (SM4) does not exist; the SMODE3 pin is a no connect. In version 1 the SMODE3 pin contains an internal pull-down resistor making this version backwards compatible with version 0 sockets.
2. SSYNC on version 0 must be ONLY one SCLK period high in SM3 or 2 SCLK periods high in SM1 and SM2 to indicate the start of a frame. Also, on version 0 in SM1 or SM2, SSYNC must be EXACTLY one SCLK period high, at the beginning of each word. In version 1, SSYNC can be high for an arbitrary number of SCLKs beyond the one in SM3 or two in SM1 and SM2. Also in SM1 and SM2, the one-SCLK-wide SSYNCs at each word are not needed. In version 1, SM3 and SM4, the codec only looks for a low-to-high edge of SSYNC to start a frame; in SM1 and SM2 a low-to-high edge of SSYNC, being high for two SCLK periods, starts a frame.

MECHANICAL DATA



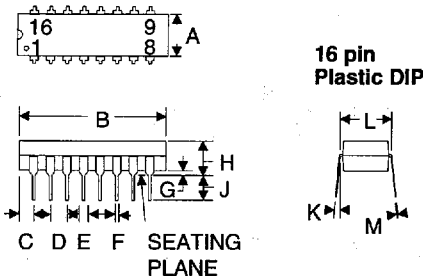
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	14.73	15.34	0.580	0.604
B	35.20	35.92	1.386	1.414
C	2.54 BSC		0.100 BSC	
D	0.76	1.40	0.030	0.055
E	0.38	0.53	0.015	0.021
F	1.02	1.52	0.040	0.060
G	2.79	4.32	0.110	0.170
H	2.54	4.57	0.100	0.180
J	-	10°	-	10°
K	14.99	15.49	0.590	0.610
L	0.20	0.30	0.008	0.012



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	9.14	10.2	0.360	0.400
C	0.38	1.52	0.015	0.060
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

NOTES:

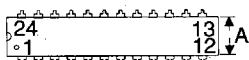
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



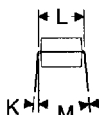
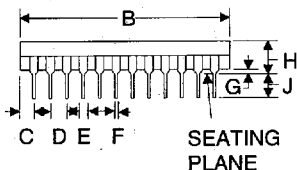
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	18.80	19.30	0.740	0.760
C	1.32	2.89	0.015	0.035
D	2.54 BSC		0.100 BSC	
E	1.02	1.78	0.040	0.070
F	0.38	0.53	0.015	0.021
G	0.51	1.02	0.020	0.040
H	3.81	5.08	0.150	0.200
J	2.92	3.43	0.115	0.135
K	0°	10°	0°	10°
L	7.62BSC		0.300BSC	
M	0.20	0.38	0.008	0.015

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13MM (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.



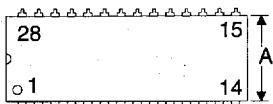
**24 pin
Plastic
Skinny DIP**



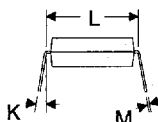
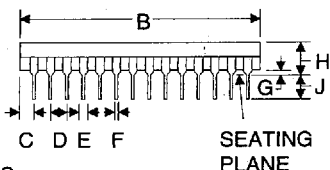
NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.60	0.240	0.260
B	31.37	32.13	1.235	1.265
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	4.57	0.155	0.180
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	7.62 BSC		0.300 BSC	
M	0.20	0.38	0.008	0.015



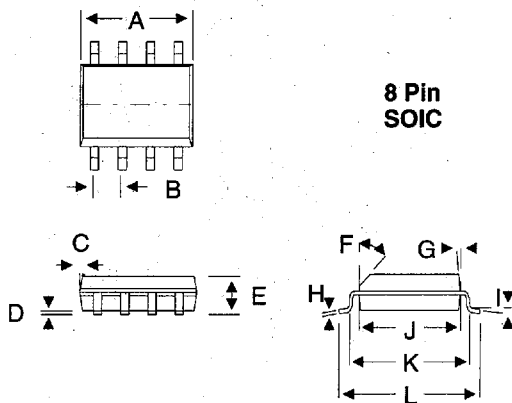
**28 pin
Plastic DIP**



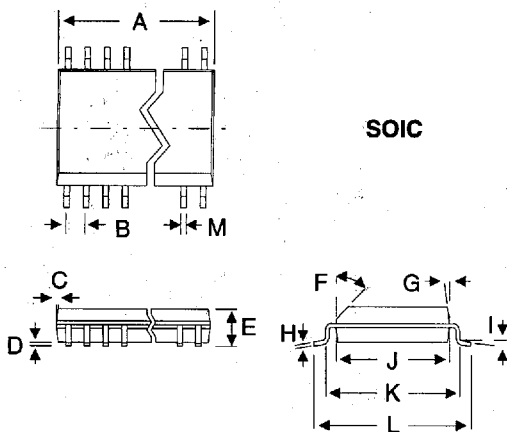
NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25MM (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.72	14.22	0.540	0.560
B	36.45	37.21	1.435	1.465
C	1.65	2.16	0.065	0.085
D	2.54 BSC		0.100 BSC	
E	1.02	1.52	0.040	0.060
F	0.36	0.56	0.014	0.022
G	0.51	1.02	0.020	0.040
H	3.94	5.08	0.155	0.200
J	2.92	3.43	0.115	0.135
K	0°	15°	0°	15°
L	15.24 BSC		0.600 BSC	
M	0.20	0.38	0.008	0.015



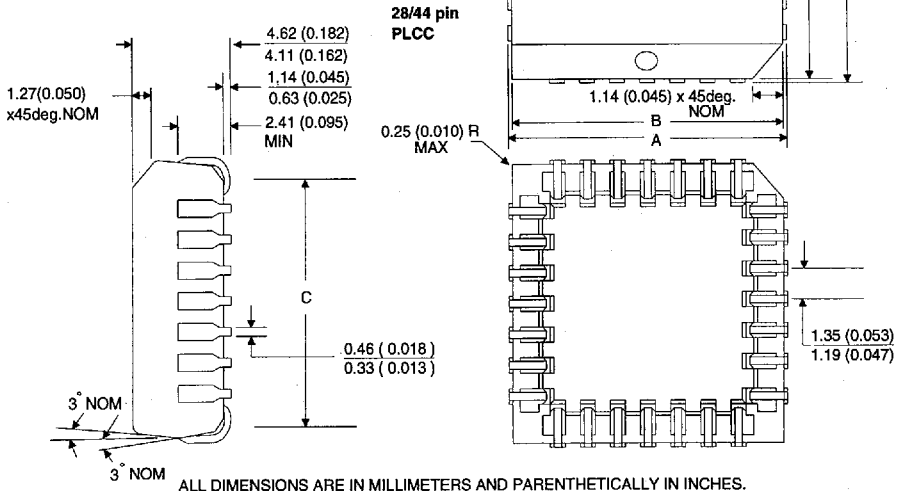
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.25	5.30	0.207	0.209
B	1.27 TYP		0.050 TYP	
C	7° NOM		7° NOM	
D	0.120	0.180	0.005	0.007
E	1.80	1.86	0.071	0.073
F	45° NOM		45° NOM	
G	7° NOM		7° NOM	
H	0.195	0.205	0.0078	0.0082
I	2°	4°	2°	4°
J	-	-	-	-
K	6.57	6.63	0.259	0.261
L	7.85	7.95	0.308	0.312



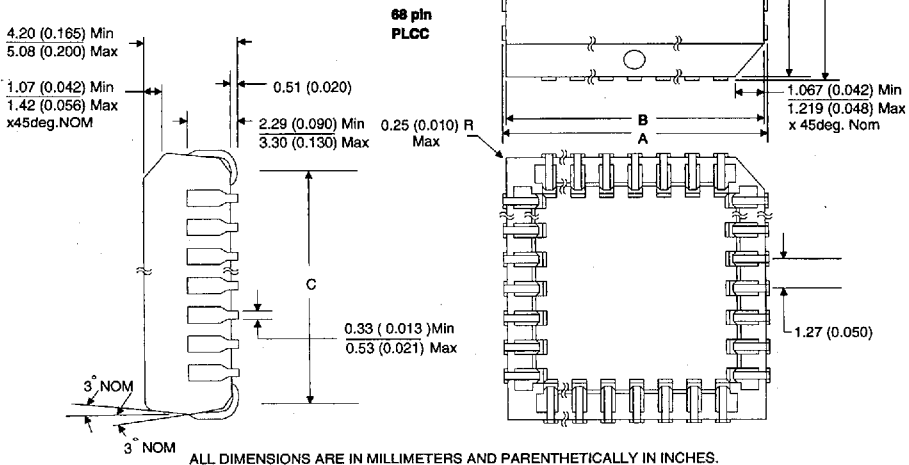
pins	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
16	9.91	10.41	0.390	0.410
20	12.45	12.95	0.490	0.510
24	14.99	15.50	0.590	0.610
28	17.53	18.03	0.690	0.710

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	see table above			
B	1.27	BSC	0.050	BSC
C	7° NOM		7° NOM	
D	0.127	0.330	0.005	0.013
E	2.41	2.67	0.095	0.105
F	45° NOM		45° NOM	
G	7° NOM		7° NOM	
H	0.203	0.381	0.008	0.015
I	2°	8°	2°	8°
J	7.42	7.59	0.292	0.298
K	8.76	9.02	0.345	0.355
L	10.16	10.67	0.400	0.420
M	0.33	0.51	0.013	0.020

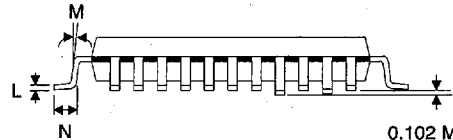
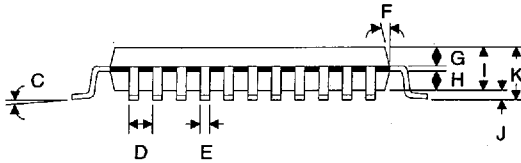
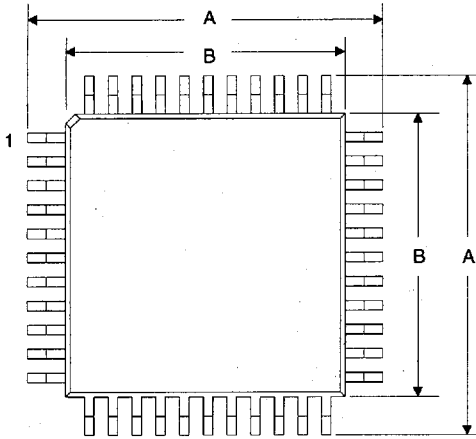
NO. OF TERMINAL	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
28	12.32 (0.485)	12.57 (0.495)	11.43 (0.450)	11.58 (0.456)	9.91 (0.390)	10.92 (0.430)
44	17.40 (0.685)	17.65 (0.695)	16.51 (0.650)	16.66 (0.656)	14.98 (0.590)	16.00 (0.630)



	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
68	25.02 (0.985)	25.27 (0.995)	24.13 (0.950)	24.33 (0.958)	22.61 (0.890)	23.62 (0.930)

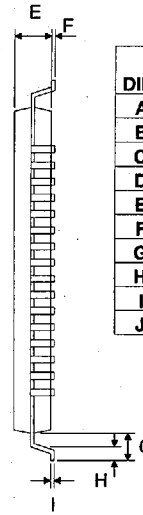
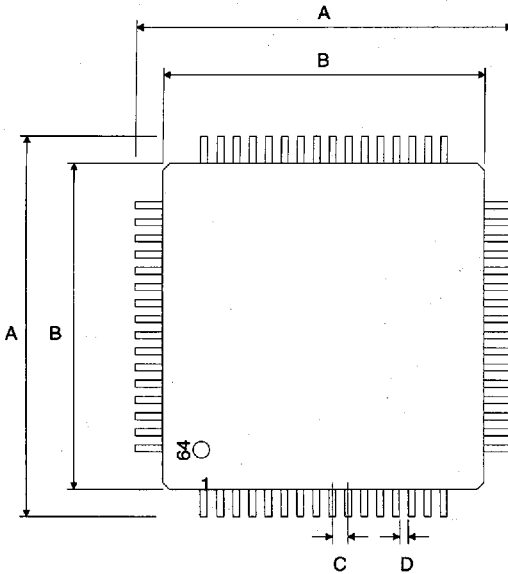


44 PIN QUAD FLATPACK

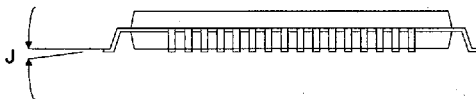


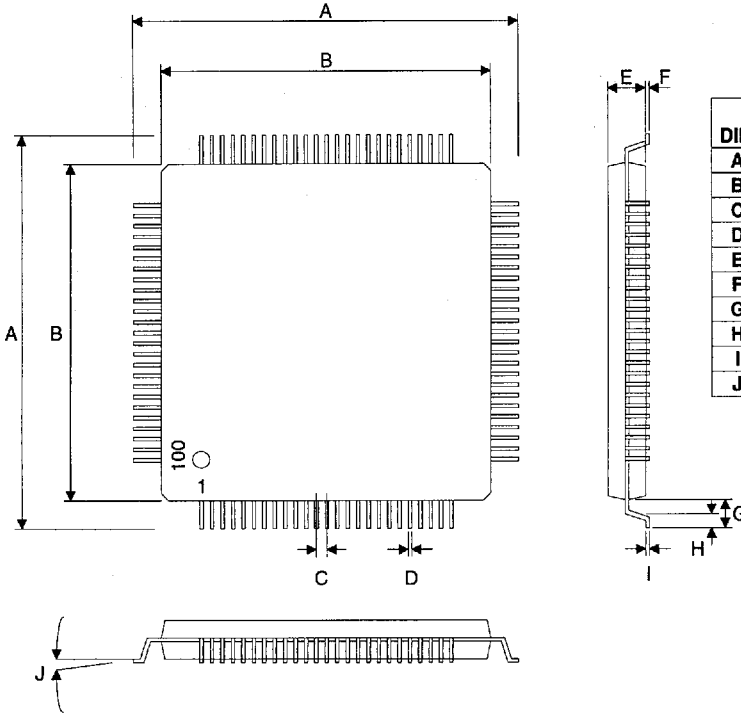
0.102 MAX
Lead Coplanarity

44 Pin TQFP				
1.4 mm Package Thickness				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	11.75	12.25	0.463	0.482
B	9.90	10.10	0.390	0.398
C	0°	7°	0°	7°
D	0.80 BSC		0.031 BSC	
E	0.35 BSC		0.014 BSC	
F		12°		12°
G	0.54	0.74	0.021	0.029
H	0.54	0.74	0.021	0.029
I	1.35	1.50	0.053	0.059
J	0.05		0.002	
K		1.60		0.063
L		0.17		0.007
M	2°	10°	2°	10°
N	0.35	0.65	0.014	0.026



64 Pin TQFP				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.00 BSC		0.472 BSC	
B	10.00 BSC		0.393 BSC	
C	0.50 BSC		0.020 BSC	
D	0.14	0.30	0.005	0.012
E	0.95	1.12	0.037	0.044
F	0.05	0.15	0.002	0.006
G	1.00 BSC		0.039 BSC	
H	0.45	0.75	0.018	0.030
I	0.09	0.18	0.003	0.007
J	0°	7°	0°	7°





100-pin TQFP

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.75	16.25	0.620	0.640
B	13.90	14.10	0.547	0.555
C	0.50 BSC		0.020 BSC	
D	0.10	0.20	0.004	0.012
E	1.25	1.55	0.049	0.061
F	0.00	0.20	0.000	0.008
G	1.00 BSC		0.039 BSC	
H	0.35	0.65	0.014	0.026
I	0.077	0.177	0.003	0.007
J	0°	10°	0°	10°