

## 512K x 16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

FEBRUARY 2005

### FEATURES

- High-speed access time: 45ns, 55ns
- CMOS low power operation
  - 36 mW (typical) operating
  - 12  $\mu$ W (typical) CMOS standby
- TTL compatible interface levels
- Single power supply
  - 1.65V--2.2V  $V_{DD}$  (62WV51216ALL)
  - 2.5V--3.6V  $V_{DD}$  (62WV51216BLL)
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Lead-free available

### DESCRIPTION

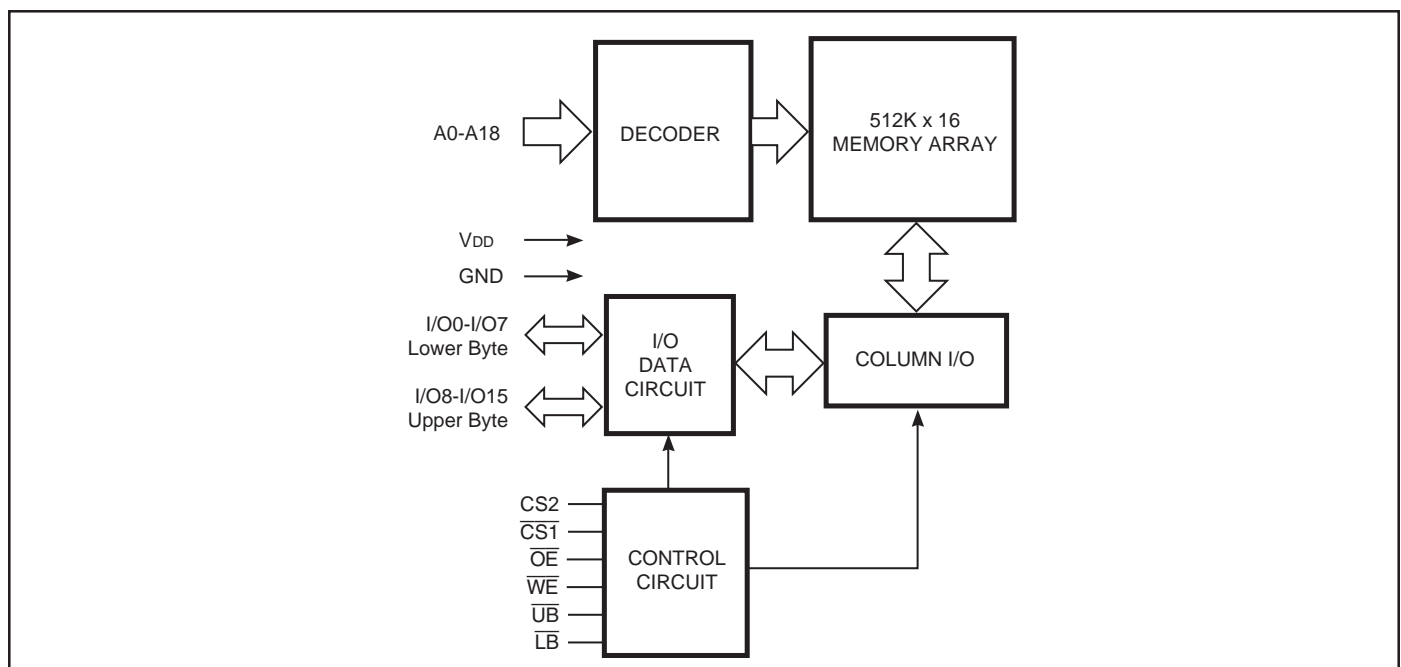
The *ISSI* IS62WV51216ALL/IS62WV51216BLL are high-speed, 8M bit static RAMs organized as 512K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When  $\overline{CS1}$  is HIGH (deselected) or when CS2 is LOW (deselected) or when  $\overline{CS1}$  is LOW, CS2 is HIGH and both  $\overline{LB}$  and  $\overline{UB}$  are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory. A data byte allows Upper Byte ( $\overline{UB}$ ) and Lower Byte ( $\overline{LB}$ ) access.

The IS62WV51216ALL and IS62WV51216BLL are packaged in the JEDEC standard 48-pin mini BGA (7.2mm x 8.7mm) and 44-Pin TSOP (TYPE II).

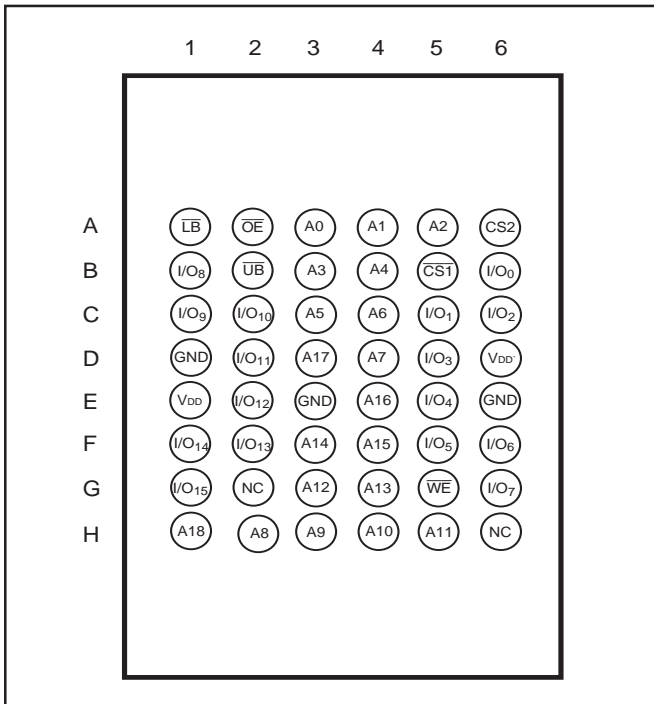
### FUNCTIONAL BLOCK DIAGRAM



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**PIN CONFIGURATIONS**

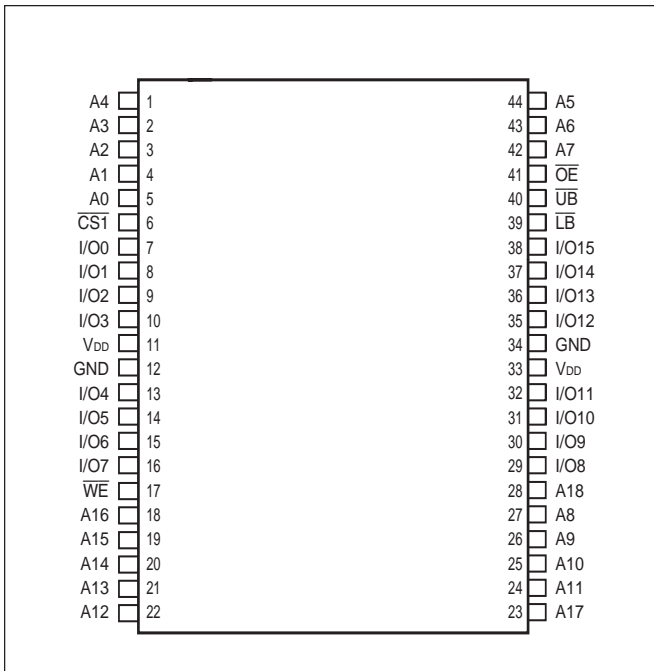
**48-Pin mini BGA (7.2mm x 8.7mm)**



**PIN DESCRIPTIONS**

A0-A18	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CS1}$ , CS2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
VDD	Power
GND	Ground

**44-Pin TSOP (Type II)**



## TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN		V <sub>DD</sub> Current
							I/O0-I/O7	I/O8-I/O15	
Not Selected	X	H	X	X	X	X	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
	X	X	L	X	X	X	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
	X	X	X	X	H	H	High-Z	High-Z	I <sub>SB1</sub> , I <sub>SB2</sub>
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	I <sub>CC</sub>
	H	L	H	H	X	L	High-Z	High-Z	I <sub>CC</sub>
Read	H	L	H	L	L	H	DOUT	High-Z	I <sub>CC</sub>
	H	L	H	L	H	L	High-Z	DOUT	
	H	L	H	L	L	L	DOUT	DOUT	
Write	L	L	H	X	L	H	DIN	High-Z	I <sub>CC</sub>
	L	L	H	X	H	L	High-Z	DIN	
	L	L	H	X	L	L	DIN	DIN	

OPERATING RANGE (V<sub>DD</sub>)

Range	Ambient Temperature	IS62WV51216ALL (70ns)	IS62WV51216BLL (55ns, 70ns)	IS62WV51216BLL (45ns)
Commercial	0°C to +70°C	1.65V - 2.2V	2.5V - 3.6V	3.0 - 3.6V
Industrial	-40°C to +85°C	1.65V - 2.2V	2.5V - 3.6V	

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.2 to V <sub>DD</sub> +0.3	V
T <sub>BIAS</sub>	Temperature Under Bias	-40 to +85	°C
V <sub>DD</sub>	V <sub>DD</sub> Related to GND	-0.2 to +3.8	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

**Note:**

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC ELECTRICAL CHARACTERISTICS** (Over Operating Range)

Symbol	Parameter	Test Conditions	V <sub>DD</sub>	Min.	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA	1.65-2.2V	1.4	—	V
		I <sub>OH</sub> = -1 mA	2.5-3.6V	2.2	—	V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA	1.65-2.2V	—	0.2	V
		I <sub>OL</sub> = 2.1 mA	2.5-3.6V	—	0.4	V
V <sub>IH</sub>	Input HIGH Voltage		1.65-2.2V	1.4	V <sub>DD</sub> + 0.2	V
			2.5-3.6V	2.2	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub> <sup>(1)</sup>	Input LOW Voltage		1.65-2.2V	-0.2	0.4	V
			2.5-3.6V	-0.2	0.6	V
I <sub>LI</sub>	Input Leakage	GND ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>		-1	1	μA
I <sub>LO</sub>	Output Leakage	GND ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> , Outputs Disabled		-1	1	μA

**Notes:**

1. V<sub>IL</sub> (min.) = -1.0V for pulse width less than 10 ns.

**CAPACITANCE<sup>(1)</sup>**

Symbol	Parameter	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	8	pF
C <sub>OUT</sub>	Input/Output Capacitance	V <sub>OUT</sub> = 0V	10	pF

**Note:**

1. Tested initially and after any design or process changes that may affect these parameters.

**AC TEST CONDITIONS**

Parameter	62WV51216ALL (Unit)	62WV51216BLL (Unit)
Input Pulse Level	0.4V to V <sub>DD</sub> -0.2	0.4V to V <sub>DD</sub> -0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V <sub>REF</sub>	V <sub>REF</sub>
Output Load	See Figures 1 and 2	See Figures 1 and 2

	62WV51216ALL (1.65V - 2.2V)	62WV51216BLL (2.5V - 3.6V)
R1(Ω)	3070	1029
R2(Ω)	3150	1728
V <sub>REF</sub>	0.9V	1.5V
V <sub>TM</sub>	1.8V	2.8V

**AC TEST LOADS**

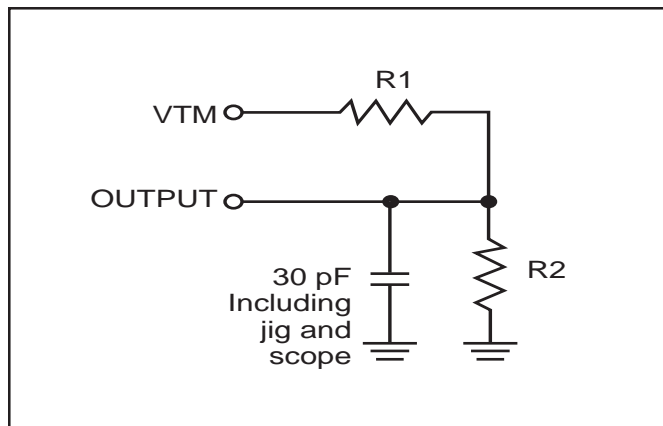


Figure 1

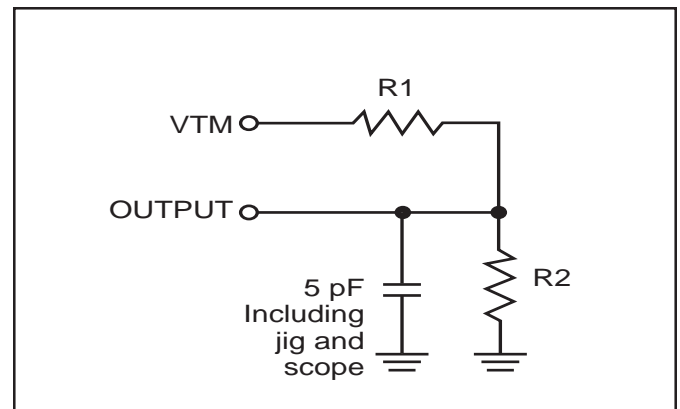


Figure 2

IS62WV51216ALL, POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 70	Unit
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max.,	Com.	20	mA
		I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Ind.	25	
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max., $\overline{CS1} = 0.2V$	Com.	4	mA
		$\overline{WE} = V_{DD} - 0.2V$	Ind.	4	
		CS2 = V <sub>DD</sub> - 0.2V, f = 1MHz			
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max.,	Com.	0.3	mA
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	Ind.	0.3	
		$\overline{CS1} = V_{IH}$ , CS2 = V <sub>IL</sub> , f = 1 MHz			
	<b>OR</b>				
	ULB Control	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IL}$ , f = 0, $\overline{UB} = V_{IH}$ , $\overline{LB} = V_{IH}$			
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max.,	Com.	15	μA
		$\overline{CS1} \geq V_{DD} - 0.2V$ ,	Ind.	21	
		CS2 ≤ 0.2V,	typ. <sup>(1)</sup>	3	
		V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0			
	<b>OR</b>				
	ULB Control	V <sub>DD</sub> = Max., $\overline{CS1} = V_{IL}$ , CS2 = V <sub>IH</sub> V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0; $\overline{UB}/\overline{LB} = V_{DD} - 0.2V$			

**Note:**

1. Typical values are measured at V<sub>DD</sub> = 1.8V, T<sub>A</sub> = 25°C and not 100% tested.

IS62WV51216BLL, POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	Test Conditions		Max.	Max.	Max.	Unit
				45	55	70	
I <sub>CC</sub>	V <sub>DD</sub> Dynamic Operating Supply Current	V <sub>DD</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>	Com.	35	30	25	mA
			Ind.	40	35	30	
I <sub>CC1</sub>	Operating Supply Current	V <sub>DD</sub> = Max., $\overline{CS1} = 0.2V$ $\overline{WE} = V_{DD} - 0.2V$ CS2 = V <sub>DD</sub> - 0.2V, f = 1MHz	Com.	5	5	5	mA
			Ind.	5	5	5	
I <sub>SB1</sub>	TTL Standby Current (TTL Inputs)	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IH}$ , CS2 = V <sub>IL</sub> , f = 1 MHz	Com.	0.3	0.3	0.3	mA
			Ind.	0.3	0.3	0.3	
	<b>OR</b>						
	ULB Control	V <sub>DD</sub> = Max., V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> $\overline{CS1} = V_{IL}$ , f = 0, $\overline{UB} = V_{IH}$ , $\overline{LB} = V_{IH}$					
I <sub>SB2</sub>	CMOS Standby Current (CMOS Inputs)	V <sub>DD</sub> = Max., $\overline{CS1} \geq V_{DD} - 0.2V$ , CS2 ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0	Com.	20	20	20	μA
			Ind. typ. <sup>(2)</sup>	25	25	25	
	<b>OR</b>						
	ULB Control	V <sub>DD</sub> = Max., $\overline{CS1} = V_{IL}$ , CS2 = V <sub>IH</sub> V <sub>IN</sub> ≥ V <sub>DD</sub> - 0.2V, or V <sub>IN</sub> ≤ 0.2V, f = 0; $\overline{UB}/\overline{LB} = V_{DD} - 0.2V$					

**Note:**

- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
- Typical values are measured at V<sub>DD</sub> = 3.0V, T<sub>A</sub> = 25°C and not 100% tested.

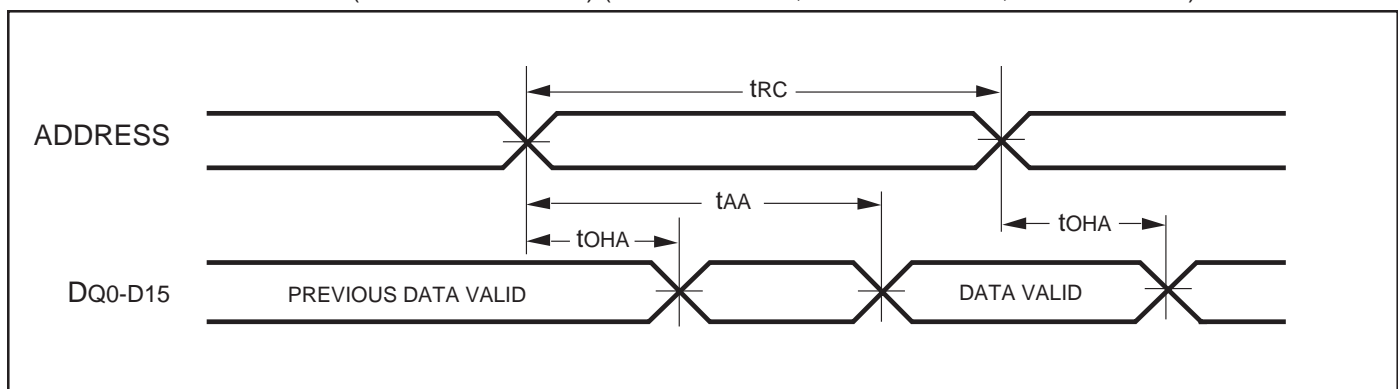
READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

Symbol	Parameter	45 ns		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read Cycle Time	45	—	55	—	70	—	ns
t <sub>AA</sub>	Address Access Time	—	45	—	55	—	70	ns
t <sub>OHA</sub>	Output Hold Time	10	—	10	—	10	—	ns
t <sub>ACS1</sub> /t <sub>ACS2</sub>	$\overline{\text{CS1}}$ /CS2 Access Time	—	45	—	55	—	70	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ Access Time	—	20	—	25	—	35	ns
t <sub>HZOE</sub> <sup>(2)</sup>	$\overline{\text{OE}}$ to High-Z Output	—	15	—	20	—	25	ns
t <sub>LZOE</sub> <sup>(2)</sup>	$\overline{\text{OE}}$ to Low-Z Output	5	—	5	—	5	—	ns
t <sub>HZCS1</sub> /t <sub>HZCS2</sub> <sup>(2)</sup>	$\overline{\text{CS1}}$ /CS2 to High-Z Output	0	15	0	20	0	25	ns
t <sub>LZCS1</sub> /t <sub>LZCS2</sub> <sup>(2)</sup>	$\overline{\text{CS1}}$ /CS2 to Low-Z Output	10	—	10	—	10	—	ns
t <sub>BA</sub>	$\overline{\text{LB}}$ , $\overline{\text{UB}}$ Access Time	—	45	—	55	—	70	ns
t <sub>HZB</sub>	$\overline{\text{LB}}$ , $\overline{\text{UB}}$ to High-Z Output	0	15	0	20	0	25	ns
t <sub>LZB</sub>	$\overline{\text{LB}}$ , $\overline{\text{UB}}$ to Low-Z Output	0	—	0	—	0	—	ns

## Notes:

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V<sub>DD</sub>-0.2V/0.4V to V<sub>DD</sub>-0.3V and output loading specified in Figure 1.
- Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

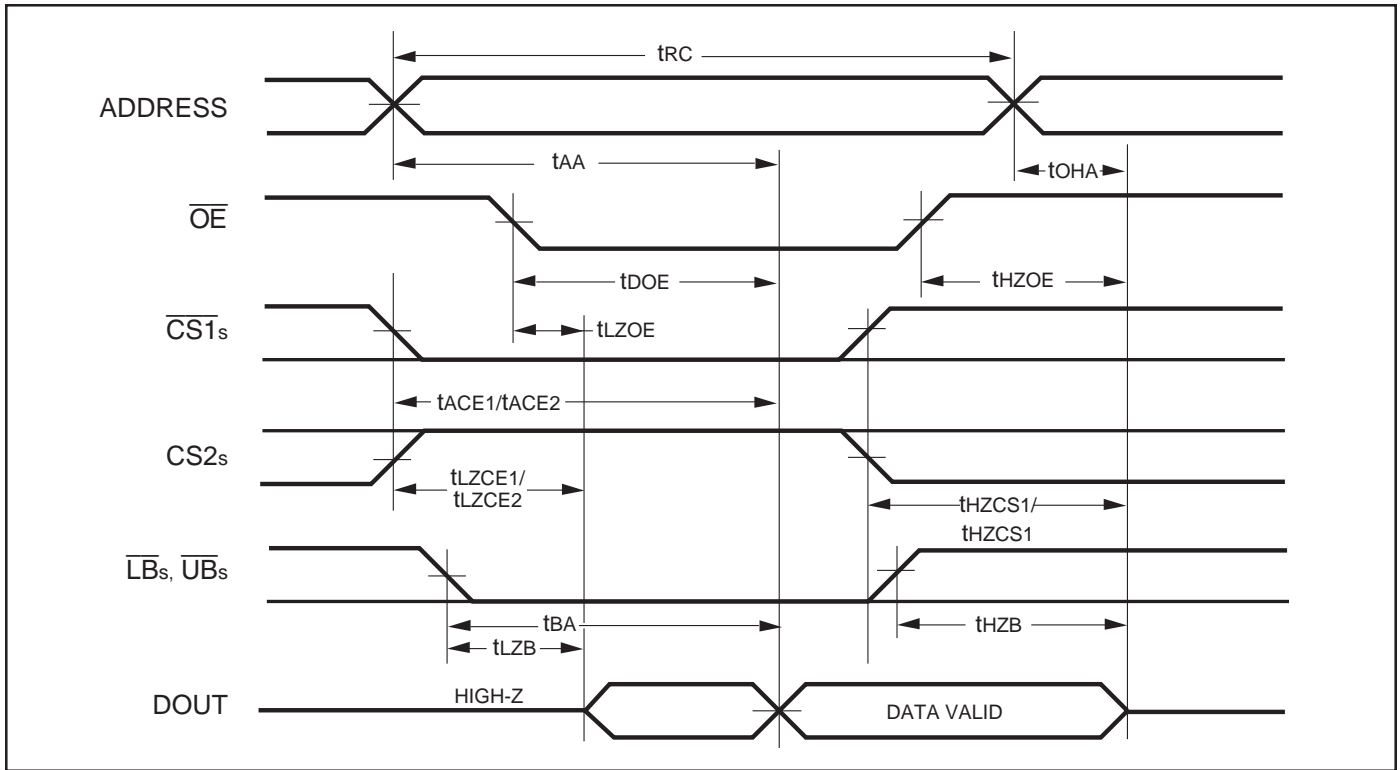
## AC WAVEFORMS

READ CYCLE NO. 1<sup>(1,2)</sup> (Address Controlled) ( $\overline{\text{CS1}} = \overline{\text{OE}} = V_{\text{IL}}$ , CS2 =  $\overline{\text{WE}} = V_{\text{IH}}$ ,  $\overline{\text{UB}}$  or  $\overline{\text{LB}} = V_{\text{IL}}$ )



AC WAVEFORMS

READ CYCLE NO. 2<sup>(1,3)</sup> ( $\overline{CS1}$ , CS2,  $\overline{OE}$ , AND  $\overline{UB}/\overline{LB}$  Controlled)



Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CS1}$ ,  $\overline{UB}$ , or  $\overline{LB} = V_{IL}$ .  $CS2 = \overline{WE} = V_{IH}$ .
3. Address is valid prior to or coincident with  $\overline{CS1}$  LOW transition.

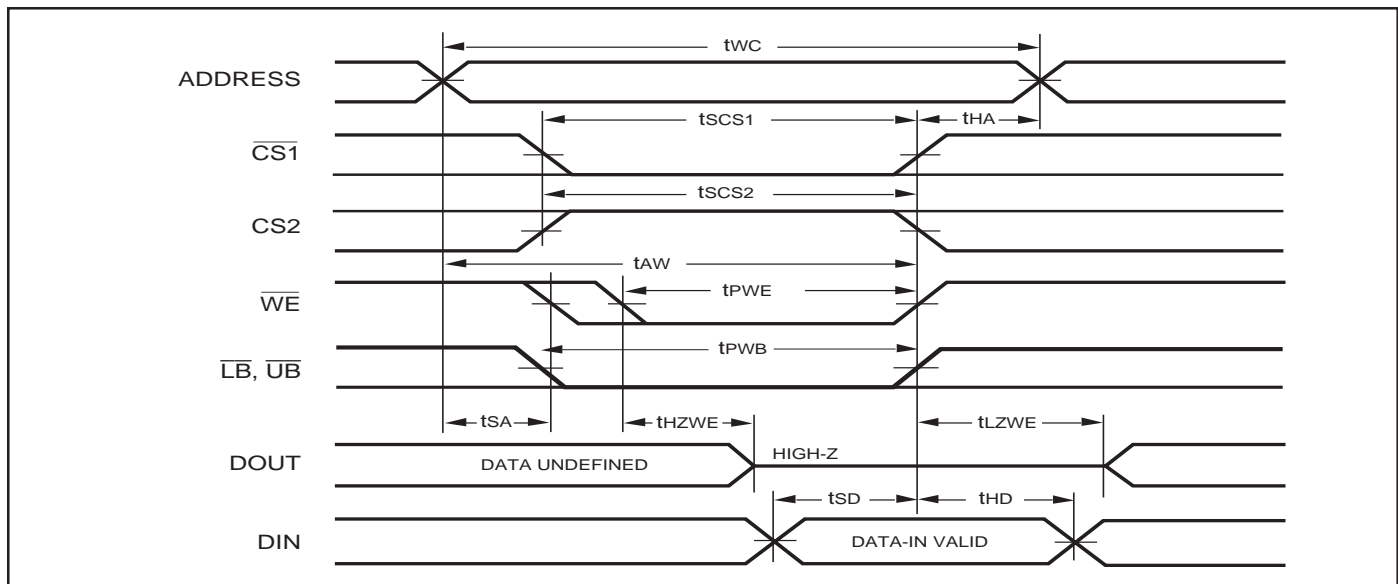
WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup> (Over Operating Range)

Symbol	Parameter	45ns		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{WC}$	Write Cycle Time	45	—	55	—	70	—	ns
$t_{SCS1}/t_{SCS2}$	$\overline{CS1}/CS2$ to Write End	35	—	45	—	60	—	ns
$t_{AW}$	Address Setup Time to Write End	35	—	45	—	60	—	ns
$t_{HA}$	Address Hold from Write End	0	—	0	—	0	—	ns
$t_{SA}$	Address Setup Time	0	—	0	—	0	—	ns
$t_{PWB}$	$\overline{LB}$ , $\overline{UB}$ Valid to End of Write	35	—	45	—	60	—	ns
$t_{PWE}^{(4)}$	$\overline{WE}$ Pulse Width	35	—	40	—	50	—	ns
$t_{SD}$	Data Setup to Write End	20	—	25	—	30	—	ns
$t_{HD}$	Data Hold from Write End	0	—	0	—	0	—	ns
$t_{HZWE}^{(3)}$	$\overline{WE}$ LOW to High-Z Output	—	20	—	20	—	30	ns
$t_{LZWE}^{(3)}$	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	5	—	ns

## Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to  $V_{DD}-0.2V/0.4V$  to  $V_{DD}-0.3V$  and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of  $\overline{CS1}$  LOW, CS2 HIGH and  $\overline{UB}$  or  $\overline{LB}$ , and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.
4.  $t_{PWE} > t_{HZWE} + t_{SD}$  when  $\overline{OE}$  is LOW.

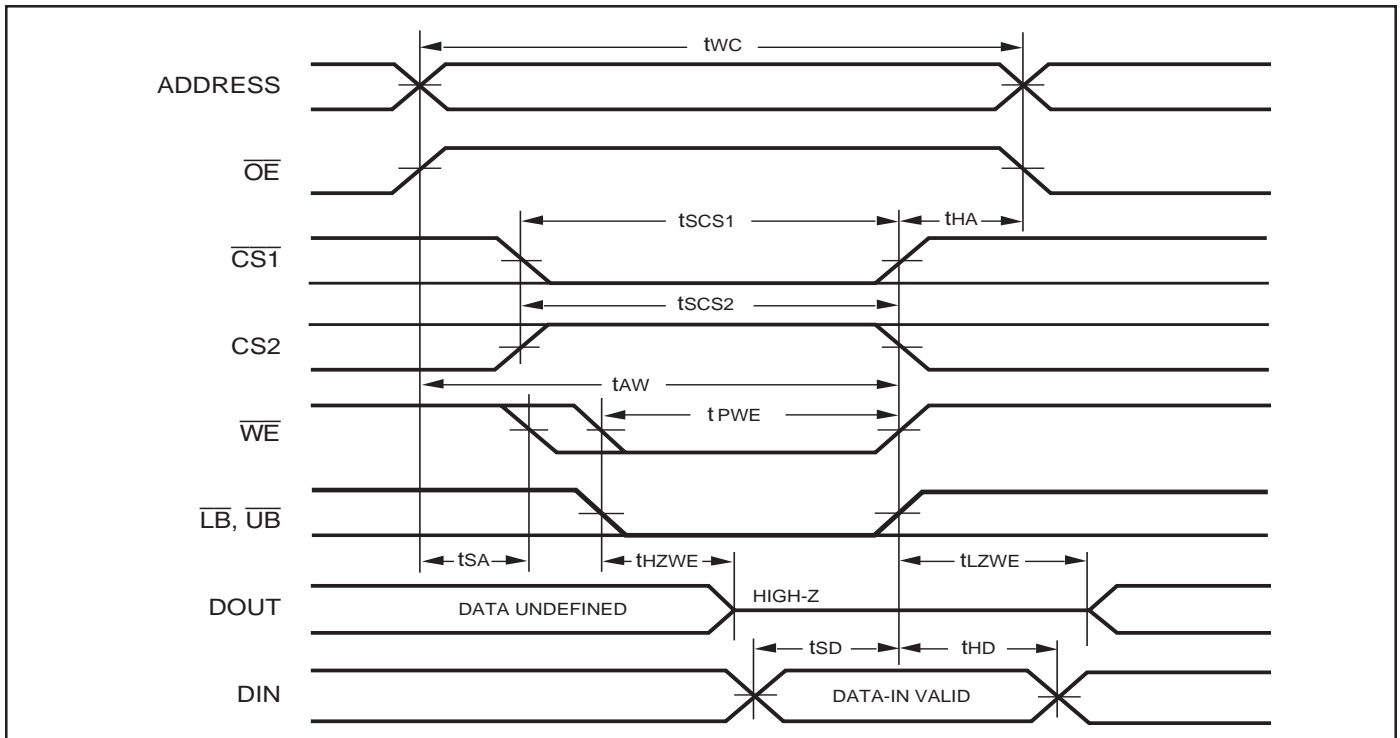
## AC WAVEFORMS

WRITE CYCLE NO. 1<sup>(1,2)</sup> ( $\overline{CS1}$  Controlled,  $\overline{OE} = \text{HIGH or LOW}$ )

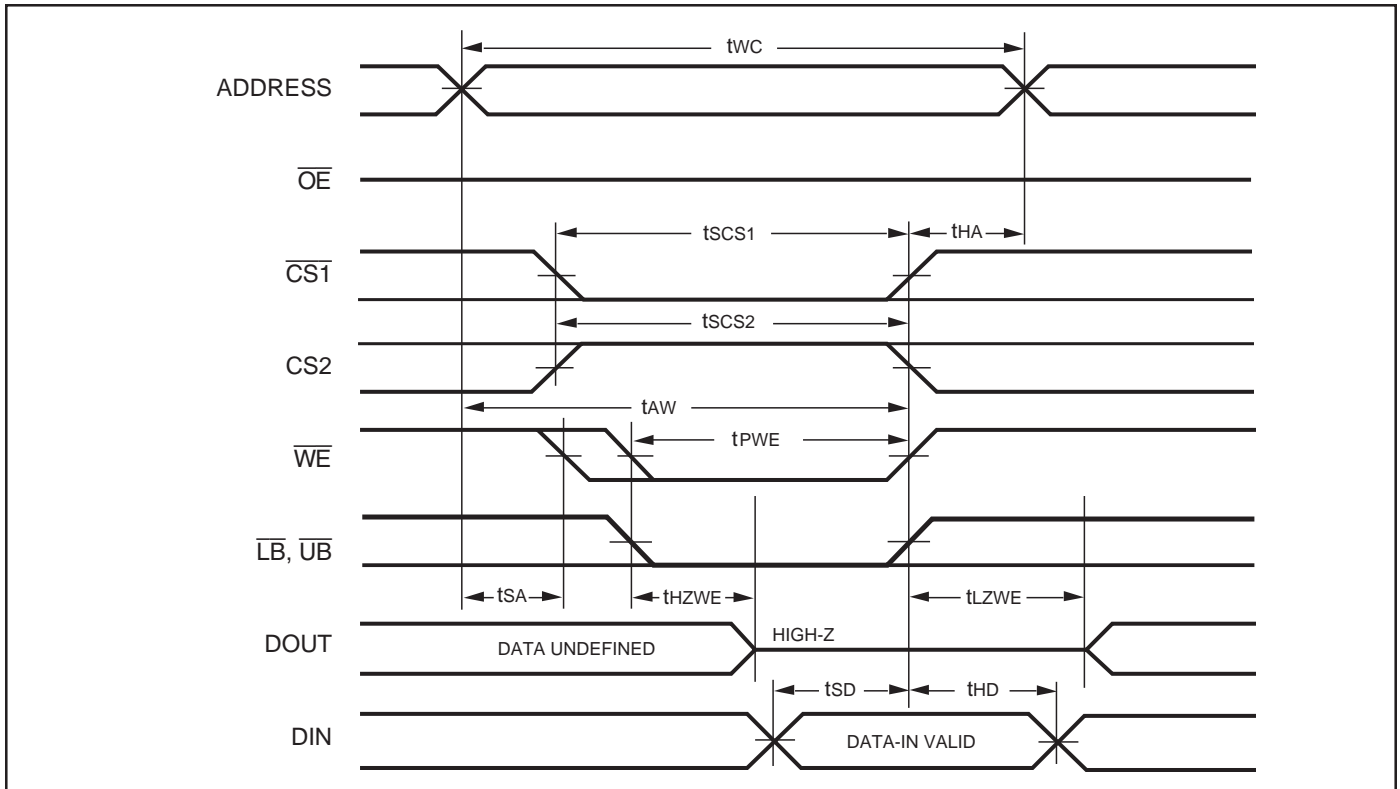
## Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the  $\overline{CS1}$ , CS2 and  $\overline{WE}$  inputs and at least one of the  $\overline{LB}$  and  $\overline{UB}$  inputs being in the LOW state.
2.  $WRITE = (\overline{CS1}) [ (\overline{LB}) = (\overline{UB}) ] (\overline{WE})$ .

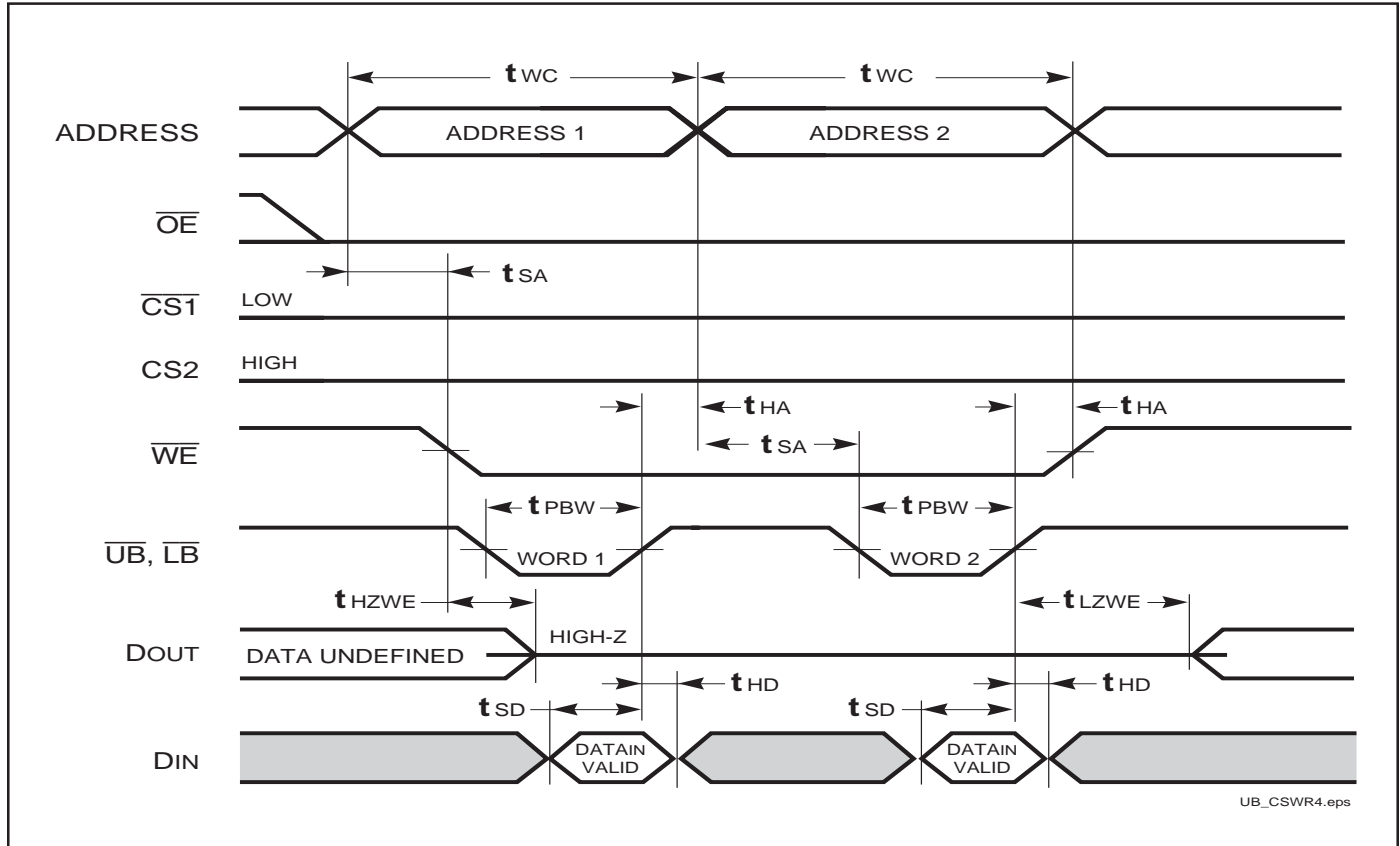
**WRITE CYCLE NO. 2** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is HIGH During Write Cycle)



**WRITE CYCLE NO. 3** ( $\overline{WE}$  Controlled:  $\overline{OE}$  is LOW During Write Cycle)



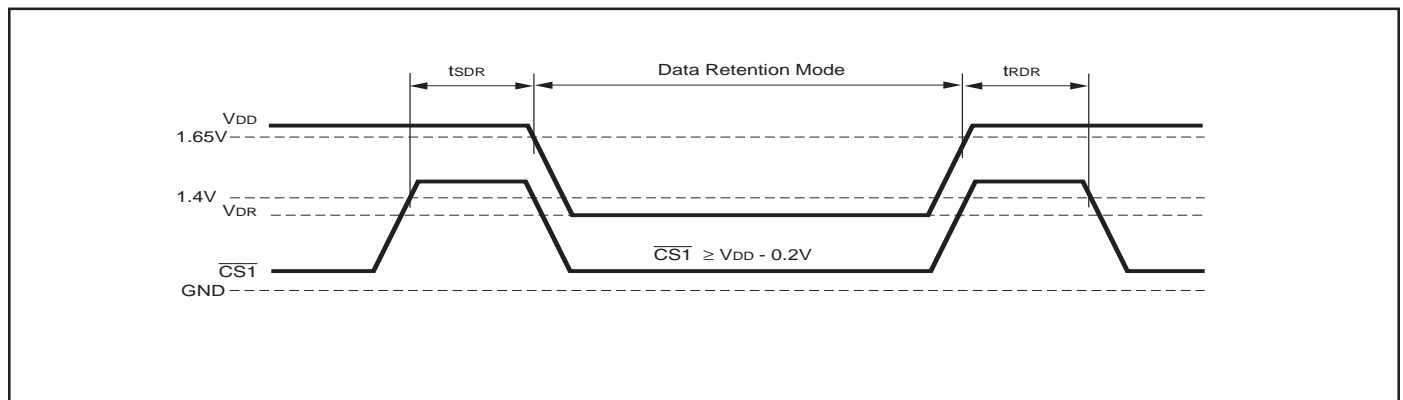
WRITE CYCLE NO. 4 ( $\overline{UB}/\overline{LB}$  Controlled)



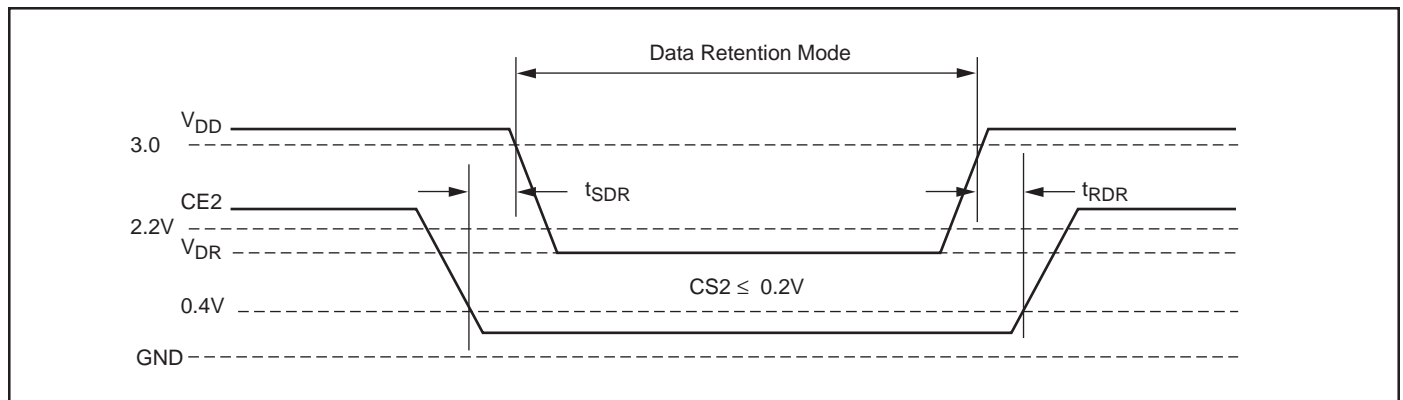
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	See Data Retention Waveform	1.2	3.6	V
I <sub>DR</sub>	Data Retention Current	V <sub>DD</sub> = 1.2V, $\overline{CS1} \geq V_{DD} - 0.2V$	—	20	μA
t <sub>SDR</sub>	Data Retention Setup Time	See Data Retention Waveform	0	—	ns
t <sub>RDR</sub>	Recovery Time	See Data Retention Waveform	t <sub>RC</sub>	—	ns

DATA RETENTION WAVEFORM ( $\overline{CS1}$  Controlled)



DATA RETENTION WAVEFORM (CS2 Controlled)



## ORDERING INFORMATION

IS62WV51216ALL (1.65V - 2.2V)

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
70	IS62WV51216ALL-70TI	TSOP-II
	IS62WV51216ALL-70BI	mini BGA (7.2mm x 8.7mm)
	IS62WV51216ALL-70XI	DIE

## ORDERING INFORMATION

IS62WV51216BLL (2.5V - 3.6V)

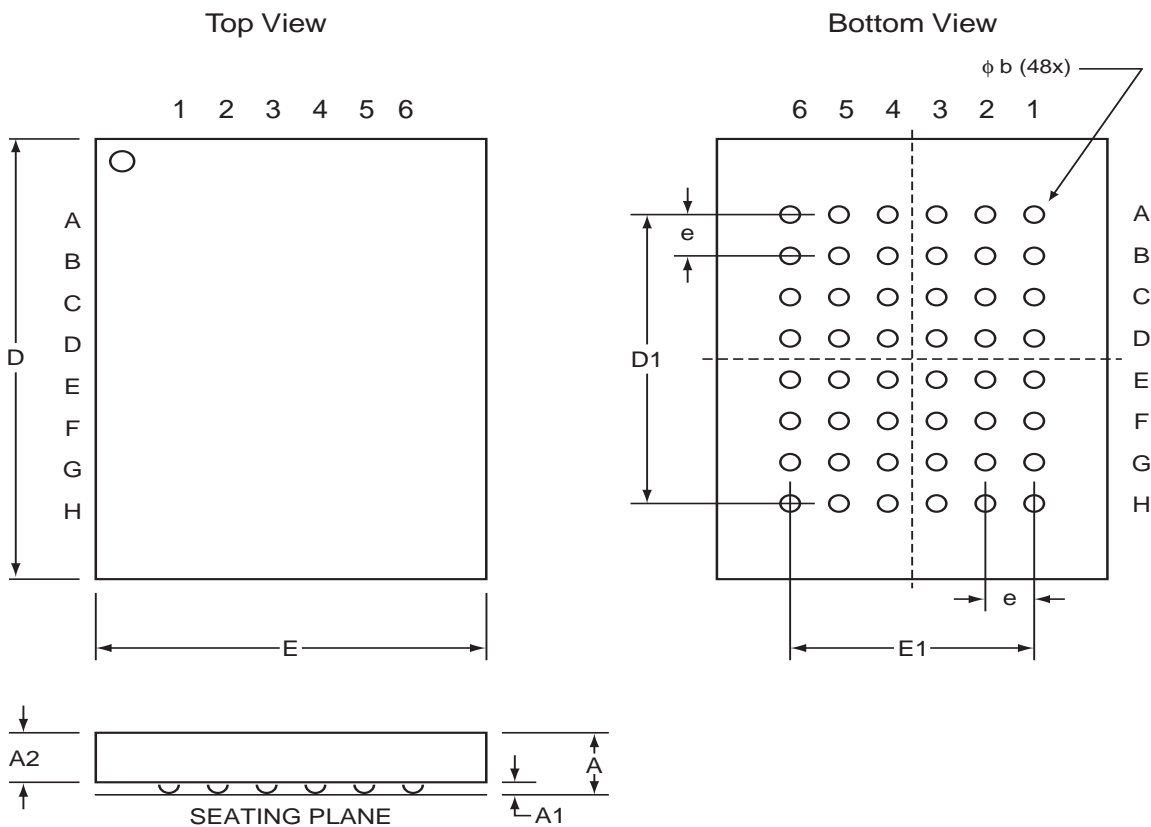
Commercial Range: 0°C to +70°C

Speed (ns)	Order Part No.	Package
45	IS62WV51216BLL-45B	mini BGA (7.2mm x 8.7mm)

Industrial Range: -40°C to +85°C

Speed (ns)	Order Part No.	Package
55	IS62WV51216BLL-55TI	TSOP-II
	IS62WV51216BLL-55TLI	TSOP-II, Lead-free
	IS62WV51216BLL-55BI	mini BGA (7.2mm x 8.7mm)
	IS62WV51216BLL-55BLI	mini BGA (7.2mm x 8.7mm), Lead-free
70	IS62WV51216BLL-70XI	DIE

**Mini Ball Grid Array**  
**Package Code: B (48-pin)**



**mBGA - 7.2mm x 8.7mm**

	MILLIMETERS			INCHES		
Sym.	Min.	Typ.	Max.	Min.	Typ.	Max.
N0.						
Leads		<b>48</b>				
A	—	—	1.20	—	—	0.047
A1	0.24	—	0.30	0.009	—	0.012
A2	0.60	—	—	0.024	—	—
D	8.60	8.70	8.80	0.339	0.343	0.346
D1		5.25BSC			0.207BSC	
E	7.10	7.20	7.30	0.280	0.283	0.287
E1		3.75BSC			0.148BSC	
e		0.75BSC			0.030BSC	
b	0.30	0.35	0.40	0.012	0.014	0.016

Notes:

- Controlling dimensions are in millimeters.

# PACKAGING INFORMATION

## Plastic TSOP Package Code: T (Type II)



**Notes:**

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.



Plastic TSOP (T - Type II)

Symbol	Millimeters		Inches		Millimeters		Inches		Millimeters		Inches	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Ref. Std.												
No. Leads (N)	32				44				50			
A	—	1.20	—	0.047	—	1.20	—	0.047	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15	0.002	0.006
b	0.30	0.52	0.012	0.020	0.30	0.45	0.012	0.018	0.30	0.45	0.012	0.018
C	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008	0.12	0.21	0.005	0.008
D	20.82	21.08	0.820	0.830	18.31	18.52	0.721	0.729	20.82	21.08	0.820	0.830
E1	10.03	10.29	0.391	0.400	10.03	10.29	0.395	0.405	10.03	10.29	0.395	0.405
E	11.56	11.96	0.451	0.466	11.56	11.96	0.455	0.471	11.56	11.96	0.455	0.471
e	1.27 BSC		0.050 BSC		0.80 BSC		0.032 BSC		0.80 BSC		0.031 BSC	
L	0.40	0.60	0.016	0.024	0.41	0.60	0.016	0.024	0.40	0.60	0.016	0.024
ZD	0.95 REF		0.037 REF		0.81 REF		0.032 REF		0.88 REF		0.035 REF	
α	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°	0°	5°

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