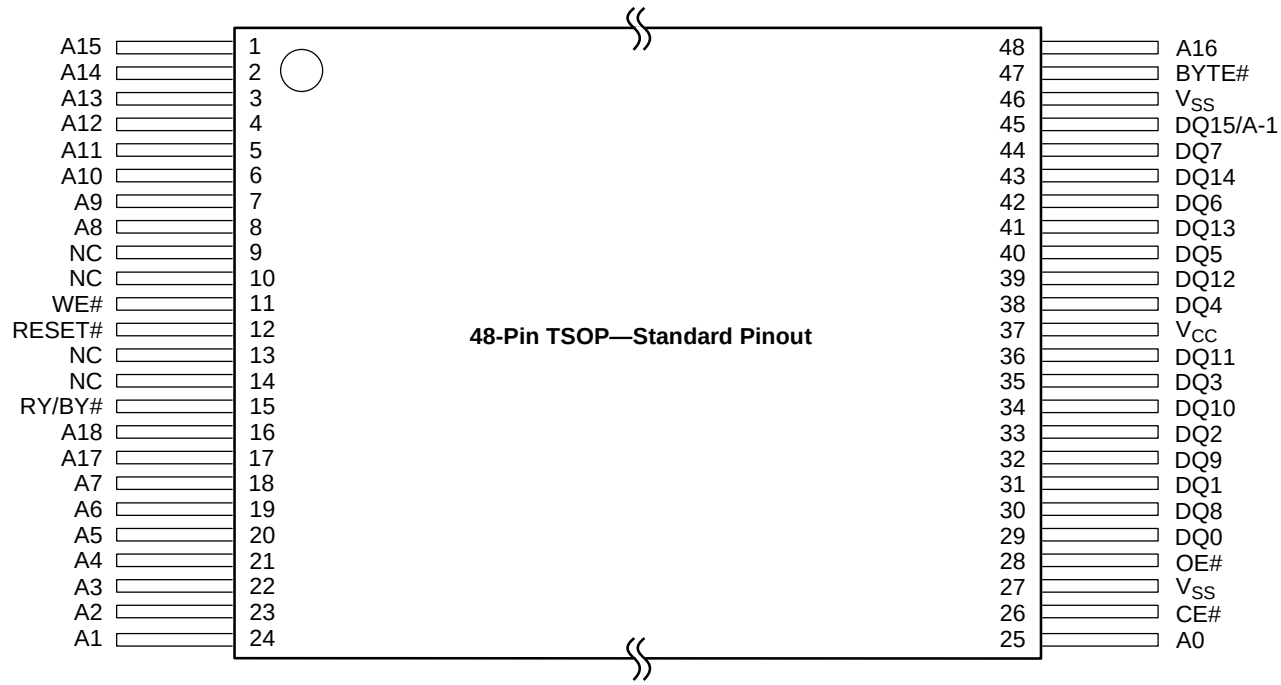
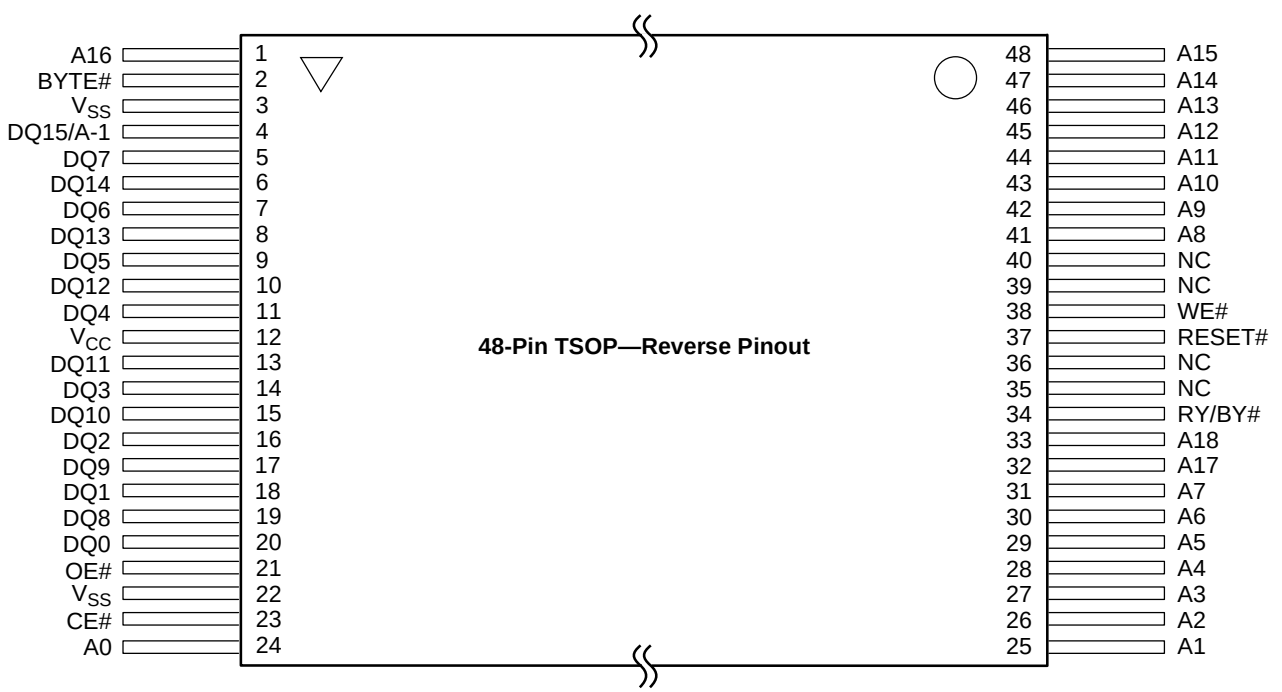
CONNECTION DIAGRAMS

This device is also available in Known Good Die (KGD) form. Refer to publication number 21631 for more information.



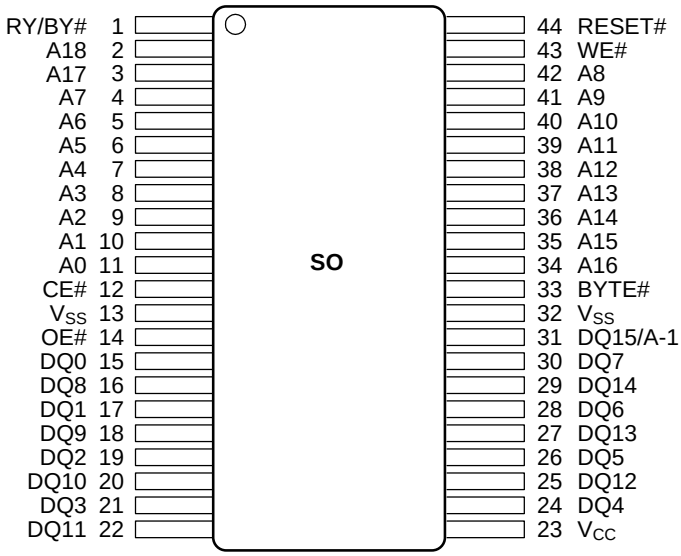
48-Pin TSOP—Standard Pinout



48-Pin TSOP—Reverse Pinout

CONNECTION DIAGRAMS

This device is also available in Known Good Die (KGD) form. Refer to publication number 21631 for more information.



FBGA
Top View, Balls Facing Down

A6	B6	C6	D6	E6	F6	G6	H6
A13	A12	A14	A15	A16	BYTE#	DQ15/A-1	V_{SS}
A5	B5	C5	D5	E5	F5	G5	H5
A9	A8	A10	A11	DQ7	DQ14	DQ13	DQ6
A4	B4	C4	D4	E4	F4	G4	H4
WE#	RESET#	NC	NC	DQ5	DQ12	V_{CC}	DQ4
A3	B3	C3	D3	E3	F3	G3	H3
RY/BY#	NC	A18	NC	DQ2	DQ10	DQ11	DQ3
A2	B2	C2	D2	E2	F2	G2	H2
A7	A17	A6	A5	DQ0	DQ8	DQ9	DQ1
A1	B1	C1	D1	E1	F1	G1	H1
A3	A4	A2	A1	A0	CE#	OE#	V_{SS}

Special Handling Instructions for FBGA Package

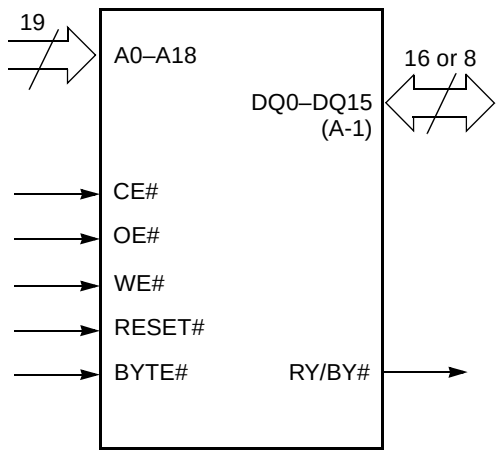
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN CONFIGURATION

A0–A18	=	19 addresses
DQ0–DQ14	=	15 data inputs/outputs
DQ15/A-1	=	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	=	Selects 8-bit or 16-bit mode
CE#	=	Chip enable
OE#	=	Output enable
WE#	=	Write enable
RESET#	=	Hardware reset pin, active low
RY/BY#	=	Ready/Busy# output
V_{CC}	=	+5.0 V single power supply (see Product Selector Guide for device speed ratings and voltage supply tolerances)
V_{SS}	=	Device ground
NC	=	Pin not connected internally

LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

Am29F800B T -70 E C

TEMPERATURE RANGE

C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE

E = 48-Pin Thin Small Outline Package (TSOP)
Standard Pinout (TS 048)
F = 48-Pin Thin Small Outline Package (TSOP)
Reverse Pinout (TSR048)
S = 44-Pin Small Outline Package (SO 044)
WB = 48-Ball Fine Pitch Ball Grid Array (FBGA)
0.80 mm pitch, 6 x 9 mm package (FBB048)

This device is also available in Known Good Die (KGD) form. See publication number 21536 for more information.

SPEED OPTION

See Product Selector Guide and Valid Combinations

BOOT CODE SECTOR ARCHITECTURE

T = Top sector
B = Bottom sector

DEVICE NUMBER/DESCRIPTION

Am29F800B
8 Megabit (1 M x 8-Bit/512K x 16-Bit) CMOS Flash Memory
5.0 Volt-only Read, Program and Erase

Valid Combinations	
AM29F800BT-55, AM29F800BB-55	EC, EI, EE, FC, FI, FE, SC, SI, SE
AM29F800BT-70, AM29F800BB-70	
AM29F800BT-90, AM29F800BB-90	
AM29F800BT-120, AM29F800BB-120	
AM29F800BT-150, AM29F800BB-150	

Valid Combinations for FBGA Packages			
Order Number		**Package Marking**	
AM29F800BT-55, AM29F800BB-55	WBC, WBI, WBE	F800BT55V, F800BB55V	C, I, E
AM29F800BT-70, AM29F800BB-70		F800BT70V, F800BB70V	
AM29F800BT-90, AM29F800BB-90		F800BT90V, F800BB90V	
AM29F800BT-120, AM29F800BB-120		F800BT12V, F800BB12V	
AM29F800BT-150, AM29F800BB-150		F800BT15V, F800BB15V	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. The appropriate device bus operations table lists the inputs and control levels required, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Am29F800B Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	A0–A18	DQ0–DQ7	DQ8–DQ15	
							BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	A_{IN}	D_{OUT}	D_{OUT}	High-Z
Write	L	H	L	H	A_{IN}	D_{IN}	D_{IN}	High-Z
CMOS Standby	V_{CC} ± 0.5 V	X	X	V_{CC} ± 0.5 V	X	High-Z	High-Z	High-Z
TTL Standby	H	X	X	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Hardware Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Temporary Sector Unprotect (See Note)	X	X	X	V_{ID}	A_{IN}	D_{IN}	D_{IN}	X

Legend:
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 12.0 ± 0.5 V, X = Don't Care, D_{IN} = Data In, D_{OUT} = Data Out, A_{IN} = Address In

Note: *See the sections on Sector Group Protection and Temporary Sector Unprotect for more information.*

Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins DQ15–DQ0 operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See "Reading Array Data" for more information. Refer to the AC Read Operations table for timing specifications and to the Read Operations Timings diagram for the timing waveforms. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

An erase operation can erase one sector, multiple sectors, or the entire device. The Sector Address Tables indicate the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. See the "Command Defini-

tions" section for details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the "Autoselect Mode" and "Autoselect Command Sequence" sections for more information.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification tables and timing diagrams for write operations.

Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to "Write Operation Status" for more information, and to each AC Characteristics section for timing diagrams.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when CE# and RESET# pins are both held at $V_{CC} \pm 0.5$ V. (Note that this is a more restricted voltage range than V_{IH}.) The device enters the TTL standby mode when CE# and RESET# pins are both held at V_{IH}. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

The device also enters the standby mode when the RESET# pin is driven low. Refer to the next section, "RESET#: Hardware Reset Pin".

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

In the DC Characteristics tables, I_{CC3} represents the standby current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the system drives the RESET# pin low for at least a period of t_{RP}, the device **immediately terminates** any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{IL}, the device enters the TTL standby mode; if RESET# is held at $V_{SS} \pm 0.5$ V, the device enters the CMOS standby mode.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is "1"), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the AC Characteristics tables for RESET# parameters and timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.