

DRAM

MT4LC4M4E8, MT4LC4M4E9

For the latest data sheet revisions, please refer to the Micron Web site: www.micron.com/mti/msp/html/datasheet.html

FEATURES

- Industry-standard x4 pinout, timing, functions and packages
- High-performance, low-power CMOS silicon-gate process
- Single +3.3V \pm 0.3V power supply
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: RAS#-ONLY, HIDDEN and CAS#-BEFORE-RAS# (CBR)
- Optional self refresh (S) for low-power data retention
- 11 row, 11 column addresses (2K refresh) or 12 row, 10 column addresses (4K refresh)
- Extended Data-Out (EDO) PAGE MODE access

OPTIONS

- Refresh Addressing

2,048 (2K) rows	E8
4,096 (4K) rows	E9
- Packages

Plastic SOJ (300 mil)	DJ
Plastic TSOP (300 mil)	TG
- Timing

50ns access	-5
60ns access	-6
- Refresh Rates

Standard Refresh	None
Self Refresh (128ms period)	S*

NOTE: 1. The 4 Meg x 4 EDO DRAM base number differentiates the offerings in one place - MT4LC4M4E8. The fifth field distinguishes various options: E8 designates a 2K refresh and E9 designates a 4K refresh for EDO DRAMs.
2. The “#” symbol indicates signal is active LOW.

*Contact factory for availability

KEY TIMING PARAMETERS

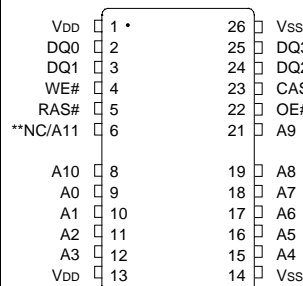
SPEED	t _{RC}	t _{RAC}	t _{PC}	t _{AA}	t _{CAC}	t _{CAS}
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

GENERAL DESCRIPTION

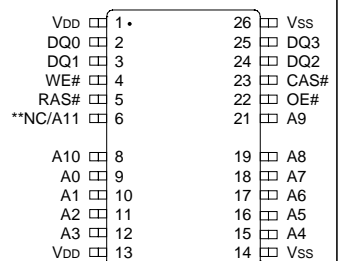
The 4 Meg x 4 DRAM is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x4 configuration. RAS# is used to latch the row address (first 11 bits for 2K and first 12 bits for 4K). Once the page has been opened by RAS#, CAS# is used to latch the column address

PIN ASSIGNMENT (Top View)

24/26-Pin SOJ



24/26-Pin TSOP



** NC on 2K refresh and A11 on 4K refresh options.

4 MEG x 4 EDO DRAM PART NUMBERS

PART NUMBER	REFRESH ADDRESSING	PACKAGE	REFRESH
MT4LC4M4E8DJ-x	2K	SOJ	Standard
MT4LC4M4E8DJ-x S	2K	SOJ	Self
MT4LC4M4E8TG-x	2K	TSOP	Standard
MT4LC4M4E8TG-x S	2K	TSOP	Self
MT4LC4M4E9DJ-x	4K	SOJ	Standard
MT4LC4M4E9DJ-x S	4K	SOJ	Self
MT4LC4M4E9TG-x	4K	TSOP	Standard
MT4LC4M4E9TG-x S	4K	TSOP	Self

x = speed

(the latter 11 bits for 2K and the latter 10 bits for 4K; address pins A10 and A11 are “Don’t Care”). READ and WRITE cycles are selected with the WE# input.

A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# is taken LOW. During EARLY WRITE cycles, the data outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE

GENERAL DESCRIPTION (continued)

cycles, OE# must be taken HIGH to disable the data outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no WRITE will occur, and the data outputs will drive read data from the accessed location.

The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by WE# and OE#.

The 4 Meg x 4 DRAM must be refreshed periodically in order to retain stored data.

PAGE ACCESS

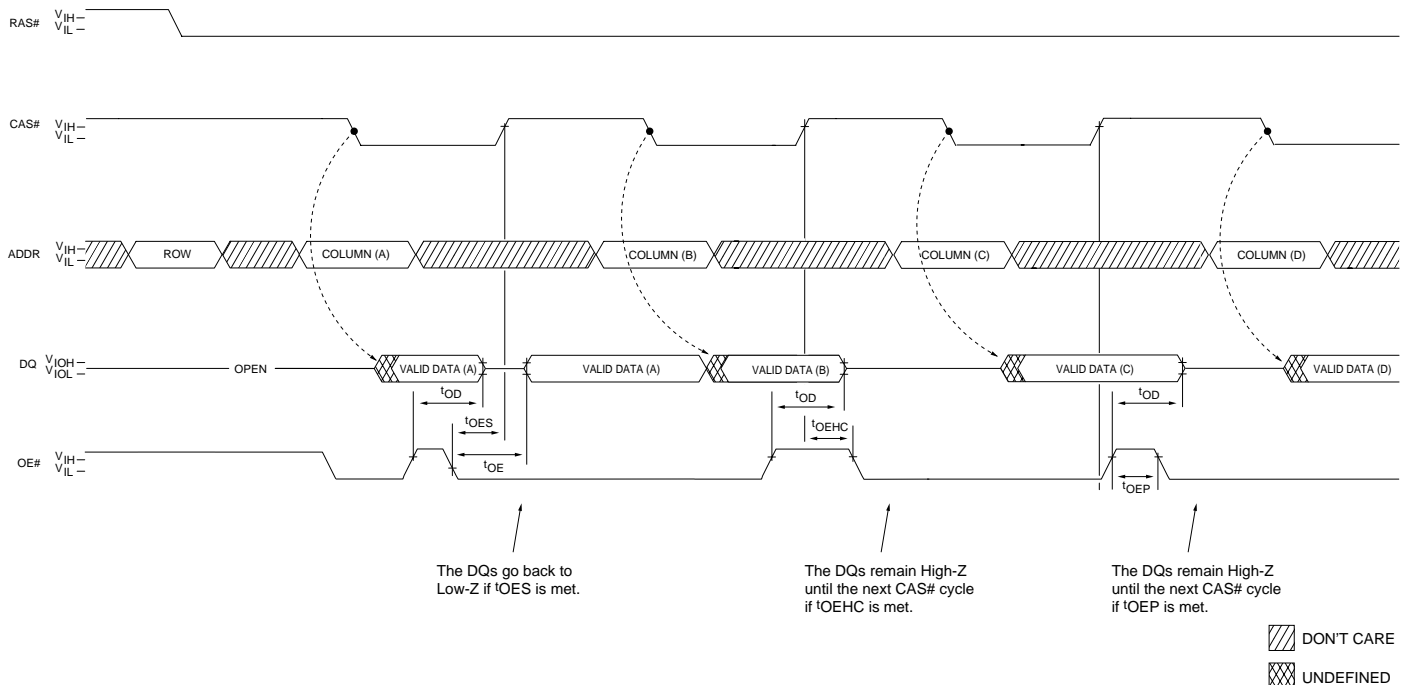
Page operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The page cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the page mode of operation, i.e., closes the page.

EDO PAGE MODE

The 4 Meg x 4 EDO DRAM provides EDO PAGE MODE, which is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# returns HIGH. EDO allows CAS# precharge time (t_{CP}) to occur without the output data going invalid. This elimination of CAS# output control allows pipelined READs.

FAST-PAGE-MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate like FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z (refer to Figure 1). WE# can also perform the function of disabling the output devices under certain conditions, as shown in Figure 2.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alterna-



**Figure 1
OE# CONTROL OF DQs**

EDO PAGE MODE (continued)

tively, pulsing WE# to the idle banks during CAS# HIGH time will also High-Z the outputs. Independent of OE# control, the outputs will disable after t^{OFF}, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last.

DRAM REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# REFRESH cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses (2,048 for 2K and 4,096 for 4K) are executed within t^{REF} (MAX), regardless of sequence. The CBR and SELF REFRESH cycles will invoke the internal refresh counter for automatic RAS# addressing.

An optional self refresh mode is also available on the "S" version. The self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified t^{RASS}. The "S" option allows the user the choice of a fully static, low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms,

or 31.25µs per row for a 4K refresh and 62.5µs per row for a 2K refresh, when using a distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or battery backup mode.

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of t^{RPS}. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes a RAS#-ONLY or burst refresh sequence, all rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

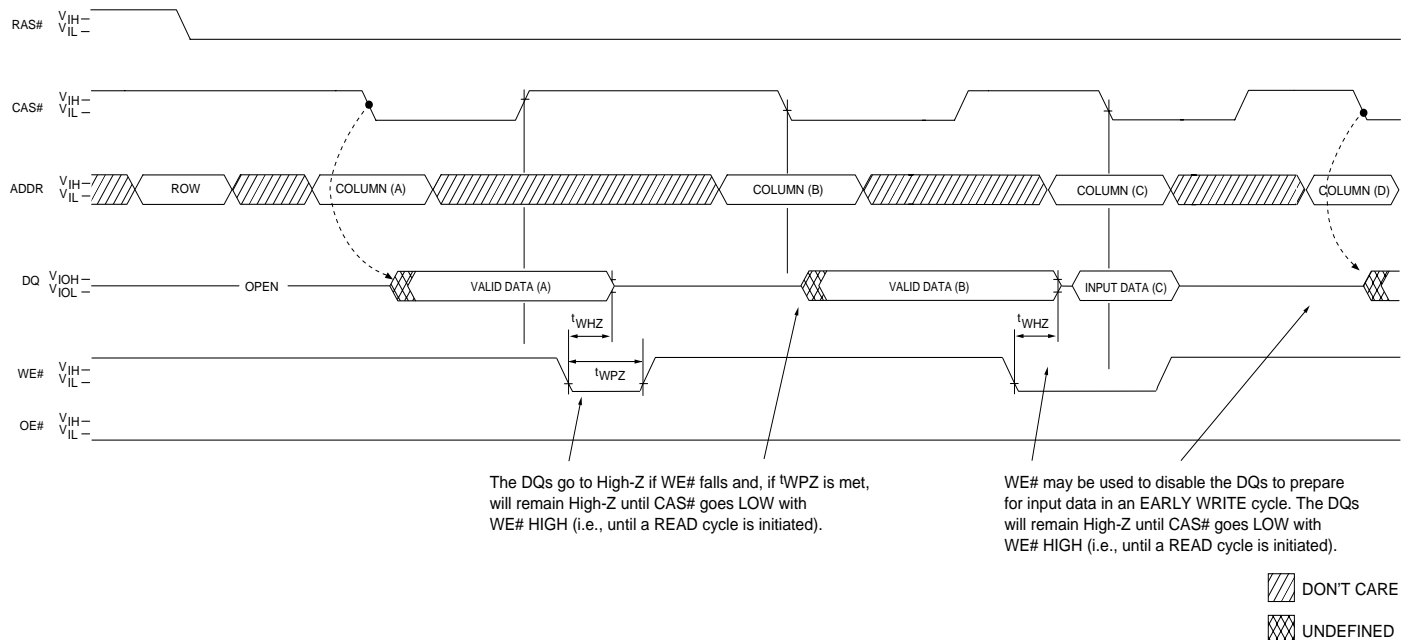
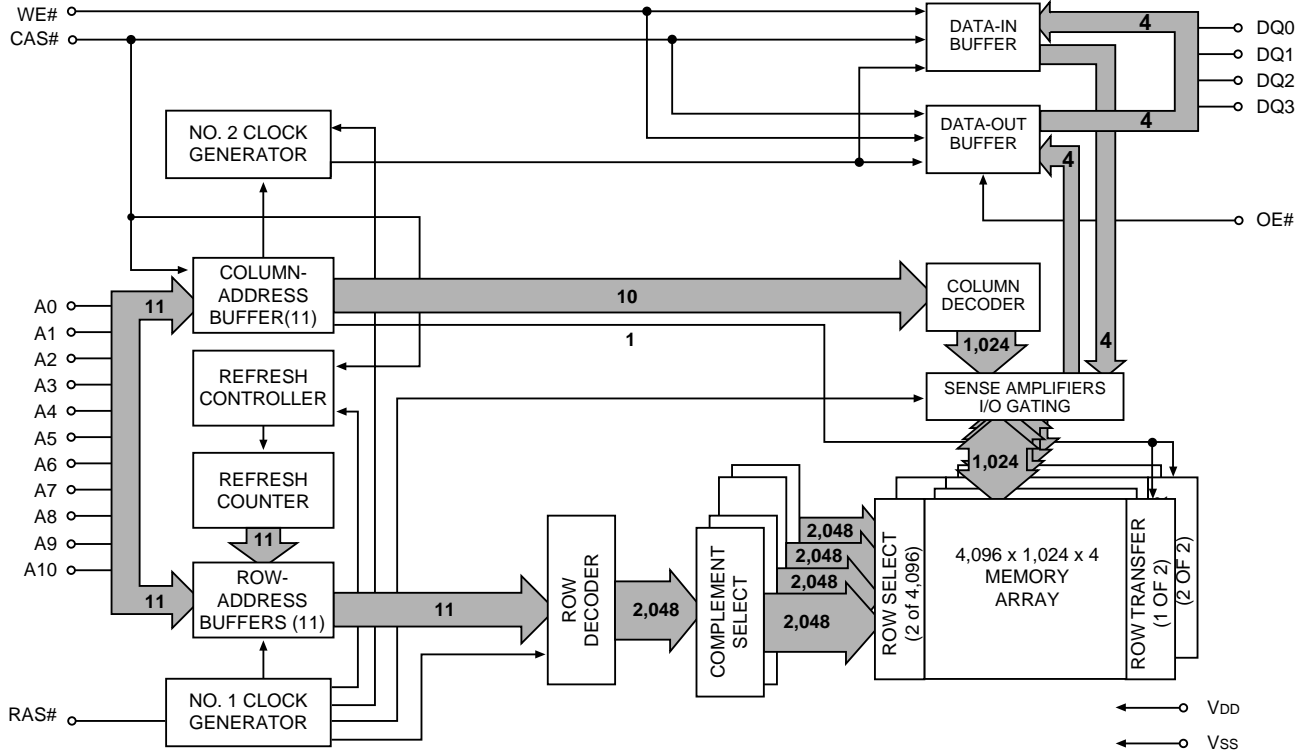
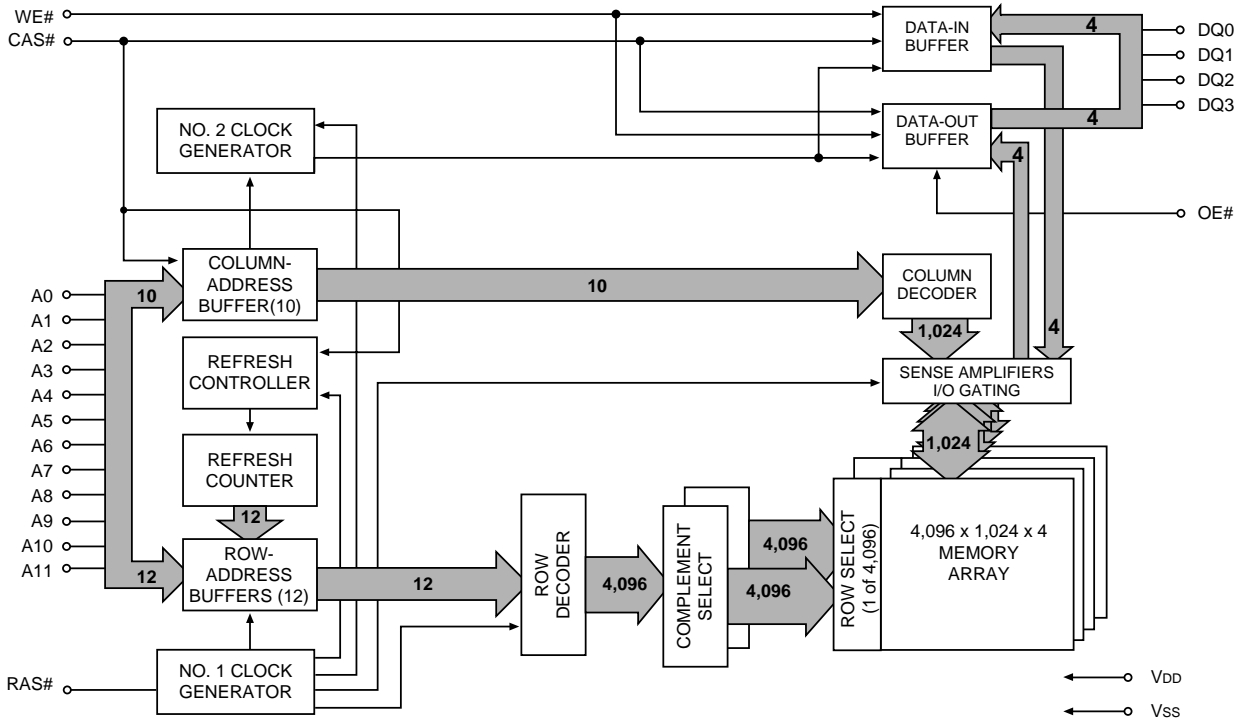


Figure 2
WE# CONTROL OF DQs

FUNCTIONAL BLOCK DIAGRAM - 2K REFRESH



FUNCTIONAL BLOCK DIAGRAM - 4K REFRESH



ABSOLUTE MAXIMUM RATINGS*

Voltage on V _{DD} Pin Relative to V _{SS}	-1V to +4.6V
Voltage on NC, Inputs or I/O Pins Relative to V _{SS}	-1V to +4.6V
Operating Temperature, T _A (ambient)	0°C to +70°C
Storage Temperature (plastic)	-55°C to +150°C
Power Dissipation	1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1) (V_{DD} = +3.3V ± 0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V _{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Valid Logic 1; All inputs, I/Os and any NC	V _{IH}	2	5.5	V	26
INPUT LOW VOLTAGE: Valid Logic 0; All inputs, I/Os and any NC	V _{IL}	-0.5	0.8	V	26
INPUT LEAKAGE CURRENT: Any input at V _{IN} (0V ≤ V _{IN} ≤ V _{DD} + 0.3V); All other pins not under test = 0V	I _I	-2	2	μA	4
OUTPUT HIGH VOLTAGE: I _{OUT} = -2mA	V _{OH}	2.4	–	V	
OUTPUT LOW VOLTAGE: I _{OUT} = 2mA	V _{OL}	–	0.4	V	
OUTPUT LEAKAGE CURRENT: Any output at V _{OUT} (0V ≤ V _{OUT} ≤ V _{DD} + 0.3V); DQ is disabled and in High-Z state	I _{OZ}	-5	5	μA	

I_{CC} OPERATING CONDITIONS AND MAXIMUM LIMITS

 (Notes: 1, 2, 3, 5, 8) ($V_{DD} = +3.3V \pm 0.3V$)

PARAMETER/CONDITION	SYMBOL	SPEED	2K REFRESH	4K REFRESH	UNITS	NOTES
STANDBY CURRENT: TTL (RAS# = CAS# = V_{IH})	I _{CC1}	ALL	1	1	mA	
STANDBY CURRENT: CMOS (non-"S" version only) (RAS# = CAS# = other inputs = $V_{DD} - 0.2V$)	I _{CC2}	ALL	500	500	μA	
STANDBY CURRENT: CMOS ("S" version only) (RAS# = CAS# = other inputs = $V_{DD} - 0.2V$)	I _{CC2}	ALL	150	150	μA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: $t_{RC} = t_{RC} [MIN]$)	I _{CC3}	-5 -6	110 100	90 80	mA	6
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS# = V_{IL} , CAS#, address cycling: $t_{PC} = t_{PC} [MIN]$)	I _{CC4}	-5 -6	110 100	100 90	mA	6
REFRESH CURRENT: RAS#-ONLY Average power supply current (RAS# cycling, CAS# = V_{IH} : $t_{RC} = t_{RC} [MIN]$)	I _{CC5}	-5 -6	110 100	90 80	mA	
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: $t_{RC} = t_{RC} [MIN]$)	I _{CC6}	-5 -6	110 100	90 80	mA	7, 9
REFRESH CURRENT: Extended ("S" version only) Average power supply current: CAS# = 0.2V or CBR cycling; RAS# = $t_{RAS} (MIN)$; WE# = $V_{DD} - 0.2V$; A0-A11, OE# and D _{IN} = $V_{DD} - 0.2V$ or 0.2V (D _{IN} may be left open)	I _{CC7}	ALL	300	300	μA	7, 9
		t_{RC}	62.5	31.25	μs	25
REFRESH CURRENT: Self ("S" version only) Average power supply current: CBR with RAS# $\geq t_{RASS} (MIN)$ and CAS# held LOW; WE# = $V_{DD} - 0.2V$; A0-A11, OE# and D _{IN} = $V_{DD} - 0.2V$ or 0.2V (D _{IN} may be left open)	I _{CC8}	ALL	300	300	μA	7, 9

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C _{I1}	5	pF	8
Input Capacitance: RAS#, CAS#, WE#, OE#	C _{I2}	7	pF	8
Input/Output Capacitance: DQ	C _{I0}	7	pF	8

AC ELECTRICAL CHARACTERISTICS

(Notes: 2, 3, 9, 10, 11, 12) (V_{DD} = +3.3V ± 0.3V)

AC CHARACTERISTICS PARAMETER	SYMBOL	-5		-6		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Access time from column address	t ^{AA}		25		30	ns	
Column-address setup to CAS# precharge	t ^{ACH}	12		15		ns	
Column-address hold time (referenced to RAS#)	t ^{AR}	38		45		ns	
Column-address setup time	t ^{ASC}	0		0		ns	
Row-address setup time	t ^{ASR}	0		0		ns	
Column address to WE# delay time	t ^{AWD}	42		49		ns	13
Access time from CAS#	t ^{CAC}		13		15	ns	14
Column-address hold time	t ^{CAH}	8		10		ns	
CAS# pulse width	t ^{CAS}	8	10,000	10	10,000	ns	
CAS# LOW to "Don't Care" during Self Refresh	t ^{CHD}	15		15		ns	
CAS# hold time (CBR Refresh)	t ^{CHR}	8		10		ns	7
CAS# to output in Low-Z	t ^{CLZ}	0		0		ns	
Data output hold after next CAS# LOW	t ^{COH}	3		3		ns	
CAS# precharge time	t ^{CP}	8		10		ns	15
Access time from CAS# precharge	t ^{CPA}		28		35	ns	
CAS# to RAS# precharge time	t ^{CRP}	5		5		ns	
CAS# hold time	t ^{CSH}	38		45		ns	
CAS# setup time (CBR Refresh)	t ^{CSR}	5		5		ns	
CAS# to WE# delay time	t ^{CWD}	28		35		ns	13
WRITE command to CAS# lead time	t ^{CWL}	8		10		ns	
Data-in hold time	t ^{DH}	8		10		ns	16
Data-in setup time	t ^{DS}	0		0		ns	16
Output disable	t ^{OD}	0	12	0	15	ns	
Output enable	t ^{OE}		12		15	ns	17
OE# hold time from WE# during READ-MODIFY-WRITE cycle	t ^{OEH}	8		10		ns	18
OE# HIGH hold from CAS# HIGH	t ^{OEHC}	5		10		ns	18
OE# HIGH pulse width	t ^{OEP}	5		5		ns	
OE# LOW to CAS# HIGH setup time	t ^{OES}	4		5		ns	
Output buffer turn-off delay	t ^{OFF}	0	12	0	15	ns	20

AC ELECTRICAL CHARACTERISTICS

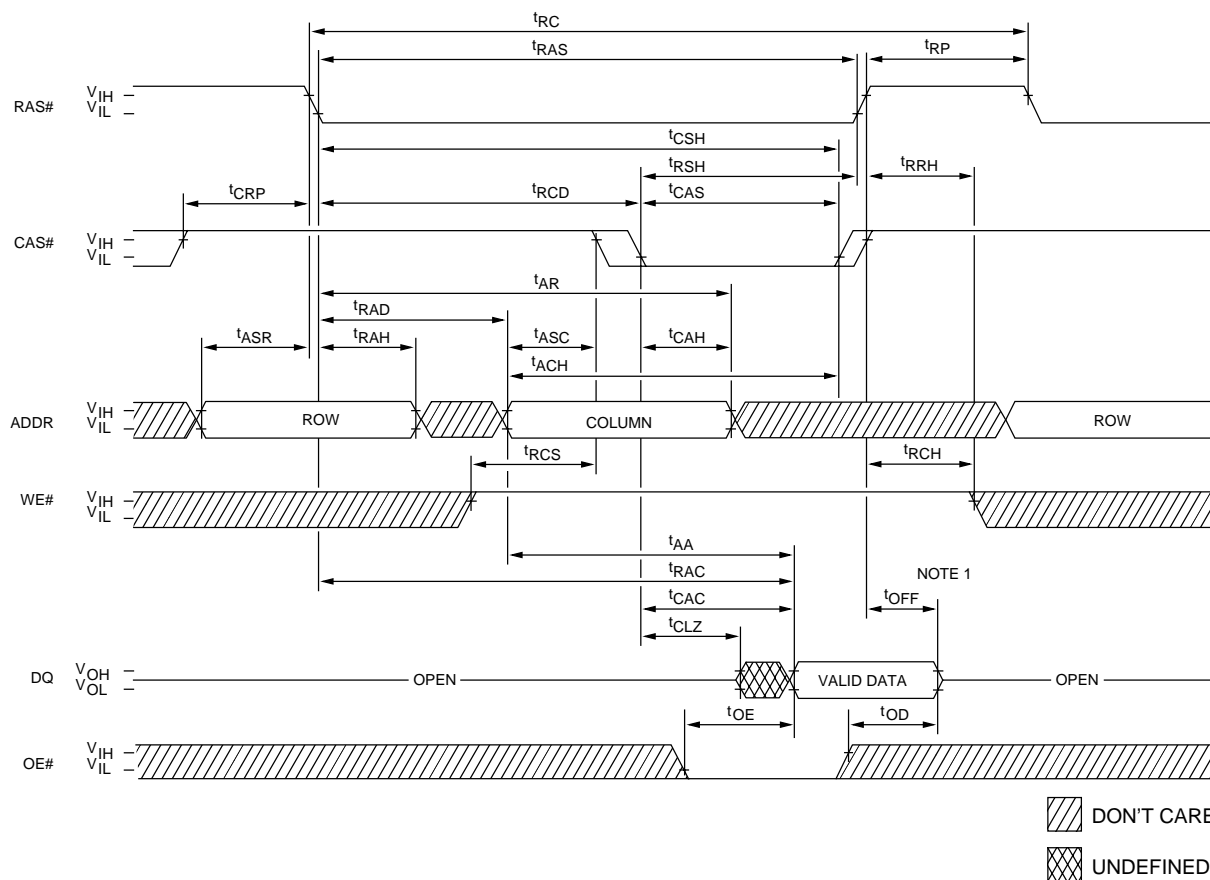
(Notes: 2, 3, 9, 10, 11, 12) ($V_{DD} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS PARAMETER	SYMBOL	-5		-6		UNITS	NOTES
		MIN	MAX	MIN	MAX		
OE# setup prior to RAS# during HIDDEN REFRESH cycle	t_{ORD}	0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	t_{PC}	20		25		ns	
EDO-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	47		56		ns	
Access time from RAS#	t_{RAC}		50		60	ns	19
RAS# to column-address delay time	t_{RAD}	9		12		ns	21
Row-address hold time	t_{RAH}	9		10		ns	
RAS# pulse width	t_{RAS}	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	t_{RASP}	50	125,000	60	125,000	ns	7
RAS# pulse width during Self Refresh	t_{RASS}	100		100		μ s	
Random READ or WRITE cycle time	t_{RC}	84		104		ns	
RAS# to CAS# delay time	t_{RCD}	11		14		ns	22
READ command hold time (referenced to CAS#)	t_{RCH}	0		0		ns	23
READ command setup time	t_{RCS}	0		0		ns	
Refresh period (2,048 cycles)	t_{REF}		32		32	ms	
Refresh period (4,096 cycles)	t_{REF}		64		64	ms	
Refresh period "S" version	t_{REF}		128		128	ms	
RAS# precharge time	t_{RP}	30		40		ns	
RAS# to CAS# precharge time	t_{RPC}	5		5		ns	
RAS# precharge time exiting Self Refresh	t_{RPS}	90		105		ns	
READ command hold time (referenced to RAS#)	t_{RRH}	0		0		ns	23
RAS# hold time	t_{RSH}	13		15		ns	
READ-WRITE cycle time	t_{RWC}	116		140		ns	
RAS# to WE# delay time	t_{RWD}	67		79		ns	13
WRITE command to RAS# lead time	t_{RWL}	13		15		ns	
Transition time (rise or fall)	t_T	2	50	2	50	ns	
WRITE command hold time	t_{WCH}	8		10		ns	
WRITE command hold time (referenced to RAS#)	t_{WCR}	38		45		ns	
WE# command setup time	t_{WCS}	0		0		ns	13
Output disable delay from WE#	t_{WHZ}	0	12	0	15	ns	
WRITE command pulse width	t_{WP}	5		5		ns	
WE# pulse to disable at CAS# HIGH	t_{WPZ}	10		10		ns	
WE# hold time (CBR Refresh)	t_{WRH}	8		10		ns	6, 7
WE# setup time (CBR Refresh)	t_{WRP}	8		10		ns	6, 7

NOTES

1. All voltages referenced to V_{SS} .
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$) is ensured.
3. An initial pause of $100\mu\text{s}$ is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
4. NC pins are assumed to be left floating and are not tested for leakage.
5. ICC is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
6. Column address changed once each cycle.
7. Enables on-chip refresh and address counters.
8. This parameter is sampled. $V_{DD} = +3.3\text{V}$; $f = 1\text{ MHz}$.
9. AC characteristics assume $t_T = 2.5\text{ns}$.
10. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
11. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
12. Measured with a load equivalent to two TTL gates and 100pF ; and $V_{OL} = 0.8\text{V}$ and $V_{OH} = 2\text{V}$.
13. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are not restrictive operating parameters. t_{WCS} applies to EARLY WRITE cycles. t_{RWD} , t_{AWD} and t_{CWD} apply to READ-MODIFY-WRITE cycles. If $t_{WCS} \geq t_{WCS}$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{WCS} < t_{WCS}$ (MIN) and $t_{RWD} \geq t_{RWD}$ (MIN), $t_{AWD} \geq t_{AWD}$ (MIN) and $t_{CWD} \geq t_{CWD}$ (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW results in a LATE WRITE (OE#-controlled) cycle. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not applicable in a LATE WRITE cycle.
14. Requires that t_{AA} and t_{RAC} are not violated.
15. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for t_{CP} .
16. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
17. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, WE# must be pulsed during CAS# HIGH time in order to place I/O buffers in High-Z.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OEH} met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after t_{OEH} is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.
19. Requires that t_{AA} and t_{CAC} are not violated.
20. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} . It is referenced from the rising edge of RAS# or CAS#, whichever occurs last.
21. The t_{RAD} (MAX) limit is no longer specified. t_{RAD} (MAX) was specified as a reference point only. If t_{RAD} was greater than the specified t_{RAD} (MAX) limit, then access time was controlled exclusively by t_{AA} (t_{RAC} and t_{CAC} no longer applied). With or without the t_{RAD} (MAX) limit, t_{AA} , t_{RAC} and t_{CAC} must always be met.
22. The t_{RCD} (MAX) limit is no longer specified. t_{RCD} (MAX) was specified as a reference point only. If t_{RCD} was greater than the specified t_{RCD} (MAX) limit, then access time was controlled exclusively by t_{CAC} (t_{RAC} [MIN] no longer applied). With or without the t_{RCD} limit, t_{AA} and t_{CAC} must always be met.
23. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# is LOW and OE# is HIGH.
25. The refresh period is extended from 32ms (2K refresh) or 64ms (4K refresh) to 128ms (both 2K and 4K refresh). For 4K refresh, $t_{RC} = 31.25\mu\text{s}$ (128ms/4,096 rows = $31.25\mu\text{s}$) and for 2K refresh, $t_{RC} = 62.5\mu\text{s}$ (128ms/2,048 rows = $62.5\mu\text{s}$).
26. V_{IH} overshoot: V_{IH} (MAX) = $V_{DD} + 2\text{V}$ for a pulse width $\leq 10\text{ns}$, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width $\leq 10\text{ns}$, and the pulse width cannot be greater than one third of the cycle rate.

READ CYCLE



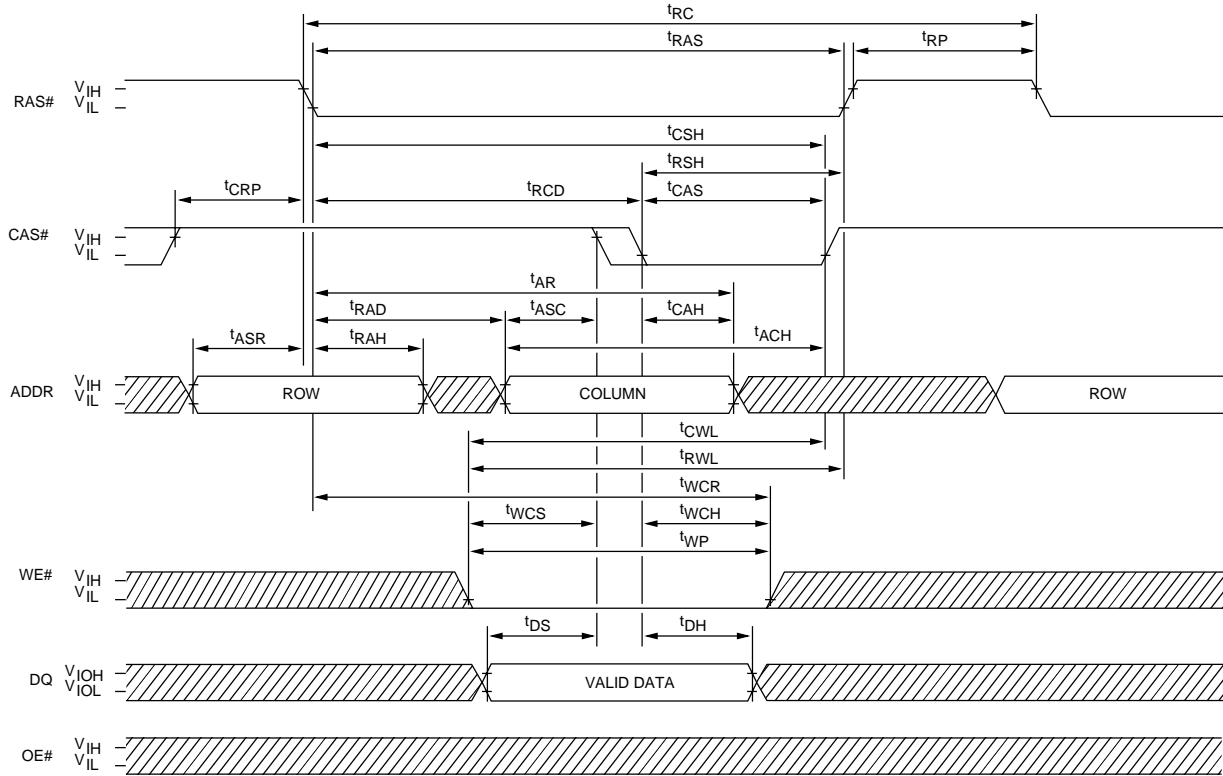
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		25		30	ns
t_{ACH}	12		15		ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAC}		13		15	ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CLZ}	0		0		ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{OD}	0	12	0	15	ns
t_{OE}		12		15	ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{OFF}	0	12	0	15	ns
t_{RAC}		50		60	ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RC}	84		104		ns
t_{RCD}	11		14		ns
t_{RCH}	0		0		ns
t_{RCS}	0		0		ns
t_{RP}	30		40		ns
t_{RRH}	0		0		ns
t_{RSH}	13		15		ns

NOTE: 1. t_{OFF} is referenced from rising edge of RAS# or CAS#, whichever occurs last.

EARLY WRITE CYCLE



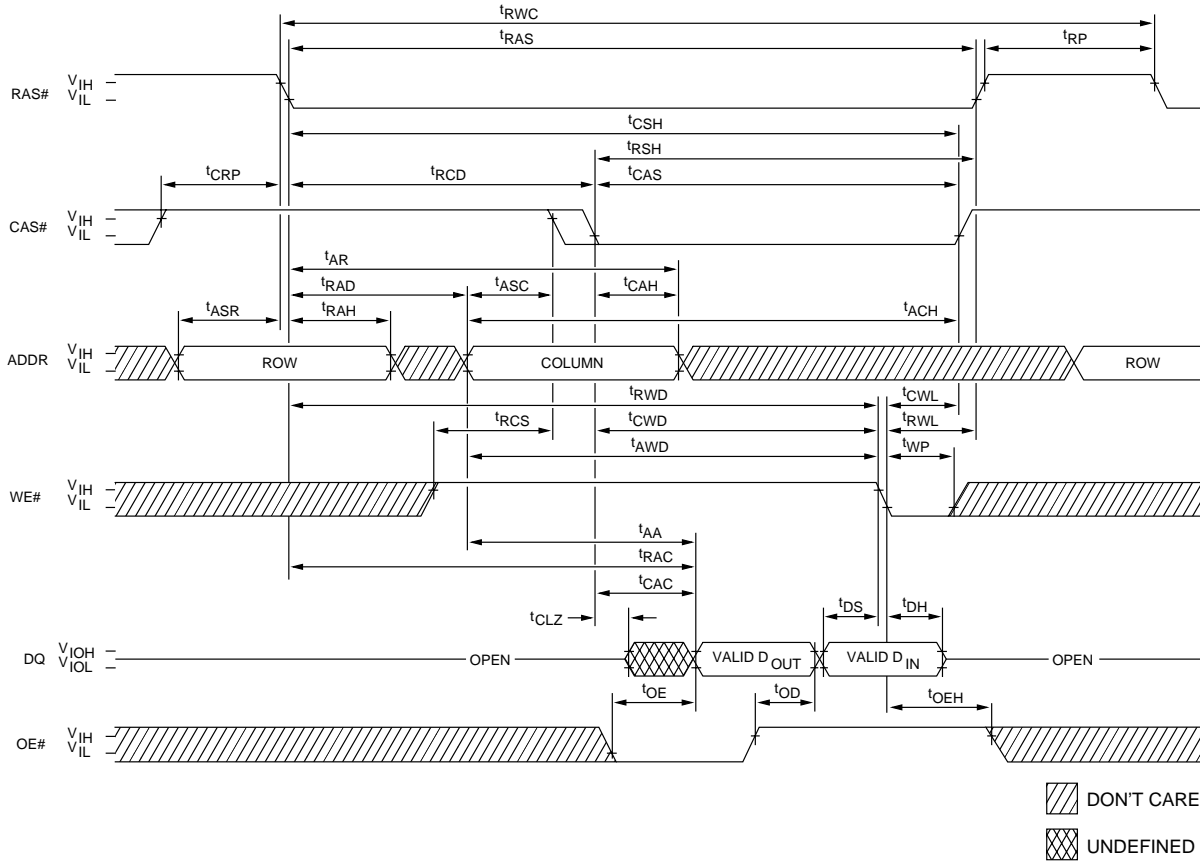
DON'T CARE
 UNDEFINED

TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{ACH}	12		15		ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{CWL}	8		10		ns
t_{DH}	8		10		ns
t_{DS}	0		0		ns
t_{RAD}	9		12		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{RAH}	9		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RC}	84		104		ns
t_{RCD}	11		14		ns
t_{RP}	30		40		ns
t_{RSH}	13		15		ns
t_{RWL}	13		15		ns
t_{WCH}	8		10		ns
t_{WCR}	38		45		ns
t_{WCS}	0		0		ns
t_{WP}	5		5		ns

READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)

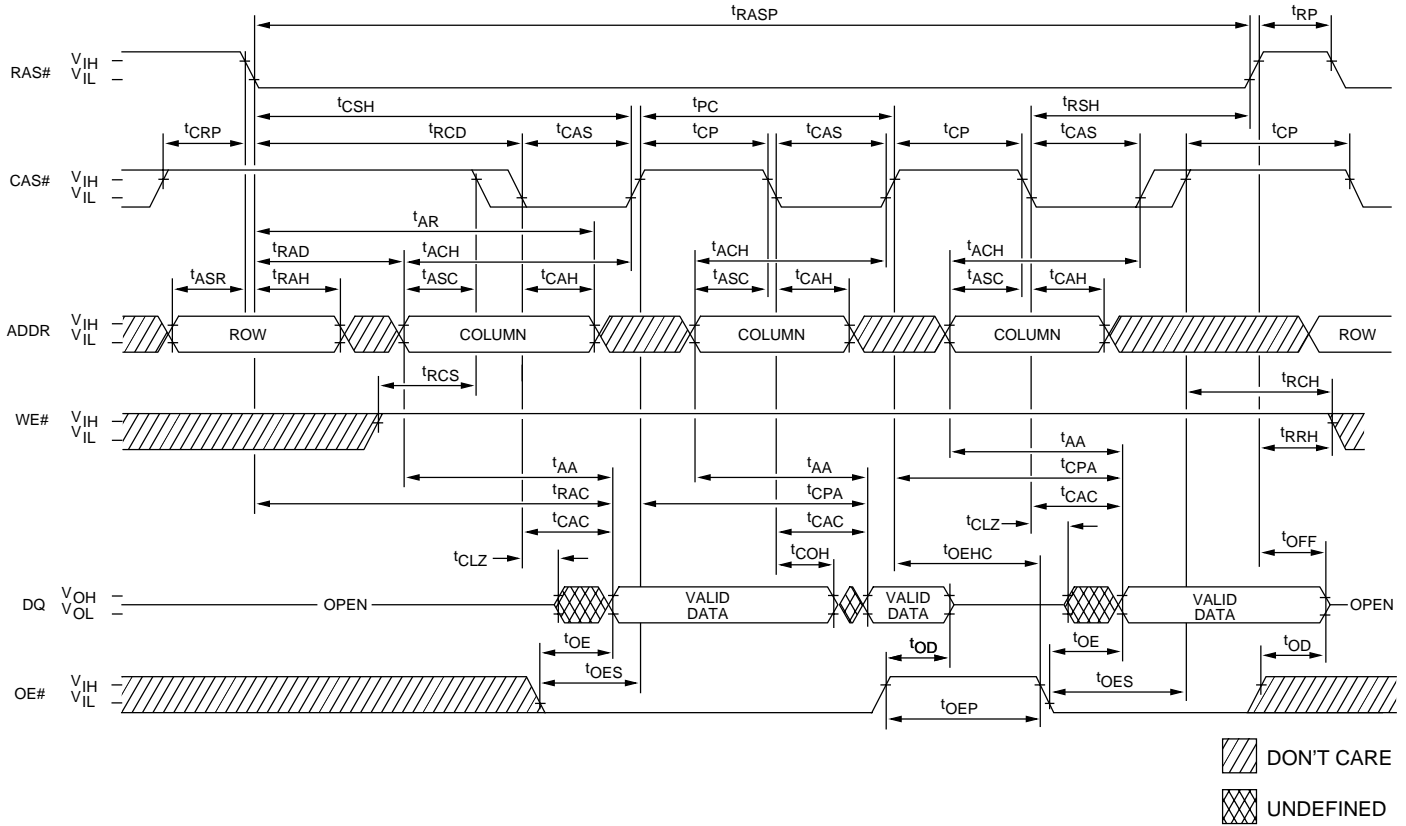


TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		25		30	ns
t_{ACH}	12		15		ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{AWD}	42		49		ns
t_{ASR}	0		0		ns
t_{CAC}		13		15	ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CLZ}	0		0		ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{CWD}	28		35		ns
t_{CWL}	8		10		ns
t_{DH}	8		10		ns
t_{DS}	0		0		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{OD}	0	12	0	15	ns
t_{OE}		12		15	ns
t_{OEH}	8		10		ns
t_{RAC}		50		60	ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RCD}	11		14		ns
t_{RCS}	0		0		ns
t_{RP}	30		40		ns
t_{RSH}	13		15		ns
t_{RWC}	116		140		ns
t_{RWD}	67		79		ns
t_{RWL}	13		15		ns
t_{WP}	5		5		ns

EDO-PAGE-MODE READ CYCLE

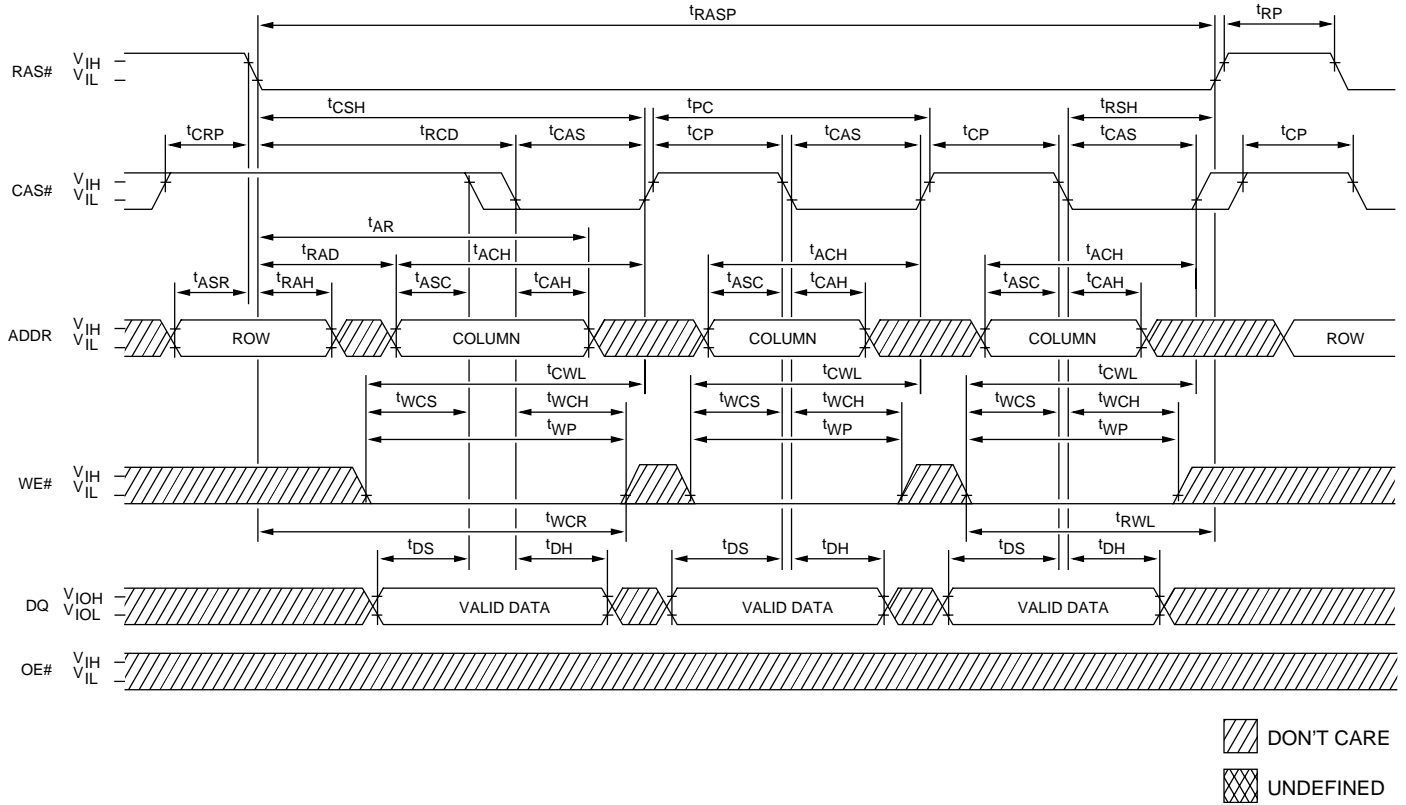


TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tOD	0	12	0	15	ns
tOE		12		15	ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tOEHC	5		10		ns
tOEP	5		5		ns
tOES	4		5		ns
tOFF	0	12	0	15	ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRRH	0		0		ns
tRSH	13		15		ns

EDO-PAGE-MODE EARLY WRITE CYCLE

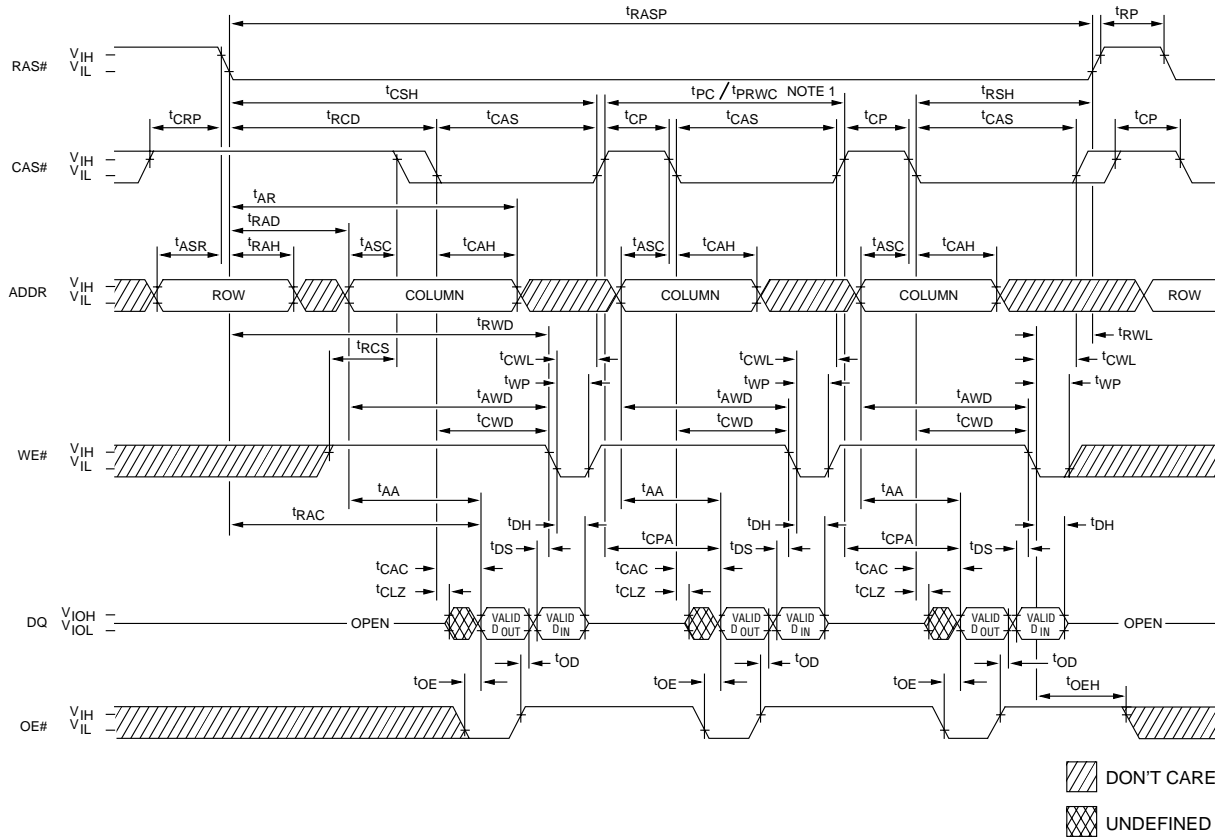


TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{ACH}	12		15		ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CP}	8		10		ns
t_{CRP}	5		5		ns
t_{CSH}	38		45		ns
t_{CWL}	8		10		ns
t_{DH}	8		10		ns
t_{DS}	0		0		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{PC}	20		25		ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RASP}	50	125,000	60	125,000	ns
t_{RCD}	11		14		ns
t_{RP}	30		40		ns
t_{RSH}	13		15		ns
t_{RWL}	13		15		ns
t_{WCH}	8		10		ns
t_{WCR}	38		45		ns
t_{WCS}	0		0		ns
t_{WP}	5		5		ns

EDO-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE cycles)



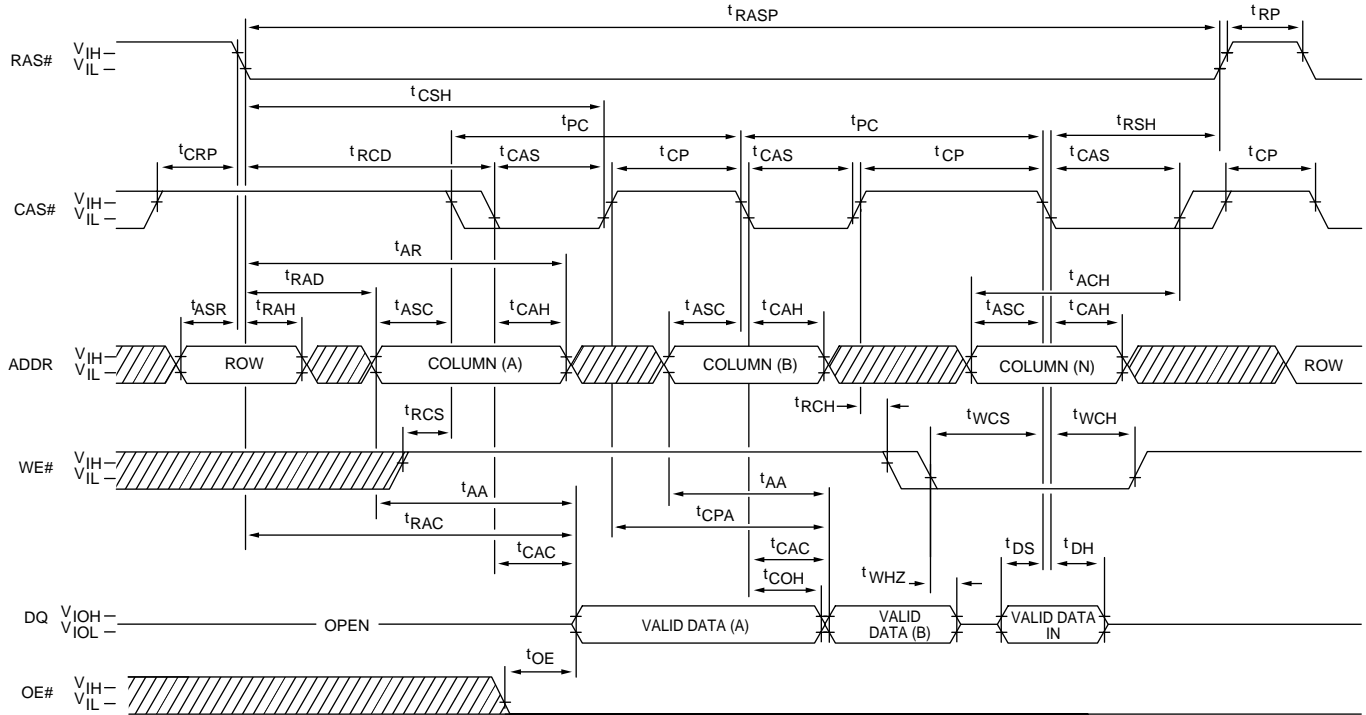
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	42		49		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tCWD	28		35		ns
tCWL	8		10		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tOD	0	12	0	15	ns
tOEH	8		10		ns
tPC	20		25		ns
tPRWC	47		56		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWD	67		79		ns
tRWL	13		15		ns
tWP	5		5		ns

NOTE: 1. tPC is for LATE WRITE cycles only.

**EDO-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)**



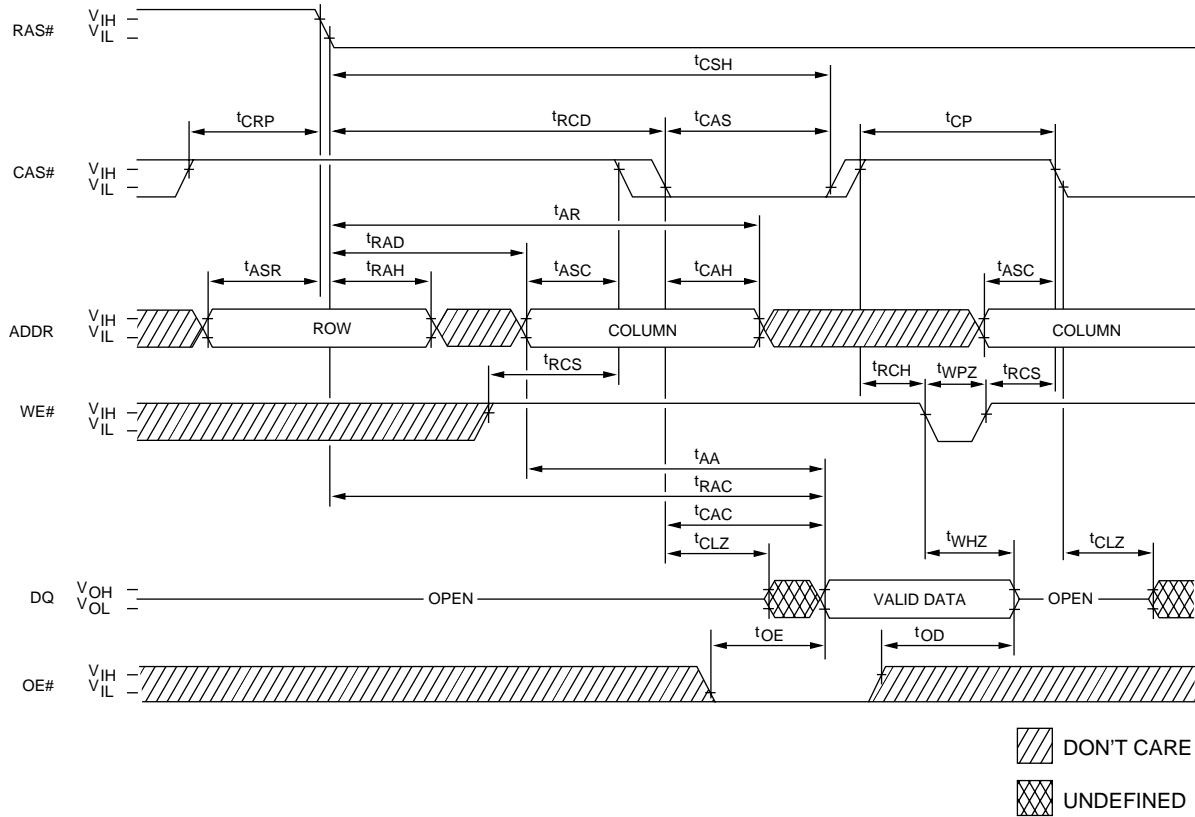
DON'T CARE
 UNDEFINED

TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{ACH}	12		15		ns
t _{AR}	38		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC}		13		15	ns
t _{CAH}	8		10		ns
t _{CAS}	8	10,000	10	10,000	ns
t _{COH}	3		3		ns
t _{CP}	8		10		ns
t _{CPA}		28		35	ns
t _{CRP}	5		5		ns
t _{CSH}	38		45		ns
t _{DH}	8		10		ns
t _{DS}	0		0		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OE}		12		15	ns
t _{PC}	20		25		ns
t _{RAC}		50		60	ns
t _{RAD}	9		12		ns
t _{RAH}	9		10		ns
t _{RASP}	50	125,000	60	125,000	ns
t _{RCD}	11		14		ns
t _{RCH}	0		0		ns
t _{RCS}	0		0		ns
t _{RP}	30		40		ns
t _{RSH}	13		15		ns
t _{WCH}	8		10		ns
t _{WCS}	0		0		ns
t _{WHZ}	0	12	0	15	ns

READ CYCLE
(With WE#-controlled disable)

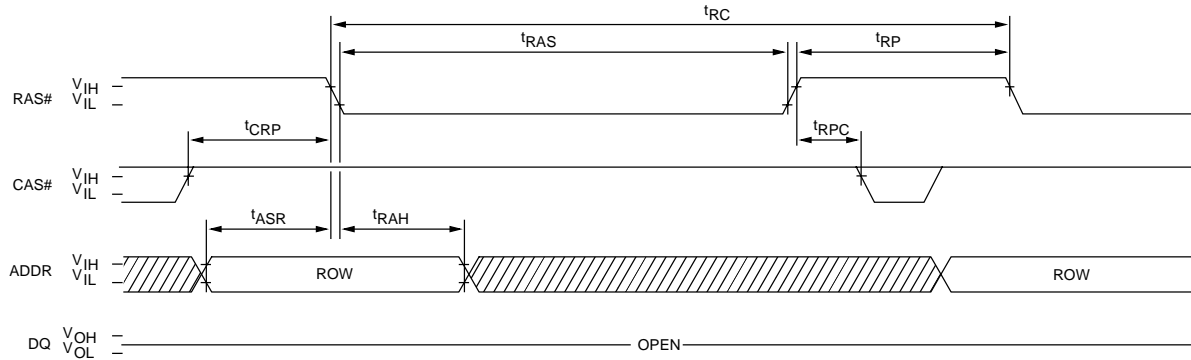


TIMING PARAMETERS

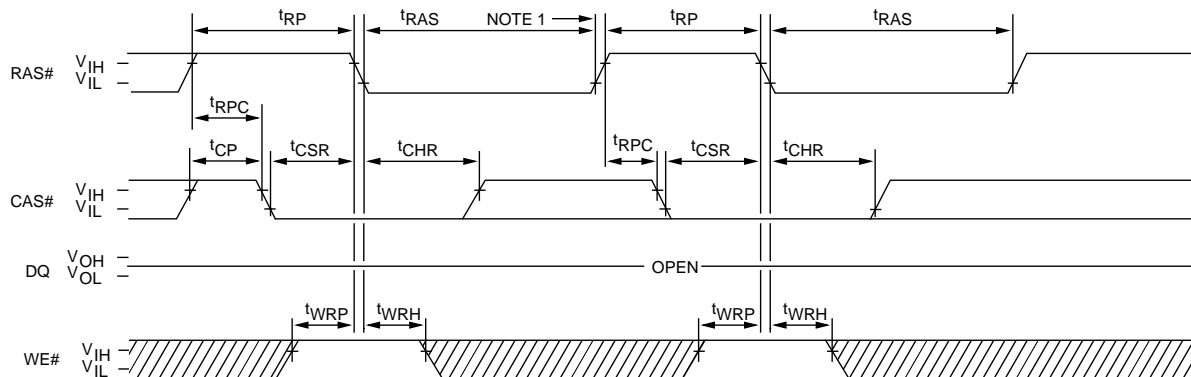
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		25		30	ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCLZ	0		0		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	38		45		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tOD	0	12	0	15	ns
tOE		12		15	ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tWHZ	0	12	0	15	ns
tWPZ	10		10		ns

RAS#-ONLY REFRESH CYCLE
(OE# and WE# = DON'T CARE)



CBR REFRESH CYCLE
(Addresses and OE# = DON'T CARE)



DON'T CARE
 UNDEFINED

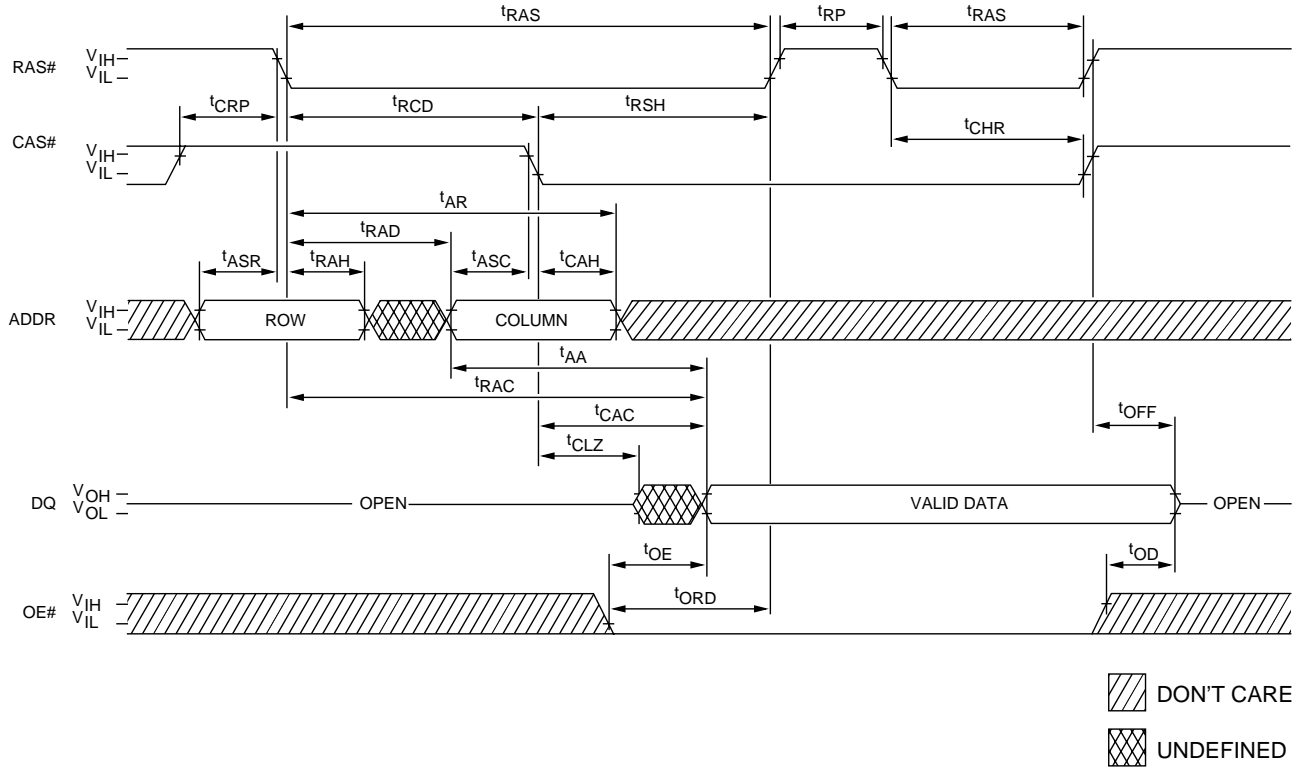
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{ASR}	0		0		ns
t _{CHR}	8		10		ns
t _{CP}	8		10		ns
t _{CRP}	5		5		ns
t _{CSR}	5		5		ns
t _{RAH}	9		10		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{RAS}	50	10,000	60	10,000	ns
t _{RC}	84		104		ns
t _{RP}	30		40		ns
t _{RPC}	5		5		ns
t _{WRH}	8		10		ns
t _{WRP}	8		10		ns

NOTE: 1. End of first CBR REFRESH cycle.

HIDDEN REFRESH CYCLE ²⁴
(WE# = HIGH; OE# = LOW)

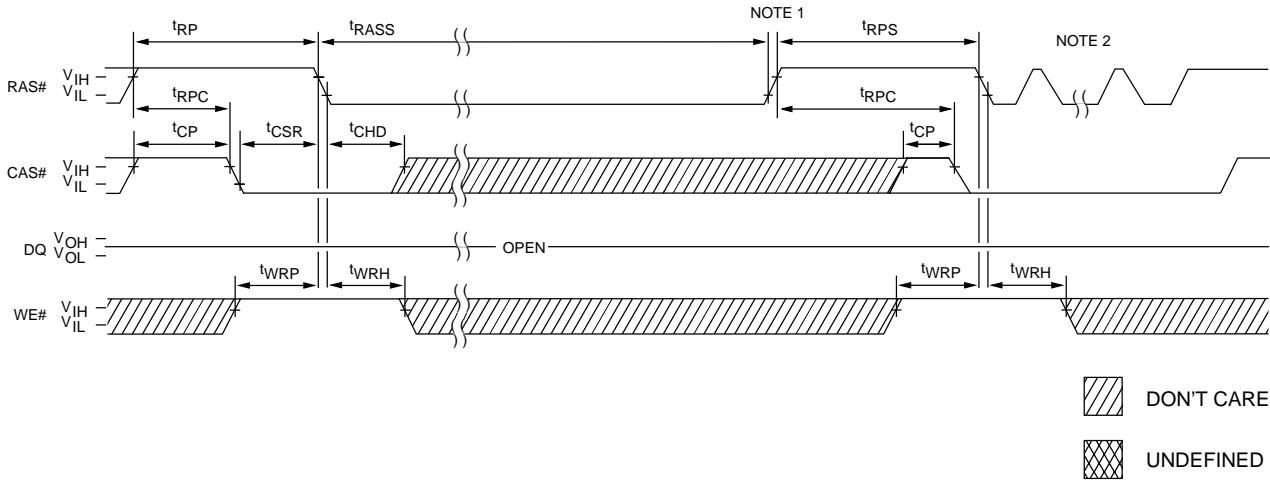


TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{AR}	38		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC}		13		15	ns
t _{CAH}	8		10		ns
t _{CHR}	8		10		ns
t _{CLZ}	0		0		ns
t _{CRP}	5		5		ns
t _{OD}	0	12	0	15	ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OE}		12		15	ns
t _{OFF}	0	12	0	15	ns
t _{ORD}	0		0		ns
t _{RAC}		50		60	ns
t _{RAD}	9		12		ns
t _{RAH}	9		10		ns
t _{RAS}	50	10,000	60	10,000	ns
t _{RCD}	11		14		ns
t _{RP}	30		40		ns
t _{RSH}	13		15		ns

SELF REFRESH CYCLE
(Addresses and OE# = DON'T CARE)



TIMING PARAMETERS

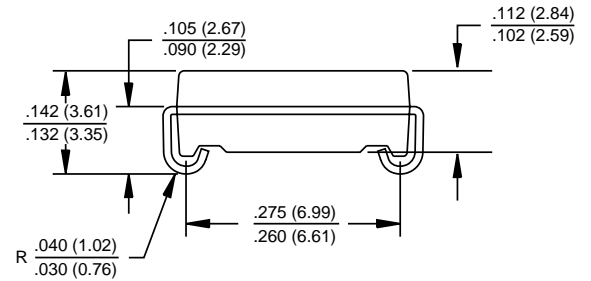
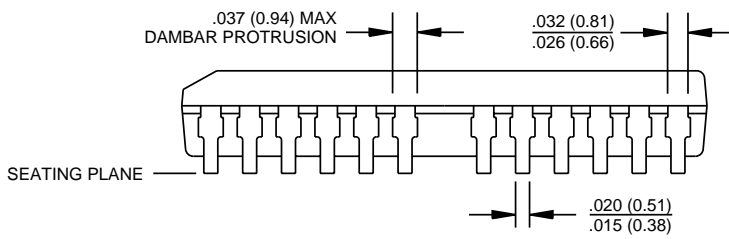
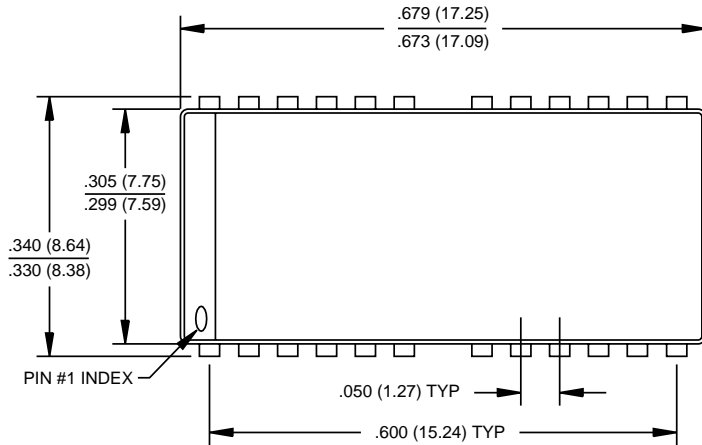
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{CHD}	15		15		ns
t_{CP}	8		10		ns
t_{CSR}	5		5		ns
t_{RASS}	100		100		μ s
t_{RP}	30		40		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{RPC}	5		5		ns
t_{RPS}	90		105		ns
t_{WRH}	8		10		ns
t_{WRP}	8		10		ns

NOTE: 1. Once t_{RASS} (MIN) is met and RAS# remains LOW, the DRAM will enter self refresh mode.
2. Once t_{RPS} is satisfied, a complete burst of all rows should be executed.

24/26-PIN PLASTIC SOJ (300 mil)

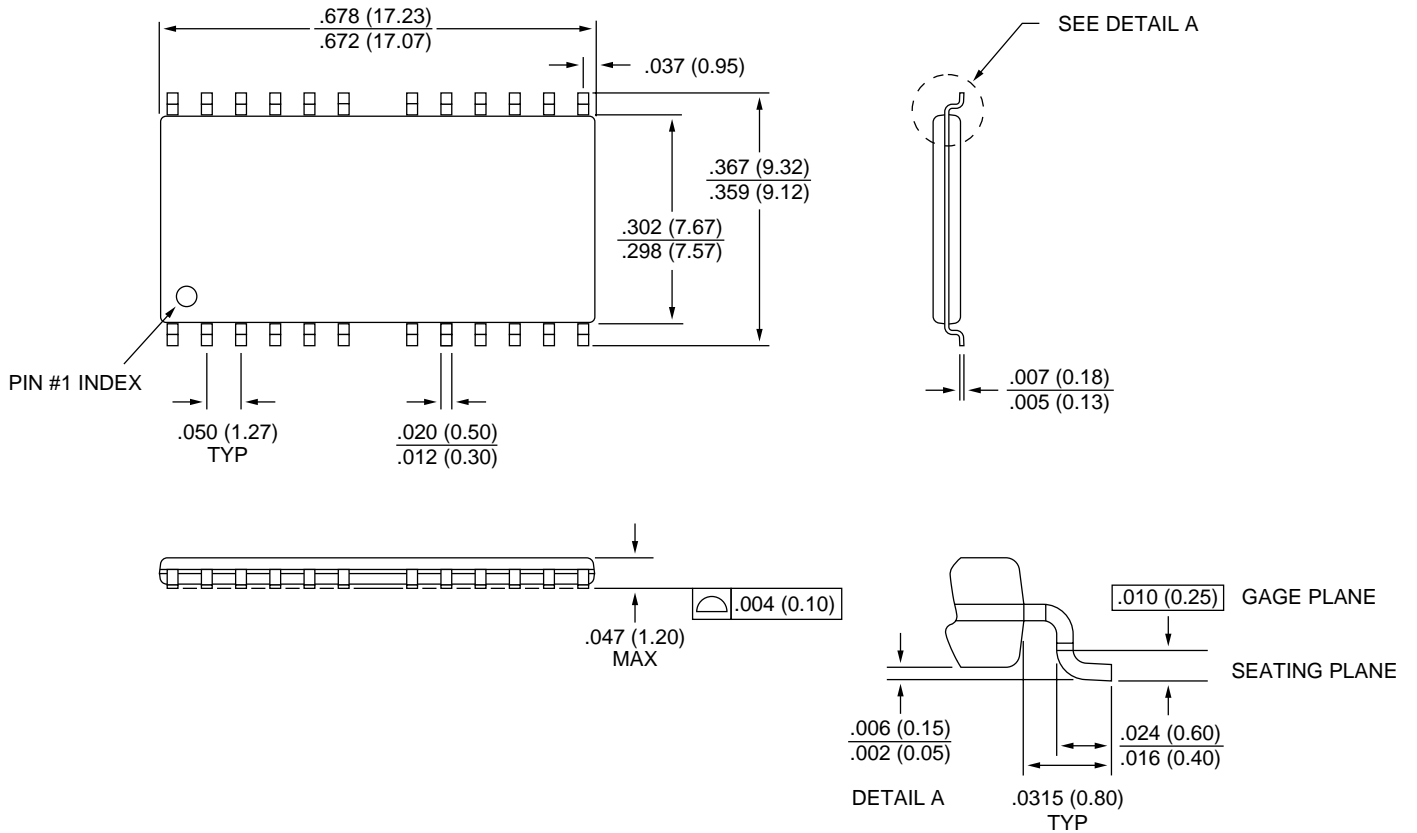
DA-1



- NOTE:**
1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
 2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

24/26-PIN PLASTIC TSOP (300 mil)

DB-1



- NOTE:**
1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.
 2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.