

16 Mbit (x16) Multi-Purpose Flash

SST39LF160 / SST39VF160



Data Sheet

FEATURES:

- **Organized as 1M x16**
- **Single Voltage Read and Write Operations**
 - 3.0-3.6V for SST39LF160
 - 2.7-3.6V for SST39VF160
- **Superior Reliability**
 - Endurance: 100,000 Cycles (typical)
 - Greater than 100 years Data Retention
- **Low Power Consumption (typical values at 14 MHz)**
 - Active Current: 12 mA (typical)
 - Standby Current: 4 μ A (typical)
 - Auto Low Power Mode: 4 μ A (typical)
- **Sector-Erase Capability**
 - Uniform 2 KWord sectors
- **Fast Read Access Time**
 - 55 ns for SST39LF160
 - 70 and 90 ns for SST39VF160
- **Latched Address and Data**
- **Fast Erase and Word-Program**
 - Sector-Erase Time: 18 ms (typical)
 - Block-Erase Time: 18 ms (typical)
 - Chip-Erase Time: 70 ms (typical)
 - Word-Program Time: 14 μ s (typical)
 - Chip Rewrite Time: 15 seconds (typical) for SST39LF/VF160
- **Automatic Write Timing**
 - Internal V_{PP} Generation
- **End-of-Write Detection**
 - Toggle Bit
 - Data# Polling
- **CMOS I/O Compatibility**
- **JEDEC Standard**
 - Flash EEPROM Pinouts and command sets
- **Packages Available**
 - 48-lead TSOP (12mm x 20mm)
 - 48-ball TFBGA (8mm x 10mm)

PRODUCT DESCRIPTION

The SST39LF/VF160 devices are 1M x16 CMOS Multi-Purpose Flash (MPF) manufactured with SST's proprietary, high performance CMOS SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain better reliability and manufacturability compared with alternate approaches. The SST39LF160 write (Program or Erase) with a 3.0-3.6V power supply. The SST39VF160 write (Program or Erase) with a 2.7-3.6V power supply. These devices conform to JEDEC standard pinouts for x16 memories.

Featuring high performance Word-Program, the SST39LF/VF160 devices provide a typical Word-Program time of 14 μ sec. These devices use Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent write, they have on-chip hardware and Software Data Protection schemes. Designed, manufactured, and tested for a wide spectrum of applications, these devices are offered with a guaranteed typical endurance of 10,000 cycles. Data retention is rated at greater than 100 years.

The SST39LF/VF160 devices are suited for applications that require convenient and economical updating of program, configuration, or data memory. For all system applications, they significantly improve performance and reliability, while lowering power consumption. They inherently use less energy during Erase and Program than alternative flash technologies. The total energy consumed is a function of the applied voltage, current, and time of

application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash technologies. These devices also improve flexibility while lowering the cost for program, data, and configuration storage applications.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles.

To meet high density, surface mount requirements, the SST39LF/VF160 are offered in a 48-lead TSOP and a 48-ball TFBGA package. See Figures 1 and 2 for pin assignments.

Device Operation

Commands are used to initiate the memory operation functions of the device. Commands are written to the device using standard microprocessor write sequences. A command is written by asserting WE# low while keeping CE# low. The address bus is latched on the falling edge of WE# or CE#, whichever occurs last. The data bus is latched on the rising edge of WE# or CE#, whichever occurs first.



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The SST39LF/VF160 also have the **Auto Low Power** mode which puts the device in a near standby mode after data has been accessed with a valid Read operation. This reduces the I_{DD} active read current from typically 15 mA to typically 4 μ A. The Auto Low Power mode reduces the typical I_{DD} active read current to the range of 1 mA/MHz of read cycle time. The device exits the Auto Low Power mode with any address transition or control signal transition used to initiate another Read cycle, with no access time penalty. Note that the device does not enter Auto Low Power mode after power-up with CE# held steadily low until the first address transition or CE# is driven high.

Read

The Read operation of the SST39LF/VF160 is controlled by CE# and OE#, both have to be low for the system to obtain data from the outputs. CE# is used for device selection. When CE# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 3).

Word-Program Operation

The SST39LF/VF160 are programmed on a word-by-word basis. Before programming, the sector where the word exists must be fully erased. The Program operation is accomplished in three steps. The first step is the three-byte load sequence for Software Data Protection. The second step is to load word address and word data. During the Word-Program operation, the addresses are latched on the falling edge of either CE# or WE#, whichever occurs last. The data is latched on the rising edge of either CE# or WE#, whichever occurs first. The third step is the internal Program operation which is initiated after the rising edge of the fourth WE# or CE#, whichever occurs first. The Program operation, once initiated, will be completed within 20 μ s. See Figures 4 and 5 for WE# and CE# controlled Program operation timing diagrams and Figure 16 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during the internal Program operation are ignored.

Sector-/Block-Erase Operation

The Sector- (or Block-) Erase operation allows the system to erase the device on a sector-by-sector (or block-by-block) basis. The SST39LF/VF160 offer both Sector-Erase and Block-Erase modes. The sector architecture is based on uniform sector size of 2 KWord. The Block-Erase mode

is based on uniform block size of 32 KWord. The Sector-Erase operation is initiated by executing a six-byte command sequence with Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (50H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. The End-of-Erase operation can be determined using either Data# Polling or Toggle Bit methods. See Figures 9 and 10 for timing waveforms. Any commands issued during the Sector- or Block-Erase operation are ignored.

Chip-Erase Operation

The SST39LF/VF160 provide a Chip-Erase operation, which allows the user to erase the entire memory array to the "1" state. This is useful when the entire device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 5555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or CE#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bit or Data# Polling. See Table 4 for the command sequence, Figure 8 for timing diagram, and Figure 19 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.

Write Operation Status Detection

The SST39LF/VF160 provide two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ₇) and Toggle Bit (DQ₆). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling or Toggle Bit read may be simultaneous with the completion of the write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ₇ or DQ₆. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.



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Data# Polling (DQ₇)

When the SST39LF/VF160 are in the internal Program operation, any attempt to read DQ₇ will produce the complement of the true data. Once the Program operation is completed, DQ₇ will produce true data. Note that even though DQ₇ may have valid data immediately following the completion of an internal Write operation, the remaining data outputs may still be invalid: valid data on the entire data bus will appear in subsequent successive Read cycles after an interval of 1 μ s. During internal Erase operation, any attempt to read DQ₇ will produce a '0'. Once the internal Erase operation is completed, DQ₇ will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block- or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 6 for Data# Polling timing diagram and Figure 17 for a flowchart.

Toggle Bit (DQ₆)

During the internal Program or Erase operation, any consecutive attempts to read DQ₆ will produce alternating 1s and 0s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ₆ bit will stop toggling. The Toggle Bit is valid after the rising edge of fourth WE# (or CE#) pulse for Program operation. For Sector-, Block- or Chip-Erase, the Toggle Bit is valid after the rising edge of sixth WE# (or CE#) pulse. See Figure 7 for Toggle Bit timing diagram and Figure 17 for a flowchart.

Data Protection

The SST39LF/VF160 provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or CE# pulse of less than 5 ns will not initiate a write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, CE# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Software Data Protection (SDP)

The SST39LF/VF160 provide the JEDEC approved Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte sequence. These devices are shipped with the Software Data Protection permanently enabled. See Table 4 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within T_{RC}. The contents of DQ₁₅-DQ₈ can be V_{IL} or V_{IH}, but no other value, during any SDP command sequence.

Common Flash Memory Interface (CFI)

The SST39LF/VF160 also contain the CFI information to describe the characteristics of the device. In order to enter the CFI Query mode, the system must load the three-byte sequence, similar to the Software ID Entry command. The last byte cycle of this command loads 98H (CFI Query command) to address 5555H. Once the device enters the CFI Query mode, the system can read CFI data at the addresses given in Tables 5 through 7. The system must write the CFI Exit command to return to Read mode from the CFI Query mode.

Product Identification

The Product Identification mode identifies the devices as the SST39LF/VF160 and manufacturer as SST. This mode may be accessed by software operations. Users may use the Software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Table 4 for software operation, Figure 11 for the Software ID Entry and Read timing diagram, and Figure 18 for the Software ID Entry command sequence flowchart.

TABLE 1: PRODUCT IDENTIFICATION

	Address	Data
Manufacturer's ID	0000H	00BFH
Device ID SST39LF/VF160	0001H	2782H

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**Product Identification Mode Exit/
CFI Mode Exit**

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read mode. This command may also be used to reset the device to the

Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. Please note that the Software ID Exit/CFI Exit command is ignored during an internal Program or Erase operation. See Table 4 for software command codes, Figure 13 for timing waveform, and Figure 18 for a flowchart.

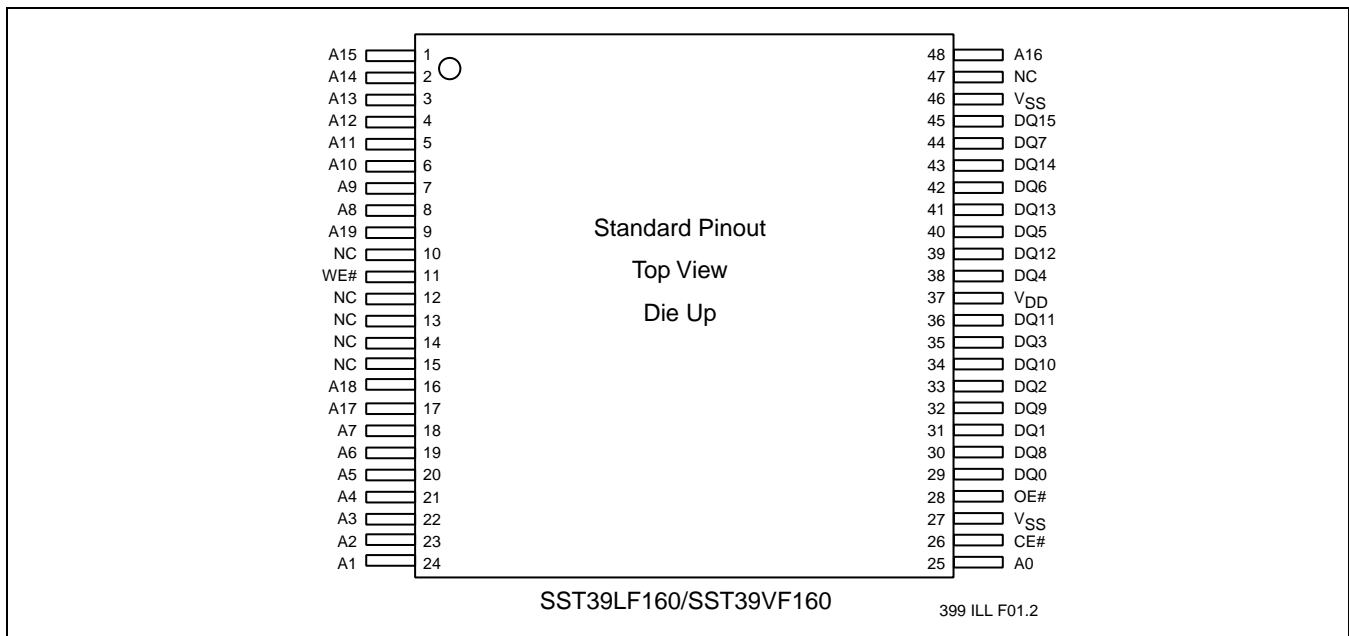
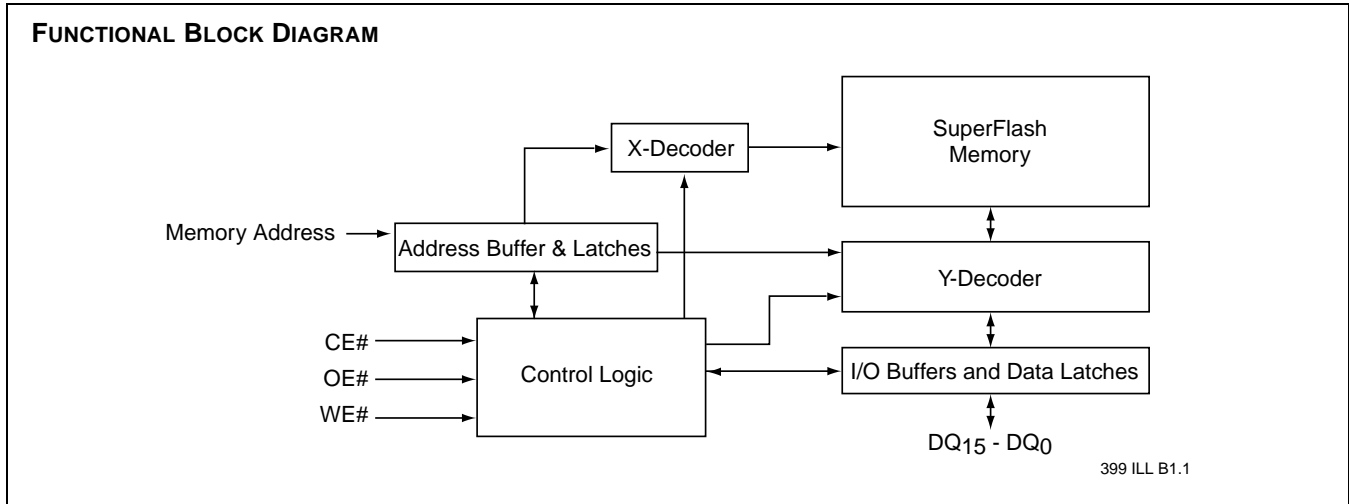


FIGURE 1: PIN ASSIGNMENTS FOR 48-LEAD TSOP



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TABLE 3: OPERATION MODES SELECTION

Mode	CE#	OE#	WE#	DQ	Address
Read	V _{IL}	V _{IL}	V _{IH}	D _{OUT}	A _{IN}
Program	V _{IL}	V _{IH}	V _{IL}	D _{IN}	A _{IN}
Erase	V _{IL}	V _{IH}	V _{IL}	X ¹	Sector or Block address, XXH for Chip-Erase
Standby	V _{IH}	X	X	High Z	X
Write Inhibit	X	V _{IL}	X	High Z/ D _{OUT}	X
	X	X	V _{IH}	High Z/ D _{OUT}	X
Product Identification					
Software Mode	V _{IL}	V _{IL}	V _{IH}		See Table 4

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1. X can be V_{IL} or V_{IH}, but no other value

TABLE 4: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr ¹	Data ²	Addr ¹	Data ²	Addr ¹	Data ²	Addr ¹	Data ²	Addr ¹	Data ²	Addr ¹	Data ²
Word-Program	5555H	AAH	2AAAH	55H	5555H	A0H	WA ³	Data				
Sector-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA _X ⁴	30H
Block-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	BA _X ⁴	50H
Chip-Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Software ID Entry ^{5,6}	5555H	AAH	2AAAH	55H	5555H	90H						
CFI Query Entry ⁵	5555H	AAH	2AAAH	55H	5555H	98H						
Software ID Exit ⁷ / CFI Exit	XXH	F0H										
Software ID Exit ⁷ / CFI Exit	5555H	AAH	2AAAH	55H	5555H	F0H						

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1. Address format A₁₄-A₀ (Hex), Addresses A₁₉-A₁₅ can be V_{IL} or V_{IH}, but no other value, for Command sequence for SST39LF/VF160
2. DQ₁₅ - DQ₈ can be V_{IL} or V_{IH}, but no other value, for Command sequence
3. WA = Program word address
4. SA_X for Sector-Erase; uses A₁₉-A₁₁ address lines
BA_X, for Block-Erase; uses A₁₉-A₁₅ address lines
5. The device does not remain in Software Product ID mode if powered down.
6. With A₁₉-A₁ = 0; SST Manufacturer's ID = 00BFH, is read with A₀ = 0,
SST39LF/VF160 Device ID = 2782H, is read with A₀ = 1
7. Both Software ID Exit operations are equivalent



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TABLE 5: CFI QUERY IDENTIFICATION STRING¹ FOR SST39LF/VF160

Address	Data	Data
10H	0051H	Query Unique ASCII string "QRY"
11H	0052H	
12H	0059H	
13H	0001H	Primary OEM command set
14H	0007H	
15H	0000H	Address for Primary Extended Table
16H	0000H	
17H	0000H	Alternate OEM command set (00H = none exists)
18H	0000H	
19H	0000H	Address for Alternate OEM extended Table (00H = none exists)
1AH	0000H	

1. Refer to CFI publication 100 for more details.

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TABLE 6: SYSTEM INTERFACE INFORMATION FOR SST39LF/VF160

Address	Data	Data
1BH	0027H ¹	V _{DD} Min (Program/Erase)
	0030H ¹	DQ ₇ -DQ ₄ : Volts, DQ ₃ -DQ ₀ : 100 millivolts
1CH	0036H	V _{DD} Max (Program/Erase) DQ ₇ -DQ ₄ : Volts, DQ ₃ -DQ ₀ : 100 millivolts
1DH	0000H	V _{PP} min (00H = no V _{PP} pin)
1EH	0000H	V _{PP} max (00H = no V _{PP} pin)
1FH	0004H	Typical time out for Word-Program 2 ^N μs (2 ⁴ = 16 μs)
20H	0000H	Typical time out for min size buffer program 2 ^N μs (00H = not supported)
21H	0004H	Typical time out for individual Sector/Block-Erase 2 ^N ms (2 ⁴ = 16 ms)
22H	0006H	Typical time out for Chip-Erase 2 ^N ms (2 ⁶ = 64 ms)
23H	0001H	Maximum time out for Word-Program 2 ^N times typical (2 ¹ x 2 ⁴ = 32 μs)
24H	0000H	Maximum time out for buffer program 2 ^N times typical
25H	0001H	Maximum time out for individual Sector/Block-Erase 2 ^N times typical (2 ¹ x 2 ⁴ = 32 ms)
26H	0001H	Maximum time out for Chip-Erase 2 ^N times typical (2 ¹ x 2 ⁶ = 128 ms)

1. 0030H for SST39LF160 and 0027H for SST39VF160

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TABLE 7: DEVICE GEOMETRY INFORMATION FOR SST39LF/VF160

Address	Data	Data
27H	0015H	Device size = 2 ^N Bytes (15H = 21; 2 ²¹ = 2 MByte)
28H	0001H	Flash Device Interface description; 0001H = x16-only asynchronous interface
29H	0000H	
2AH	0000H	Maximum number of bytes in multi-byte write = 2 ^N (00H = not supported)
2BH	0000H	
2CH	0002H	Number of Erase Sector/Block sizes supported by device
2DH	00FFH	Sector Information (y + 1 = Number of sectors; z x 256B = sector size)
2EH	0001H	
2FH	0010H	
30H	0000H	
31H	003FH	Block Information (y + 1 = Number of blocks; z x 256B = block size)
32H	0000H	
33H	0000H	
34H	0001H	

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Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential	-0.5V to $V_{DD}+0.5V$
Transient Voltage (<20 ns) on Any Pin to Ground Potential	-2.0V to $V_{DD}+2.0V$
Voltage on A ₉ Pin to Ground Potential	-0.5V to 13.2V
Package Power Dissipation Capability (Ta = 25°C)	1.0W
Surface Mount Lead Soldering Temperature (3 Seconds)	240°C
Output Short Circuit Current ¹	50 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE: SST39LF160

Range	Ambient Temp	V _{DD}
Commercial	0°C to +70°C	3.0-3.6V

OPERATING RANGE: SST39VF160

Range	Ambient Temp	V _{DD}
Commercial	0°C to +70°C	2.7-3.6V
Industrial	-40°C to +85°C	2.7-3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time	5 ns
Output Load	CL = 30 pF for SST39LF160
Output Load	CL = 100 pF for SST39VF160
See Figures 14 and 15	



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TABLE 8: DC OPERATING CHARACTERISTICS
 $V_{DD} = 3.0\text{-}3.6\text{V}$ FOR SST39LF160 AND $2.7\text{-}3.6\text{V}$ FOR SST39VF160¹

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}	Power Supply Current				Address input= V_{ILT}/V_{IHT} , at $f=1/T_{RC}$ Min, $V_{DD}=V_{DD}$ Max
	Read ²		20	mA	$CE\#=V_{IL}$, $OE\#=WE\#=V_{IH}$, all I/Os open
	Program and Erase		30	mA	$CE\#=WE\#=V_{IL}$, $OE\#=V_{IH}$
I_{SB}	Standby V_{DD} Current		20	μA	$CE\#=V_{IHC}$, $V_{DD}=V_{DD}$ Max
I_{ALP}	Auto Low Power Current		20	μA	$CE\#=V_{ILC}$, $V_{DD}=V_{DD}$ Max, all inputs = V_{SS} or V_{DD} , $WE\#=V_{IHC}$
I_{LI}	Input Leakage Current		1	μA	$V_{IN}=\text{GND to } V_{DD}$, $V_{DD}=V_{DD}$ Max
I_{LO}	Output Leakage Current		10	μA	$V_{OUT}=\text{GND to } V_{DD}$, $V_{DD}=V_{DD}$ Max
V_{IL}	Input Low Voltage		0.8	V	$V_{DD}=V_{DD}$ Min
V_{ILC}	Input Low Voltage (CMOS)		0.3	V	$V_{DD}=V_{DD}$ Max
V_{IH}	Input High Voltage	$0.7 V_{DD}$		V	$V_{DD}=V_{DD}$ Max
V_{IHC}	Input High Voltage (CMOS)	$V_{DD}-0.3$		V	$V_{DD}=V_{DD}$ Max
V_{OL}	Output Low Voltage		0.2	V	$I_{OL}=100 \mu\text{A}$, $V_{DD}=V_{DD}$ Min
V_{OH}	Output High Voltage	$V_{DD}-0.2$		V	$I_{OH} = -100 \mu\text{A}$, $V_{DD}=V_{DD}$ Min

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1. Typical conditions for the Active Current shown on the front data sheet page are average values at 25°C (room temperature), and $V_{DD} = 3\text{V}$ for VF devices or $V_{DD} = 5\text{V}$ for SF devices. Not 100% tested.
2. Values are for 70 ns conditions. See the *Multi-Purpose Flash Power Rating* application note for further information.

TABLE 9: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}^1$	Power-up to Read Operation	100	μs
$T_{PU-WRITE}^1$	Power-up to Program/Erase Operation	100	μs

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: CAPACITANCE ($T_a = 25^\circ\text{C}$, $f=1$ Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}^1$	I/O Pin Capacitance	$V_{I/O} = 0\text{V}$	12 pF
C_{IN}^1	Input Capacitance	$V_{IN} = 0\text{V}$	6 pF

T10.0 399

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 11: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
$N_{END}^{1,2}$	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}^1	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}^1	Latch Up	$100 + I_{DD}$	mA	JEDEC Standard 78

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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. N_{END} endurance rating is qualified as a 10,000 cycle minimum for the whole device. A sector- or block-level rating would result in a higher minimum specification.



AC CHARACTERISTICS

TABLE 12: READ CYCLE TIMING PARAMETERS $V_{DD} = 3.0-3.6V$ FOR SST39LF160 AND $2.7-3.6V$ FOR SST39VF160

Symbol	Parameter	SST39LF160-55		SST39VF160-70		SST39VF160-90		Units
		Min	Max	Min	Max	Min	Max	
T_{RC}	Read Cycle Time	55		70		90		ns
T_{CE}	Chip Enable Access Time		55		70		90	ns
T_{AA}	Address Access Time		55		70		90	ns
T_{OE}	Output Enable Access Time		30		35		45	ns
T_{CLZ}^1	CE# Low to Active Output	0		0		0		ns
T_{OLZ}^1	OE# Low to Active Output	0		0		0		ns
T_{CHZ}^1	CE# High to High-Z Output		15		20		30	ns
T_{OHZ}^1	OE# High to High-Z Output		15		20		30	ns
T_{OH}^1	Output Hold from Address Change	0		0		0		ns

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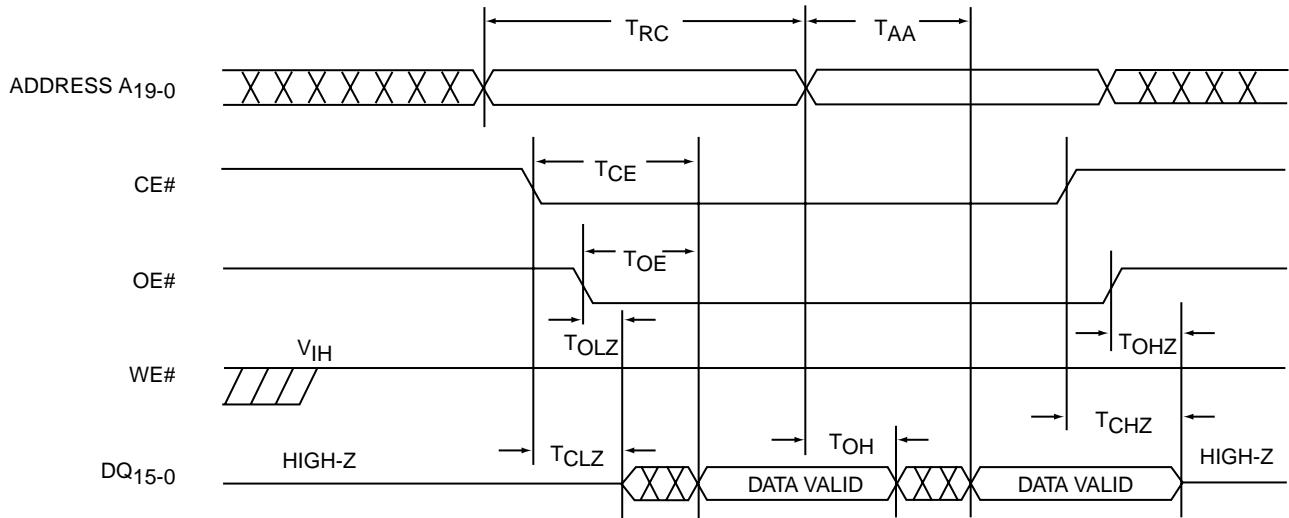
1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 13: PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{BP}	Word-Program Time		20	μs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	30		ns
T_{CS}	WE# and CE# Setup Time	0		ns
T_{CH}	WE# and CE# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{CP}	CE# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH}^1	WE# Pulse Width High	30		ns
T_{CPH}^1	CE# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
T_{DH}^1	Data Hold Time	0		ns
T_{IDA}^1	Software ID Access and Exit Time		150	ns
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase		100	ms

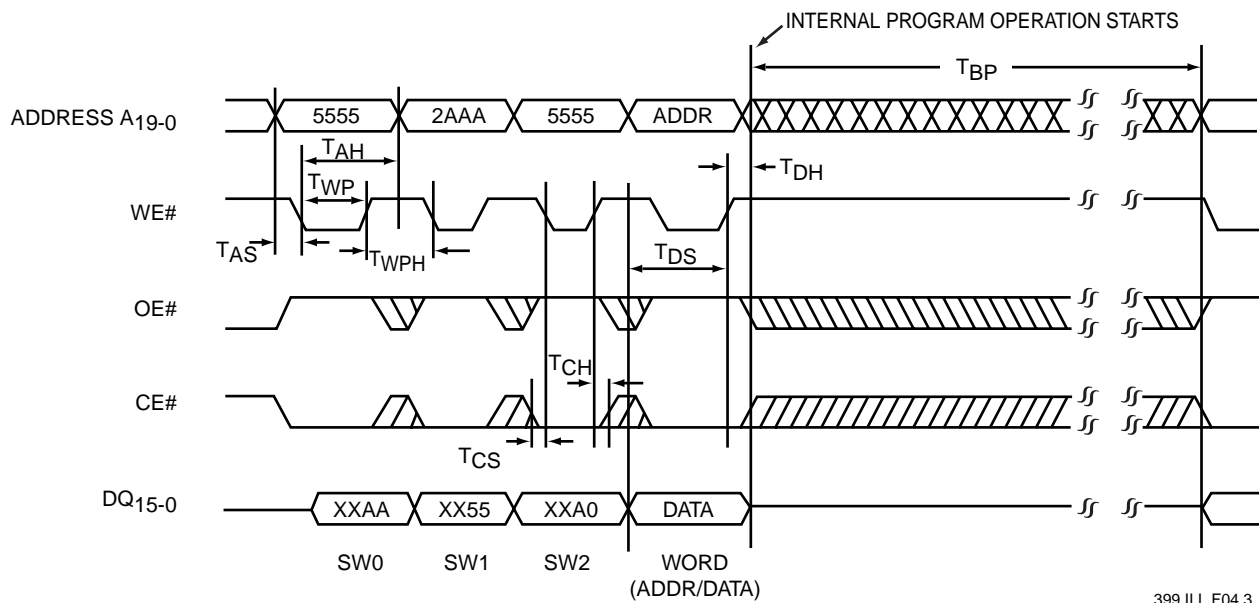
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1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



399 ILL F03.2

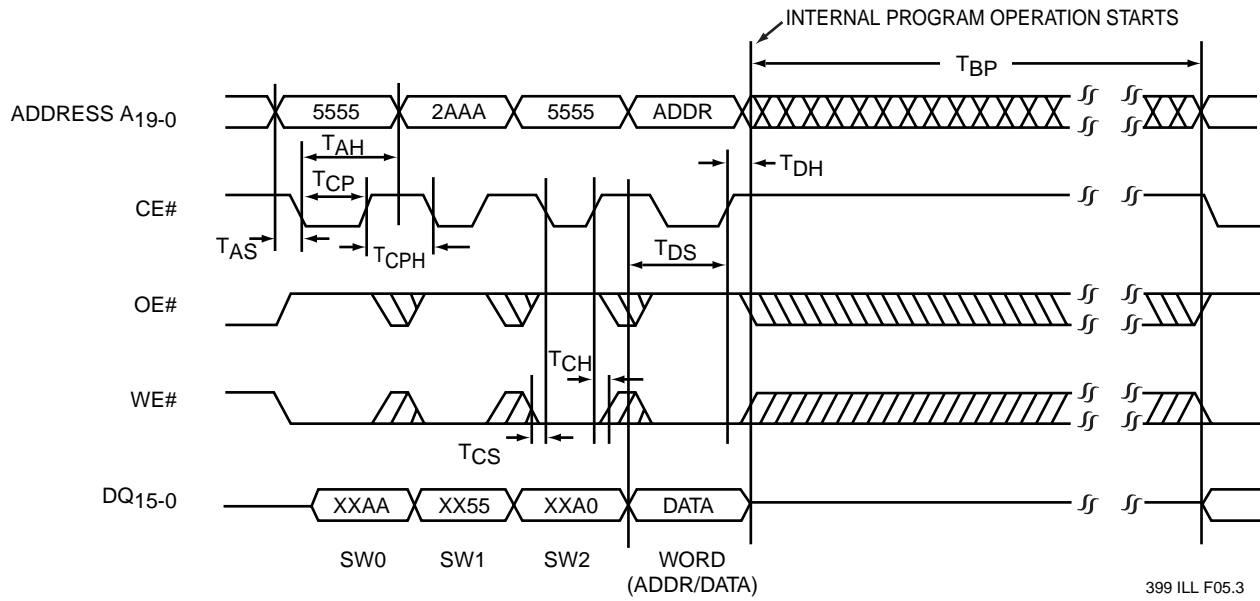
FIGURE 3: READ CYCLE TIMING DIAGRAM



399 ILL F04.3

Note: X can be V_{IL} or V_{IH} , but no other value

FIGURE 4: WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



Note: X can be V_{IL} or V_{IH}, but no other value

FIGURE 5: CE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM

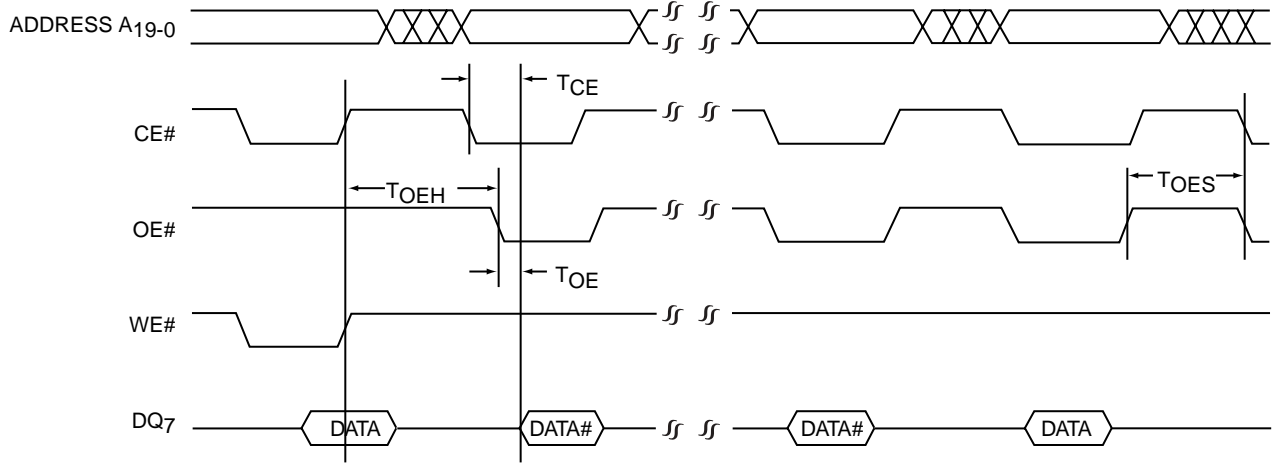
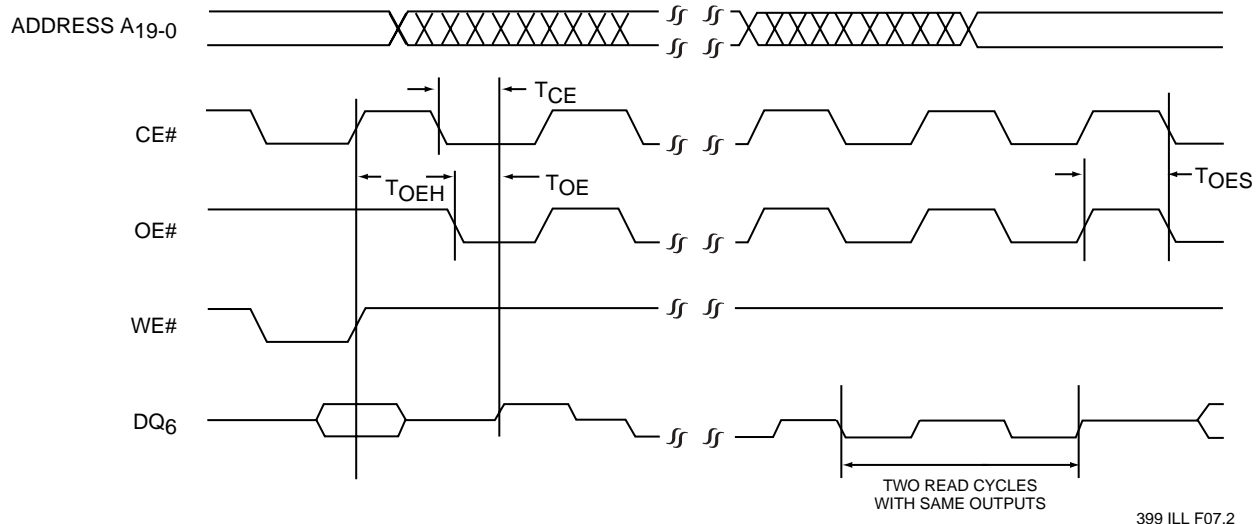
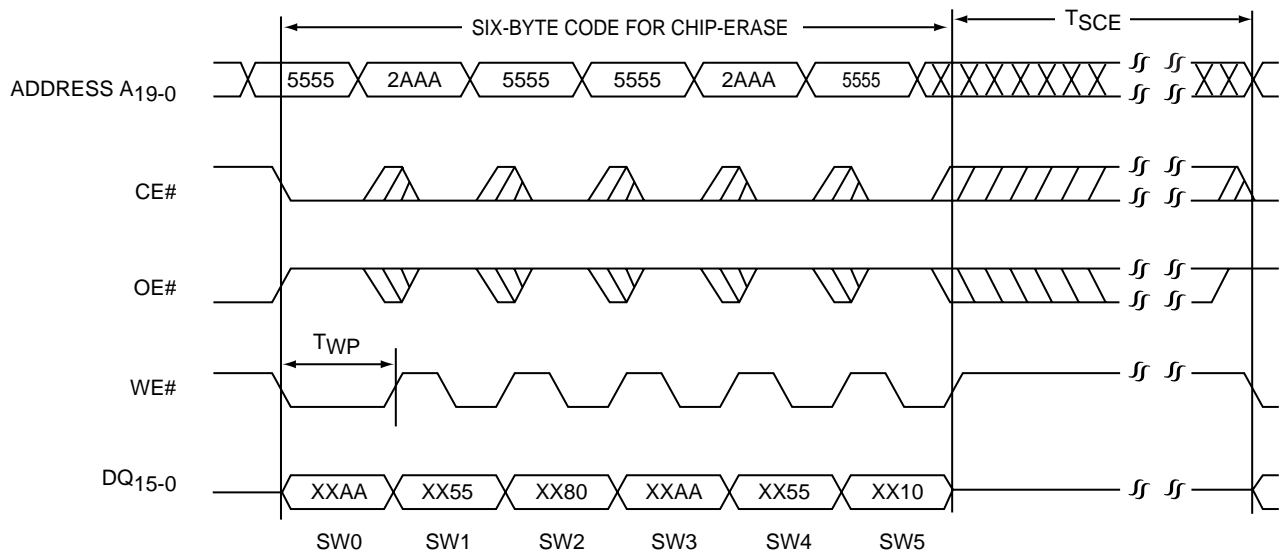


FIGURE 6: DATA# POLLING TIMING DIAGRAM



399 ILL F07.2

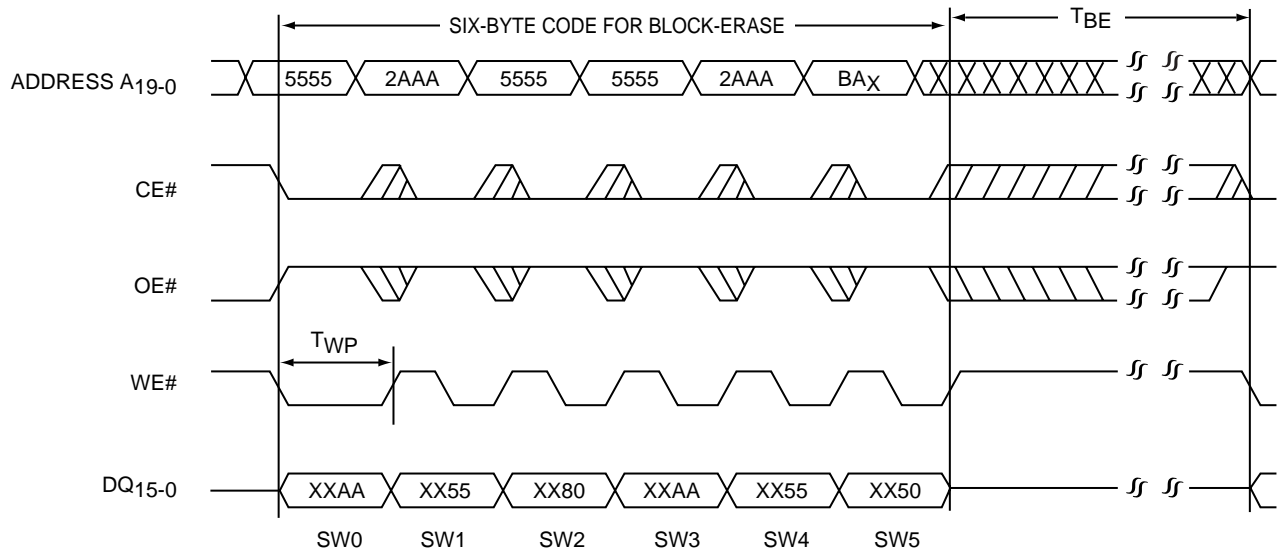
FIGURE 7: TOGGLE BIT TIMING DIAGRAM



399 ILL F08.3

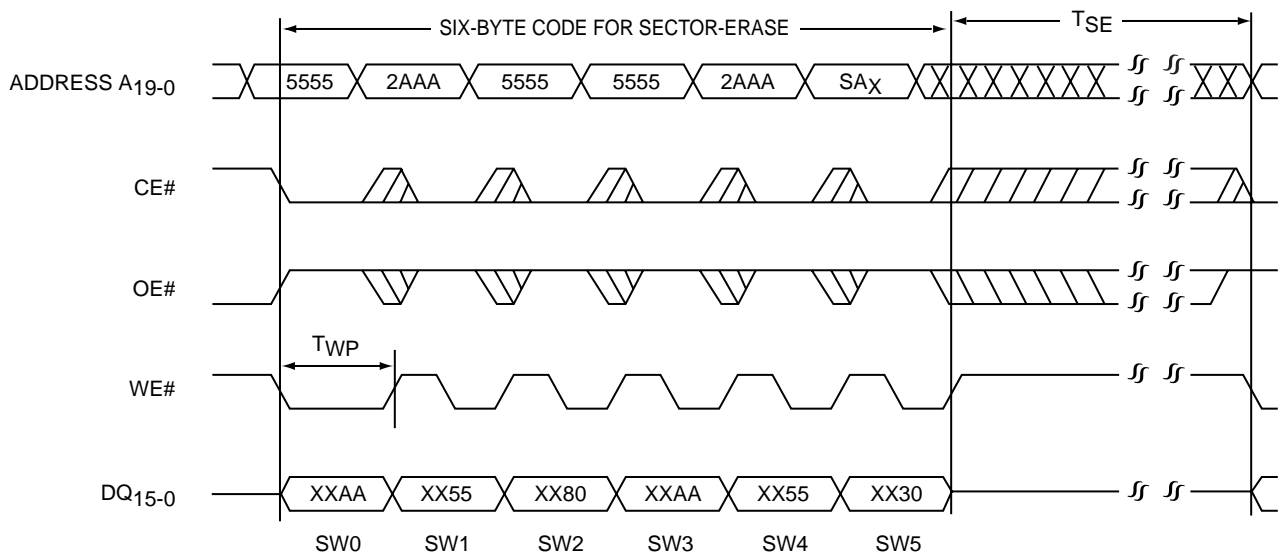
Note: This device also supports CE# controlled Chip-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 13)
X can be V_{IL} or V_{IH} , but no other value

FIGURE 8: WE# CONTROLLED CHIP-ERASE TIMING DIAGRAM



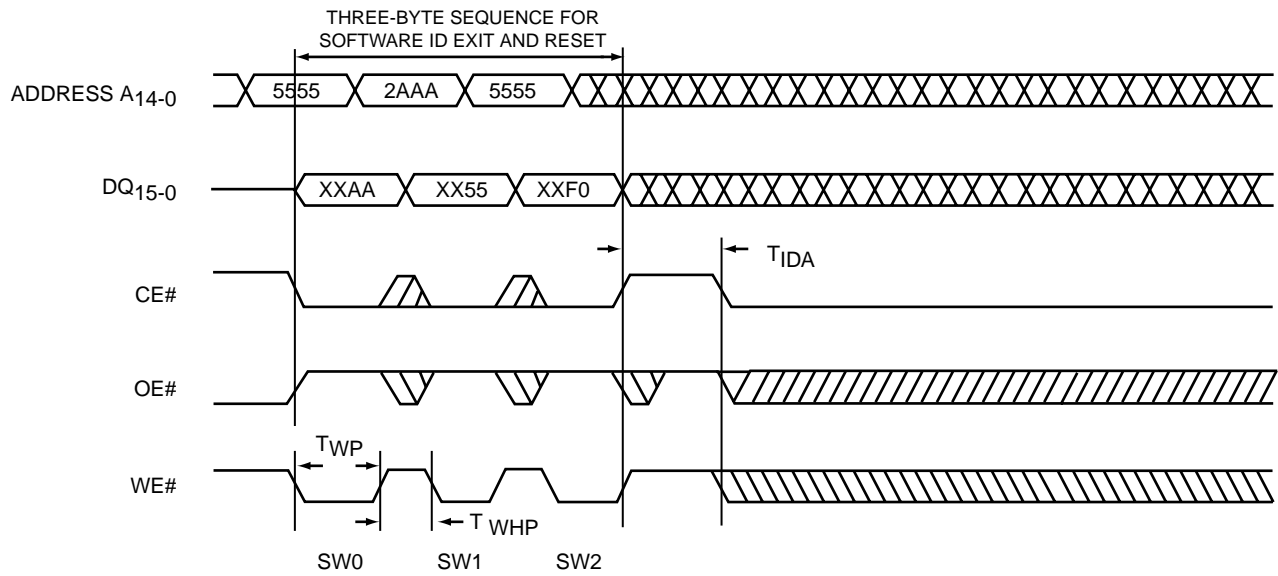
Note: This device also supports CE# controlled Block-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 13)
 BA_x = Block Address
 X can be V_{IL} or V_{IH} , but no other value

FIGURE 9: WE# CONTROLLED BLOCK-ERASE TIMING DIAGRAM



Note: This device also supports CE# controlled Sector-Erase operation. The WE# and CE# signals are interchangeable as long as minimum timings are met. (See Table 13)
 SA_x = Sector Address
 X can be V_{IL} or V_{IH} , but no other value

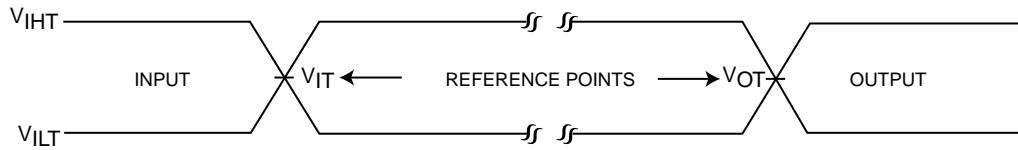
FIGURE 10: WE# CONTROLLED SECTOR-ERASE TIMING DIAGRAM



Note: X can be V_{IL} or V_{IH} , but no other value

399 ILL F10.1

FIGURE 13: SOFTWARE ID EXIT/CFI EXIT



AC test inputs are driven at V_{IHT} ($0.9 V_{DD}$) for a logic "1" and V_{ILT} ($0.1 V_{DD}$) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} ($0.5 V_{DD}$) and V_{OT} ($0.5 V_{DD}$). Input rise and fall times ($10\% \leftrightarrow 90\%$) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
 V_{OT} - V_{OUTPUT} Test
 V_{IHT} - V_{INPUT} HIGH Test
 V_{ILT} - V_{INPUT} LOW Test

FIGURE 14: AC INPUT/OUTPUT REFERENCE WAVEFORMS

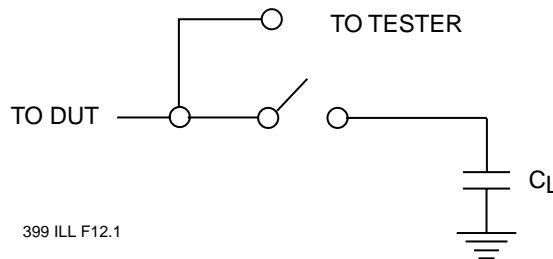


FIGURE 15: A TEST LOAD EXAMPLE

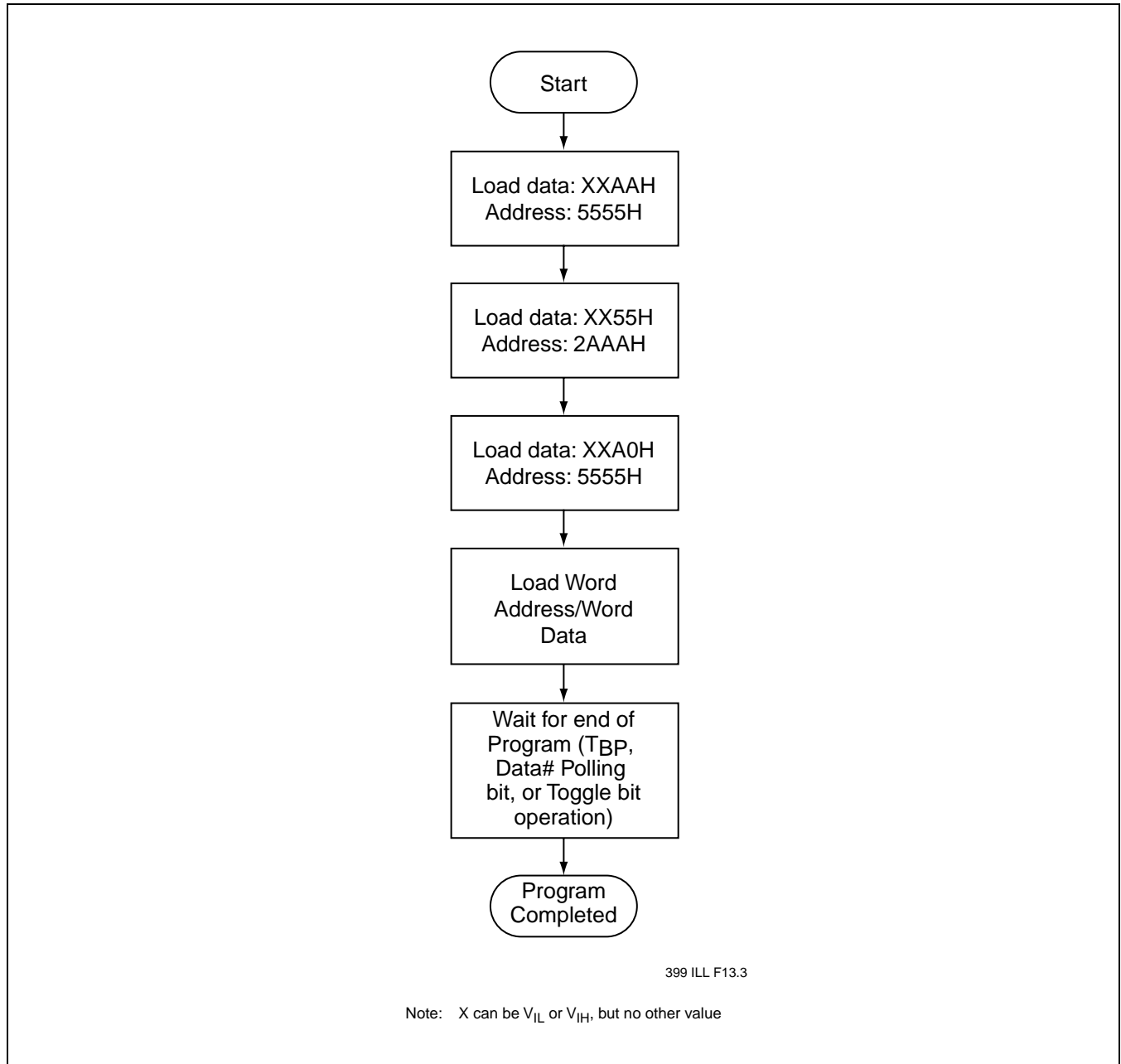


FIGURE 16: WORD-PROGRAM ALGORITHM

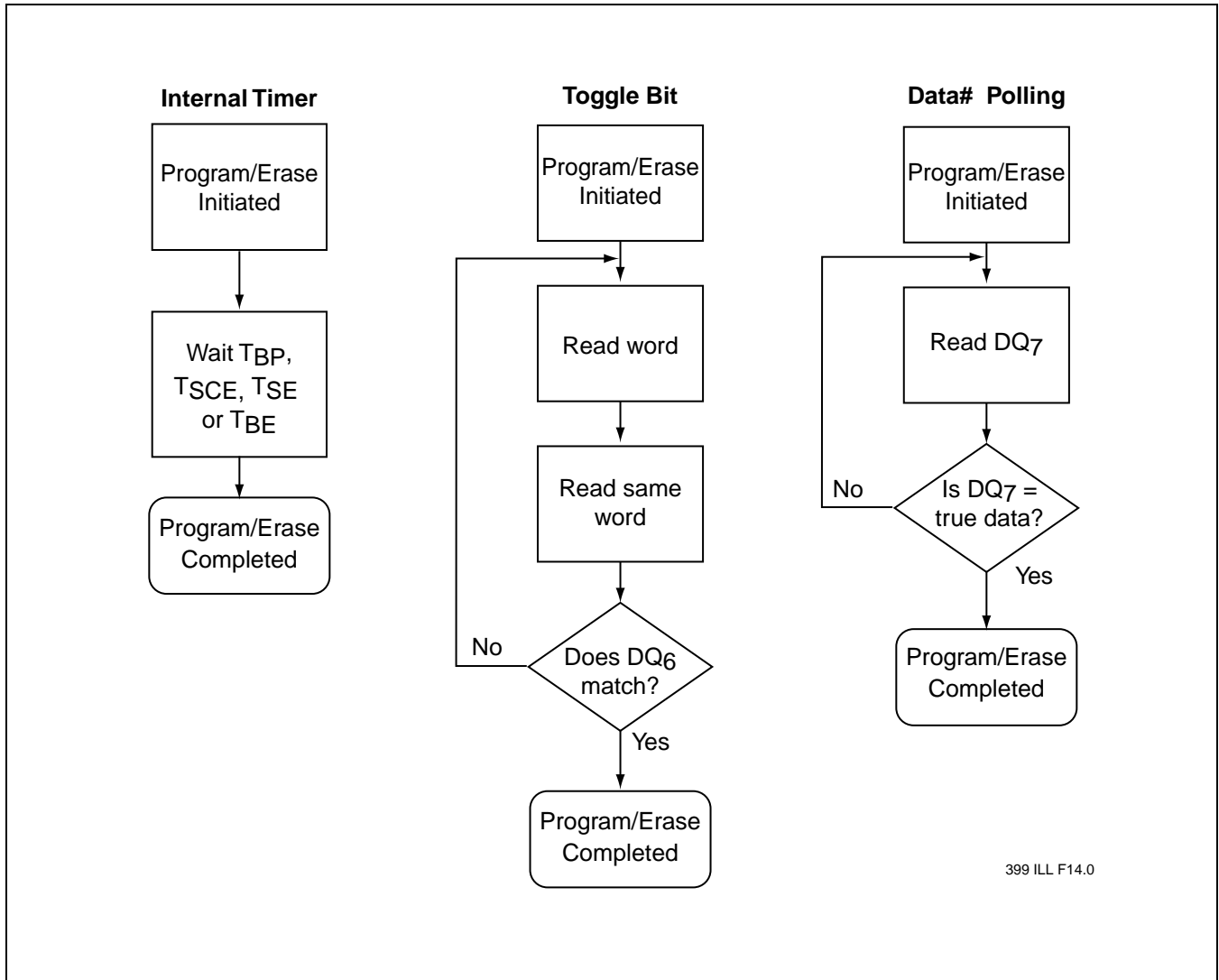


FIGURE 17: WAIT OPTIONS

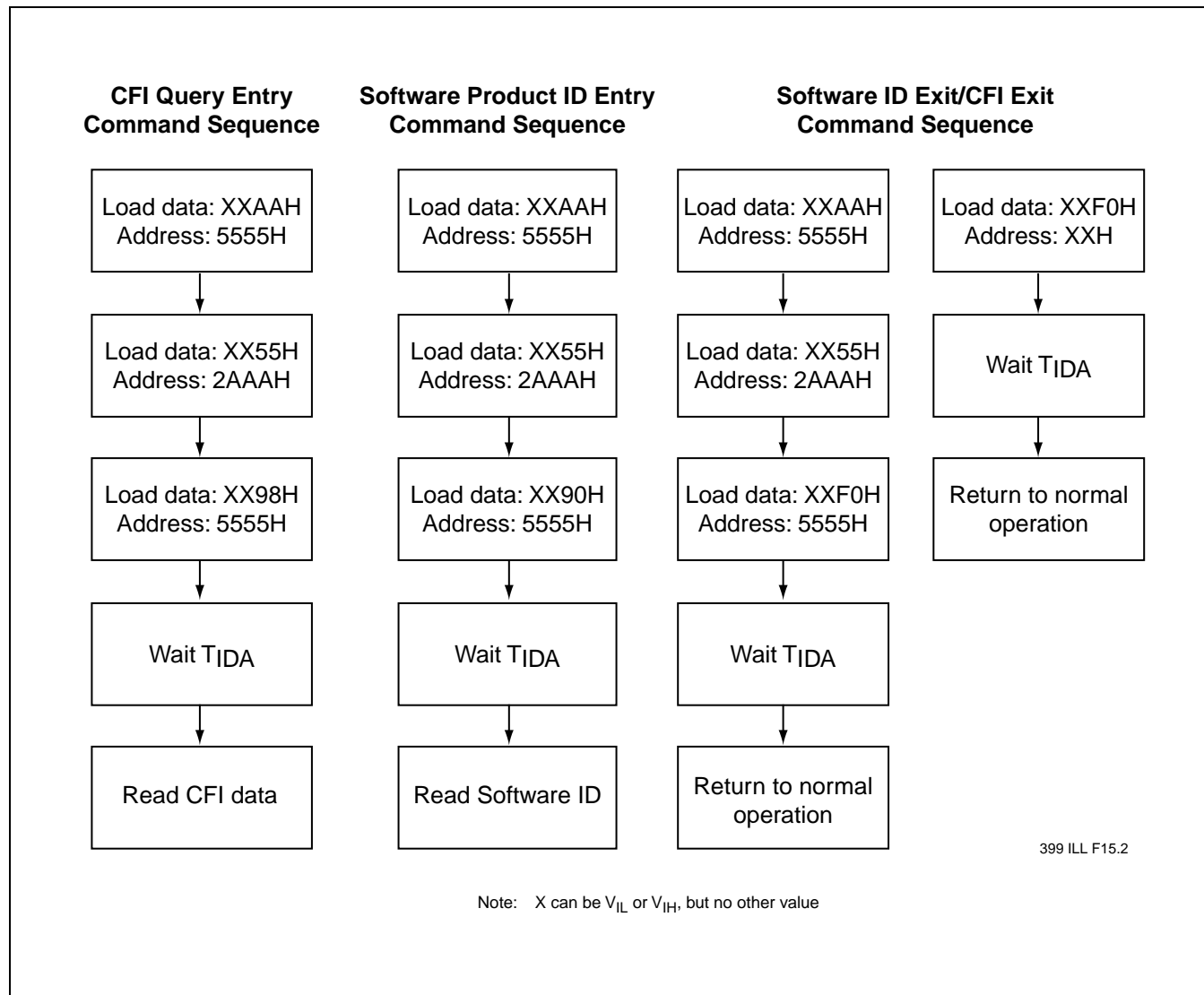


FIGURE 18: SOFTWARE PRODUCT ID/CFI COMMAND FLOWCHARTS

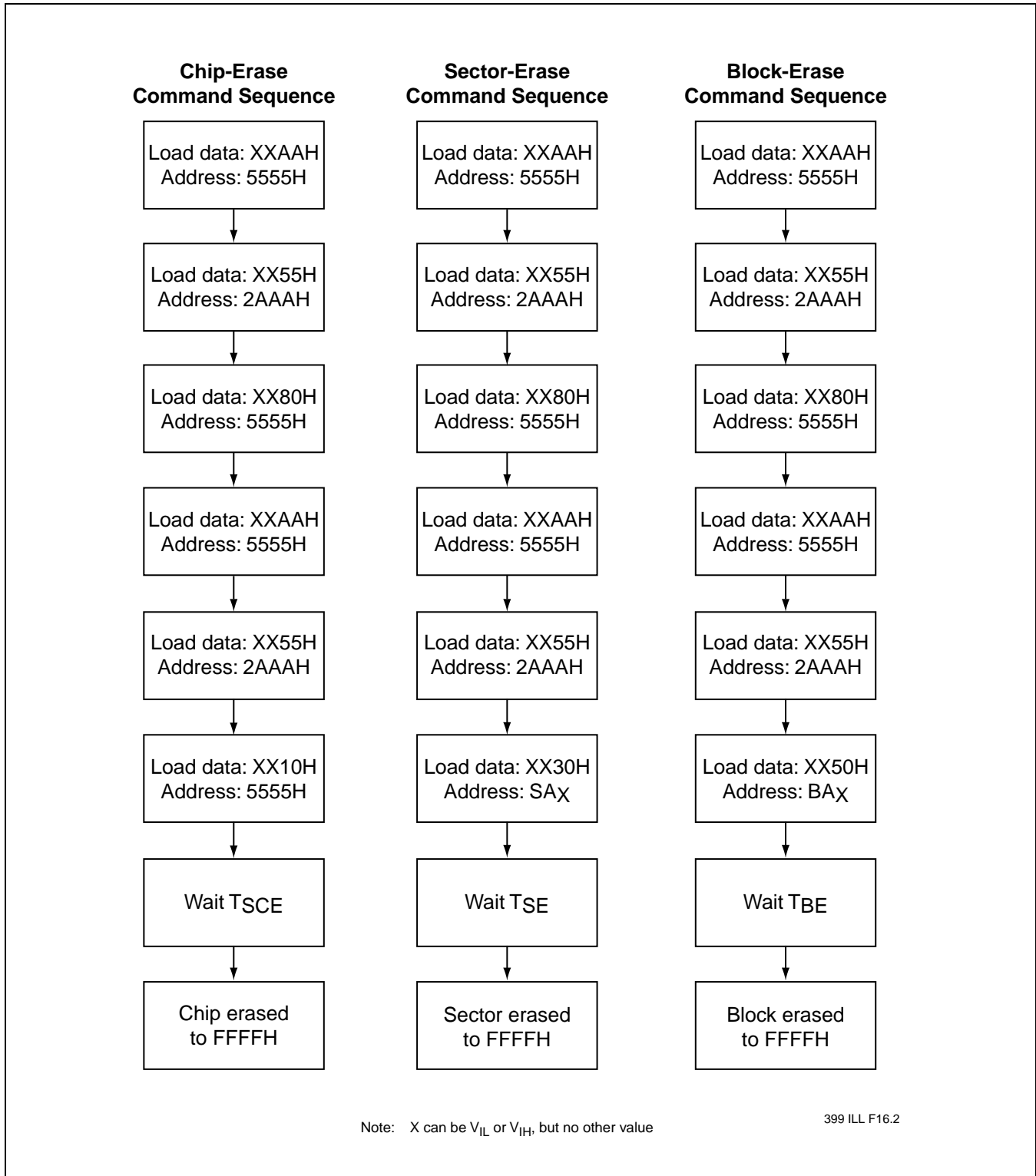
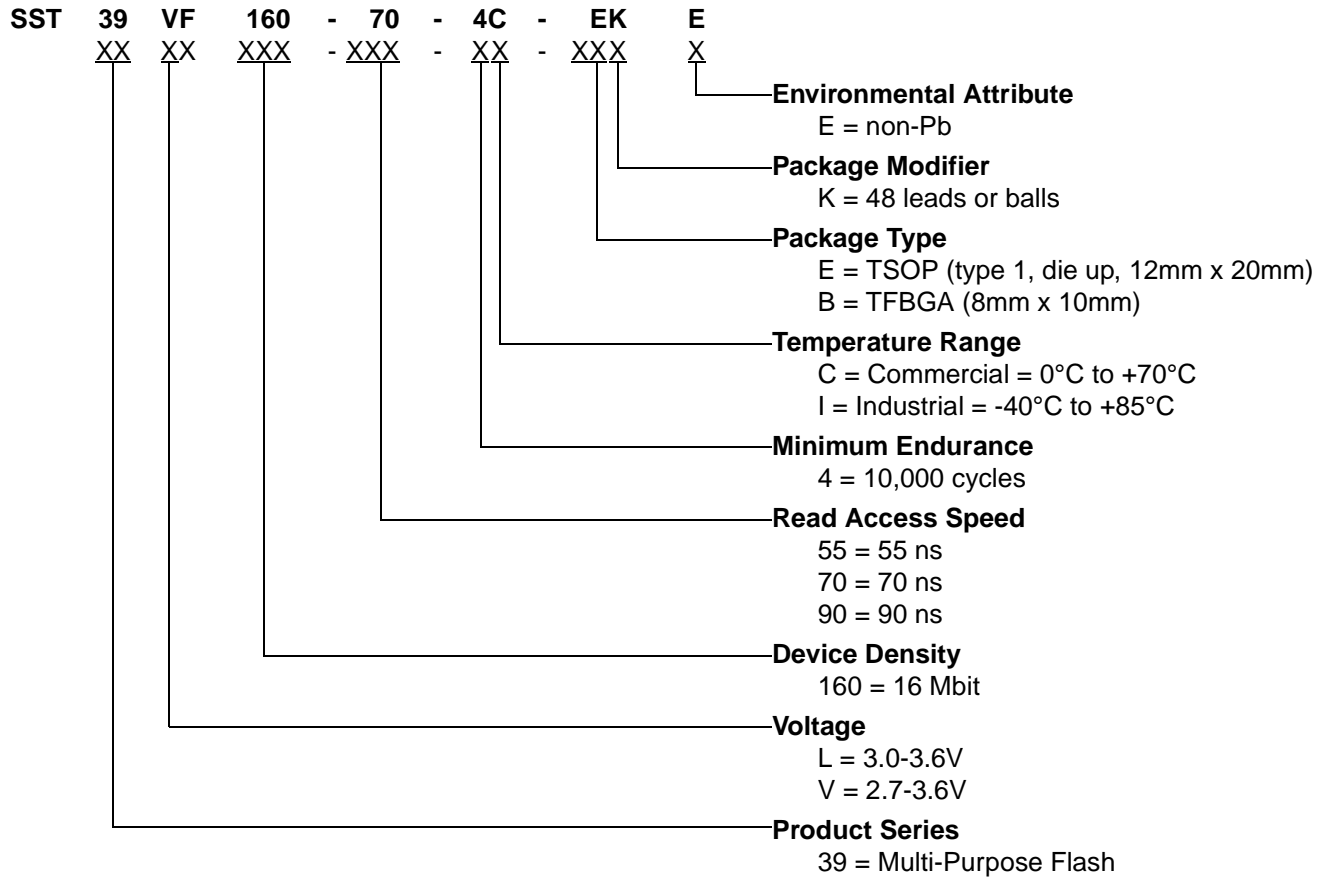


FIGURE 19: ERASE COMMAND SEQUENCE



PRODUCT ORDERING INFORMATION



Valid combinations for SST39LF160

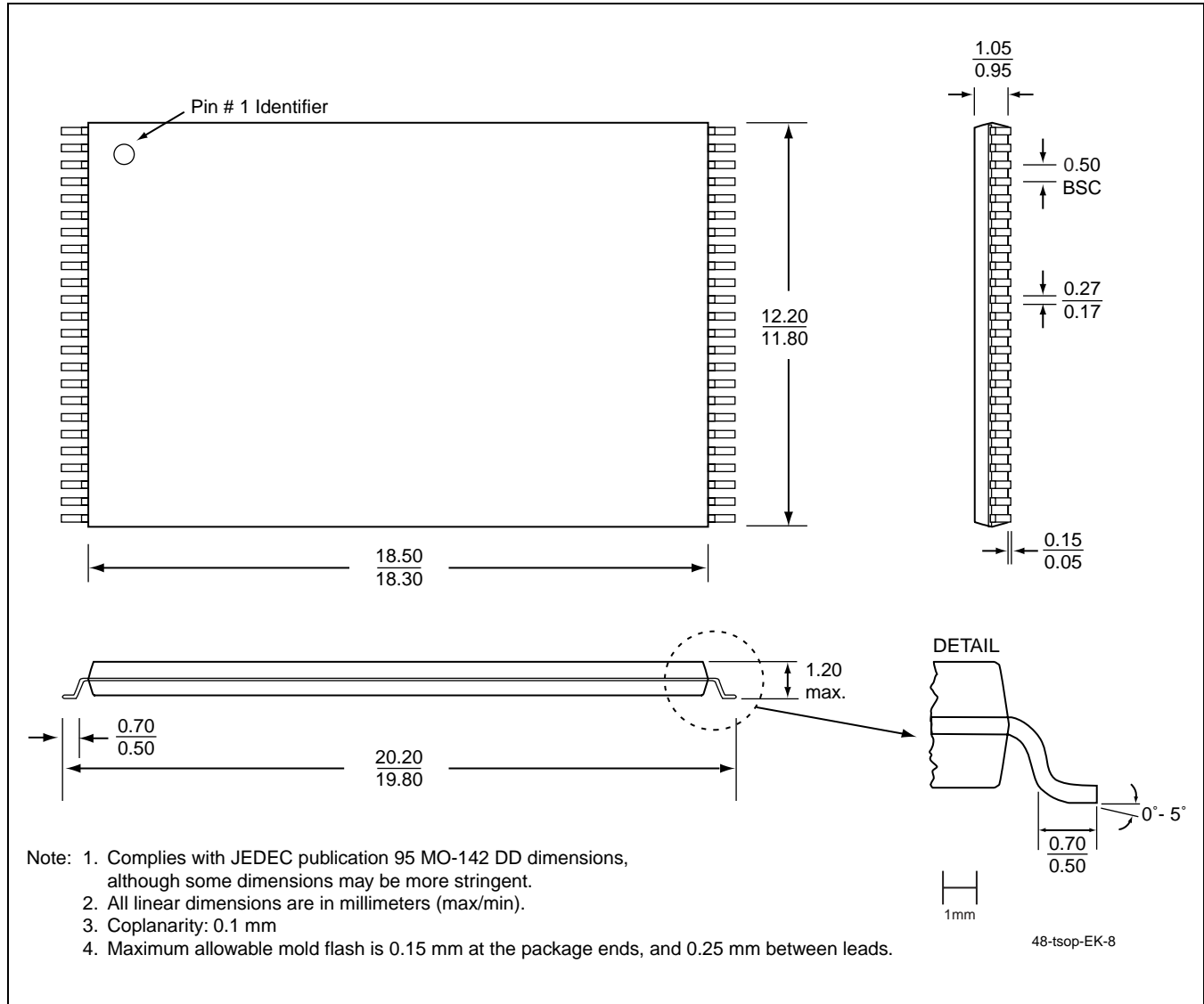
SST39LF160-55-4C-EK SST39LF160-55-4C-BK
 SST39LF160-55-4C-EKE

Valid combinations for SST39VF160

SST39VF160-70-4C-EK SST39VF160-70-4C-BK
 SST39VF160-70-4C-EKE
 SST39VF160-90-4C-EK SST39VF160-90-4C-BK
 SST39VF160-90-4C-EKE
 SST39VF160-70-4I-EK SST39VF160-70-4I-BK
 SST39VF160-70-4I-EKE
 SST39VF160-90-4I-EK SST39VF160-90-4I-BK
 SST39VF160-90-4I-EKE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

PACKAGING DIAGRAMS

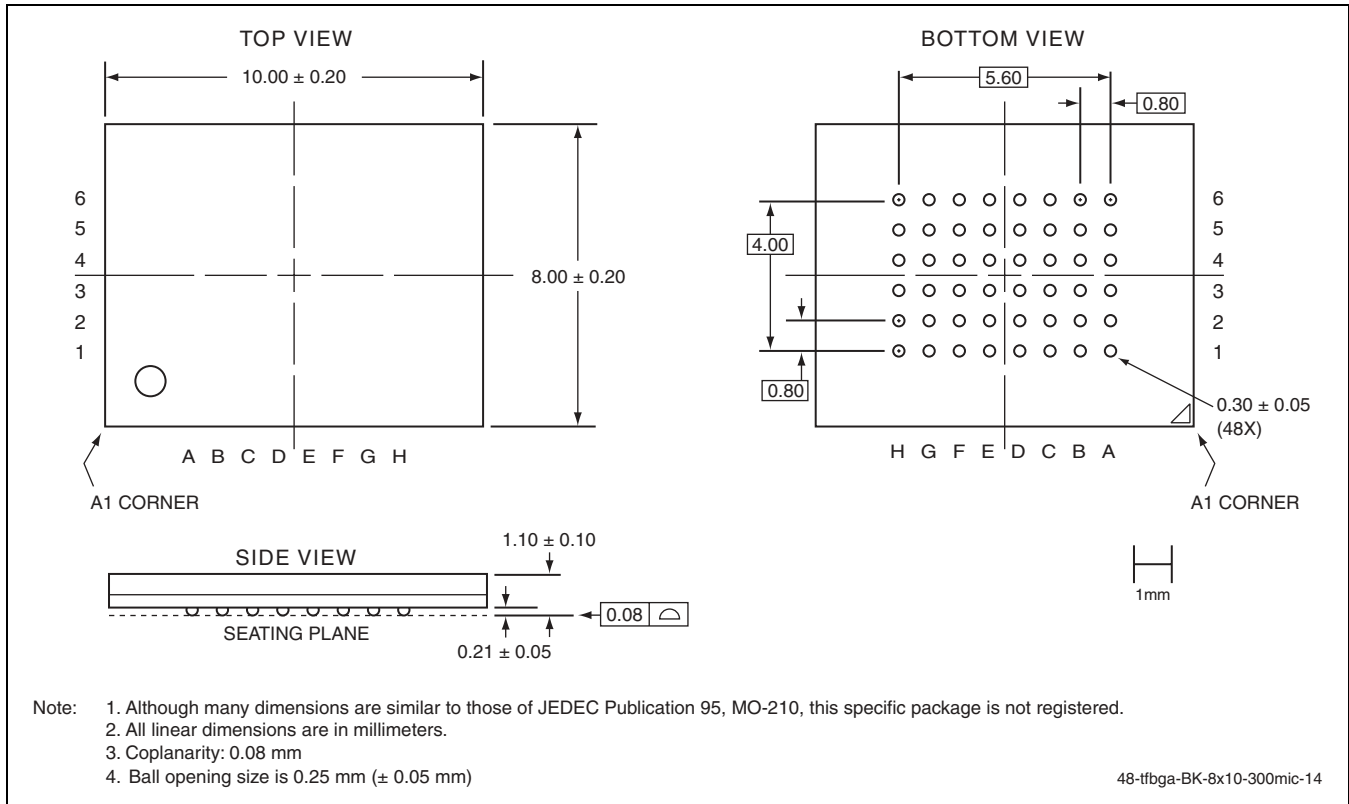


48-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 12MM X 20MM
SST PACKAGE CODE: EK



16 Mbit Multi-Purpose Flash SST39LF160 / SST39VF160

Data Sheet



**48-BALL THIN-PROFILE, FINE-PITCH BALL GRID ARRAY (TFBGA) 8MM X 10MM
SST PACKAGE CODE: BK**

TABLE 14: REVISION HISTORY

Number	Description	Date
02	<ul style="list-style-type: none"> 2002 Data Book 	May 2002
03	<ul style="list-style-type: none"> Removed B3K package Re-introduced BK package Changes to Table 8 on page 9 <ul style="list-style-type: none"> Added footnotes for MPF power usage and Typical conditions Clarified the Test Conditions for Power Supply Current and Read parameters Corrected I_{DD} Program and Erase Current parameter from 25 mA to 30 mA Corrected I_{ALP} Test Condition for CE# from V_{IHC} to V_{ILC} 	Mar 2003
04	<ul style="list-style-type: none"> 2004 Data Book Updated the BK package diagram Added non-Pb MPNs and removed footnote (See page 22) 	Nov 2003