Winbond Electronics Corp.

4M × 4 BANKS × 16 BIT DDR SDRAM

Table of Contents-

1. GENERAL DESCRIPTION

W942516CH is a CMOS Double Data Rate synchronous dynamic random access memory (DDR SDRAM), organized as 4,194,304 words × 4 banks × 16 bits. Using pipelined architecture and 0.13 μm process technology, W942516CH delivers a data bandwidth of up to 400M words per second (-5). To fully comply with the personal computer industrial standard, W942516CH is sorted into four speed grades: -5, -6, -7, -75 The -5 is compliant to the 200 MHz/CL2.5 & CL3 specification, The -6 is compliant to the 166 MHz/CL2.5 specification, the -7 is compliant to the 143 MHz/CL2.5 or DDR266/CL2 specification, the -75 is compliant to the DDR266/CL2.5 specification.

All Inputs reference to the positive edge of CLK (except for DQ, DM, and CKE). The timing reference point for the differential clock is when the CLK and $\overline{CLK}$ signals cross during a transition. And Write and Read data are synschronized with the both edges of DQS (Data Strobe).

By having a programmable Mode Register, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance. W942516CH is ideal for main memory in high performance applications.

2. FEATURES

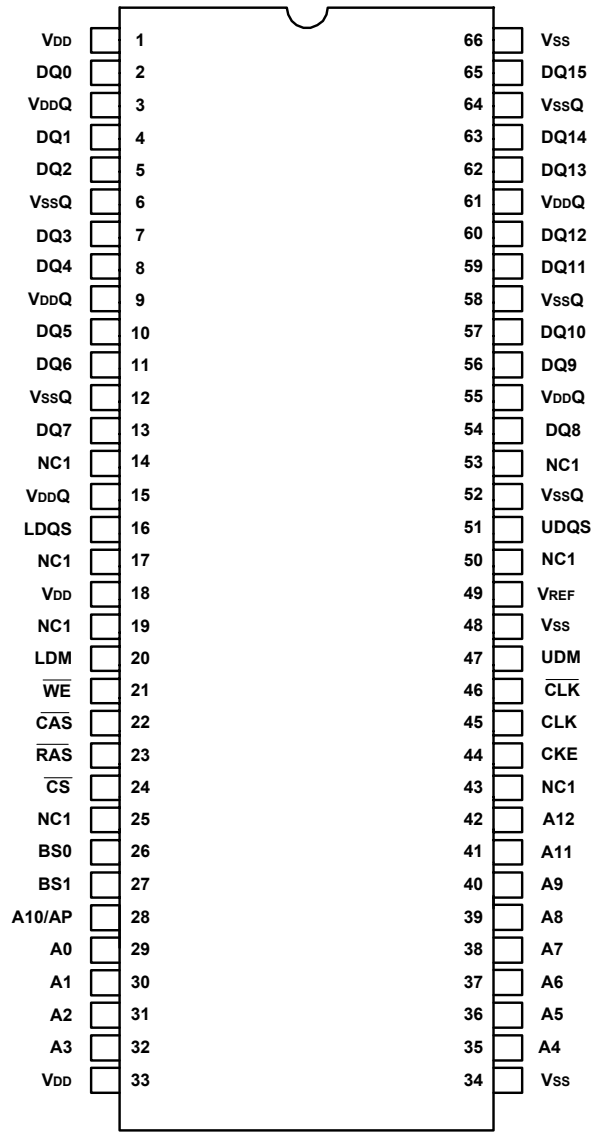
- 2.5V ±0.2V Power Supply for DDR266
- 2.5V ±0.2V Power Supply for DDR333
- 2.6V ±0.1V Power Supply for DDR400
- Up to 200 MHz Clock Frequency
- Double Data Rate architecture; two data transfers per clock cycle
- Differential clock inputs (CLK and $\overline{CLK}$)
- DQS is edge-aligned with data for Read; center-aligned with data for Write
- CAS Latency: 2, 2.5 and 3
- Burst Length: 2, 4 and 8
- Auto Refresh and Self Refresh
- Precharged Power Down and Active Power Down
- Write Data Mask
- Write Latency = 1
- 8K Refresh Cycles / 64 mS
- Interface: SSTL-2
- Packaged in TSOP II 66-pin, 400 x 875 mil, 0.65 mm pin pitch

3. KEY PARAMETERS

SYMBOL	DESCRIPTION		MIN./MAX.	-7	-75
t_{CK}	Clock Cycle Time	CL = 2	Min.	7.5 nS	8 nS
		CL = 2.5	Min.	7 nS	7.5 nS
t_{RAS}	Active to Precharge Command Period		Min.	45 nS	45 nS
t_{RC}	Active to Ref/Active Command Period		Min.	65 nS	65 nS
I_{DD1}	Operation Current (Single bank)		Max.	120 mA	120 mA
I_{DD4}	Burst Operation Current		Max.	165 mA	155 mA
I_{DD6}	Self-Refresh Current		Max.	3 mA	3 mA

SYMBOL	DESCRIPTION		MIN./MAX.	-5	-6
t_{CK}	Clock Cycle Time	CL = 2.5	Min.	5 nS	6 nS
		CL = 3	Min.	5 nS	6 nS
t_{RAS}	Active to Precharge Command Period		Min.	40 nS	42 nS
t_{RC}	Active to Ref/Active Command Period		Min.	55 nS	60 nS
I_{DD1}	Operation Current (Single bank)		Max.	120 mA	120 mA
I_{DD4}	Burst Operation Current		Max.	165 mA	165 mA
I_{DD6}	Self-Refresh Current		Max.	3 mA	3 mA

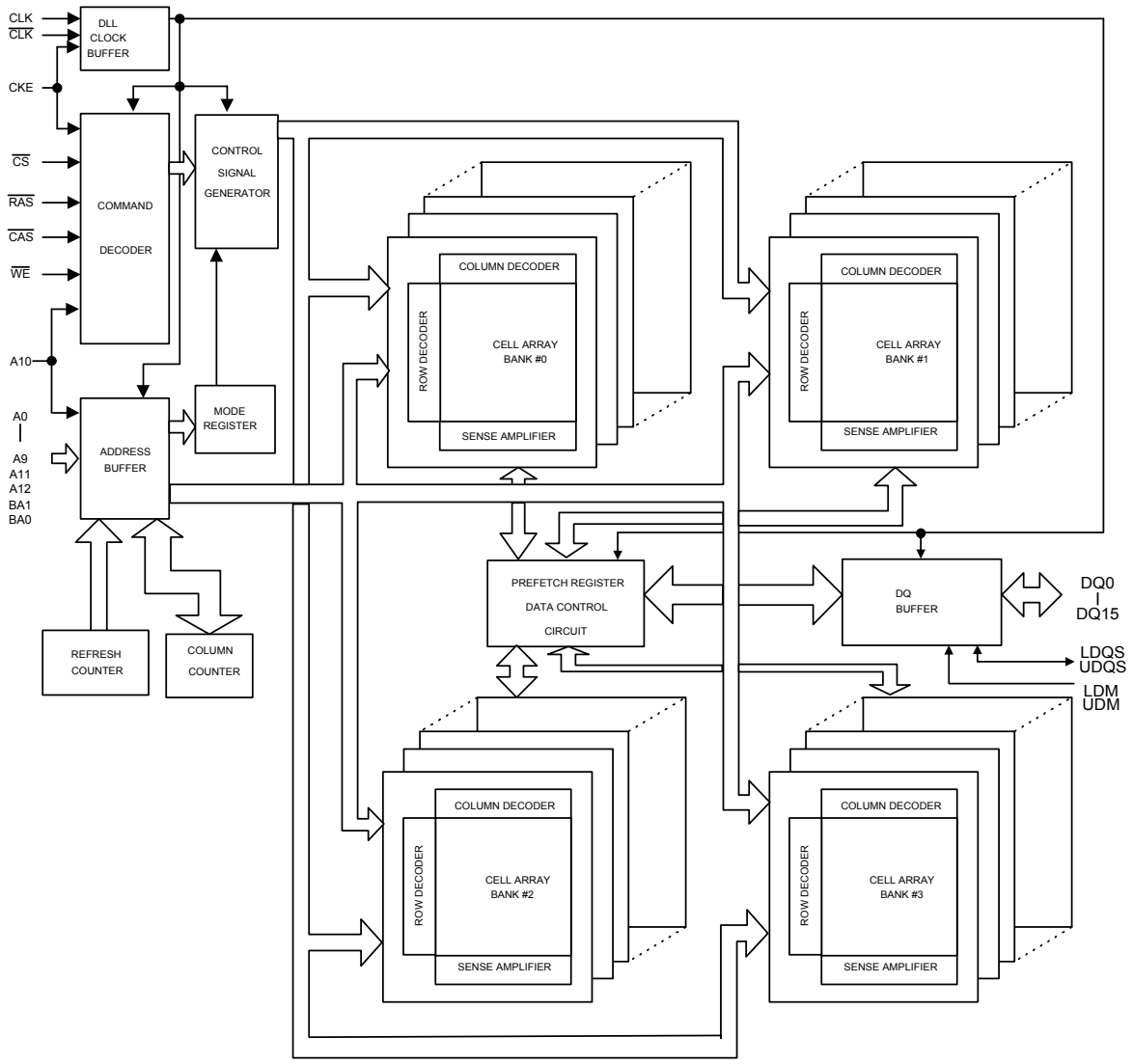
4. PIN CONFIGURATION



5. PIN DESCRIPTION

PIN NUMBER	PIN NAME	FUNCTION	DESCRIPTION
28 – 32, 35 – 42	A0 – A12	Address	Multiplexed pins for row and column address. Row address: A0 – A12. Column address: A0 – A8. (A10 is used for Auto Precharge)
26, 27	BS0, BS1	Bank Select	Select bank to activate during row address latch time, or bank to read/write during column address latch time.
2, 4, 5, 7, 8, 10, 11, 13, 54, 56, 57, 59, 60, 62, 63, 65	DQ0 – DQ15	Data Input/ Output	The DQ0 – DQ7 input and output data are synchronized with both edges of DQS.
16,51	LDQS, UDQS	Data Strobe	DQS is Bi-directional signal. DQS is input signal during write operation and output signal during read operation. It is Edge-aligned with read data, Center-aligned with write data.
24	$\overline{CS}$	Chip Select	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
23, 22, 21	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Command Inputs	Command inputs (along with $\overline{CS}$) define the command being entered.
20, 47	LDM, UDM	Write Mask	When DM is asserted “high” in burst write, the input data is masked. DM is synchronized with both edges of DQS.
45, 46	CLK, $\overline{CLK}$	Differential Clock Inputs	All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of $\overline{CLK}$.
44	CKE	Clock Enable	CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self Refresh mode is entered.
49	V_{REF}	Reference Voltage	V_{REF} is reference voltage for inputs.
1, 18, 33	V_{DD}	Power (+2.5V)	Power for logic circuit inside DDR SDRAM.
34, 48, 66	V_{SS}	Ground	Ground for logic circuit inside DDR SDRAM.
3, 9, 15, 55, 61	V_{DDQ}	Power (+2.5V) for I/O Buffer	Separated power from V_{DD}, used for output buffer, to improve noise.
6, 12, 52, 58, 64	V_{SSQ}	Ground for I/O Buffer	Separated ground from V_{SS}, used for output buffer, to improve noise.
14, 17, 19, 25, 43, 50, 53	NC1	No Connection	No connection

6. BLOCK DIAGRAM



NOTE:
The cell array configuration is 8912 * 512 * 16

7. ELECRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT
Input/Output Voltage	V_{IN}, V_{OUT}	-0.3 – V_{DDQ} +0.3	V
Power Supply Voltage	V_{DD}, V_{DDQ}	-0.3 – 3.6	V
Operating Temperature	T_{OPR}	0 – 70	°C
Storage Temperature	T_{STG}	-55 – 150	°C
Soldering Temperature (10s)	T_{SOLDER}	260	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OUT}	50	mA

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

7.2 Recommended DC Operating Conditions

(T_A = 0 to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	2.3	2.5	2.7	V	2
V_{DDQ}	Power Supply Voltage (for I/O Buffer)	2.3	2.5	V_{DD}	V	2
V_{REF}	Input reference Voltage	0.49 x V_{DDQ}	0.50 x V_{DDQ}	0.51 x V_{DDQ}	V	2, 3
V_{TT}	Termination Voltage (System)	V_{REF} - 0.04	VREF	V_{REF} + 0.04	V	2, 8
V_{IH} (DC)	Input High Voltage (DC)	V_{REF} + 0.15	-	V_{DDQ} + 0.3	V	2
V_{IL} (DC)	Input Low Voltage (DC)	-0.3	-	V_{REF} - 0.15	V	2
V_{ICK} (DC)	Differential Clock DC Input Voltage	-0.3	-	V_{DDQ} + 0.3	V	15
V_{ID} (DC)	Input Differential Voltage. CLK and $\overline{CLK}$ inputs (DC)	0.36	-	V_{DDQ} + 0.6	V	13, 15
V_{IH} (AC)	Input High Voltage (AC)	V_{REF} + 0.31	-	-	V	2
V_{IL} (AC)	Input Low Voltage (AC)	-	-	V_{REF} - 0.31	V	2
V_{ID} (AC)	Input Differential Voltage. CLK and $\overline{CLK}$ inputs (AC)	0.7	-	V_{DDQ} + 0.6	V	13, 15
V_X (AC)	Differential AC input Cross Point Voltage	V_{DDQ}/2 - 0.2	-	V_{DDQ}/2 + 0.2	V	12, 15
V_{ISO} (AC)	Differential Clock AC Middle Point	V_{DDQ}/2 - 0.2	-	V_{DDQ}/2 + 0.2	V	14, 15

Notes: Undershoot Limit: V_{IL} (min) = -0.9V with a pulse width $\leq$ 5 nS

Overshoot Limit: V_{IH} (max) = V_{DD}Q +0.9V with a pulse width $\leq$ 5 nS

V_{IH} (DC) and V_{IL} (DC) are levels to maintain the current logic state.

V_{IH} (AC) and V_{IL} (AC) are levels to change to the new logic state.

7.3 Capacitance

(V_{DD} = V_{DDQ} = 2.5V ±0.2V, f = 1 MHz, T_A = 25 °C, $V_{OUT\ (DC)}$ = V_{DDQ}/2, V_{OUT} (Peak to Peak) = 0.2V)

SYMBOL	PARAMETER	MIN.	MAX.	DELTA (MAX.)	UNIT
C_{IN}	Input Capacitance (except for CLK pins)	2.0	3.0	0.5	pF
C_{CLK}	Input Capacitance (CLK pins)	2.0	3.0	0.25	pF
$C_{I/O}$	DQ, DQS, DM Capacitance	4.0	5.0	0.5	pF
C_{NC1}	NC1 Pin Capacitance	-	1.5	-	pF
C_{NC2}	NC2 Pin Capacitance	4.0	5.0	-	pF

Notes: These parameters are periodically sampled and not 100% tested.

The NC2 pins have additional capacitance for adjustment of the adjacent pin capacitance.

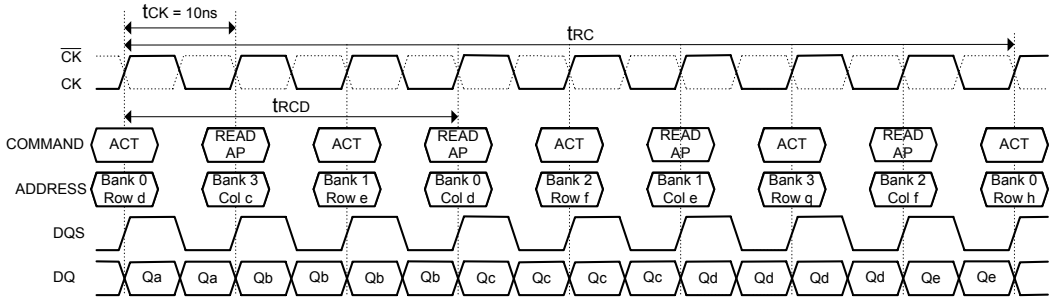
The NC2 pins have Power and Ground clamp.

7.4 Leakage and Output Buffer Characteristics

SYMBOL	PARAMETER		MIN.	MAX.	UNITS	NOTES
$I_{I\ (L)}$	Input Leakage Current (0V ≤ V_{IN} ≤ V_{DDQ}, All other pins not under test = 0V)		-2	2	µA	
$I_{O\ (L)}$	Output Leakage Current (Output disabled, 0V ≤ V_{OUT} ≤ V_{DDQ})		-5	5	µA	
V_{OH}	Output High Voltage (under AC test load condition)	Full Strength	V_{TT} +0.76	-	V	
V_{OL}	Output Low Voltage (under AC test load condition)		-	V_{TT} -0.76	V	
$I_{OH\ (DC)}$	Output Minimum Source DC Current		-15.2	-	mA	4, 6
$I_{OL\ (DC)}$	Output Minimum Sink DC Current		15.2	-	mA	4, 6
$I_{OH\ (DC)}$	Output Minimum Source DC Current	Half Strength	-10.4	-	mA	5
$I_{OL\ (DC)}$	Output Minimum Sink DC Current		10.4	-	mA	5

7.5 DC Characteristics

SYM.	PARAMETER	MAX.				UNIT	NOTES
		-5	-6	-7	-75		
I_{DD0}	OPERATING CURRENT: One Bank Active-Precharge; t_{RC} = t_{RC} min; t_{CK} = t_{CK} min; DQ, DM and DQS inputs changing twice per clock cycle; Address and control inputs changing once per clock cycle	110	110	110	110		7
I_{DD1}	OPERATING CURRENT: One Bank Active-Read-Precharge; Burst = 2; t_{RC} = t_{RC} min; CL = 2.5; t_{CK} = t_{CK} min; I_{OUT} = 0 mA; Address and control inputs changing once per clock cycle.	120	120	120	120		7, 9
I_{DD2P}	PRECHARGE-POWER-DOWN STANDBY CURRENT: All Banks Idle; Power down mode; CKE ≤ V_{IL} max; t_{CK} = t_{CK} min; Vin = V_{REF} for DQ, DQS and DM	2	2	2	2		
I_{DD2F}	IDLE FLOATING STANDBY CURRENT: $\overline{CS}$ ≥ V_{IH} min; All Banks Idle; CKE ≥ V_{IH} min; Address and other control inputs changing once per clock cycle; Vin = Vref for DQ, DQS and DM	45	45	45	40		7
I_{DD2N}	IDLE STANDBY CURRENT: $\overline{CS}$ ≥ V_{IH} min; All Banks Idle; CKE ≥ V_{IH} min; t_{CK} = t_{CK} min; Address and other control inputs changing once per clock cycle; Vin ≥ V_{IH} min or Vin ≤ V_{IL} max for DQ, DQS and DM	45	45	45	40		7
I_{DD2Q}	IDLE QUIET STANDBY CURRENT: $\overline{CS}$ ≥ V_{IH} min; All Banks Idle; CKE ≥ V_{IH} min; t_{CK} = t_{CK} min; Address and other control inputs stable; Vin ≥ V_{REF} for DQ, DQS and DM	40	40	40	35	mA	7
I_{DD3P}	ACTIVE POWER-DOWN STANDBY CURRENT: One Bank Active; Power down mode; CKE ≤ V_{IL} max; t_{CK} = t_{CK} min	20	20	20	20		
I_{DD3N}	ACTIVE STANDBY CURRENT: $\overline{CS}$ ≥ V_{IH} min; CKE ≥ V_{IH} min; One Bank Active-Precharge; t_{RC} = t_{RAS} max; t_{CK} = t_{CK} min; DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	70	70	70	65		7
I_{DD4R}	OPERATING CURRENT: Burst = 2; Reads; Continuous burst; One Bank Active; Address and control inputs changing once per clock cycle; CL=2.5; t_{CK} = t_{CK} min; I_{OUT} = 0mA	165	165	165	155		7, 9
I_{DD4W}	OPERATING CURRENT: Burst = 2; Write; Continuous burst; One Bank Active; Address and control inputs changing once per clock cycle; CL = 2.5; t_{CK} = t_{CK} min; DQ, DM and DQS inputs changing twice per clock cycle	165	165	165	155		7
I_{DD5}	AUTO REFRESH CURRENT: t_{RC} = t_{RFC} min	190	190	190	190		7
I_{DD6}	SELF REFRESH CURRENT: CKE ≤ 0.2V	3	3	3	3		
I_{DD7}	RANDOM READ CURRENT: 4 Banks Active Read with activate every 20ns, Auto-Precharge Read every 20 nS; Burst = 4; t_{RCD} = 3; I_{OUT} = 0mA; DQ, DM and DQS inputs changing twice per clock cycle; Address changing once per clock cycle	270	270	270	270		



RANDOM READ CURRENT Timing (I_{DD7})

7.6 AC Characteristics and Operating Condition

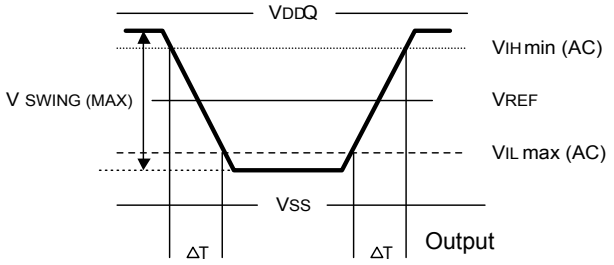
(Notes: 10, 12)

SYMBOL	PARAMETER		-7		-75		UNITS	NOTES
			MIN.	MAX.	MIN.	MAX.		
t_{RC}	Active to Ref/Active Command Period		65		65		nS	
t_{RFC}	Ref to Ref/Active Command Period		75		75			
t_{RAS}	Active to Precharge Command Period		45	100000	45	100000		
t_{RCD}	Active to Read/Write Command Delay Time		20		20			
t_{RAP}	Active to Read with Auto Precharge Enable		15		15			
t_{CCD}	Read/Write(a) to Read/Write(b) Command Period		1		1		t_{CK}	
t_{RP}	Precharge to Active Command Period		20		20		nS	
t_{RRD}	Active(a) to Active(b) Command Period		15		15			
t_{WR}	Write Recovery Time		15		15			
t_{DAL}	Auto Precharge Write Recovery + Precharge Time		30		30			
t_{CK}	CLK Cycle Time	CL = 2	7.5	15	8	15		
		CL = 2.5	7	15	7.5	15		
t_{AC}	Data Access Time from CLK, $\overline{CLK}$		-0.75	0.75	-0.75	0.75		16
t_{DQSCK}	DQS Output Access Time from CLK, $\overline{CLK}$		-0.75	0.75	-0.75	0.75		
t_{DQSQ}	Data Strobe Edge to Output Data Edge Skew			0.5		0.5		
t_{CH}	CLk High Level Width		0.45	0.55	0.45	0.55	t_{CK}	11
t_{CL}	CLK Low Level Width		0.45	0.55	0.45	0.55		
t_{HP}	CLK Half Period (minimum of actual t_{CH}, t_{CL})		Min. (t_{CL},t_{CH})		Min. (t_{CL},t_{CH})		nS	
t_{QH}	DQ Output Data Hold Time from DQS		T_{HP} -0.75		T_{HP} -0.75			
t_{RPRE}	DQS Read Preamble Time		0.9	1.1	0.9	1.1	t_{CK}	11
t_{RPST}	DQS Read Postamble Time		0.4	0.6	0.4	0.6		
t_{DS}	DQ and DM Setup Time		0.5		0.5		nS	
t_{DH}	DQ and DM Hold Time		0.5		0.5			
t_{DIPW}	DQ and DM Input Pulse Width (for each input)		1.75		1.75			
t_{DQSH}	DQS Input High Pulse Width		0.35		0.35		t_{CK}	11
t_{DQSL}	DQS Input Low Pulse Width		0.35		0.35			
t_{DSS}	DQS Falling Edge to CLK Setup Time		0.2		0.2			
t_{DSH}	DQS Falling Edge Hold Time from CLK		0.2		0.2			
t_{WPRES}	Clock to DQS Write Preamble Set-up Time		0		0		nS	
t_{WPRE}	DQS Write Preamble Time		0.25		0.25		t_{CK}	11
t_{WPST}	DQS Write Postamble Time		0.4		0.4			
t_{DQSS}	Write Command to First DQS Latching Transition		0.75	1.25	0.75	1.25		
t_{DSSK}	UDQS – LDQS Skew (x 16)		-0.25	0.25	-0.25	0.25		
t_{IS}	Input Setup Time		0.9		0.9		nS	
t_{IH}	Input Hold Time		0.9		0.9			
t_{IPW}	Control & Address Input Pulse Width (for each input)		2.2		2.2			
t_{HZ}	Data-out High-impedance Time from CLK, $\overline{CLK}$		-0.75	0.75	-0.75	0.75		
t_{LZ}	Data-out Low-impedance Time from CLK, $\overline{CLK}$		-0.75	0.75	-0.75	0.75		
$t_{T(SS)}$	SSTL Input Transition		0.5	1.5	0.5	1.5		
t_{WTR}	Internal Write to Read Command Delay		1		1		t_{CK}	
t_{XSNR}	Exit Self Refresh to non-Read Command		75		75		ns	
t_{XSRD}	Exit Self Refresh to Read Command		10		10		t_{CK}	
t_{REF}	Refresh Time (8k)			64		64	mS	
t_{MRD}	Mode Register Set Cycle Time		15		15		nS	

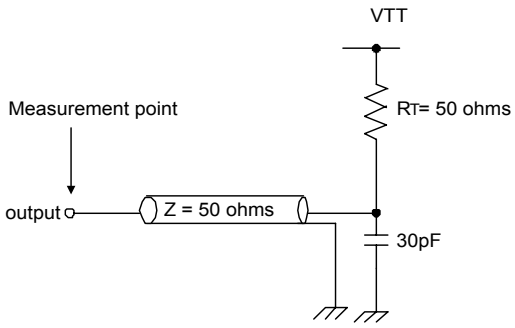
SYM.	PARAMETER		-5		-6		UNITS	NOTES
			MIN.	MAX.	MIN.	MAX.		
tRC	Active to Ref/Active Command Period		55		60		nS	
tRFC	Ref to Ref/Active Command Period		70		72			
tRAS	Active to Precharge Command Period		40	70000	42	100000		
tRCD	Active to Read/Write Command Delay Time		15		18			
tRAP	Active to Read with Auto Precharge Enable		15		15			
tCCD	Read/Write(a) to Read/Write(b) Command Period		1		1		tCK	
tRP	Precharge to Active Command Period		15		18		nS	
tRRD	Active(a) to Active(b) Command Period		10		12			
tWR	Write Recovery Time		15		15			
tDAL	Auto Precharge Write Recovery + Precharge Time		30		30			
tCK	CLK Cycle Time	2.5	5	10	6	12		
		3	5	10	6	12		
tAC	Data Access Time from CLK, $\overline{CLK}$		-0.7	0.7	-0.7	0.7		16
tDQSCK	DQS Output Access Time from CLK, $\overline{CLK}$		-0.55	0.55	-0.6	0.6		
tDQSQ	Data Strobe Edge to Output Data Edge Skew			0.4		0.45		
tCH	CLk High Level Width		0.45	0.55	0.45	0.55	tCK	11
tCL	CLK Low Level Width		0.45	0.55	0.45	0.55		
tHP	CLK Half Period (minimum of actual tCH, tCL)		Min. (tCL,tCH)		Min. (tCL,tCH)		nS	
tQH	DQ Output Data Hold Time from DQS		tHP -0.5		tHP -0.55			
tRPRE	DQS Read Preamble Time		0.9	1.1	0.9	1.1	tCK	11
tRPST	DQS Read Postamble Time		0.4	0.6	0.4	0.6		
tDS	DQ and DM Setup Time		0.4		0.45		nS	
tDH	DQ and DM Hold Time		0.4		0.45			
tDIPW	DQ and DM Input Pulse Width (for each input)		1.75		1.75			
tDQSH	DQS Input High Pulse Width		0.35		0.35		tCK	11
tDQSL	DQS Input Low Pulse Width		0.35		0.35			
tDSS	DQS Falling Edge to CLK Setup Time		0.2		0.2			
tDSH	DQS Falling Edge Hold Time from CLK		0.2		0.2			
tWPRES	Clock to DQS Write Preamble Set-up Time		0		0		nS	
tWPRE	DQS Write Preamble Time		0.25		0.25		tCK	11
tWPST	DQS Write Postamble Time		0.4	0.6	0.4	0.6		
tDQSS	Write Command to First DQS Latching Transition		0.72	1.28	0.75	1.25		
tDSSK	UDQS – LDQS Skew (x 16)		-0.25	0.25	-0.25	0.25		
tIS	Input Setup Time		0.6		0.75		nS	
tIH	Input Hold Time		0.6		0.75			
tIPW	Control & Address Input Pulse Width (for each input)		2.2		2.2			
tHZ	Data-out High-impedance Time from CLK, $\overline{CLK}$			Max tAC	-0.7	0.7		
tLZ	Data-out Low-impedance Time from CLK, $\overline{CLK}$		-0.7	0.7	-0.7	0.7		
tT(SS)	SSTL Input Transition		0.5	1.5	0.5	1.5		
tWTR	Internal Write to Read Command Delay		2		2		tCK	
tXSNR	Exit Self Refresh to non-Read Command		75		75		ns	
tXSRD	Exit Self Refresh to Read Command		10		10		tCK	
tREF	Refresh Time (8k)			64		64	mS	
tMRD	Mode Register Set Cycle Time		10		12		nS	

7.7 AC Test Conditions

PARAMETER	SYMBOL	VALUE	UNIT
Input High Voltage (AC)	V_{IH}	V_{REF} +0.31	V
Input Low Voltage (AC)	V_{IL}	V_{REF} -0.31	V
Input Reference Voltage	V_{REF}	0.5 x V_{DDQ}	V
Termination Voltage	V_{TT}	0.5 x V_{DDQ}	V
Input Signal Peak to Peak Swing	V_{SWING}	1.0	V
Differential Clock Input Reference Voltage	V_R	V_x (AC)	V
Input Difference Voltage. CLK and $\overline{CLK}$ Inputs (AC)	V_{ID} (AC)	1.5	V
Input Signal Minimum Slew Rate	SLEW	1.0	V/nS
Output Timing Measurement Reference Voltage	V_{OTR}	0.5 x V_{DDQ}	V



SLEW = (V_{IH} min (AC) - V_{IL}max (AC)) /ΔT



A.C. TEST LOAD (A)

Notes:

(1) Conditions outside the limits listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device.

(2) All voltages are referenced to V_{SS}, V_{SSQ}. .(2.6V±0.1V for DDR400)

(3) Peak to peak AC noise on V_{REF} may not exceed ±2% $V_{REF(DC)}$.

(4) V_{OH} = 1.95V, V_{OL} = 0.35V

(5) V_{OH} = 1.9V, V_{OL} = 0.4V

(6) The values of $I_{OH(DC)}$ is based on V_{DDQ} = 2.3V and V_{TT} = 1.19V.
The values of $I_{OL(DC)}$ is based on V_{DDQ} = 2.3V and V_{TT} = 1.11V.

(7) These parameters depend on the cycle rate and these values are measured at a cycle rate with the minimum values of t_{CK} and t_{RC}.

(8) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

(9) These parameters depend on the output loading. Specified values are obtained with the output open.

(10) Transition times are measured between $V_{IH\ min(AC)}$ and $V_{IL\ max(AC)}$.Transition (rise and fall) of input signals have a fixed slope.

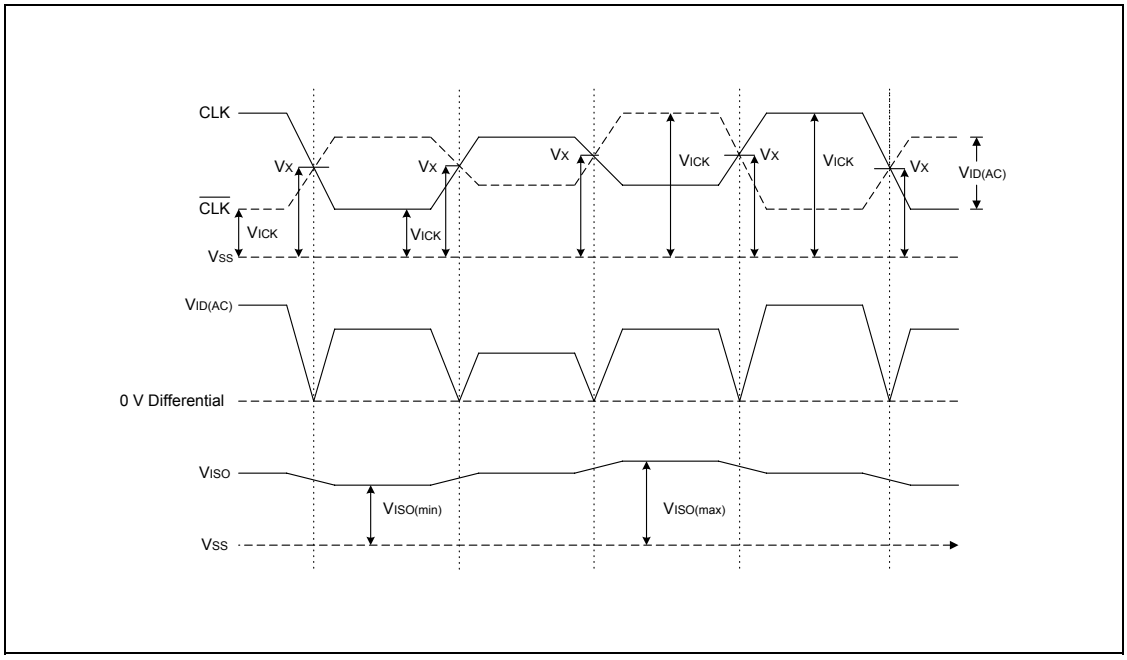
(11) IF the result of nominal calculation with regard to t_{CK} contains more than one decimal place, the result is rounded up to the nearest decimal place.
(i.e., T_{DQSS} = 0.75 × t_{CK}, t_{CK} = 7.5 nS, 0.75 × 7.5 nS = 5.625 nS is rounded up to 5.6 nS.)

(12) V_X is the differential clock cross point voltage where input timing measurement is referenced.

(13) V_{ID} is magnitude of the difference between CLK input level and $\overline{CLK}$ input level.

(14) V_{ISO} means {V_{ICK}(CLK)+V_{ICK}($\overline{CLK}$)}/2.

(15) Refer to the figure below.



(16) t_{AC} and t_{DQSCK} depend on the clock jitter. These timing are measured at stable clock.

8. OPERATION MODE

The following table shows the operation commands.

8.1 Simplified Truth Table

SYM.	COMMAND	DEVICE STATE	CKEN-1	CKEN	DM(4)	BS0, BS1	A10	A12, A11, A9-A0	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
ACT	Bank Active	Idle(3)	H	X	X	V	V	V	L	L	H	H
PRE	Bank Precharge	Any(3)	H	X	X	V	L	X	L	L	H	L
PREA	Precharge All	Any	H	X	X	X	H	X	L	L	H	L
WRIT	Write	Active(3)	H	X	X	V	L	V	L	H	L	L
WRITA	Write with Auto Precharge	Active(3)	H	X	X	V	H	V	L	H	L	L
READ	Read	Active(3)	H	X	X	V	L	V	L	H	L	H
READA	Read with Auto Precharge	Active(3)	H	X	X	V	H	V	L	H	L	H
MRS	Mode Register Set	Idle	H	X	X	L, L	C	C	L	L	L	L
EMRS	Extended Mode Regiser Set	Idle	H	X	X	H, L	V	V	L	L	L	L
NOP	No Operation	Any	H	X	X	X	X	X	L	H	H	H
BST	Burst Read Stop	Active	H	X	X	X	X	X	L	H	H	L
DSL	Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
AREF	Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
SELF	Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
SELEX	Self Refresh Exit	Idle (Self Refresh)	L	H	X	X	X	X	H	X	X	X
									L	H	H	X
PD	Power Down Dode Entry	Idle/ Active(5)	H	L	X	X	X	X	H	X	X	X
									L	H	H	X
PDEX	Power Down Mode Exit	Any (Power Down)	L	H	X	X	X	X	H	X	X	X
									L	H	H	X
WDE	Data Write Enable	Active	H	X	L	X	X	X	X	X	X	X
WDD	Data Write Disable	Active	H	X	H	X	X	X	X	X	X	X

Notes:

1. V = Valid X = Don't Care L = Low level H = High level
2. CKE_n signal is input level when commands are issued.
   CKE_{n-1} signal is input level one clock cycle before the commands are issued.
4. These are state designated by the BS0, BS1 signals.
5. LDM, UDM (W942516CH)
6. Power Down Mode can not entry in the burst cycle.

8.2 Function Truth Table

(Note 1)

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESS	COMMAND	ACTION	NOTES
Idle	H	X	X	X	X	DSL	Nop	
	L	H	H	X	X	NOP/BST	Nop	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	Row activating	
	L	L	H	L	BS, A10	PRE/PREA	Nop	
	L	L	L	H	X	AREF/SELF	Refresh or Self refresh	2
	L	L	L	L	Op-Code	MRS/EMRS	Mode register accessing	2
Row Active	H	X	X	X	X	DSL	Nop	
	L	H	H	X	X	NOP/BST	Nop	
	L	H	L	H	BS, CA, A10	READ/READA	Begin read: Determine AP	4
	L	H	L	L	BS, CA, A10	WRIT/WRITA	Begin write: Determine AP	4
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	Precharge	5
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Read	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	Burst stop	
	L	H	L	H	BS, CA, A10	READ/READA	Term burst, new read: Determine AP	6
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	Term burst, precharging	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	Term burst, start read: Determine AP	6, 7
	L	H	L	L	BS, CA, A10	WRIT/WRITA	Term burst, start read: Determine AP	6
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	Term burst. precharging	8
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

Function Truth Table, continued

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESS	COMMAND	ACTION	NOTES
Read with Auto Prechange	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	ILLEGAL	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Precharging	H	X	X	X	X	DSL	Nop-> Idle after t_{RP}	
	L	H	H	H	X	NOP	Nop-> Idle after t_{RP}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	Idle after t_{RP}	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Row Activating	H	X	X	X	X	DSL	Nop-> Row active after t_{RCD}	
	L	H	H	H	X	NOP	Nop-> Row active after t_{RCD}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

Function Truth Table, continued

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESS	COMMAND	ACTION	NOTES
Write Recovering	H	X	X	X	X	DSL	Nop->Row active after t_{WR}	
	L	H	H	H	X	NOP	Nop->Row active after t_{WR}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write Recovering with Auto Precharge	H	X	X	X	X	DSL	Nop->Enter precharge after t_{WR}	
	L	H	H	H	X	NOP	Nop->Enter precharge after t_{WR}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BS, CA, A10	READ/READA	ILLEGAL	3
	L	H	L	L	BS, CA, A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BS, RA	ACT	ILLEGAL	3
	L	L	H	L	BS, A10	PRE/PREA	ILLEGAL	3
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Refreshing	H	X	X	X	X	DSL	Nop->Idle after t_{RC}	
	L	H	H	H	X	NOP	Nop->Idle after t_{RC}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	X	READ/WRIT	ILLEGAL	
	L	L	H	X	X	ACT/PRE/PREA	ILLEGAL	
	L	L	L	X	X	AREF/SELF/MRS/EMRS	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	DSL	Nop->Row after t_{MRD}	
	L	H	H	H	X	NOP	Nop->Row after t_{MRD}	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	X	X	READ/WRIT	ILLEGAL	
	L	L	X	X	X	ACT/PRE/PREA/AREF/SELF/MRS/EMRS	ILLEGAL	

Notes:
1. All entries assume that CKE was active (High level) during the preceding clock cycle and the current clock cycle.
2. Illegal if any bank is not idle.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BS), depending on the state of that bank.
4. Illegal if t_{RCD} is not satisfied.
5. Illegal if t_{RAS} is not satisfied.
6. Must satisfy burst interrupt condition.
7. Must avoid bus contention, bus turn around, and/or satisfy write recovery requirements.
8. Must mask preceding data which don't satisfy t_{WR}

Remark: H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data

8.3 Function Truth Table for CKE

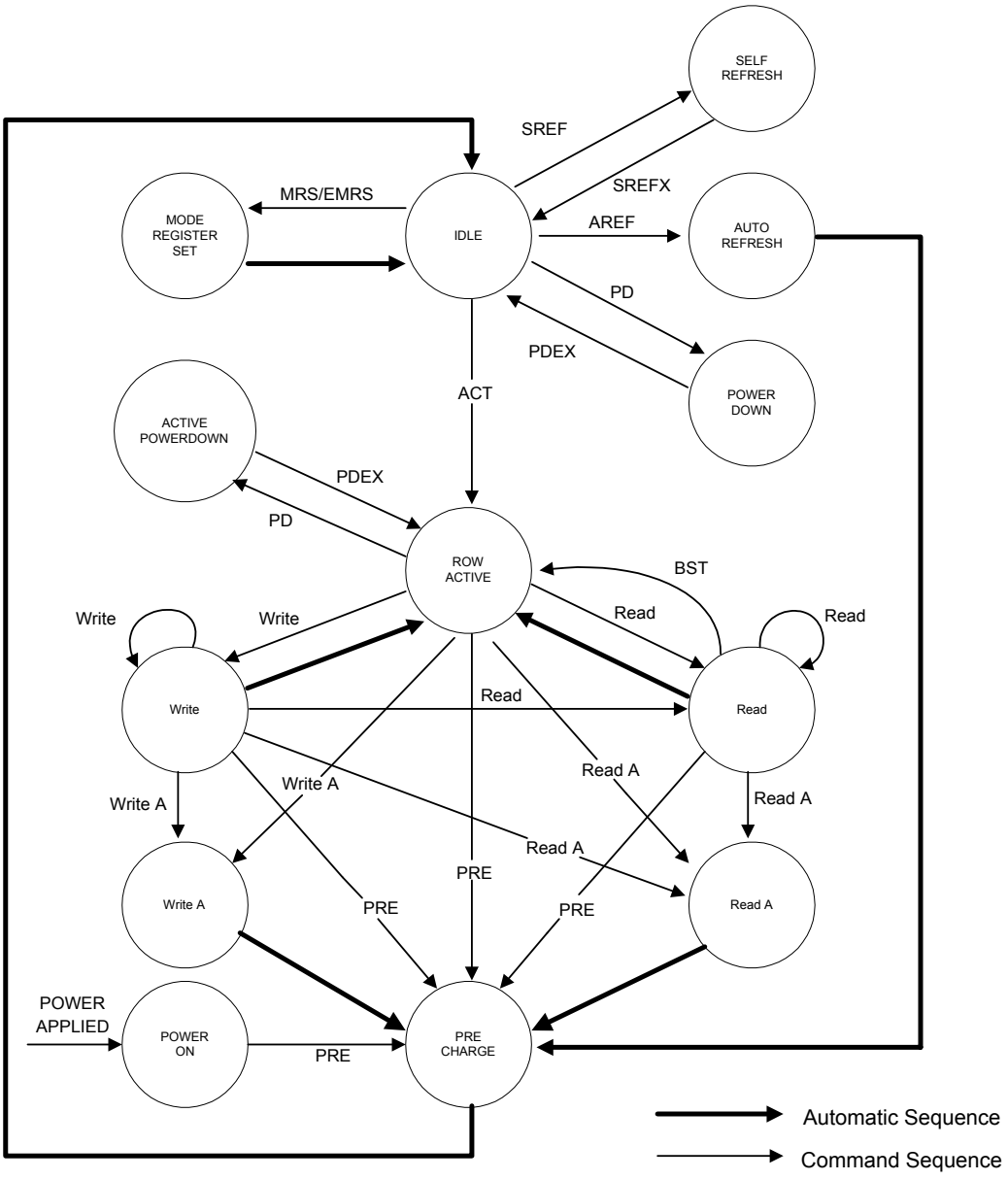
CURRENT STATE	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESS	ACTION	NOTES
	n-1	n							
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh->Idle after t_{XSNR}	
	L	H	L	H	H	X	X	Exit Self Refresh->Idle after t_{XSNR}	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	Maintain Self Refresh	
Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	X	X	X	X	X	Exit Power down->Idle after t_{IS}	
	L	L	X	X	X	X	X	Maintain power down mode	
All banks Idle	H	H	X	X	X	X	X	Refer to Function Truth Table	
	H	L	H	X	X	X	X	Enter Power down	2
	H	L	L	H	H	X	X	Enter Power down	2
	H	L	L	L	L	H	X	Self Refresh	1
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	X	X	X	X	X	X	Power down	2
Row Active	H	H	X	X	X	X	X	Refer to Function Truth Table	
	H	L	H	X	X	X	X	Enter Power down	2
	H	L	L	H	H	X	X	Enter Power down	2
	H	L	L	L	L	H	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	X	X	X	X	X	X	Power down	
Any State Other Than Listed Above	H	H	X	X	X	X	X	Refer to Function Truth Table	

Notes:

1. Self refresh can enter only from the all banks idle state.
2. Power down can enter only from bank idle or row active state.

Remark: H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data

8.4 Simplified Stated Diagram



9. FUNCTIONAL DESCRIPTION

9.1 Power Up Sequence

(1) Apply power and attempt to CKE at a low state ($\leq$0.2V), all other inputs may be undefined
   1) Apply V_{DD} before or at the same time as V_{DDQ}.
   2) Apply V_{DDQ} before or at the same time as V_{TT} and V_{REF}.

(2) Start Clock and maintain stable condition for 200 μS (min.).

(3) After stable power and clock, apply NOP and take CKE high.

(4) Issue EMRS (Extended Mode Register Set) to enable DLL and establish Output Driver Type.

(5) Issue MRS (Mode Register Set) to reset DLL and set device to idle with bit A8.
(an additional 200 cycles(min) of clock are required for DLL Lock)

(6) Issue precharge command for all banks of the device.

(7) Issue two or more Auto Refresh commands.

(8) Issue MRS-Initialize device operation.
(If device operation mode is set at sequence 5, sequence 8 can be skipped.)

9.2 Command Function

1. Bank Activate Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "H", $\overline{WE}$ = "H", BS0, BS1 = Bank, A0 to A12 = Row Address)

The Bank Activate command activates the bank designated by the BS (Bank address) signal. Row addresses are latched on A0 to A12 when this command is issued and the cell data is read out of the sense amplifiers. The maximum time that each bank can be held in the active state is specified as $t_{RAS\ (max)}$. After this command is issued, Read or Write operation can be executed.

2. Bank Precharge Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "H", $\overline{WE}$ = "L", BS0, BS1 = Bank, A10 = "L", A0 to A9, A11, A12 = Don't care)

The Bank Precharge command percharges the bank designated by BS. The precharged bank is switched from the active state to the idle state.

3. Precharge All Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "H", $\overline{WE}$ = "L", BS0, BS1 = Don't care, A10 = "H", A0 to A9, A11, A12 = Don't care)

The Precharge All command precharges all banks simultaneously. Then all banks are switched to the idle state.

4. Write Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BS0, BS1 = Bank, A10 = "L", A0 to A9, A11 = Column Address)

The write command performs a Write operation to the bank designated by BS. The write data are latched at both edges of DQS. The length of the write data (Burst Length) and column access sequence (Addressing Mode) must be in the Mode Register at power-up prior to the Write operation.

5. Write with Auto Precharge Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BS0, BS1 = Bank, A10 = "H", A0 to A9, A11 = Column Address)

The Write with Auto Precharge command performs the Precharge operation automatically after the Write operation. This command must not be interrupted by any other commands.

6. Read Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", BS0, BS1 = Bank, A10 = "L", A0 to A9, A11 = Column Address)

The Read command performs a Read operation to the bank designated by BS. The read data are synchronized with both edges of DQS. The length of read data (Burst Length), Addressing Mode and $\overline{CAS}$ Latency (access time from $\overline{CAS}$ command in a clock cycle) must be programmed in the Mode Register at power-up prior to the Read operation.

7. Read with Auto Precharge Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", BS0, BS1 = Bank, A10 = "H", A0 to A9, A11 = Column Address)

The Read with Auto precharge command automatically performs the Precharge operation after the Read operation.

1) READA $\geq t_{RAS\ (min)}$ - (BL/2) x t_{CK}

   Internal precharge operation begins after BL/2 cycle from Read with Auto Precharge command.

2) $t_{RCD(min)} \leq$ READA < $t_{RAS(min)}$ - (BL/2) x t_{CK}

   Data can be read with shortest latency, but the internal Precharge operation does not begin until after $t_{RAS\ (min)}$ has completed.

   This command must not be interrupted by any other command.

8. Mode Register Set Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BS0 = "L", BS1 = "L", A0 to A12 = Register Data)

The Mode Register Set command programs the values of $\overline{CAS}$ latency, Addressing Mode, Burst Length and DLL reset in the Mode Register. The default values in the Mode Register after power-up are undefined, therefore this command must be issued during the power-up sequence. Also, this command can be issued while all banks are in the idle state. Refer to the table for specific codes.

9. Extended Mode Register Set Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BS0 = "H", BS1 = "L", A0 to A12 = Register data)

The Extended Mode Register Set command can be implemented as needed for function extensions to the standard (SDR-SDRAM). Currently the only available mode in EMRS is DLL enable/disable, decoded by A0. The default value of the extended mode register is not defined; therefore this command must be issued during the power-up sequence for enabling DLL. Refer to the table for specific codes.

10. No-Operation Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "H", $\overline{WE}$ = "H")

The No-Operation command simply performs no operation (same command as Device Deselect).

11. Burst Read Stop Command

($\overline{RAS}$ = "H", $\overline{CAS}$ = "H", $\overline{WE}$ = "L")

The Burst stop command is used to stop the burst operation. This command is only valid during a Burst Read operation.

12. Device Deselect Command

($\overline{CS}$ = "H")

The Device Deselect command disables the command decoder so that the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Address inputs are ignored. This command is similar to the No-Operation command.

13. Auto Refresh Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", CKE = "L", BS0, BS1, A0 to A12 = Don't care)

The Auto Refresh command is used to refresh the row address provided by the internal refresh counter. The Refresh operation must be performed 8192 times within 64ms. The next command can be issued after t_{REF} from the end of the Auto Refresh command. When the Auto Refresh command is used, all banks must be in the idle state.

14. Self Refresh Entry Command

($\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "H", CKE = "L", BS0, BS1, A0 to A12 = don't care)

The Self Refresh Entry command is used to enter Self Refresh mode. While the device is in Self Refresh mode, all input and output buffer (except the CKE buffer) are disabled and the Refresh operation is automatically performed. Self Refresh mode is exited by taking CKE "high" (the Self Refresh Exit command). During self refresh, DLLI is disable.

15. Self Refresh Exit Command

(CKE = "H", $\overline{CS}$ = "H" or CKE = "H", $\overline{RAS}$ = "H", $\overline{CAS}$ = "H")

This command is used to exit from Self Refresh mode. Any subsequent commands can be issued after t_{XSNR} (t_{XSRD} for Read Command) from the end of this command.

16. Data Write Enable /Disable Command

(DM = "L/H" or LDM, UDM = "L/H")

During a Write cycle, the DM or LDM, UDM signal functions as Data Mask and can control every word of the input data. The LDM signal controls DQ0 to DQ7 and UDM signal controls DQ8 to DQ15.

9.3 Read Operation

Issuing the Bank Activate command to the idle bank puts it into the active state. When the Read command is issued after t_{RCD} from the Bank Activate command, the data is read out sequentially, synchronized with both edges of DQS (Burst Read operation). The initial read data becomes available after $\overline{CAS}$ latency from the issuing of the Read command. The $\overline{CAS}$ latency must be set in the Mode Register at power-up.

When the Precharge Operation is performed on a bank during a Burst Read and operation, the Burst operation is terminated.

When the Read with Auto Precharge command is issued, the Precharge operation is performed automatically after the Read cycle, then the bank is switched to the idle state. This command cannot be interrupted by any other commands. Refer to the diagrams for Read operation.

9.4 Write Operation

Issuing the Write command after t_{RCD} from the bank activate command. The input data is latched sequentially, synchronizing with both edges(rising &falling) of DQS after the Write command (Burst write operation). The burst length of the Write data (Burst Length) and Addressing Mode must be set in the Mode Register at power-up.

When the Precharge operation is performed in a bank during a Burst Write operation, the Burst operation is terminated.

When the Write with Auto Precharge command is issued, the Precharge operation is performed automatically after the Write cycle, then the bank is switched to the idle state, The Write with Auto Precharge command cannot be interrupted by any other command for the entire burst data duration.

Refer to the diagrams for Write operation.

9.5 Precharge

There are two Commands, which perform the precharge operation (Bank Precharge and Precharge All). When the Bank Precharge command is issued to the active bank, the bank is precharged and then switched to the idle state. The Bank Precharge command can precharge one bank independently of the other bank and hold the unprecharged bank in the active state. The maximum time each bank can be held in the active state is specified as $t_{RAS\ (max)}$. Therefore, each bank must be precharged within $t_{RAS(max)}$ from the bank activate command.

The Precharge All command can be used to precharge all banks simultaneously. Even if banks are not in the active state, the Precharge All command can still be issued. In this case, the Precharge operation is performed only for the active bank and the precharge bank is then switched to the idle state.

9.6 Burst Termination

When the Precharge command is used for a bank in a Burst cycle, the Burst operation is terminated. When Burst Read cycle is interrupted by the Precharge command, read operation is disabled after clock cycle of ($\overline{CAS}$ latency) from the Precharge command. When the Burst Write cycle is interrupted by the Precharge command . the input circuit is reset at the same clock cycle at which the precharge command is issued. In this case, the DM signal must be asserted "high": during t_{WR} to prevent writing the invalided data to the cell array.

When the Burst Read Stop command is issued for the bank in a Burst Read cycle, the Burst Read operation is terminated. The Burst read Stop command is not supported during a write burst operation. Refer to the diagrams for Burst termination.

9.7 Refresh Operation

Two types of Refresh operation can be performed on the device: Auto Refresh and Self Refresh. By repeating the Auto Refresh cycle, each bank in turn refreshed automatically. The Refresh operation must be performed 8192 times(rows)within 64ms. The period between the Auto Refresh command and the next command is specified by t_{RFC}.

Self Refresh mode enter issuing the Self Refresh command (CKE asserted "low"). while all banks are in the idle state. The device is in Self Refresh mode for as long as cke held "low". In the case of 8192 burst Auto Refresh commands, 8192 burst Auto Refresh commands must be performed within 7.8 μS before entering and after exiting the Self Refresh mode. In the case of distributed Auto Refresh commands, distributed auto refresh commands must be issued every 7.8 μS and the last distributed Auto Refresh commands must be performed within 7.8 μS before entering the self refresh mode. After exiting from the Self Refresh mode, the refresh operation must be performed within 7.8 μS. In Self Refresh mode, all input/output buffers are disable, resulting in lower power dissipation (except CKE buffer). Refer to the diagrams for Refresh operation.

9.8 Power Down Mode

Two types of Power Down Mode can be performed on the device: Active Standby Power Down Mode and Precharge Standby Power Down Mode.

When the device enters the Power Down Mode, all input/output buffers and DLL are disabled resulting in low power dissipation (except CKE buffer).

Power Down Mode enter asserting CKE "low" while the device is not running a burst cycle. Taking CKE: "high" can exit this mode. When CKE goes high, a No operation command must be input at next CLK rising edge. Refer to the diagrams for Power Down Mode.

9.9 Mode Register Operation

The mode register is programmed by the Mode Register Set command (MRS/EMRS) when all banks are in the idle state. The data to be set in the Mode Register is transferred using the A0 to A12 and BS0, BS1 address inputs.

The Mode Register designates the operation mode for the read or write cycle. The register is divided into five filed: (1) Burst Length field to set the length of burst data (2) Addressing Mode selected bit to designate the column access sequence in a Burst cycle (3) $\overline{CAS}$ Latency field to set the assess time in clock cycle (4) DLL reset field to reset the dll (5) Regular/Extended Mode Register filed to select a

type of MRS (Regular/Extended MRS). EMRS cycle can be implemented the extended function (DLL enable/Disable mode)

The initial value of the Mode Register (including EMRS) after power up is undefined; therefore the Mode Register Set command must be issued before power operation.

1. Burst Length field (A2 to A0)

This field specifies the data length for column access using the A2 to A0 pins and sets the Burst Length to be 2, 4, and 8 words.

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2 words
0	1	0	4 words
0	1	1	8 words
1	x	x	Reserved

2. Addressing Mode Select (A3)

The Addressing Mode can be one of two modes; Interleave mode or Sequential Mode, When the A3 bit is "0", Sequential mode is selected. When the A3 bit is "1", Interleave mode is selected. Both addressing Mode support burst length 2, 4, and 8 words.

A3	Addressing Mode
0	Sequential
0	Interleave

- **Address Sequence of Sequential Mode**

  A column access is performed by incrementing the column address input to the device. The address is varied by the Burst Length as the following.

Addressing Sequence of Sequential Mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	n	2 words (address bits is A0)
Data 1	n + 1	not carried from A0 to A1
Data 2	n + 2	4 words (address bit A0, A1)
Data 3	n + 3	Not carried from A1 to A2
Data 4	n + 4	
Data 5	n + 5	8 words (address bits A2, A1 and A0)
Data 6	n + 6	Not carried from A2 to A3
Data 7	n + 7	

- **Addressing Sequence of Interleave Mode**

  A Column access is started from the inputted column address and is performed by interleaving the address bits in the sequence shown as the following.

9.9.1.1 Address Sequence for Interleave Mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	A8 A7 A6 A5 A4 A3 A2 A1 A0	2 words
Data 1	A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$	
Data 2	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0	4 words
Data 3	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ $\overline{A0}$	
Data 4	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 A0	8 words
Data 5	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 $\overline{A0}$	
Data 6	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ A0	
Data 7	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ $\overline{A0}$	

3. $\overline{CAS}$ Latency field (A6 to A4)

This field specifies the number of clock cycles from the assertion of the Read command to the first data read. The minimum values of $\overline{CAS}$ Latency depends on the frequency of CLK.

A6	A5	A4	$\overline{CAS}$ Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	2.5
1	1	1	Reserved

4. DLL Reset bit (A8)

This bit is used to reset DLL. When the A8 bit is "1", DLL is reset.

5. Mode Register /Extended Mode register change bits (BS0, BS1)

These bits are used to select MRS/EMRS.

BS1	BS0	A12-A0
0	0	Regular MRS Cycle
0	1	Extended MRS Cycle
1	x	Reserved

6. Extended Mode Register field

1) DLL Switch field (A0)

This bit is used to select DLL enable or disable

A0	DLL
0	Enable
1	Disable

2) Output Driver Size Control field (A1)

This bit is used to select Output Driver Size, both Full strength and Half strength are based on JEDEC standard.

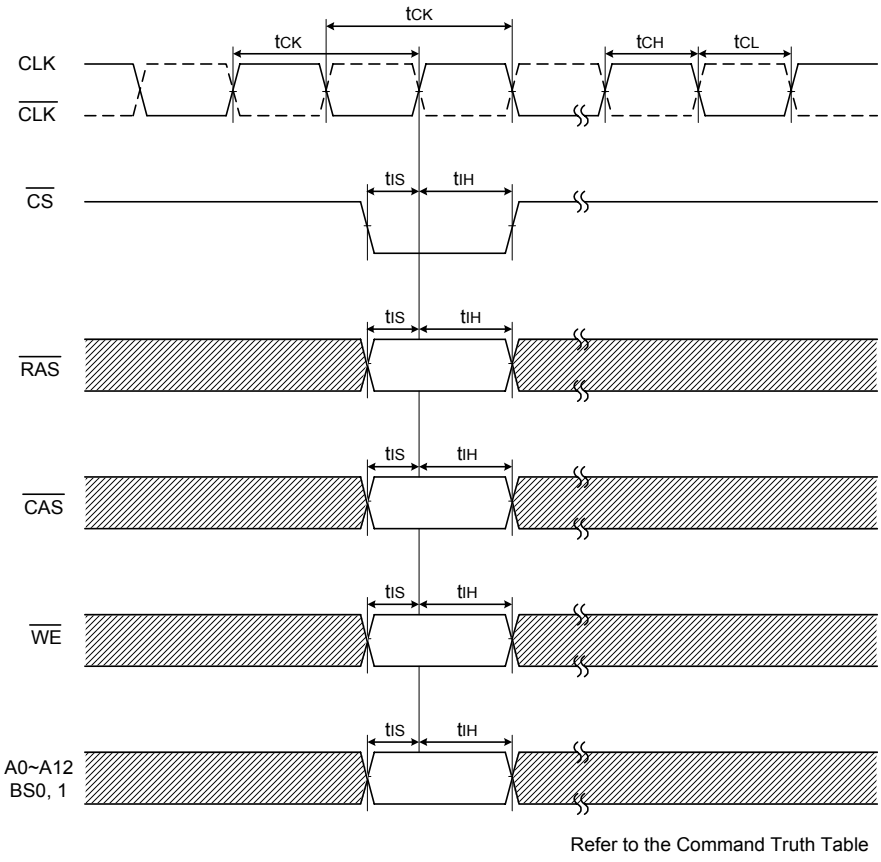
A1	Output Driver
0	Full Strength
1	Half Strength

7. Reserved field

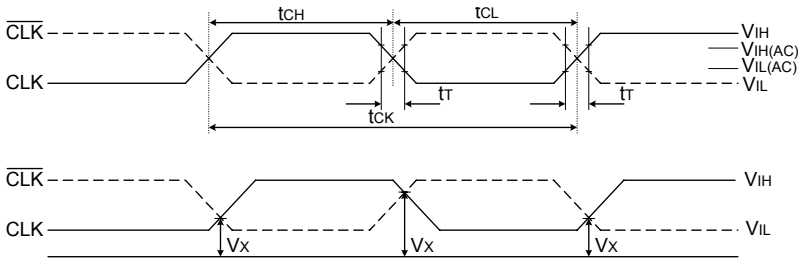
- Test mode entry bit (A7)
  This bit is used to enter Test mode and must be set to "0" for normal operation.
- Reserved bits (A9, A10, A11, A12)
  These bits are reserved for future operations. They must be set to "0" for normal operation.

10. TIMING WAVEFORMS

10.1 Command Input Timing

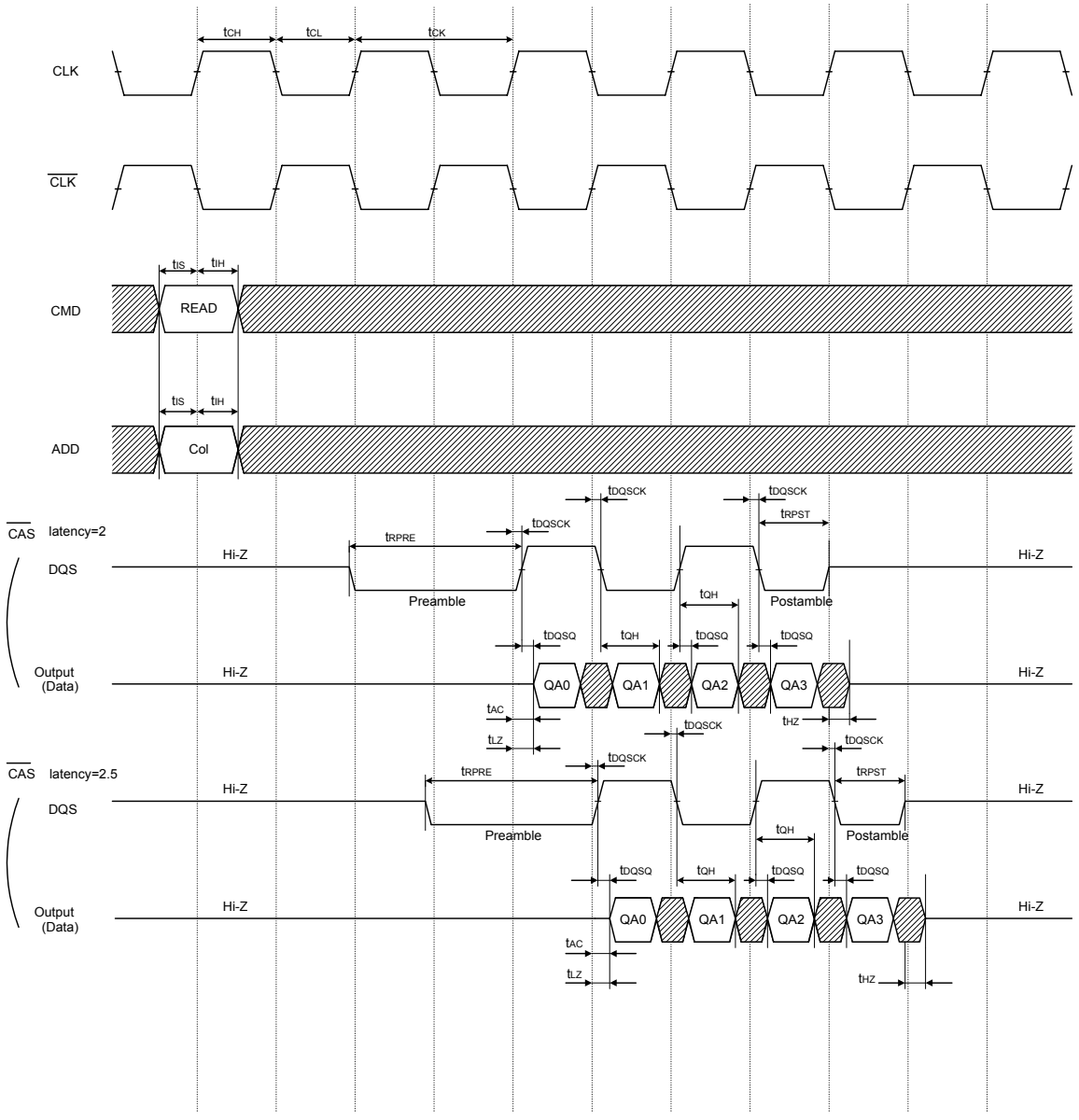


10.2 Timing of the CLK Signals



Timing Waveforms, continued

10.3 Read Timing (Burst Length = 4)

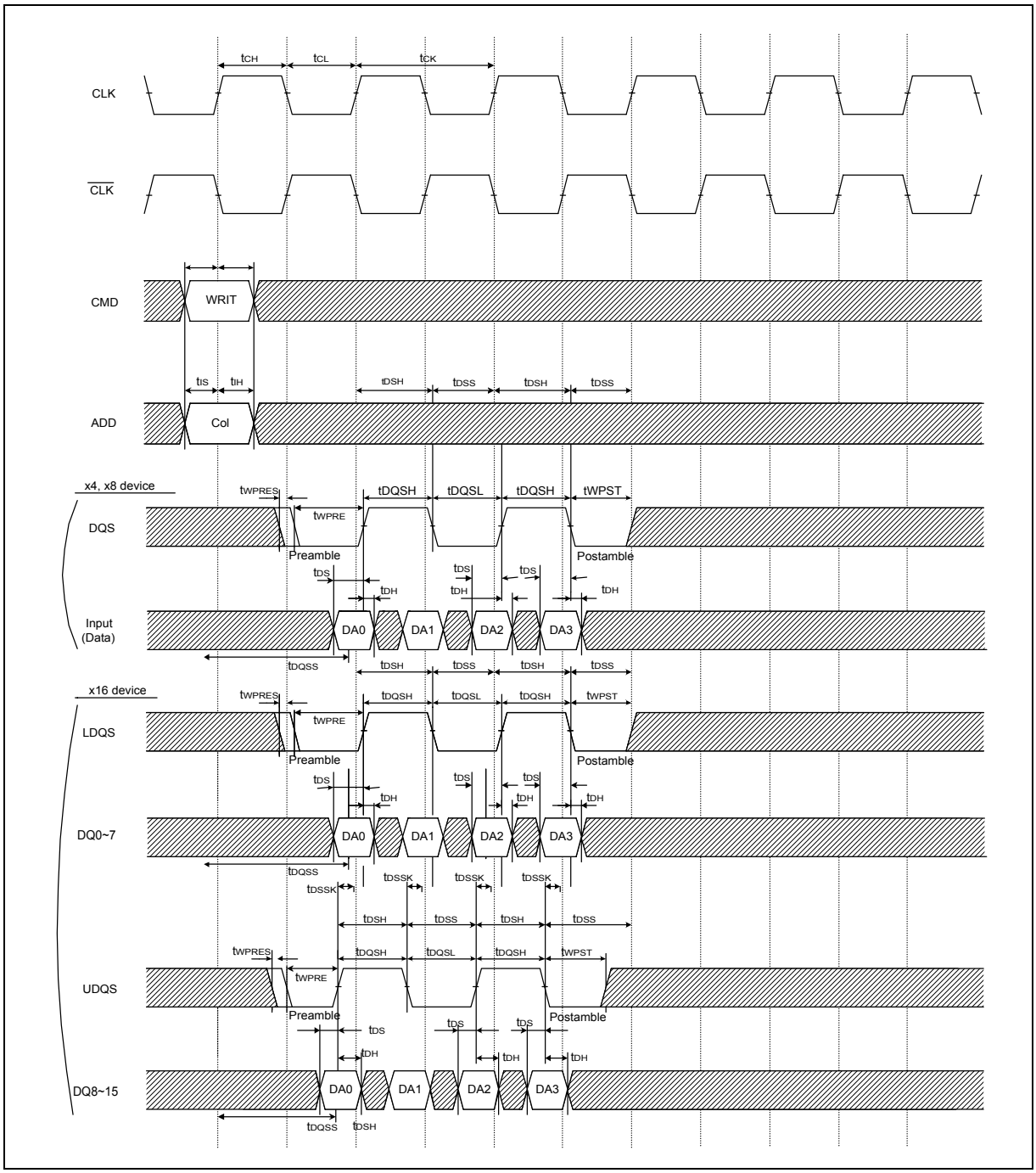


Note: The correspondence of LDQS, UDQS to DQ. (W942516AH)

LDQS	DQ0~7
UDQS	DQ8~15

Timing Waveforms, continued

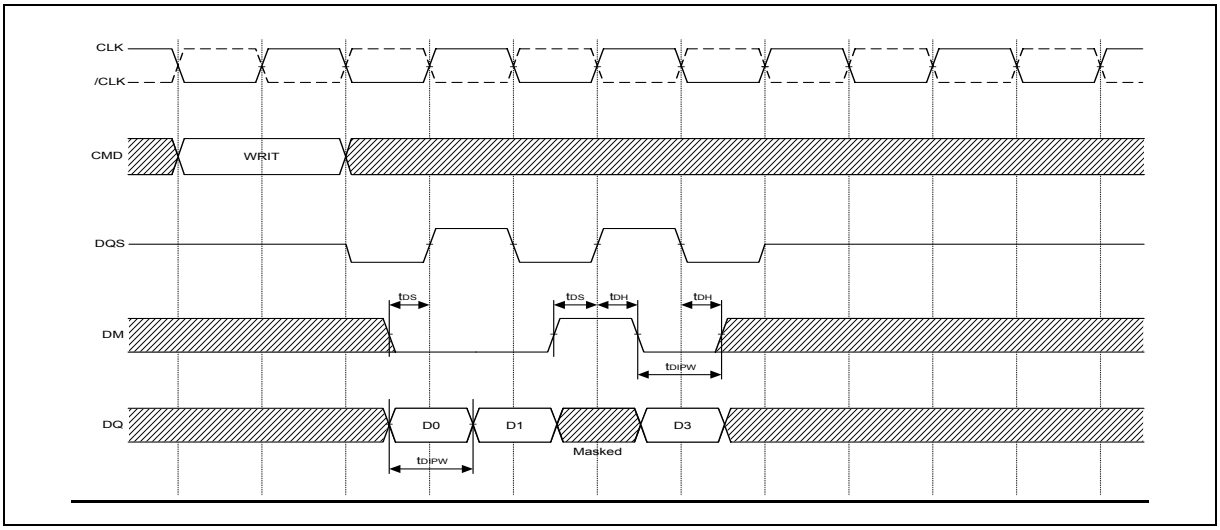
10.4 Write Timing (Burst Length = 4)



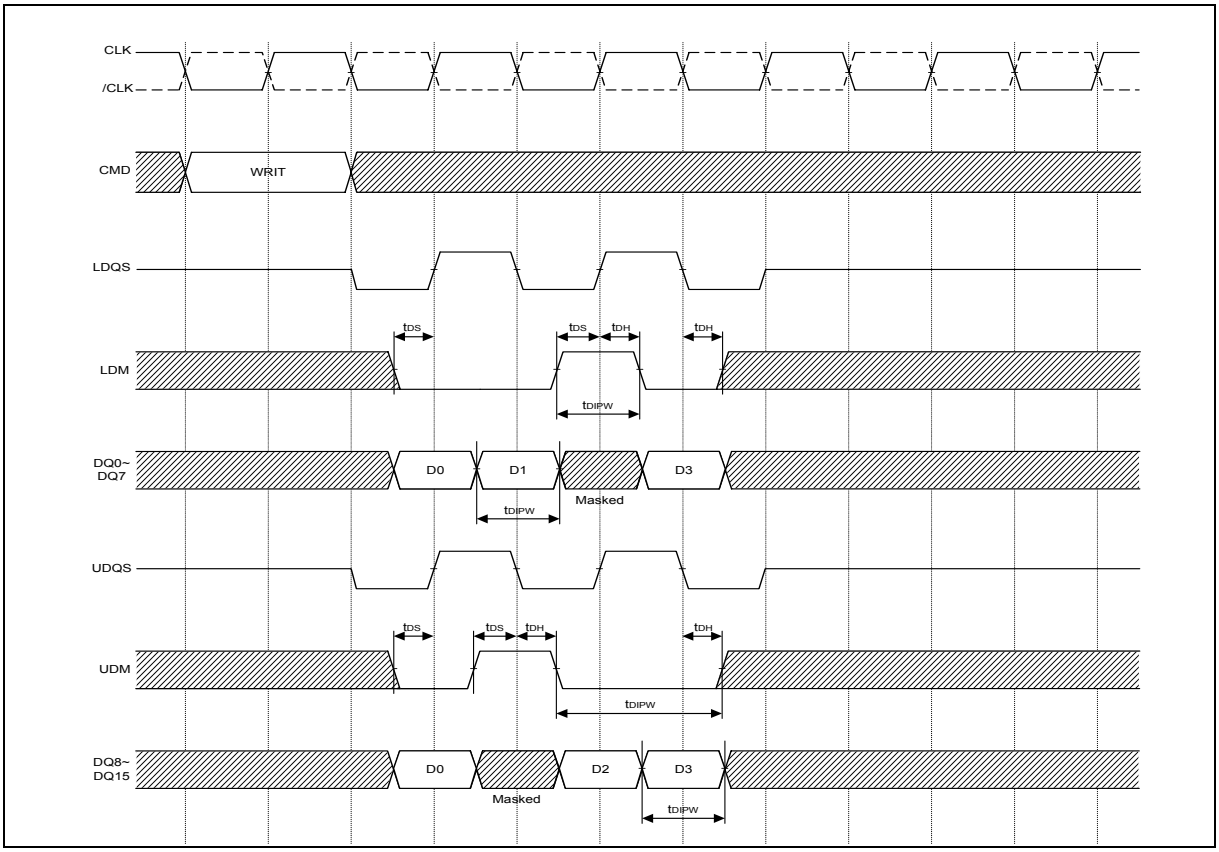
Note: x16 has 2DQS's (UDQS for uper byte and LDQS for lower byte). Even if one of the 2 bytes is not used, both UDQS and LDQS must be toggled.

Timing Waveforms, continued

10.5 DM, Data Mask (W942508CH /W942504CH)

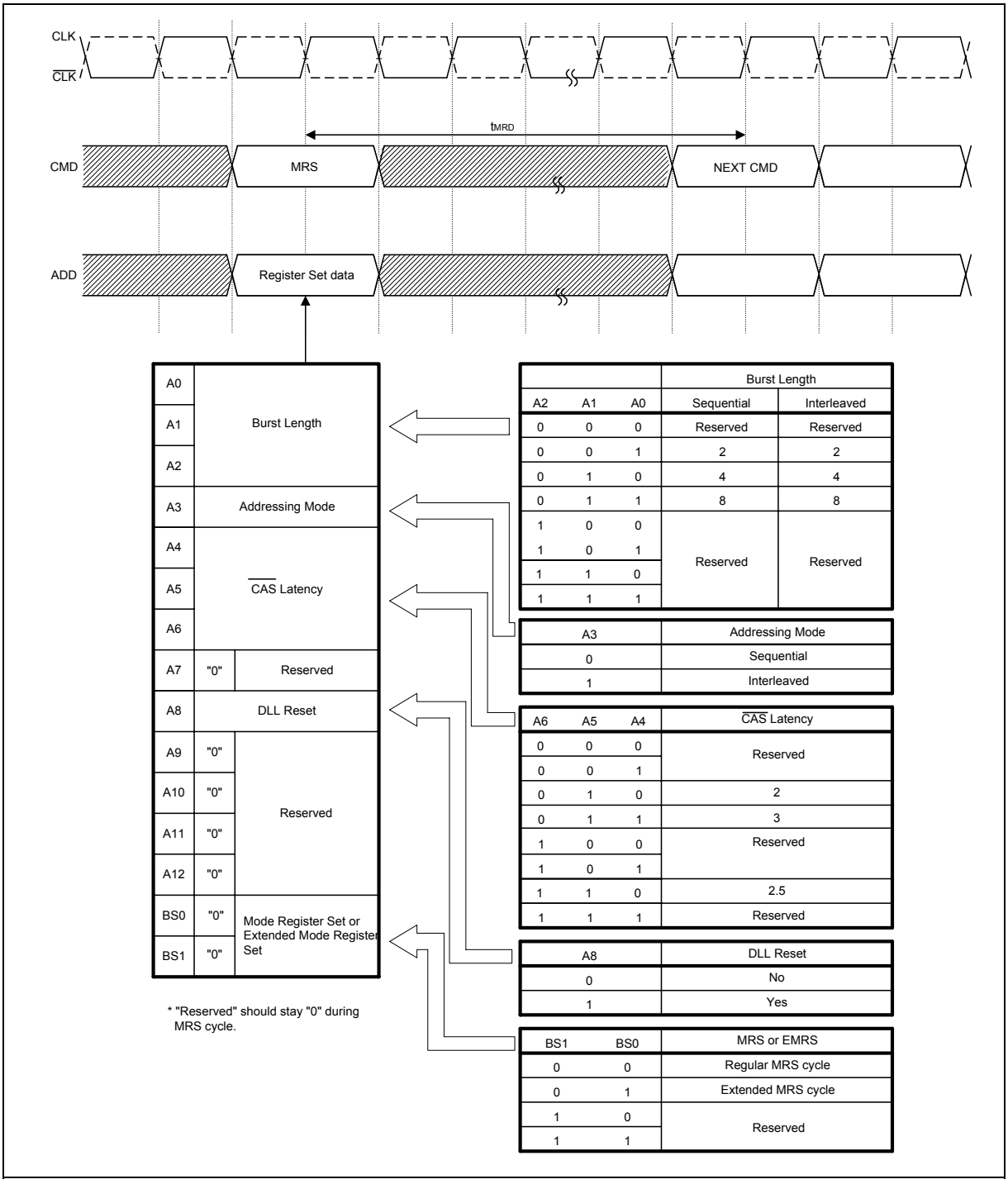


10.6 DM, Data Mask (W942516CH)



Timing Waveforms, continued

10.7 Mode Register Set (MRS) Timing



			Burst Length	
A2	A1	A0	Sequential	Interleaved
0	0	0	Reserved	Reserved
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1		
1	1	0		
1	1	1		

A3	Addressing Mode
0	Sequential
1	Interleaved

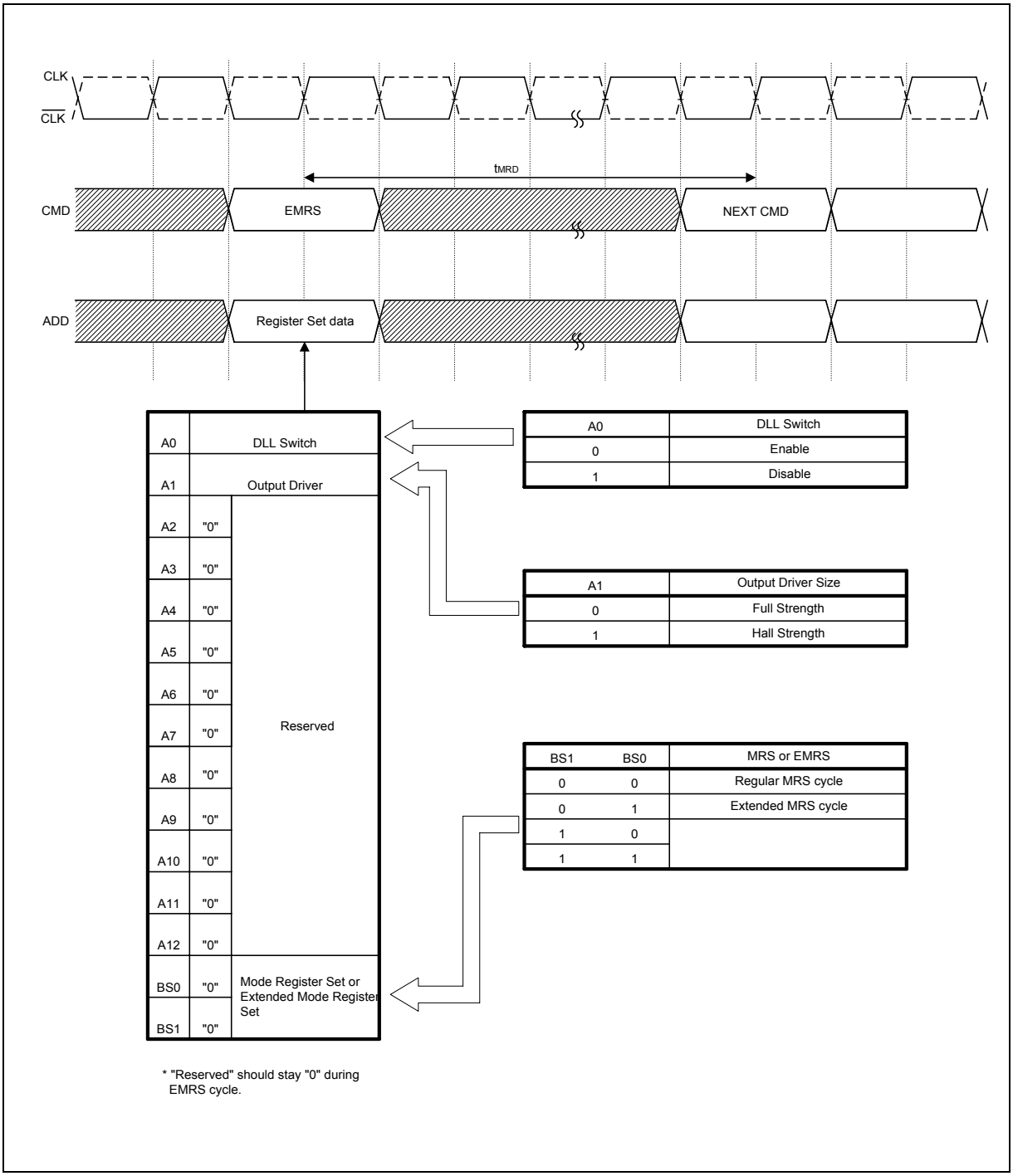
A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	
1	1	0	2.5
1	1	1	Reserved

A8	DLL Reset
0	No
1	Yes

BS1	BS0	MRS or EMRS
0	0	Regular MRS cycle
0	1	Extended MRS cycle
1	0	Reserved
1	1	

Timing Waveforms, continued

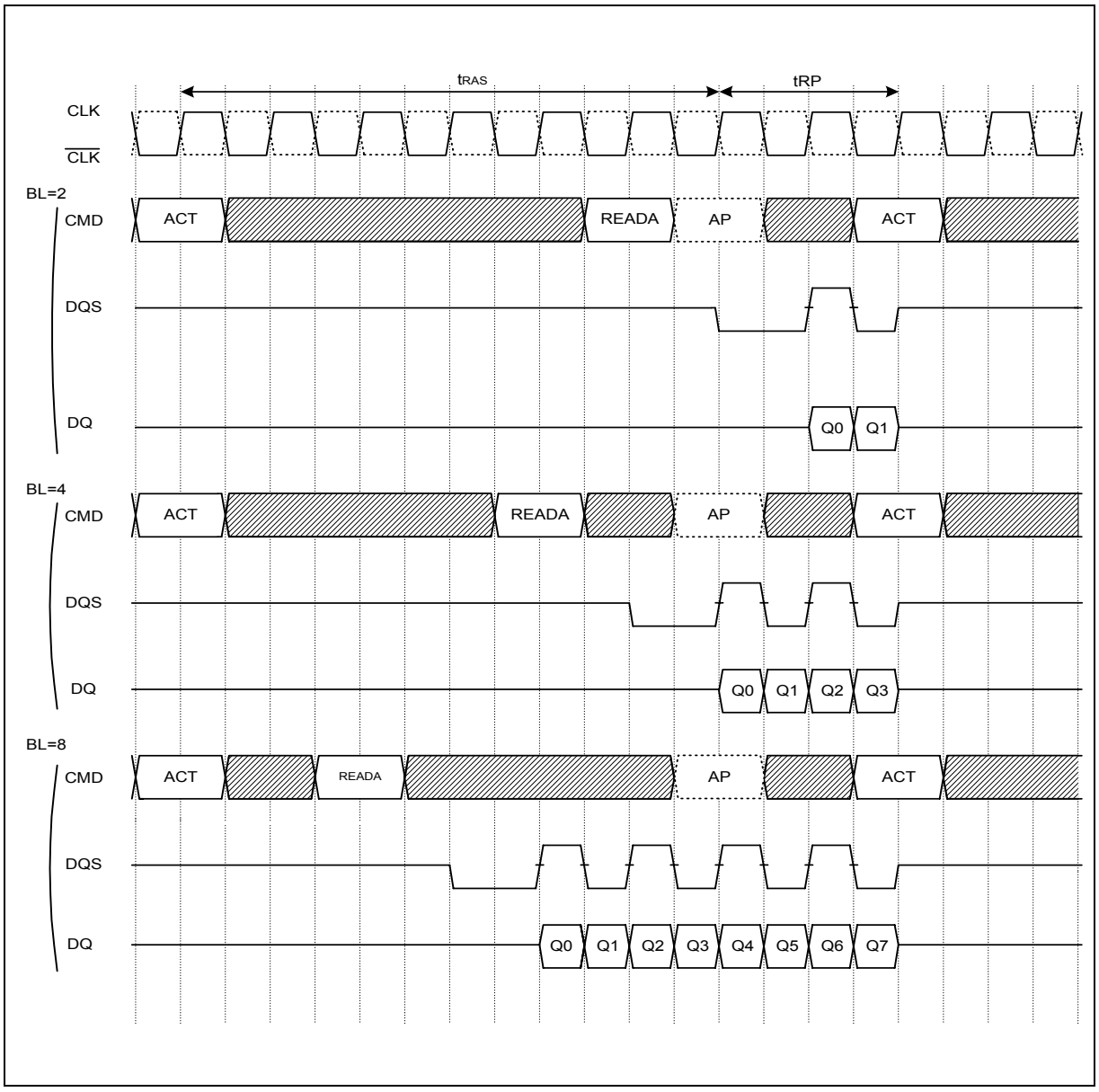
10.8 Extend Mode Register Set (EMRS) Timing



Timing Waveforms, continued

10.9 Auto Precharge Timing (Read Cycle, CL = 2)

1) tRCD (READA) ≥ tRAS (min) – (BL/2) × tCK



Notes: CL2 shown; same command operation timing with CL = 2.5

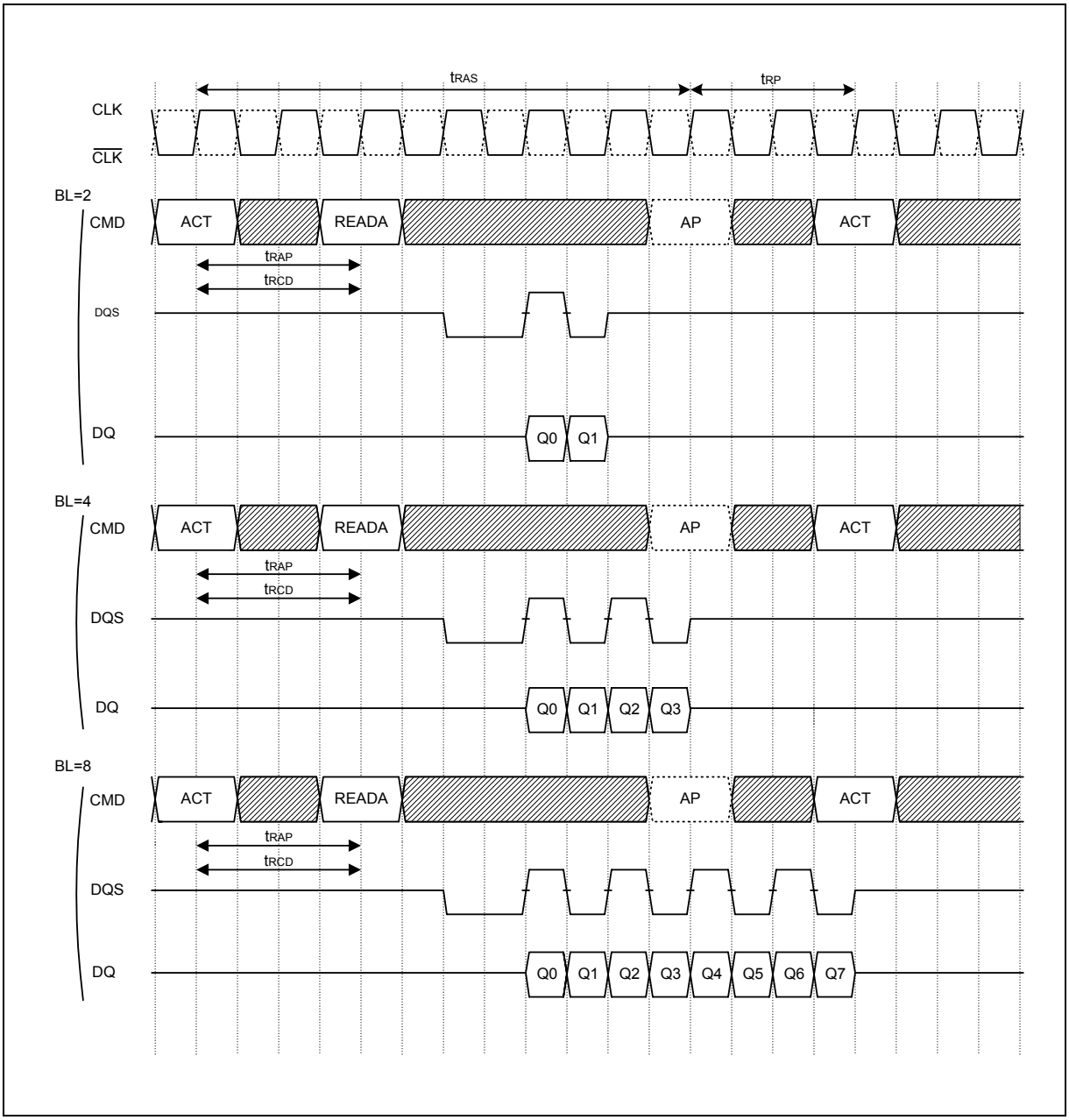
In this case, the internal precharge operation begin after BL/2 cycle from READA command.

AP Represents the start of internal precharging.

The Read with Auto precharge command cannot be interrupted by any other command.

Auto Precharge Timing (Read cycle, CL = 2), continued

2) tRCD/RAP(min) ≤ tRCD (READA) < tRAS (min) – (BL/2) × tCK



Notes: CL2 shown; same command operation timing with CL = 2.5

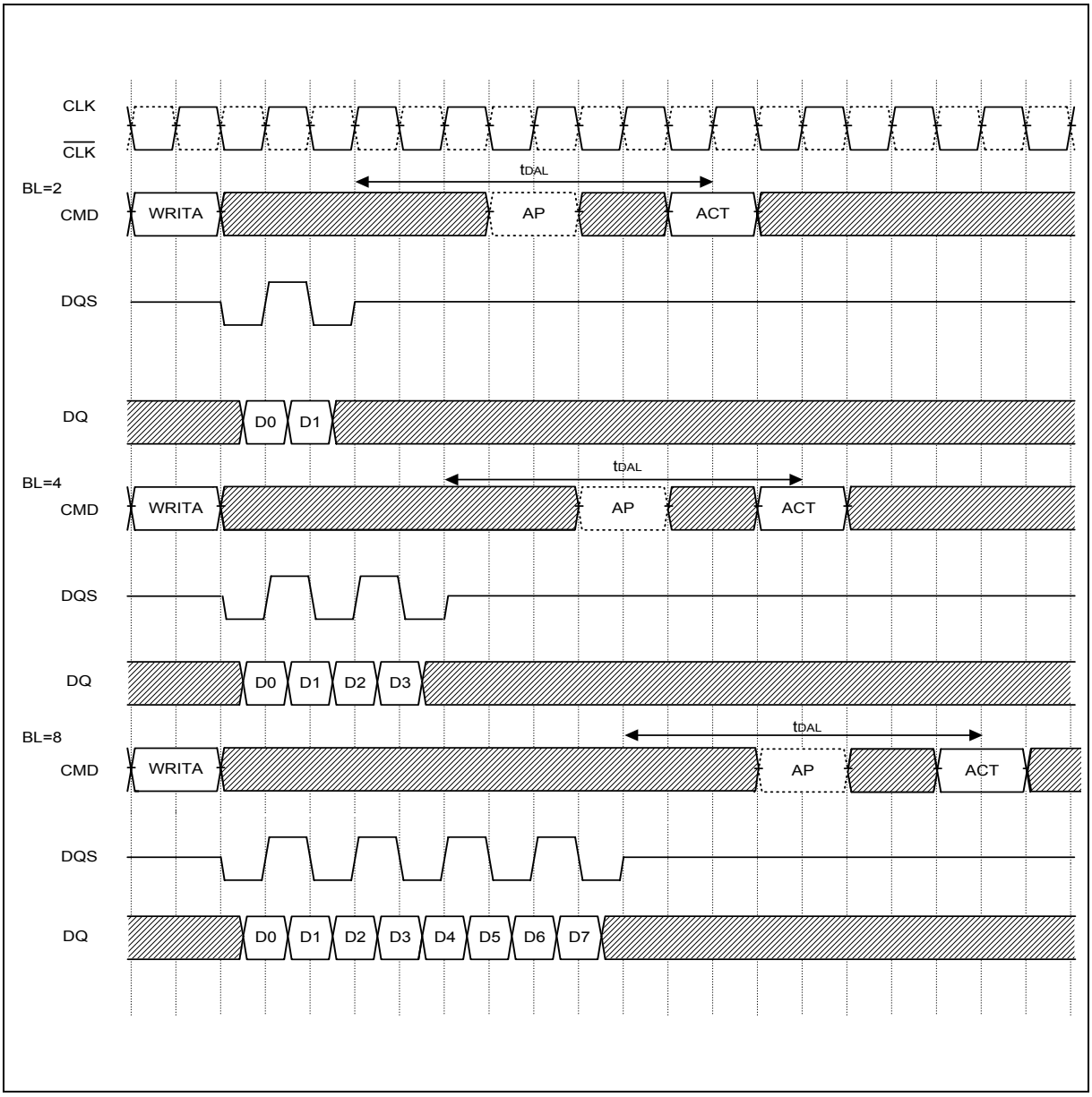
In this case, the internal precharge operation does not begin until after tRAS (min) has command.

AP Represents the start of internal precharging.

The Read with Auto Precharge command cannot be interrupted by any other command.

Timing Waveforms, continued

10.10 Auto Precharge Timing (Write Cycle)

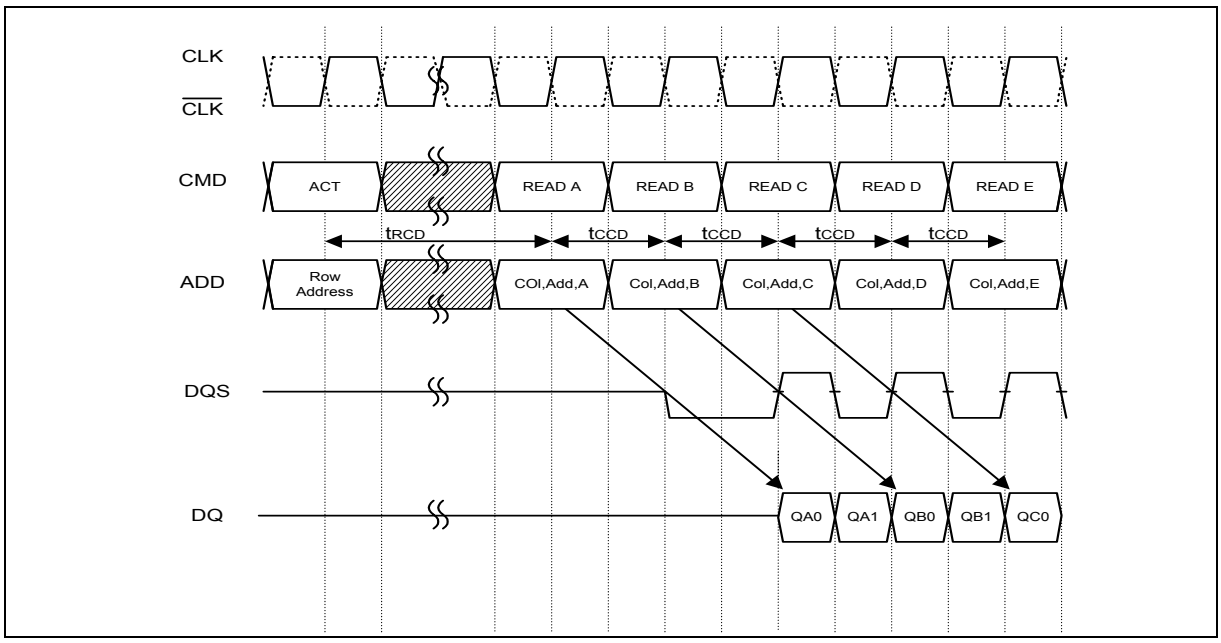


The Write with Auto Precharge command cannot be interrupted by any other command.

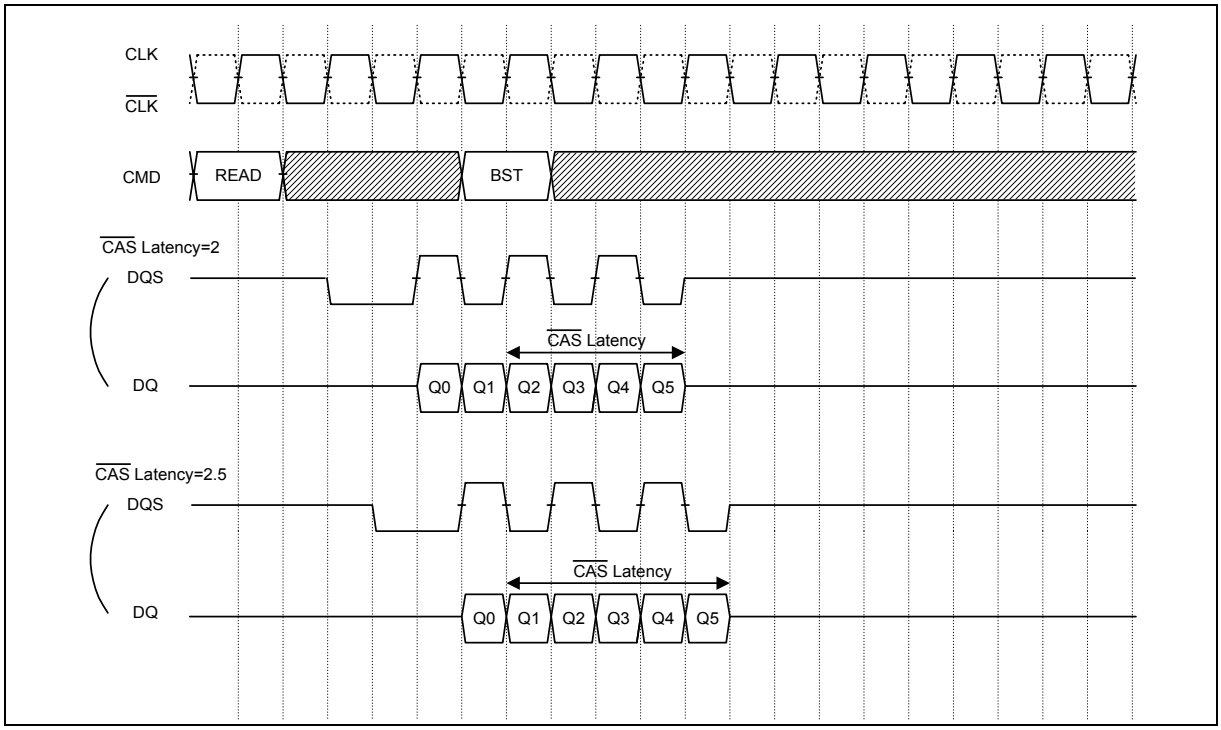
AP Represents the start of internal precharging .

Timing Waveforms, continued

10.11 Read Interrupted by Read (CL = 2, BL = 2, 4, 8)

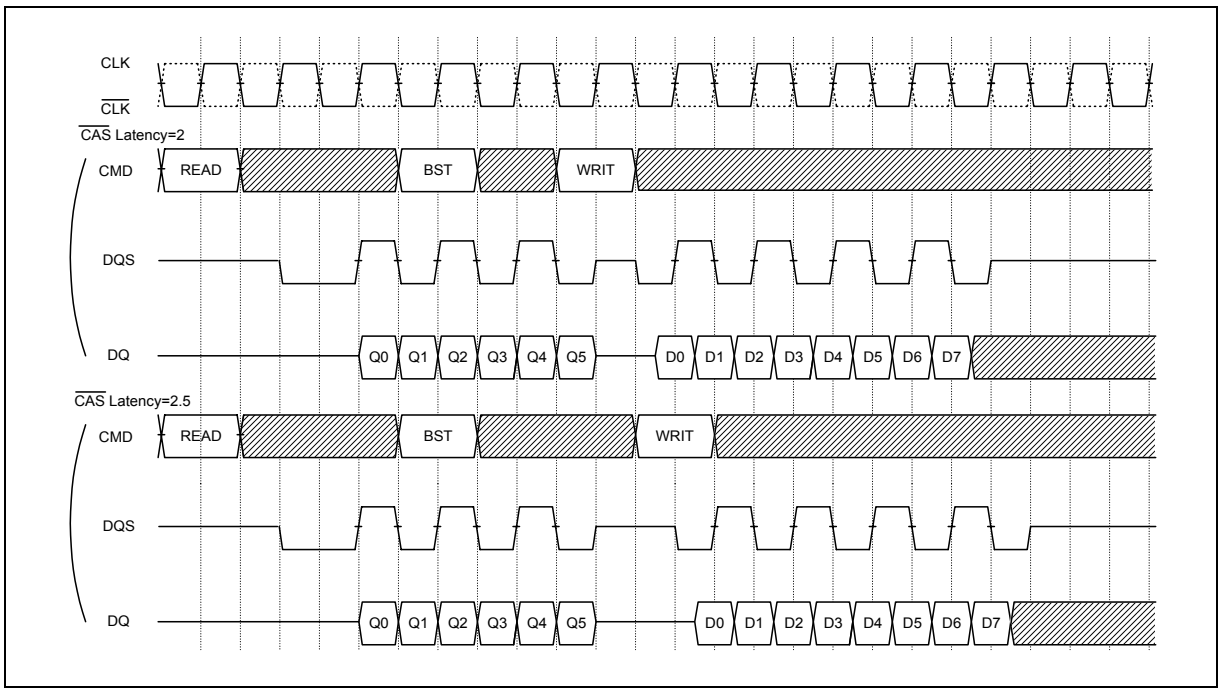


10.12 Burst Read Stop (BL = 8)



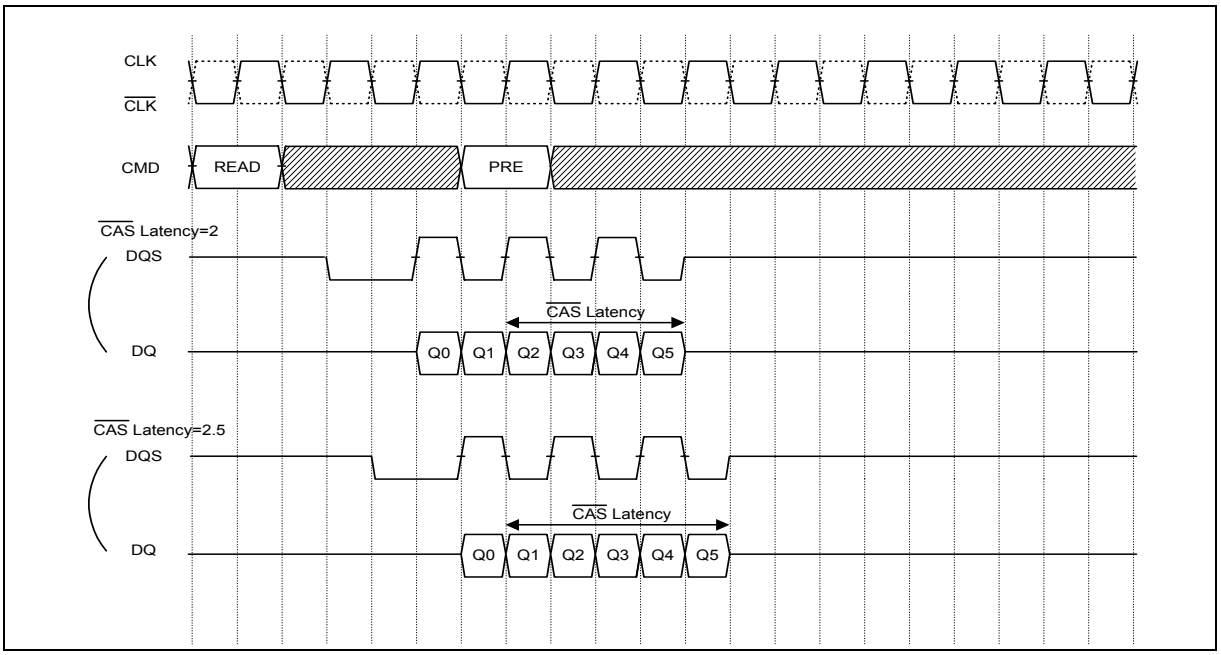
Timing Waveforms, continued

10.13 Read Interrupted by Write & BST (BL = 8)



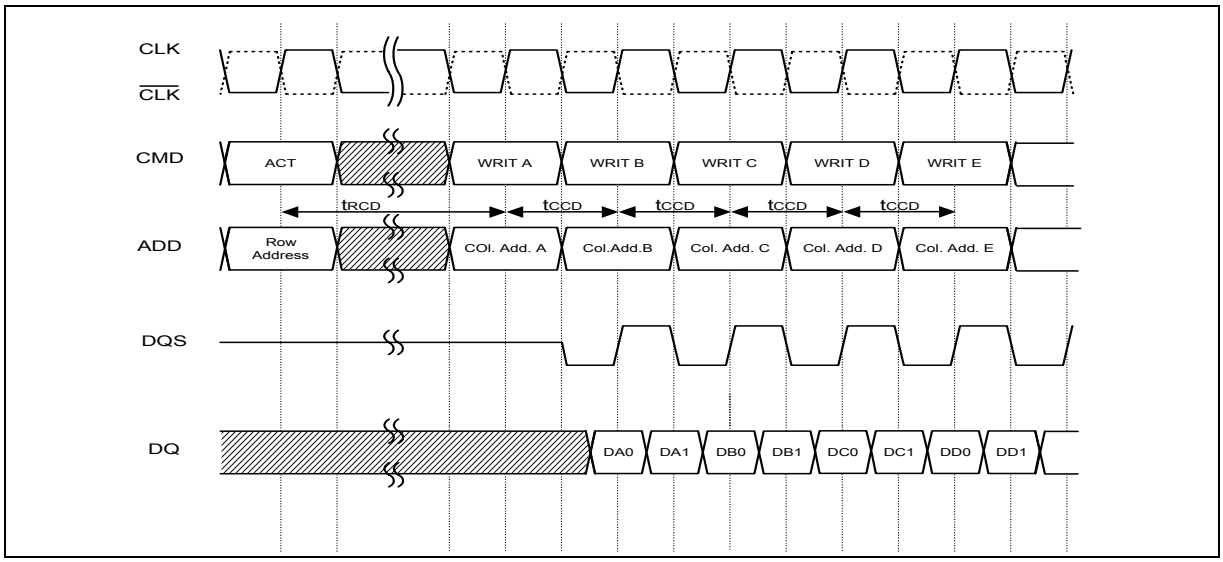
Burst Read cycle must be terminated by BST Command to avoid I/O conflict.

10.14 Read Interrupted by Precharge (BL = 8)

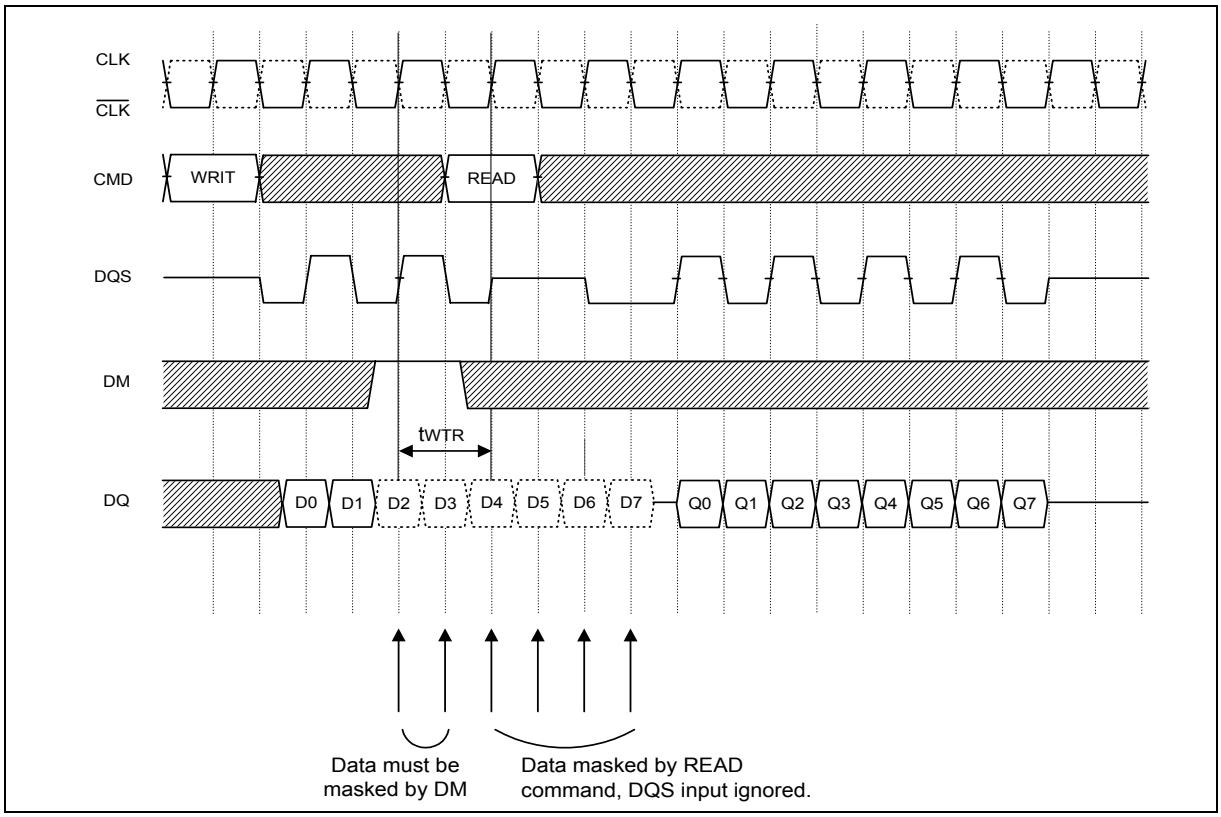


Timing Waveforms, continued

10.15 Write Interrupted by Write (BL = 2, 4, 8)

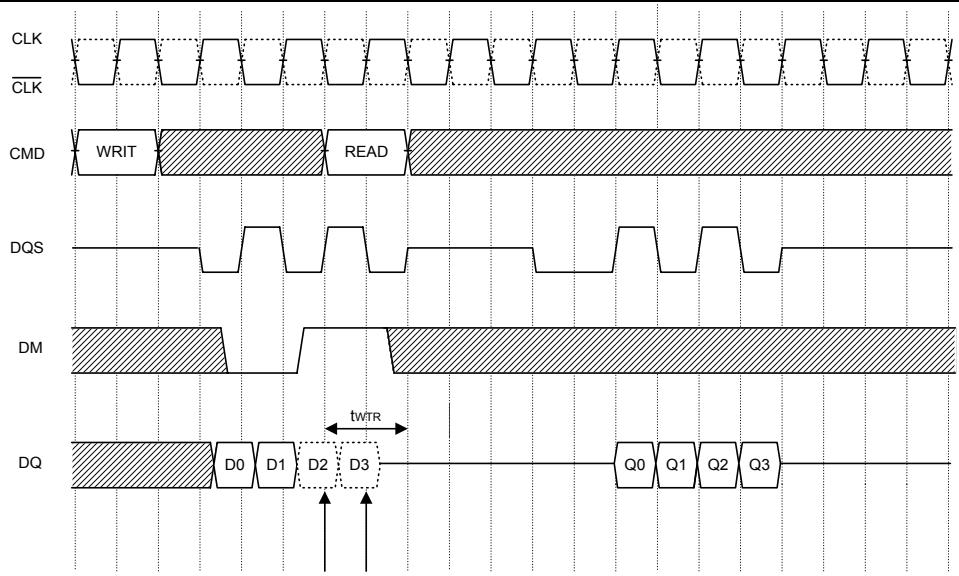


10.16 Write Interrupted by Read (CL = 2, BL = 8)

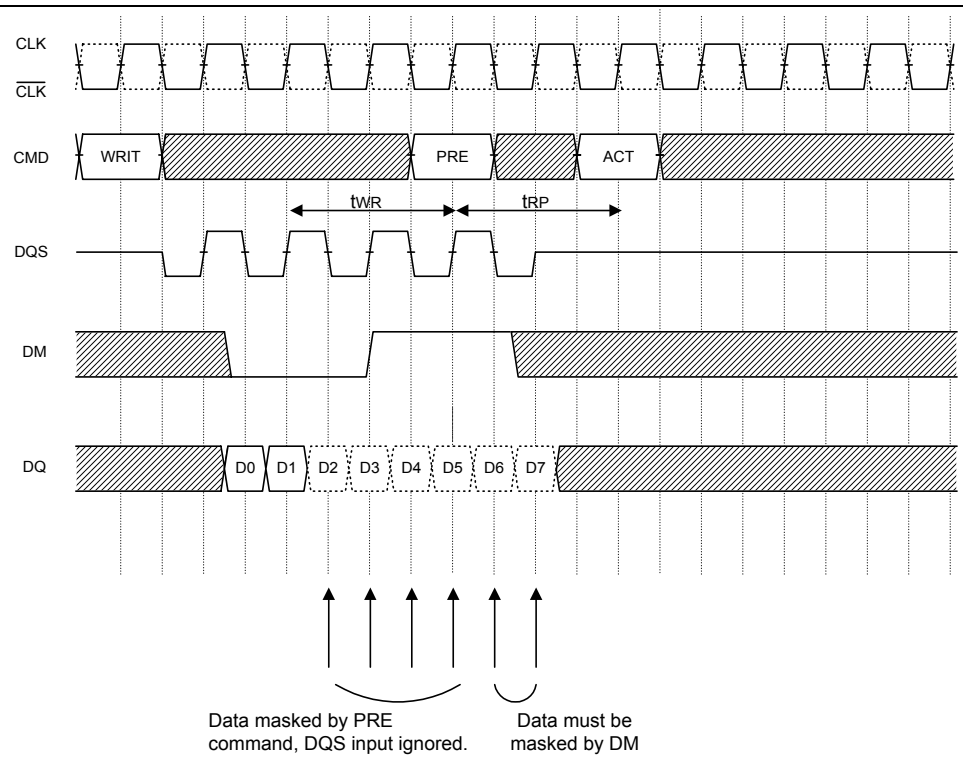


Timing Waveforms, continued

10.17 Write Interrupted by Read (CL = 2.5, BL = 4)



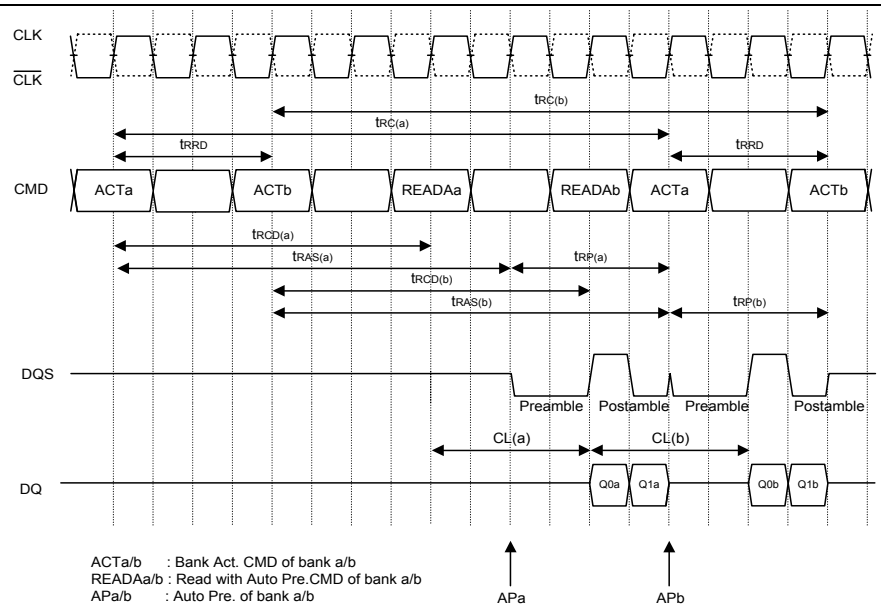
10.18 Write Interrupted by Precharge (BL = 8)



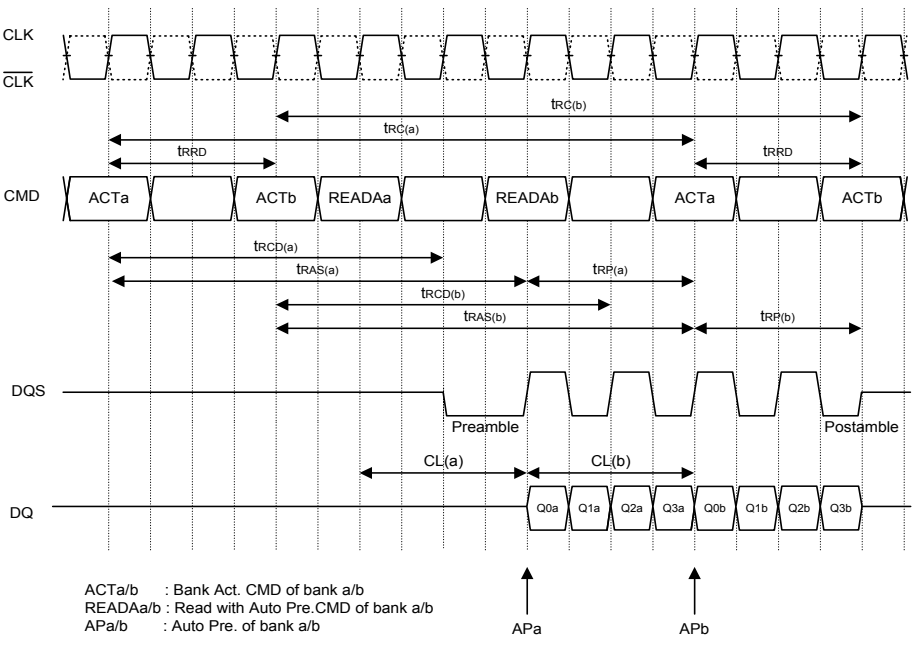
Timing Waveforms, continued

10.19 2 Bank Interleave Read Operation (CL = 2, BL = 2)

∗ tCK = 100 MHz

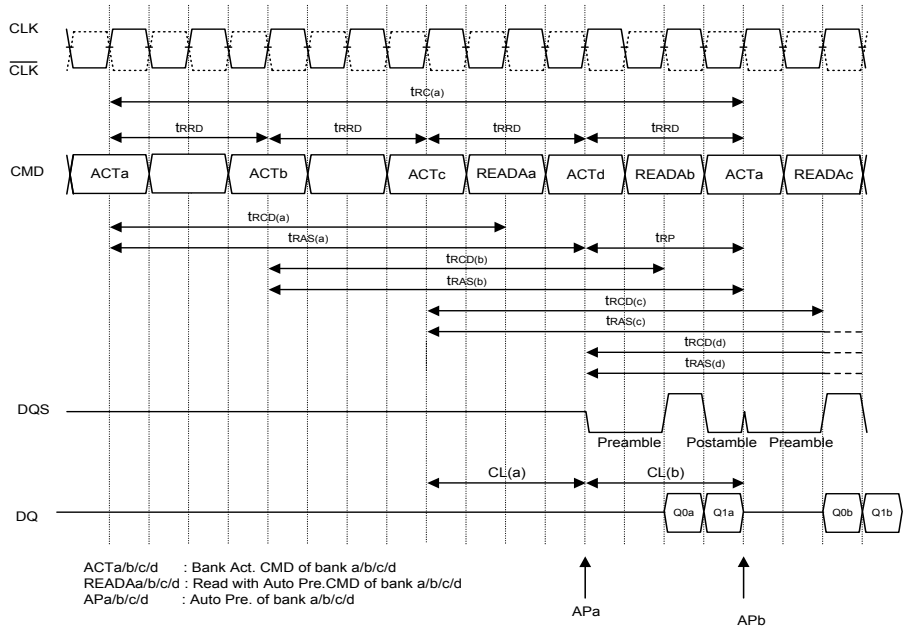


10.20 2 Bank Interleave Read Operation (CL = 2, BL = 4)

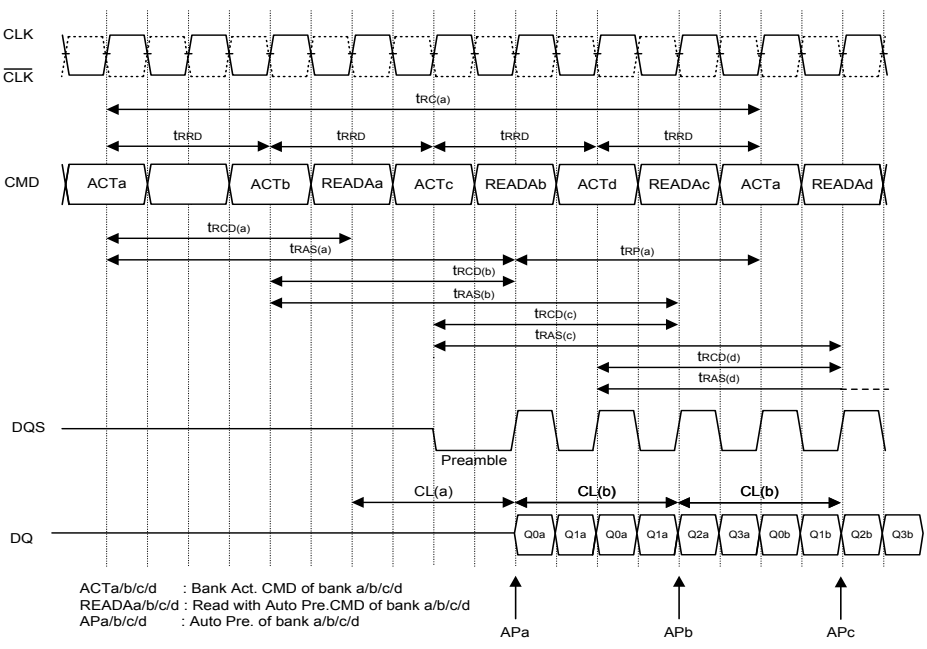


Timing Waveforms, continued

10.21 4 Bank Interleave Read Operation (CL = 2, BL = 2)

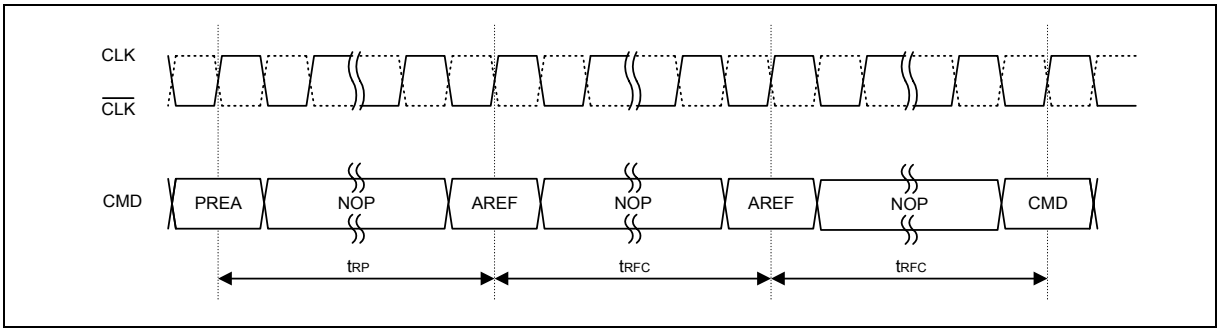


10.22 4 Bank Interleave Read Operation (CL = 2, BL = 4)



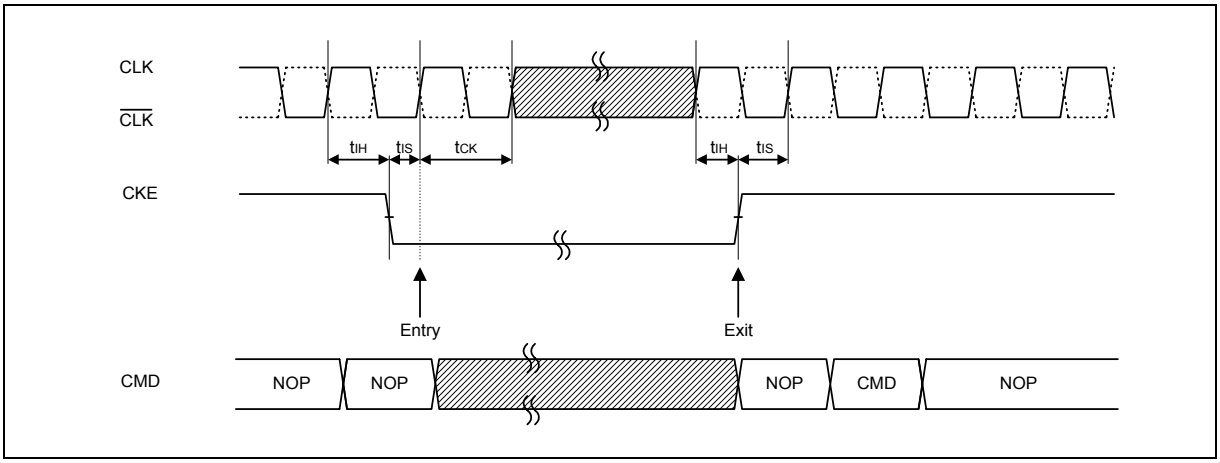
Timing Waveforms, continued

10.23 Auto Refresh Cycle

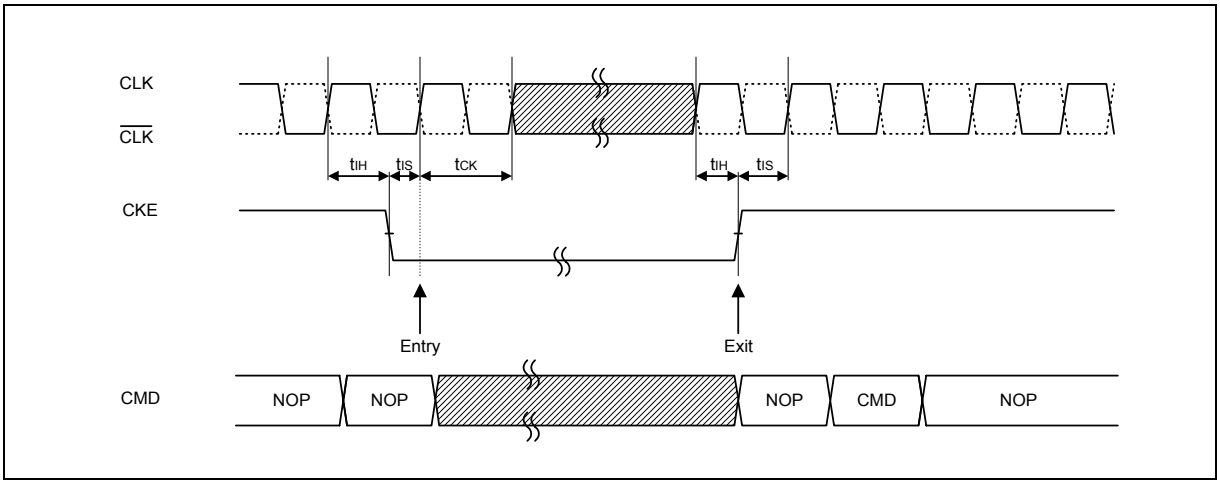


CKE has to be kept "High" level for Auto-Refresh cycle.

10.24 Active Power Down Mode Entry and Exit Timing

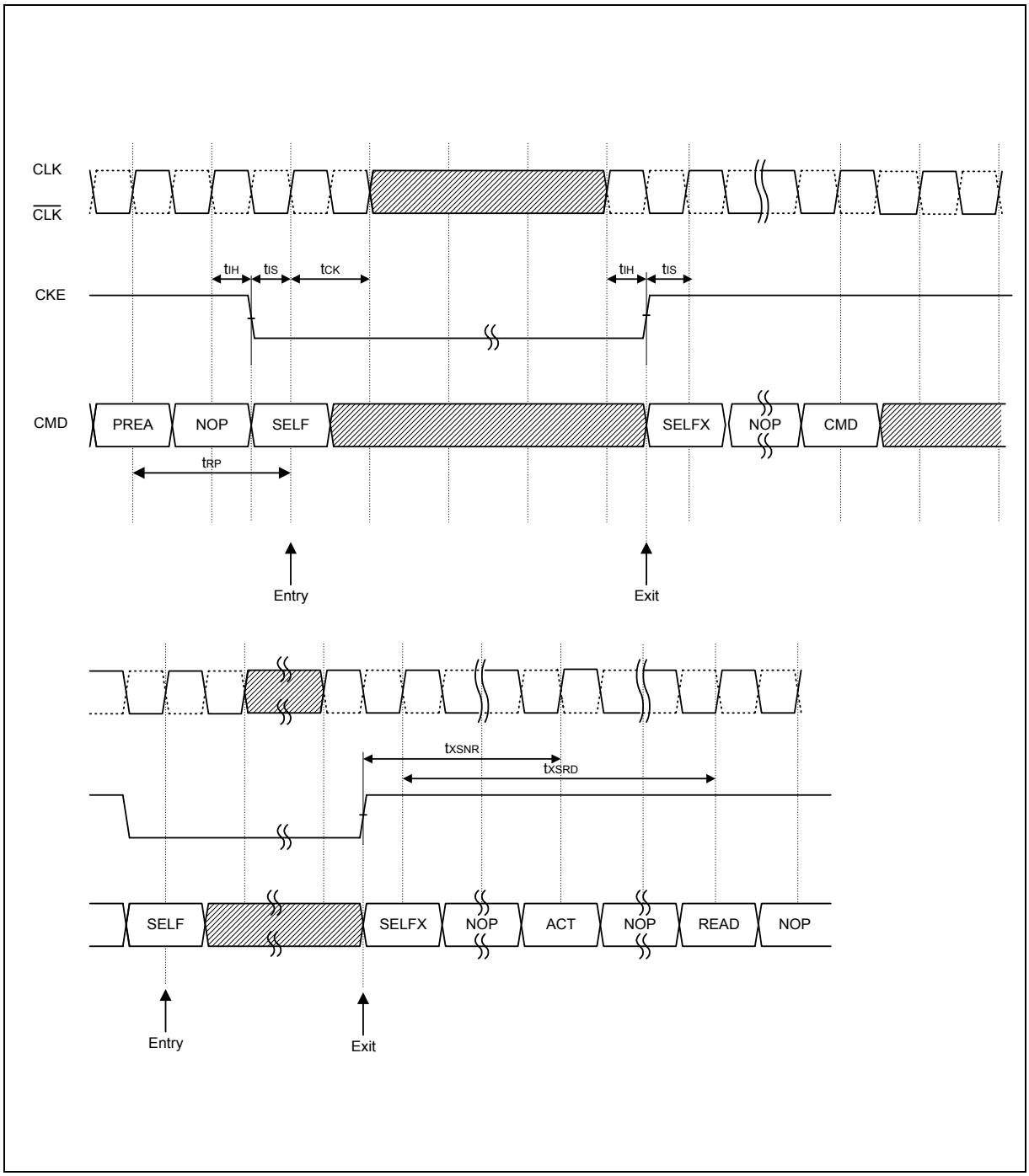


10.25 Precharged Power Down Mode Entry and Exit Timing



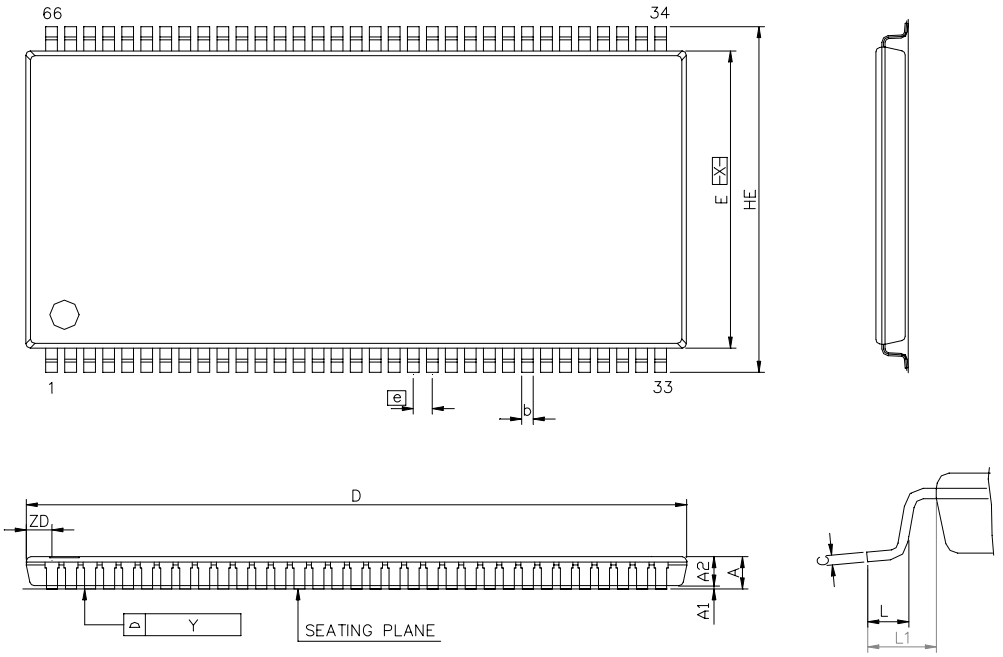
Timing Waveforms, continued

10.26 Self Refresh Entry and Exit Timing



11. PACKAGE DIMENSION

TSOP 66l – 400 mil



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.20	–	–	0.047
A1	0.05	–	0.15	0.002	–	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.042
b	0.17	0.24	0.32	0.007	0.009	0.013
c	0.09	0.145	0.2	0.004	0.006	0.008
D	–	–	22.62	–	–	0.891
HE	11.74	11.76	11.78	0.462	0.463	0.464
E	10.15	10.16	10.17	0.3996	0.400	0.4004
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.6	0.8	0.10	0.024	0.031	0.0039
e	0.65 BASIC			0.026 BASIC		
Y	0.1 BASIC			0.004 BASIC		
ZD	0.71 REF			0.028 REF		

12. REVISION HISTORY

REVISION	DATE	PAGE	DESCRIPTION
A1	Aug. 28, 2002	-	Preliminary datasheet
	Jan. 9, 2003	28	Add CAS Latency = 3 option
	Feb. 14, 2003	-	Modified AC timing spec.
A2	May 20, 2003		Add CL2.5 optional in DDR400

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

Winbond Electronics (Shanghai) Ltd.
27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Taipei Office
9F, No.480, Rueiguang Rd.,
Neihu District, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064