SmartV.90 USB Modem Device Set

V.90 CX81801 Smart Modem with CX20493 SmartDAA® and CX11253 USB Interface Device

Data Sheet

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CONEXANT™

Revision Record

Revision	Date	Comments
B	2/24/2003	Rev. B release.
A	10/17/2002	Initial release.

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1. Introduction

1.1 Overview

The Conexant™ SmartV.90 USB Modem supports V.90 analog data modem operation with V.44 data compression and supports 14.4 kbps fax modem operation. In addition, the modem supports remote telephone answering machine (TAM) and USB host interface operation. Table 1-1 lists the ordering information.

The modem operates with PSTN telephone lines worldwide. The modem is CDC-compliant and is supported by Microsoft CDC modem drivers.

Conexant's SmartDAA® technology (patent pending) eliminates the need for a costly analog transformer, relays, and opto-isolators typically used in discrete DAA (Data Access Arrangement) implementations The SmartDAA architecture also simplifies product implementation by eliminating the need for country-specific board configurations enabling worldwide homologation of a single modem board design and a single bill of materials (BOM).

The SmartDAA system-powered DAA operates reliably without drawing power from the line, unlike line-powered DAAs which operate poorly when line current is insufficient due to long lines or poor line conditions. Enhanced features, such as monitoring of local extension status without going off-hook, are also supported.

Incorporating Conexant's proprietary Digital Isolation Barrier (DIB) design (patent pending) and other innovative DAA features, the SmartDAA architecture simplifies application design, minimizes layout area, and reduces component cost.

The SmartV.90 USB Modem device set, consisting of a CX81801 Smart Modem in a 128-pin TQFP, a CX20493 SmartDAA LSD in a 28-pin QFN, and a CX11253 USB Interface Device (UID) in a 64-pin TQFP, supports data/fax/TAM operation with hardware-based modem controller, digital signal processing, and DAA/telephone line interface functions (Figure 1-1 and Figure 1-2).

The CX81801 Smart Modem integrates modem controller (MCU), modem data pump (MDP), 256 KB ROM, 32 KB RAM, and SmartDAA system side device (SSD) functions onto a single die.

Low profile, small TQFP packages and reduced voltage operation with low power consumption make this device set an ideal solution for embedded applications using USB host interface.

Table 1-1. SmartV.90 USB Modem Ordering Information

Model/Order/Part Numbers				
Marketing Name	**Device Set Order No.**	**Smart Modem [128-Pin TQFP] Part No.**	**Line Side Device (LSD) [28-Pin QFN] Part No.**	**USB Interface Device (UID) [64-Pin TQFP] Part No.**
SmartV.90 USB	DS56-L514-001	CX81801-34	CX20493-21	CX11253-11

Customized modem firmware is not necessary, but can be executed from optional external flash ROM memory. Additionally, added/modified country profiles can be executed from internal SRAM (maximum of one profile) or serial EEPROM.

The modem operates by executing firmware from internal ROM and RAM. Customized modem firmware and added/modified country profiles can be executed from internal SRAM or serial EEPROM. Additionally, if external firmware is used with optional external ROM/flash ROM, the firmware can be modified to support additional/modified country profiles.

In V.90 data mode, the modem can receive data at speeds up to 56 kbps from a digitally connected V.90-compatible central site modem. A V.90 modem takes advantage of the PSTN which is primarily digital except for the client modem to central office local loop and are ideal for applications such as remote access to an Internet Service Provider (ISP), on-line service, or corporate site. In this mode, the modem can transmit data at speeds up to V.34 rates.

In V.34 data mode, the modem operates at line speeds up to 33.6 kbps.

In V.32 bis data mode, the modem operates at lines speeds up to 14.4 kbps.

Data compression (V.44/V.42 bis/MNP 5) and error correction (V.42/MNP 2-4) modes are supported to maximize data throughput and data transfer integrity. V.44 is a more efficient data compression than V.42 bis that significantly increases downstream throughput thus reducing the download time for the types of files associated with Internet use, such as Web pages and uncompressed files such as graphics, image, audio, and document files. V.44 data compression can achieve compression rates of more than 25% over V.42bis. Typical compression ratio for V.44 on Web type data is approximately 6-1 resulting in overall effective data throughput rate up to 300 kbps for a 56 kbps-connection. Non-error-correcting mode is also supported.

In V.22 bis fast connect mode, the modem can connect at 2400 bps with a very short training time, which is very efficient for small data transfers.

Fax Group 3 send and receive rates are supported up to 14.4 kbps with T.30 protocol.

Downloadable architecture supports downloading of updated/upgraded or customized MCU firmware and MDP code modules from the host/DTE to the Smart Modem.

V.80 synchronous access mode supports host-controlled communication protocols, e. g., H.324 video conferencing.

In TAM mode, enhanced 2-bit or 4-bit per sample coding schemes at 8 kHz sample rate provide flexible format compatibility and allows efficient digital storage of voice/audio. Also supported are 8-bit linear and IMA 4-bit ADPCM coding. This mode supports applications such as digital telephone answering machine, voice annotation, and recording from and playback to the telephone line.

This data sheet describes the modem capabilities. Commands and parameters are defined in the Commands Reference Manual (Doc. No. 100722).

Figure 1-1. SmartV.90 USB Modem Simplified Interface Diagram

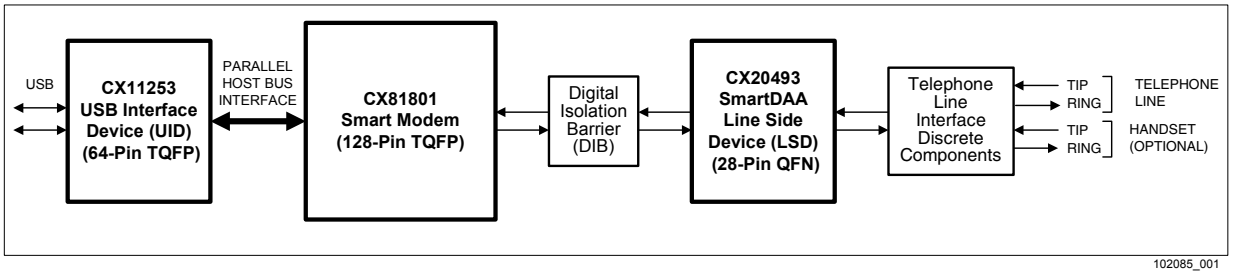
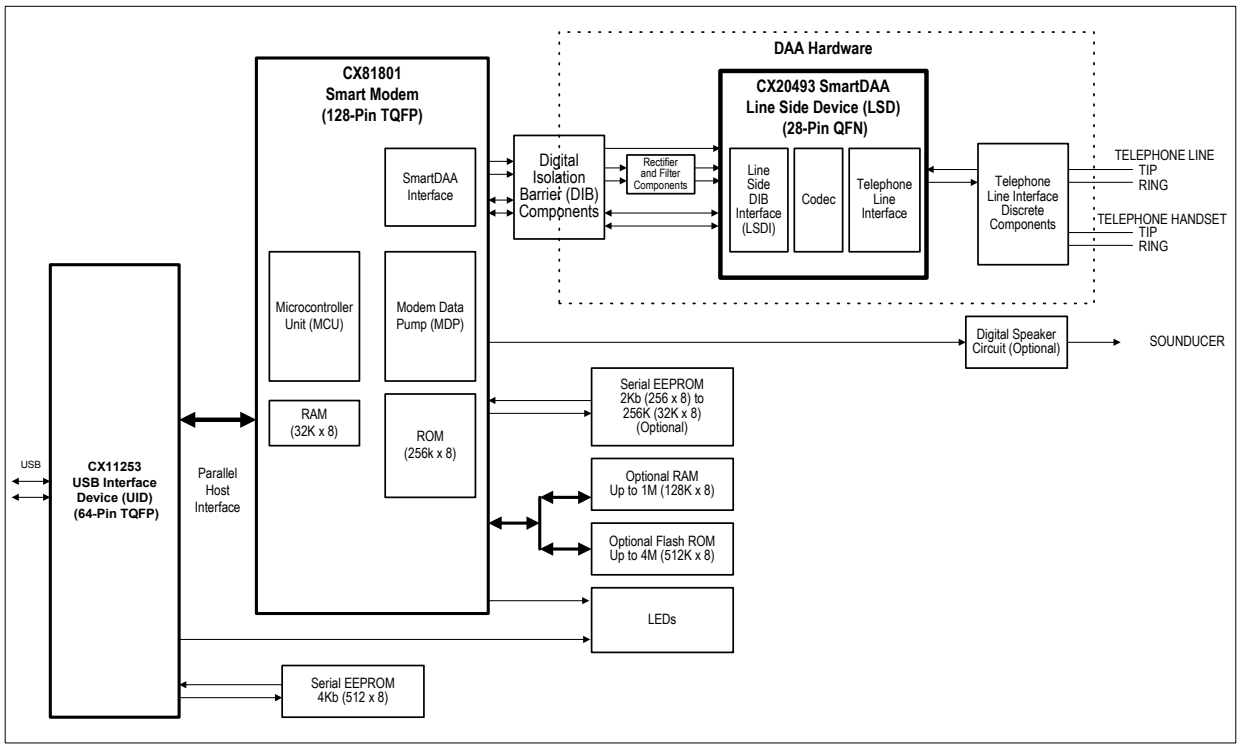


Figure 1-2. SmartV.90 USB Modem Major Interfaces



1.2 Features

1.2.1 General Modem Features

- Data modem
  - ITU-T V.90, V.34, V.32bis, V.32, V.22 bis, V.22, V.23, and V.21; Bell 212A and Bell 103
  - V.250 and V.251 commands
- V.22 bis fast connect
- Data compression and error correction
  - V.44 data compression
  - V.42 bis and MNP 5 data compression
  - V.42 LAPM and MNP 2-4 error correction
- Fax modem send and receive rates up to 14.4 kbps
  - V.17, V.29, V.27 ter, and V.21 channel 2
  - EIA/TIA 578 Class 1 and T.31 Class 1.0
- V.80 synchronous access mode supports host-controlled communication protocols with H.324 interface support
- Interfaces to optional external ROM/flash ROM, RAM, and/or optional serial EEPROM
- Downloadable Architecture
  - Downloadable MCU firmware from the host/DTE to flash ROM
  - Downloadable MDP code modules from the MCU transparent to the host
- Data/Fax/Voice call discrimination
- Hardware-based modem controller
- Hardware-based digital signal processor (DSP)
- Worldwide operation
  - Complies to TBR21 and other country requirements
  - Caller ID detection for many countries
  - Call progress, blacklisting
  - Internal ROM includes default values for 29 countries
  - Additional modified country profiles can be stored in internal SRAM or optional serial EEPROM
- On-hook Caller ID detection
- Distinctive ring detect
- Modem customization available through patch code that can be stored in optional serial EEPROM or internal SRAM
- Telephony/TAM
  - V.253 commands
  - 2-bit and 4-bit Conexant ADPCM, 8-bit linear PCM, and 4-bit IMA coding
  - 8 kHz sample rate
  - Concurrent DTMF, ring, and Caller ID detection

- Flow control and speed buffering
- Automatic format/speed sensing
- Asynchronous data
- CX11253 hardware
  - Full speed (12 MHz) USB interface device implementation
    - Suspend/Resume
    - Vendor specific descriptions
    - Bus powered USB device
  - LED driver outputs
  - +5V to +3.3V voltage regulators on-chip
- Single configuration profile stored in host
- System compatibility
  - Microsoft Windows 98SE, Windows ME, Windows 2000 and Windows XP operating systems
- Thin packages support low profile designs (1.6 mm max. height)
  - CX81801 Smart Modem in 128-pin TQFP
  - CX20493 LSD in 28-pin QFN
  - CX11253 UID in 64-pin TQFP
- +3.3V operation with +5V tolerant digital inputs
- Typical power use
  - 620 mW (Operating); 6 mW (Suspend)

1.2.2 SmartDAA Features

- System side powered DAA operates under poor line current supply conditions
- Modem Wake-on-Ring
- Ring detection
- Line polarity reversal detection
- Line current loss detection
- Pulse dialing
- Line-in-use detection during on-hook operation
- Remote hang-up detection for efficient call termination
- Extension pickup detection
- Call waiting detection
- Digital PBX line protection
- Meets worldwide DC VI masks requirements

1.2.3 Applications

- Embedded systems
- Gaming devices
- Remote monitoring and data collection systems
- Retail modems

1.3 Technical Overview

1.3.1 General Description

The SmartV.90 USB Device Set provides the processing core for a complete system design featuring data/fax modem, and remote TAM.

Modem operation, including dialing, call progress, telephone line interface, TAM interface, and host interface functions are supported and controlled through the V.250, V.251, and V.253-compatible command set.

The modem hardware connects to the host PC via a USB connection. The OEM adds a crystal circuit, serial EEPROM, telephone line interface, and other discrete components as required by the modem model, and a Microsoft CDC-compliant modem driver to complete the system.

The modem hardware connects to the host via a USB interface. The OEM adds a crystal circuit, DIB components, telephone line interface, telephone handset interface, optional external serial EEPROM, optional external ROM/flash ROM, optional external RAM, and other supporting discrete components as required by the application to complete the system.

Customized modem firmware can be supported by the use of external memory in various combinations, e.g., either external ROM/flash ROM (up to 256 KB), or external serial EEPROM (256 to 32 KB) and external RAM (up to 128 KB). To support country profile addition or modification, external serial EEPROM (256 to 32 KB) can be installed. Customized code can include OEM-defined commands, i.e., identification codes (I3), identifier string (I4), manufacturer identification (+GMI), model identification (+GMM), and revision identification (+GMR), as well as code modification.

1.3.2 MCU Firmware

MCU firmware performs processing of general modem control, command sets, data modem, error correction and data compression (ECC), fax class 1, fax class 1.0, voice/audio/TAM, worldwide, V.80, and USB host interface functions.

MCU firmware can be customized to include OEM-defined commands, i.e., identification codes (I3), identifier string (I4), manufacturer identification (+GMI), model identification (+GMM), and revision identification (+GMR), as well as code modification.

The modem firmware is provided in object code form for the OEM to program into external ROM/flash ROM. The modem firmware may also be provided in source code form under a source code addendum license agreement. External ROM/Flash ROM and RAM must be installed in order to operate the modem with customized firmware.

1.3.3 Operating Modes

1.3.3.1 Data/Fax Modes

In V.90 data modem mode, the modem can receive data from a digital source using a V.90-compatible central site modem at line speeds up to 56 kbps. Asymmetrical data transmission supports sending data at line speeds up to V.34 rates. This mode can fallback to full-duplex V.34 mode and to lower rates as dictated by line conditions.

In V.34 data modem mode, the modem can operate in 2-wire, full-duplex, asynchronous modes at line rates up to 33.6 kbps. Data modem modes perform complete handshake and data rate negotiations. Using V.34 modulation to optimize modem configuration for line conditions, the modem can connect at the highest data rate that the channel can support from 33600 bps down to 2400 bps with automatic fallback. Automode operation in V.34 is provided in accordance with PN3320 and in V.32 bis in accordance with PN2330. All tone and pattern detection functions required by the applicable ITU or Bell standards are supported.

In V.32 bis data modem mode, the modem can operate at line speeds up to 14.4 kbps.

In V.22 bis fast connect data mode, the modem can connect at 2400 bps with a very short training time, which is very efficient for small data transfers.

In fax modem mode, the modem can operate in 2-wire, half-duplex, synchronous modes and can support Group 3 facsimile send and receive speeds of 14400, 12000, 9600, 7200, 4800, and 2400 bps. Fax data transmission and reception performed by the modem are controlled and monitored through the EIA/TIA-578 Fax Class 1, or T.31 Fax Class 1.0 command interface. Full HDLC formatting, zero insertion/deletion, and CRC generation/checking are provided.

1.3.3.2 V.44 Data Compression

V.44 provides more efficient data compression than V.42 bis that significantly decreases the download time for the types of files associated with Internet use. This significant improvement is most noticeable when browsing and searching the web since HTML text files are highly compressible. (The improved performance amount varies both with the actual format and with the content of individual pages and files.)

1.3.3.3 Synchronous Access Mode (SAM) - Video Conferencing

V.80 Synchronous Access Mode between the modem and the host/DTE is provided for host-controlled communication protocols, e.g., H.324 video conferencing applications.

Voice-call-first (VCF) before switching to a videophone call is also supported.

1.3.3.4 Worldwide Operation

The modem operates in TBR21-compliant and other countries. Country-dependent modem parameters for functions such as dialing, carrier transmit level, calling tone, call progress tone detection, answer tone detection, blacklisting, caller ID, and relay control are programmable.

SmartDAA technology allows a single PCB design and single BOM to be homologated worldwide. Advanced features such as extension pickup detection, remote hang-up detection, line-in-use detection, and digital PBX detection are supported.

Country code IDs are defined by ITU-T T.35.

Internal ROM includes default profiles for 29 countries including TBR21-compliant profiles. Additional country profiles can be stored in internal SRAM or external serial EEPROM (request additional country profiles from a Conexant Sales Office). Duplicate country profiles stored in internal SRAM or external serial EEPROM will override the profiles in internal RAM firmware. The default countries supported are listed in Table 1-2.

Table 1-2. Default Countries Supported

Country	Country Code	Call Waiting Tone Detection (CW) Supported	On-Hook Type 1 Caller ID (CID) Supported	Off-Hook Type 2 Called ID (CID2) Supported
Australia	09	X		
Austria	0A	X	X	
Belgium	0F	X		
Brazil	16	X		
China	26	X	X	
Denmark	31	X	X	
Finland	3C	X	X	
France	3D	X	X	X
Germany	42	X	X	
Greece	46	X		
India	53		X	
Ireland	57			
Italy	59	X		
Japan	00	X	X	X
Korea	61	X		
Malaysia	6C	X		
Mexico	73			
Netherlands	7B			
Norway	82	X		
Poland	8A	X		
Portugal	8B	X		
Singapore	9C	X	X	X
South Africa	9F	X		
Spain	A0	X		
Sweden	A5	X		
Switzerland	A6	X		
Taiwan	FE	X	X	
United Kingdom	B4	X	X	X
United States	B5	X	X	X

1.3.3.5 TAM Mode

TAM Mode features include 8-bit linear coding at 8 kHz sample rate. Tone detection/ generation, call discrimination, and concurrent DTMF detection are also supported.

TAM Mode is supported by four submodes:

- Online Voice Command Mode supports connection to the telephone line.
- Voice Receive Mode supports recording voice or audio data input from the telephone line.
- Voice Transmit Mode supports playback of voice or audio data to the telephone line.
- Full-duplex Receive and Transmit Mode.

1.3.4 Reference Designs

Data/fax/TAM reference design for an external modem is available to minimize application design time, reduce development cost, and accelerate market entry. The part number for this design is: is design is: RD01-D690.

A design package is available in electronic form. This package includes schematics, bill of materials (BOM), vendor part list (VPL), board layout files in Gerber format, and complete documentation.

1.4 Hardware Description

SmartDAA™ technology (patent pending) eliminates the need for a costly analog transformer, relays, and opto-isolators that are typically used in discrete DAA implementations. The programmable SmartDAA architecture simplifies product implementation in worldwide markets by eliminating the need for country-specific components.

1.4.1 CX81801 Smart Modem

The CX81801 Smart Modem, packaged in a 128-pin TQFP, includes a Microcontroller (MCU), a Modem Data Pump (MDP), 256 KB internal ROM, 32 KB internal RAM, and SmartDAA interface functions.

The Smart Modem connects to the CX11253 host via a parallel bus interface.

The Smart Modem performs the command processing and host interface functions. The crystal frequency is 28.224 MHz.

The Smart Modem optionally connects to external OEM-supplied ROM/flash ROM and RAM over a non-multiplexed 19-bit address bus and 8-bit data bus.

The Smart Modem optionally connects to an external OEM-supplied serial EEPROM over a dedicated 2-line serial interface. The capacity of the EEPROM can be 256 bytes up to 32 KB. The EEPROM can hold information such as firmware configuration customization, country code parameters, and cellular drivers.

The Smart Modem performs telephone line signal modulation/demodulation in a hardware digital signal processor (DSP) which reduces computational load on the host processor.

The SmartDAA Interface communicates with, and supplies power and clock to, the LSD through the DIB.

1.4.2 Digital Isolation Barrier

The OEM-supplied Digital Isolation Barrier (DIB) electrically DC isolates the Smart Modem from the LSD and telephone line. The Smart Modem is connected to a fixed digital ground and operates with standard CMOS logic levels. The LSD is connected to a floating ground and can tolerate high voltage input (compatible with telephone line and typical surge requirements).

The DIB transformer couples power and clock from the Smart Modem to the LSD.

The DIB data channel supports bidirectional half-duplex serial transfer of data, control, and status information between the Smart Modem and the LSD over two lines.

1.4.3 CX20493 SmartDAA Line Side Device

The CX20493 SmartDAA Line Side Device (LSD) includes a Line Side DIB Interface (LSDI), a coder/decoder (codec), and a Telephone Line Interface (TLI).

The LSDI communicates with, and receives power and clock from, the SmartDAA interface in the Smart Modem through the DIB.

LSD power is received from the MDP PWRCLKP and PWRCLKN pins via the DIB through a half-wave rectifying diode and capacitive power filter circuit connected to the DIB transformer secondary winding.

The CLK input is also accepted from the DIB transformer secondary winding through a capacitor and a resistor in series.

Information is transferred between the LSD and the Smart Modem through the DIB_P and DIB_N pins. These pins connect to the Smart Modem DIB_DATAP and DIB_DATAN pins, respectively, through the DIB.

The TLI integrates DAA and direct telephone line interface functions and connects directly to the line TIP and RING pins, as well as to external line protection components.

Direct LSD connection to TIP and RING allows real-time measurement of telephone line parameters, such as the telephone central office (CO) battery voltage, individual telephone line (copper wire) resistance, and allows dynamic regulation of the off-hook TIP and RING voltage and total current drawn from the central office (CO). This allows the modem to maintain compliance with U.S. and worldwide regulations and to actively control the DAA power dissipation.

1.5 Commands

The modem supports data modem, fax class 1 or 1.0 modem, TAM, and V.80 commands, and S Registers in accordance with modem model options. See Doc. No. 100722 for a description of the commands.

Data Modem Operation. Data modem functions operate in response to the AT commands when +FCLASS=0. Default parameters support U.S./Canada operation.

Fax Modem Operation. Facsimile functions operate in response to fax class 1 commands when +FCLASS=1 or to fax class 1.0 commands when +FCLASS=1.0.

2. Technical Specifications

2.1 USB Interface Operation

See Section 5.

2.2 Establishing Data Modem Connections

2.2.1 Telephone Number Directory

The modem supports four telephone number entries in a directory that can be saved in an optional serial NVRAM. Each telephone number can be up to 32 characters (including the command line terminating carriage return) in length. A telephone number can be saved using the &Zn=x command, and a saved telephone number can be dialed using the DS=n command.

2.2.2 Dialing

DTMF Dialing. DTMF dialing using DTMF tone pairs is supported in accordance with ITU-T Q.23. The transmit tone level complies with Bell Publication 47001.

Pulse Dialing. Pulse dialing is supported in accordance with EIA/TIA-496-A.

Blind Dialing. The modem can blind dial in the absence of a dial tone if enabled by the X0, X1, or X3 command.

2.2.3 Modem Handshaking Protocol

If a tone is not detected within the time specified in the S7 register after the last digit is dialed, the modem aborts the call attempt.

2.2.4 Call Progress Tone Detection

Ringback, equipment busy, congested tone, warble tone, and progress tones can be detected in accordance with the applicable standard.

2.2.5 Answer Tone Detection

Answer tone can be detected over the frequency range of 2100 ± 40 Hz in ITU-T modes and 2225 ± 40 Hz in Bell modes.

2.2.6 Ring Detection

A ring signal can be detected from a TTL-compatible 15.3 Hz to 68 Hz square wave input.

2.2.7 Billing Protection

When the modem goes off-hook to answer an incoming call, both transmission and reception of data are prevented for 2 seconds (data modem) or 4 seconds (fax adaptive answer) to allow transmission of the billing tone signal.

2.2.8 Connection Speeds

The modem functions as a data modem when the +FCLASS=0 command is active.

Line connection can be selected using the +MS command. The +MS command selects modulation, enables/disables automode, and selects minimum and maximum line speeds (Table 2-1).

2.2.9 Automode

Automode detection can be enabled by the +MS command to allow the modem to connect to a remote modem in accordance with draft PN-3320 for V.34 (Table 2-1).

Table 2-1. +MS Command Automode Connectivity

<mod>	Modulation	Possible Rates (bps) [1]	Notes
V21	V.21	300	
V22	V.22	1200	
V22B	V.22 bis	2400 or 1200	
V23	V.23	1200	See Note 2
V32	V.32	9600 or 4800	
V32B	V.32 bis	14400, 12000, 9600, 7200, or 4800	
V34	V.34	33600, 31200, 28800, 26400, 24000, 21600, 19200, 16800, 14400, 12000, 9600, 7200, 4800, or 2400	
V90	V.90	56000, 54667, 53333, 52000, 50667, 49333, 48000, 46667, 45333, 44000, 42667, 41333, 40000, 38667, 37333, 36000, 34667, 33333, 32000, 30667, 29333, 28000	Default
B103	Bell 103	300	
B212	Bell 212	1200	

Notes:

1. See optional <automode>, <min_rate>, and <max_rate> subparameters for the +MS command.
2. For V.23, originating modes transmit at 75 bps and receive at 1200 bps; answering modes transmit at 1200 bps and receive at 75 bps. The rate is always specified as 1200 bps. V.23 half duplex is not supported.
3. If the DTE speed is set to less than the maximum supported DCE speed in automode, the maximum connection speed is limited to the DTE speed.

2.3 Data Mode

Data mode exists when a telephone line connection has been established between modems and all handshaking has been completed.

2.3.1 Speed Buffering (Normal Mode)

Speed buffering allows a DTE to send data to, and receive data from, a modem at a speed different than the line speed. The modem supports speed buffering at all line speeds.

2.3.2 Flow Control

DTE-to-Modem Flow Control. If the modem-to-line speed is less than the DTE-to-modem speed, the modem supports XOFF/XON or RTS/CTS flow control with the DTE to ensure data integrity.

2.3.3 Escape Sequence Detection

The +++ escape sequence can be used to return control to the command mode from the data mode. Escape sequence detection is disabled by an S2 Register value greater than 127.

2.3.4 BREAK Detection

The modem can detect a BREAK signal from either the DTE or the remote modem. The \Kn command determines the modem response to a received BREAK signal.

2.3.5 Telephone Line Monitoring

GSTN Cleardown (V.90, V.34, V.32 bis, V.32). Upon receiving GSTN Cleardown from the remote modem in a non-error correcting mode, the modem cleanly terminates the call.

Loss of Carrier (V.22 bis and Below). If carrier is lost for a time greater than specified by the S10 register, the modem disconnects (except MNP 10).

2.3.6 Fall Forward/Fallback (V.90/V.34/V.32 bis/V.32)

During initial handshake, the modem will fallback to the optimal line connection within V.90/V.34/V.32 bis/V.32 mode depending upon signal quality if automode is enabled by the +MS or N1 command.

When connected in V.90/V.34/V.32 bis/V.32 mode, the modem will fall forward or fallback to the optimal line speed within the current modulation depending upon signal quality if fall forward/fallback is enabled by the %E2 command.

2.3.7 Retrain

The modem may lose synchronization with the received line signal under poor or changing line conditions. If this occurs, retraining may be initiated to attempt recovery depending on the type of connection.

The modem initiates a retrain if line quality becomes unacceptable if enabled by the %E command. The modem continues to retrain until an acceptable connection is achieved, or until 30 seconds elapse resulting in line disconnect.

2.3.8 Programmable Inactivity Timer

The modem disconnects from the line if data is not sent or received for a specified length of time. In normal or error-correction mode, this inactivity timer is reset when data is received from either the DTE or from the line. This timer can be set to a value between 0 and 255 seconds by using register S30. A value of 0 disables the inactivity timer.

2.3.9 DTE Signal Monitoring (Serial DTE Interface Only)

DTR#. When DTR# is asserted, the modem responds in accordance with the &Dn and &Qn commands.

RTS#. RTS# is used for flow control if enabled by the &K command in normal or error-correction mode.

2.4 Error Correction and Data Compression

2.4.1 V.42 Error Correction

V.42 supports two methods of error correction: LAPM and, as a fallback, MNP 4. The modem provides a detection and negotiation technique for determining and establishing the best method of error correction between two modems.

2.4.2 MNP 2-4 Error Correction

MNP 2-4 is a data link protocol that uses error correction algorithms to ensure data integrity. Supporting stream mode, the modem sends data frames in varying lengths depending on the amount of time between characters coming from the DTE.

2.4.3 V.44 Data Compression

V.44 data compression encodes pages and files associated with Web pages more efficiently than V.42 bis. These files include WEB pages, graphics and image files, and document files. V.44 can provide an effective data throughput rate up to DTE rate for a 56-kbps connection. The improved performance amount varies both with the actual format and with the content of individual pages and files.

2.4.4 V.42 bis Data Compression

V.42 bis data compression mode, enabled by the %Cn command or S46 register, operates when a LAPM or MNP 10 connection is established.

The V.42 bis data compression employs a “string learning” algorithm in which a string of characters from the DTE is encoded as a fixed length codeword. Two 2-KB dictionaries are used to store the strings. These dictionaries are dynamically updated during normal operation.

2.4.5 MNP 5 Data Compression

MNP 5 data compression mode, enabled by the %Cn command, operates during an MNP connection.

In MNP 5, the modem increases its throughput by compressing data into tokens before transmitting it to the remote modem, and by decompressing encoded received data before sending it to the DTE.

2.5 Telephony Extensions

The following telephony extension features are supported and can be typically be implemented in designs for set-top box applications and TAM software applications to enhance end-user experience:

- Line In Use detection
- Extension Pickup detection
- Remote Hang-up detection

2.5.1 Line In Use Detection

The Line In Use Detection feature can stop the modem from disturbing the phone line when the line is already being used. When an automated system tries to dial using ATDT and the phone line is in use, the modem will not go off hook and will respond with the message “LINE IN USE”.

2.5.2 Extension Pickup Detection

The Extension Pickup Detection feature (also commonly referred as PPD or Parallel phone detection) allows the modem to detect when another telephony device (i.e., fax machine, phone, satellite/cable box) is attempting to use the phone line.

This feature can be used to quickly drop a modem connection in the event when a user picks up an extension phone line. For example, this feature allows set top boxes with an integrated SmartV.90 USB modem to give normal voice users the highest priority over the telephone line.

This feature can also be used in Telephone Answering Machine applications (TAM). Its main use would be to stop the TAM operation when a phone is picked up.

2.5.3 Remote Hangup Detection

The Remote Hangup Detection feature will cause the modem go back onhook during a data connection when the remote modem is disconnected for abnormal termination reasons (remote phone line unplugged, remote server/modem shutdown. For Voice applications, this method can be used in addition to silence detection to determine when a remote caller has hung up to terminate a voice recording.

2.6 Fax Class 1 and Fax Class 1.0 Operation

Facsimile functions operate in response to fax class 1 commands when +FCLASS=1 or to fax class 1.0 commands when +FCLASS=1.0.

In the fax mode, the on-line behavior of the modem is different from the data (non-fax) mode. After dialing, modem operation is controlled by fax commands. Some AT commands are still valid but may operate differently than in data modem mode.

Calling tone is generated in accordance with T.30.

2.7 Caller ID

Type I Caller ID (On-Hook Caller ID) is supported for U.S. and many other countries (see Section 2.8). Caller ID is enabled/disabled using the +VCID command. When enabled, caller ID information (date, time, caller code, and name) can be passed to the DTE in formatted or unformatted form. Inquiry support allows the current caller ID mode and mode capabilities of the modem to be retrieved from the modem.

2.8 Worldwide Country Support

Internal modem firmware supports 29 country profiles (see Section 1.3.2). These country profiles include the following country-dependent parameters:

- Dial tone detection levels and frequency ranges.
- DTMF dialing parameters: Transmit output level, DTMF signal duration, and DTMF interdigit interval.
- Pulse dialing parameters: Make/break times, set/clear times, and dial codes are programmable
- Ring detection frequency range.
- Type I Caller ID is supported for many countries. Consult firmware release notes for a list of the supported countries and the criteria for additional country support.
- Blind dialing enabled/disable.
- Carrier transmit level (through S91 for data and S92 for fax). The maximum, minimum, and default values can be defined to match specific country and DAA requirements.
- Calling tone is generated in accordance with V.25. Calling tone may be toggled (enabled/disabled) by inclusion of a “^” character in a dial string. It may also be disabled.
- Frequency and cadence of tones for busy, ringback, congested, warble, dial tone 1, and dial tone 2.
- Answer tone detection period.
- Blacklist parameters. The modem can operate in accordance with requirements of individual countries to prevent misuse of the network by limiting repeated calls to the same number when previous call attempts have failed. Call failure can be detected for reasons such as no dial tone, number busy, no answer, no ringback detected, voice (rather than modem) detected, and key abort (dial attempt aborted by user). Actions resulting from such failures can include specification of minimum inter-call delay, extended delay between calls, and maximum numbers of retries before the number is permanently forbidden ("blacklisted").

These country profiles may be altered or customized by modifying the country-dependent parameters. Additional profiles may also be included. There are two ways to add or modify profiles:

- Incorporating additional or modified profiles into external flash ROM containing the entire modem firmware code.
- Linking additional or modified profiles from an external serial EEPROM (needed only if the external flash ROM capacity is exceeded).

Please contact an FAE at the local Conexant sales office if a country code customization is required.

2.9 Diagnostics

2.9.1 Commanded Tests

Diagnostics are performed in response to &T commands.

Analog Loopback (&T1 Command). Data from the local DTE is sent to the modem, which loops the data back to the local DTE.

2.9.2 Power On Reset Tests

Upon power on, the modem performs tests of the modem, internal and external RAM, and NVRAM. If the modem, internal RAM, or external RAM test fails, the TMIND# output is pulsed (serial interface version) or the DCD bit in the parallel interface register is pulsed (parallel interface version) as follows:

- Internal or external RAM test fails: One pulse cycle (pulse cycle = 0.5 sec. on, 0.5 sec. off) every 1.5 seconds.
- Modem device test fails: Three pulse cycles every 1.5 seconds.

If the NVRAM test fails (due to NVRAM failure or if NVRAM is not installed), the test failure is reported by AT commands that normally use the NVRAM, e.g., the &V command.

2.10 Low Power Sleep Mode

Sleep Mode Entry. The modem enters the low power sleep mode when no line connection exists and no host activity occurs for the period of time specified in the S24 register. All modem circuits are turned off except the internal clock circuitry in order to consume reduced power while being able to immediately wake up and resume normal operation.

Wake-up. Wake-up occurs when a ring is detected on the telephone line, the host writes to the modem (parallel interface), or the DTE sends a character to the modem (serial interface).

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3. Hardware Interface

3.1 CX11253 UID Hardware Pins and Signals

3.1.1 General

3.1.1.1 USB Interface

Differential data plus and data minus signals (DP and DM) interface to the USB port.

3.1.1.2 LED Interface

Dedicated LED output signals are provided for Power status, Carrier Detect status, and Transmit/Receive Data status. The Off-Hook relay control signal can also be used for Off-Hook LED status.

3.1.1.3 Serial EEPROM Interface

A serial EEPROM is required to store the USB device, configuration, interface, and endpoint descriptors. Device descriptors include Vendor ID, Product ID, Device Release Number, Manufacturer Name, Product Name, and Serial Number.

Connection to an Atmel AT24C04N-10-2.7 or equivalent is supported.

3.1.2 CX11253 UID Signal Interface, Pin Assignments, and Signal Definitions

CX11253 UID hardware interface signals are shown by major interface in Figure 3-1,.

CX11253 UID 64-pin TQFP pin signals are shown in Figure 3-2, and are listed in Table 3-1.

CX11253 UID hardware interface signals are defined in Table 3-2.

CX11253 UID input/output descriptors are defined in Table 3-3.

CX11253 UID DC electrical characteristics are listed Table 3-4.

Figure 3-1. CX11253 UID 64-Pin TQFP Hardware Signals

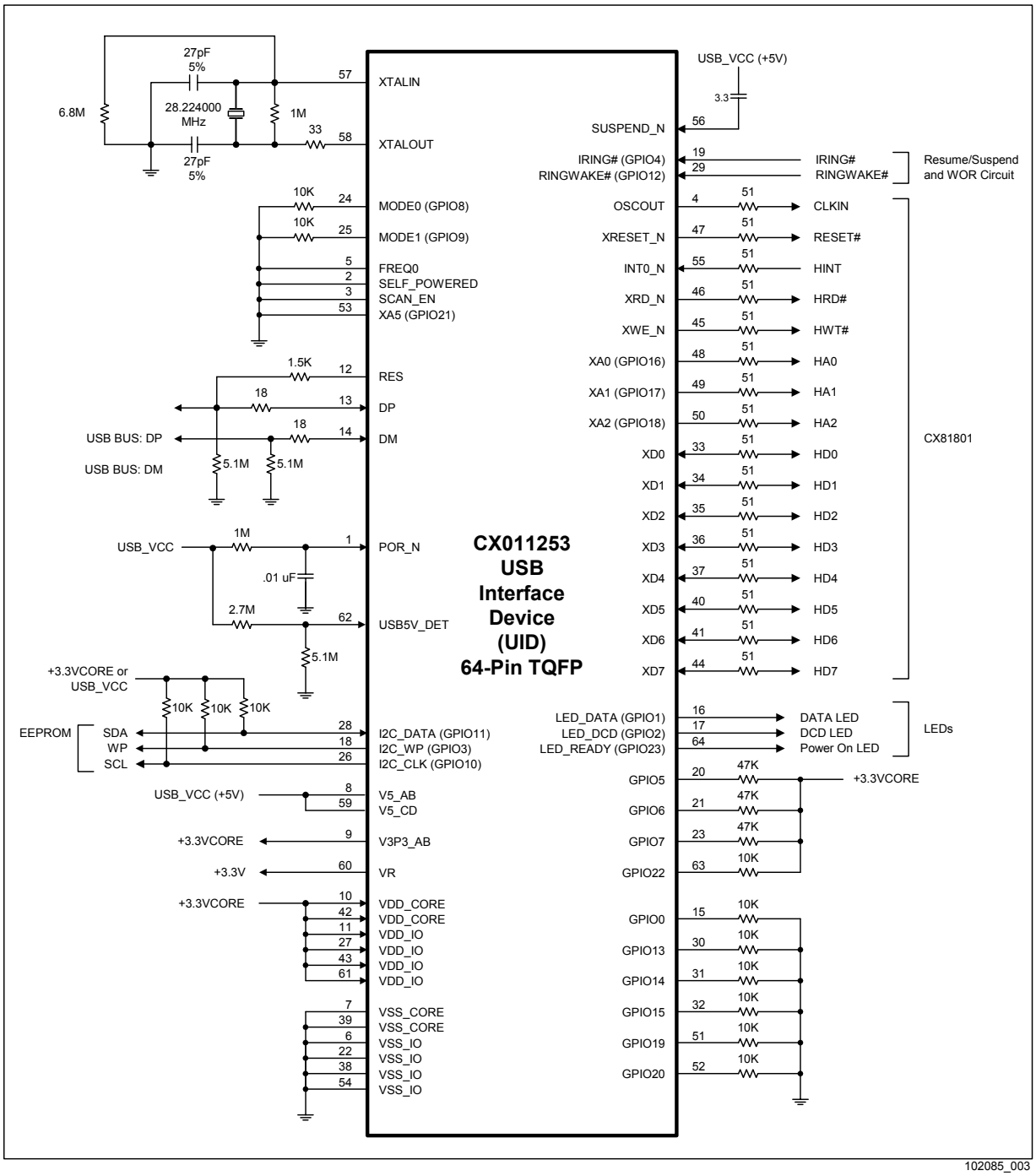

Figure 3-2. CX11253 UID 64-Pin TQFP Pin Signals

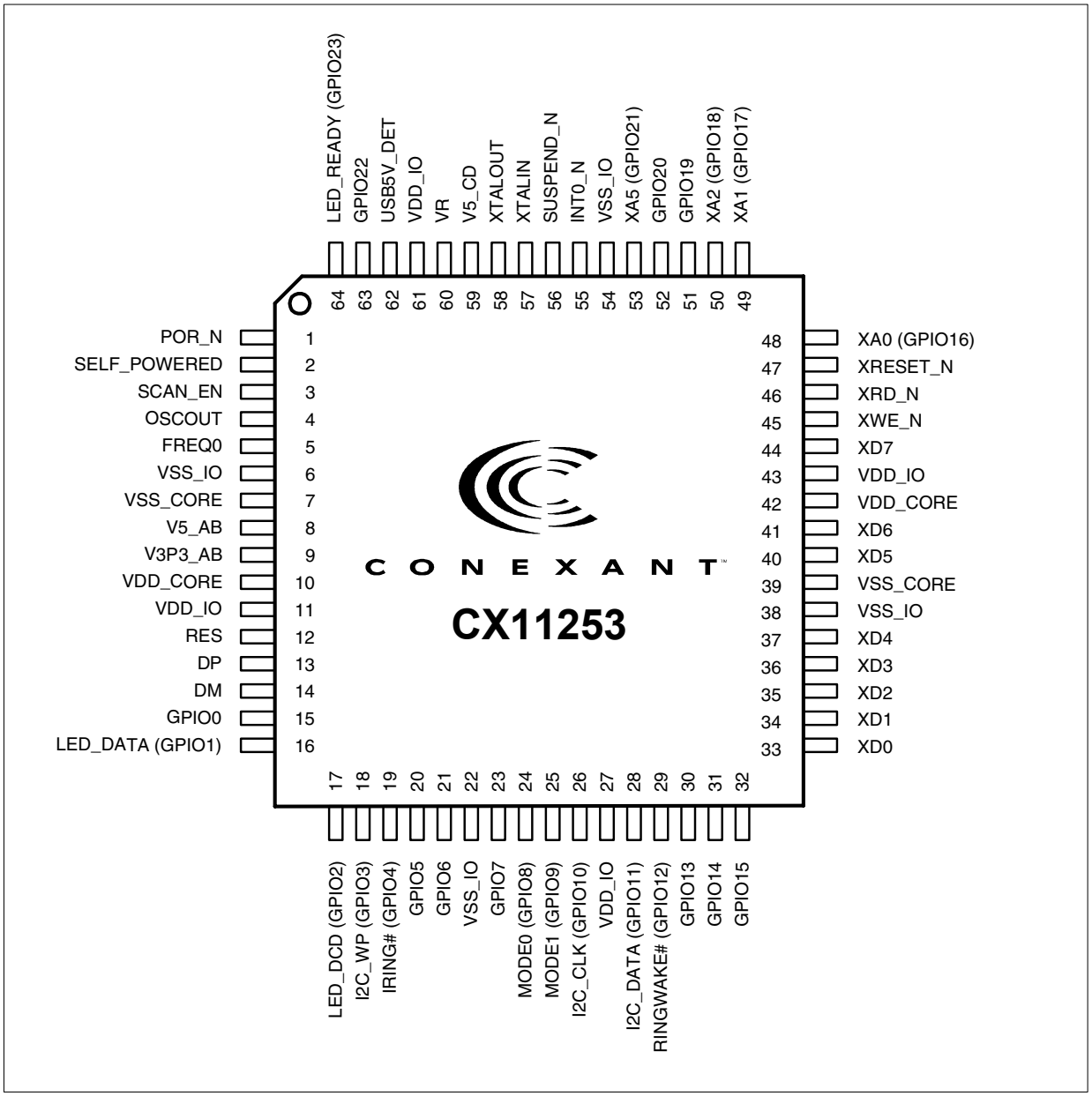

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Table 3-1. CX11253 UID 64-Pin TQFP Pin Signals

Pin	Signal	Pin	Signal
1	POR_N	33	XD0
2	SELF_POWERED	34	XD1
3	SCAN_EN	35	XD2
4	OSCOUT	36	XD3
5	FREQ0	37	XD4
6	VSS_IO	38	VSS_IO
7	VSS_CORE	39	VSS_CORE
8	V5_AB	40	XD5
9	V3P3_AB	41	XD6
10	VDD_CORE	42	VDD_CORE
11	VDD_IO	43	VDD_IO
12	RES	44	XD7
13	DP	45	XWE_N
14	DM	46	XRD_N
15	GPIO0	47	XRESET_N
16	LED_DATA (GPIO1)	48	XA0 (GPIO16)
17	LED_DCD (GPIO2)	49	XA1 (GPIO17)
18	I2C_WP (GPIO3)	50	XA2 (GPIO18)
19	IRING# (GPIO4)	51	GPIO19
20	GPIO5	52	GPIO20
21	GPIO6	53	XA5 (GPIO21)
22	VSS_IO	54	VSS_IO
23	GPIO7	55	INT0_N
24	MODE0 (GPIO8)	56	SUSPEND_N
25	MODE1 (GPIO9)	57	XTALIN
26	I2C_CLK (GPIO10)	58	XTALOUT
27	VDD_IO	59	V5_CD
28	I2C_DATA (GPIO11)	60	VR
29	RINGWAKE# (GPIO12)	61	VDD_IO
30	GPIO13	62	USB5V_DET
31	GPIO14	63	GPIO22
32	GPIO15	64	LED_READY (GPIO23)

Table 3-2. CX11253 UID Pin Signal Definitions

Label	Pin No.	I/O	I/O Type	Signal Name/Description
System				
XTALIN XTALOUT	57 58	I O	Ix Ox	**UID Crystal/Clock In and Crystal Out.** Connect XTALIN and XTALOUT to an external 28.224 MHz crystal circuit.
OSCOUT	4	O	Ot	**Clock Out.** 28.224 MHz output clock. Connect to CX81801 CLKIN pin through 51 Ω
POR_N	1	I	Itst	**Reset.** The active low POR_N input resets all internal machines and registers in the UID and DSP. Connect to USB_VCC through 1 MΩ and to GND through 0.01 μF.
MODE0 (GPIO8)	24	I	It/Ot12	**Mode Select 0.** Connect to GND through 10 KΩ.
MODE1 (GPIO9)	25	I	It/Ot12	**Mode Select 1.** Connect to GND through 10 KΩ.
FREQ0	5	I	It	**Frequency Select.** Connect to GND for 28.224 MHz operation.
SELF_POWERED	2	I	It	**Power Mode Select**. Selects self-powered (high) or externally powered (low). Connect to GND.
SCAN_MODE	3	I	Itpd	**Scan Mode.** Connect to GND.
XA5 (GPIO21)	53	O	Ot2	**Not Used.** Connect to GND.
SUSPEND_N	56	I	It	**Clock Startup Control.** Connect to USB_VCC through 3.3 μF.
USB Interface				
DP DM	13 14	I/O I/O	Iua/Oua Iua/Oua	**USB Port**. DP and DM are the differential data plus and data minus signals of the USB port, the upstream differential port. These lines do not have internal pullup resistors. Connect DP and DM to USB_DATAP and USB_DATAM, respectively, through 18 Ω. Connect USB_DM to GND through a 5.1 MΩ resistor. Connect USB_DM to GND through a 5.1 MΩ resistor.
RES	12	I	It	**Reset.** Connect to USB_DATAP through 1.5 KΩ.
USB5 V_DET	62	I	It	**USB 5 V Detect.** Detects +5 V on the USB_+5 pin. Connect to the USB_VCC pin through 2.7 MΩ and to GND through 5.1 MΩ.
Power and Ground				
V5_AB	8	P	PWR	**+5V Input Power to Voltage Regulator V3P3_AB**. Connect to +5V.
V5_CD	59	P	PWR	**+5V Input Power to Voltage Regulator VR.** Connect to +5V.
V3P3_AB	9	P	PWR	**+3.3V Output Power from Voltage Regulator V3P3_AB**. Connect to UID: VDD pins through +3.3VCORE capacitive filter.
VR	60	P	PWR	**+3.3V Output Power from Voltage Regulator VR**. Connect to UID: DVDD pins through +3.3V capacitive filter.
VDD_CORE	10, 42	P	PWR	**+3.3V Supply Voltage for Core Digital Circuits**. Connect to UID: V3P3_AB pin through +3.3VCORE capacitive filter.
VDD_IO	11, 27, 43, 61	P	PWR	**+3.3V Supply Voltage for I/O Digital Circuits**. Connect to UID: V3P3_AB pin through +3.3VCORE capacitive filter.
VSS_CORE	7, 39	G	GND	**Digital Ground for Core Circuits.** Connect to digital ground.
VSS_IO	6, 22, 38, 54	G	GND	**Digital Ground for I/O Circuits.** Connect to digital ground.
Serial EEPROM Interface				
I2C_WP (GPIO3)	18	O	It/Ot12	**Serial EEPROM Write Pulse**. Connect to serial EEPROM: WP and to +3.3VCORE or USB_VCC through 10K Ω.
I2C_CLK (GPIO10)	26	O	It/Ot12	**Serial EEPROM Shift Clock**. Connect to serial EEPROM: SCL and to +3.3VCORE or USB_VCC through 10K Ω.
I2C_DATA (GPIO11)	28	I/O	It/Ot12	**Serial EEPROM Bidirectional Data.** Connect to EEPROM: SDA and to +3.3VCORE or USB_VCC through 10K Ω.

Table 3-2. CX11253 UID Pin Signal Definitions (Continued)

Label	Pin No.	I/O	I/O Type	Signal Name/Description
Suspend/Resume and Wake-on-Ring Circuit Interface				
IRING# (GPIO4)	19	I	It/Ot12	**Ring Indicate.** A low-going edge used to initiate presence of a ring frequency on the telephone line. Typically connected to the output of an optoisolator or equivalent. The idle state (no ringing) output of the ring detect circuit should be high. Connect to Suspend/Resume and Wake-on-Ring circuit
RINGWAKE# (GPIO12)	29	I	It/Ot12	**Ring Wakeup.** Active low input that indicates that a ring has been detected to wake up the UID from suspend mode. Connect to Suspend/Resume and Wake-on-Ring circuit.
CX81801 Interface				
INT0_N	55	I	Itpd	**Interrupt.** Connect to CX81810 HINT pin through 51 Ω.
XRESET_N	47	O	Otpd2	**Reset Output.** Active low output. Connect to CX81801 RESET# pin through 51 Ω.
XRD_N	46	O	Otpd2	**Read Enable.** Connect to CX81810 HRD# pin through 51 Ω.
XWE_N	45	O	Otpd2	**Write Enable.** Connect to CX81810 HWT# pin through 51 Ω.
XA2 (GPIO18) XA1 (GPIO17) XA0 (GPIO16)	50 49 48	O	Otpd2	**Address Output Lines 2-0.** Connect XA[2:0] to CX81810 HA[2:0], respectively, each line through 51 Ω.
XD[7:0]	44, 41-40, 37-33	I/O	Itpd/Ot2	**Bidirectional Data Lines 7-0.** Connect XD[7:0] to CX81810 HD[7:0], respectively, each line through 51 Ω.
LED Interface				
LED_DATA (GPIO1)	16	O	It/Ot12	**Transmit/Receive Data.** Active high output used to drive the Transmit/Receive Data LED indicator. LED_DATA (GPIO1) output ON (high) corresponds to the indicator on.
LED_DCD (GPIO2)	17	O	It/Ot12	**Carrier Detect Status.** Active high output used to drive the Carrier Detect LED indicator. LED_DCD (GPIO2) output ON (high) corresponds to the indicator on.
LED_READY (GPIO23)	64	O	It/Ot12	**Power On Status.** Active high output used to drive the Power On LED indicator. LED_READY (GPIO23) output ON (high) corresponds to the indicator on.
Not Used				
GPIO5	20	I/O	It/Ot12	**GPIO5.** Connect to +3.3VCORE through 47 KΩ.
GPIO6	21	I/O	It/Ot12	**GPIO6.** Connect to +3.3VCORE through 47 KΩ.
GPIO7	23	I/O	It/Ot12	**GPIO7.** Connect to +3.3VCORE through 47 KΩ.
GPIO22	63	I/O	It/Ot12	**GPIO22.** Connect to +3.3VCORE through 10 KΩ.
GPIO0	15	I/O	It/Ot12	**GPIO0.** Connect to ground through 10 KΩ.
GPIO13	30	I/O	It/Ot12	**GPIO13.** Connect to ground through 10 KΩ.
GPIO14	31	I/O	It/Ot12	**GPIO14.** Connect to ground through 10 KΩ.
GPIO15	32	I/O	It/Ot12	**GPIO15.** Connect to ground through 10 KΩ.
GPIO19	51	I/O	It/Ot12	**GPIO19.** Connect to ground through 10 KΩ.
GPIO20	52	I/O	It/Ot12	**GPIO20.** Connect to ground through 10 KΩ.

Table 3-3. CX11253 UID Input/Output Type Descriptions

Type	Description
It	Digital input, TTL compatible.
Itpd	Digital input, TTL compatible, internal 50 KΩ (typical) pull-down resistor to ground. If not externally driven, the input assumes a low state.
Itpu	Digital input, TTL compatible, internal 50 KΩ (typical) pull-up resistor to VDD. If not externally driven, the input assumes a high state.
Itst	Digital input, TTL compatible, Schmitt trigger.
Ot2	Digital output, TTL compatible, 2 mA.
Ot12	Digital output, TTL compatible, 12 mA.
Otod2	Digital output, TTL compatible, open drain, 2 mA.
Otod12	Digital output, TTL compatible, open drain, 12 mA.
NC	No external connection allowed (pin may be connected to internal circuitry).
USB	Analog input/output, USB driver and receiver.
Notes: See electrical characteristics in Table 3-4. TTL compatible inputs will accept a voltage of ≥ 2.0 volts as a logic one level and a voltage of ≤ 0.8 volts as a logic zero level.	

Table 3-4. CX11253 UID DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input High Voltage	V_{IH}	2.0	–	VDD + 0.3	VDC	
Input Low Voltage	V_{IL}	–0.3	–	0.8	VDC	
Input High Current	I_{IH}			40	µA	V_{IN} = 5.25V, V_{CC} = 5.25V,
Input Low Current	I_{IL}			400	µA	V_{CC} = 5.25V
Input Leakage Current	I_{IN}	–	–	±2.5	µADC	V_{IN} = 0.8V to (VDD-1V)
Output High Voltage	V_{OH}	2.4	–	–	VDC	I_{LOAD} = – 100 µA
Output Low Voltage	V_{OL}	–	–	0.4	VDC	I_{LOAD} = See Table 3-3.
Notes: Test Conditions: V5_AB and V5_CD = 5V ± 5%, TA = 0°C to 70°C, (unless otherwise stated).						

3.2 CX81801 Smart Modem Hardware Pins and Signals

3.2.1 General

3.2.1.1 LSD Interface (Through DIB)

The DIB interface signals are:

- Clock and Power Positive (PWRCLKP); output
- Clock and Power Negative (PWRCLKN); output
- Data Positive (DIB_DATAP); input/output
- Data Negative (DIB_DATAN); input/output

3.2.1.2 Call Progress Speaker Interface

The call progress speaker interface signal is:

- Digital speaker output (DSPKOUT); output

DSPKOUT is a square wave output in Data/Fax mode used for call progress or carrier monitoring. This output can be optionally connected to a low-cost on-board speaker, e.g., a sounducer, or to an analog speaker circuit.

3.2.1.3 Serial EEPROM Interface

A 2-line serial interface to an optional serial EEPROM is supported. The interface signals are:

- Bidirectional Data input/output (NVMDATA)
- Clock output (NVMCLK)

The EEPROM can hold information such as firmware customization and country code parameters. Data stored in EEPROM takes precedence over the factory default settings. Note: This information is usually stored in flash ROM; serial EEPROM is required only if storage is required for more than 31 country profiles.

The EEPROM size can range from 2 Kb (256 bits x 8) to 256 Kb (32Kb x 8). A 2-Kb EEPROM must be 100 kHz or 400 kHz; higher capacity EEPROMs must be 400 kHz.

3.2.1.4 External Bus Interface

The external bus optionally connects to OEM-supplied external memory:

- Up to 4 Mb (512K x 8) ROM/flash ROM
- Up to 1 Mb (128K x 8) RAM

The non-multiplexed external bus interface signals are:

- Eight bidirectional Data lines (D0-D7)
- 19 Address output lines (A0-A18)
- Read Enable output (READ#)
- Write Enable output (WRITE#)
- ROM Chip Select output (ROMSEL#)
- RAM Chip Select output (RAMSEL#)

3.2.2 Parallel Host Bus Interface

The parallel host interface signals are:

- Host Reset control input line (RESET#)
- Host Chip Select control input (HCS#)
- Host Read control input (HRD#) and Host Write control input (HWT#)
- Host Interrupt output line (HINT)
- Three Host Address input lines (HA0-HA2)
- Eight Host Data lines (HD0-HD7)

3.2.3 CX81801 Signal Interface, Pin Assignments, and Signal Definitions

CX81801 Smart Modem 128-pin TQFP hardware interface signals for parallel interface are shown by major interface in Figure 3-3, are shown by pin number in Figure 3-4, and are listed by pin number in Table 3-5. The Smart Modem hardware interface signals for parallel interface are defined in Table 3-6.

I/O types are defined in Table 3-7.

DC electrical characteristics are listed in Table 3-8.

Figure 3-3. CX81801 Smart Modem Hardware Signals

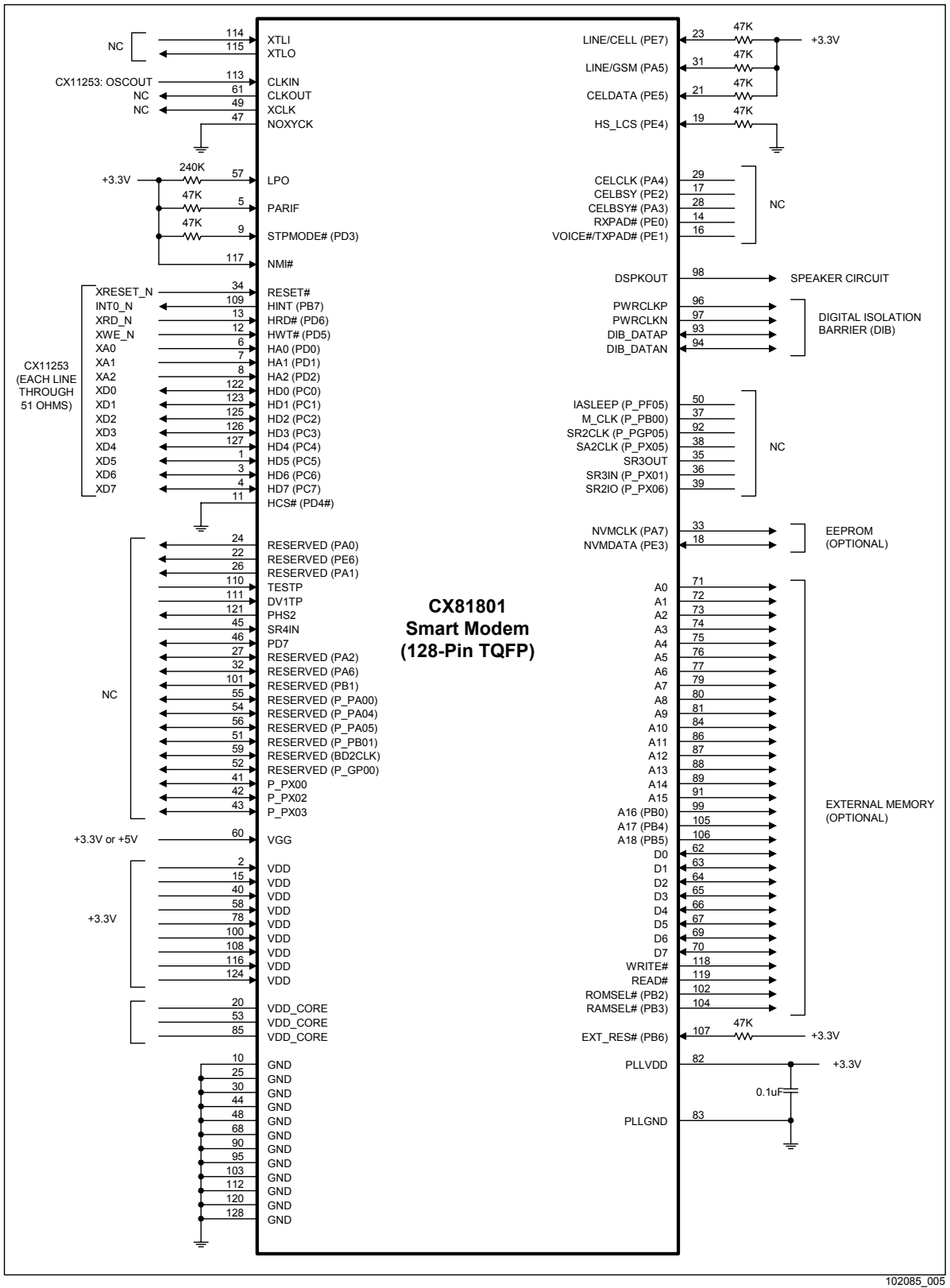

Figure 3-4. CX81801 Smart Modem 128-Pin TQFP Pin Signals

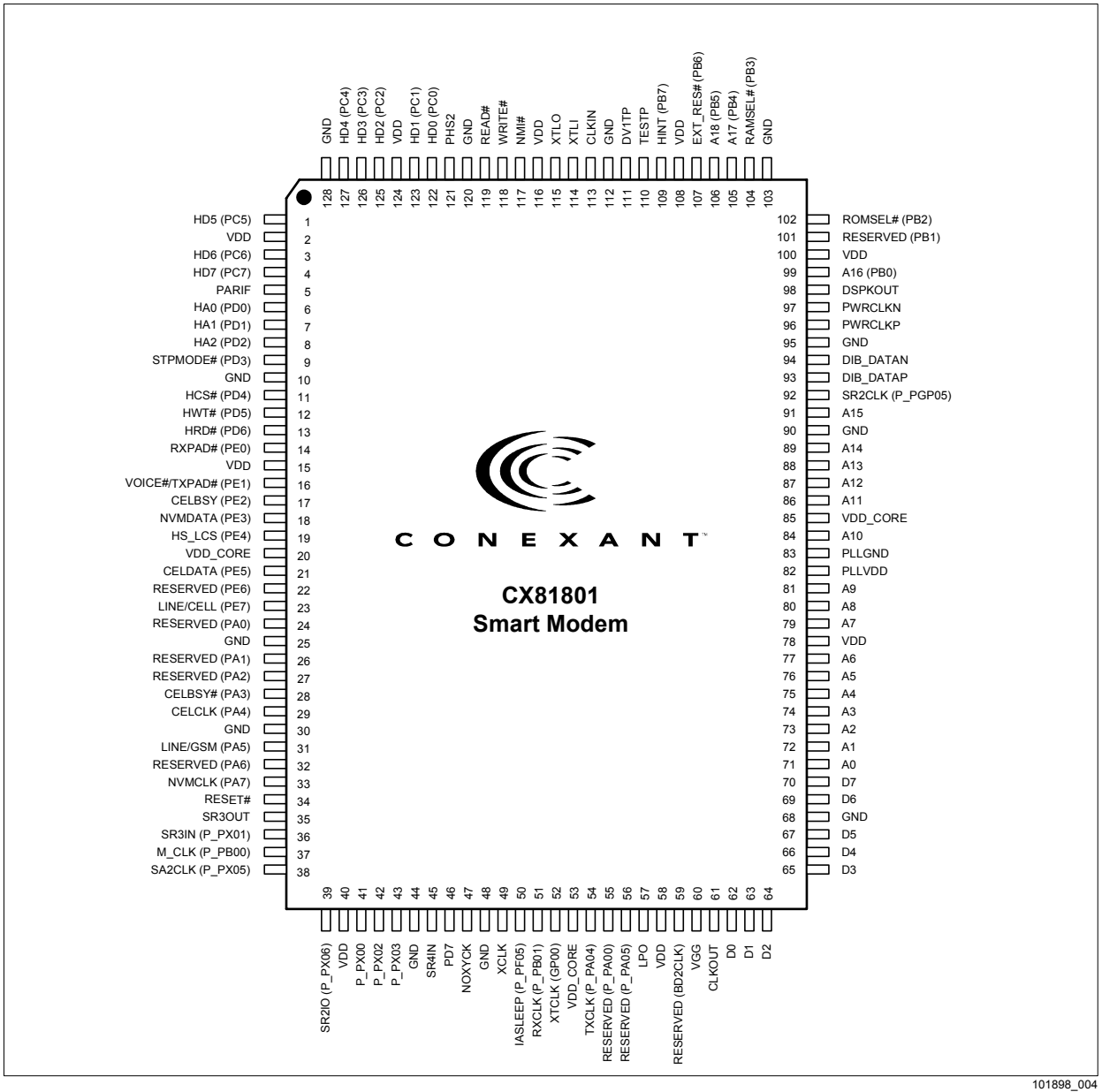

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Table 3-5. CX81801 Smart Modem 128-Pin TQFP Pin Signals

Pin	Signal Label	Pin	Signal Label
1	HD5 (PC5)	65	D3
2	VDD	66	D4
3	HD6 (PC6)	67	D5
4	HD7 (PC7)	68	GND
5	PARIF	69	D6
6	HA0 (PD0)	70	D7
7	HA1 (PD1)	71	A0
8	HA2 (PD2)	72	A1
9	STPMODE# (PD3)	73	A2
10	GND	74	A3
11	HCS# (PD4)	75	A4
12	HWT# (PD5)	76	A5
13	HRD# (PD6)	77	A6
14	RXPAD# (PE0)	78	VDD
15	VDD	79	A7
16	VOICE#/TXPAD# (PE1)	80	A8
17	CELBSY (PE2)	81	A9
18	NVMDATA (PE3)	82	PLLVDD
19	HS_LCS (PE4)	83	PLLGND
20	VDD_CORE	84	A10
21	CELDATA (PE5)	85	VDD_CORE
22	SSD_RING# (PE6)	86	A11
23	LINE/CELL (PE7)	87	A12
24	RESERVED (PA0)	88	A13
25	GND	89	A14
26	SSD_INT (PA1)	90	GND
27	PA2	91	A15
28	CELBSY# (PA3)	92	SR2CLK (P_PGP05)
29	CELCLK (PA4)	93	DIB_DATAP
30	GND	94	DIB_DATAN
31	LINE/GSM (PA5)	95	GND
32	PA6	96	PWRCLKP
33	NVMCLK (PA7)	97	PWRCLKN
34	RESET#	98	DSPKOUT
35	SR3OUT	99	A16 (PB0)
36	SR3IN (P_PX01)	100	VDD
37	M_CLK (P_PB00)	101	RESERVED (PB1)
38	SA2CLK (P_PX05)	102	ROMSEL# (PB2)
39	SR2IO (P_PX06)	103	GND
40	VDD	104	RAMSEL# (PB3)
41	P_PX00	105	A17 (PB4)
42	P_PX02	106	A18 (PB5)
43	P_PX03	107	EXT_RES# (PB6)
44	GND	108	VDD
45	SR4IN	109	HINT (PB7)
46	PD7	110	TESTP
47	NOXYCK	111	DV1TP
48	GND	112	GND
49	XCLK	113	CLKIN
50	IASLEEP (P_PF05)	114	XTLI

Table 3-5. CX81801 Smart Modem 128-Pin TQFP Pin Signals (Continued)

Pin	Signal Label	Pin	Signal Label
51	RESERVED (P_PB01)	115	XTLO
52	RESERVED (GP00)	116	VDD
53	VDD_CORE	117	NMI#
54	RESERVED (P_PA04)	118	WRITE#
55	RESERVED (P_PA00)	119	READ#
56	RESERVED (P_PA05)	120	GND
57	LPO	121	PHS2
58	VDD	122	HD0 (PC0)
59	RESERVED (BD2CLK)	123	HD1 (PC1)
60	VGG	124	VDD
61	CLKOUT	125	HD2 (PC2)
62	D0	126	HD3 (PC3)
63	D1	127	HD4 (PC4)
64	D2	128	GND

Table 3-6. CX81801 Smart Modem Pin Signal Definitions

Label	Pin	I/O	I/O Type	Signal Name/Description
System				
XTLI, XTLO	114, 115	I, O	Ix, Ox	**Crystal In and Crystal Out.** If an external 28.224 MHz crystal circuit is used instead of an external clock circuit, connect XTLI and XTLO to the external crystal circuit and leave CLKIN open. Typically, leave open and use CLKIN.
CLKIN	113	I	It	**Clock In.** If this external 28.224 MHz clock input is used instead of an external crystal circuit, connect CLKIN to the CX11253 OSCOUT pin through 51 Ω clock output and leave XTLI and XTLO open (recommended).
CLKOUT	61	O	It/Ot2	**Clock Out.** 28.224 MHz output clock. Leave open.
PARIF	5	I	Itpu	**Parallel/Serial Interface Select.** Connect to +3.3 V through 47 KΩ to select parallel host interface operation. CX81801 operation in serial interface mode is not described in this document (see SmartV.XX Modem Data Sheet, Doc. No. 101898 for CX81801 operation in serial interface mode.)
STPMODE# (PD3)	9	I	Ith/Ot2	**Stop Mode.** Not used. Connect to +3.3 V through 47 KΩ.
NMI#	117	I	Ithpu	**Non-Maskable Interrupt.** Not used. Connect to +3.3V.
RESET#	34	I	It	**Reset.** The active low RESET# input resets the CX81801 logic, and restores the saved configuration from serial EEPROM or returns the modem to the factory default values if NVRAM is not present. RESET# low holds the modem in the reset state; RESET# going high releases the modem from the reset state. After application of VDD, RESET# must be held low for at least 15 ms after the VDD power reaches operating range. The modem device set is ready to use 25 ms after the low-to-high transition of RESET#. Connect RESET# input to the CX11253 XRESET_N pin through 51 Ω.
VGG	60	P	PWRG	**I/O Signaling Voltage Source.** Connect to +3.3V for +3.3V inputs or +5V for +5V inputs.
VDD	2, 15, 40, 58, 78, 100, 108, 116, 124	P	PWR	**Digital Supply Voltage.** Connect to VCC (+3.3V, filtered).
VDD_CORE	20, 53, 85	P	PWR	**Core Voltage.** Internal core voltage.
GND	10, 25, 30, 44, 48, 68, 90, 95, 103, 112, 120, 128	G	GND	**Digital Ground.** Connect to digital ground (GND).
LPO	57	I	I/O	**Low Power Oscillator.** Connect to +3.3V through 240 KΩ.
NOXYCK	47	I	Itpu	**Disable XCLK Output**. When low, disables XCLK output (reduces internal power consumption). When high, enables XCLK output. Connect to GND.
PLLVDD	82	P	PWR	**PLL Circuit Digital Supply Voltage.** Connect to +3.3V and to GND through 1 μF.
PLLGND	83	G	GND	**PLL Circuit Digital Ground.** Connect to GND.
Serial EEPROM (NVRAM) Interface				
NVMCLK (PA7)	33	O	It/Ot2	**NVRAM Clock.** NVMCLK output high enables the EEPROM. Connect to EEPROM SCL pin.
NVMDATA (PE3)	18	I/O	It/Ot2	**NVRAM Data.** The NVMDATA pin supplies a serial data interface to the EEPROM. Connect to EEPROM SDA pin and to +3.3V through 10 KΩ.
LED Interface				
OHIND#/RXPAD# (PE0)	14	O	It/Ot8	**Off-Hook Indicator.** Active low. Connect to LED circuit.

Table 3-5. CX81801 Smart Modem Pin Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
DIB Interface				
PWRCLKP	96	O	Odpc	**Clock and Power Positive.** Provides clock and power to the LSD. Connect to DIB transformer primary winding non-dotted terminal.
PWRCLKN	97	O	Odpc	**Clock and Power Negative.** Provides clock and power to the LSD. Connect to DIB transformer primary winding dotted terminal.
DIB_DATAP	93	I/O	Idd/Odd	**Data Positive.** Transfers data, control, and status information between the Smart Modem and the LSD. Connect to LSD through DIB data positive channel components.
DIB_DATAN	94	I/0	Idd/Odd	**Data Negative.** Transfers data, control, and status information between the Smart Modem and the LSD. Connect to LSD through DIB data negative channel components.
External Bus Interface				
A0-A9, A10-A15, A16 (PB0), A17 (PB4), A18 (PB5)	71-77, 79-81, 84, 86-89, 91, 99, 105, 106	O, O, O, O, O	It/Ot8, It/Ot8, It/Ot2, It/Ot2, It/Ot2	**Address Lines 0-18.** A0-A18 are the address output lines used to access optional external memory; up to 4 Mb (512 KB) ROM/flash ROM using A0-A18 and up to 1 Mb (128 KB) RAM using A0-A16. The 256 KB base modem ROM code is located in the 0-256 KB address range. Leave open if not used.
D0-D7	62-67, 69-70	I/O	Ith/Ot2	**Data Line 0-7.** D0-D7 are the bidirectional external memory bus data lines. Leave open if not used.
READ#	119	O	It/Ot2	**Read Enable.** READ# output low enables data transfer from the selected device to the D0-D7 lines. Leave open if not used.
WRITE#	118	O	It/Ot2	**Write Enable.** WRITE# output low enables data transfer from the D0-D7 lines to the selected device. Leave open if not used.
ROMSEL# (PB2)	102	O	Ot2	**ROM Select**. ROMSEL# (PB2, ES3) output low selects the external ROM/flash ROM. Leave open if not used.
RAMSEL# (PB3)	104	O	It/Ot2	**RAM Select.** RAMSEL# (PB3, ES2) output low selects the external RAM. Leave open if not used.
EXT_RES# (PB6)	107	O	It/Ot2	**External Device Reset.** Active low reset for external devices. Connect to +3.3 V through 47 KΩ.
Parallel Host Interface				
HCS# (PD4)	11	I	It	**Host Bus Chip Select.** HCS# input low enables the MCU host bus interface. Connect to GND.
HWT# (PD5)	12	I	Ithpu	**Host Bus Write.** HWT# is an active low, write control input. HWT# low allows the host to write data or control words into a selected MCU register. Connect to CX11253 XWE_N pin through 51 Ω.
HRD# (PD6)	13	I	Ithpu	**Host Bus Read.** HRD# is an active low, read control input. HRD# low allows the host to read status information or data from a selected MCU register. Connect to CX11253 XRD_N pin through 51 Ω.
HINT (PB7)	109	O	It/Ot8	**Host Bus Interrupt.** HINT output is set high when the receiver error flag, received data available, transmitter holding register empty, or modem status interrupt is asserted. HINT is reset low upon the appropriate interrupt service or master reset operation. Connect to CX11253 INT0_N pin through 51 Ω.
HA0-HA2 (PD0-PD2)	6-8	I	Ithpd/Ot2	**Host Bus Address Lines 0-2.** During a host read or write operation with HCS# low, HA0-HA2 select an internal MCU 16550A-compatible register. Connect to CX11253 XA[2:0] pins through 51 Ω.
HD0-HD7 (PC0-PC7)	122-123, 125-127, 1, 3-4	I/O	Ith/Ot8	**Host Bus Data Lines 0-7**. HD0-HD7 are three-state input/output lines providing bidirectional communication between the host and the MCU. Data, control words, and status information are transferred over HD0-HD7. Connect to CX11253 XD[7:0] pins through 51 Ω.

Table 3-5. CX81801 Smart Modem Pin Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
Speaker Interface				
DSPKOUT	98	O	It/Ot2	**Modem Speaker Digital Output.** The DSPKOUT digital output reflects the received analog input signal digitized to TTL high or low level by an internal comparator. Typically, connect to a digital call progress speaker circuit.
Test				
TESTP	110	I	Itpu	**Test.** Used for factory test only. Leave open.
DV1TP	111	I	Itpu	**Test.** Used for factory test only. Connect to GND.
Not Used				
IASLEEP (P_PF05)	50	O	Ot2	**Not Used.** Leave open.
M_CLK (P_PB00)	37	O	It/Ot2	**Not Used**. Leave open.
SR2CLK (P_PGP05)	92	I	Itpu/Ot2	**Not Used.** Leave open.
SA2CLK (P_PX05)	38	I	Itpu/Ot2	**Not Used.** Leave open.
SR3OUT	35	O	Ot2	**Not Used.** Leave open.
SR3IN (P_PX01)	36	I	Itk/Ot2	**Not Used.** Leave open.
SR2IO (P_PX06)	39	O	It/Ot2	**Not Used.** Leave open.
LINE/CELL (PE7)	23	I	It/Ot8	**Not Used.** Connect to +3.3 V through 47 KΩ.
LINE/GSM (PA5)	31	I	It/Ot2	**Not Used.** Connect to +3.3 V through 47 KΩ.
GSM/RXD (PA2)	27	I	It/Ot2	**Not Used.** Leave open.
GSM/TXD (PA6)	32	O	It/Ot2	**Not Used.** Leave open.
CELCLK (PA4)	29	I	Itpu/Ot2	**Not Used.** Leave open.
CELDATA (PE5)	21	I/O	It/Ot2	**Not Used.** Connect to +3.3 V through 47 KΩ.
CELBSY (PE2)	17	O	It/Ot2	**Not Used.** Leave open.
CELBSY# (PA3)	28	I	Itpu/Ot2	**Not Used.** Leave open.
VOICE#/TXPAD# (PE1)	16	O	It/Ot2	**Not Used.** Leave open.
HS_LCS (PE4)	19	I	It/Ot2	**Not Used.** Connect to GND through 47 KΩ.
XCLK	49	O	It/Ot2	**Not Used.** Leave open.
PHS2	121	O	Ot2	**Not Used.** Leave open.
SR4RIN	45	I	Itk	**Not Used.** Leave open.
PD7	46	I/O	It/Ot2	**Not Used.** Connect to +3.3 V through 47 KΩ.
RESERVED (P_PA05)	56	I/O	Itk/Ot2	**Reserved.** Connect to +3.3 V through 240 KΩ.
RESERVED (PA0)	24	O	It/Ot2	**Reserved.** Connect to +3.3 V through 47 KΩ.
RESERVED (PE6)	22	O	It/Ot2	**Reserved.** Connect to +3.3 V through 47 KΩ.
RESERVED (PA1)	26	O	It/Ot2	**Reserved.** Connect to +3.3 V through 47 KΩ.
RESERVED (PB1)	101	O	It/Ot2	**Reserved.** Leave open.
RESERVED (P_PA00)	55	I/O	Itpu/Ot2	**Reserved.** Leave open.
RESERVED (P_PA04)	54	I/O	Itpu/Ot2	**Reserved.** Leave open.
RESERVED (P_PB01)	51	I/O	Itpu/Ot2	**Reserved.** Leave open.
RESERVED (P_BD2CLK)	59	I/O	Itpu/Ot2	**Reserved.** Leave open.
RESERVED (GP00)	52	I/O	It/Ot2	**Reserved.** Leave open.
P_PX00	41	I/O	It/Ot8	**Not Used.** Leave open.
P_PX02	42	I/O	Itpu/Ot2	**Not Used.** Leave open.
P_PX03	43	I/O	Itpu/Ot2	**Not Used.** Leave open.

Notes:

1. I/O Types: See Table 3-7.

2. Interface Legend:
   DIB Digital Isolation Barrier
   NC No internal pin connection
   RESERVED = No external connection allowed (may have internal connection).

Table 3-7. CX81801 Smart Modem I/O Type Definitions

I/O Type	Description
Idd/Odd	Digital input/output, DIB data transceiver
Ix/Ox	I/O, wire
It/Ot2	Digital input, +5V tolerant/ Digital output, 2 mA, Z_{INT} = 120 Ω
Itk/Ot2	Digital input, +5V tolerant, keeper/ Digital output, 2 mA, Z_{INT} = 120 Ω
Itpu/Ot2	Digital input, +5V tolerant, 75k Ω pull up/ Digital output, 2 mA, Z_{INT} = 120 Ω
It/Ot8	Digital input, +5V tolerant,/ Digital output, 8 mA, Z_{INT} = 50 Ω
Ithpd/Ot2	Digital input, +5V tolerant, hysteresis, 75k Ω pull down/ Digital output, 2 mA, Z_{INT} = 120 Ω
Ith/Ot2	Digital input, +5V tolerant, hysteresis/Digital output, 2 mA, Z_{INT} = 120 Ω
Ith/Ot8	Digital input, +5V tolerant, hysteresis/Digital output, 8 mA, Z_{INT} = 50 Ω
It	Digital input, +5V tolerant
Itk	Digital input, +5V tolerant, keeper
Itkpu	Digital input, +5V tolerant, keeper, 75k Ω pull up
Itpu	Digital input, +5V tolerant, 75k Ω pull up
Ithpu	Digital input, +5V tolerant, hysteresis, 75k Ω pull up
Odpc	Digital output with adjustable drive, DIB clock and power
Ot2	Digital output, three-state, 2 mA, Z_{INT} = 120 Ω
PWR	VCC Power
PWRG	VGG Power
GND	Ground

NOTES:

1. See DC characteristics in Table 3-8.
2. I/O Type corresponds to the device Pad Type. The I/O column in signal interface tables refers to signal I/O direction used in the application.

Table 3-8. CX81801 Smart Modem DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage Low	VIL					
+5V tolerant		0	–	0.8	V	
+5V tolerant hysteresis		0	–	0.3 *VGG	V	
Input Voltage High	VIH		–		V	
+5V tolerant		2	–	5.25	V	
+5V tolerant hysteresis		0.7 * VDD	–	5.25	V	
Input Hysteresis	VH		–		V	
+3V hysteresis		0.5	–		V	
+5V tolerant, hysteresis		0.3	–		V	
Output Voltage Low	VOL					
Z_{INT} = 120 Ω		0	–	0.4	V	IOL = 2 mA
Z_{INT} = 50 Ω		0	–	0.4	V	IOL = 8 mA
Output Voltage High	VOH		–		V	
Z_{INT} = 120 Ω		2.4	–	VDD	V	IOL = -2 mA
Z_{INT} = 50 Ω		2.4	–	VDD	V	IOL = -8 mA
Pull-Up Resistance	Rpu	50	–	200	kΩ	
Pull-Down Resistance	Rpd	50	–	200	kΩ	
Test Conditions unless otherwise stated: VDD = +3.3 ± 0.3 VDC; TA = 0°C to 70°C; external load = 50 pF.						

3.3 CX20493 LSD Hardware Pins and Signals

3.3.1 CX20493 LSD Signal Summary

3.3.1.1 Smart Modem Interface (Through DIB)

The DIB interface, power, and ground signals are:

- Clock (CLK, pin 26); input
- Digital Power (PWR+, pin 7); unregulated input power
- Regulated Digital Voltage Supply (DVdd, pin 24)
- Digital Ground (DGnd, pin 23); digital ground
- Regulated Analog Voltage Supply (AVdd, pin 2)
- Analog Ground (AGnd, pin 6); analog ground
- Data Positive (DIB_P, pin 27); input/output
- Data Negative (DIB_N, pin 28); input/output

3.3.1.2 Telephone Line Interface

The telephone line interface signals are:

- RING 1 AC Coupled (RAC1, pin 21); input
- TIP 1 AC Coupled (TAC1, pin 20); input
- RING 2 AC Coupled (RAC2, pin 19); input
- TIP 2 AC Coupled (TAC2, pin 18); input
- TIP and RING DC Measurement (TRDC, pin 12); input
- Electronic Inductor Capacitor (EIC, pin 11)
- Electronic Inductor Output (EIO, pin 17)
- Electronic Inductor Feedback (EIF, pin 16)
- Receive Analog Input (RXI, pin 9); input
- Transmit Output (TXO, pin 14); output
- Transmit Feedback (TXF, pin 13); input
- Virtual Impedance 0 (VZ, pin 10); input
- Electronic Inductor Ground (DC_GND, pin 15)

3.3.1.3 Voltage References

There are three reference voltage pins:

- Output Middle (Center) Reference Voltage (Vc, pin 3); output for decoupling
- Output Reference Voltage (VRef, pin 4); output for decoupling
- Bias Resistor (RBias, pin 5); input

3.3.1.4 General Purpose Input/Output

There is one unassigned general purpose input/output pin:

- General Purpose Input/Output 1 (GPIO1, pin 1); input/output

3.3.1.5 No Connects

Three pins are not used:

- No Connect 1 (NC1, pin 8); no internal connection
- No Connect 2 (NC2, pin 22); no internal connection
- No Connect 3 (NC3, pin 25); no internal connection

3.3.2 CX20493 LSD Pin Assignments and Signal Definitions

CX20493 LSD hardware interface signals are shown by major interface in Figure 3-5, are shown by pin number in Figure 3-6, and are listed by pin number in Table 3-9.

CX20493 LSD hardware interface signals are defined in Table 3-10.

CX20493 LSD GPIO DC electrical characteristics are specified in Table 3-11.

CX20493 LSD AVdd DC electrical characteristics are listed in Table 3-12.

Figure 3-5. CX20493 LSD Hardware Interface Signals

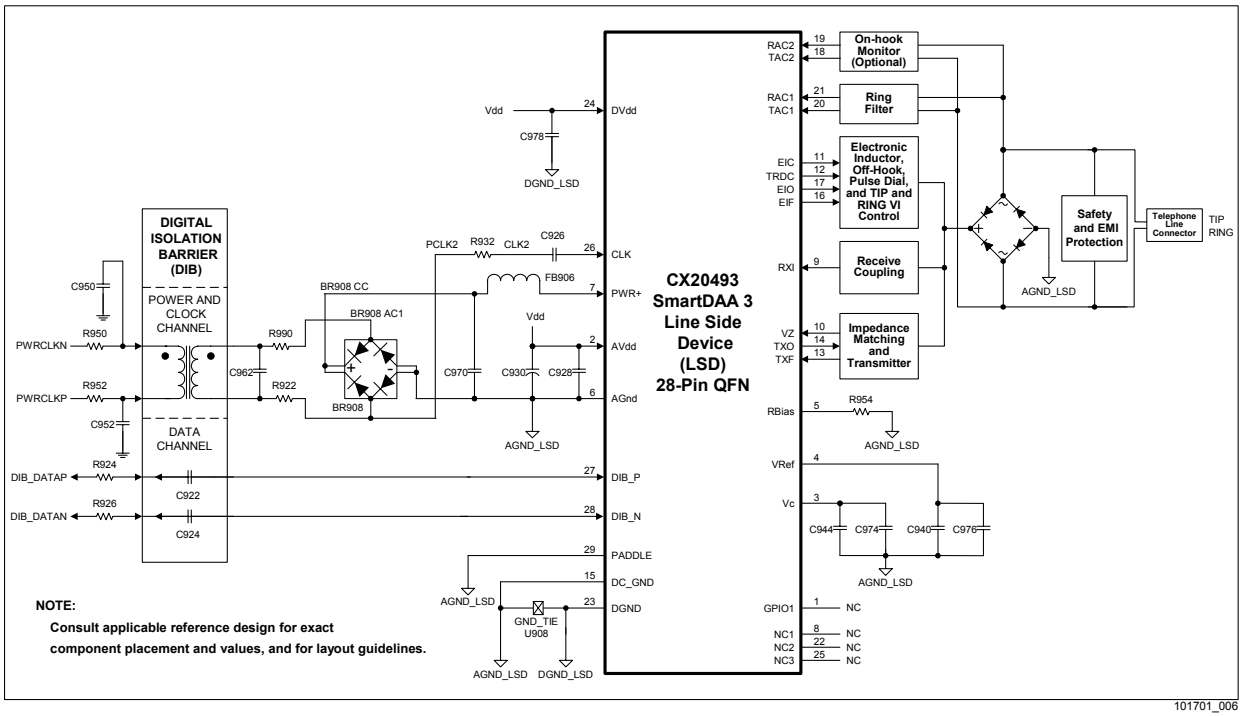


Figure 3-6. CX20493 LSD 28-Pin QFN Pin Signals

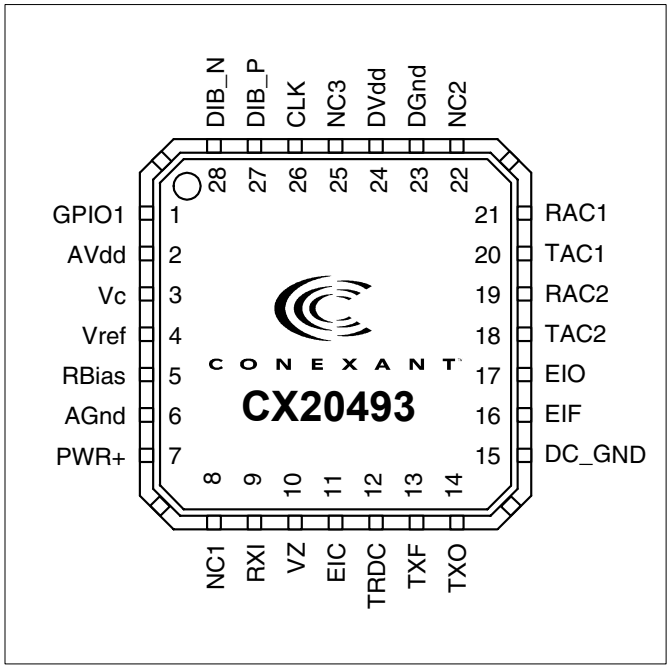


Table 3-9. CX20493 LSD 28-Pin QFN Pin Signals

Pin	Signal Label	Pin	Signal Label
1	GPIO1	15	DC_GND
2	AVdd	16	EIF
3	Vc	17	EIO
4	VRef	18	TAC2
5	RBias	19	RAC2
6	AGnd	20	TAC1
7	PWR+	21	RAC1
8	NC1	22	NC2
9	RXI	23	DGnd
10	VZ	24	DVdd
11	EIC	25	NC3
12	TRDC	26	CLK
13	TXF	27	DIB_P
14	TXO	28	DIB_N

Table 3-10. CX20493 LSD Hardware Signal Definitions

Label	Pin	I/O	I/O Type	Signal Name/Description
System Signals				
AVdd	2	PWR	PWR	**Regulated Power Output.** Provides external power for LSD digital circuits and a connection point for external decoupling. (AVdd is routed internally to LSD analog circuits.) See PWR+ pin description. Connect to LSD DVdd pin and connect to AGND_LSD through C928 and C930 in parallel. C928 and C930 must be placed close to pins 2 and 6. C930 must have ESR < 2 Ω.
AGnd	6	AGND_LSD	AGND_LSD	**Analog Ground.** Connect to DIB transformer secondary winding undotted terminal through BR908, R990, and R922.
VRef	4	REF	REF	**Output Reference Voltage.** Connect to AGND_LSD through C940 and C976, which must be placed close to pin 4. Ensure a very close proximity between C940 and the VRef pin. C940 must have a maximum ESR of 2 Ω.
Vc	3	REF	REF	**Output Middle Reference Voltage.** Connect to AGND_LSD through C944 and C974, which must be placed close to pin 3. Ensure a very close proximity between C944 and the Vc pin. Use a short path and a wide trace to AGND_LSD pin.
PWR+	7	PWR	PWR	**Unregulated Power Input.** Provides unregulated input power to the LSD. PWR+ pin is an input which takes unregulated +3.2V to +4.5V from the DIB power supply made up of the transformer, full-wave rectifier, and filter capacitors. The PWR+ input is regulated by an internal linear regulator to +3.3V ± 5% which is routed to the AVdd pin. If PWR+ is less than +3.4V, then AVdd is equal to the unregulated PWR+ input value minus 150 mV. Connect to DIB transformer secondary winding dotted terminal through FB906, BR908, R990, and R922. Connect transformer side of FB906 to AGND_LSD though C970. Place FB906 and C970 close to pin 7 and pin 6 (AGnd).
DVdd	24	PWR	PWR	**Digital Power Input.** Input power for LSD digital circuits. Connect to LSD AVdd pin and connect to DGND_LSD through C978. Place C978 near pin 24.
DGnd	23	DGND_LSD	DGND_LSD	**LSD Digital Ground.** Connect to DGND_LSD, and to AGND_LSD at the DGND_LSD/AGND_LSD tie point (U908).
PADDLE	—	AGND_LSD	AGND_LSD	**Paddle Ground.** Referred to as pin 29 in schematics. Connect to AGND_LSD.
DIB Interface Signals				
CLK	26	I	I	**Clock.** Provides input clock, AC coupled to the LSD**.** Connect to DIB transformer secondary winding undotted terminal through C926 (closest to the CX20493), R932, then R922 in series. Connect the R932 and R922 node to LSD AGND pin through full-wave rectifier BR908. Place C926 near pin 26 and place R932 near C926.
DIB_P	27	I/O	I/O	**Data and Control Positive.** Connect to DIBDAT_P through R924 in series with C922. DIB_P and DIB_N signals are differential and half-duplex bidirectional.
DIB_N	28	I/O	I/O	**Data and Control Negative.** Connect to DIBDAT_N through R926 in series with C924. DIB_P and DIB_N signals are differential and half-duplex bidirectional.

Table 3-11. CX20493 LSD Hardware Signal Definitions (Continued)

Label	Pin	I/O	I/O Type	Signal Name/Description
TIP and RING Interface				
RAC1 TAC1	21 20	I I	Ia Ia	**RING1 AC Coupled and TIP1 AC Coupled.** AC-coupled voltage from telephone line used to detect ring. Connect RAC1 to the diode bridge AC node (RING) through R902 (connects to pin 21) and C902 in series. Connect TAC1 to the diode bridge AC node (TIP) through R904 (connects to pin 20) and C904 in series.
RAC2 TAC2	19 18	I I	Ia Ia	**RING2 AC Coupled and TIP2 AC Coupled.** AC-coupled voltage from telephone line used to optionally detect signal while on-hook. Connect RAC2 to the diode bridge AC node (RING) through R948 (connects to pin 19) and C948. Leave open if not used. Connect TAC2 to the diode bridge AC node (TIP) through R946 (connects to pin 21) and C946. Leave open if not used.
EIC	11	O	Oa	**Electronic Inductor Capacitor Switch.** Internally switched to TRDC when pulse dialing. Connect to AGND_LSD through C958.
TRDC	12	I	Ia	**TIP and RING DC Measurement.** Input on-hook voltage (from a resistive divider). Used internally to extract TIP and RING DC voltage and Line Polarity Reversal (LPR) information. R906 and C918 must be placed very close to pin 12.
EIO	17	O	Oa	**Electronic Inductor Output.** Calculated voltage is applied to this output to control off-hook and DC VI mask operation. Connect to base of Q902.
DC_GND	15	GND	AGND_LSD	**LSD Electronic Inductor Ground.** Connect to AGND_LSD and to the GND_LSD/AGND_LSD tie point (U908).
EIF	16	I	Ia	**Electronic Inductor Feedback.** Connect to emitter of Q904 through R968.
RXI	9	I	Ia	**Receive Analog Input.** Receiver operational amplifier inverting input. AC coupled to the Bridge CC node through R910 (connects to pin 9) and C912 in series. R910 and C912 must be placed very close to pin 9. The length of the PCB trace connecting R910 to the RXI pin must be kept at an absolute minimum.
RBias	5	I	Ia	**Receiver Bias.** Connect to AGND_LSD through R954, which must be placed close to pin 5.
VZ	10	I	Ia	**Virtual Impedance.** Input signal used to provide line complex impedance matching for worldwide countries. AC coupled to Bridge CC node through R908 (connects to pin 10) and C910 in series. R908 and C910 must be placed very close to pin 10. The length of the PCB trace connecting R908 to the VZ pin must be kept at an absolute minimum.
TXO	14	O	Oa	**Transmit Output.** Outputs transmit signal and impedance matching signal; connect to base of transmitter transistor Q906.
TXF	13	I	Ia	**Transmit Feedback.** Connect to emitter of transmitter transistor Q906.
Not Used				
GPIO1	1	I/O	It/Ot12	**General Purpose I/O 1**. Leave open if not used.
NC1	8			**No Connect.** No internal connection. Leave open.
NC2	22			**No Connect.** No internal connection. Leave open.
NC3	25			**No Connect.** No internal connection. Leave open.

Notes:

1. I/O types*:

Ia	Analog input
It	Digital input*
Oa	Analog output
Ot12	Digital output*
AGND_LSD	Isolated LSD Analog Ground (isolated from the host system ground)
GND_LSD	Isolated LSD Digital Ground (isolated from the host system ground)

*See Section CX20493 LSD GPIO DC Electrical Characteristics (Table 3-11).

2. Refer to applicable reference design for exact component placement and values.

Table 3-11. CX20493 LSD GPIO DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Voltage	V_{IN}	-0.30	–	3.465	V	DVdd = +3.465V
Input Voltage Low	V_{IL}	–	–	1.0	V	
Input Voltage High	V_{IH}	1.6	–	–	V	
Output Voltage Low	V_{OL}	0	–	0.33	V	
Output Voltage High	V_{OH}	2.97	–	–	V	
Input Leakage Current	–	-10	–	10	µA	
Output Leakage Current (High Impedance)	–	-10	–	10	µA	
GPIO Output Sink Current at 0.33 V maximum	–	2.4	–	-	mA	
GPIO Output Source Current at 2.97 V minimum	–	2.4	–	-	mA	
GPIO Rise Time/Fall Time		20		100	ns	
Test Conditions unless otherwise stated: DVdd = +3.3V +5%; TA = 0°C to 70°C; external load = 50 pF						

Table 3-12. CX20493 AVdd DC Electrical Characteristics

PWR+ Input	AVdd Output
+3.4V < PWR+ < +4.5V	+3.3V ± 5%
+3.2V < PWR+ < +3.39V	3.05V < AVdd < 3.24V
See PWR+, AVdd, and DVdd descriptions in Table 3-10.	

3.4 Electrical and Environmental Specifications

3.4.1 Operating Conditions, Absolute Maximum Ratings, and Power Requirements

The operating conditions are specified in Table 3-13.

The absolute maximum ratings are listed in Table 3-14.

The current and power requirements are listed in

Table 3-15.

Table 3-13. Operating Conditions

Parameter	Symbol	Limits	Units
+ 5V Supply Voltage (CX11253)	V5_AB, V5_CD	+5.0	VDC
+ 3.3V Supply Voltage (CX11253)	VDD_CORE, VDD_IO		VDC
+ 3.3V Supply Voltage (CX81801)	VDD	+3.0 to +3.6	VDC
Operating Ambient Temperature	T_A	0 to +70	°C

Table 3-14. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage (CX81801)	VDD	-0.5 to +4.0	VDC
Input Voltage (CX81801)	V_{IN}	-0.5 to (VGG +0.5)*	VDC
Analog Inputs (CX81801)	V_{IN}	-0.3 to (VAA + 0.5)	VDC
Voltage Applied to Outputs in High Impedance (Off) State (CX81801)	V_{HZ}	-0.5 to (VGG +0.5)*	VDC
+5 V supply voltage (CX11253)	V5_AB, V5_CD	-0.5 to + 6.0	V
+3.3V supply voltage(CX11253)	VDD_CORE, VDD_IO	-0.5 to +4.0	V
Input voltage(CX11253)	V_{IN}	-0.5 to (VDD +0.3)	V
Voltage applied to outputs in high impedance (off) state(CX11253)	V_{HZ}	-0.5 to (VDD +0.3)*	V
Storage Temperature Range	T_{STG}	-55 to +125	°C
DC Input Clamp Current	I_{IK}	±20	mA
DC Output Clamp Current	I_{OK}	±20	mA
Static Discharge Voltage (25°C)	V_{ESD}	±2500	VDC
Latch-up Current (25°C)	I_{TRIG}	±400	mA
* VGG = +3.3V ± 0.3V or +5V ± 5%.			

Handling CMOS Devices

The device contains circuitry to protect the inputs against damage due to high static voltages. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage.

An unterminated input can acquire unpredictable voltages through coupling with stray capacitance and internal cross talk. Both power dissipation and device noise immunity degrades. Therefore, all inputs should be connected to an appropriate supply voltage.

Input signals should never exceed the voltage range from -0.5V to VGG + 0.5V. This prevents forward biasing the input protection diodes and possibly entering a latch up mode due to high current transients.

Table 3-15. Current and Power Requirements

	Conditions	Current		Power	
UID Bus State	**UID Powered**	**Typical Current (mA)**	**Maximum Current (mA)**	**Typical Power (mW)**	**Maximum Power (mW)**
Suspend	Yes	1.2	1.4	6	7.35
Enumeration	Yes	36	41	180	215
Operating (Idle)	Yes	121	139	605	730
Operating (Connected)	Yes	124	143	620	750

Notes:

1. Operating voltage: UID VDD = +5.0 V ± 0.25 V.
2. Test conditions: UID VDD = +5.0 V for typical values; VDD = + 5.25 V for maximum values.
3. Current and power is shown for UID VDD. The DSP +3.3 V power is supplied by the UID.

3.4.2 Interface and Timing Waveforms

3.4.2.1 External Memory Bus Timing

The external memory bus timing is listed in Table 3-16 and illustrated in Figure 3-7.

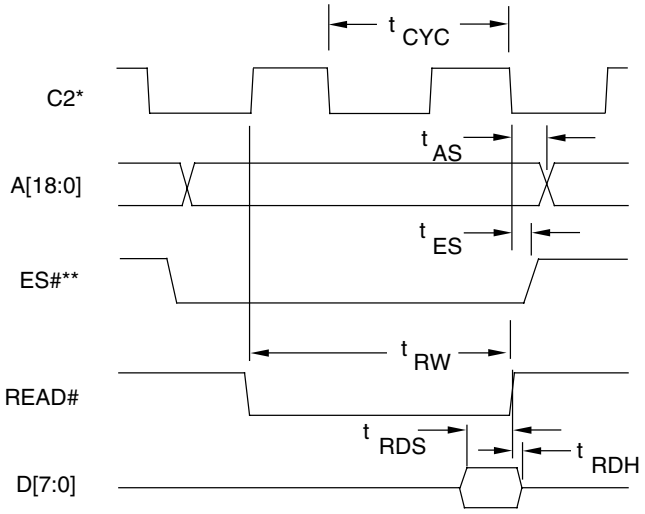
Table 3-16. Timing - External Memory Bus

Symbol	Parameter	Min	Typ.	Max	Units
t_{FI}	Internal Operating Frequency	28.224	–	–	MHz
t_{CYC}	Internal Operating Clock Cycle	30	–	–	ns
Read					
t_{AS}	READ# High to Address Valid	–	6.5	9	ns
t_{ES}	READ# High to ES Valid	–	8	11	ns
t_{RW}	READ# Pulse Width	15	–	105	ns
t_{RDS}	Read Data Valid to READ# High	6.1	–	–	ns
t_{RDH}	READ# High to Read Data Hold	0	0	–	ns
Write					
t_{AS}	WRITE# High to Address Valid	–	6.5	8	ns
t_{ES}	WRITE# High to ES Valid	–	8	11	ns
t_{WW}	WRITE# to WRITE# Pulse Width	15	–	105	ns
t_{WTD}	WRITE# Low to Write Data Valid	–	5	8.2	ns
t_{WTH}	WRITE# High to Write Data Hold	5.0	–	–	ns

Notes:

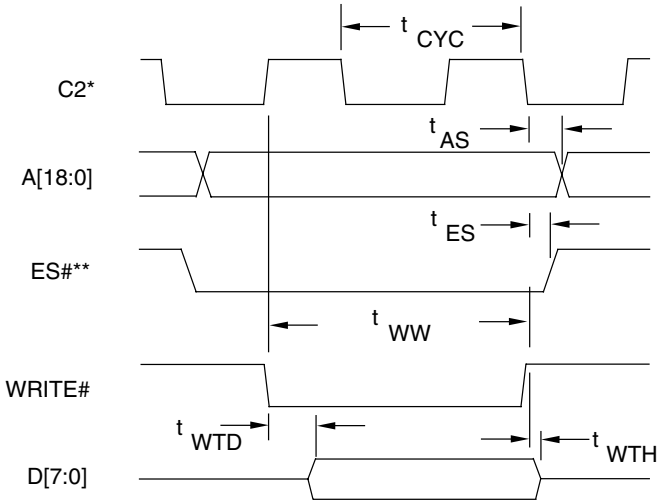
1. ES = RAMSEL# or ROMSEL#.
2. Read pulse width and write pulse width:
   RAM: t_{RW}, t_{WW} = 0.5 t_{CYC} = 15 for Non-Extended Cycle Timing
   ROM: t_{RW}, t_{WW} = 3.5 t_{CYC} = 105 for Extended Cycle Timing
3. Memory speed determination:
   RAM: $t_{ACCESS} = t_{CYC} - t_{ES} - t_{RDS}$ = 330 - 8 - 6.1 = 15.9 ns (i.e., use 15 ns memory)
   ROM: $t_{ACCESS} = 4(t_{CYC}) - t_{ES} - t_{RDS}$ = 4(30) - 8 - 6.1 = 105.9 ns (i.e., use 90 ns memory).
4. Output Enable to Output Delay Timing:
   RAM: $t_{OE} = t_{RW} - t_{RDS} = 0.5(t_{CYC}) - t_{RDS}$ = 15 - 6.1 = 8.9 ns
   ROM: $t_{OE} = t_{RW} - t_{RDS} = 3.5(t_{CYC}) - t_{RDS}$ = 105 - 6.1 = 98.9 ns.

Figure 3-7. Waveforms - External Memory Bus



* C2 = Internal Phase 2 clock.
** ES# = RAMSEL# or ROMSEL#.

Read Timing



* C2 = Internal Phase 2 clock.
** ES# = RAMSEL# or ROMSEL#.

Write Timing

100491 F3-09 WF EB

3.4.2.2 Parallel Host Bus Timing

The parallel host bus timing is listed in Table 3-17 and illustrated in Figure 3-8.

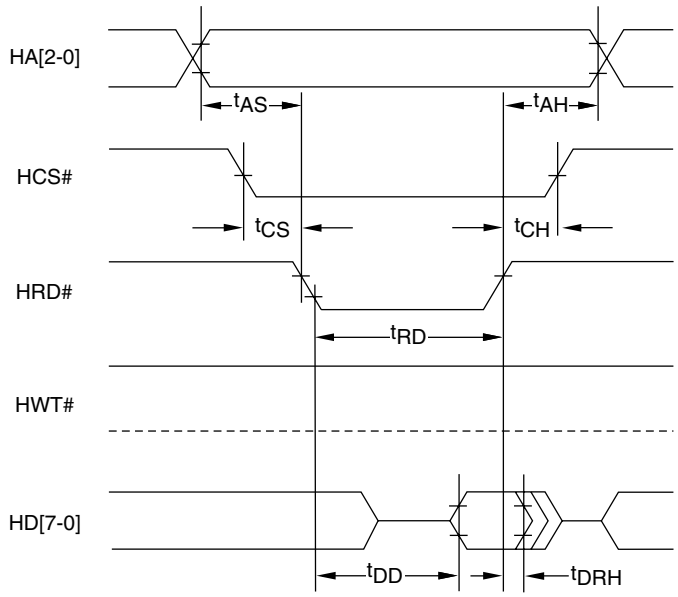
Table 3-17. Timing - Parallel Host Bus

Symbol	Parameter	Min	Max	Units
READ (See Notes 1, 2, 3, 4, 5, and 6)				
t_{AS}	Address Setup	5	–	ns
t_{AH}	Address Hold	10	–	ns
t_{CS}	Chip Select Setup	0	–	ns
t_{CH}	Chip Select Hold	10	–	ns
t_{RD}	HRD# Strobe Width	45	–	ns
t_{DD}	Read Data Delay	–	25	ns
t_{DRH}	Read Data Hold	5	–	ns
WRITE (See Notes 1, 2, 3, 4, 5, and 6)				
t_{AS}	Address Setup	5	–	ns
t_{AH}	Address Hold	15	–	ns
t_{CS}	Chip Select Setup	0	–	ns
t_{CH}	Chip Select Hold	10	–	ns
t_{WT}	HWT# Strobe Width	75	–	ns
t_{DS}	Write Data Setup (see Note 4)	–	20	ns
t_{DWH}	Write Data Hold (see Note 5)	5	–	ns

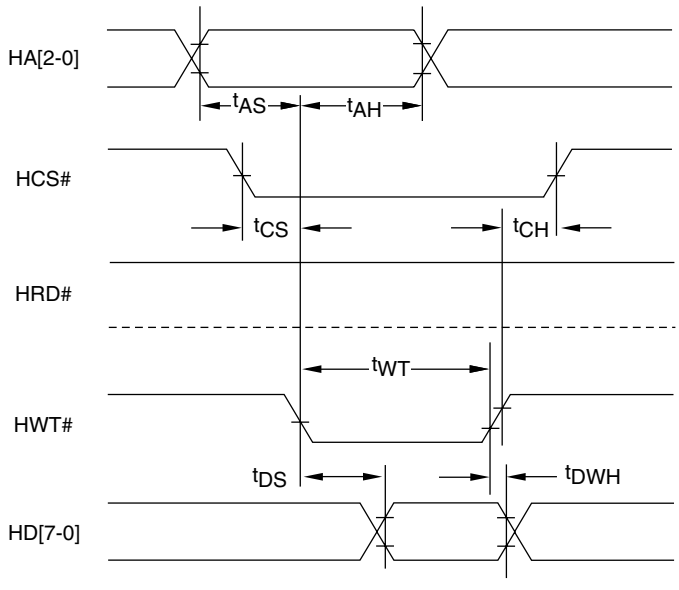
Notes:

1. When the host executes consecutive Rx FIFO reads, a minimum delay of 2 times the internal CPU clock cycle plus 15 ns (85.86 ns at 28.224 MHz) is required from the falling edge of HRD# to the falling edge of the next Host Rx FIFO HRD# clock.
2. When the Host executes consecutive Tx FIFO writes, a minimum delay of 2 times the internal CPU clock cycle plus 15 ns (85.86 ns at 28.224 MHz) is required from the falling edge of HWT# to the falling edge of the next Host Tx FIFO HWT# clock.
3. t_{RD}, t_{WT} = t_{CYC} + 15 ns.
4. t_{DS} is measured from the point at which both HCS# and HWT# are active.
5. t_{DWH} is measured from the point at which either HCS# and HWT# become inactive.
6. Clock frequency = 28.224 MHz clock.

Figure 3-8. Waveforms - Parallel Host Bus



a. Host Read



b. Host Write

100491 F3-10 WF-HB

3.5 Crystal Specifications

Crystal specifications are listed in Table 3-18.

Table 3-18. Crystal Specifications

Characteristic	Value
Frequency	28.224 MHz nominal
Calibration tolerance including effects due to temperature and aging	±100 ppm (C_L = 16.5 and 19.5 pF)
Oscillation mode	Fundamental
Calibration mode	Parallel resonant
Load capacitance, C_L	18 pF nom.
Shunt Capacitance, C_O	7 pF max.
Series resistance, R_1	35-60 Ω max. @20 nW drive level
Drive level	100µW correlation; 500µW max.
Operating temperature	0°C to 70°C
Storage temperature	–40°C to 85°C

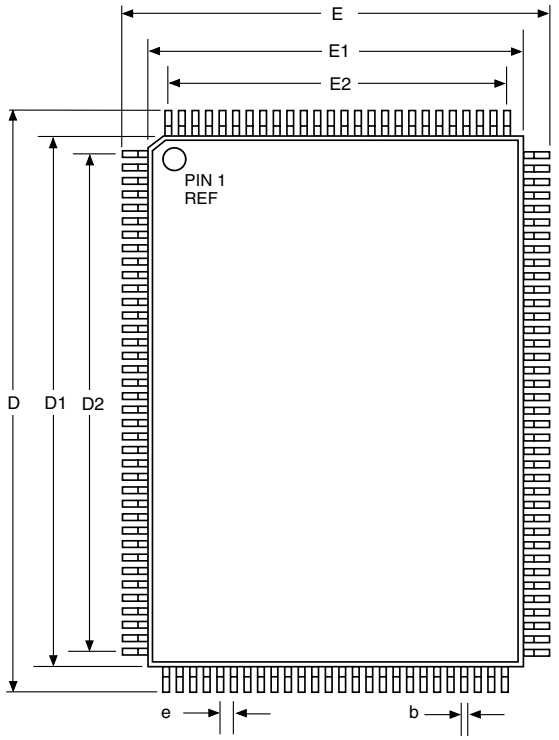
4. Package Dimensions

The 128-pin TQFP package dimensions are shown in Figure 4-1.

The 64-pin TQFP package dimensions are shown in Figure 4-2.

The 28-pin QFN package dimensions are shown in Figure 4-3.

Figure 4-1. Package Dimensions - 128-Pin TQFP



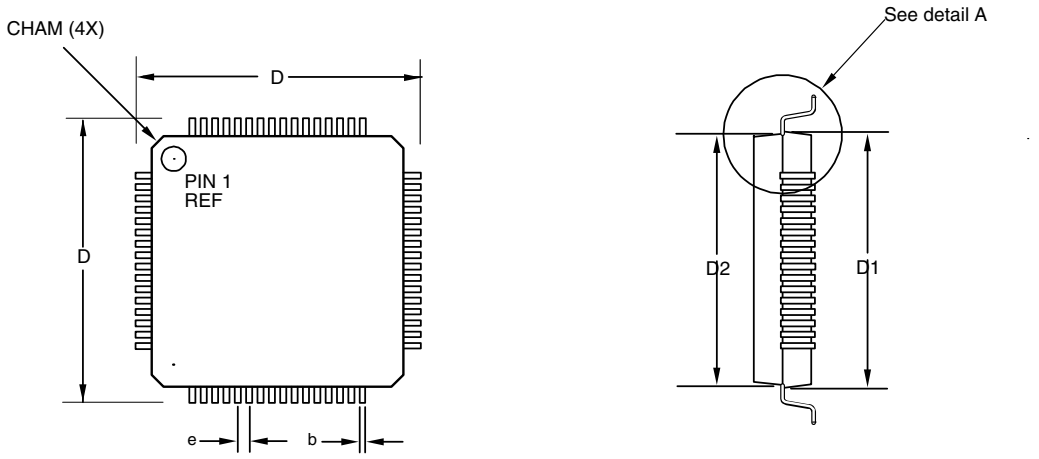
Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.0059
A2	1.4 REF		0.0551 REF	
D	21.75	22.25	0.8563	0.8760
D1	20.0 REF		0.7874 REF	
D2	18.5 REF		0.7283 REF	
E	15.75	16.25	0.6201	0.6398
E1	14.0 REF		0.5512 REF	
E2	12.5 REF		0.4921 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.50 BSC		0.0197 BSC	
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity	0.08 MAX		0.0031 MAX	

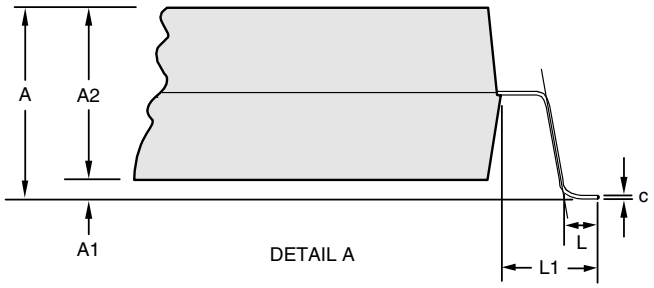
Ref: 128-PIN TQFP (GP00-D264)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

PD-TQFP-128 (040395)

Figure 4-2. Package Dimensions - 64-Pin TQFP





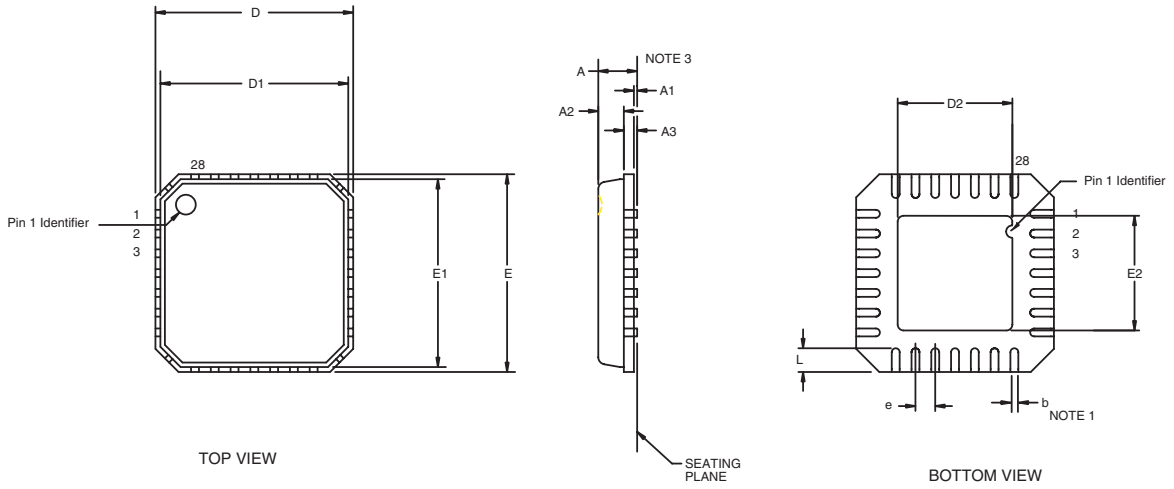
Dim.	Millimeters			Inches*		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.45		1.55	0.057		0.061
A1	0.05		0.15	0.002		0.006
A2	1.35		1.45	0.053		0.057
D	11.85		12.15	0.467		0.478
D1	9.95		10.05	0.392		0.396
D2	9.80		9.90	0.386		0.390
L	0.45		0.75	0.018		0.030
L1	1.00 REF			0.039 REF		
e	0.50 BSC			0.020 BSC		
b	0.15		0.25	0.006		0.010
c	0.11		0.17	0.004		0.007

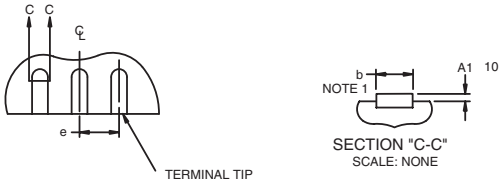
Ref: 64-PIN TQFP (GP00-D450)

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may include round-off errors.

PD_GP00-D450

Figure 4-3. Package Dimensions - 28-Pin QFN





Symbol	Dimensions (Millimeters)		
	Min.	Nom.	Max.
e		0.5 BSC	
L	0.50	0.60	0.75
b	0.23	0.28	0.35
D2	2.95	3.10	3.25
E2	2.95	3.10	3.25
A	-	0.85	1.00
A1	0.00	0.01	0.05
A2	-	0.65	0.80
A3	0.15	0.20	0.25
D	4.90	5.00	5.10
D1	4.65	4.75	4.85
E	4.90	5.00	5.10
E1	4.65	4.75	4.85
Ref. GP00-D682-001			

NOTES:

1. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
2. PACKAGE WARPAGE MAX 0.05mm.
3. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.

PD_GP00-D682-001

5. USB General Operation

5.1 Descriptors

USB devices report their attributes using descriptors. A descriptor is a data structure with a defined format, which begins with a byte-wide field that contains the total number of bytes in the descriptor followed by a byte-wide field that identifies the descriptor type.

Class and vendor specific descriptors may be returned in one of two ways. Class and vendor specific descriptors that are related to standard descriptors are returned in the same data buffer as the standard descriptor. If a class or vendor specific descriptor is not related to a standard descriptor, it is returned using class or vendor specific requests.

5.1.1 Device Descriptor

A device descriptor describes general information about a USB device, which applies globally to the device and all of the device's configurations (Table 5-1). A USB device has only one device descriptor. Vendor ID, Product ID, and Device Release Number can be changed. The Manufacturer Name, Product Name, and Serial Number can also be customized.

Table 5-1. Device Descriptors

Offset	Field	Size	Value	Default (Hex.)	Description
0	*bLength*	1	Number	12	Size of this descriptor in bytes.
1	*bDescriptorType*	1	Constant	01	DEVICE Descriptor Type.
2	*bcdUSB*	2	BCD	0110	USB Specification Release Number in Binary-Coded Decimal (i.e., 2.10 is 0x210). This field identifies the release of the USB Specification that the device and its descriptors are compliant with.
4	*bDeviceClass*	1	Class	02	Class code (assigned by USB). If this field is reset to 0, each interface within a configuration specifies its own class information and the various interfaces operate independently. If this field is set to a value between 1 and 0xFE, the device supports different class specifications on different interfaces and the interfaces may not operate independently. This value identifies the class definition used for the aggregate interfaces. (For example, a CD-ROM device with audio and digital data interfaces that require transport control to eject CDs or start them spinning.) If this field is set to 0xFF, the device class is vendor specific.
5	*bDeviceSubClass*	1	SubClass	00	Subclass code (assigned by USB). These codes are qualified by the value of the bDeviceClass field. If the *bDeviceClass* field is reset to 0, this field must also be reset to 0. If the *bDeviceClass* field is not set to 0xFF, all values are reserved for assignment by USB.
6	*bDeviceProtocol*	1	Protocol	FF	Protocol code (assigned by USB). These codes are qualified by the value of the *bDeviceClass* and the *bDeviceSubClass* fields. If a device supports class-specific protocols on a device basis as opposed to an interface basis, this code identifies the protocols that the device uses as defined by the specification of the device class. If this field is reset to 0, the device does not use class specific protocols on a device basis. However, it may use class specific protocols on an interface basis. If this field is set to 0xFF, the device uses a vendor specific protocol on a device basis.
7	*bMaxPacketSize0*	1	Number	40	Maximum packet size for endpoint zero (only 8, 16, 32, or 64 are valid).
8	*idVendor*	2	ID	0572	Vendor ID (Conexant ID assigned by usb.org). The OEM ID will be assigned by usb.org.
10	*idProduct*	2	ID	13xx	Product ID (assigned by the Conexant) and stored in OEM-supplied serial EEPROM: 13xx for data/fax/RTAM
12	*bcdDevice*	2	BCD	0100	Device release number in binary-coded decimal.
14	*iManufacturer*	1	Index	01	Index of string descriptor describing manufacturer.
15	*iProduct*	1	Index	02	Index of string descriptor describing product.
16	*iSerialNumber*	1	Index	00	Index of string descriptor describing the device's serial number.
17	*bNumConfigurations*	1	Number	01	Number of possible configurations.

5.1.2 Configuration Descriptor

A configuration descriptor describes information about a specific device configuration (see Table 5-2). The descriptor describes the number of interfaces provided by the configuration.

Table 5-2. Configuration Descriptors

Offset	Field	Size	Value	Default (Hex.)	Description
0	*bLength*	1	Number	09	Size of this descriptor in bytes.
1	*bDescriptorType*	1	Constant	02	CONFIGURATION.
2	*wTotalLength*	2	Number	0057	Total length of data returned for this configuration. Includes the combined length of all descriptors (configuration, interface, endpoint, and class or vendor specific) returned for this configuration.
4	*bNumInterfaces*	1	Number	02	Number of interfaces supported by this configuration.
5	*bConfigurationValue*	1	Number	01	Value to use as an argument to Set Configuration to select this configuration.
6	*iConfiguration*	1	Index	03	Index of string descriptor describing this configuration.
7	*bmAttributes*	1	Bitmap	A0	Configuration characteristics D7 Bus Powered D6 Self Powered D5 Remote Wakeup D4..0 Reserved (reset to 0) A device configuration that uses power from the bus and a local source sets both D7 and D6. The actual power source at runtime may be determined using the Get Status device request. If a device configuration supports remote wakeup, D5 is set to 1.
8	*MaxPower*	1	mA	7D	Maximum power consumption of USB device from the bus in this specific configuration when the device is fully operational. Expressed in 2 mA units (i.e., 50 = 100 mA). Note: A device configuration reports whether the configuration is bus-powered or self-powered. Device status reports whether the device is currently self-powered. If a device is disconnected from its external power source, it updates device status to indicate that it is no longer self-powered. A device may not increase its power draw from the bus, when it loses its external power source, beyond the amount reported by its configuration. If a device can continue to operate when disconnected from its external power source, it continues to do so. If the device cannot continue to operate, it fails operations it can no longer support. Host software may determine the cause of the failure by checking the status and noting the loss of the device's power source.

5.1.3 Interface Descriptor

An interface descriptor describes a specific interface provided by the associated configuration (see Table 5-3). It is always returned as part of a configuration descriptor. An interface descriptor never includes endpoint zero in the number of endpoints.

Table 5-3. Interface Descriptors

Offset	Field	Size	Value	Default (Hex.)	Description
0	*bLength*	1	Number	09	Size of this descriptor in bytes.
1	*bDescriptorType*	1	Constant	04	INTERFACE Descriptor Type.
2	*bInterfaceNumber*	1	Number	00	Number of interface. Zero-based value identifying the index in the array of concurrent interfaces supported by this configuration.
3	*bAlternateSetting*	1	Number	00	Value used to select alternate setting for the interface identified in the prior field.
4	*bNumEndpoints*	1	Number	04	Number of endpoints used by this interface (excluding endpoint zero). If this value is 0, this interface only uses endpoint zero.
5	*bInterfaceClass*	1	Class	0A	Class code (assigned by USB). If this field is reset to 0, the interface does not belong to any USB specified device class. If this field is set to 0xFF, the interface class is vendor specific. All other values are reserved for assignment by USB.
6	*bInterfaceSubClass*	1	SubClass	00	Subclass code (assigned by USB). These codes are qualified by the value of the *bInterfaceClass* field. If the *bInterfaceClass* field is reset to 0, this field must also be reset to 0. If the *bInterfaceClass* field is not set to 0xFF, all values are reserved for assignment by USB.
7	*bInterfaceProtocol*	1	Protocol	00	Protocol code (assigned by USB). These codes are qualified by the value of the *bInterfaceClass* and the *bInterfaceSubClass* fields. If an interface supports class-specific requests, this code identifies the protocols that the device uses as defined by the specification of the device class. If this field is reset to 0, the device does not use a class specific protocol on this interface. If this field is set to 0xFF, the device uses a vendor specific protocol for this interface.
8	*iInterface*	1	Index	04	Index of string descriptor describing this interface.

5.1.4 Endpoint Descriptor

Each endpoint used for an interface has its own descriptor, which contains the information required by the host to determine the bandwidth requirements of each endpoint (see Table 5-4). An endpoint descriptor, like an Interface Descriptor, is always returned as part of a configuration descriptor. The default values are:

Bulk In 1: 07058102400000

Bulk Out 1: 07050102400000

Bulk In 3: 07058302400000

Bulk Out 3: 07050302400000

Table 5-4. Endpoint Descriptors

Offset	Field	Size	Value	Description
0	*bLength*	1	Number	Size of this descriptor in bytes.
1	*bDescriptorType*	1	Constant	ENDPOINT Descriptor Type.
2	*bEndpointAddress*	1	Endpoint	The address of the endpoint on the USB device described by this descriptor. The address is encoded as follows: Bit 0..3: The endpoint number Bit 4..6: Reserved, reset to 0 Bit 7: Direction, ignored for control endpoints 0 OUT endpoint 1 IN endpoint
3	*bmAttributes*	1	Bit Map	This field describes the endpoint's attributes when it is configured using the *bConfigurationValue*. Bit 0..1: Transfer Type 00 Control 01 Isochronous 10 Bulk 11 Interrupt All other bits are reserved
4	*wMaxPacketSize*	2	Number	Maximum packet size this endpoint is capable of sending or receiving when this configuration is selected. For isochronous endpoints, this value is used to reserve the bus time in the schedule, required for the per frame data payloads. The pipe may, on an ongoing basis, actually use less bandwidth than that reserved. The device reports, if necessary, the actual bandwidth used via its normal, non-USB defined mechanisms. For interrupt, bulk, and control endpoints smaller data payloads may be sent, but will terminate the transfer and may or may not require intervention to restart. Refer to Chapter 5 for more information.
6	*bInterval*	1	Number	Interval for polling endpoint for data transfers. Expressed in milliseconds. This field is ignored for bulk and control endpoints. For isochronous endpoints this field must be set to 1. For interrupt endpoints, this field may range from 1 to 255.

5.1.5 Enumeration

The CX11253 enumeration process consists of the following steps:

1. Get device descriptor. The host requests and reads the device descriptor to determine maximum packet size.
2. Set address. The host sends the CX11253's function address in a data packet using function endpoint 0. Device firmware interprets this data.
3. Get device descriptor. The host requests and reads the device descriptor to determine such information as device class, USB Specification compliance level, maximum packet size for endpoint 0, vendor id, product id. Etc.
4. Get configuration descriptor. The host requests and reads the device configuration descriptor to determine such information as the number of interfaces and endpoints; endpoint transfer type, packet size, and direction; power source; maximum power; etc. When the host requests the configuration descriptor, all related interface and endpoint descriptors are returned.
5. Set configuration. The host assigns a configuration value to the device to establish the current configuration.

5.1.6 Endpoint Pairs

Data transfers with the host are made to/from endpoint pairs on the USB module. The CX11253 provides the function endpoint pairs listed in Table 5-5.

Table 5-5. Endpoint Pairs

Endpoint Pair	Max. Packet Size	USB Data Transfer Types
Function Endpoint 0	64 bytes	Control
Function Endpoint 1	64 bytes	Bulk
Function Endpoint 2	64 bytes	Interrupt
Function Endpoint 3	64 bytes	Bulk

NOTES

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