

Typical Application V_{DD} = 2.7V to 5.5V Typical bypass 0.1 μF Address (set as desired for ADDR one of three addresses) To hardware LM73 ALERT shutdown To / from SMBDAT processor SMBCI K 2-wire interface 20147803 I²C is a registered trademark of Philips Electronics N.V. Corporation

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LM73 2.7V, SOT-23, 11-to-14 Bit Digital Temperature Sensor

with 2-Wire Interface **General Description**

The LM73 is an integrated, digital-output temperature sensor featuring an incremental Delta-Sigma ADC with a two-wire interface that is compatible with the SMBus and I²C® interfaces. The host can guery the LM73 at any time to read temperature. Available in a 6-pin SOT-23 package, the LM73 occupies very little board area while operating over a wide temperature range (-40°C to 150°C) and providing ±1.0°C accuracy from -10°C to 80°C. The user can optimize between the conversion time and the sensitivity of the LM73 by programming it to report temperature in any of four different resolutions. Defaulting to 11-bit mode (0.25°C/LSB), the LM73 measures temperature in a maximum time of 14 ms, making it ideal for applications that require temperature data very soon after power-up. In its maximum resolution, 14-bit mode (0.03125°C/LSB), the LM73 is optimized to sense very small changes in temperature.

N**ational** Semiconductor

A single multi-level address line selects one of three unique device addresses. An open-drain ALERT output goes active when the temperature exceeds a programmable limit. Both the data and clock lines are filtered for excellent noise tolerance and reliable communication. Additionally, a time-out feature on the clock and data lines causes the LM73 to automatically reset these lines if either is held low for an extended time, thus exiting any bus lock-up condition without processor intervention.

Applications

- Portable Electronics
- Notebook Computers
- Automotive
- System Thermal Management
- Office Electronics

Key Specifications

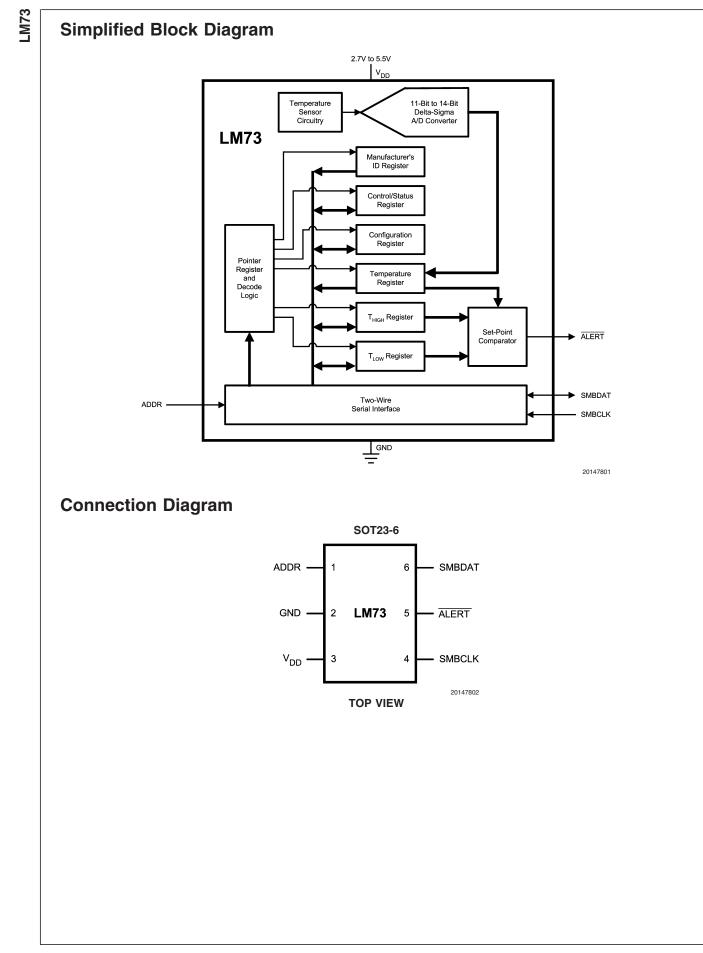
 Supply Voltage 		2.7V to 5.5V
 Supply Current 	operating	320 µA (typ)
		495 µA (max)
	shutdown	8 µA (max)
		1.9 µA (typ)
Temperature	–10°C to 80°C	±1.0°C (max)
Accuracy	–25°C to 115°C	±1.5°C (max)
	–40°C to 150°C	±2.0°C (max)
Resolution		0.25°C to
		0.03125°C
Conversion Time	11-bit (0.25°C)	14 ms (max)
	14-bit (0.03125°C)	112 ms (max)

Features

- Single address pin offers choice of three selectable addresses per version for a total of six possible addresses.
- SMBus and I²C-compatible two-wire interface
- Supports 400 kHz operation
- Shutdown mode with one-shot feature available for very low average power consumption
- Programmable digital temperature resolution from 11 bits to 14 bits.
- Fast conversion rate ideal for guick power up and measuring rapidly changing temperature
- Open-drain ALERT output pin goes active when temperature is above a programmed temperature limit
- Very stable, low-noise digital ouput.
- UL Recognized Component 91

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Daut Number	Package	NS Package	Transport	SMBus Device Address	
Part Number	Marking	Number	Media	Address Pin	Device Address
LM73CIMK-0	T730	MK06A	1000 Units on	Float	1001 000
		(Thin SOT23-6)	Tape and Reel	Ground	1001 001
				V _{DD}	1001 010
LM73CIMKX-0	T730	MK06A	3000 Units on	Float	1001 000
		(Thin SOT23-6)	Tape and Reel	Ground	1001 001
				V _{DD}	1001 010
LM73CIMK-1	T731	MK06A	1000 Units on	Float	1001 100
		(Thin SOT23-6)	Tape and Reel	Ground	1001 101
				V _{DD}	1001 110
LM73CIMKX-1	T731	MK06A	3000 Units on	Float	1001 100
		(Thin SOT23-6)	Tape and Reel	Ground	1001 101
				V _{DD}	1001 110

Note 1: Available in RoHS-compliant packages. More details at www.national.com.

Pin Descriptions

Label	Pin #	Туре	Equivalent Circuit	Function
ADDR	1	Logic Input, three levels	PIN Snap D1 Back D2 D3 D3 D	Address Select Input: One of three device addresses is selected by connecting to ground, left floating, or connecting to V _{DD} .
GND	2	Ground		Ground
V _{DD}	3	Power		Supply Voltage
SMBCLK	4	CMOS Logic Input		Serial Clock: SMBus clock signal. Operates up to 400 kHz. Low-pass filtered.
ALERT	5	Open-Drain Output		Digital output which goes active whenever the measured temperature exceeds a programmable temperature limit.
SMBDAT	6	Open-Drain Input/Output	GND	Serial Data: SMBus bi-directional data signal used to transfer serial data synchronous to the SMBCLK. Low-pass filtered.

(Note 4)

Absolute Maximum Ratings (Note 2)

Supply Voltage	–0.3 V to 6.0 V				
Voltage at Any Pin	–0.3 V to (V _{DD} + 0.5 V)				
Input Current at Any Pin (No	ote 3) ±5 mA				
Storage Temperature	–65°C to +150°C				
ESD Susceptibility (Note 5)					
Human Body Model	2000 V				
Machine Model	200 V				
Soldering process must comply with National					
Semiconductor's Reflow Ter	mperature Profile				
specifications. Refer to www	v.national.com/packaging.				

Operating Ratings

(Note 2)

Specified Temperature Range

Supply Voltage Range (V_{DD})

T_{MIN}≤T_A≤T_{MAX} $\text{-40}^{\circ}\text{C} \leq \text{T}_{\text{A}} \leq \text{+150}^{\circ}\text{C}$ +2.7V to +5.5V

Temperature-to-Digital Converter Characteristics

Unless otherwise noted, these specifications apply for $V_{DD} = 2.7V$ to 5.5V. Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX} ; all other limits $T_A = T_J = +25^{\circ}$ C, unless otherwise noted. T_A is the ambient temperature. T_J is the junction temperature.

Parameter	Conditions		Typical	Limits	Units
			(Note 6)	(Note 7)	(Limit)
Accuracy (Note 8)	$V_{DD} = 2.7V$ to	$T_A = -10^{\circ}C$ to $80^{\circ}C$		±1.0	°C (max)
	$V_{DD} = 4.5V$	T _A = –25°C to 115°C		±1.5	°C (max)
		$T_{A} = -40^{\circ}C \text{ to } 150^{\circ}C$		±2.0	°C (max)
	V_{DD} > 4.5V to	$T_A = -10^{\circ}C$ to $80^{\circ}C$		±1.5	°C (max)
	$V_{DD} = 5.5V$	T _A = -25°C to 115°C		±2.0	°C (max)
		$T_{A} = -40^{\circ}C \text{ to } 150^{\circ}C$		±2.5	°C (max)
Resolution	RES1 Bit = 0, RES0	Bit = 0	11		Bits
			0.25		°C/LSB
	RES1 Bit = 0, RES0) Bit = 1	12		Bits
			0.125		°C/LSB
	RES1 Bit = 1, RES0 Bit = 0		13		Bits
			0.0625		°C/LSB
	RES1 Bit = 1, RES0 Bit = 1		14		Bits
			0.03125		°C/LSB
Temperature Conversion	RES1 Bit = 0, RES0 Bit = 0		10.1	14	ms (max)
Time (Note 9)	RES1 Bit = 0, RES0) Bit = 1	20.2	28	ms (max)
	RES1 Bit = 1, RES0	Bit = 0	40.4	56	ms (max)
	RES1 Bit = 1, RES0) Bit = 1	80.8	112	ms (max)
Quiescent Current	Continuous Convers	ion Mode, SMBus inactive	320	495	μA (max)
	Shutdown, bus-idle	timers on	120	175	μA (max)
	Shutdown, bus-idle	timers off	1.9	8	μA (max)
Power-On Reset	Measured on V _{DD} in	put, falling edge		0.9	V (min)
Threshold					

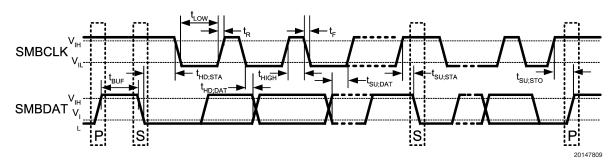
LM73

Logic Electrical Characteristics DIGITAL DC CHARACTERISTICS

Unless otherwise noted, these specifications apply for $V_{DD} = 2.7V$ to 5.5V. Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX} ; all other limits $T_A = T_J = +25$ °C, unless otherwise noted. T_A is the ambient temperature. T_J is the junction temperature.

	Parameter		Conditions	Typical		imits	Units
				(Note 6)	(N	lote 7)	(Limit)
	SMBCLK INPUTS			1			
/ _{IH}	Logical "1" Input Voltage				0.	7*V _{DD}	V (min)
/ _{IL}	Logical "0" Input Voltage				0.	3*V _{DD}	V (max)
/ _{IN;HYST}	SMBDAT and SMBCLK Digital Input Hysteresis			0.07*V _{DD}			V
IH	Logical "1" Input Current	V _{IN} =	= V _{DD}	0.01		2	µA (max)
IL	Logical "0" Input Current	<u> </u>	= 0 V	-0.01		-2	µA (max)
D _{IN}	Input Capacitance			5			pF
	ALERT OUTPUTS	1		1	1		
ОН	High Level Output Current	V _{OH}	= V _{DD}	0.01		2	µA (max)
/ _{OL}	SMBus Low Level Output Voltage		: 3 mA			0.4	V (max)
DDRES				1			. ,
/ _{IH;ADDRE}					V _{DD} m	inus 0.100	V (min)
IL;ADDRE		<u> </u>				0.100	V (max)
IH; ADDRES		V.N. =	= V _{DD}	0.01		2	μA (max)
IL:ADDRES			= 0 V	-0.01		-2	μA (max)
,	DIGITAL SWITCHING CHARACTERISTIC		•••	0.01		-	p. (11007)
Boldfac	otherwise noted, these specifications apply the limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX} Parameter	; all o	other limits $T_A =$	T _J = +25°C, un	less otherwi	se noted.	Units
Symbol	Falameter		Condit	.10115	(Note 6)	(Note 7)	(Limit)
,					(14010-0)		(Emmy
						400	kHz (may
f _{SMB}	SMBus Clock Frequency					400	
						100	Hz (min)
t _{LOW}	SMBus Clock Low Time					100 300	Hz (min) ns (min)
t _{LOW} t _{HIGH}	SMBus Clock Low Time SMBus Clock High Time		C 400 pE			100 300 300	Hz (min) ns (min) ns (min)
t _{LOW}	SMBus Clock Low Time		C _L = 400 pF			100 300	Hz (min) ns (min) ns (min)
t _{LOW} t _{HIGH} t _{F;SMBO}	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10)	set of	$C_L = 400 \text{ pF}$ $I_{PULL-UP} \leq 3 \text{ mA}$			100 300 300 250	ns (min) ns (max)
t _{LOW} t _{HIGH} t _{F;SMBO}	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10) SMBDAT and SMBCLK Time Low for Res	set of				100 300 250 15	Hz (min) ns (min) ns (min) ns (max) ms (min)
t _{LOW} t _{HIGH} t _{F;SMBO}	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10) SMBDAT and SMBCLK Time Low for Res Serial Interface (Note 11)	set of				100 300 250 15 45	Hz (min) ns (min) ns (min) ns (max) ms (min) ms (max
t _{LOW} t _{HIGH} t _{F;SMBO} t _{TIMEOUT} t _{SU;DAT}	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10) SMBDAT and SMBCLK Time Low for Res Serial Interface (Note 11) Data In Setup Time to SMBCLK High					100 300 250 15	Hz (min) ns (min) ns (min) ns (max) ms (max) ns (max)
t _{LOW} t _{HIGH} t _{F;SMBO}	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10) SMBDAT and SMBCLK Time Low for Res Serial Interface (Note 11)					100 300 250 15 45 100	Hz (min) ns (min) ns (min) ns (max) ms (min) ms (max)
t _{LOW} t _{HIGH} t _{F;SMBO} t _{TIMEOUT} t _{SU;DAT} t _{hD;DATI}	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10) SMBDAT and SMBCLK Time Low for Res Serial Interface (Note 11) Data In Setup Time to SMBCLK High Data Hold Time: Data In Stable after SMB					100 300 250 15 45 100	Hz (min) ns (min) ns (min) ns (max) ms (max) ms (max ns (min) ns (min)
t _{LOW} t _{HIGH} t _{F;SMBO} t _{TIMEOUT} t _{SU;DAT}	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10) SMBDAT and SMBCLK Time Low for Res Serial Interface (Note 11) Data In Setup Time to SMBCLK High Data Hold Time: Data In Stable after SME Low					100 300 250 15 45 100 0	Hz (min) ns (min) ns (min) ns (max) ms (max) ms (max ns (min) ns (min)
t _{LOW} t _{HIGH} t _{F;SMBO} t _{TIMEOUT} t _{SU;DAT} t _{HD;DATO}	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10) SMBDAT and SMBCLK Time Low for Res Serial Interface (Note 11) Data In Setup Time to SMBCLK High Data Hold Time: Data In Stable after SME Low Data Hold Time: Data Out Stable after	3CLK				100 300 250 15 45 100 0	Hz (min) ns (min) ns (min) ns (max) ms (max) ms (max) ns (min) ns (min)
t _{LOW} t _{HIGH} t _{F;SMBO} t _{TIMEOUT} t _{SU;DAT} t _{HD;DATO}	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10) SMBDAT and SMBCLK Time Low for Res Serial Interface (Note 11) Data In Setup Time to SMBCLK High Data Hold Time: Data In Stable after SMB Low Data Hold Time: Data Out Stable after SMBCLK Low	BCLK				100 300 300 250 15 45 100 0 30	Hz (min) ns (min) ns (min) ns (max) ms (max) ms (max) ns (min) ns (min)
t _{LOW} t _{HIGH} t _{F;SMBO} t _{TIMEOUT} t _{SU;DAT} t _{HD;DATO}	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10) SMBDAT and SMBCLK Time Low for Res Serial Interface (Note 11) Data In Setup Time to SMBCLK High Data Hold Time: Data In Stable after SMB Low Data Hold Time: Data Out Stable after SMBCLK Low Start Condition SMBDAT Low to SMBCLK	BCLK				100 300 300 250 15 45 100 0 30	Hz (min) ns (min) ns (min) ns (max) ms (max) ms (max) ns (min) ns (min)
t _{LOW} t _{HIGH} t _{F;SMBO} t _{TIMEOUT} t _{SU;DAT} t _{HD;DATO} t _{HD;STA}	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10) SMBDAT and SMBCLK Time Low for Res Serial Interface (Note 11) Data In Setup Time to SMBCLK High Data Hold Time: Data In Stable after SMB Low Data Hold Time: Data Out Stable after SMBCLK Low Start Condition SMBDAT Low to SMBCLH Low (Start condition hold before the first of	3CLK K clock				100 300 300 250 15 45 100 0 30	Hz (min) ns (min) ns (max) ms (max) ms (max) ns (min) ns (min) ns (min) ns (min)
t _{LOW} t _{HIGH} t _{F;SMBO} t _{TIMEOUT} t _{SU;DAT} t _{hD;DATI}	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10) SMBDAT and SMBCLK Time Low for Res Serial Interface (Note 11) Data In Setup Time to SMBCLK High Data Hold Time: Data In Stable after SME Low Data Hold Time: Data Out Stable after SMBCLK Low Start Condition SMBDAT Low to SMBCLK Low (Start condition hold before the first of falling edge)	3CLK K clock				100 300 300 250 15 45 100 0 300 60	Hz (min) ns (min) ns (min) ns (max) ms (max) ms (max ns (min) ns (min) ns (min) ns (min)
t _{LOW} t _{HIGH} t _{F;SMBO} t _{TIMEOUT} t _{SU;DAT} t _{HD;DATO} t _{HD;STA}	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10) SMBDAT and SMBCLK Time Low for Res Serial Interface (Note 11) Data In Setup Time to SMBCLK High Data Hold Time: Data In Stable after SME Low Data Hold Time: Data Out Stable after SMBCLK Low Start Condition SMBDAT Low to SMBCLH Low (Start condition hold before the first of falling edge) Stop Condition SMBCLK High to SMBDAT	3CLK C clock T				100 300 300 250 15 45 100 0 300 60	Hz (min) ns (min) ns (max) ms (max) ms (max) ms (max) ns (min) ns (min) ns (min) ns (min)
t _{LOW} t _{HIGH} t _{F;SMBO} t _{TIMEOUT} t _{SU;DAT} t _{HD;DATO} t _{HD;STA} t _{SU;STO}	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10) SMBDAT and SMBCLK Time Low for Res Serial Interface (Note 11) Data In Setup Time to SMBCLK High Data Hold Time: Data In Stable after SMB Low Data Hold Time: Data Out Stable after SMBCLK Low Start Condition SMBDAT Low to SMBCLK Low (Start condition hold before the first of falling edge) Stop Condition SMBCLK High to SMBDAT Low (Stop Condition Setup)	3CLK C clock T				100 300 300 250 15 45 100 0 30 60 50	Hz (min) ns (min) ns (max) ms (max) ms (max) ms (max) ns (min) ns (min) ns (min) ns (min)
t _{LOW} t _{HIGH} t _{F;SMBO} t _{TIMEOUT} t _{SU;DAT} t _{HD;DATO} t _{HD;STA} t _{SU;STO}	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10) SMBDAT and SMBCLK Time Low for Res Serial Interface (Note 11) Data In Setup Time to SMBCLK High Data Hold Time: Data In Stable after SMB Low Data Hold Time: Data Out Stable after SMBCLK Low Start Condition SMBDAT Low to SMBCLK Low (Start condition hold before the first of falling edge) Stop Condition SMBCLK High to SMBDAT Low (Stop Condition Setup) SMBus Repeated Start-Condition Setup T	3CLK Colock T				100 300 300 250 15 45 100 0 30 60 50	Hz (min) ns (min) ns (max) ms (max) ms (max) ms (max ns (min) ns (min) ns (min) ns (min) ns (min) ns (min)
tLOW tHIGH tF;SMBO tTIMEOUT tSU;DAT tHD;DATO tHD;STA tSU;STO	SMBus Clock Low Time SMBus Clock High Time Output Fall Time (Note 10) SMBDAT and SMBCLK Time Low for Res Serial Interface (Note 11) Data In Setup Time to SMBCLK High Data Hold Time: Data In Stable after SME Low Data Hold Time: Data Out Stable after SMBCLK Low Start Condition SMBDAT Low to SMBCLF Low (Start condition hold before the first of falling edge) Stop Condition SMBCLK High to SMBDAT Low (Stop Condition Setup) SMBUS Repeated Start-Condition Setup T SMBCLK High to SMBDAT Low	3CLK Colock T				100 300 300 250 15 45 100 0 300 60 50 50	Hz (min) ns (min) ns (min) ns (max) ms (max) ns (max)

SMBus Communication



Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 3: When the input voltage (V₁) at any pin exceeds the power supplies (V₁ < GND or V₁ > V_{DD}), the current at that pin should be limited to 5 mA.

Note 4: Reflow temperature profiles are different for lead-free and non-lead-free packages.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor. Machine model, 200 pF discharged directly into each pin.

Note 6: Typicals are at $T_A = 25^{\circ}C$ and represent most likely parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Local temperature accuracy does not include the effects of self-heating. The rise in temperature due to self-heating is the product of the internal power dissipation of the LM73 and the thermal resistance.

Note 9: This specification is provided only to indicate how often temperature data is updated. The LM73 can be read at any time without regard to conversion state (and will yield last conversion result).

Note 10: The output fall time is measured from (V_{IL;MAX} - 0.15V) to (V_{IH;MIN} + 0.15V).

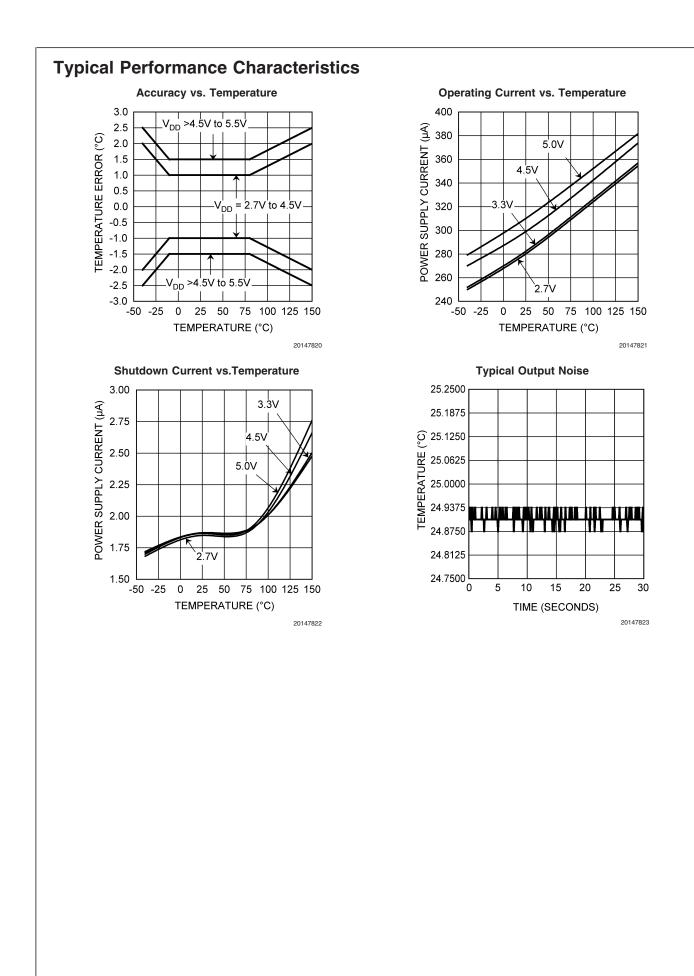
Note 11: Holding the SMBDAT and/or SMBCLK lines Low for a time interval greater than t_{TIMEOUT} will reset the LM73's SMBus state machine, setting SMBDAT and SMBCLK pins to a high impedance state.

Note 12: Represents the time from V_{DD} reaching the power-on-reset level to the LM73 communications being functional. After an additional time equal to one temperature conversion time, valid temperature will be available in the Temperature Register.

Note 13: A write to an invalid pointer address is not allowed. If the master writes an invalid address to the Pointer Register, (1) the LM73 will not acknowledge the address and (2) the Pointer Register will continue to contain the last value stored in it.

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1.0 Functional Description

The LM73 is a digital temperature sensor that senses the temperature of its die using a sigma-delta analog-to-digital converter and stores the temperature in the Temperature Register. The LM73's 2-wire serial interface is compatible with SMBus 2.0 and I²C. Please see the SMBus 2.0 specification for a detailed description of the differences between the I²C bus and SMBus.

The temperature resolution is programmable, allowing the host system to select the optimal configuration between sensitivity and conversion time. The LM73 can be placed in shutdown to minimize power consumption when temperature data is not required. While in shutdown, a 1-shot conversion mode allows system control of the conversion rate for ultimate flexibility.

The LM73 features the following registers. See Section 2.0 for a complete list of the pointer address, content, and reset state of each register.

- 1. Pointer Register
- 2. Temperature Register
- 3. Configuration Register
- 4. T_{HIGH} Register
- 5. T_{LOW} Register
- 6. Control/Status Register
- 7. Identification Register

1.1 POWER-ON RESET

The power-on reset (POR) state is the point at which the supply voltage rises above the power-on reset threshold (specified in the electrical specifications table), generating an internal reset. Each of the registers contains a defined value upon POR and this data remains there until any of the following occurs:

- 1. The first temperature conversion is completed, causing the Temperature Register and various status bits to be updated internally, depending on the value of the measured temperature
- 2. The master writes different data to any R/W bits
- 3. The LM73 is powered down

1.2 ONE-SHOT CONVERSION

The LM73 features a one-shot conversion bit, which is used to initiate a single conversion and comparison cycle when the LM73 is in shutdown mode. While the LM73 is in shutdown mode, writing a "1" to the One-Shot bit in the Configuration Register will cause the LM73 to perform a single temperature conversion and update the Temperature Register and the affected status bits. Operating the LM73 in this one-shot mode allows for extremely low average-power consumption, making it ideal for low-power applications.

When the One-Shot bit is set, the LM73 initiates a temperature conversion. After this initiation, but before the completion of the conversion and resultant register updates, the LM73 is in a "one-shot" state. During this state, the Data Available (DAV) flag in the Control/Status register is "0" and the Temperature Register contains the value 8000h (-256°C). All other registers contain the data that was present before initiating the one-shot conversion. After the temperature measurement is complete, the DAV flag will be set to "1" and the temperature register will contain the resultant measured temperature.

1.3 TEMPERATURE DATA FORMAT

The resolution of the temperature data and the size of the data word are user-selectable through bits RES1 and RES0 in the Control/Status Register. By default, the LM73 temperature stores the measured temperature in an 11-bit (10 bits plus sign) word with one least significant bit (LSB) equal to 0.25°C. The maximum word size is 14 bits (13-bits plus sign) with a resolution of 0.03125 °C/LSB.

CONTF	OL BIT	DATA FORMAT		
RES1	RES0	WORD SIZE	RESOLUTION	
0	0	11 bits	0.25 °C/LSB	
0	1	12 bits	0.125 °C/LSB	
1	0	13 bits	0.0625 °C/LSB	
1	1	14 bits	0.03125 °C/LSB	

The temperature data is reported in 2's complement format. The word is stored in the 16-bit Temperature Register and is left justified in this register. Unused temperature-data bits are always reported as "0".

Temperature	Digital Output		
	Binary	Hex	
+150°C	0100 1011 0000 0000	4B00h	
+25°C	0000 1100 1000 0000	0C80h	
+1°C	0000 0000 1000 0000	0080h	
+0.25°C	0000 0000 0010 0000	0020h	
0°C	0000 0000 0000 0000	0000h	
–0.25°C	1111 1111 1110 0000	FFE0h	
−1°C	1111 1111 1000 0000	FF80h	
–25°C	1111 0011 1000 0000	F380h	
-40°C	1110 1100 0000 0000	EC00h	

11-bit (10-bit plus sign)

12-bit (11-bit plus sign)

Temperature	Digital Output		
	Binary	Hex	
+150°C	0100 1011 0000 0000	4B00h	
+25°C	0000 1100 1000 0000	0C80h	
+1°C	0000 0000 1000 0000	0080h	
+0.125°C	0000 0000 0001 0000	0010h	
0°C	0000 0000 0000 0000	0000h	
–0.125°C	1111 1111 1111 0000	FFF0h	
−1°C	1111 1111 1000 0000	FF80h	
–25°C	1111 0011 1000 0000	F380h	
-40°C	1110 1100 0000 0000	EC00h	

1.0 Functional Description (Continued)

Temperature	Digital Output		
	Binary	Hex	
+150°C	0100 1011 0000 0000	4B00h	
+25°C	0000 1100 1000 0000	0C80h	
+1°C	0000 0000 1000 0000	0080h	
+0.0625°C	0000 0000 0000 1000	0008h	
0°C	0000 0000 0000 0000	0000h	
–0.0625°C	1111 1111 1111 1000	FFF8h	
−1°C	1111 1111 1000 0000	FF80h	
–25°C	1111 0011 1000 0000	F380h	
–40°C	1110 1100 0000 0000	EC00h	

13-bit (12-bit plus sign)

14-bit (13-bit plus sign)

Temperature	Digital Output		
	Binary	Hex	
+150°C	0100 1011 0000 0000	4B00h	
+25°C	0000 1100 1000 0000	0C80h	
+1°C	0000 0000 1000 0000	0080h	
+0.03125°C	0000 0000 0000 0100	0004h	
0°C	0000 0000 0000 0000	0000h	
–0.03125°C	1111 1111 1111 1100	FFFCh	
−1°C	1111 1111 1000 0000	FF80h	
–25°C	1111 0011 1000 0000	F380h	
–40°C	1110 1100 0000 0000	EC00h	

1.4 SMBus INTERFACE

The LM73 operates as a slave on the SMBus. The SMBDAT line is bidirectional. The SMBCLK line is is an input only. The LM73 never drives the SMBCLK line and it does not support clock stretching.

The LM73 uses a 7-bit slave address. It is available in two versions. Each version can be configured for one of three unique slave addresses, for a total of six unique address.

Part Number		Device
Part Number	Address Pin	Address
LM73-0	Float	1001 000
	Ground	1001 001
	V_{DD}	1001 010
LM73-1	Float	1001 100
	Ground	1001 101
	V_{DD}	1001 110

The SMBDAT output is an open-drain output and does not have internal pull-ups. A "high" level will not be observed on this pin until pull-up current is provided by some external source, typically a pull-up resistor. Choice of resistor value depends on many system factors but, in general, the pull-up resistor should be as large as possible without effecting the SMBus desired data rate. This will minimize any internal temperature reading errors due to internal heating of the LM73.

The LM73 features an integrated low-pass filter on both the SMBCLK and the SMBDAT line. These filters increase communications reliability in noisy environments.

If either the SMBCLK or SMBDAT line is held low for a time greater than $t_{TIMEOUT}$ (see Logic Electrical Characteristics for the value of $t_{TIMEOUT}$), the LM73 state machine will reset to the SMBus idle state, releasing the data line. Once the SMBDAT is released high, the master may initiate an SMBus start.

1.5 ALERT FUNCTION

The ALERT output is an over-temperature indicator. At the end of every temperature conversion, the measured temperature is compared to the value in the T_{HIGH} Register. If the measured temperature exceeds the value stored in T_{HIGH} , the ALERT output goes active (see Figure *Figure 1*). This over-temperature condition will also cause the ALRT_STAT bit in the Control/Status Register to change value (this bit mirrors the logic level of the ALERT pin).

The ALERT pin and the ALRT_STAT bit are cleared when any of the following occur:

- 1. The measured temperature falls below the value stored in the ${\rm T}_{\rm LOW}$ Register
- 2. A "1" is written to the ALERT Reset bit in the Configuration Register
- 3. The master resets it through an SMBus Alert Response Address (ARA) procedure

If $\overline{\text{ALERT}}$ has been cleared by the master writing a "1" to the $\overline{\text{ALERT}}$ Reset bit, while the measured temperature still exceeds the T_{HIGH} setpoint, ALERT will go active again after the completion of the next temperature conversion.

Each temperature reading is associated with a Temperature High (THI) and a Temperature Low (TLOW) flag in the Control/Status Register. A digital comparison determines whether that reading is above the T_{HIGH} setpoint or below the T_{LOW} setpoint. If so, the corresponding flag is set. All digital comparisons to the T_{HIGH} , and T_{LOW} values are based on an 11-bit temperature comparison. Regardless of the resolution setting of the LM73, the lower three temperature LSBs will not affect the state of the ALERT output, THI flag, and TLOW flag.

1.0 Functional Description (Continued)

LM73

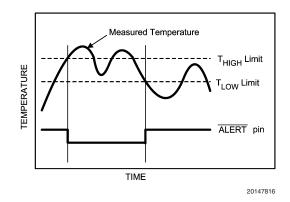
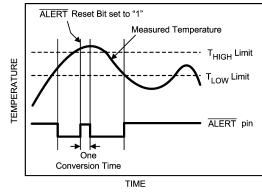


FIGURE 1. ALERT Temperature Response cleared when temperature crosses T_{LOW}



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FIGURE 2. ALERT Temperature Response cleared by writing a "1" to the ALERT Reset Bit.

1.6 COMMUNICATING with the LM73

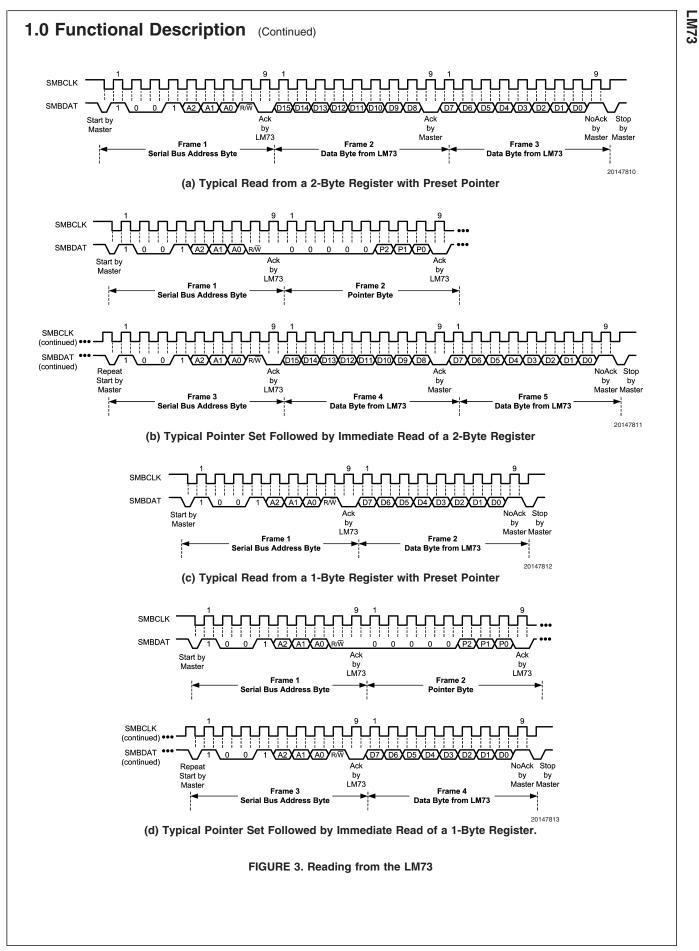
The data registers in the LM73 are selected by the Pointer Register. At power-up the Pointer Register is set to "00h", the location for the Temperature Register. The Pointer Register latches the last location it was set to. Note that all Pointer Register bits are decoded; any incorrect pointer values will not be acknowledged and will not be stored in the Pointer Register (Note 13).

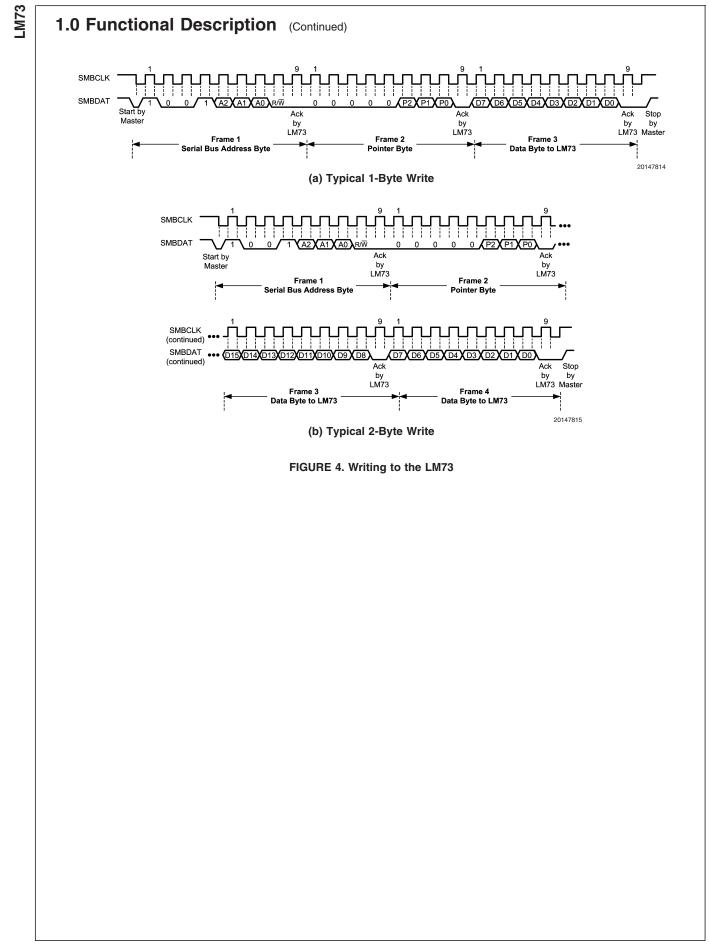
A **Write** to the LM73 will always include the address byte and the pointer byte.

A Read from the LM73 can take place either of two ways:

- If the location latched in the Pointer Register is correct (that is, the Pointer Register is pre-set prior to the read), then the read can simply consist of an address byte, followed by retrieving the data byte. Most of the time it is expected that the Pointer Register will point to Temperature Registers because that will be the data most frequently read from the LM73.
- 2. If the Pointer Register needs to be set, then an address byte, pointer byte, repeat start, and another address byte will accomplish a read.

The data byte is read out of the LM73 by the most significant bit first. At the end of a read, the LM73 can accept either an Acknowledge or No Acknowledge bit from the Master. No Acknowledge is typically used as a signal to the slave that the Master has read its last byte.



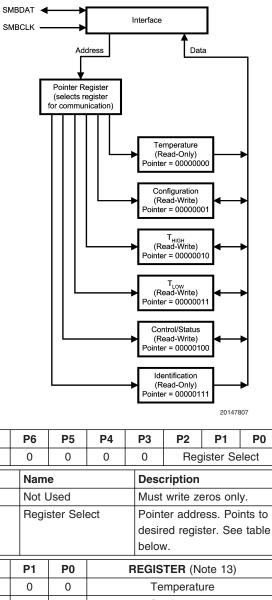


2.0 LM73 Registers

The LM73's internal registers are selected by the Pointer register. The Pointer register latches the last location that it was set to. The pointer register and all internal registers are described below. All registers reset at device power up.

2.1 POINTER REGISTER

The diagram below shows the Pointer Register, the six internal registers to which it points, and their associated pointer addresses.



P2	P1	P0	REGISTER (Note 13)
0	0	0	Temperature
0	0	1	Configuration
0	1	0	T _{HIGH}
0	1	1	T _{LOW}
1	0	0	Control / Status
1	1	1	Identification

P7

0

Bits

7:3

2:0

2.0 LM73 Registers (Continued)

2.2 TEMPERATURE DATA REGISTER

Pointer Address 00h (Read Only) Reset State: 7FFCh (+255.96875°C) One-Shot State: 8000h (-256°C)

D1	5	D14	D13	D12	D11	D10	D9	D8			
SIG	θN	128°C	64°C	32°C	16°C	8°C	4°C	2°C			
D	7	D6	D5	D4	D3	D2	D1	D0			
1°	С	0.5°C	0.25°C	0.125°C	0.0625°C	0.03125°C	reserved	reserved			
Bits	Name		Description								
15:2	Temp	perature Data	Represents the temperature that was measured by the most recent temperature conversion. On Power-up, this data is invalid until the Data Available (DAV) bit in the Control/Status register is high (after the completion of the first temperature conversion). The resolution is user-progammable from 11-bit resolution (0.25°C/LSB) through 14-bit resolution (0.03125°C/LSB). The desired resolution is programmed with bits 5 and 6 of the Control/Status register.								
1:0	Not U	lsed	Return zeros u	ipon read.							

2.3 CONFIGURATION REGISTER

Pointer Address 01h (R/W)

Reset State: 40h

1	D7 D6		D5	D4	D3	D2	D1	D0				
F	PD reserve		ALRT EN	ALRT EN ALRT POL ALRT RST ONE SHOT reserved								
Bits	Name	9	Description	Description								
7	Full Power Down		Writing a 1 to this bit puts the LM73 in shutdown mode for power conservation. Writing a 0 puts the LM73 into normal mode.									
6	reserv	ved	User must writ	e only a 1 to thi	s bit							
5	ALERT Enable		A 0 in this location enables the ALERT output. A 1 disables it. This bit also controls the ALERT Status bit (the Control/Status Register, Bit 3) since that bit reflects the state of the Alert pin.									
4	ALEF	T Polarity	When set to 1, the ALERT pin and ALERT Status bit are active-high. When 0, it is active-low.									
3	ALEF	RT Reset	Writing a 1 to this bit resets the ALERT pin and the ALERT Status bit. It will always be 0 when read.									
2	One Shot		When in shutdown mode (Bit 7 is 1), initiates a single temperature conversion and update of the temperature register with new temperature data. Has no effect when in continuous conversion mode (i.e., when Bit 7 is 0). Always returns a 0 when read.									
1:0	Rese	rved	User must writ	User must write only a 0 to these bits.								

2.4 T_{HIGH} UPPER-LIMIT REGISTER

Pointer Address 02h (R/W)

Reset State: 7FE0h (+255.75°C)

D	15	D14	D13	D12	D11	D10	D9	D8		
SIGN		128°C	64°C	32°C 16°C 8°C 4°C				2°C		
D)7	D6	D5	D4	D3	D2	D1	D0		
1°C		0.5°C	0.25°C	reserved						
Bits	Name)	Description	Description						
15:5	1	r-Limit erature	If the measured temperature that is stored in this register exceeds this user-programmable upper temperature limit, the ALERT pin will go active and the THIGH flag in the Control/Status register will be set to 1. Two's complement format.							
4:0	0 Reserved Returns zeros upon read. Recommend writing zeros only in these bits.									

2.0 LM73 Registers (Continued)

2.5 T_{LOW} LOWER-LIMIT REGISTER

Pointer Address 03h (R/W)

Reset State: 8000h (-256°C)

D15		D14	D13	D12	D11	D10	D9	D8		
SIGN		128°C	64°C	32°C 16°C 8°C 4°C		4°C	2°C			
D7		D6	D5	D4 D3 D2		D2	D1	D0		
1°C		0.5°C	0.25°C	reserved						
Bits	Name)	Description							
15:5	Lowe	r-Limit	If the measured temperature that is stored in the temperature register falls below this							
	Temperature		user-programmable lower temperature limit, the $\overline{\text{ALERT}}$ pin will be deactivated and the T _{LOW}							
			flag in the Control/Status register will be set to 1. Two's complement format.							
4:0 Reserved			Returns zeros upon read. Recommend writing zeros only in these bits.							

2.6 CONTROL/STATUS REGISTER

Pointer Address 04h (R/W)

Reset State: 08h

D7		D6	D5	D4	D3	D2	D1	D0		
TO	TO_DIS RES1		RES0 reserved ALRT_STAT THI TLOW DAV							
Bits	Name	e	Description	Description						
7	Time	-Out Disable	Disable the tim	ne-out feature or	n the SMBDAT a	and SMBCLK lir	nes if set to 1. Se	tting this bit		
			turns off the bu	us-idle timers, e	nabling the LM7	3 to operate at	lowest shutdown	current.		
6:5	Temp	perature	Selects one of	four user-progr	ammable temper	ature data reso	olutions			
	Reso	lution	00: 0.25°C/LSE	B, 11-bit word (1	0 bits plus sign)					
			01: 0.125°C/LS	B, 12-bit word	(11 bits plus sigr	ı)				
			10: 0.0625°C/L	SB, 13-bit word	l (12 bits plus sig	jn)				
			11: 0.03125°C	LSB, 14-bit wor	rd (13 bits plus s	ign)				
4	reser	ved	Always returns	zero when rea	d. Recommend o	customer write a	zero only.			
3	ALEF	RT Pin Status					T output is high.			
			output is reset under any of the following conditions: (1) Cleared by writing a 1 to the ALERT							
			Reset bit in the configuration register, (2) Measured temperature falls below the T_{LOW} limit,							
			or (3) cleared via the ARA sequence. Recommend customer write zero only.							
2	Temperature High		Bit is set to 1 when the measured temperature exceeds the $T_{\mbox{\scriptsize HIGH}}$ limit stored in the							
	Flag		programmable T_{HIGH} register. Flag is reset to 0 when both of the following conditions are							
			met: (1) measured temperature no longer exceeds the programmed T_{HIGH} limit and (2) upon							
			reading the Control/Status register. If the temperature is not longer above the T _{HIGH} limit, this							
			status bit remains set until it is read by the master so that the system can check the history							
			of what caused the $\overline{\text{ALERT}}$ output to go active. This bit is not cleared after every read if the measured temperature is still above the T _{HIGH} limit.							
1	Temperature Low Flag		Bit is set to 1 when the measured temperature falls below the T_{LOW} limit stored in the							
			programmable T_{LOW} register. Flag is reset to 0 when both of the following conditions are							
			met: (1) measured temperature is no longer below the programmed T_{LOW} limit and (2) upon							
			reading the Control/Status register. If the temperature is no longer below the T_{LOW} limit, the status bit remains set until it is read by the master so that the system can check the history							
			of what cause the ALERT output to go active. This bit is not cleared after every read if							
			temperature is still below T _{LOW} limit.							
0	Data Available Flag									
0			This bit is 0 when the LM73 is in the process of converting a new temperature. It is 1 when the conversion is done. After initiating a temperature conversion while operating in the							
							nen the conversion	-		
							erature register is			
			00 0				power-up, the L			
			U U		•	,	mode (the defaul			
				t) this bit will alv						

LM73

2.0 LM73 Registers (Continued)

2.7 IDENTIFICATION REGISTER

Pointer Address 07h (Read Only)

Reset State: 0190h

D15		D14	D13	D12	D11	D10	D9	D8	
C)	0	0	0	0	0	0	1	
D	7 D6		D5	D4	D3	D2	D1	D0	
1		0	0	1	0	0			
Bits	Name Description								
15:8		facturer fication Byte	Always returns 01h to uniquely identify the manufacturer as National Semiconductor Corporation.						
7:4	Product Identification Nibble		Always returns 9h to uniquely identify this part as the LM73 Temperature Sensor.						
		Always returns	Oh to uniquely	identify the revis	sion as level zero	р.			

3.0 Application Hints

3.1 THERMAL PATH CONSIDERATIONS

To get the expected results when measuring temperature with an integrated circuit temperature sensor like the LM73, it is important to understand that the sensor measures its own die temperature. For the LM73, the best thermal path between the die and the outside world is through the LM73's pins. In the SOT23 package, all the pins on the LM73 will have an equal effect on the die temperature. Because the pins represent a good thermal path to the LM73 die, the LM73 will provide an accurate measurement of the temperature of the printed circuit board on which it is mounted. There is a less efficient thermal path between the plastic package and the LM73 die. If the ambient air temperature is significantly different from the printed circuit board temperature, it will have a small effect on the measured temperature.

3.2 OUTPUT CONSIDERATIONS: TIGHT ACCURACY, RESOLUTION AND LOW NOISE

The LM73 is well suited for applications that require tight temperature measurement accuracy. In many applications, the low temperature error can mean better system performance and, by eliminating a system calibration step, lower production cost.

With digital resolution as fine as 0.03125 °C/LSB, the LM73 senses and reports very small changes in its temperature, making it ideal for applications where temperature sensitivity is important. For example, the LM73 enables the system to quickly identify the direction of temperature change, allowing the processor to take compensating action before the system reaches a critical temperature.

The LM73 has very low output noise, typically 0.015°C rms, which makes it ideal for applications where stable thermal compensation is a priority. For example, in a temperature-compensated oscillator application, the very small deviation in successive temperature readings translates to a stable frequency output from the oscillator.

