5 Volt, Byte Alterable E^{2}PROM

FEATURES

- **55ns Access Time**
- **Simple Byte and Page Write**
  - **Single 5V Supply**
    - **No External High Voltages or V$_{PP}$ Control Circuits**
  - **Self-Timed**
    - **No Erase Before Write**
    - **No Complex Programming Algorithms**
    - **No Overerase Problem**
- **Low Power CMOS**
  - **40 mA Active Current Max.**
  - **200 μA Standby Current Max.**
- **Fast Write Cycle Times**
  - **64 Byte Page Write Operation**
  - **Byte or Page Write Cycle: 2ms Typical**
  - **Complete Memory Rewrite: 0.25 sec. Typical**
  - **Effective Byte Write Cycle Time: 32μs Typical**
- **Software Data Protection**
- **End of Write Detection**
  - **$\overline{\text{DATA}}$ Polling**
  - **Toggle Bit**

- **High Reliability**
  - **Endurance: 100,000 Cycles**
  - **Data Retention: 100 Years**
- **JEDEC Approved Byte-Wide Pinout**

DESCRIPTION

The X28HC64 is an 8K x 8 E^{2}PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28HC64 is a 5V only device. The X28HC64 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28HC64 supports a 64-byte page write operation, effectively providing a 32μs/byte write cycle and enabling the entire memory to be typically written in 0.25 seconds. The X28HC64 also features $\overline{\text{DATA}}$ Polling and Toggle Bit Polling, two methods providing early end of write detection. In addition, the X28HC64 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E^{2}PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.
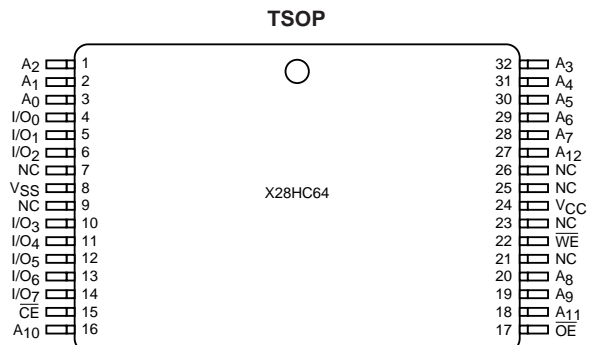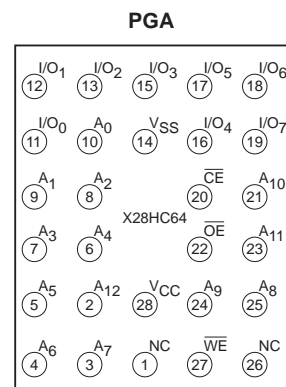
PIN CONFIGURATIONS
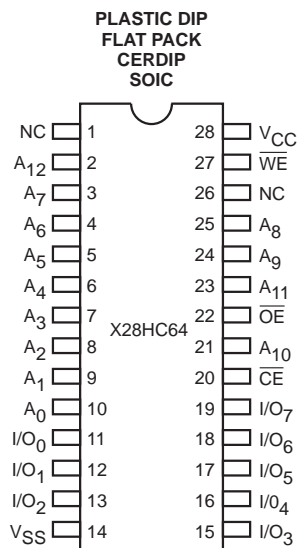
3857 FHD F02.1

3857 FHD F03

3857 ILL F22

3857 FHD F04

Characteristics subject to change without notice
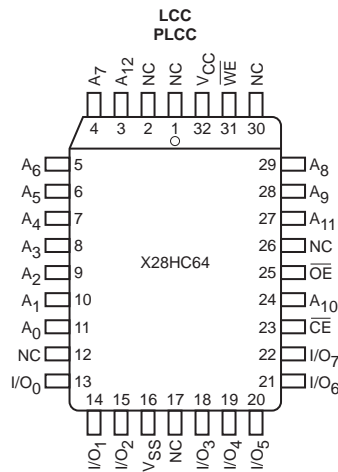
X28HC64

PIN DESCRIPTIONS

Addresses (A$_0$–A$_{12}$)

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O$_0$–I/O$_7$)

Data is written to or read from the X28HC64 through the I/O pins.
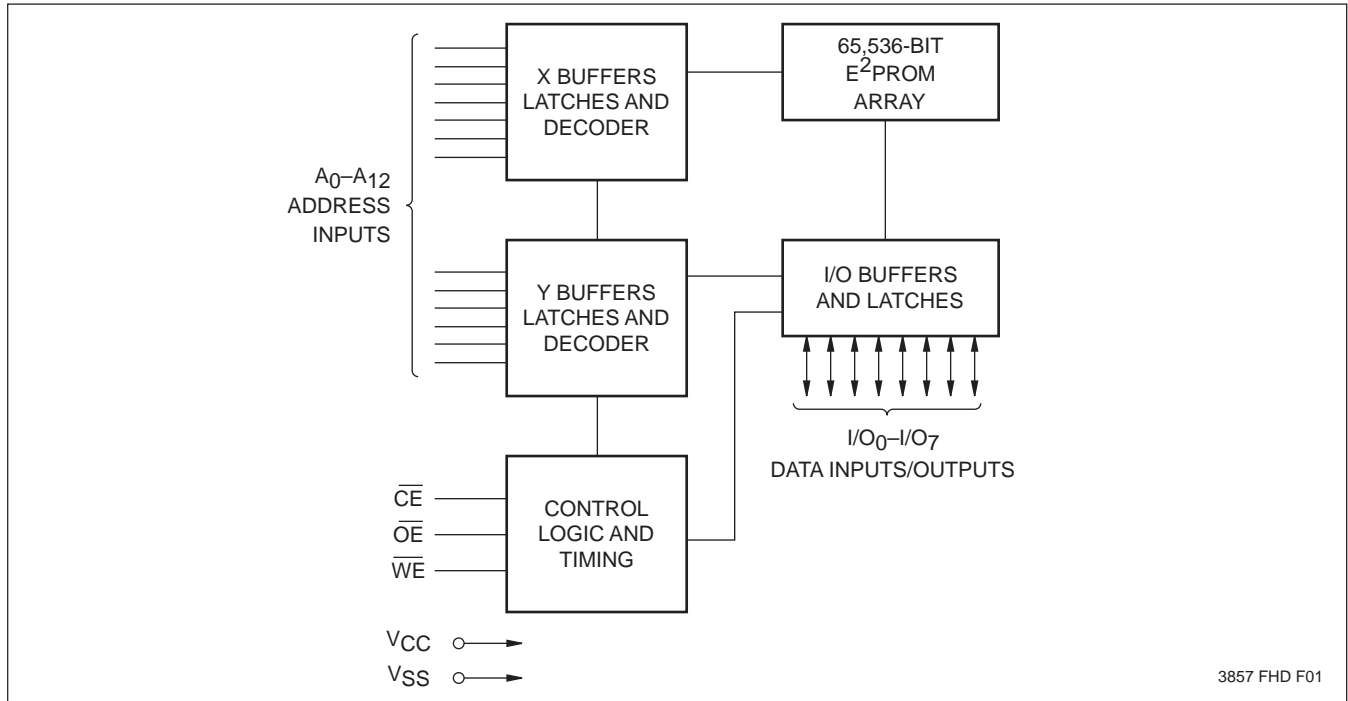
Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X28HC64.

PIN NAMES

Symbol	Description
A$_0$–A$_{12}$	Address Inputs
I/O$_0$–I/O$_7$	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V$_{CC}$	+5V
V$_{SS}$	Ground
NC	No Connect

3857 PGM T01

FUNCTIONAL DIAGRAM

3857 FHD F01

2