NEC

MOS INTEGRATED CIRCUIT

# μPD720113

## USB 2.0 HUB CONTROLLER

The μPD720113 is a USB 2.0 hub device that complies with the Universal Serial Bus (USB) Specification Revision 2.0 and works up to 480 Mbps. USB 2.0 compliant transceivers are integrated for upstream and all downstream ports. The μPD720113 works backward compatible either when any one of the downstream ports is connected to a USB 1.1 compliant device, or when the upstream port is connected to a USB 1.1 compliant host.

**Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.**
**μPD720113 User's Manual: S16619E**

### FEATURES

- Compliant with Universal Serial Bus Specification Revision 2.0 (Data Rate 1.5/12/480 Mbps)
- Certified by USB implementers forum and granted the USB 2.0 high-speed Logo
- High-speed or full-speed packet protocol sequencer for Endpoint 0/1
- 7 (Max.) downstream facing ports
- All downstream facing ports can handle high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction.
- Supports split transaction to handle full-speed and low-speed transaction on downstream facing ports when Hub controller is working in high-speed mode.
- One Transaction Translator per Hub and supports four non-periodic buffers
- Support self-powered mode
- Supports Over-current detection and Individual or ganged power control
- Supports configurable vendor ID, product ID, string descriptors and others with external Serial ROM
- Supports "non-removable" attribution on individual port
- Uses 30 MHz X'tal, or clock input
- 2.5 V and 3.3 V power supplies



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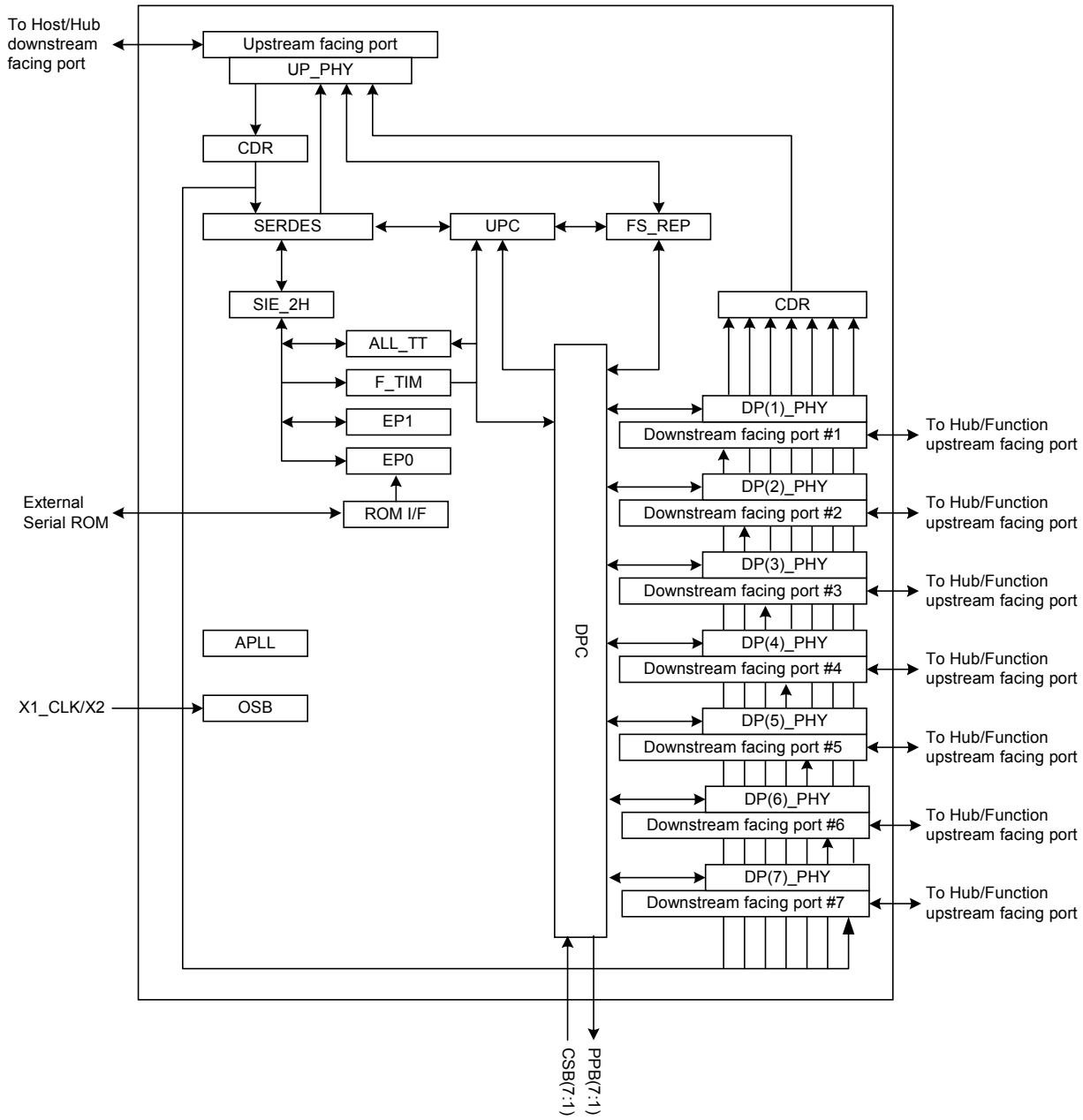
**The mark ★ shows major revised points.**

## ORDERING INFORMATION

| Part Number | Package | Remark |
|---|---|---|
| μPD720113GK-9EU | 80-pin plastic TQFP (Fine pitch) (12 × 12) | |
| ★ μPD720113GK-9EU-A | 80-pin plastic TQFP (Fine pitch) (12 × 12) | Lead-free product |

## BLOCK DIAGRAM



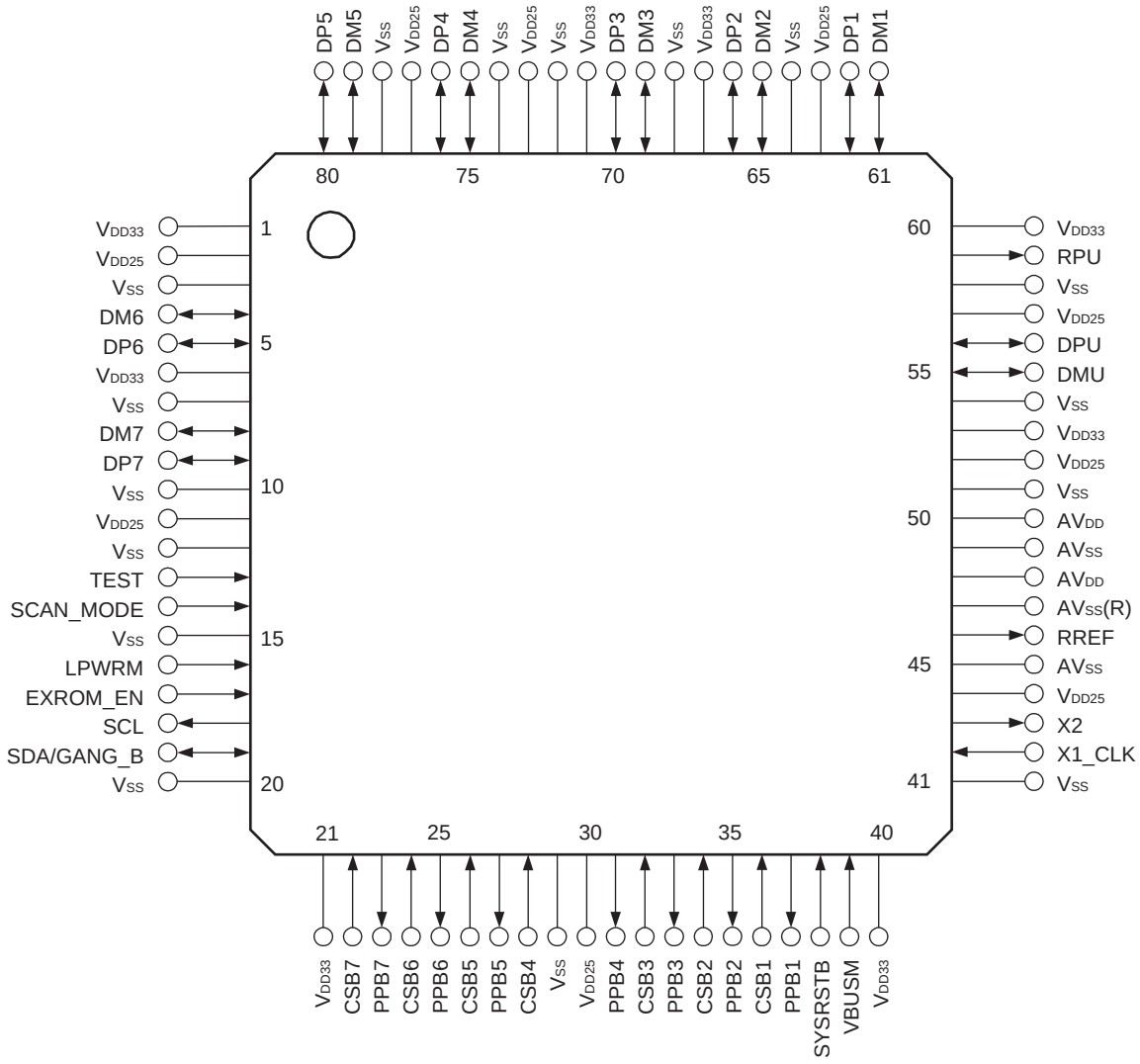
| | | |
|---|---|---|
| APLL | : | Generates all clocks of Hub. |
| ALL_TT | : | Translates the high-speed transactions (split transactions) for full/low-speed device to full/low-speed transactions. ALL_TT buffers the data transfer from either upstream or downstream direction. For OUT transaction, ALL_TT buffers data from upstream port and sends it out to the downstream facing ports after speed conversion from high-speed to full/low-speed. For IN transaction, ALL_TT buffers data from downstream ports and sends it out to the upstream facing ports after speed conversion from full/low-speed to high-speed. |
| CDR | : | Data & clock recovery circuit |
| DPC | : | Downstream Port Controller handles Port Reset, Enable, Disable, Suspend and Resume |
| DP(n)_PHY | : | Downstream transceiver supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction |
| EP0 | : | Endpoint 0 controller |
| EP1 | : | Endpoint 1 controller |
| F_TIM (Frame Timer) | : | Manages hub's synchronization by using micro-SOF which is received at upstream port, and generates SOF packet when full/low-speed device is attached to downstream facing port. |
| FS_REP | : | Full/low-speed repeater is enabled when the μPD720113 are worked at full-speed mode |
| OSB | : | Oscillator Block |
| ROM I/F | : | Interface block for external Serial ROM which contains user-defined descriptors |
| SERDES | : | Serializer and Deserializer |
| SIE_2H | : | Serial Interface Engine (SIE) controls USB2.0 and 1.1 protocol sequencer. |
| UP_PHY | : | Upstream Transceiver supports high-speed (480 Mbps), full-speed (12 Mbps) transaction |
| UPC | : | Upstream Port Controller handles Suspend and Resume |

## PIN CONFIGURATION (TOP VIEW)

- **80-pin plastic TQFP (Fine pitch) (12 × 12)**

μPD720113GK-9EU

★ μPD720113GK-9EU-A



| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---|---|---|---|---|---|---|---|
| 1 | $V_{DD33}$ | 21 | $V_{DD33}$ | 41 | $V_{SS}$ | 61 | DM1 |
| 2 | $V_{DD25}$ | 22 | CSB7 | 42 | X1_CLK | 62 | DP1 |
| 3 | $V_{SS}$ | 23 | PPB7 | 43 | X2 | 63 | $V_{DD25}$ |
| 4 | DM6 | 24 | CSB6 | 44 | $V_{DD25}$ | 64 | $V_{SS}$ |
| 5 | DP6 | 25 | PPB6 | 45 | $AV_{SS}$ | 65 | DM2 |
| 6 | $V_{DD33}$ | 26 | CSB5 | 46 | RREF | 66 | DP2 |
| 7 | $V_{SS}$ | 27 | PPB5 | 47 | $AV_{SS}$(R) | 67 | $V_{DD33}$ |
| 8 | DM7 | 28 | CSB4 | 48 | $AV_{DD}$ | 68 | $V_{SS}$ |
| 9 | DP7 | 29 | $V_{SS}$ | 49 | $AV_{SS}$ | 69 | DM3 |
| 10 | $V_{SS}$ | 30 | $V_{DD25}$ | 50 | $AV_{DD}$ | 70 | DP3 |
| 11 | $V_{DD25}$ | 31 | PPB4 | 51 | $V_{SS}$ | 71 | $V_{DD33}$ |
| 12 | $V_{SS}$ | 32 | CSB3 | 52 | $V_{DD25}$ | 72 | $V_{SS}$ |
| 13 | TEST | 33 | PPB3 | 53 | $V_{DD33}$ | 73 | $V_{DD25}$ |
| 14 | SCAN_MODE | 34 | CSB2 | 54 | $V_{SS}$ | 74 | $V_{SS}$ |
| 15 | $V_{SS}$ | 35 | PPB2 | 55 | DMU | 75 | DM4 |
| 16 | LPWRM | 36 | CSB1 | 56 | DPU | 76 | DP4 |
| 17 | EXROM_EN | 37 | PPB1 | 57 | $V_{DD25}$ | 77 | $V_{DD25}$ |
| 18 | SCL | 38 | SYSRSTB | 58 | $V_{SS}$ | 78 | $V_{SS}$ |
| 19 | SDA/GANG_B | 39 | VBUSM | 59 | RPU | 79 | DM5 |
| 20 | $V_{SS}$ | 40 | $V_{DD33}$ | 60 | $V_{DD33}$ | 80 | DP5 |

**Remark** $AV_{SS}$(R) should be used to connect RREF through 1 % precision reference resistor of 2.43 kΩ.

## 1. PIN INFORMATION

| Pin Name | I/O | Buffer Type | Active Level | Function |
|---|---|---|---|---|
| X1_CLK | I | 2.5 V Input | | Crystal oscillator in or clock input |
| X2 | O | 2.5 V Output | | Oscillator out |
| SYSRSTB | I | 5 V tolerant Schmitt Input | Low | Asynchronous chip reset |
| RPU | A (O) | USB Pull-up control | | External 1.5 kΩ pull-up resistor control |
| DP(7:1) | I/O | USB D+ signal I/O | | USB's downstream facing port D+ signal |
| DM(7:1) | I/O | USB D– signal I/O | | USB's downstream facing port D– signal |
| DPU | I/O | USB D+ signal I/O | | USB's upstream facing port D+ signal |
| DMU | I/O | USB D– signal I/O | | USB's upstream facing port D– signal |
| LPWRM | I | 3.3 V Schmitt Input | | Local power monitor |
| RREF | A (O) | Analog | | Reference resistor |
| CSB(7:1) | I | 5 V tolerant Input | Low | Port's over-current status input |
| PPB(7:1) | O | 5 V tolerant N-ch open drain | Low | Port's power supply control output |
| VBUSM | I | 5 V tolerant Schmitt input | | $V_{BUS}$ monitor |
| SCL | O | 3.3 V Output | | External serial ROM clock out |
| SDA/GANG_B | I/O | 3.3 V Schmitt I/O | | External serial ROM data IO or power management mode select |
| EXROM_EN | I | 3.3 V Schmitt Input | | External serial ROM input enable |
| TEST | I | 3.3 V Input | | Test signal |
| SCAN_MODE | I | 3.3 V Input | | Test signal |
| $V_{DD33}$ | | | | 3.3 V $V_{DD}$ |
| $V_{DD25}$ | | | | 2.5 V $V_{DD}$ |
| $AV_{DD}$ | | | | 2.5 V $V_{DD}$ for analog circuit |
| $V_{SS}$ | | | | $V_{SS}$ |
| $AV_{SS}$ | | | | $V_{SS}$ for analog circuit |
| $AV_{SS}$(R) | | | | $V_{SS}$ for reference resistor. Connect to $AV_{SS}$. |

**Remark** "5 V tolerant" means that the buffer is 3 V buffer with 5 V tolerant circuit.

## 2. ELECTRICAL SPECIFICATIONS

### 2.1 Buffer List

- 2.5 V Oscillator interface
  X1_CLK, X2
- 5 V Schmitt input buffer
  SYSRSTB, CSB(7:1), VBUSM
- 3.3 V Schmitt input buffer
  LPWRM
- 3.3 V input buffer
  EXROM_EN, TEST, SCAN_MODE
- 3.3 V $I_{OL}$ = 3 mA bi-directional Schmitt input buffer with input enable (OR-type)
  SDA/GANG_B
- 3.3 V $I_{OL}$ = 3 mA output buffer
  SCL
- 5 V $I_{OL}$ = 12 mA N-ch open drain buffer
  PPB(7:1)
- USB2.0 interface
  RPU, DPU, DMU, DP(7:1), DM(7:1), RREF

Above, “5 V” refers to a 3 V input buffer that is 5 V tolerant (has 5 V maximum input voltage). Therefore, it is possible to have a 5 V connection for an external bus.

## 2.2 Terminology

**Terms Used in Absolute Maximum Ratings**

| Parameter | Symbol | Meaning |
|---|---|---|
| Power supply voltage | $V_{DD33}$<br>$V_{DD25}$<br>$AV_{DD}$ | Indicates voltage range within which damage or reduced reliability will not result when power is applied to a $V_{DD}$ pin. |
| Input voltage | $V_I$ | Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin. |
| Output voltage | $V_O$ | Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin. |
| Output current | $I_O$ | Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when current flows out of or into an output pin. |
| Operating temperature | $T_A$ | Indicates the ambient temperature range for normal logic operations. |
| Storage temperature | $T_{stg}$ | Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device. |

**Terms Used in Recommended Operating Range**

| Parameter | Symbol | Meaning |
|---|---|---|
| Power supply voltage | $V_{DD33}$<br>$V_{DD25}$<br>$AV_{DD}$ | Indicates the voltage range for normal logic operations to occur when $V_{SS}$ = 0 V. |
| High-level input voltage | $V_{IH}$ | Indicates the voltage, applied to the input pins of the device, which indicates the high level state for normal operation of the input buffer.<br>* If a voltage that is equal to or greater than the “MIN.” value is applied, the input voltage is guaranteed as high level voltage. |
| Low-level input voltage | $V_{IL}$ | Indicates the voltage, applied to the input pins of the device, which indicates the low level state for normal operation of the input buffer.<br>* If a voltage that is equal to or less than the “MAX.” value is applied, the input voltage is guaranteed as low level voltage. |
| Hysteresis voltage | $V_H$ | Indicates the differential between the positive trigger voltage and the negative trigger voltage. |
| Input rise time | $t_{ri}$ | Indicates allowable input signal transition time from $0.1 \times V_{DD}$ to $0.9 \times V_{DD}$. |
| Input fall time | $t_{fi}$ | Indicates allowable input signal transition time from $0.9 \times V_{DD}$ to $0.1 \times V_{DD}$. |

**Terms Used in DC Characteristics**

| Parameter | Symbol | Meaning |
|---|---|---|
| Off-state output leakage current | $I_{OZ}$ | Indicates the current that flows into a 3-state output pin when it is in a high-impedance state and a voltage is applied to the pin. |
| Output short circuit current | $I_{OS}$ | Indicates the current that flows from an output pin when it is shorted to GND while it is at high-level. |
| Input leakage current | $I_I$ | Indicates the current that flows into an input pin when a voltage is applied to the pin. |
| Low-level output current | $I_{OL}$ | Indicates the current that can flow into an output pin in the low-level state without raising the output voltage above the specified $V_{OL}$. |
| High-level output current | $I_{OH}$ | Indicates the current that can flow out of an output pin in the high-level state without reducing the output voltage below the specified $V_{OH}$. (A negative current indicates current flowing out of the pin.) |

## 2.3 Electrical Specifications

**Absolute Maximum Ratings**

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power supply voltage | $V_{DD33}$ | | −0.5 to +4.6 | V |
| | $V_{DD25}$ | | −0.5 to +3.6 | V |
| | $AV_{DD}$ | | −0.5 to +3.6 | V |
| Input/output voltage | $V_I/V_O$ | | | |
| 2.5 V input/output voltage | | 2.3 V ≤ $V_{DD25}$ ≤ 2.7 V<br>$V_I/V_O$ < $V_{DD25}$ + 0.9 V | −0.5 to +3.6 | V |
| 3.3 V input/output voltage | | 3.0 V ≤ $V_{DD33}$ ≤ 3.6 V<br>$V_I/V_O$ < $V_{DD33}$ + 1.0 V | −0.5 to +4.6 | V |
| 5 V input/out voltage | | 3.0 V ≤ $V_{DD33}$ ≤ 3.6 V<br>$V_I/V_O$ < $V_{DD33}$ + 3.0 V | −0.5 to +6.6 | V |
| Output current | $I_O$ | $I_{OL}$ = 3 mA<br>$I_{OL}$ = 6 mA<br>$I_{OL}$ = 12 mA | 10<br>20<br>40 | mA<br>mA<br>mA |
| Operating temperature | $T_A$ | | 0 to +70 | °C |
| Storage temperature | $T_{stg}$ | | −65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.**

**Recommended Operating Ranges**

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Operating voltage | $V_{DD33}$ | 3.3 V for $V_{DD33}$ pins | 3.14 | 3.30 | 3.46 | V |
| | $V_{DD25}$ | 2.5 V for $V_{DD25}$ pins | 2.3 | 2.5 | 2.7 | V |
| | $AV_{DD}$ | 2.5 V for $AV_{DD}$ pins | 2.3 | 2.5 | 2.7 | V |
| High-level input voltage | $V_{IH}$ | | | | | |
| 2.5 V High-level input voltage | | | 1.7 | | $V_{DD25}$ | V |
| 3.3 V High-level input voltage | | | 2.0 | | $V_{DD33}$ | V |
| 5.0 V High-level input voltage | | | 2.0 | | 5.5 | V |
| Low-level input voltage | $V_{IL}$ | | | | | |
| 2.5 V Low-level input voltage | | | 0 | | 0.7 | V |
| 3.3 V Low-level input voltage | | | 0 | | 0.8 | V |
| 5.0 V Low-level input voltage | | | 0 | | 0.8 | V |
| Hysteresis voltage | $V_H$ | | | | | |
| 5 V Hysteresis voltage | | | 0.3 | | 1.5 | V |
| 3.3 V Hysteresis voltage | | | 0.2 | | 1.0 | V |
| Input rise time for SYSRSTB | $t_{rst}$ | | | | 10 | ms |
| Input rise time | $t_{ri}$ | | | | | |
| Normal buffer | | | 0 | | 200 | ns |
| Schmitt buffer | | | 0 | | 10 | ms |
| Input fall time | $t_{fi}$ | | | | | |
| Normal buffer | | | 0 | | 200 | ns |
| Schmitt buffer | | | 0 | | 10 | ms |

**Two power supply rails limitation.**

The μPD720113 has two power supply rails (2.5 V, 3.3 V). The system will require the time when power supply rail is stable at $V_{DD}$ level. And, there will be difference between the time of $V_{DD25}$ and $V_{DD33}$. The μPD720113 requires that $V_{DD25}$ should be stable before $V_{DD33}$ becomes stable. At any case, the system must ensure that the absolute maximum ratings for $V_I$ /$V_O$ are not exceeded. System reset signaling should be asserted more than specified time after both $V_{DD25}$ and $V_{DD33}$ are stable.

**DC Characteristics**

| Parameter | Symbol | Condition | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Off-state output leakage current | $I_{OZ}$ | $V_O = V_{DD33}, V_{DD25}$ or $V_{SS}$ | | ±10 | μA |
| Output short circuit current | $I_{OS}$ Note | | | −250 | mA |
| Low-level output current | $I_{OL}$ | | | | |
| 3.3 V low-level output current | | $V_{OL}$ = 0.4 V | 3 | | mA |
| 3.3 V low-level output current | | $V_{OL}$ = 0.4 V | 6 | | mA |
| 5.0 V low-level output current | | $V_{OL}$ = 0.4 V | 12 | | mA |
| High-level output current | $I_{OH}$ | | | | |
| 3.3 V high-level output current | | $V_{OH}$ = 2.4 V | −3 | | mA |
| 3.3 V high-level output current | | $V_{OH}$ = 2.4 V | −6 | | mA |
| 5.0 V high-level output current | | $V_{OH}$ = 2.4 V | −2 | | mA |
| Input leakage current | $I_I$ | | | | |
| 3.3 V buffer | | $V_I = V_{DD}$ or $V_{SS}$ | | ±10 | μA |
| 5.0 V buffer | | $V_I = V_{DD}$ or $V_{SS}$ | | ±10 | μA |

**Note** The output short circuit time is measured at one second or less and is tested with only one pin on the LSI.

**USB Interface Block**

| Parameter | Symbol | Conditions | MIN | MAX | Unit |
|---|---|---|---|---|---|
| Output pin impedance | $Z_{HSDRV}$ | Includes $R_S$ resistor | 40.5 | 49.5 | Ω |
| Bus pull-up resistor on upstream facing port | $R_{PU}$ | | 1.425 | 1.575 | kΩ |
| Bus pull-up resistor on downstream facing port | $R_{PD}$ | | 14.25 | 15.75 | kΩ |
| Termination voltage for upstream facing port pullup (full-speed) | $V_{TERM}$ | | 3.0 | 3.6 | V |
| **Input Levels for Low-/full-speed:** | | | | | |
| High-level input voltage (drive) | $V_{IH}$ | | 2.0 | | V |
| High-level input voltage (floating) | $V_{IHZ}$ | | 2.7 | 3.6 | V |
| Low-level input voltage | $V_{IL}$ | | | 0.8 | V |
| Differential input sensitivity | $V_{DI}$ | $\lvert(D+) - (D-)\rvert$ | 0.2 | | V |
| Differential common mode range | $V_{CM}$ | Includes $V_{DI}$ range | 0.8 | 2.5 | V |
| **Output Levels for Low-/full-speed:** | | | | | |
| High-level output voltage | $V_{OH}$ | $R_L$ of 14.25 kΩ to GND | 2.8 | 3.6 | V |
| Low-level output voltage | $V_{OL}$ | $R_L$ of 1.425 kΩ to 3.6 V | 0.0 | 0.3 | V |
| SE1 | $V_{OSE1}$ | | 0.8 | | V |
| Output signal crossover point voltage | $V_{CRS}$ | | 1.3 | 2.0 | V |
| **Input Levels for High-speed:** | | | | | |
| High-speed squelch detection threshold (differential signal) | $V_{HSSQ}$ | | 100 | 150 | mV |
| High-speed disconnect detection threshold (differential signal) | $V_{HSDSC}$ | | 525 | 625 | mV |
| High-speed data signaling common mode voltage range | $V_{HSCM}$ | | −50 | +500 | mV |
| High-speed differential input signaling levels | See Figure 2-4. | | | | |
| **Output Levels for High-speed:** | | | | | |
| High-speed idle state | $V_{HSOI}$ | | −10.0 | +10 | mV |
| High-speed data signaling high | $V_{HSOH}$ | | 360 | 440 | mV |
| High-speed data signaling low | $V_{HSOL}$ | | −10.0 | +10 | mV |
| Chirp J level (different signal) | $V_{CHIRPJ}$ | | 700 | 1100 | mV |
| Chirp K level (different signal) | $V_{CHIRPK}$ | | −900 | −500 | mV |

**Figure 2-1. Differential Input Sensitivity Range for Low-/full-speed**

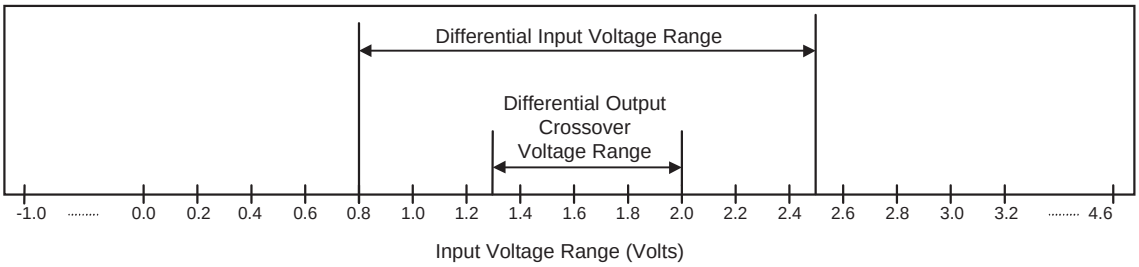



**Figure 2-2. Full-speed Buffer $V_{OH}/I_{OH}$ Characteristics for High-speed Capable Transceiver**

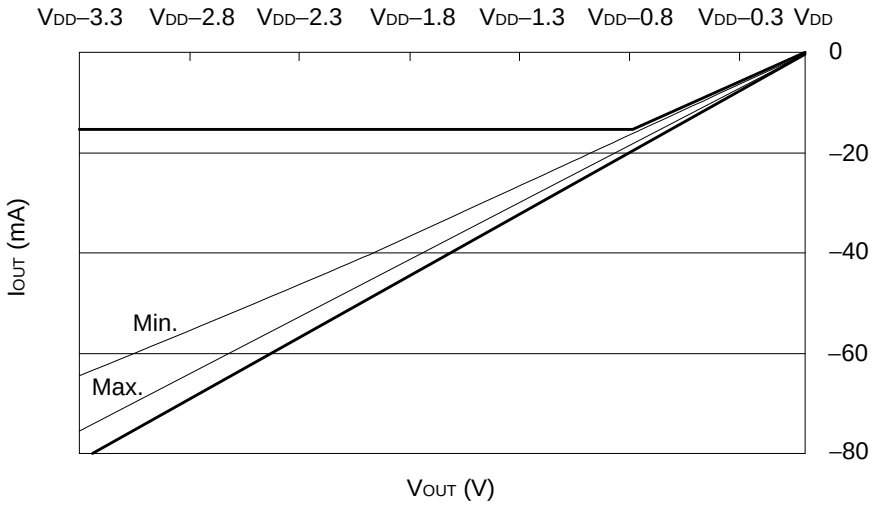



**Figure 2-3. Full-speed Buffer $V_{OL}/I_{OL}$ Characteristics for High-speed Capable Transceiver**

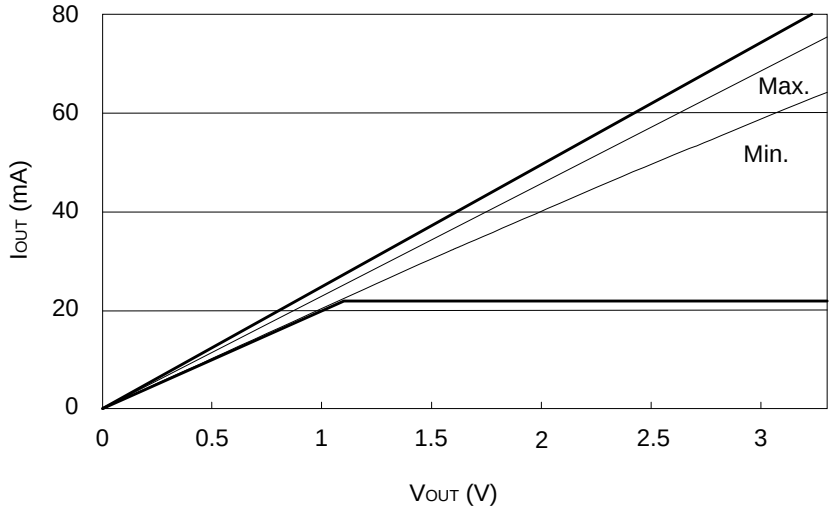


**Figure 2-4. Receiver Sensitivity for Transceiver at DP/DM**

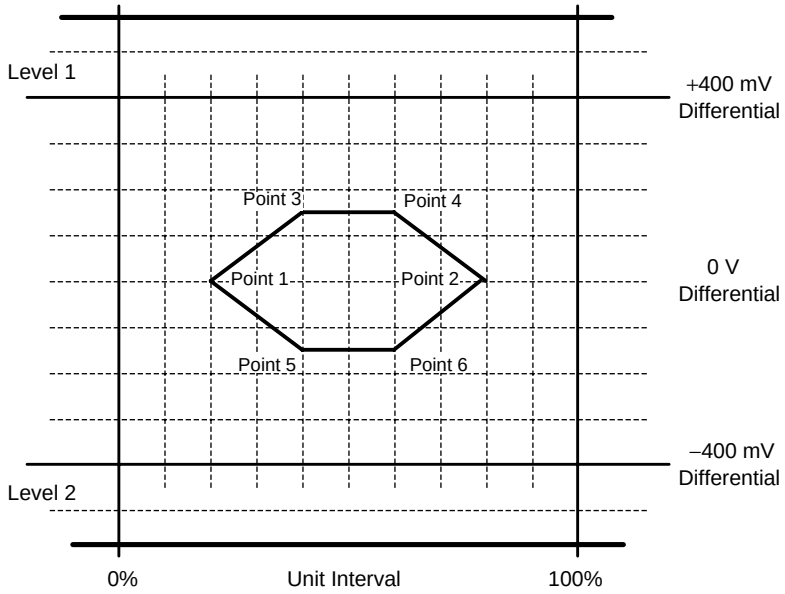
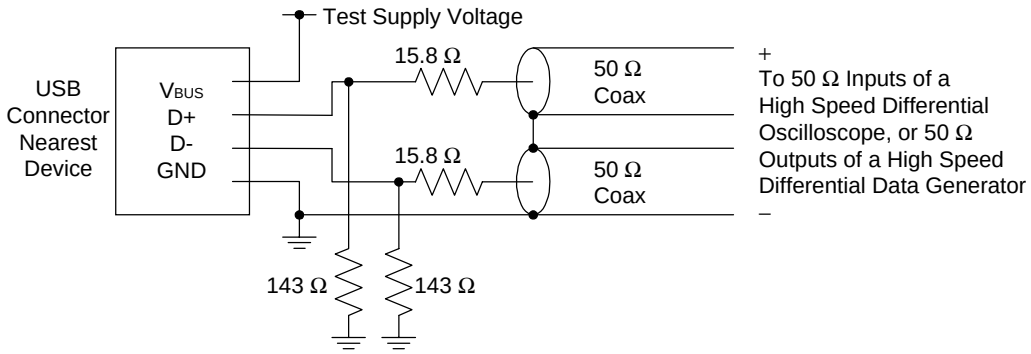



**Figure 2-5. Receiver Measurement Fixtures**



**Power Consumption**

| Parameter | Symbol | Condition | TYP. | Unit |
|---|---|---|---|---|
| Power Consumption | $P_{W-0}$ | The power consumption under the state without suspend. All the ports do not connect to any function. [Note] | | |
| | | Hub controller is operating at full-speed mode. | 44 | mA (2.5 V) |
| | | | 2.2 | mA (3.3 V) |
| | | Hub controller is operating at high-speed mode. | 84 | mA (2.5 V) |
| | | | 23 | mA (3.3 V) |
| | $P_{W-5}$ | The power consumption under the state without suspend. The number of active ports is 5. | | |
| | | Hub controller is operating at full-speed mode. | 44 | mA (2.5 V) |
| | | | 8.9 | mA (3.3 V) |
| | | Hub controller is operating at high-speed mode. | 138 | mA (2.5 V) |
| | | | 85 | mA (3.3 V) |
| | $P_{W-6}$ | The power consumption under the state without suspend. The number of active ports is 6. | | |
| | | Hub controller is operating at full-speed mode. | 44 | mA (2.5 V) |
| | | | 10 | mA (3.3 V) |
| | | Hub controller is operating at high-speed mode. | 148 | mA (2.5 V) |
| | | | 98 | mA (3.3 V) |
| | $P_{W-7}$ | The power consumption under the state without suspend. The number of active ports is 7. | | |
| | | Hub controller is operating at full-speed mode. | 44 | mA (2.5 V) |
| | | | 12 | mA (3.3 V) |
| | | Hub controller is operating at high-speed mode. | 158 | mA (2.5 V) |
| | | | 111 | mA (3.3 V) |
| | $P_{W\_S}$ | The power consumption under suspend state. The internal clock is stopped. | 0.68 | mA (2.5 V) |
| | | | 0.24 | mA (3.3 V) |

**Note** When any device is not connected to all the ports, the power consumption does not depend on the number of active ports.

**System Clock Ratings**

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | $f_{CLK}$ | X'tal | −500 ppm | 30 | +500 ppm | MHz |
| | | Oscillator block | −500 ppm | 30 | +500 ppm | MHz |
| Clock Duty cycle | $t_{DUTY}$ | | 40 | 50 | 60 | % |

**Remarks 1.** Recommended accuracy of clock frequency is ± 100 ppm.

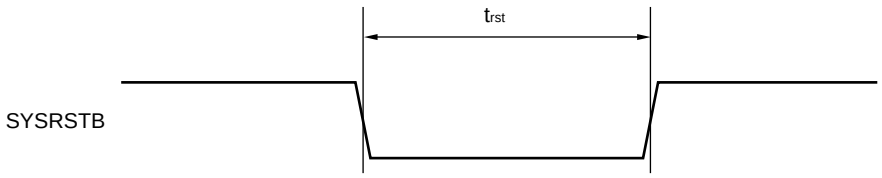
**2.** Required accuracy of X'tal or oscillator block is including initial frequency accuracy, the spread of X'tal capacitor loading, supply voltage, temperature, and aging, etc.

**AC Characteristics ($V_{DD}$ = 3.14 to 3.46 V, $T_A$ = 0 to +70°C)**

**System Reset Timing**

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Reset active time (Figure 2-6) | $t_{rst}$ | | 5 | | μs |

**Figure 2-6. System Reset Timing**



**Over-current Response Timing**

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Over-current response time from CSB low to PPB high (Figure 2-7) | $t_{OC}$ | | 500 | | 625 | μs |

**Figure 2-7. Over-current Response Timing**

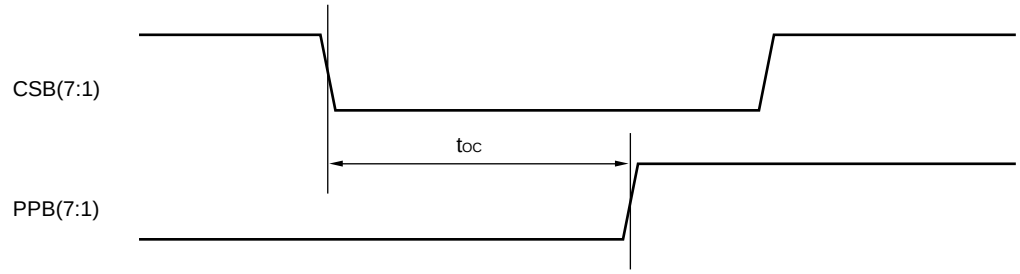
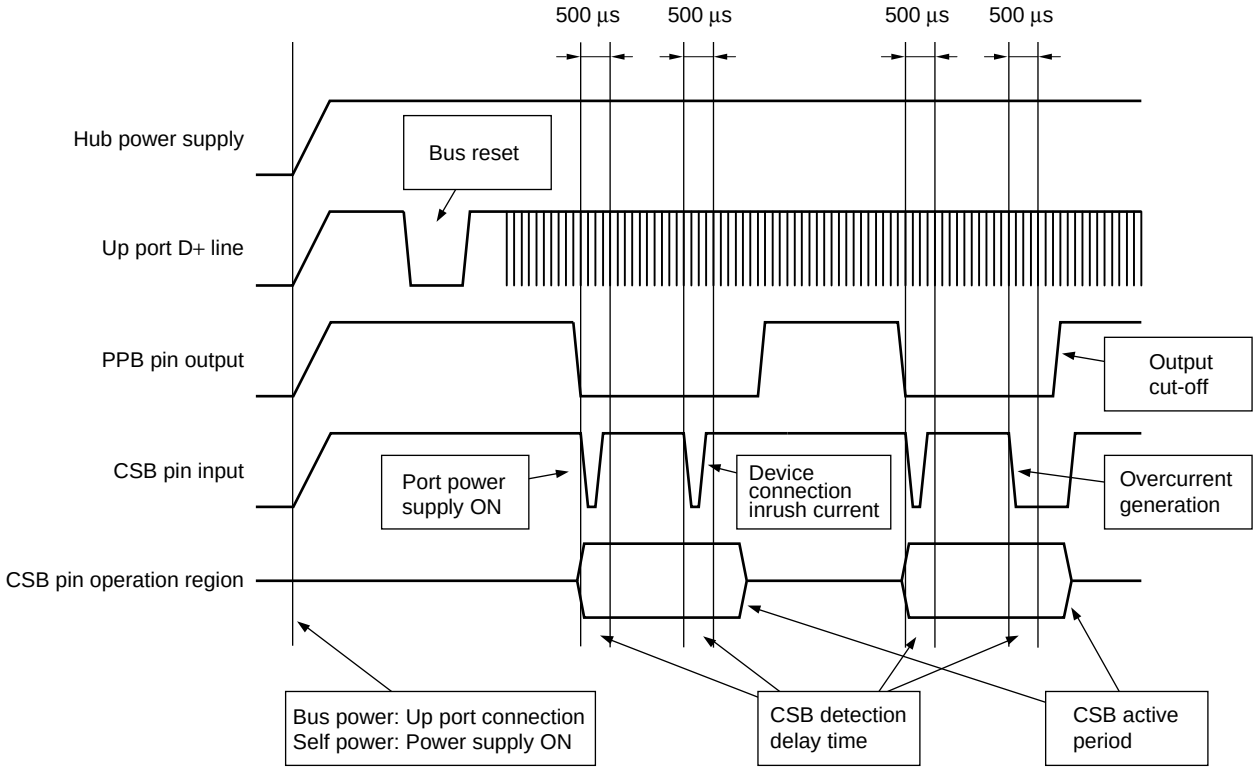



**Figure 2-8. CSB/PPB Timing**




**Remark** The active period of the CSB pin is in effect only when the PPB pin is ON.
There is a delay time of approximately 500 μs duration at the CSB pin.

**External Serial ROM Timing**

| Parameter | Symbol | Condition | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Clock frequency | $f_{SCL}$ | | | 94.6 | 100 | kHz |
| Clock pulse width low | $t_{LOW}$ | | 4700 | | | ns |
| Clock pulse width high | $t_{HIGH}$ | | 4000 | | | ns |
| Clock low to data out valid | $t_{AA}$ | | 100 | | 3500 | ns |
| Time the bus must be free before a new transmission can start | $t_{BUF}$ | | 4700 | | | ns |
| Start hold time | $t_{HD.STA}$ | | 4000 | | | ns |
| Start setup time | $t_{SU.STA}$ | | 4700 | | | ns |
| Data in hold time | $t_{HD.DTA}$ | | 0 | | | ns |
| Data in setup time | $t_{SU.DTA}$ | | 250 | | | ns |
| Stop setup time | $t_{SU.STO}$ | | 4700 | | | ns |
| Data out hold time | $t_{DH}$ | | 300 | | | ns |
| Write cycle time | $t_{WR}$ | | | | 15 | ms |

**Figure 2-9. External Serial ROM Bus Timing**

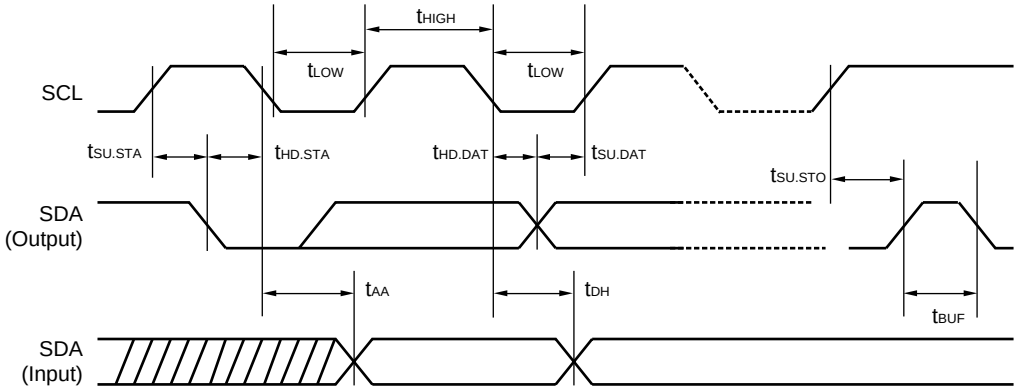
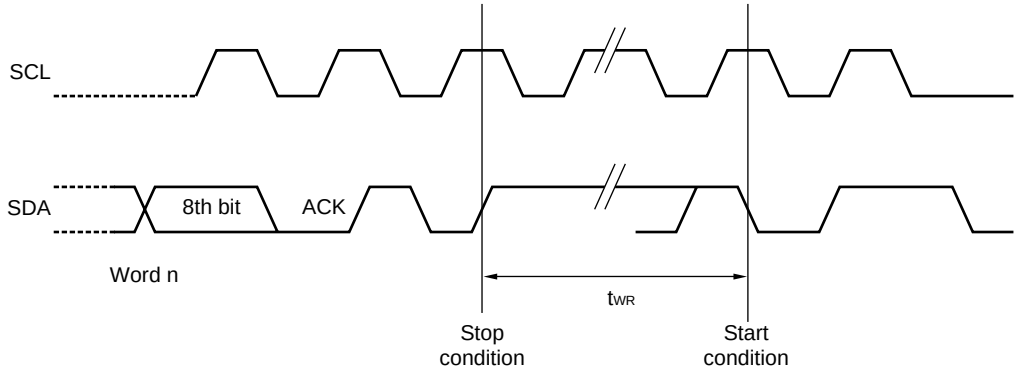



**Figure 2-10. External Serial ROM Write Cycle Timing**



**USB Interface Block**

(1/4)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| **Low-speed Electrical Characteristics** | | | | | |
| Rise time (10% to 90%) | $t_{LR}$ | $C_L$ = 200 pF to 600 pF | 75 | 300 | ns |
| Fall time (90% to 10%) | $t_{LF}$ | $C_L$ = 200 pF to 600 pF | 75 | 300 | ns |
| Differential rise and fall time matching | $t_{LRFM}$ | ($t_{LR}/t_{LF}$) Note | 80 | 125 | % |
| Low-speed data rate | $t_{LDRATHS}$ | Average bit rate | 1.49925 | 1.50075 | Mbps |
| Downstream facing port source jitter total (including frequency tolerance) (Figure 2-15): | | | | | |
| To next transition | $t_{DDJ1}$ | | −25 | +25 | ns |
| For paired transitions | $t_{DDJ2}$ | | −14 | +14 | ns |
| Downstream facing port differential receiver jitter total (including frequency tolerance) (Figure 2-17): | | | | | |
| To next transition | $t_{UJR1}$ | | −152 | +152 | ns |
| For paired transitions | $t_{UJR2}$ | | −200 | +200 | ns |
| Source SE0 interval of EOP (Figure 2-16) | $t_{LEOPT}$ | | 1.25 | 1.5 | μs |
| Receiver SE0 interval of EOP (Figure 2-16) | $t_{LEOPR}$ | | 670 | | ns |
| Width of SE0 interval during differential transition | $t_{LST}$ | | | 210 | ns |
| Hub differential data delay (Figure 2-13) | $t_{LHDD}$ | | | 300 | ns |
| Hub differential driver jitter (including cable) (Figure 2-13): | | | | | |
| Downstream facing port | | | | | |
| To next transition | $t_{LDHJ1}$ | | −45 | +45 | ns |
| For paired transitions | $t_{LDHJ2}$ | | −15 | +15 | ns |
| Upstream facing port | | | | | |
| To next transition | $t_{LUHJ1}$ | | −45 | +45 | ns |
| For paired transitions | $t_{LUHJ2}$ | | −45 | +45 | ns |
| Data bit width distortion after SOP (Figure 2-13) | $t_{LSOP}$ | | −60 | +60 | ns |
| Hub EOP delay relative to $t_{HDD}$ (Figure 2-14) | $t_{LEOPD}$ | | 0 | 200 | ns |
| Hub EOP output width skew (Figure 2-14) | $t_{LHESK}$ | | −300 | +300 | ns |
| **Full-speed Electrical Characteristics** | | | | | |
| Rise time (10% to 90%) | $t_{FR}$ | $C_L$ = 50 pF, $R_S$ = 36 Ω | 4 | 20 | ns |
| Fall time (90% to 10%) | $t_{FF}$ | $C_L$ = 50 pF, $R_S$ = 36 Ω | 4 | 20 | ns |
| Differential rise and fall time matching | $t_{FRFM}$ | ($t_{FR}/t_{FF}$) | 90 | 111.11 | % |
| Full-speed data rate | $t_{FDRATHS}$ | Average bit rate | 11.9940 | 12.0060 | Mbps |
| Frame interval | $t_{FRAME}$ | | 0.9995 | 1.0005 | ms |

**Note** Excluding the first transition from the Idle state.

(2/4)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| **Full-speed Electrical Characteristics (Continued)** | | | | | |
| Consecutive frame interval jitter | $t_{RFI}$ | No clock adjustment | | 42 | ns |
| Source jitter total (including frequency tolerance) (Figure 2-15): | | **Note** | | | |
| To next transition | $t_{DJ1}$ | | −3.5 | +3.5 | ns |
| For paired transitions | $t_{DJ2}$ | | −4.0 | +4.0 | ns |
| Source jitter for differential transition to SE0 transition (Figure 2-16) | $t_{FDEOP}$ | | −2 | +5 | ns |
| Receiver jitter (Figure 2-17): | | | | | |
| To Next Transition | $t_{JR1}$ | | −18.5 | +18.5 | ns |
| For Paired Transitions | $t_{JR2}$ | | −9 | +9 | ns |
| Source SE0 interval of EOP (Figure 2-16) | $t_{FEOPT}$ | | 160 | 175 | ns |
| Receiver SE0 interval of EOP (Figure 2-16) | $t_{FEOPR}$ | | 82 | | ns |
| Width of SE0 interval during differential transition | $t_{FST}$ | | | 14 | ns |
| Hub differential data delay (Figure 2-13) | | | | | |
| (with cable) | $t_{HDD1}$ | | | 70 | ns |
| (without cable) | $t_{HDD2}$ | | | 44 | ns |
| Hub differential driver jitter (including cable) (Figure 2-13): | | | | | |
| To next transition | $t_{HDJ1}$ | | −3 | +3 | ns |
| For paired transitions | $t_{HDJ2}$ | | −1 | +1 | ns |
| Data bit width distortion after SOP (Figure 2-13) | $t_{FSOP}$ | | −5 | +5 | ns |
| Hub EOP delay relative to $t_{HDD}$ (Figure 2-14) | $t_{FEOPD}$ | | 0 | 15 | ns |
| Hub EOP output width skew (Figure 2-14) | $t_{FHESK}$ | | −15 | +15 | ns |
| **High-speed Electrical Characteristics** | | | | | |
| Rise time (10% to 90%) | $t_{HSR}$ | | 500 | | ps |
| Fall time (90% to 10%) | $t_{HSF}$ | | 500 | | ps |
| Driver waveform | See Figure 2-11. | | | | |
| High-speed data rate | $t_{HSDRAT}$ | | 479.760 | 480.240 | Mbps |
| Microframe interval | $t_{HSFRAM}$ | | 124.9375 | 125.0625 | μs |
| Consecutive microframe interval difference | $t_{HSRFI}$ | | | 4 high-speed | Bit times |
| Data source jitter | See Figure 2-11. | | | | |
| Receiver jitter tolerance | See Figure 2-4. | | | | |
| Hub data delay (without cable) | $t_{HSHDD}$ | | | 36 high-speed+4 ns | Bit times |
| Hub data jitter | See Figure 2-4, Figure 2-11. | | | | |
| Hub delay variation range | $t_{HSHDV}$ | | | 5 high-speed | Bit times |

**Note** Excluding the first transition from the Idle state.

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| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| **Hub Event Timings** | | | | | |
| Time to detect a downstream facing port connect event (Figure 2-19):<br>Awake hub<br>Suspended hub | $t_{DCNN}$ | | <br>2.5<br>2.5 | <br>2000<br>12000 | <br>μs<br>μs |
| Time to detect a disconnect event at a hub's downstream facing port (Figure 2-18) | $t_{DDIS}$ | | 2.0 | 2.5 | μs |
| Duration of driving resume to a downstream port (only from a controlling hub) | $t_{DRSMDN}$ | | 20 | | ms |
| Time from detecting downstream resume to rebroadcast | $t_{URSM}$ | | | 1.0 | ms |
| Duration of driving reset to a downstream facing port (Figure 2-20) | $t_{DRST}$ | Only for a SetPortFeature (PORT_RESET) request | 10 | 20 | ms |
| Time to detect a long K from upstream | $t_{URLK}$ | | 2.5 | 100 | μs |
| Time to detect a long SE0 from upstream | $t_{URLSE0}$ | | 2.5 | 10000 | μs |
| Duration of repeating SE0 upstream (for low-/full-speed repeater) | $t_{URPSE0}$ | | | 23 | FS Bit times |
| Inter-packet delay (for high-speed) of packets traveling in same direction | $t_{HSIPDSD}$ | | 88 | | Bit times |
| Inter-packet delay (for high-speed) of packets traveling in opposite direction | $t_{HSIPDOD}$ | | 8 | | Bit times |
| Inter-packet delay for device/root hub response with detachable cable for high-speed | $t_{HSRSPIPD1}$ | | | 192 | Bit times |
| Time of which a Chirp J or Chirp K must be continuously detected (filtered) by hub or device during Reset handshake | $t_{FILT}$ | | 2.5 | | μs |
| Time after end of device Chirp K by which hub must start driving first Chirp K in the hub's chirp sequence | $t_{WTDCH}$ | | | 100 | μs |
| Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream by hub during reset | $t_{DCHBIT}$ | | 40 | 60 | μs |
| Time before end of reset by which a hub must end its downstream chirp sequence | $t_{DCHSE0}$ | | 100 | 500 | μs |
| Time from internal power good to device pulling D+ beyond $V_{IHZ}$ (Figure 2-20) | $t_{SIGATT}$ | | | 100 | ms |
| Debounce interval provided by USB system software after attach (Figure 2-20) | $t_{ATTDB}$ | | | 100 | ms |
| Maximum duration of suspend averaging interval | $t_{SUSAVGI}$ | | | 1 | s |
| Period of idle bus before device can initiate resume | $t_{WTRSM}$ | | 5 | | ms |
| Duration of driving resume upstream | $t_{DRSMUP}$ | | 1 | 15 | ms |

(4/4)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| **Hub Event Timings (Continued)** | | | | | |
| Resume recovery time | $t_{RSMRCY}$ | Remote-wakeup is enabled | 10 | | ms |
| Time to detect a reset from upstream for non high-speed capable devices | $t_{DETRST}$ | | 2.5 | 10000 | μs |
| Reset recovery time (Figure 2-20) | $t_{RSTRCY}$ | | | 10 | ms |
| Inter-packet delay for full-speed | $t_{IPD}$ | | 2 | | Bit times |
| Inter-packet delay for device response with detachable cable for full-speed | $t_{RSPIPD1}$ | | | 6.5 | Bit times |
| SetAddress() completion time | $t_{DSETADDR}$ | | | 50 | ms |
| Time to complete standard request with no data | $t_{DRQCMPLTND}$ | | | 50 | ms |
| Time to deliver first and subsequent (except last) data for standard request | $t_{DRETDATA1}$ | | | 500 | ms |
| Time to deliver last data for standard request | $t_{DRETDATAN}$ | | | 50 | ms |
| Time for which a suspended hub will see a continuous SE0 on upstream before beginning the high-speed detection handshake | $t_{FILTSE0}$ | | 2.5 | | μs |
| Time a hub operating in non-suspended full-speed will wait after start of SE0 on upstream before beginning the high-speed detection handshake | $t_{WTRSTFS}$ | | 2.5 | 3000 | ms |
| Time a hub operating in high-speed will wait after start of SE0 on upstream before reverting to full-speed | $t_{WTREV}$ | | 3.0 | 3.125 | ms |
| Time a hub will wait after reverting to full-speed before sampling the bus state on upstream and beginning the high-speed will wait after start of SE0 on upstream before reverting to full-speed | $t_{WTRSTHS}$ | | 100 | 875 | ms |
| Minimum duration of a Chirp K on upstream from a hub within the reset protocol | $t_{UCH}$ | | 1.0 | | ms |
| Time after start of SE0 on upstream by which a hub will complete its Chirp K within the reset protocol | $t_{UCHEND}$ | | | 7.0 | ms |
| Time between detection of downstream chip and entering high-speed state | $t_{WTHS}$ | | | 500 | μs |
| Time after end of upstream Chirp at which hub reverts to full-speed default state if no downstream Chirp is detected | $t_{WTFS}$ | | 1.0 | 2.5 | ms |

**Figure 2-11. Transmit Waveform for Transceiver at DP/DM**

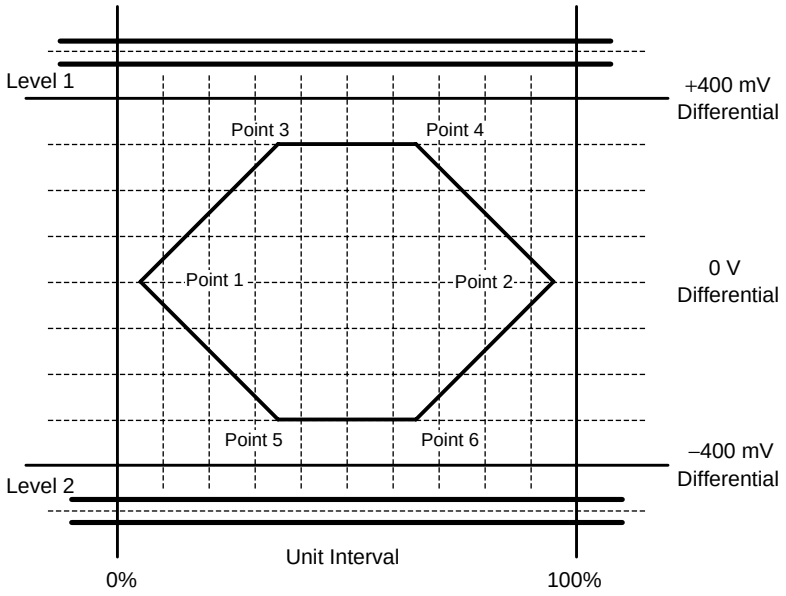
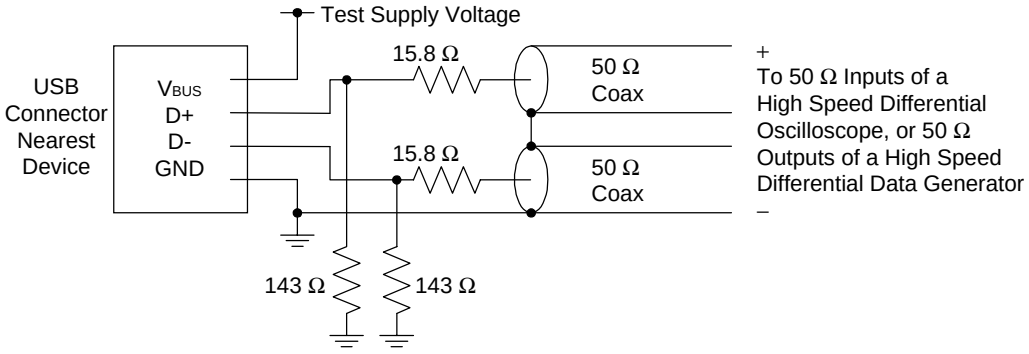
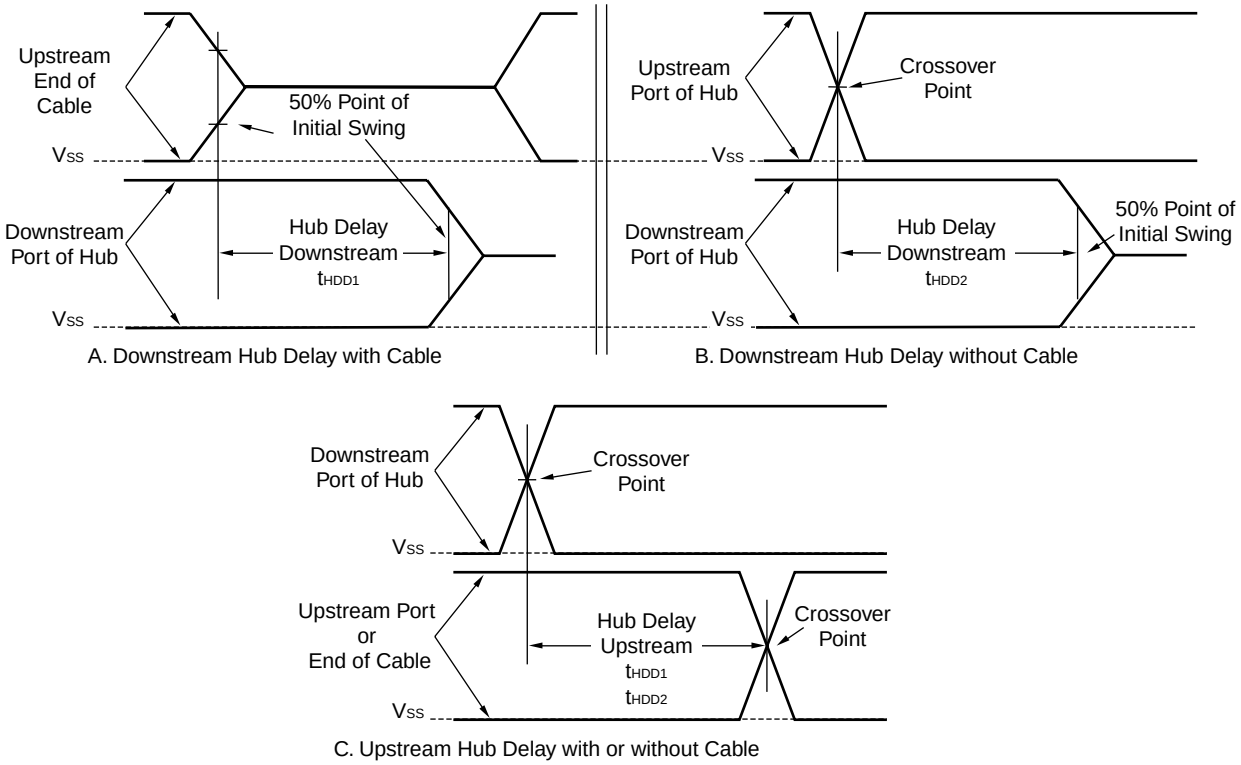



**Figure 2-12. Transmitter Measurement Fixtures**



**Timing Diagram**

**Figure 2-13. Hub Differential Delay, Differential Jitter, and SOP Distortion**




Hub Differential Jitter:

$t_{HDJ1} = t_{HDDx}(J) - t_{HDDx}(K)$ or $t_{HDDx}(K) - t_{HDDx}(J)$ Consecutive Transitions

$t_{HDJ2} = t_{HDDx}(J) - t_{HDDx}(J)$ or $t_{HDDx}(K) - t_{HDDx}(K)$ Paired Transitions

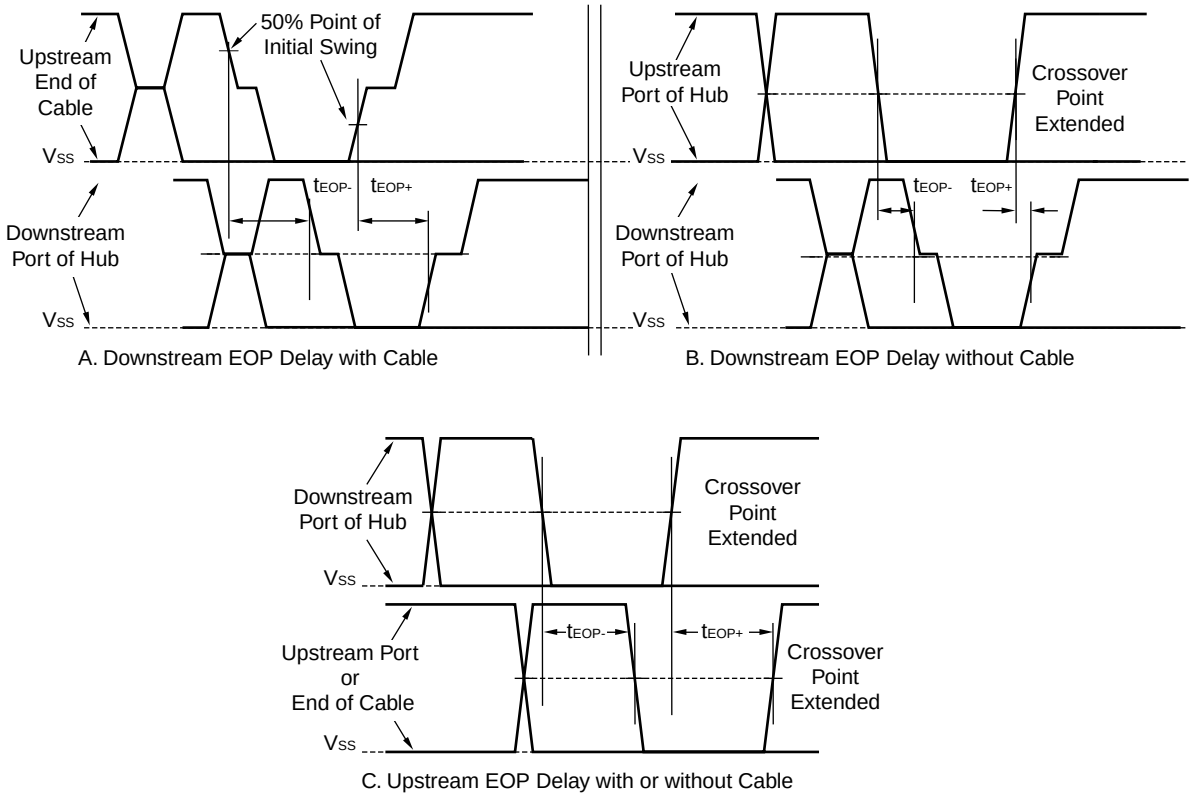
Bit after SOP Width Distortion (same as data jitter for SOP and next J transition):

$t_{FSOP} = t_{HDDx}(\text{next J}) - t_{HDDx}(\text{SOP})$

Low-speed timings are determined in the same way for:

$t_{LHDD}$, $t_{LDHJ1}$, $t_{LDJH2}$, $t_{LUHJ1}$, $t_{LUJH2}$, and $t_{LSOP}$

**Figure 2-14. Hub EOP Delay and EOP Skew**




EOP Delay:

$t_{FEOPD} = t_{EOPy} - t_{HDDx}$

($t_{EOPy}$ means that this equation applies to $t_{EOP-}$ and $t_{EOP+}$)

EOP Skew:

$t_{FHESK} = t_{EOP+} - t_{EOP-}$

Low-speed timings are determined in the same way for:

$t_{LEOPD}$ and $t_{LHESK}$

**Figure 2-15. USB Differential Data Jitter for Low-/full-speed**

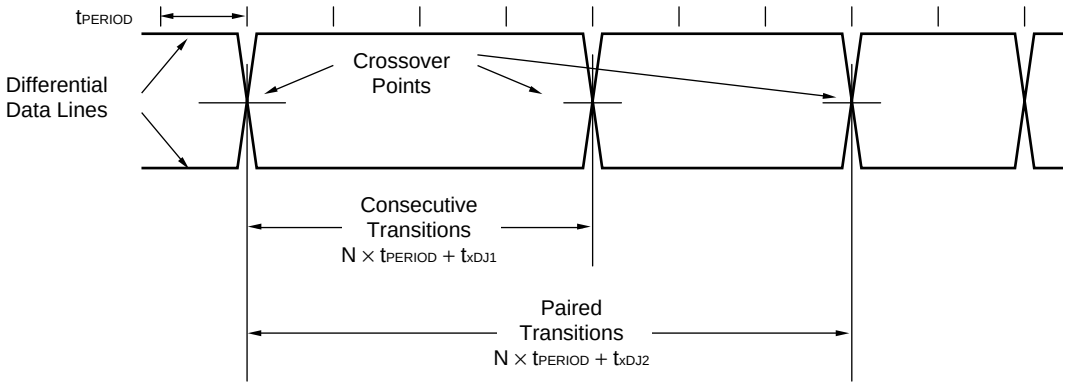



**Figure 2-16. USB Differential-to-EOP Transition Skew and EOP Width for Low-/full-speed**

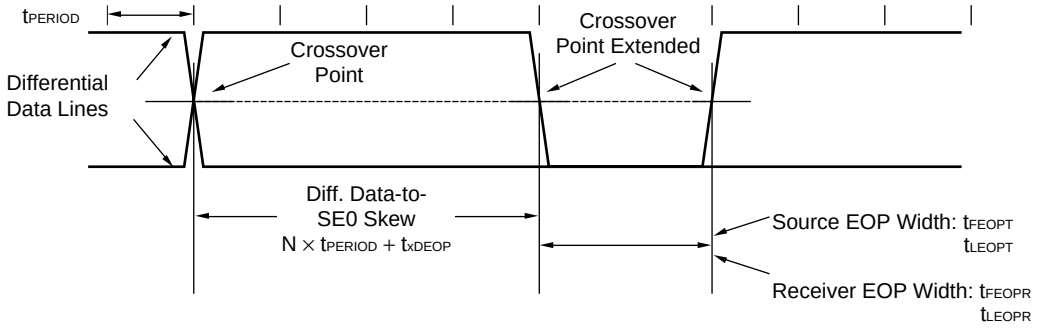



**Figure 2-17. USB Receiver Jitter Tolerance for Low-/full-speed**

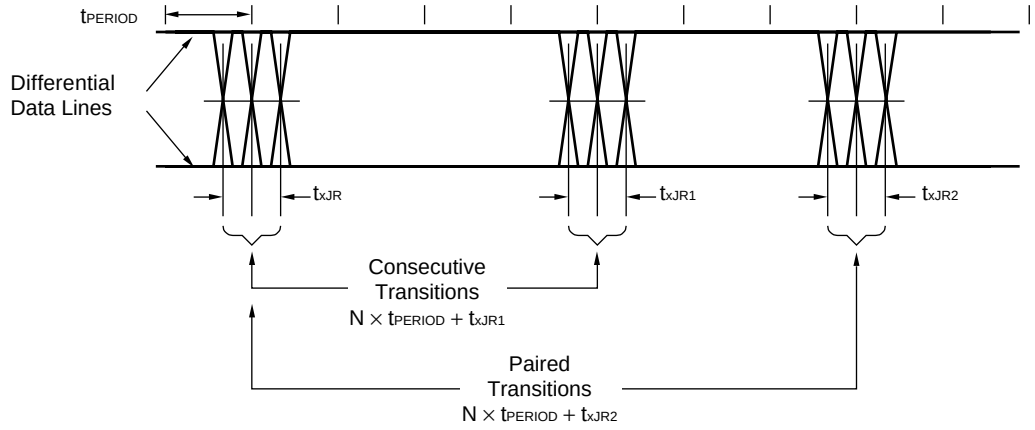


**Figure 2-18. Low-/full-speed Disconnect Detection**

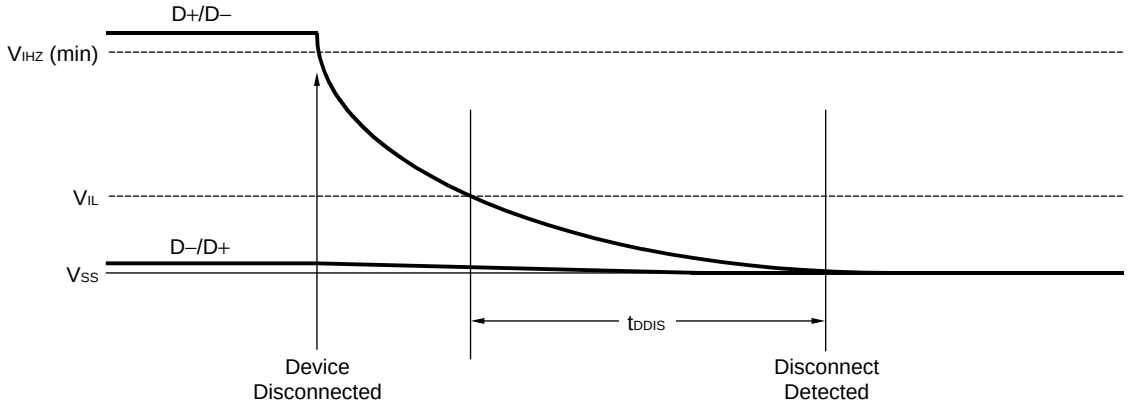



**Figure 2-19. Full-/high-speed Device Connect Detection**

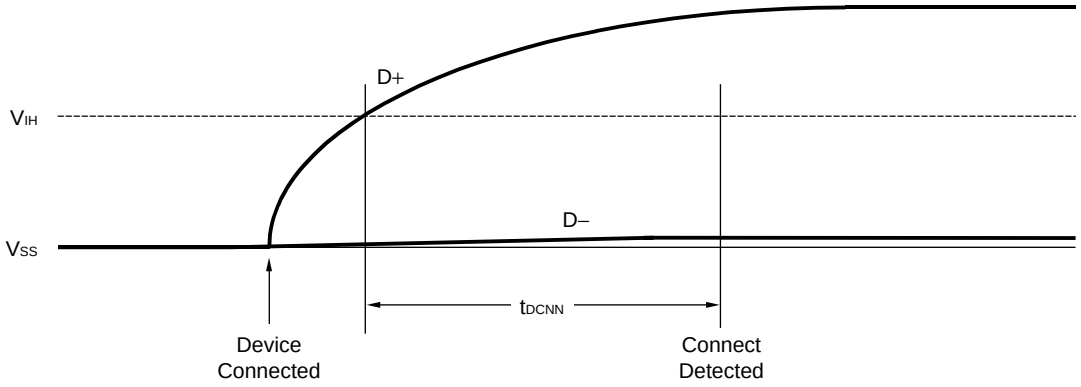
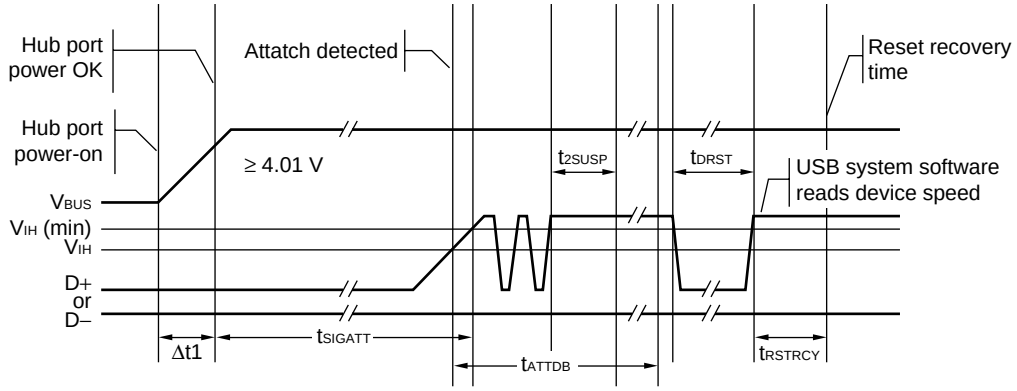
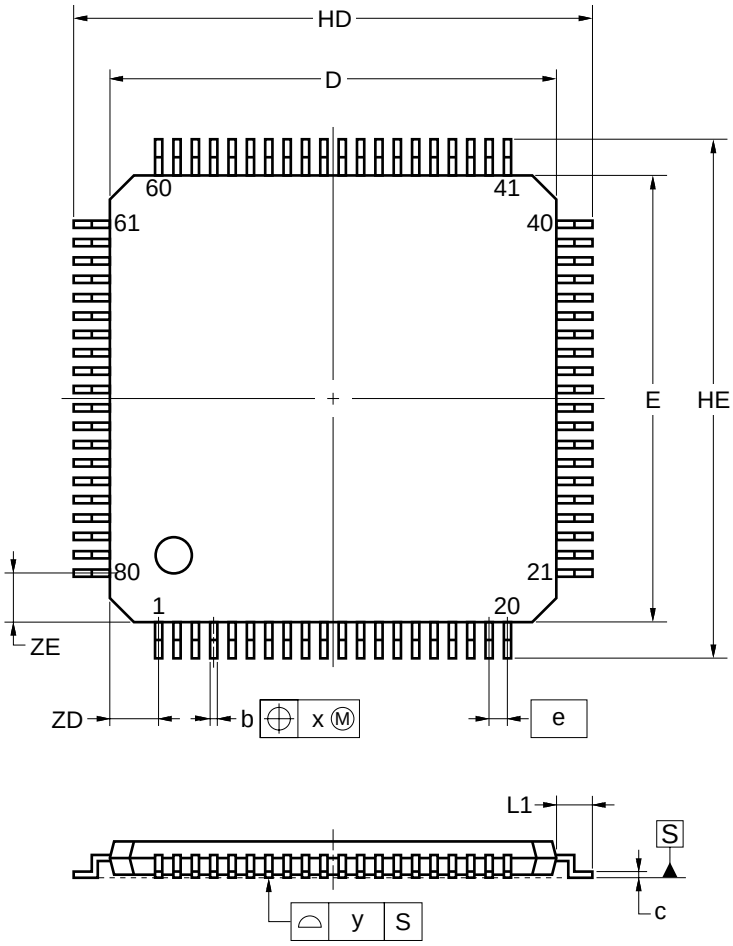



**Figure 2-20. Power-on and Connection Events Timing**

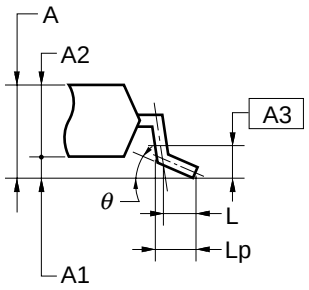


## 3. PACKAGE DRAWING

## 80-PIN PLASTIC TQFP (FINE PITCH) (12x12)




detail of lead end




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 12.00±0.20 |
| E | 12.00±0.20 |
| A2 | 1.00 |
| HD | 14.00±0.20 |
| HE | 14.00±0.20 |
| A | 1.10±0.10 |
| A1 | 0.10±0.05 |
| A3 | 0.25 |
| Lp | 0.60±0.15 |
| b | 0.22±0.05 |
| c | $0.17^{+0.03}_{-0.07}$ |
| θ | $3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 1.25 |
| ZE | 1.25 |
| L | 0.50 |
| L1 | 1.00±0.20 |

**K80GK-50-9EU**

**NOTE**
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

## 4. RECOMMENDED SOLDERING CONDITIONS

The μPD720113 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

**μPD720113GK-9EU: 80-pin plastic TQFP (Fine pitch) (12 × 12)**

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher),<br>Count: Three times or less<br>Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 hours) | IR35-103-3 |
| Partial heating | Pin temperature: 300°C max., Time: 3 seconds max. (per pin row) | – |

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

★ **μPD720113GK-9EU-A: 80-pin plastic TQFP (Fine pitch) (12 × 12) Lead-free product**

| Soldering Method | Soldering Conditions | Symbol |
|---|---|---|
| Infrared reflow | Package peak temperature: 245°C, Time: 60 seconds max. (at 220°C or higher),<br>Count: Three times or less<br>Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours) | IR45-107-3 |
| Partial heating | Pin temperature: 300°C max., Time: 3 seconds max. (per pin row) | – |

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

**[MEMO]**

## NOTES FOR CMOS DEVICES

**① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN).

**② HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

**③ PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

**④ STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

**⑤ POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

**⑥ INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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