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MITSUBISHI(MICMPTR/MIPRC)



# M5L8257P-5

## PROGRAMMABLE DMA CONTROLLER

T-52-33-19

## DESCRIPTION

The M5L8257P-5 is a programmable 4-channel direct memory access (DMA) controller. It is produced using the N-channel silicon-gate ED-MOS process and is specifically designed to simplify data transfer at high speeds for microcomputer systems.

The LSI operates on a single 5V power supply.

## FEATURES

- Single 5V supply voltage
- TTL compatible interface
- Priority DMA request logic
- Channel-masking function
- Terminal count and Modulo 128 outputs
- 4-channel DMA controller
- Compatible with MELPS85 devices

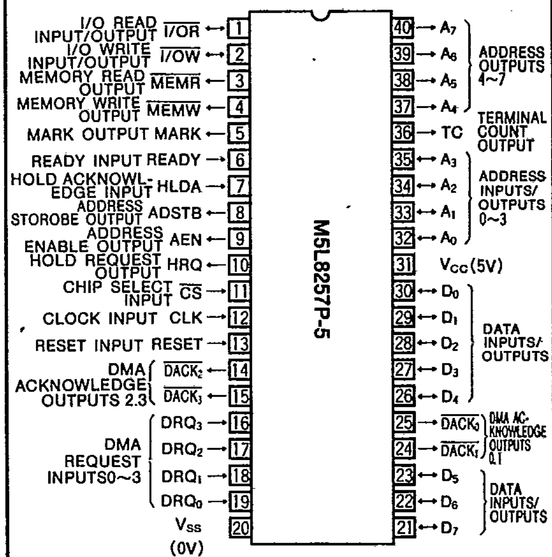
## APPLICATION

DMA control of peripheral equipment such as floppy disks and CRT terminals that require high-speed data transfer.

## FUNCTION

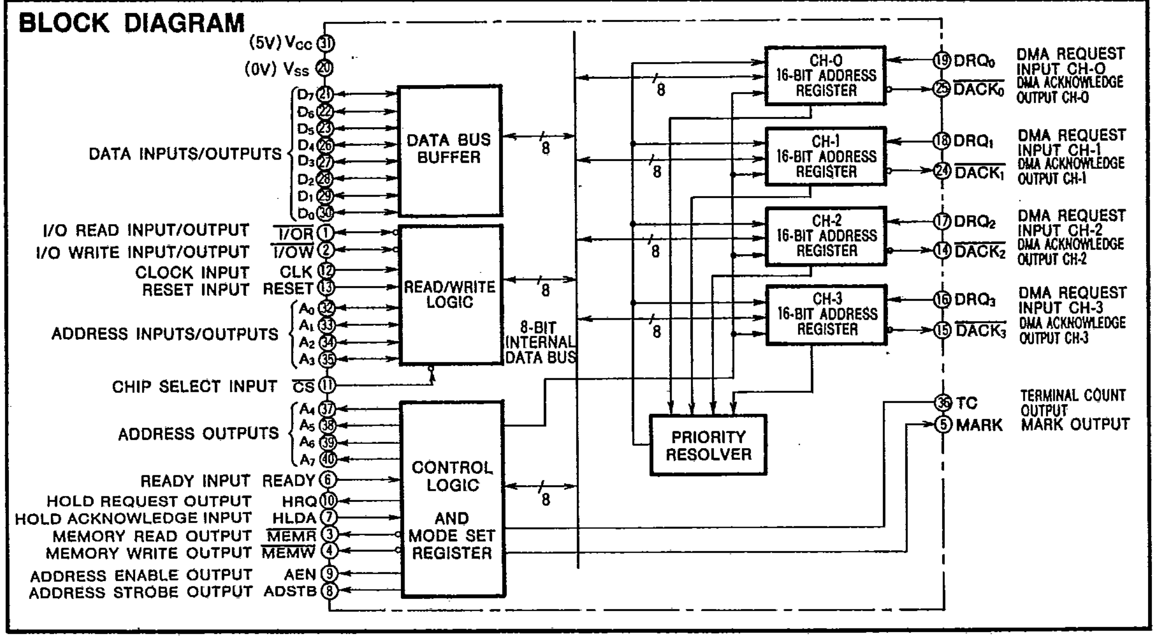
The M5L8257P-5 controller is used in combination with the M5L8212P 8-bit input/output port in 8-bit microcomputer systems. It consists of a channel section to acknowledge DMA requests, control logic to exchange commands and data with the CPU, read/write logic, and registers to hold transfer addresses and count the number of bytes to be transferred. When a DMA request is made to an unmasked channel from the peripherals after setting of the transfer mode, transfer-start address and the number of transferred bytes for the registers, the M5L8257P-5 issues a priority request for the use of the bus to the CPU. On receiving an HLDA signal from the CPU, it sends a DMA acknowledge signal to the channel with the highest priority, starting DMA operation. During DMA operation, the contents of the high-order 8 bits of the transfer memory address are transmitted to the M5L8212P address-latch device through pins $D_0 \sim D_7$. The contents of the low-order 8 bits are transmitted through pins $A_0 \sim A_7$. After address transmission, DMA transfer can be started by dispatching read and write signals to the memories and peripherals.

## PIN CONFIGURATION (TOP VIEW)




Outline 40P4

## BLOCK DIAGRAM



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## OPERATION

### I/O Read Input/Output ($\overline{I/OR}$)

When the M5L8257P-5 is in slave-mode operation, this threestate, bidirectional pin serves for inputting and reads the upper/lower bytes of the 8-bit status register or 16-bit DMA address register and the high/low order bytes of the terminal counter.

In the master mode, the pin gives control output and is used to obtain data from a peripheral equipment during the DMA write cycle.

### I/O Write Input/Output ($\overline{I/OW}$)

This pin is also of the three-state bidirectional type. When the M5L8257P-5 is in slave-mode operation, it serves for inputting and loads the contents of the data bus on the 8-bit status register and the upper/lower bytes of the 16-bit terminal counter or 16-bit DMA address register.

### Memory Read Output ($\overline{MEMR}$)

This active-low three-state output is used to read data from the addressed memory location during DMA read cycles.

### Memory Write Output ($\overline{MEMW}$)

This active-low three-state output is used to write data into the addressed memory location during DMA write cycles.

### Mark Output (MARK)

This signal notifies that the DMA transfer cycle for each channel is the 128th cycle since the previous MARK output.

### Ready Input (READY)

This asynchronous input is used to extend the memory read and write cycles in the M5L8257P-5 with wait states if the selected memory requires longer access time.

### Hold Acknowledge Input (HLDA)

This input from the CPU indicates that the system bus is controlled by the M5L8257P-5.

### Address Strobe Output (ADSTB)

This output strobes the most significant byte of the memory address into the M5L8212P (8-bit input/output port) through the data bus.

### Address Enable Output (AEN)

This signal is used to disable the system data bus and system control bus by means of the bus enable pin on the system controller. It may also be used to inhibit non-DMA devices from responding during DMA cycles.

### Hold Request Output (HRQ)

This output requests control of the system bus. HRQ will normally be applied to the HOLD input on the CPU.

### Chip-Select Input ($\overline{CS}$)

This pin is active on a low-level. It enable the $\overline{I/OR}$ and $\overline{I/OW}$ signals output from the CPU, when the M5L8257P-5 is in slave-mode operation.

In the master mode, it is disabled to prevent the chip from selecting itself while performing the DMA function.

### Clock Input (CLK)

This pin generates internal timing for the M5L8257P-5 and is connected to the $\phi$ (TTL) output of the system clock.

### Reset Input (RESET)

This asynchronous input clears some registers and control lines inside the M5L8257P-5.

### DMA Acknowledge Outputs ($\overline{DACK0}$~$\overline{DACK3}$)

These active-low outputs indicate that the peripheral equipment connected to the channel in question can execute the DMA cycle.

### DMA Request Inputs (DRQ0~DRQ3)

These independent, asynchronous channel-request inputs are used to secure use of the DMA cycle for the peripherals.

### Data-Bus Buffer

This three-state, bidirectional, 8-bit buffer interfaces the M5L8257P-5 to the CPU for data transfer. During a DMA cycle the upper 8 bits of the DMA address are output to the M5L8212P latch device through this buffer.

### Address Inputs/Outputs ($A_0$~$A_3$)

The four bits of these input/output pins are bidirectional. When the M5L8257P-5 is in slave-mode operation, serve to input and address the internal registers. In the case of master operation, they output the low-order 4 bits of the 16-bit memory address.

### Terminal Count Output (TC)

When the terminal count registers became (3FFF)H, terminal count signal is out. And this signal notifies that the present DMA cycle is the last cycle for this data block.

### Address Inputs/Outputs ($A_4$~$A_7$)

These four address lines are three-state outputs which constitute bits 4 through 7 of the memory address generated by the M5L8257P-5 during all DMA cycles.



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**Register Initialization**

Two 16-bit registers are provided for each of the 4 channels.

**DMA Address register**

| 15 | | | | | | | | | | | | | | | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $A_{15}$ | $A_{14}$ | $A_{13}$ | $A_{12}$ | $A_{11}$ | $A_{10}$ | $A_9$ | $A_8$ | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ |

DMA TRANSFER STARTING ADDRESS

**Terminal count register**

| 15 | 14 | 13 | | | | | | | | | | | | | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Rd | Wr | $C_{13}$ | $C_{12}$ | $C_{11}$ | $C_{10}$ | $C_9$ | $C_8$ | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ |

DMA MODE — NUMBER OF TRANSFERRED BYTES−1

The DMA transfer starting address, number of transferred bytes, and DMA mode are written for each channel in 2 steps using the 8-bit data bus. The lower-order and upper-order bytes are automatically indicated by the first-last flip-flop for the writing and reading in 2 continuous steps.

The DMA mode (read, write, or verify) is indicated by the upper 2 bits of the terminal count register. The read mode refers to the operation of peripheral devices reading data out of memory. The write mode refers to data from peripheral devices being written into memory. The verify mode sends neither the read nor the write signals and performs a date check at the peripheral device.

In addition to the above-mentioned registers, there is a mode set register and a status register.

**Mode set register (write only)**

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| AL | TCS | EW | RP | EN3 | EN2 | EN1 | EN0 |

ADDED FUNCTION SETTING BITS — CHANNEL ENABLE BITS

**Status Register (read only)**

| 7 | | | | | | | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | UP | TC3 | TC2 | TC1 | TC0 |

The upper-order 4 bits of the mode set register are used to select the added function, as described in 5-66. The lower-order 4 bits are mask bits for each channel. When set to 1, DMA requests are allowed. When the reset signal is input, all bits of the mode set and status registers are reset and DMA is inhibited for all channels. Therefore, to execute DMA operations, registers must first be initialized. An example of such an initialization is shown below.

MODESET:

```
MVI  A, ADDL
OUT  00#:  Channel 0 lower-order address
MVI  A, ADDH
OUT  00#:  Channel 0 upper-order address
MVI  A, TCL
OUT  01#:  Channel 0 terminal count lower-order
MVI  A, TCH
OUT  01#:  Channel 0 terminal count upper-order
MVI  A, XX
OUT  08#:  Mode set resister
```

As can be seen from the above example, until the contents of the address register and terminal count register become valid, the enable bit of the mode set register must not be set. This prevents memory contents from being destroyed by improper DRQ signals from peripheral devices.

## DMA OPERATION DESCRIPTION

When a DMA request signal is received at the DRQ pin from a peripheral device after register initialization for a channel that is not masked, the M5L8257P-5 outputs a hold request signal to the CPU to begin DMA operation ($S_1$).

The CPU, upon receipt of the HRQ signal, outputs the HLDA signal which reserves capture of the bus after it has executed the present instruction to place this system in the hold state.

When the M5L8257P-5 receives the HLDA signal, an internal priority determining circuit selects the channel with the highest priority for the beginning of data transfer ($S_0$).

Upon the next $S_1$ state, the address signal is sent. The lower-order 8 bits and upper-order 8 bits are sent by means of the $A_0 \sim A_7$ and $D_0 \sim D_7$ pins respectively, latched into the M5L8212P and output at pins $A_8 \sim A_{15}$. Simultaneous with this, the AEN signal is output to prohibit the selection of a device not capable of DMA.

In the $S_2$ state, the read, extended write, and DACK signals are output and data transferred from memory or a peripheral device appears on the data bus.

In the $S_3$ state, the write signal required to write data from the bus is output. At this time if the remaining number of bytes to be transferred from the presently selected channel has reached 0, the terminal count (TC) signal is output. Simultaneously with this, after each 128-byte data transfer a mark signal is output as required. In addition, in this state the READY pin is sampled and, if low-level, the wait state ($S_W$) is entered. This is used to perform DMA with slow access memory devices. In the verify mode, READY input is ignored.



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In the $S_4$ state, the DRQ and HLDA pins are sampled at the end of a transferred byte as the address signal, control signals, and $\overline{\text{DACK}}$ signal are held to determine if transfer will continue.
As described above, transfer of 1 byte requires a minimum of 4 states for execution. For example, if a 2MHz clock input is used, the maximum transfer rate is 500k byte/s.

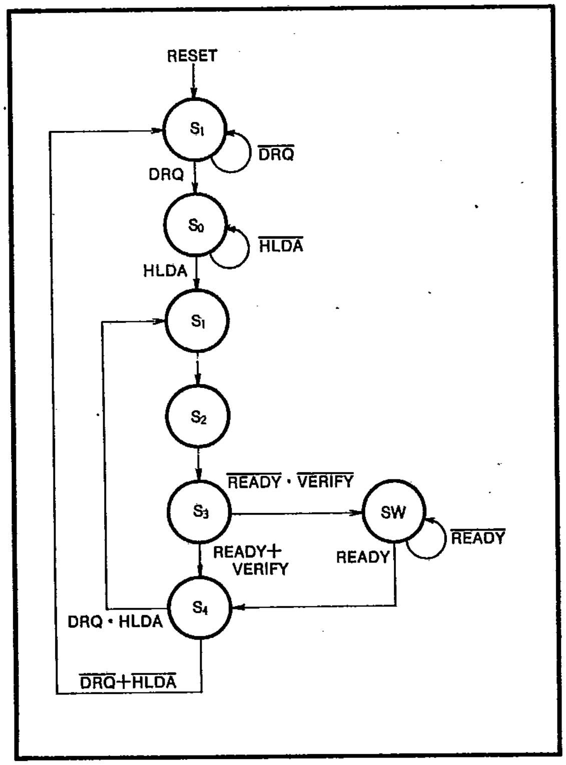


**Fig. 1** DMA Operation state transition diagram

## MEMORY MAPPED I/O

When using memory mapped I/O, it is neccessary to change the connections for the control signals.

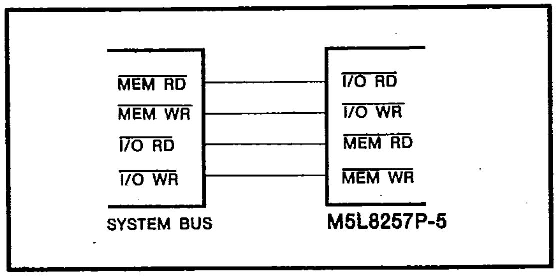


**Fig. 2** Memory mapped I/O

Also, the read mode and write mode specifications for setting the mode of the terminal count are reversed.



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## INTERNAL REGISTERS OF THE M5L8257P-5

| | Upper | | | | | | | | Lower | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | $D_7$ | $D_6$ | $D_5$ | $D_4$ | $D_3$ | $D_2$ | $D_1$ | $D_0$ | |
| channel-0 | $A_{15}$ | $A_{14}$ | $A_{13}$ | $A_{12}$ | $A_{11}$ | $A_{10}$ | $A_9$ | $A_8$ | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | DMA address |
| | Rd | Wr | $C_{13}$ | $C_{12}$ | $C_{11}$ | $C_{10}$ | $C_9$ | $C_8$ | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ | terminal count |
| channel-1 | $A_{15}$ | $A_{14}$ | $A_{13}$ | $A_{12}$ | $A_{11}$ | $A_{10}$ | $A_9$ | $A_8$ | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | DMA address |
| | Rd | Wr | $C_{13}$ | $C_{12}$ | $C_{11}$ | $C_{10}$ | $C_9$ | $C_8$ | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ | terminal count |
| channel-2 | $A_{15}$ | $A_{14}$ | $A_{13}$ | $A_{12}$ | $A_{11}$ | $A_{10}$ | $A_9$ | $A_8$ | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | DMA address |
| | Rd | Wr | $C_{13}$ | $C_{12}$ | $C_{11}$ | $C_{10}$ | $C_9$ | $C_8$ | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ | terminal count |
| channel-3 | $A_{15}$ | $A_{14}$ | $A_{13}$ | $A_{12}$ | $A_{11}$ | $A_{10}$ | $A_9$ | $A_8$ | $A_7$ | $A_6$ | $A_5$ | $A_4$ | $A_3$ | $A_2$ | $A_1$ | $A_0$ | DMA address |
| | Rd | Wr | $C_{13}$ | $C_{12}$ | $C_{11}$ | $C_{10}$ | $C_9$ | $C_8$ | $C_7$ | $C_6$ | $C_5$ | $C_4$ | $C_3$ | $C_2$ | $C_1$ | $C_0$ | terminal count |
| | | | | | | | | | AL | TCS | EW | RP | EN3 | EN2 | EN1 | EN0 | Mode setting (for write only) |
| | | | | | | | | | 0 | 0 | 0 | UP | TC3 | TC2 | TC1 | TC0 | Status (for read only) |

$A_0 \sim A_{15}$ : Address of the memories for which DMA will be carried out from now on. In initialization, DMA start addresses must be written.

$C_0 \sim C_{13}$ : Terminal counts-in this IC (the number of remaining transfer bytes minus 1) The address is decremented for each DMA transfer of one byte, and when the transfer is finished, becomes $(3FFF)_H$. If additional DRQ signals are input, the address continues to be decremented.

Rd, Wr : Used for DMA-mode setting by the following convention:

| Rd | Wr | Mode to be set |
|---|---|---|
| 0 | 0 | DMA verify |
| 0 | 1 | DMA write |
| 1 | 0 | DMA read |
| 1 | 1 | Prohibition |

AL : Automatic load mode. When this bit has been set, contents of the channel 3 register are written, as are on the channel 2 register when channel 2 DMA transfer comes to an end. This mode allows quick, automatic chaining operations without intervention of the software.

EW : Extended write signal mode. When this bit has been set, write signals can be transmitted in advance to memories and peripheral equipment requiring long access time.

TCS : Terminal count stop. When a DMA transfer process is complete, with terminal-count output, the channel-enable mask of that channel is reset, prohibiting subsequent DMA cycles.

RP : Rotating priority mode. The setting of this mode allows the priority order to be rotated by each byte transfer. The setting priority is fixed with the channel 0 as highest, followed by channel 1, 2 and 3 in descending order.

| Channel used for the present data transfer | | CH-0 | CH-1 | CH-2 | CH-3 |
|---|---|---|---|---|---|
| Priority list for the next cycle | 1 | CH-1 | CH-2 | CH-3 | CH-0 |
| | 2 | CH-2 | CH-3 | CH-0 | CH-1 |
| | 3 | CH-3 | CH-0 | CH-1 | CH-2 |
| | 4 | CH-0 | CH-1 | CH-2 | CH-3 |

EN0~EN3 : Channel-enable bit. This mask prohibits or allows the DMA request. When the reset signal is applied, all channels are disabled.

UP : Update flag. This is set when register contents are transferred in an automatic load mode from channel 3 to channel 2.

TC0~TC3 : Terminal-count status flags. At the time of terminal-count output, the flag corresponding to the channel is set: The flag is, set by reading the status register, annd is unaffected by the TCS bits.



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## REGISTER ADDRESS

| Address Input | | | | F/L | Register |
|---|---|---|---|---|---|
| $A_3$ | $A_2$ | $A_1$ | $A_0$ | | |
| 0 | 0 | 0 | 0 | 0 | channel 0 DMA address Low-order |
| 0 | 0 | 0 | 0 | 1 | channel 0 DMA address High-order |
| 0 | 0 | 0 | 1 | 0 | channel 0 terminal count Low-order |
| 0 | 0 | 0 | 1 | 1 | channel 0 terminal count High-order |
| 0 | 0 | 1 | 0 | 0 | channel 1 DMA address Low-order |
| 0 | 0 | 1 | 0 | 1 | channel 1 DMA address High-order |
| 0 | 0 | 1 | 1 | 0 | channel 1 terminal count Low-order |
| 0 | 0 | 1 | 1 | 1 | channel 1 terminal count High-order |
| 0 | 1 | 0 | 0 | 0 | channel 2 DMA address Low-order |
| 0 | 1 | 0 | 0 | 1 | channel 2 DMA address High-order |
| 0 | 1 | 0 | 1 | 0 | channel 2 terminal count Low-order |
| 0 | 1 | 0 | 1 | 1 | channel 2 terminal count High-order |
| 0 | 1 | 1 | 0 | 0 | channel 3 DMA address Low-order |
| 0 | 1 | 1 | 0 | 1 | channel 3 DMA address High-order |
| 0 | 1 | 1 | 1 | 0 | channel 3 terminal count Low-order |
| 0 | 1 | 1 | 1 | 1 | channel 3 terminal count High-order |
| 1 | 0 | 0 | 0 | — | Mode Setting (for Write Only) |
| 1 | 0 | 0 | 0 | — | Status (for Read Only) |

F/L : First/last flip-flop. This is toggled when register-write or read operations for each channel are finished, and specifies whether the next write or read operaton is to be for the upper bytes or the lower bytes. This means that write and read operations for each register must be carried out for a set of lower and higher bytes.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Power-supply voltage | With respect to $V_{SS}$ | −0.5~7 | V |
| $V_I$ | Input voltage | | −0.5~7 | V |
| $V_O$ | Output voltage | | −0.5~7 | V |
| $P_d$ | Power dissipation (max.) | $T_a$=25℃ | 1000 | mW |
| $T_{opr}$ | Operating free-air temperature range | | −20~75 | ℃ |
| $T_{stg}$ | Storage temperature range | | −65~150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS ($T_a$=−20~75℃, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Power-supply voltage | 4.75 | 5 | 5.25 | V |
| $V_{SS}$ | Power-supply voltage (GND) | | 0 | | V |



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## ELECTRICAL CHARACTERISTICS ($T_a$=−20~75℃, $V_{CC}$=5V±5%, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits Min | Limits Typ | Limits Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 2.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage | | −0.5 | | 0.8 | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$=1.6mA | | | 0.45 | V |
| $V_{OH1}$ | High-level output voltage for AB, DB and AEN | $I_{OH}$=−150μA | 2.4 | | | V |
| $V_{OH2}$ | High-level output voltage for HRQ | $I_{OH}$=−80μA | 3.3 | | | V |
| $V_{OH3}$ | High-level output voltage for others | | 2.4 | | | V |
| $I_{CC}$ | Supply current from $V_{CC}$ | | | | 120 | mA |
| $I_I$ | Input current | $V_I$=0V, $V_{CC}$ | −10 | | 10 | μA |
| $I_{OZ}$ | Off-state output current | $V_O$=0V~$V_{CC}$ | −10 | | 10 | μA |
| $C_I$ | Input terminal capacitance | $T_a$=25℃, $V_{CC}$=$V_{SS}$ Pins other than that under measurement are set to 0V, $f_C$=1MHz | | | 10 | pF |
| $C_{I/O}$ | Input/output terminal capacitance | | | | 20 | pF |

## TIMING REQUIREMENTS ($T_a$=−20~75℃, $V_{CC}$=5V±5%, $V_{SS}$=0V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits Min | Limits Typ | Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{w(R)}$ | Read pulse width | | 250 | | | ns |
| $t_{su(A-R)}$ $t_{su(CS-R)}$ | Address or $\overline{CS}$ setup time before read | | 0 | | | ns |
| $t_{h(R-A)}$ $t_{h(R-CS)}$ | Address or $\overline{CS}$ hold time after read | | 0 | | | ns |
| $t_{w(W)}$ | White pulse width | | 200 | | | ns |
| $t_{su(A-W)}$ | Address setup time before write | | 20 | | | ns |
| $t_{h(W-A)}$ | Address hold time after write | | 0 | | | ns |
| $t_{su(DQ-W)}$ | Data setup time before write | | 200 | | | ns |
| $t_{h(W-DQ)}$ | Data hold time after write | | 0 | | | ns |
| $t_{w(RST)}$ | Reset pulse width | | 300 | | | ns |
| $t_{su(Vcc-RST)}$ | Supply voltage setup time before reset | | 500 | | | ns |
| $t_r$ | Input signal rise time | | | | 20 | ns |
| $t_f$ | Input signal fall time | | | | 20 | ns |
| $t_{su(RST-W)}$ | Reset setup time before write | | 2 | | | $t_{C(\phi)}$ |
| $t_{C(\phi)}$ | Clock cycle time | | 0.32 | | 4 | μs |
| $t_{w(\phi)}$ | Clock pulse width high-level | | 80 | | $0.8t_{C(\phi)}$ | ns |
| $t_{su(DRQ-\phi)}$ | DRQ setup time before clock | | 70 | | | ns |
| $t_{h(HLDA-DRQ)}$ | DRQ hold time after HLDA | | 0 | | | ns |
| $t_{su(HLDA-\phi)}$ | HLDA setup time before clock | | 100 | | | ns |
| $t_{su(RDY-\phi)}$ | Ready setup time before clock | | 30 | | | ns |
| $t_{h(\phi-RDY)}$ | Ready hold time after clock | | 20 | | | ns |

## SLAVE MODE SWITCHING CHARACTERISTICS ($T_a$=−20~75℃, $V_{CC}$=5V±5%, $V_{SS}$=0V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits Min | Limits Typ | Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PZV(R-DQ)}$ | Output data enable time after read | $C_L$=150pF | 0 | | 200 | ns |
| $t_{PVZ(R-DQ)}$ | Output data disable time after read | | 20 | | 100 | ns |



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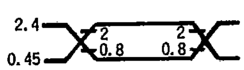
## DMA MODE SWITCHING CHARACTERISTICS ($T_a=-20\sim75°C$, $V_{CC}=5V\pm5\%$, $V_{SS}=0V$, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits Min | Limits Typ | Limits Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PLH(\phi-HRQ)}$<br>$t_{PHL(\phi-HRQ)}$ | Propagation time from clock to HRQ (Note1) | | | | 160 | ns |
| $t_{PLH(\phi-HRQ)}$<br>$t_{PHL(\phi-HRQ)}$ | Propagation time from clock to HRQ (Note3) | | | | 250 | ns |
| $t_{PLH(\phi-AEN)}$ | Propagation time from clock to AEN (Note1) | | | | 300 | ns |
| $t_{PHL(\phi-AEN)}$ | Propagation time from clock to AEN (Note1) | | | | 200 | ns |
| $t_{PZV(AEN-A)}$ | Propagation time from AEN to address active (Note4) | | 20 | | | ns |
| $t_{PZV(\phi-A)}$ | Propagation time from clock to address active (Note2) | | | | 250 | ns |
| $t_{PVZ(\phi-A)}$ | Propagation time from clock to address floating (Note2) | | | | 150 | ns |
| $t_{PLH(\phi-A)}$ | Address setup time after clock (Note2) | | | | 250 | ns |
| $t_{h(\phi-A)}$ | Address hold time after clock (Note2) | | $t_{PLH(\phi-A)}-50$ | | | ns |
| $t_{h(R-A)}$ | Address hold time after read (Note4) | | 60 | | | ns |
| $t_{h(W-A)}$ | Address hold time after write (Note4) | | 300 | | | ns |
| $t_{PZV(\phi-DQ)}$ | Propagation time from clock to data active | | | | 300 | ns |
| $t_{PVZ(\phi-DQ)}$ | Propagation time from clock to data floating (Note2) | | $t_{PHL(\phi-ASTB)}+20$ | | 170 | ns |
| $t_{PHL(A-ASTB)}$ | Propagation time from address to address strobe (Note2) | | 100 | | | ns |
| $t_{h(ASTB-A)}$ | Propagation time from address strobe to address hold (Note4) | | 50 | | | ns |
| $t_{PLH(\phi-ASTB)}$ | Propagation time from clock to address strobe (Note1) | | | | 200 | ns |
| $t_{PHL(\phi-ASTB)}$ | Propagation time from clock to address strobe (Note1) | | | | 140 | ns |
| $t_{W(ASTB)}$ | Address strobe pulse width (Note4) | | $t_{C(\phi)}-100$ | | | ns |
| $t_{PHL(AS-R)}$<br>$t_{PHL(AS-WE)}$ | Propagation time from address strobe to read or extended write (Note4) | | 70 | | | ns |
| $t_{h(DQ-R)}$<br>$t_{h(DQ-WE)}$ | Read or extended write hold time after data (Note4) | | 20 | | | ns |
| $t_{PLH(\phi-DACK)}$<br>$t_{PHL(\phi-TC/MARK)}$<br>$t_{PLH(\phi-TC/MARK)}$ | Propagation time from clock to $\overline{DACK}$ or TC/MARK (Note1, 5) | | | | 250 | ns |
| $t_{PHL(\phi-R)}$<br>$t_{PHL(\phi-W)}$<br>$t_{PHL(\phi-WE)}$ | Propagation time from clock to read, write or extended write (Note2, 6) | | | | 200 | ns |
| $t_{PLH(\phi-R)}$<br>$t_{PLH(\phi-W)}$ | Propagation time from clock to read or write (Note2, 7) | | | | 200 | ns |
| $t_{PZV(\phi-R)}$<br>$t_{PZV(\phi-W)}$ | Propagation time from clock to read active or write active (Note2) | | | | 300 | ns |
| $t_{PVZ(\phi-R)}$<br>$t_{PVZ(\phi-W)}$ | Propagation time from clock to read floating or write floating (Note2) | | | | 150 | ns |
| $t_{W(R)}$ | Read pulse width (Note4) | | $2t_{C(\phi)}+t_{W(\phi)}-50$ | | | ns |
| $t_{W(W)}$ | Write pulse width (Note4) | | $t_{C(\phi)}-50$ | | | ns |
| $t_{W(WE)}$ | Extended write pulse width (Note4) | | $2t_{C(\phi)}-50$ | | | ns |

Note 1 : Load=1TTL
2 : Load=1TTL+50pF
3 : Load=1TTL+($R_L$=3.3kΩ), $V_{OH}$=3.3V
4 : Tracking specification

Note 5 : $\Delta t_{PLH(\phi-DACK)}$<50ns, $\Delta t_{PHL(\phi-TC/MARK)}$<50ns, $\Delta t_{PLH(\phi-TC/MARK)}$<50ns
6 : $\Delta t_{PHL(\phi-R)}$<50ns, $\Delta t_{PHL(\phi-W)}$<50ns, $\Delta t_{PHL(\phi-WE)}$<50ns
7 : $\Delta t_{PLH(\phi-R)}$<50ns, $\Delta t_{PLH(\phi-W)}$<50ns
8 : A, C Testing waveform

| | | |
|---|---|---|
| Input pulse level | | 0.45~2.4V |
| Input pulse rise time | | 20ns |
| Input pulse fall time | | 20ns |
| Reference level | input | $V_{IH}$=2V, $V_{IL}$=0.8V |
| | output | $V_{OH}$=2V, $V_{OL}$=0.8V |



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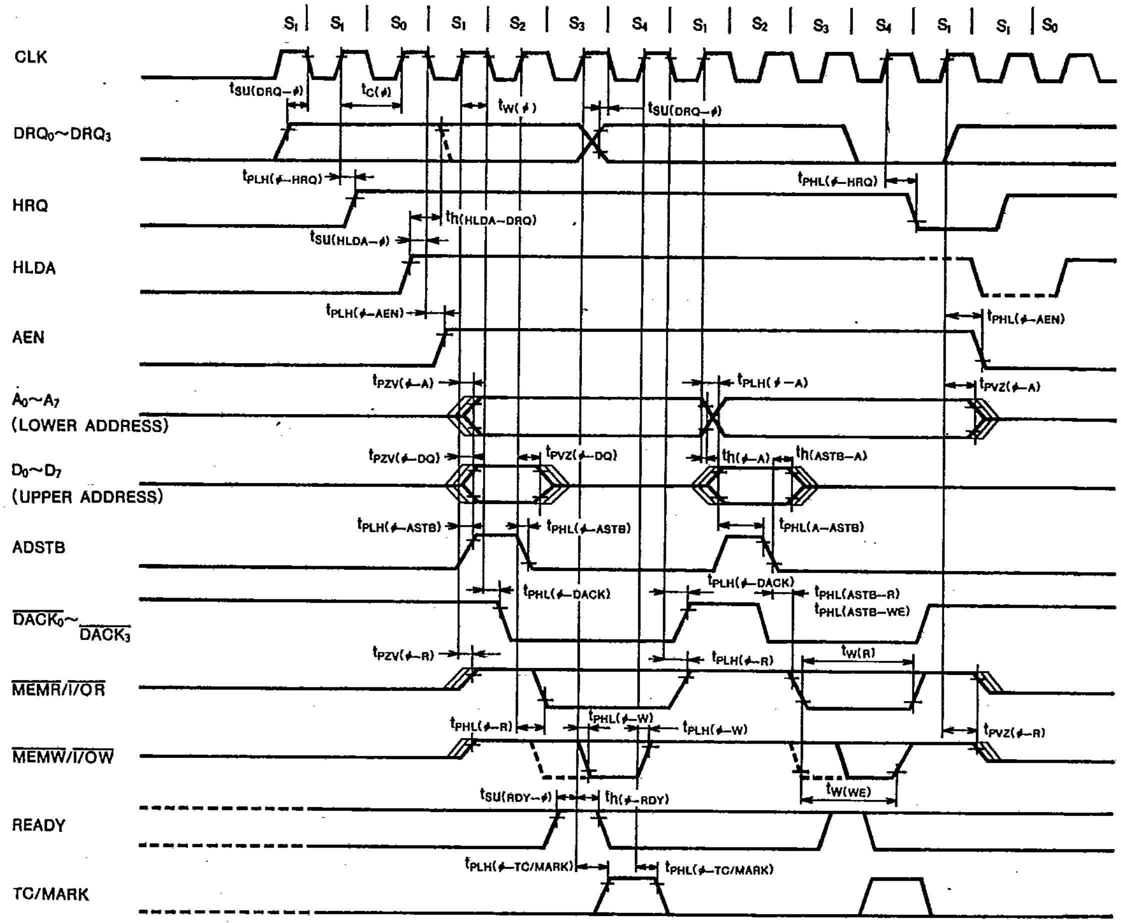
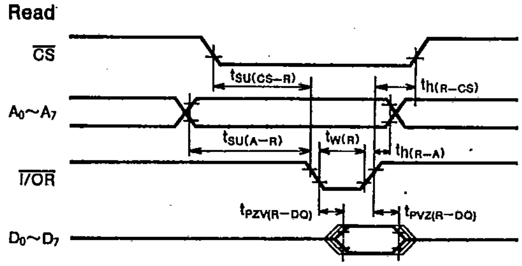
## TIMING DIAGRAMS

### DMA Mode

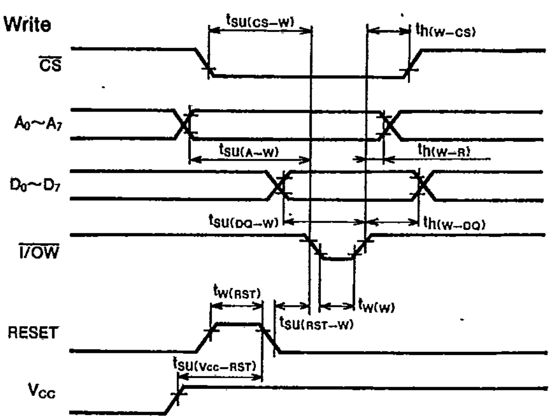



### Slave Mode

Read




Write






MITSUBISHI ELECTRIC

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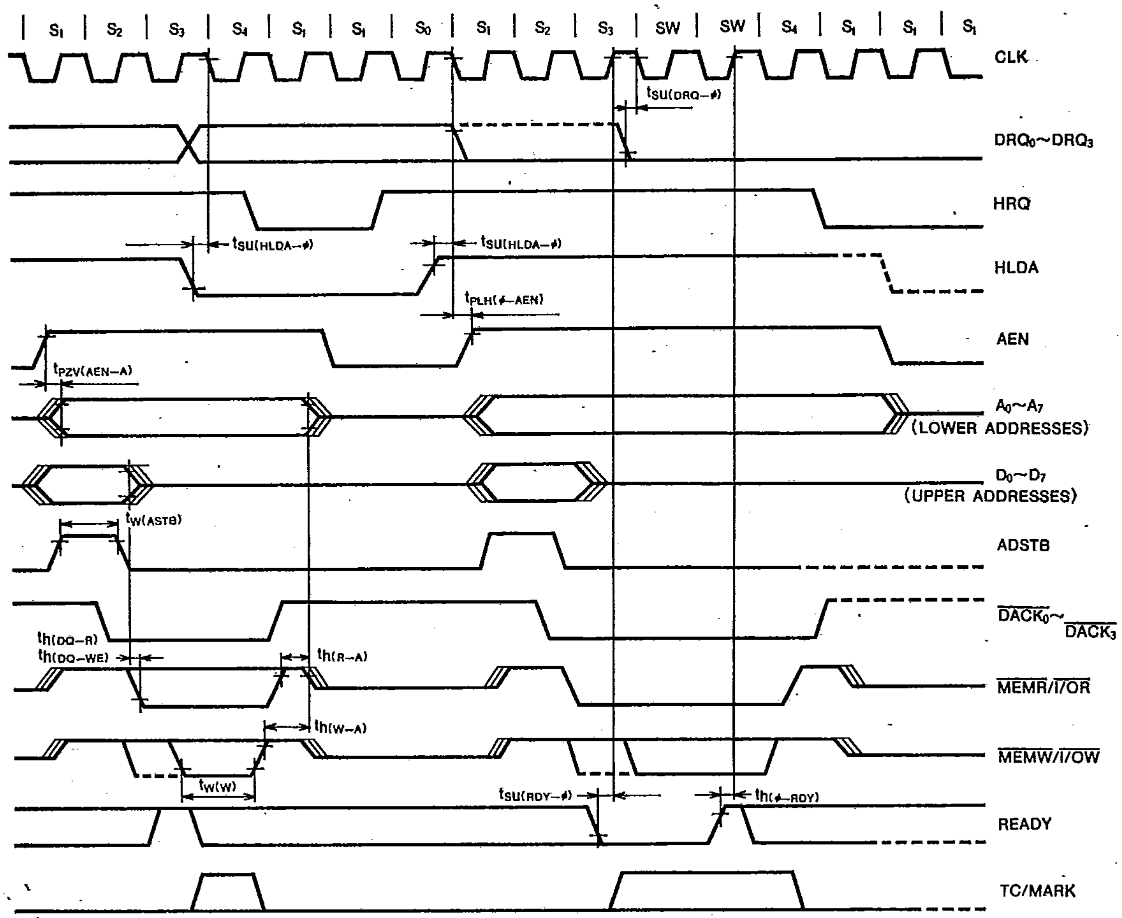
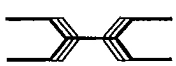



Note 9 :



The center line indicates a floating (high-impedance) state.



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